

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

TQ DELTA, LLC,)	
)	
Plaintiff,)	
)	
v.)	C.A. No. 13-cv-1835-RGA
)	
2WIRE, INC.,)	
)	
Defendant.)	
)	

**DEFENDANT 2WIRE, INC.'S OPPOSITION TO PLAINTIFF TQ DELTA, LLC'S
MOTION FOR SUMMARY JUDGMENT OF NO INVALIDITY OF FAMILY 3 PATENT
CLAIMS UNDER 35 U.S.C. § 103**

Dated: March 8, 2019

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TQ Delta Exhibit 2013
COMMScope, INC. v. TQ DELTA LLC
IPR2023-00064

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I. INTRODUCTION

TQ Delta, LLC's ("TQ Delta") motion for summary judgment of no invalidity under 35 U.S.C. § 103 of claim 1 of U.S. Patent No. 8,276,048, claim 5 of U.S. Patent No. 7,836,381, claim 13 of U.S. Patent No. 7,844,882, and claim 19 of U.S. Patent No. 8,495,473 should be denied in its entirety.

For the invalidity grounds that form the basis of 2Wire's pending Motion for Summary Judgment of Invalidity (D.I. 773, 774), and that also are addressed in TQ Delta's motion, 2Wire, not TQ Delta, is entitled to summary judgment. For these two combinations, TQ Delta does not argue that either combination – (1) U.S. Patent No. 7,296,208 to Mazzoni (hereafter, "Mazzoni") with ITU-T standard G.993.1, and (2) Mazzoni with ITU-T contribution LB-031 –VDSL2 – Constraining Interleaver Complexity (hereafter, "LB-031") – lacks disclosure of any limitation of the claims. Nor could it, given that TQ Delta's own expert, Dr. Cooklev, admitted at his deposition that Mazzoni discloses the "shared memory" that TQ Delta claims is the centerpiece of the Family 3 patents. TQ Delta argues only that one of ordinary skill in the art ("POSITA") would not be motivated to combine the references, or that together, the references somehow would be incompatible or inoperable. TQ Delta's argument, however, ignores that a POSITA is assumed to apply his or her ordinary skill and creativity in combining the references, so TQ Delta's only argument fails.

For those invalidity grounds not addressed in 2Wire's pending invalidity motion, summary judgment should be denied because there are genuine disputes of material fact with respect to whether those combinations render obvious the asserted claims. 2Wire has adduced evidence from its expert, Dr. Krista Jacobsen, that those combinations of references render obvious the asserted claims. TQ Delta argues that Dr. Jacobsen made admissions at her deposition that conflict with her opinions regarding these obviousness combinations. TQ Delta

is wrong, but even if Dr. Jacobsen's deposition testimony could be construed as presented by TQ Delta that still would not justify summary judgment for TQ Delta. Any purported inconsistency between Dr. Jacobsen's deposition testimony and her opinions goes to the credibility of her opinions, which cannot be resolved on summary judgment.

II. NATURE AND STAGE OF THE PROCEEDING

TQ Delta filed this patent infringement lawsuit against 2Wire on November 4, 2013, asserting infringement of twenty-four patents across six patent families. *See* D.I. 1, D.I. 6 (Complaint, and First Amended Complaint, respectively). The Court split the case into separate trials on individual patent families. *See* D.I. 280 (Third Amended Scheduling Order). Family 3 is currently at issue, and TQ Delta asserts claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent.

Fact and expert discovery is now closed. A pretrial conference for 2Wire's trial on Family 3 is set for May 10, 2019, and trial is set for May 20, 2019. *See* D.I. 513 (Final Scheduling Order).

III. FACTUAL BACKGROUND

A. The Family 3 Patents.

The claims of the Family 3 patents are directed to methods, systems, and apparatuses for allocating shared memory between transmitter and receiver latency paths. *See* D.I. 767 (Declaration of Anna Targowska), Ex. 3 ('882 patent) at 4:1–3.¹ The transmitter and receiver latency paths can share an interleaver/deinterleaver memory, which can be allocated to the transmitter's interleaver and to the receiver's deinterleaver. *Id.* at 4:5–9, 9:18–21.

The Family 3 patents provide an example in which a first transceiver sends a message to

¹ The Family 3 patents share a common specification and have the same drawings. References to the specification herein will be to the '882 patent.

a second transceiver indicating the number of supported transmitter and receiver latency paths, the maximum interleaver memory for each of the latency paths, and the maximum total or shared memory for all of the latency paths. *Id.* at 8:9–19. The first transceiver then selects settings (i.e., Reed-Solomon parameter values N and R, and the interleaver depth, D) for each of the latency paths. *Id.* at 8:21–22.

B. The Asserted Claims.

Claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent recite as follows.²

'048 Patent, Claim 1	'381 Patent, Claim 5	'882 Patent, Claim 13
1. A system that allocates shared memory comprising: a transceiver that is capable of:	5. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:	13. A system that allocates shared memory comprising: a transceiver that performs:
transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;	transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;	transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;
determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;	determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;	determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
allocating a first number of bytes of the shared memory to the interleaver to interleave	allocating, in the transceiver, a first number of bytes of the shared memory to the	allocating a first number of bytes of the shared memory to the deinterleaver to

² The claim language set forth here reflects the edits set forth in the Certificates of Correction for claim 5 of the '381 patent and claim 13 of the '882 patent. In a separate motion, 2Wire challenges the validity of those certificates of correction.

the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;	deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;	deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;
allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and	allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and	allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and
interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.	deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.	deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

Claim 19 of the '473 patent recites:

19. An apparatus comprising:

a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path, the multicarrier communications transceiver being associated with a memory,

wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

IV. LEGAL STANDARD

Summary judgment is appropriate only where the record, read in the light most favorable to the non-moving party, indicates that “there is no genuine issue as to any material fact and . . . the moving party is entitled to a judgment as a matter of law.” Fed. R. Civ. P. 56(c). To avoid summary judgment, the non-moving party need only present sufficient evidence upon which a jury might reasonably return a verdict in its favor. *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248-49 (1986); *C.R. Bard, Inc. v. Advanced Cardiovascular Sys., Inc.*, 911 F.2d 670, 672-73 (Fed. Cir. 1990). In determining whether a genuine issue of material fact exists, the district court views the evidence in the light most favorable to the nonmoving party and resolves all doubts in its favor. *Id.* “Credibility determinations, the weighing of evidence, and the drawing of legitimate inferences from the facts are jury functions, not those of a judge, whether he is ruling on a motion for summary judgment or for a directed verdict.” *Anderson*, 477 U.S. at 255.

An accused infringer must establish by clear and convincing evidence that the claims at issue are invalid, whether by anticipation or obviousness. *See Transclean Corp. v. Bridgewood Servs., Inc.*, 290 F.3d 1364, 1370 (Fed. Cir. 2002). A patent is obvious “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

V. ARGUMENT

For those combinations of references where 2Wire moved for summary judgment of invalidity – LB-031 and Mazzoni for all asserted claims, and G.993.1 and Mazzoni for claim 19 of the ’473 patent – 2Wire has established that it is entitled to summary judgment of invalidity.

See generally D.I. 774. For the remaining combinations of references, genuine disputes of material fact preclude summary judgment for TQ Delta.

A. 2Wire, Not TQ Delta, Is Entitled to Summary Judgment On The Obviousness Combinations Addressed In Both 2Wire’s Own Summary Judgment Motion, And TQ Delta’s Motion.

1. LB-031 in Combination With Mazzoni.

As established in 2Wire’s Family 3 Invalidity Motion, LB-031 in combination with Mazzoni discloses each limitation of the Asserted Family 3 Claims. *See generally* D.I. 774 at 11-20; D.I. 775 (Opening Declaration of Dr. Krista Jacobsen), ¶¶ 356-520. 2Wire also has established that a POSITA would have been motivated to combine the teachings of Mazzoni with the teachings of LB-031. *See generally* D.I. 774 at 19-20; D.I. 775 (Jacobsen Opening Decl.), ¶¶ 521-531. To avoid unnecessary repetition, 2Wire refers back to its motion for summary judgment.

TQ Delta does not argue that the combination of LB-031 and Mazzoni fails to disclose any limitation of the Asserted Family 3 Claims. TQ Delta cannot possibly argue that Mazzoni does not disclose “shared memory” because its own expert, Dr. Cooklev, admits that Mazzoni discloses that limitation. Walsh Decl.,³ Ex. B (Cooklev Dep. Tr.); 147:1-8. TQ Delta also cannot argue that LB-031 does not disclose the messaging scheme recited in the claims, given its similarity with the messaging scheme specified by the VDSL2 standard that forms the basis for TQ Delta’s infringement position in this case. Instead, TQ Delta takes issue only with the evidence regarding whether the references can be combined. In its motion, 2Wire demonstrates that they can be.

³ “Walsh Decl.” as used herein refers to the Omnibus Declaration of Rachel M. Walsh in Support of 2Wire, Inc.’s Oppositions to TQ Delta, LLC’s Family 3 Motions, filed concurrently herewith.

TQ Delta first argues that “modifying LB-031 by adding shared memory would disrupt the operation of LB-031 rendering it inoperable.” D.I. 778 at 11. TQ Delta contends that LB-031 and Mazzoni cannot be combined because the resulting transceiver would have a memory deficiency, which TQ Delta refers to colloquially as the “Mazzoni problem.” *See* D.I. 778 at 12. This argument assumes that a POSITA would make no modification to either Mazzoni or LB-031, which is contrary to the law. A proper obviousness analysis “take[s] account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418. Such an argument, which requires assuming that “a person of ordinary skill in the art can only perform combinations of a puzzle element A with a perfectly fitting puzzle element B,” is contrary to the law. *ClassCo, Inc. v. Apple, Inc.*, 838 F.3d 1214, 1219 (Fed. Cir. 2016) (upholding Board’s finding of motivation to combine).⁴

Taking into account such inferences and creative steps, Dr. Jacobsen opined that a POSITA would be motivated to combine the messaging scheme of LB-031 with Mazzoni. D.I. 775 (Jacobsen Opening Decl.), ¶¶ 521-531. A POSITA would have recognized the shortcomings Mazzoni and LB-031, for example, that Mazzoni described a table of pre-defined services and settings, and that the teachings of LB-031, in particular, the exchange of interleaver/deinterleaver capabilities during initialization, would enable Mazzoni’s transceivers to partition its shared memory between the interleaver and deinterleaver without requiring all possible services and settings to be pre-defined. *See id.* at ¶ 526. As Dr. Jacobsen opined, this would result in a more

⁴ The cases that TQ Delta cites regarding motivation to combine are distinguishable. *See* D.I. 778 at 3-4. Unlike the expert in *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1351-52 (Fed. Cir. 2014), 2Wire and Dr. Jacobsen have explained how a POSITA would be motivated to combine Mazzoni and LB-031, including how such a combination could be implemented. Unlike the combinations at issue in *MediaTek, Inc. v. Freescale Semiconductor, Inc.*, No. 11-CV-5341, 2014 WL 2854705, at *2 (N.D. Cal. June 20, 2014), crediting the skill of the POSITA, 2Wire has shown that the combination of the references would be operable.

flexible transceiver. *Id.* 2Wire has presented **unrebutted** evidence that a POSITA would understand how to make these modifications, such as adjusting the amount of memory in a transceiver (thereby circumventing TQ Delta’s purported “Mazzoni problem”). Jacobsen Opp. Decl.,⁵ ¶ 700; *see also id.* at ¶ 129.

Finally, TQ Delta misstates Dr. Jacobsen’s testimony in an attempt to show that she somehow admitted that Mazzoni in combination with LB-031 would be inoperable or incompatible. *See* D.I. 778 at 12-14. At her deposition, Dr. Jacobsen specifically and clearly disagreed with TQ Delta’s counsel’s characterization of LB-031. She testified as follows (Walsh Decl., Ex. C (Jacobsen Dep. Tr.), 509:22-510:5 (emphasis added):

Q. ... So – so to get to that point, it sounds like you agree that, if you literally used only messaging that said, “This is my maximum downstream, and this is my maximum upstream,” and then the devices could use up to that amount, it sounds like you don’t challenge Dr. Cooklev’s argument that that wouldn’t work with Mazzoni; correct?

A. I don’t think that would work, **but I also don’t think that that’s what LB-031 suggests doing.**

Elsewhere, Dr. Jacobsen agrees with the uncontroversial statement that Mazzoni allocates memory between interleaving and deinterleaving, depending on the service used, and that it would have sufficient memory to support the services programmed into its tables. *See id.* at (Jacobsen Dep. Tr.) 495:22-496:24. TQ Delta also states, without providing citation or explanation, that the benefit of Mazzoni would not be realized, or that memory would not be shared if memory were added. These conclusory statements do not create a genuine dispute of material fact, nor do they affect 2Wire’s showing that Mazzoni and LB-031 disclose each limitation of the Asserted Family 3 Claims.

⁵ “Jacobsen Opp. Decl.” refers to the Omnibus Declaration of Dr. Krista S. Jacobsen in Support of 2Wire Inc.’s Oppositions to TQ Delta, LLC’s Family 3 Motions, filed concurrently herewith.

2. Mazzoni in Combination with G.993.1.

2Wire has presented evidence that Mazzoni in combination with G.993.1 discloses each limitation of claim 19 of the '473 patent in its Motion for Summary Judgment of Invalidity for Family 3, and that summary judgment for 2Wire is warranted on that ground. D.I. 774 at 5-11. 2Wire also has shown that a POSITA would have been motivated to combine Mazzoni with G.993.1. D.I. 775 (Jacobsen Opening Decl.) ¶¶ 532-582. In its motion, TQ Delta argues only that a POSITA would not be motivated to combine Mazzoni with G.993.1.

First, TQ Delta first refers again to what it calls the “Mazzoni problem” in combining the two references. This argument fails for the same reason it fails with respect to the Mazzoni / LB-031 combination, discussed above. *See supra*, Section V.A.1. In short, there is no “Mazzoni problem.”

Second, TQ Delta’s argument that combining Mazzoni with G.993.1 would result in a transceiver with too little memory completely ignores that a POSITA is assumed to use his or her ordinary creativity in combining references. Dr. Jacobsen has opined that a POSITA would understand that it would be trivial to add memory to a transceiver to support the desired services. Jacobsen Opp. Decl., ¶ 128. Whether memory is shared or not, it is difficult to imagine that a POSITA would design a transceiver with too little memory to support the desired services. And TQ Delta and its expert, Dr. Cooklev, present no evidence that such a simple modification would be impossible, or not within the capacity of a POSITA. *See KSR*, 550 U.S. at 418. Not only has TQ Delta failed to show that it is entitled to summary judgment, it has raised no serious challenge to 2Wire’s motion for invalidity of claim 19 of the '473 patent over the combination of Mazzoni and G.993.1.

B. Genuine Disputes Of Material Fact Preclude Summary Judgment On The Obviousness Combinations Addressed Only In TQ Delta’s Motion.

1. LB-031 in Combination With the Knowledge of One of Ordinary Skill in the Art.

- a. LB-031 in Combination With the Knowledge of a POSITA Discloses Shared Memory.

2Wire has adduced evidence that LB-031 in combination with the knowledge of a POSITA discloses “shared memory” and “where in a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.”⁶ *See* Jacobsen Opp. Decl., ¶¶ 170-186, 226-230, 263-265, 280-297. LB-031 discloses allocating memory between an interleaver and a deinterleaver in a VDSL system, and describes allocating memory by exchanging the interleaver delay in octets. *Id.* at ¶ 171. Dr. Jacobsen opines that a POSITA would understand, given the disclosure of LB-031, that it would be used with shared memory. *Id.* at ¶ 172. The concept of shared memory was well-known by the time of the invention, and LB-031 describes how the “actual amount of memory required for interleaving and deinterleaving is implementation specific, and that a VDSL2 implementation can support a larger memory than is actually required.” *Id.* Dr. Jacobsen further opines that a POSITA would have combined this well-known concept of shared memory with the disclosure of LB-031. *Id.* at ¶ 173. No more evidence is needed to show a genuine dispute of material fact.

TQ Delta’s citation to Dr. Jacobsen deposition testimony regarding this combination does not justify summary judgment. *See Kaavo Inc. v. Amazon.com Inc.*, 323 F. Supp. 3d 630, 635 (D. Del. 2018) (noting that on summary judgment, the Court “may not make credibility determinations or weigh the evidence”). Dr. Jacobsen testified, consistent with the opinions in

⁶ TQ Delta equates these claim elements, which appear in different claims. For purposes of this motion, 2Wire does the same. TQ Delta does not directly address both of these limitations in its motion (*see* D.I. 778 at 7). If it does so in reply, 2Wire reserves the right to respond.

her invalidity reports, that a POSITA would understand that LB-031 could be – but does not necessarily have to be – used with shared memory. Walsh Decl., Ex. C (Jacobsen Dep. Tr.), 550:17-21 (“Q. . . . But given the disclosure of LB-031, is it necessarily the case that it could only be used with a device that implements shared memory? A. I don’t think the disclosure of LB-031 is limited to use with a shared memory.”). 2Wire has shown that there is a genuine dispute of material fact as to whether LB-031 in combination with the knowledge of a POSITA discloses shared memory.

b. LB-031 is Compatible with Shared Memory.

TQ Delta’s argument that the messaging scheme disclosed in LB-031 is supposedly incompatible with the use of shared memory does not justify summary judgment.

First, LB-031’s messaging scheme transfers parameters similar to the messages in the VDSL2 standard that forms the basis of TQ Delta’s infringement theories. *See* D.I. 791 (TQ Delta’s MSJ re infringement). In particular, TQ Delta asserts that the O-PMS message of VDSL2 contains a parameter called “max_delay_octet,” which purportedly meets the limitation “transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver [or interleaver].” *See, e.g.*, D.I. 792 (Targowska Decl. in support of TQ Delta’s MSJ of Infringement), Ex. 15 (Opening Report of Dr. Todor Cooklev), ¶¶ 232-236. LB-031 similarly discloses transmitting messages specifying interleaver delay in octets: “[f]or interoperability reasons, the VTU-O and VTU-R much exchange the interleaver delay in terms of octets.” D.I. 770 (Targowska Decl.), Ex. 14, (LB-031) at 3. Dr. Jacobsen has explained how this LB-031 message discloses the claimed message, at least within TQ Delta’s interpretation of the claims. Jacobsen Opp. Decl., ¶¶ 190-193, 231-236, 268, 280-292. If the messaging scheme in LB-031 is incompatible with shared

memory, then TQ Delta would be hard pressed to explain why the messaging scheme in VDSL 2 is compatible with shared memory.

Second, TQ Delta takes issue with how LB-031 selects transceiver parameters, specifically in its disclosure to “select the smaller of the transmitter and receiver capabilities, in each direction,” to argue that this makes LB-031 incompatible with sharing memory. *See* D.I. 778 at 7-8; D.I. 770 (Targowska Decl.), Ex. 14, (LB-031) at p. 3. The “explanation” identified by TQ Delta from its expert, Dr. Cooklev, is a generalized example that assumes that the VTU-O and VTU-R being used with LB-031’s messaging scheme each have a dedicated upstream memory and a dedicated downstream memory, *i.e.*, dedicated memory. *See* D.I. 778 at 8-9 (quoting Cooklev Corr. Rebuttal Report, ¶¶ 47-52). This example does not establish that LB-031 is incompatible with shared memory as a matter of law. If instead, for example, the messaging scheme of LB-031 were used with a VTU-O having 60 kilobytes of shared memory, and it received a message containing capabilities of 40 kB for deinterleaving and 20 kB for interleaving, it allocates its memory accordingly. Jacobsen Opp. Decl. ¶ 183. If the same VTU-O received a message containing capabilities of 30 kB for deinterleaving and 30kB for interleaving, it would allocate its memory accordingly, and a portion of the memory that had previously been used for interleaving would now be used for deinterleaving. *Id.* Thus, in an example that actually uses shared memory, there is no such “incompatibility.”

Third, contrary to TQ Delta’s contention, Dr. Jacobsen did not admit at her deposition that LB-031 was incompatible with shared memory. *See* D.I. 778 at 9-10. Again, TQ Delta misconstrues Dr. Jacobsen’s deposition testimony. The discussion cited by TQ Delta related to the amount of delay that a VTU-O and VTU-R can support, not an amount of memory. *See* Walsh Decl., Ex. C (Jacobsen Dep. Tr.), 518:8-520:6. Because the delay and the amount of

memory used to meet a delay can be different, Dr. Jacobsen's deposition testimony does not indicate that there is a certain quantity of unused memory, even if this were sufficient for purported incompatibility. *See* Jacobsen Opp. Decl., ¶¶ 96-100. The other scenario identified by TQ Delta, where a transceiver has a total of 20 kilobytes of memory, but cannot support a total of 12 kilobytes of memory upstream and 12 kilobytes of memory downstream does not bear on this issue either, because it addresses the total amount of memory, not whether or how memory could be shared. *Id.* at ¶ 184. TQ Delta has failed to show that it is entitled to summary judgment on this combination.

2. LB-031 in Combination With Voith.

TQ Delta has failed to show that there are no genuine disputes of material fact with respect to whether the combination of LB-031 and Voith renders claim 19 of the '473 patent obvious. TQ Delta argues that neither reference discloses shared memory, and that LB-031 "prevents" memory sharing. Both of these arguments fail.

First, 2Wire has presented evidence that a POSITA would understand Voith to disclose memory that can be allocated to interleaving and deinterleaving functions at different times, as required by the claims. *See* Jacobsen Opp. Decl., ¶¶ 607-628. In particular, Voith describes an ADSL transceiver that includes a forward error correction encoding function. D.I. 770 (Targowska Decl.), Ex. 16 (Voith), col. 5:58-62. An interleaving function and a deinterleaving function arbitrate for use of an external interleave/deinterleave memory that shares a single common external memory interface. *Id.* at col. 5:65-6:4. Thus, 2Wire has presented evidence that Voith discloses this limitation.

Contrary to TQ Delta's argument, Dr. Jacobsen did not admit at her deposition that Voith does not disclose shared memory. Again, as with the other references, her testimony acknowledges that one could implement the disclosure of Voith using dedicated memory or

shared memory. Walsh Decl., Ex. C (Jacobsen Dep. Tr.), 555:1-6 (“Q. Is it your position that the Voith reference discloses shared memory in the way it was dis – construed by the Court? A. I believe that a person having ordinary skill would recognize that memory could be shared memory as construed by the Court.”). Her acknowledgement that the memory in Voith could be either dedicated or shared does not invalidate its use as a prior art reference. *See id.* at 555:8-16 (“Q ... But is it also consistent with the Voith disclosure that the interleave/deinterleaver memory block 66 could include separate dedicated memory spaces for the interleaver and de-interleaver? A. It could be either dedicated or shared. Q. And the Voith reference itself doesn’t explicitly describe whether it is dedicated or shared; right? A. It does not say one way or the other.”).

Second, TQ Delta repeats its arguments that LB-031 is “incompatible” with shared memory. For the same reasons as stated above, this argument fails. *See supra*, Section V.B.1.b.

3. Voith in Combination with G.993.1, or Voith in Combination with G.993.1 and Mazzoni.

TQ Delta is also not entitled to summary judgment of no invalidity of claim 19 of the ’473 patent over Voith in combination with G.993.1, or in the alternative, Voith in combination with G.993.1 and Mazzoni. In its motion, TQ Delta largely repeats the same arguments – that Voith does not disclose shared memory, and that G.993.1 is “incompatible” with sharing memory – and they fail for the same reasons.

First, 2Wire has presented evidence that a POSITA would understand Voith to disclose memory that can be allocated to interleaving and deinterleaving functions at different times, as required by the claims. *See* Jacobsen Opp. Decl., ¶¶ 607-628; *see supra*, Section V.B.3.

Second, Dr. Jacobsen did not, as TQ Delta contends, admit that Voith does not disclose shared memory. Again, as with the combination of Voith and LB-031, her testimony

acknowledges that one could implement the disclosure of Voith using either dedicated memory or shared memory. Walsh Decl., Ex. C (Jacobsen Dep. Tr.), 555:1-6 (“Q. Is it your position that the Voith reference discloses shared memory in the way it was dis – construed by the Court? A. I believe that a person having ordinary skill would recognize that memory could be shared memory as construed by the Court.”).

Third, TQ Delta repeats its argument a POSITA would not be motivated to combine Voith and G.993.1 because the messaging scheme of G.993.1 is supposedly “incompatible” with shared memory for the same reasons that LB-031 is supposedly “incompatible” with shared memory. D.I. 778 at 17. That argument fails for the same reasons as TQ Delta’s incompatibility arguments with respect to LB-031. *See supra*, Section V.A.1.b. TQ Delta’s argument improperly glosses over the strong similarities between the messaging scheme of G.993.1 and the messaging scheme of G.993.2, the latter of which that forms the basis for TQ Delta’s infringement theory in this case. Dr. Jacobsen explains that G.993.1 discloses an initialization procedure that allows a VDSL transmitter and receiver to exchange parameters such as Reed-Solomon settings and interleaver parameters. *See Jacobsen Opp. Decl.*, ¶¶ 67-71; D.I. 770 (Targowska Decl.), Ex. 18 (G.993.1), § 12.4.1. This includes the R-MSG2, which transfers, among other things, the Reed-Solomon capabilities and a value called “maximal interleaver memory,” expressed in bytes, and the O-MSG2, which contains the field “maximum interleaver delay,” expressed in milliseconds. D.I. 770 (Targowska Decl.), Ex. 18 (G.993.1), §§ 12.4.6.3.1.1, 12.4.6.2.1.1); *Jacobsen Opp. Decl.*, ¶¶ 68-70. In its infringement case, TQ Delta identifies the O-PMS message specified in G.993.2 as meeting the claim limitation requiring a “message received during initialization” Given this, TQ Delta has no good basis to argue

that the messaging scheme of VDSL (G.993.1), and which transfers maximal interleaver memory in bytes, and maximum interleaver delay in milliseconds, is “incompatible” with shared memory.

Fourth, TQ Delta again argues that Mazzoni would be inoperable with the messaging scheme of G.993.1 for the same reasons that Mazzoni would be inoperable with LB-031. As demonstrated above, this argument fails. *See supra*, Section V.A.1. TQ Delta’s motion for summary judgment is not warranted as to this combination.

4. Fadavi-Ardekani in Combination with G.993.1.

TQ Delta has not shown that it is entitled to summary judgment that each of the Asserted Family 3 claims is not invalid based on the combination of G.993.1 and Fadavi-Ardekani.

TQ Delta contends that the combination of Fadavi-Ardekani and G.993.1 does not disclose “shared memory” or memory “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time.” D.I. 778 at 18. Dr. Jacobsen has opined, however, that Fadavi-Ardekani discloses shared memory. Jacobsen Opp. Decl., ¶¶ 317-328. Fadavi-Ardekani describes an ADSL system that includes a interleave/deinterleave memory (IDIM) that transfers data frames to and from a framer/coder block for interleaving and deinterleaving. D.I. 770 (Targowska Decl.), Ex. 17 (Fadavi-Ardekani), col. 6:55-60. Fadavi-Ardekani teaches that “[t]he size of the IDIM and the interleave depth [of the ADSL sessions] may be varied so that a different number of sessions may be supported by the transceiver of the invention.” *Id.* at col. 7:3-5. In an “optimal implementation of the interleaver,” Fadavi-Ardekani teaches using “the same memory for receive data and transmit data,” for example, using a 20-kbyte IDIM, which is sufficient to support “a standard ADSL session at full interleave depth,” or more than one session with each using a smaller interleaver depth. *Id.* at col. 7:25-32. The memory in Fadavi-Ardekani operates in a “ping-pang” fashion where “areas of the memory buffer are alternately utilized exclusively

by one agent (a transceiver component for performing some function) and then by a second agent” and where “[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent.” *Id.* at col. 5:60-65.

Dr. Jacobsen testified that the IDIM disclosed in Fadavi-Ardekani is “shared memory” “because it ‘holds DMT frames of data and may be utilized in a ping-pang fashion.’” Jacobsen Opp. Decl., ¶ 320 (quoting Fadavi-Ardekani, col. 6:57-58). Further, she explained that there is “nothing in Fadavi-Ardekani to suggest that there is any pre-set, immovable boundary between the portion of the IDIM used for interleaving and the portion used for deinterleaving.” *Id.* at ¶ 324. 2Wire has also presented evidence that Fadavi-Ardekani discloses allocating this memory between transmit and receive functions. *Id.* at ¶¶ 342-362.

In response, TQ Delta argues only that Dr. Jacobsen supposedly admitted at her Family 3 deposition that Fadavi-Ardekani does not disclose shared memory. D.I. 778 at 18-19. She did not. In response to the hypotheticals presented to her by TQ Delta’s counsel, she testified only that using dedicated memory would be one way to implement the “session” in the hypothetical, and that “you could arrange [the memory] in a number of ways.” Walsh Decl., Ex. C (Jacobsen Dep. Tr.) 564:15-565:1. In a portion of her testimony omitted in TQ Delta’s brief, Dr. Jacobsen goes on to explain that, in the hypothetical, “you could also say the first 16 kilobytes are for interleaving, and the last 8 kilobytes are for de-interleaving. You could do it that way. You could also, on a per-session basis, say, I need 6 kilobytes for downstream, 2 kilobytes for upstream. That would be another way. And then, when you changed the number of sessions, ***that would change where the memory was allocated for downstream and upstream.***” *Id.* at 564:24-565:7 (emphasis added, underlined portion omitted). This is consistent with shared memory. In another portion of her testimony cited by TQ Delta, they again omit where she

explains how Fadavi-Ardekani could be implemented using shared memory (Jacobsen Dep. Tr.

569:13-570:9) (emphasis added on omitted portions):

Q. So the – the version of the division of memory that I went through, where you have 64 K of dedicated interleave memory, that you divide up amongst the four sessions, 8 K of dedicated de-interleaver memory that you divide up amongst the four sessions, and 4 K of fast path dedicated, that you divide up amongst the four sessions, that would not be inconsistent with Fadavi's disclosure; correct?

A. Well it depends on how you're using "dedicated," because it's all in the same buffer. Are you saying dedicated means there is an immovable boundary between the part that's used for interleaving and the part that's used for de-interleaving?

Q. Yes.

A. Okay. That would be one way of to implement this disclosure. And then the other – another way would be, instead of doing that, you would set aside interleave memory for one session and de-interleave memory for that same session, and then do the same for the additional sessions."

Similarly, in another portion of her testimony not cited by TQ Delta, Dr. Jacobsen again explains

that Fadavi-Ardekani would not be confined to dedicated memory (Walsh Decl., Ex. C,

(Jacobsen Dep. Tr.) 566:19-567:7 (emphasis added)):

Q. And the particular implementation choice is not disclosed in Fadavi, correct?

A. I don't believe Fadavi describes where, within this IDIM, the interleaving part is taking place and the de-interleaving part is taking place. He describes that the – the two portions are disjoint, but not how, from session to session, different sessions are supported within that IDIM.

Q. Okay. So – so you would agree with me that Fadavi does not necessarily disclose shared memory?

A. It doesn't disclose any particular implementation. My position is that it would be recognized as being implementable either in shared memory or dedicated memory.

Again, at most Dr. Jacobsen testified that *one* way of implementing the disclosure of Fadavi-

Ardekani would be to use dedicated memory. And, even if Dr. Jacobsen's deposition testimony

could be construed as being in conflict with the invalidity opinions disclosed in her report, that goes to her credibility, which cannot be resolved on summary judgment.

5. Fadavi-Ardekani in Combination with G.992.2.

For the combination of Fadavi-Ardekani and G.992.2, TQ Delta repeats in cursory fashion its arguments with respect to the combination of Fadavi-Ardekani and G.993.1, and those arguments fail for the same reasons. *See supra*, Section VI.B.4.

TQ Delta asserts, without explanation, that G.992.2 “is another example of a prior art DSL standard with a messaging scheme that is incompatible with shared memory.” D.I. 778, at 20. But, as Dr. Jacobsen explains, G.992.2 specifies requirements and functions of ADSL transceivers, including the selection and communication of forward error correction and interleaving parameters using initialization messages. *See Jacobsen Opp. Decl.*, ¶¶ 60-62 (description of G.992.2). Notably, TQ Delta does not contend that these messages do not disclose the messaging scheme of the Asserted Family 3 Claims.

TQ Delta’s argument that G.992.2 does not disclose “shared memory” misses the point. 2Wire has provided evidence that Fadavi-Ardekani discloses “shared memory,” and that a POSITA would be motivated to combine its teachings with G.992.2. *Jacobsen Opp. Decl.*, ¶¶ 317-328, 570-580. In the deposition testimony cited by TQ Delta, Dr. Jacobsen testified, consistent with the opinions she has expressed, that G.992.2 can be used with dedicated or shared memories. *Walsh Decl.*, Ex. C (*Jacobsen Dep. Tr.*) at 553:19-21 (“So [G.992.2] could be used with dedicated memories? A: It could be used with *dedicated or shared*.” (emphasis added)). TQ Delta has not shown an absence of genuine disputes of material fact with respect to this combination.

VI. CONCLUSION

For the reasons stated above, TQ Delta's motion for summary judgment of no invalidity should be denied in its entirety.

Dated: March 8, 2019

Respectfully submitted,

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