

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

TQ DELTA, LLC,

Plaintiff,

v.

2WIRE, INC.

Defendant.

Civil Action No. 13-cv-1835-RGA

**OPENING EXPERT REPORT ON INVALIDITY OF DR. KRISTA S. JACOBSEN
FOR FAMILY 3 PATENTS**

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I. INTRODUCTION

1. My name is Krista S. Jacobsen. I have been asked by Defendant 2Wire, Inc. to provide this report in connection with the above-captioned District Court action. Specifically, I have been asked to opine on the validity of claim 1 of U.S. Patent No. 8,276,048 (“the ’048 patent”), claim 5 of U.S. Patent No. 7,836,381 (“the ’381 patent”), claim 13 of U.S. Patent No. 7,844,882 (“the ’882 patent”), and claim 19 of U.S. Patent No. 8,495,473 (“the ’473 patent”). I understand that plaintiff TQ Delta, LLC has alleged that certain 2Wire products infringe these claims. I further understand that these patents are referred to in this action as being part of “Family 3.”

II. BACKGROUND AND QUALIFICATIONS

2. I was awarded a Ph.D. in Electrical Engineering from Stanford University in 1996, and a Master’s Degree in Electrical Engineering in 1993, also from Stanford University. I held a National Science Foundation Graduate Fellowship from 1991-94 and an IBM Graduate Fellowship from 1994-95. In 1993, I was awarded an IEEE Communications Society Scholarship.

3. I hold a Bachelor of Science Degree in Electrical Engineering, summa cum laude, from the University of Denver, which I received in 1991. From 1986-91, I held a University of Denver Honors Scholarship, and from 1987-91, I held a Colorado Scholars Scholarship. I was elected to Phi Beta Kappa in 1988, and I received the University of Denver’s Distinguished Senior Woman Award in 1990 and the University of Denver Pioneer Award in 1991. I won the Denver Section of the IEEE Student Paper Contest in 1991.

4. At Stanford, my Ph.D. research focused on technology for digital communications, including multicarrier modulation, discrete multi-tone (DMT) modulation, and orthogonal frequency division multiplexing (OFDM). My doctoral thesis topic was “Discrete

Multi-Tone-Based Communications in the Reverse Channel of Hybrid Fiber-Coax Networks.”

My research adviser was Dr. John M. Cioffi, who is known as the “father of digital subscriber lines (DSL)” and whose pioneering research in DSL earned him the Marconi Prize in 2006.

5. From 1996 to 2004, I worked as an engineer at Amati Communications Corporation, which was acquired by Texas Instruments (TI) in 1998. I was part of the team that developed the world’s first operational DMT-based VDSL transceivers. From 2004 to 2006, as a consultant, I assisted clients to determine and execute DSL standardization and product strategies, wrote computer simulations of multicarrier systems, and generated and presented technical tutorials.

6. From 1996 through 2006, I participated in several standards-setting organizations that standardized DSL systems, including ATIS T1E1.4 (later renamed NIPP-NAI), ETSI TM6, ITU-T Study Group 15, Question 4, and IEEE 802.3ah (Ethernet in the First Mile). I wrote and/or presented many dozens of technical contributions to these organizations.

7. I am a co-editor of two books on DSL technology and the author of several book chapters on multicarrier modulation, DSL technology, and DSL standardization. In addition, I have authored or co-authored numerous technical papers and magazine articles on multicarrier communications, and, in 2001-02, I co-edited an issue of the IEEE Journal on Selected Areas in Communication focused on twisted pair transmission.

8. I have over ten years of experience working in the development and standardization of DSL technologies, including those embodied in the ITU-T Recommendations involved in the above-captioned District Court actions. I am an inventor named on eleven patents solving issues presented by or related to multicarrier modulation. My experience

includes work in DSL technologies and the DSL industry both before and after the purported priority date of the Family 2 patents.

9. I am also licensed to practice before the Patent and Trademark Office. I am currently an attorney who serves as an expert consultant and witness for patent litigation, and I provide patent prosecution and counseling services in multiple areas, including telecommunications.

10. A detailed curriculum vitae showing more of my credentials is attached to this report as Appendix A.

III. COMPENSATION

11. I am being compensated for my time at the rate of \$400 per hour. This compensation is not contingent on my performance, the outcome of this matter, or any issues involved in or relating to this matter.

IV. DOCUMENTS AND OTHER MATERIALS RELIED UPON

12. In forming the opinions set forth in this declaration, I have reviewed each of the Family 3 patents that were asserted by TQ Delta in this action – U.S. Patent No. 7,831,890 (“the ’890 Patent”), along with the ’048, ’381, ’882, and ’473 patents. Additionally, I have considered my own experience and expertise concerning the knowledge of a person having ordinary skill in the relevant art during the timeframe of the claimed priority date of the Family 3 patents. I have reviewed information generally available to, and relied upon by, a person having ordinary skill at the time of the alleged invention. I have also reviewed the parties’ claim construction briefing and the Court’s order on the same.

13. In addition, I have reviewed the materials listed in Appendix B.

14. I was told to assume that the earliest possible time of the alleged invention for each of the Family 3 patents is October 12, 2004, the date on which Provisional Application No.

60/618,269, was filed. I disagree, however, that the Family 3 patents are entitled to the priority date of the provisional application, as I explain below in Section VII.G.2. I am also informed, however, that once an accused infringer has introduced sufficient evidence to put at issue whether there is prior art alleged to anticipate the claims being asserted, and that prior art is dated earlier than the apparent effective date of the asserted patent claim, the patentee has the burden of going forward with evidence and argument to the contrary.

V. LEGAL PRINCIPLES

15. Although I am licensed to practice law, I am not offering any legal opinions in this Report. My opinions are based on the Court's constructions and, where the Court did not construe a term, the meaning that term would have had to a person having ordinary skill in the art in light of the specification and the prosecution history at the time of the filing of the earliest priority application.

A. Anticipation Under 35 U.S.C. § 102

16. I am informed and understand that to anticipate a patent claim under 35 U.S.C. § 102, a single asserted prior art reference must disclose each and every element of the claimed invention, either explicitly, implicitly, or inherently, to a person of ordinary skill in the art. There must be no difference between the claimed invention and the disclosure of the alleged prior art reference as viewed from the perspective of the person of ordinary skill in the art. Also, I understand that in order for a reference to be an anticipating reference, it must describe the claimed subject matter with sufficient clarity to establish that the subject matter existed and that its existence was recognized by persons of ordinary skill in the field of the invention. In addition, I am informed and understand that in order to establish that an element of a claim is "inherent" in the disclosure of an asserted prior art reference, extrinsic evidence (or the evidence outside the four corners of the asserted prior art reference) must make clear that the missing

element is necessarily found in the prior art, and that it would be recognized as necessarily present by persons of ordinary skill in the relevant field.

17. In my opinions below, when I say that a person of ordinary skill would understand, readily understand, or recognize that an element or aspect of a claim is disclosed by a reference, I mean that the element or aspect of the claim is disclosed explicitly to a person of ordinary skill in the art.

B. Obviousness Under 35 U.S.C. § 103

18. I am informed and understand that obviousness is a determination of law based on various underlying determinations of fact. In particular, these underlying factual determinations include (1) the scope and content of the prior art; (2) the level of ordinary skill in the art at the time the claimed invention was made; (3) the differences between the claimed invention and the prior art; and (4) the extent of any proffered objective indicia of nonobviousness. I understand that the objective indicia that may be considered in such an analysis include commercial success of the patented invention (including evidence of industry recognition or awards), whether the invention fills a long-felt but unsolved need in the field, the failure of others to arrive at the invention, industry acquiescence and recognition, initial skepticism of others in the field, whether the inventors proceeded in a direction contrary to the accepted wisdom of those of ordinary skill in the art, and the taking of licenses under the patent by others, among other factors.

19. To ascertain the scope and content of the prior art, it is necessary to first examine the field of the inventor's endeavor and the particular problem for which the invention was made. The relevant prior art includes prior art in the field of the invention, and also prior art from other fields that a person of ordinary skill in the art would look to when attempting to solve the problem.

20. I understand that a claim may be rendered obvious if a person having ordinary skill in the art would understand the claimed invention as a predictable variation of a known reference.

21. I am informed and understand that an obviousness evaluation can be made using either a single reference or a combination of several prior art references. An obviousness analysis involving two or more references generally requires a reason why a person having ordinary skill in the relevant field would have combined aspects of those references in the way the asserted patent claims do. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the link may simply be common sense. An obviousness analysis can recognize that market demand, rather than scientific literature, often drives innovation, and that is sufficient motivation to combine references.

22. I understand that a particular combination of prior art references may be made by merely showing that it was obvious to try the combination. For example, common sense is a good reason for a person having ordinary skill to pursue known options when there is a design need or market pressure to solve a problem, and there are a finite number of identified, predictable solutions.

23. I am informed and understand that a determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention. Instead, it is my understanding that in order to render a patent claim invalid as being obvious from a combination of references, there must be some evidence within the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination in a way that would produce the patented invention.

24. I am further informed and understand that a proper obviousness analysis focuses on what was known or obvious to a person having ordinary skill in the art, not just the patentee. Therefore, in an obviousness analysis, neither the motivation nor the purpose of the patentee is controlling. What is important is whether there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. For example, any need or known problem in the field at the time of the alleged invention that is supposedly addressed by the patent can provide a reason for combining the limitations in the manner claimed if a combination of prior art would address the same.

25. In addition, it is my understanding that in order to find a patent claim invalid for obviousness, there must be a finding that each element in each limitation of the patent claim is disclosed, taught, or suggested by the asserted combination of prior art references or elsewhere in the relevant prior art. I understand, however, that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. But multiple prior art references or elements may, in some circumstances, be combined to render a patent claim obvious. I understand that I should consider whether there is an "apparent reason" or motivation to combine the prior art references or elements in the way the patent claims. To determine whether such an "apparent reason" or motivation to combine the prior art references or elements in the way a patent claims exists, it will often be necessary to look to the interrelated teaching of multiple prior art references, to the effects of demands known to the design community or present in the marketplace, and to the background knowledge possessed by a person of ordinary skill in the art.

26. I am further informed and understand that when an element is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either

in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation of that available element, Section 103 likely renders the invention obvious. For the same reason, I am informed and understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that such technique would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Following these principles often requires one to look to interrelated teachings of multiple patents; the effects of demands known to the design community present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known element in the manner claimed by the patent at issue. I am further informed and understand that the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, because one can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

27. I am further informed and understand that although the use of the “teaching, suggestion or motivation” test for combining references has not been completely rejected, the obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. I am informed and understand that in many fields there is little discussion of obvious techniques or combinations, and it is often the case that market demand, rather than scientific literature, drives design trends. Under the correct analysis, any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. Finally, I am informed and understand that common sense teaches that familiar items may have obvious

uses beyond their primary purposes and, in many cases, a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle.

28. I am also informed and understand that even though a prior art reference does not fully anticipate a claim of a patent, a claim may, nonetheless, be rendered obvious to one of ordinary skill in the art if the differences between the subject matter set forth in the patent claim and the prior art are such that the subject matter as a whole of the claim would have been obvious at the time the claimed invention was made.

29. I further am informed that in determining whether the claimed subject matter is obvious, one must also examine any objective indicia of nonobviousness (also called secondary considerations). I also have been informed that secondary considerations cannot overcome a strong showing of obviousness. In that regard, I am informed that secondary considerations must be commensurate in scope (proportional) with respect to the claims for which the evidence is offered to support. I have been informed that evidence of secondary considerations is not commensurate in scope if the claims are broader than the scope of such evidence. Relatedly, I have been informed that a nexus or connection between the merits of the claimed invention and the alleged evidence of secondary considerations is necessary. Specifically, I have been informed that the secondary considerations must be tied to purported novel or new elements of the claimed invention.

30. I also am informed that secondary considerations of nonobviousness include (1) whether the claimed subject matter achieved unexpected results or benefits, (2) whether the claimed subject matter satisfied a long-felt but unmet need, (3) whether the claimed subject matter was commercially successful as a result of the merits of a claimed subject matter (rather than the result of design needs, market pressure, advertising, or similar activities), (4) whether

other skilled artisans failed in their attempts to solve the same problems addressed by the invention, (5) whether others copied the claimed subject matter, and (6) whether others in the field praised claimed the subject matter.

31. Specifically, I am informed that evidence that other skilled artisans failed in their attempts to solve the same problems addressed by claimed invention is potential evidence of nonobviousness. To demonstrate failure of others, I am informed that plaintiff must establish that others skilled in the art tried and failed to find a solution for the problem allegedly solved by the invention claimed by the asserted patents. I further understand that for such evidence of failure to be relevant as an objective indicia of nonobviousness, these prior unsuccessful attempts must have failed because they lacked the claimed features of the asserted inventions. Purported failures unrelated to the patented invention are not relevant secondary considerations of nonobviousness.

32. I also am informed that evidence of a long-felt unmet need for the claimed invention is one factor courts may consider when assessing the obviousness of that invention. The underlying rationale for accepting evidence of a long-felt unmet need as evidence of nonobviousness, as I understand it, is based on the assumption that if an unmet need persists for a long time despite commercial incentives to offer a solution, the resolution of the problem may not be obvious. I also understand that the long-felt unmet need must be directly related to the subject matter of the claimed invention and must actually provide a result that meets the claimed need. I further am informed that the length of time that must pass to constitute a “long felt” need is to be determined in the light of the speed of innovation in the relevant industry. I also have been informed that long-felt, unmet need should be based upon alleged inadequacies in the technical knowledge of those skilled in the art, not due to business-driven market forces.

Lastly, I have been informed that any evidence of a need that post-dates the filing date of a challenged patent is irrelevant to the determination of nonobviousness.

33. I am further informed that “commercial success” is a legal construct that has been established through case law. I have been informed that analysis of commercial success is premised on the concept that if a product is economically successful, it may provide objective evidence of nonobviousness. I further understand that any purported commercial success of the product must be attributable to the alleged novel features of the claimed invention. I understand this to mean that, to support a finding of nonobviousness, any alleged commercial success must be driven by and attributable to the purported merits of the patented invention, and not by other factors unrelated to the allegedly novel features of the claimed invention. In other words, there must be a causal correlation, or “nexus,” between the unique merit of the claimed invention and the success of the product. I also understand that if purported commercial success is due to an element in the prior art, no nexus exists.

34. I additionally understand that an alleged infringer’s copying of a claimed invention rather than one that is in the public domain can support a finding of nonobviousness. Likewise, I am informed that to support a finding of nonobviousness, alleged industry praise must be linked to the patented invention. In other words, a patentee must show that any industry praise is attributable to material differences between the prior art and the patented invention. I have been informed that a patentee’s statements that are intended to generate interest in a product are not evidence of industry praise. Similarly, publications authored or sponsored by or on behalf of a patentee fail to demonstrate true industry praise.

35. I further understand that the near simultaneous invention by two or more equally talented inventors working independently may or may not be an indication of obviousness. In

other words, the fact that another person simultaneously and independently created the same invention claimed in the patent-in-suit can serve as an indication that the invention was obvious.

C. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

36. I have been informed that that 35 U.S.C. § 112, second paragraph, requires that a patent specification include claims particularly pointing out and distinctly claiming the subject matter which the inventor regards as his invention. I further understand that in order to comply with this requirement, a patent's claims, viewed in light of the specification and prosecution history, must inform those skilled in the art about the scope of the invention with reasonable certainty. Otherwise, the patent claims are invalid as indefinite.

37. I further have been informed that under this "reasonable certainty" standard, an undefined claim term renders a claim indefinite when it results in the existence of multiple methods leading to different results without guidance in the patent or the prosecution history. I also understand that this indefiniteness problem will persist even if someone skilled in the art could determine which method was the most appropriate.

38. I also understand that a claim may be indefinite where it employs a narrow numerical range that falls within a broader range, at least when the boundaries of the claim are not discernible. Likewise, I understand that claim language employing terms of degree may be indefinite where the language does not provide enough certainty to one of skill in the art when read in the context of the specification – for instance, where the term of degree is highly subjective and, on its face, provides little guidance to one of skill in the art such that, when combined with intrinsic evidence, the subjectivity does not provide a definition or boundaries for the term and/or does not provide any reference point for comparison.

D. Written Description Under 35 U.S.C. § 112, ¶ 1

39. I have been informed that the standard for satisfying written description with respect to a patent is that the patent specification reasonably conveys to a person having ordinary skill in the art that the inventor had possession of the subject matter of the claims as of the effective filing date.

E. Enablement Under 35 U.S.C. § 112, ¶ 1

40. I have been informed that to satisfy the enablement requirement with respect to a patent, the specification must describe the manner and process of making and using the claimed invention so as to enable the full scope of the claims, such that the public is enriched by the patent specification at least commensurate with the scope of those claims.

41. Furthermore, I understand that a patent specification that does not allow a person having ordinary skill in the art to practice the invention without undue experimentation is not enabled. I have been informed that certain factors are typically considered when evaluating the level of experimentation, such as the quantity of experimentation necessary to make or use the invention based on the content of the disclosure, the amount of direction or guidance presented by the inventor, the presence or absence of working examples, the breadth of the claims, the nature of the invention, the level of one of ordinary skill and the predictability or unpredictability of the art.

42. Therefore, I will analyze the prior art and other issues using this framework.

VI. LEVEL OF SKILL IN THE ART

43. I am informed and understand that the claims of a patent are judged from the perspective of a hypothetical construct involving a “person of ordinary skill in the art.” The “art” is the field of technology to which the patent is related. I understand that the purpose of using the viewpoint of a person of ordinary skill in the art is for objectivity. I understand that a

person of ordinary skill in the art is presumed to know and be familiar with all of the relevant art in the field at the time of invention.

44. I was also asked to provide an opinion regarding the skill level of a person of ordinary skill in the art of the Family 3 patents. I considered several factors, including the types of problems encountered in the art, the solutions to those problems, the pace of innovation in the field, the sophistication of the technology, my experience as a person who worked in the art on the Family 3 patents' priority date, and the education level of active workers in the field.

45. In my opinion, at the time of the alleged invention, a person having ordinary skill in the art would have had a bachelor's degree in electrical engineering or computer engineering and 5 years of experience in digital communications, a Master's degree in electrical engineering and 2-3 years of experience in digital communications, or a Ph.D. in electrical engineering with 1-2 years of experience in digital communications.

46. I am qualified as a person of at least ordinary skill in the art, and my qualifications enable me to provide opinions regarding the Family 3 patents from the perspective of one of ordinary skill in the art.

VII. BACKGROUND OF THE TECHNOLOGY

47. The Family 3 patents share a common specification.¹ The Family 3 patents are generally directed to methods, systems, and apparatuses for allocating shared memory between interleavers and deinterleavers.

A. Forward Error Correction and Reed Solomon Coding

48. In a digital communication system, a transmitter transmits data to a receiver over a channel. The channel attenuates and adds noise to the transmitted signal. As a result,

¹ Accordingly, citations are to U.S. Patent No. 7,844,882 ("the '882 patent") unless otherwise noted.

sometimes the bits detected by the receiver do not match the bits represented by the transmitted signal sent by the transmitter. Consequently, digital communication systems often employ certain well-known techniques to detect, and sometimes correct, errors in the received bit stream.

49. Error correction techniques enable a receiver to detect the presence of errors and also correct at least some of those errors. To apply an error correction technique, the transmitter adds redundant information to a message to be transmitted. The receiver then uses the redundant information to detect a limited number of errors that may occur anywhere in the message, and often to correct those errors. When the communication system uses an error correction technique, the receiver can correct at least some errors in the received data, which reduces and could eliminate entirely any need for the receiver to request retransmission of corrupted messages.

50. Practical error correction techniques are often called forward error correction (FEC). One type of FEC is block codes. To apply a block code, the transmitter partitions the data to be transmitted into blocks and adds redundancy to each block to form a *codeword*. The transmitter appends r redundancy symbols to each block of k symbols, without altering the original k symbols, to form codewords having $k + r$ symbols. The receiver then uses the information in the r redundancy symbols to automatically detect and correct errors in the data portion of the codeword. A well-known example of a block code is the Reed-Solomon coding used in ADSL and VDSL.

51. Many communication systems, including ADSL and VDSL, are byte-oriented systems, and each Reed-Solomon-encoded data block contains an integer number of bytes. The bytes in each Reed-Solomon codeword include K data bytes (i.e., the data to be transmitted in

the block) and R redundancy bytes that result from the Reed-Solomon code calculation. Thus, the size of each Reed-Solomon codeword is $N = K + R$ bytes long.

52. The mathematics of Reed-Solomon codes are complicated, but the essential property is that the maximum number of data elements with any number of errors that can be corrected is equal to half of the number of redundancy elements. In other words, a byte-oriented Reed-Solomon code can correct as many as $R/2$ errored data bytes, regardless of how many individual errors are within those data bytes.

53. As a simple example, if $R = 16$, up to 8 erroneous bytes can be corrected, regardless of how many bits of each errored byte are in error. Reed-Solomon codes are particularly helpful for use in environments that suffer from noise bursts because any erroneous element counts as a single error regardless of how many bits of that element are in error.

B. Interleaving and Deinterleaving

54. Interleaving is a technique used in ADSL and VDSL to improve the performance of Reed-Solomon coding in the presence of *impulse noise*, by which I mean intermittent and unpredictable bursts of noise that can temporarily overwhelm the data-carrying signal over several consecutive symbol periods. Deinterleaving is the complementary process that “undoes” interleaving. Interleaving—and, therefore, deinterleaving—have been specified in ADSL since the first T1.413 Issue 1 standard was published in 1995.

55. To apply interleaving, the transmitter shuffles consecutive bytes of the data stream in a known and systematic way before transmitting them to the receiver. As a result of the interleaving process, bytes that are adjacent in the data sequence are transmitted non-consecutively, spread out over a time interval. The receiver knows how the transmitter interleaved the bytes and reorders them before performing Reed-Solomon decoding to detect, and ideally correct, errors within the codewords.

56. Figure 1 below illustrates how the interleaving process works using a simple interleaving procedure. The transmitter separates the data elements into a number of blocks of five elements each (i.e., A1, A2, A3, A4, A5; B1, B2, B3, B4, B5; etc.). Elements from four blocks are then interleaved and transmitted in turn to create a sequence $AxBxCxDx$.

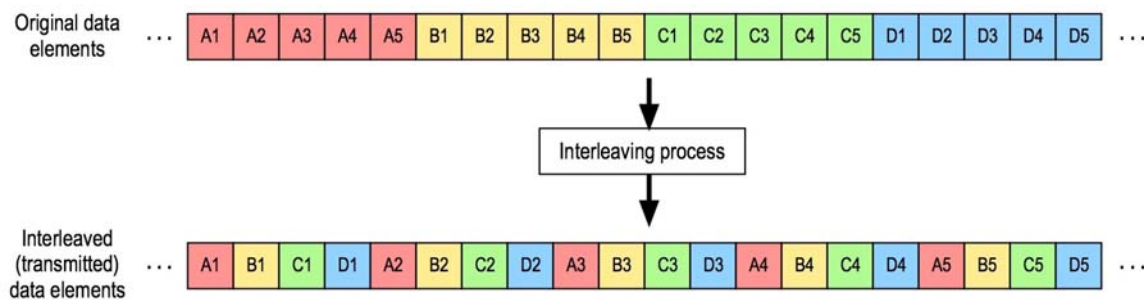


Figure 1: Interleaving example

57. Note that the interleaving process significantly increases the time interval over which the data elements from each of the individual data blocks are transmitted. Following the interleaving process in this simple example, the first and last data elements of each block are separated by 15 other data elements, and consecutive data elements of each block are separated by three other data elements. In real systems, the separation after interleaving will normally be hundreds or even thousands of bytes.

58. The receiver knows how the transmitter interleaved the data elements and can reverse the interleaving process by collecting all of the interleaved data elements and using a complementary deinterleaving process. The deinterleaving process results in the data elements being reordered into their original sequence, as shown in Figure 2 below.

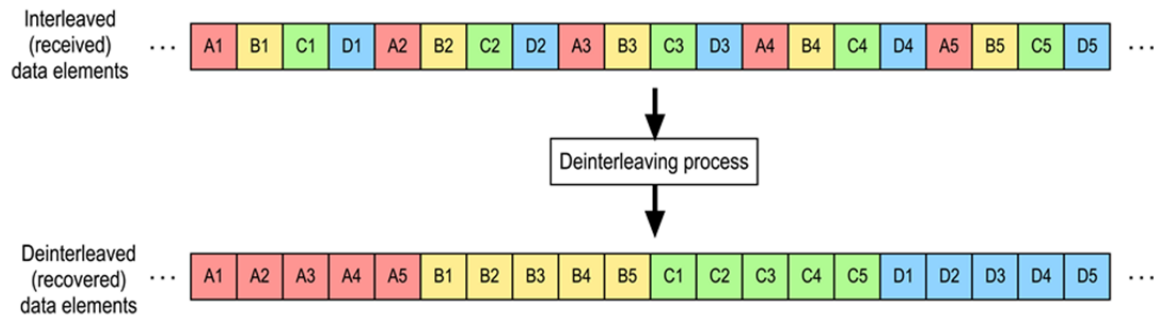


Figure 2: Deinterleaving example

59. DSL systems often use interleaving to improve the performance of the Reed-Solomon code. Errors in the received data caused by impulse noise tend to occur in bursts. Without interleaving, impulse noise causes errors that are concentrated within one or more consecutive Reed-Solomon codewords. As I explained above, a Reed-Solomon code can correct up to $R/2$ errored data elements in a codeword, where R is the number of redundancy bytes. If a single codeword has more than $R/2$ data bytes with errors, the Reed-Solomon code cannot correct all of the errors. Without interleaving, impulse noise can readily cause errors in more than $R/2$ of the bytes within a single Reed-Solomon codeword, which means the Reed-Solomon code (probably) cannot correct all of those errors.

60. If the transmitter interleaves the bytes prior to transmission, however, the effects of bursts of errors are spread out over multiple Reed-Solomon codewords when the bytes are reordered by the receiver, instead of being concentrated in a fewer number of Reed-Solomon codewords. After deinterleaving, the code can correct all of the errors as long as none of the reordered blocks of data bytes has more than $R/2$ bytes with errors.

61. As an example of the effects of impulse noise on Reed-Solomon coding effectiveness without interleaving, assume a transmitter sends a sequence of bytes as follows:

$$\left| B_0^1 \ B_1^1 \ B_2^1 \ B_3^1 \ B_4^1 \ B_5^1 \ B_6^1 \right| B_0^2 \ B_1^2 \ B_2^2 \ B_3^2 \ B_4^2 \ B_5^2 \ B_6^2 \left| B_0^3 \ B_1^3 \ B_2^3 \ B_3^3 \ B_4^3 \ B_5^3 \ B_6^3 \right| \dots$$

where the subscripts are the byte indices within a codeword, and the superscripts are the codeword indices. The vertical lines show the codeword boundaries. Assume impulse noise corrupts five consecutive bytes as shown below by Xs:

$B_0^1 \ B_1^1 \ B_2^1 \ B_3^1 \ B_4^1 \ B_5^1 \ B_6^1 \mid B_0^2 \ B_1^2 \ B_2^2 \ B_3^2 \ X \ X \ X \mid X \ X \ B_2^3 \ B_3^3 \ B_4^3 \ B_5^3 \ B_6^3 \mid \dots$

Assuming $R/2$ is 2, the Reed-Solomon code can correct the two errored bytes in the third codeword, but it cannot correct each of the three errored bytes in the second codeword.

62. ADSL and VDSL use a particular kind of interleaving called *convolutional interleaving*. Figure 3 below is an example illustrating how a transmitter performs convolutional interleaving. Visualizing the interleaver memory as a matrix, codewords are written into the rows and read out of the columns of the matrix to create the interleaved stream of bytes. In convolutional interleaving, the first bytes of the D codewords in different rows are in different columns (i.e., subsequent codewords are shifted to the right by one column when written into the rows). The deinterleaver operates similarly to the interleaver, except that the received bytes are written into the columns of the matrix and read out row by row.

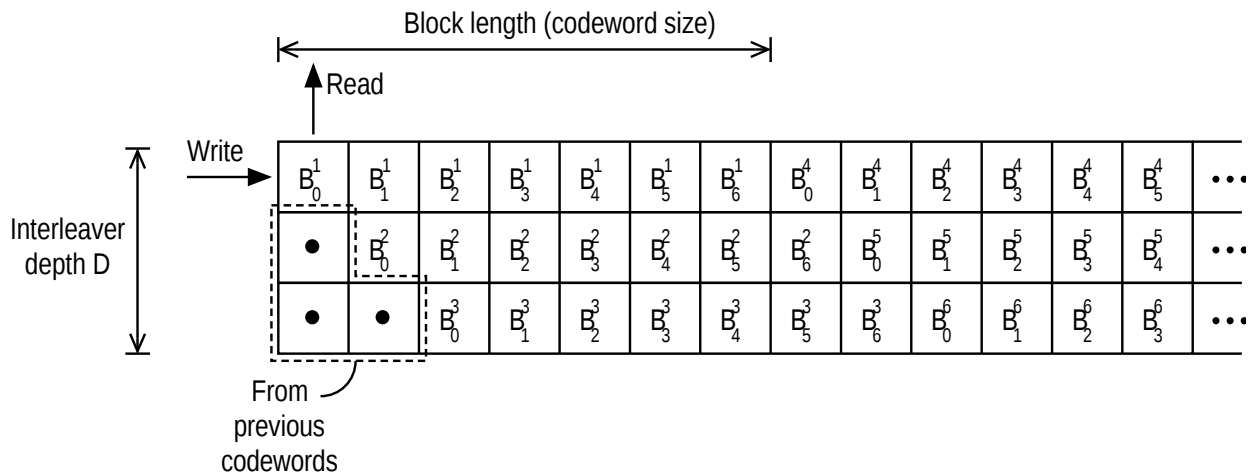


Figure 3: Convolutional interleaver with 7-byte codeword length and depth $D = 3$

63. In the example of Figure 3, the interleaver depth D is 3 bytes, and the codeword size I is 7 bytes. The large dots within the squares at the left-hand side of the figure represent bytes from previous codewords. To help with visualization of how convolutional interleaving works, the rows are depicted as never ending so that additional codewords can be added to each of the rows in sequence.

64. In order of left to right, the interleaved stream for the example convolutional interleaver shown in Figure 3 is

$B_0^1 \bullet \bullet B_1^1 B_0^2 \bullet B_2^1 B_1^2 B_0^3 B_3^1 B_2^2 B_1^3 B_4^1 B_3^2 B_2^3 B_5^1 B_4^2 B_3^3 B_6^1 B_5^2 B_4^3 \dots$

The bytes that were adjacent in the original data stream are separated by 3 bytes (the interleaver depth D) after interleaving.

65. Now if impulse noise corrupts the five consecutive bytes in the same location as shown above, the resulting interleaved stream of bytes is:

$B_0^1 \bullet \bullet B_1^1 B_0^2 \bullet B_2^1 B_1^2 B_0^3 B_3^1 B_2^2 X X X X X B_4^2 B_3^3 B_6^1 B_5^2 B_4^3 \dots$

When the bytes are deinterleaved, the resulting stream of codewords is:

$| B_0^1 B_1^1 B_2^1 B_3^1 X X B_6^1 | B_0^2 B_1^2 B_2^2 X B_4^2 B_5^2 B_6^2 | B_0^3 X X B_3^3 B_4^3 B_5^3 B_6^3 | \dots$

After the bytes have been returned to their original order, no codeword includes more than two bytes in error, and the Reed-Solomon code can correct all of the errors.

66. The process of interleaving in the transmitter and deinterleaving in the receiver introduces delay (or latency) because bytes are stored for a period of time after they are written to the interleaver or deinterleaver memory but before they are read out. All bytes have the same total delay between the input to the interleaver and the output of the deinterleaver, which is typically referred to as the *end-to-end interleaver delay* (with the understanding that the delay contributed by the deinterleaving process is included, too). In units of time, the end-to-end

interleaver delay depends on the rate at which the transmitter transmits bytes, i.e., the bit rate over the communication channel in the downstream direction, because that rate determines how quickly the transmitter processes the bytes for transmission.

67. The amount of memory needed for convolutional interleaving depends on how the interleaver and deinterleaver are implemented. The minimum amount of memory required for a convolutional interleaver and deinterleaver pair is $(D - 1) \times (I - 1)$ bytes.

68. The primary penalties for including interleaving in a communication system are increased latency (due to the end-to-end interleaver delay) and a requirement for additional memory in both the transmitter and receiver. The end-to-end interleaver delay increases with the interleaver depth. Therefore, there is a fundamental trade-off between latency and improved Reed-Solomon performance. A larger interleaver depth offers better potential to improve the performance of the Reed-Solomon coding but also increases latency.

C. Shared Memory

69. As I explain further in the prior art discussion below, the idea of a transceiver sharing a common memory for interleaving and deinterleaving was well known as of the Family 3 patents' priority date.

70. For convenience, I will sometimes distinguish in this report between a "near-end" transceiver and the "far-end" transceiver that is on the other side of a communication channel from the near-end transceiver. When the transmitter of a near-end transceiver performs interleaving, the transmitter needs to have access to an amount of memory sufficient for the transmitter to perform the interleaving procedure. Likewise, when the transmitter in the far-end transceiver performs interleaving, the near-end transceiver's receiver must have access to an amount of memory sufficient to enable it to deinterleave the data interleaved by the far-end transceiver's transmitter. And, of course, the far-end transceiver needs sufficient memory to

deinterleave the data transmitted by the near-end transmitter and to interleave the data it is transmitting to the near-end receiver.

71. There are two ways to provide the memory needed for a transceiver's interleaving and deinterleaving procedures. The first way is to provide a specified amount of dedicated interleaver memory and a specified amount of dedicated deinterleaver memory. The transmitter has exclusive access to the interleaver memory and can, at least in theory, use as much as all of the interleaver memory for interleaving. Similarly, the receiver has exclusive access to the deinterleaver memory and can, at least in theory, use as much as all of the deinterleaver memory for deinterleaving.

72. The second way to meet the transceiver's memory requirements for interleaving and deinterleaving is to provide shared memory that the transceiver can partition between its interleaver and deinterleaver on a per-connection basis. Use of a shared memory for interleaving and deinterleaving, including in DSL, was well known before the priority date of the Family 3 patents. *See, e.g.*, U.S. Patent Pub. No. 2005/0034046 by Berkmann *et al.* at Abstract (disclosing a “combined interleaving and deinterleaving circuit” with “data memory (RAM) for temporary storage of the data to be interleaved and deinterleaved”); U.S. Patent No. 6,707,822 to Fadavi-Ardekani *et al.* at Abstract (disclosing an “Interleave/De-Interleave Memory” that “is shared by multiple ADSL sessions and by the transmit and receive processes within an individual session”); U.S. Patent No. 6,381,728 to Kang at col. 5:35-38 (disclosing “double buffering [that] allows the channel interleaver memory to be used, along with the app memory, as the turbo deinterleaver memory”); U.S. Patent No. 7,269,208 to Mazzoni *et al.* at Abstract (disclosing memory having “a first memory space assigned to the interleaver and a second memory space assigned to the deinterleaver”); *id.* at col. 1:19-22 (“The present

invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system. . . .”); U.S. Patent No. 5,751,741 to Voith *et al.* at col. 4:47-50 (disclosing external interleave/deinterleave memory used by both transmitter for interleaving and receiver for deinterleaving); *id.* at col. 2:61-64 (“Generally, the present invention provides an ADSL transceiver. . . .”).

73. Once the shared memory has been partitioned between the transmitter’s interleaver and the receiver’s deinterleaver for a connection, the transmitter has exclusive access to the portion of the shared memory allocated for interleaving and can, at least in theory, use as much as all of that portion of the shared memory for interleaving. Similarly, the receiver has exclusive access to the portion of the shared memory allocated for deinterleaving and can, at least in theory, use as much as all of that portion of the shared memory for deinterleaving. When the connection terminates, the shared memory can thereafter be repartitioned, possibly differently, when new connections are established.

74. Because the interleaving procedure is performed by one transceiver, and the corresponding deinterleaving procedure is performed by a different transceiver, it is necessary for at least one of the transceivers to know the capabilities or requirements of the other transceiver in order to configure the interleaver (or deinterleaver). Otherwise, for example, the transceiver performing the interleaving procedure could use an interleave depth that requires more memory than is available to the transceiver performing the deinterleaving procedure.

75. For example, before the near-end transceiver can configure its interleaver, which establishes how much of the memory available for interleaving (in either a dedicated memory or shared memory) the transmitter will use, it needs to know something about the far-end transceiver’s deinterleaving capabilities; otherwise, the near-end transmitter could perform an

interleaving procedure that the far-end receiver is incapable of reversing (e.g., because it does not have sufficient memory). In addition, before the near-end transceiver can configure its deinterleaver, which establishes how much of the memory available for deinterleaving (in either a dedicated memory or shared memory) the receiver will use, it needs to know how the far-end transceiver will be interleaving the data; otherwise, the near-end receiver will be unable to perform the corresponding deinterleaving procedure.

76. As discussed below, since 1995, the ADSL and VDSL standards have provided for the near-end and far-end transceivers to communicate their interleaving requirements and/or capabilities to each other during an initialization procedure.

D. Latency Paths

77. Different types of data have different levels of sensitivity to delays that occur during transmission. For example, real-time voice data, such as from a telephone call, cannot tolerate large delays because delays in conversations are very annoying for the participants. In contrast, a pre-stored (i.e., non-real-time) video transmitted to a receiver (e.g., via YouTube, Netflix, HBO Go, etc.) can tolerate a substantial amount of delay because the local video playback device typically buffers at least some of the video before playing it.

78. To enable the transmission of both delay-sensitive and delay-tolerant data over the same subscriber line, the ADSL and VDSL standards, discussed below, define multiple *latency paths* that allow a single DSL connection to transfer multiple types of data having different latency requirements (or delay tolerances) at the same time. Each latency path is characterized by a distinct delay (or latency), which may be the same as or different from the delay(s) of other latency paths. For example, one latency path may be characterized by a relatively large delay because of interleaving in the transmitter and deinterleaving in the

receiver, whereas another latency path may be characterized by a relatively small delay because of little or no interleaving.

79. The delay of a particular latency path depends on the FEC and interleaving used in that path. For example, when a latency path includes both FEC and interleaving, the delay depends on the codeword size and the interleave depth.

E. Overview of DSL Standards Groups

80. Many of the aspects of ADSL and VDSL have been standardized by standard-setting organizations (SSOs), such as the Alliance for Telecommunications Industry Solutions (ATIS) and the International Telecommunications Union (ITU). This section introduces two of the working groups and the standards they produced that are relevant to the subject matter of this case and pre-date the priority date of the Family 3 patents. It also provides a brief overview of how the work in the responsible working groups is conducted.

1. T1E1.4

81. The earliest standardization work in ADSL was undertaken in the United States by the T1E1.4 technical subcommittee of Committee T1, a telecommunications standards body sponsored by ATIS and accredited by the American National Standards Institute (ANSI).

82. In 1995, ATIS published the world's first ADSL standard, T1.413. I will refer to the first version of the T1.413 standard herein as "T1.413 Issue 1." In 1998, ATIS published a revision of T1.413, which I will refer to as "T1.413 Issue 2." Both T1.413 Issue 1 and T1.413 Issue 2 specify the required operations of ADSL transceivers (referred to as the "ATU-C" and "ATU-R").

83. After releasing T1.413 Issue 2 ADSL, T1E1.4 focused less on developing stand-alone transceiver standards and more on providing inputs to the ITU-T, discussed below, regarding North American requirements and preferences for emerging DSL standards.

2. ITU-T Study Group 15, Question 4

84. In 1997, the Telecommunications Sector of the ITU, known as the ITU-T, also began working on ADSL standardization. The ITU-T generates standards called “Recommendations” for all fields of telecommunications. Recommendations are the result of work by members of the ITU-T, which include Member States (e.g., the United States and other members of the United Nations), Sector Members, and Associates. Sector Members and Associates are generally companies and other organizations.

85. DSL standardization is carried out by Study Group 15 of the ITU-T. The work of Study Group 15 is partitioned into work areas known as “Questions.” DSL standardization work takes place within Study Group 15, Question 4 (abbreviated herein as “SG15/Q4”). SG15/Q4 became the primary group responsible for defining DSL transceiver standards after T1E1.4 completed T1.413 Issue 2.

86. The ITU-T’s DSL Recommendations are primarily aimed at defining mandatory and optional functions of DSL transceivers. In 1997, among other projects, SG15/Q4 established the projects known as “G.dmt” and “G.lite.” At that time, T1.413 Issue 1 was in force, and T1E1.4 was developing what eventually became T1.413 Issue 2 ADSL. G.dmt was expected essentially to adopt T1.413 Issue 2 and add annexes addressing country-specific requirements. The work in G.dmt was eventually released in 1999 as ITU-T Recommendation G.992.1, entitled “Asymmetric digital subscriber line (ADSL) transceivers,” much of which is identical to T1.413 Issue 2. G.992.1 specifies requirements for both the ATU-C and the ATU-R to enable connections that support at least 6.144 Mbit/s in the downstream direction (i.e., toward the subscriber, from the ATU-C to the ATU-R) and at least 640 kbit/s in the upstream direction (i.e., away from the subscriber, from the ATU-R to the ATU-C) without interfering with “plain old telephone signals” (POTS) on the same subscriber line.

87. G.lite was intended to be a lower-speed version of ADSL. The work in G.lite was eventually released, also in 1999, as ITU-T Recommendation G.992.2, entitled “Splitterless asymmetric digital subscriber line (ADSL) transceivers.” Unlike G.992.1, which was designed to maximize performance, G.992.2 was designed to provide lower bit rates (i.e., a maximum of 1.536 Mbit/s downstream and 512 kbit/s upstream) by simplifying various aspects of the ATU-C and ATU-R.

88. After completing G.992.1, SG15/Q4 almost immediately began work on a revision, standardized in Recommendation G.992.3, entitled “Asymmetric digital subscriber line transceivers 2 (ADSL2),” the first version of which was approved in 2002. G.992.3 builds on many of the aspects of G.992.1 to enable connections that support at least 8 Mbit/s downstream and at least 800 kbit/s upstream.

89. In parallel with the work on ADSL2, SG15/Q4 also worked on a higher speed version of ADSL, known as ADSL2+. Recommendation G.992.5, entitled “Asymmetric Digital Subscriber Line (ADSL) transceivers – Extended bandwidth ADSL2 (ADSL2+),” was first approved in 2003. It specifies the physical layer characteristics of an ADSL transceiver that transmits over a wider bandwidth than an ADSL2 transceiver. G.992.5 is defined in a “delta document” to G.992.3, meaning that it incorporates the content of G.992.3 and specifies only changes and additions to that document. As compared to G.992.3, G.992.5 enables transceivers to transmit using twice as much bandwidth in the downstream direction to provide at least 16 Mbit/s in the downstream direction and at least 800 kbit/s in the upstream direction.

90. In June of 2004, the ITU-T’s first VDSL Recommendation, G.993.1, entitled “Very high speed digital subscriber line transceivers,” was approved. It specifies transceiver

requirements to support the transmission of asymmetric and symmetric aggregate data rates up to tens of Mbit/s on twisted pairs.

3. Operation of DSL Standards Meetings

91. Both T1E1.4 and SG15/Q4 met regularly, typically 4 to 6 times per year, to begin work on new DSL standards, to discuss and improve the draft standards being developed at the time, and eventually to submit the standards for formal approval. In order to develop and improve the standards, T1E1.4 and SG15/Q4 participants submitted documents, referred to as “contributions.” A contribution might identify a problem with an in-force standard and propose a solution for incorporation in a revision of that standard, or it might propose a new feature for a standard being developed, or it might propose to begin work on a new standard.

92. Each T1E1.4 contribution was assigned a unique identifier of the form “T1E1.4/YY-NNN” or “T1E1.4/YYYY-NNN,” where “YY” or “YYYY” indicates the year, and “NNN” is a unique 3-digit number. The unique 3-digit number would reset to 001 at the beginning of each year. Each SG15/Q4 contribution is assigned a unique identifier of the form “MM-NNN,” where “MM” is a 2-letter designator reflecting the location of the meeting (e.g., “DC” stands for “Durango, Colorado,” “LB” stands for “Leuven, Belgium,” etc.), and “NNN” is a unique 3-digit number. The unique 3-digit number resets to 001 for each SG15/Q4 meeting.

93. One unique aspect of T1E1.4, relative to many other SSO working groups, was that prior to 2004, its meetings were open to members of the public, and the contributions distributed to meeting participants and/or posted on Committee T1’s website were freely available to the public without any distribution restrictions. Thus, any member of the public could attend T1E1.4 meetings free of charge and obtain copies of the contributions submitted to that meeting. Members of the public could also download contributions from Committee T1’s website. Meetings of T1E1.4 were typically held in the United States.

94. SG15/Q4 meetings were (and are) open to and attended by members of the ITU-T. ITU-T membership was (and is) available to interested companies and organizations for an annual fee that, as of June of 2004, was 10,500 Swiss francs.² I personally attended SG15/Q4 meetings starting in 2000,³ and I recall the meetings being attended by most of the companies developing DSL chips and transceivers, as well as the service providers deploying DSL.⁴

F. Interleaving and FEC in DSL Standards

95. As explained above, interleaving and FEC, and specifically the use of Reed-Solomon coding, have been specified for ADSL since the first ADSL standard, T1.413 Issue 1, was completed in 1995. Each of the subsequent ADSL and VDSL standards released before the Family 3 patents' priority date also specifies interleaving, FEC, and protocols to enable the near-end and far-end transceivers to inform each other of their capabilities and/or requirements during the initialization procedure.

² See <https://web.archive.org/web/20040603123217/http://www.itu.int:80/ITU-T/membership/associates.html> (last visited November 16, 2018).

³ I attended SG15/Q4 on behalf of Texas Instruments until May of 2004 and on behalf of 2Wire from August of 2004 through June of 2006.

⁴ According to the Internet Archive, as of December 6, 2000 the ITU-T members included, among others: 3Com, ADTRAN, Alcatel, Analog Devices, AT&T, Aware, Bell Atlantic, Bell Canada, Bell South, Broadcom, British Telecom, Burr-Brown Corporation, Catena Networks, Centillium Communications, Cisco Systems, Conexant Systems, Copper Mountain Networks, Covad Communications, Element 14, Ericsson, Excess Bandwidth Corporation, France Telecom, Fujitsu, Globespan, Infineon, Italtel, Legerity, Level One, LG Electronics, Lucent, Marconi Communications, Matsushita, Metalink, Mitel Corporation, Mitsubishi, Motorola, NEC, Next Level Communications, Nokia, Nortel Networks, NTT, PairGain, Paradyne Corporation, Philips, PMC-Sierra, Qwest, Sagem, Sasken, SBC Communications, Siemens, Sprint, STMicroelectronics, Sumitomo, Swisscom, Telcordia, Telecom Italia, Telenor, Telesis Technologies Laboratory, Telia, Tellabs, Texas Instruments, VDSL Systems, Verizon, Velocity Communication (later renamed Ikanos), and Virata. See https://web.archive.org/web/20001206175700/http://www.itu.int:80/cgi-bin/htsh/mm/scripts/mm.list?_search=SEC%26_languageid=1 (last visited November 16, 2018).

1. Nomenclature

96. In ADSL, one transceiver is located on the service provider's side of the subscriber line, often in the service provider's central office (CO), and the other transceiver is located on the customer's side of the subscriber line. The ADSL transceiver located on the service provider's side of the subscriber line is referred to as the "ATU-C," and the ADSL transceiver located on the customer's side of the subscriber line is referred to as the "ATU-R."

97. In VDSL, one transceiver is located on the service provider's side of the subscriber line, potentially in an optical network unit (ONU), and the other transceiver is located on the customer's side of the subscriber line. The VDSL transceiver located on the service provider's side of the subscriber line is referred to as the "VTU-O," and the VDSL transceiver located on the customer's side of the subscriber line is referred to as the "VTU-R."

98. The direction of transmission from the ATU-C (or VTU-O) to the ATU-R (or VTU-R) is the *downstream* direction, and the direction of transmission from the ATU-R (or VTU-R) to the ATU-C (or VTU-O) is the *upstream* direction.

99. If interleaving is used in both the upstream and downstream directions in ADSL, both the ATU-C and ATU-R use both an interleaver and a deinterleaver. The ATU-R interleaves upstream data (for transmission to the ATU-C) and deinterleaves downstream data (interleaved by and received from the ATU-C). Conversely, the ATU-C interleaves downstream data (for transmission to the ATU-R) and deinterleaves upstream data (interleaved by and received from the ATU-R).

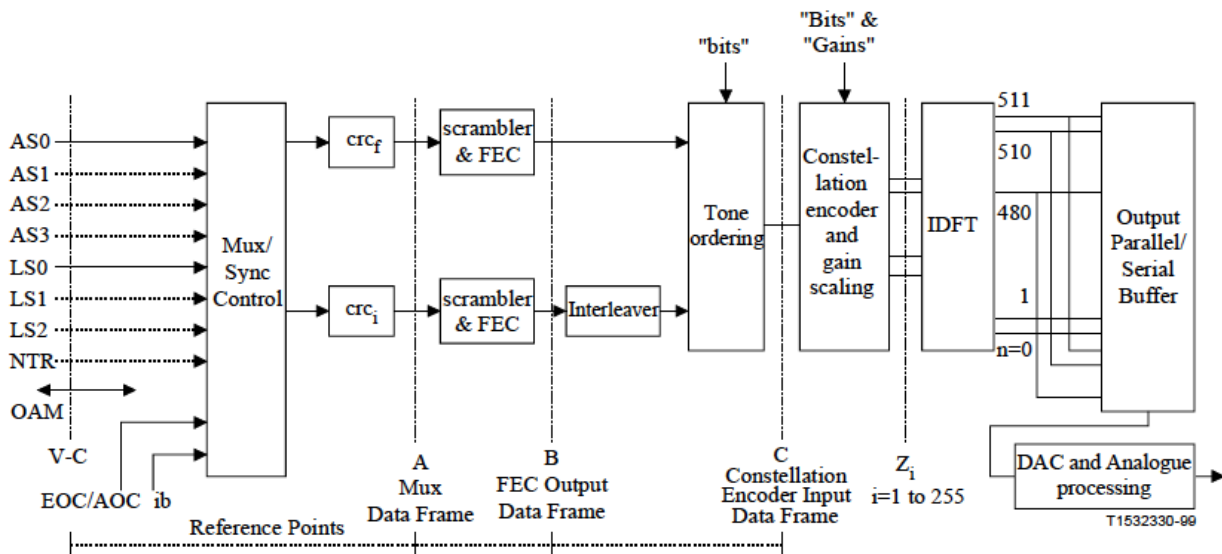
100. Similarly, in VDSL, if interleaving is used in both the upstream and downstream directions, both the VTU-O and VTU-R use both an interleaver and a deinterleaver. The VTU-R interleaves upstream data (for transmission to the VTU-O) and deinterleaves downstream data (interleaved by and received from the VTU-O). Conversely, the VTU-O interleaves

downstream data (for transmission to the VTU-R) and deinterleaves upstream data (interleaved by and received from the VTU-R).

2. G.992.1 (1999)

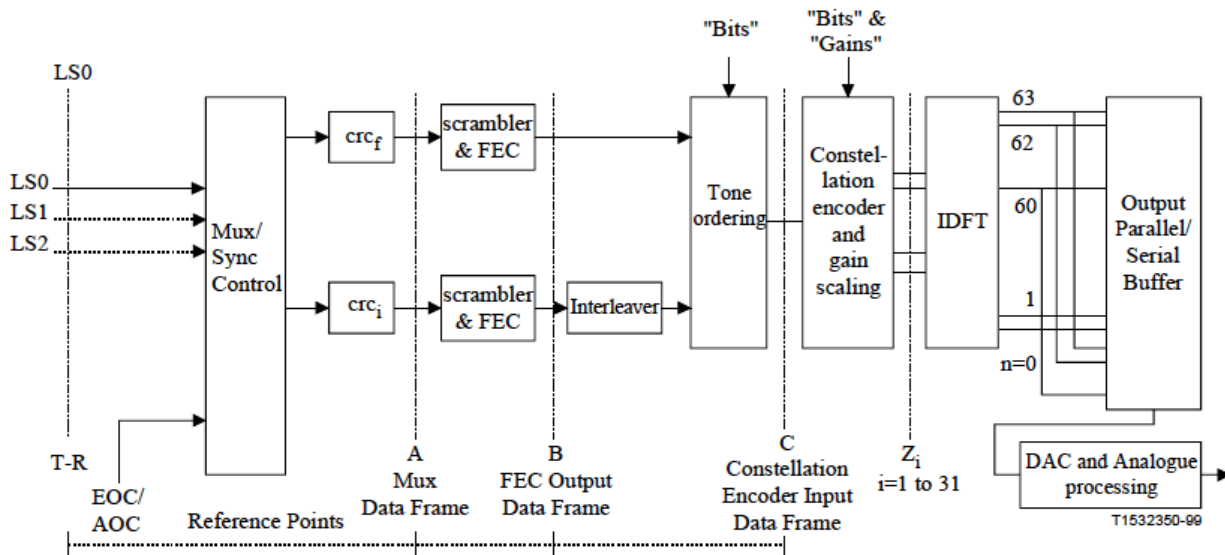
101. G.992.1 specifies dual-latency configurations using two independent data paths in both the downstream and upstream directions. G.992.1 also supports a single-latency configuration, which may include interleaving.

102. Figure 5-1 of G.992.1, copied below, is a reference diagram for the ATU-C, and Figure 5-3 of G.992.1, also copied below, is a reference diagram for the ATU-R.



NOTE – Solid versus dashed lines are used to indicate required versus optional capabilities respectively. This figure is not intended to be complete in this respect, see clauses 6 and 7 for specific details.

Figure 5-1/G.992.1 – ATU-C transmitter reference model for STM transport



NOTE – Solid versus dashed lines are used to indicate required versus optional capabilities respectively. This figure is not intended to be complete in this respect, see clauses 6 and 8 for specific details.

Figure 5-3/G.992.1 – ATU-R transmitter reference model for STM transport

In the downstream direction, there are up to two latency paths (fast and interleaved), and in the upstream direction there are also up to two latency paths (fast and interleaved), resulting in a total of four possible latency paths overall. When a single latency path is supported in one of the directions of transmission, it may use either the fast or interleaved path.

103. The key difference between the fast and interleaved paths in G.992.1 is that data in the interleaved path is both FEC encoded (using Reed-Solomon coding) and interleaved, as described previously, to improve the effectiveness of the FEC code in the presence of impulse noise. In contrast, the fast path includes FEC coding, but does not include interleaving. Therefore, the fast path has lower latency than the interleaved path, but it is also more likely to suffer from a higher error rate in the presence of impulse noise.

104. Each FEC codeword has a length of some number of bytes (i.e., N , K , and R all have units of bytes), which can be different for the fast and interleaved paths and in the downstream and upstream directions. The value of K depends on the transmitted bit rate (i.e.,

the rate at which the transmitter sends bits to the receiver on the other side of the subscriber line). The values of N , K , and R are set during the initialization procedure (with $N = K + R$).

105. G.992.1 specifies the interleave depth for the interleaved path as a number of FEC codewords.

106. During the initialization procedure, the ATU-C transmits four options for data rates and formats to the ATU-R using a signal known as “C-RATES1.” Each of the options includes downstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-C proposes to do for each option) and upstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-R will need to do for each of the options). G.992.1 at § 10.6.2. The ATU-R responds by transmitting a signal known as “R-RATES1,” in which the ATU-R echoes the four options in the order in which the ATU-R prefers them. G.992.1 at § 10.7.4.

107. Figure 10-4 of G.992.1, copied below, shows the timing of the messages transmitted by the ATU-C and ATU-R during the “exchange” phase of initialization, which follows the transmission of the C-RATES1 and R-RATES1 messages.

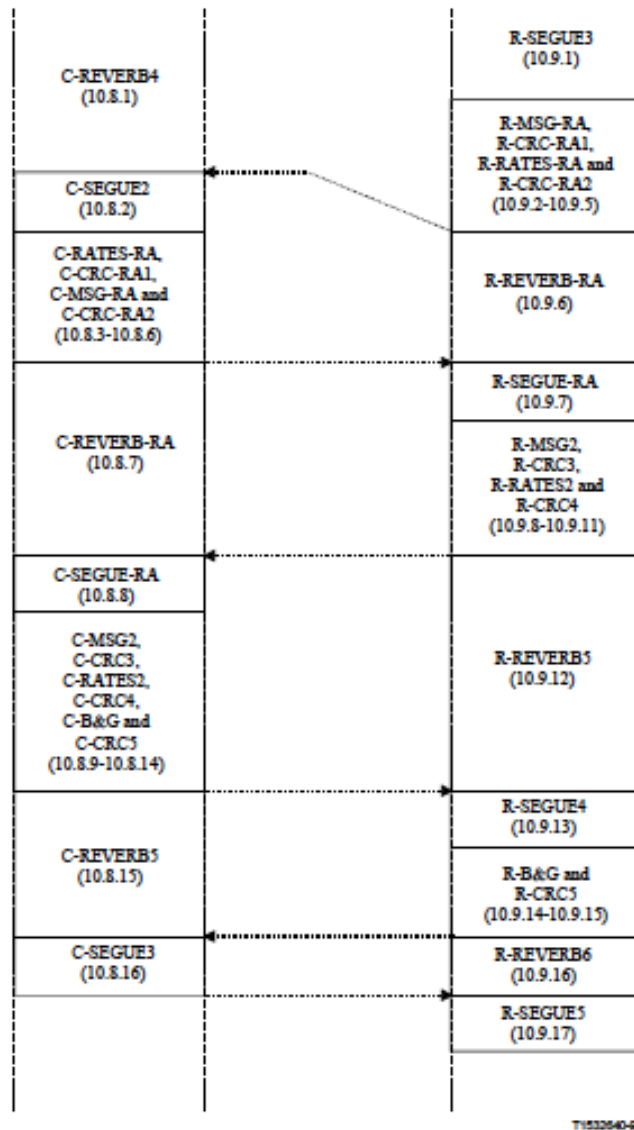


Figure 10-4/G.992.1 – Timing diagram of exchange

108. After transmitting R-RATES1 and measuring the signal-to-noise ratio (SNR) of the downstream channel, the ATU-R transmits a signal called “R-MSG-RA,” which tells the ATU-C, among other things, the maximum interleave depth the ATU-R can support. G.992.1 at §§ 10.9.2, 10.9.2.7. The ATU-R also transmits a signal called “R-RATES-RA,” which indicates either (a) the option number of the highest data rate from C-RATES1 that can be supported based on the measured SNR in the downstream direction, (b) no option selection was made but will be made later based on information in the C-RATES-RA signal the ATU-C will

transmit, or (c) the ATU-R cannot implement any of the options received in C-RATES1.

G.992.1 at § 10.9.4.

109. After receiving R-MSG-RA and R-RATES-RA, the ATU-C transmits a signal called “C-RATES-RA,” which sends four new options for data rates and formats for both upstream and downstream transmission. G.992.1 at § 10.8.3. As in C-RATES1, each of the options includes downstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-C proposes to do for each option) and upstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-R will need to do for each of the options). G.992.1 at § 10.8.3.

110. After receiving C-RATES-RA, the ATU-R transmits R-RATES2, which selects only the number of the option with the highest data rate that can be supported in the downstream direction based on the ATU-R’s measurements of the channel. G.992.1 at § 10.9.10. The ATU-C then transmits C-RATES2, which indicates the final decision on the downstream and upstream options that will be used for the connection. G.992.1 at § 10.8.11. The ATU-C’s decision combines the downstream option selected by the ATU-R with the option number with the highest upstream data rate that can be supported based on the ATU-C’s measurements of the channel. G.992.1 at § 10.8.11.

3. G.992.2 (1999)

111. G.992.2 specifies requirements and functions of ADSL transceivers intended to operate without the splitter filters required in G.992.1 to isolate ADSL signals from telephony signals on the same subscriber line. G.992.2 at Summary. Figure 2 of G.992.2, copied below, is the reference model for G.992.2 transmitters (both ATU-C and ATU-R).

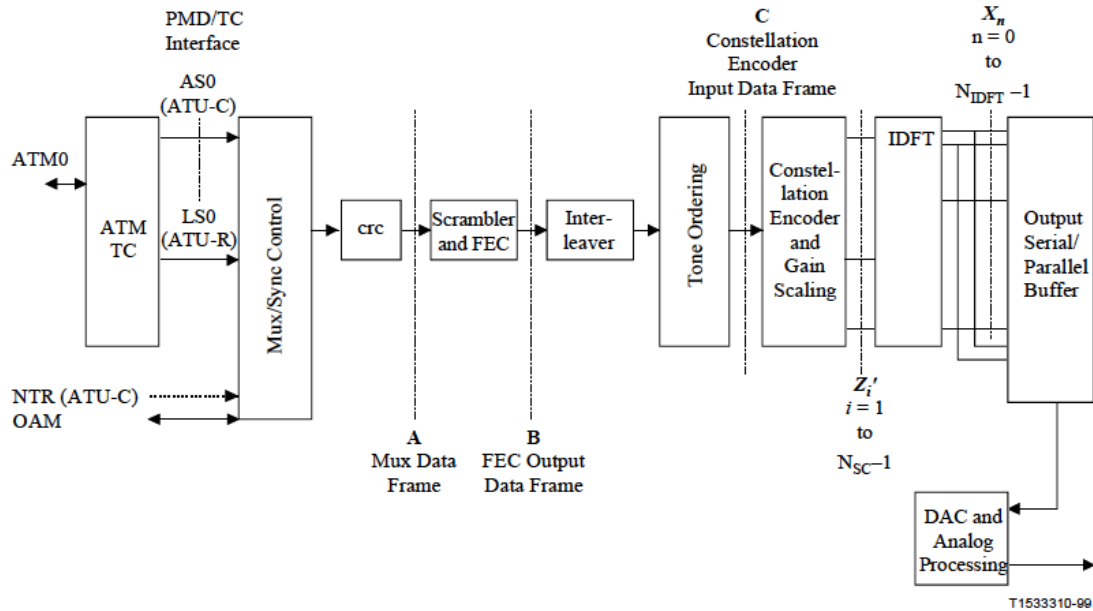


Figure 2/G.992.2 – ATU reference transmitter model

112. G.992.2 is similar to G.992.1 in how it handles the selection and communication of FEC and interleaver settings during the initialization procedure. The ATU-C transmits C-RATES1, which contains four options, in order of decreasing preference, for downstream and upstream data rates and formats. G.992.2 at § 11.9.2. Each option contains Reed-Solomon FEC and interleaver parameters, such as the downstream interleave depth in codewords. G.992.2 at § 11.9.2. The ATU-R responds by sending R-RATES1, in which the ATU-R echoes the four options received from the ATU-C in order of decreasing preference. G.992.2 at § 11.10.4.

113. Figure 26 of G.992.2, copied below, shows the “exchange” phase of initialization, which takes place after the ATU-C and ATU-R have transmitted, respectively, C-RATES1 and R-RATES1.

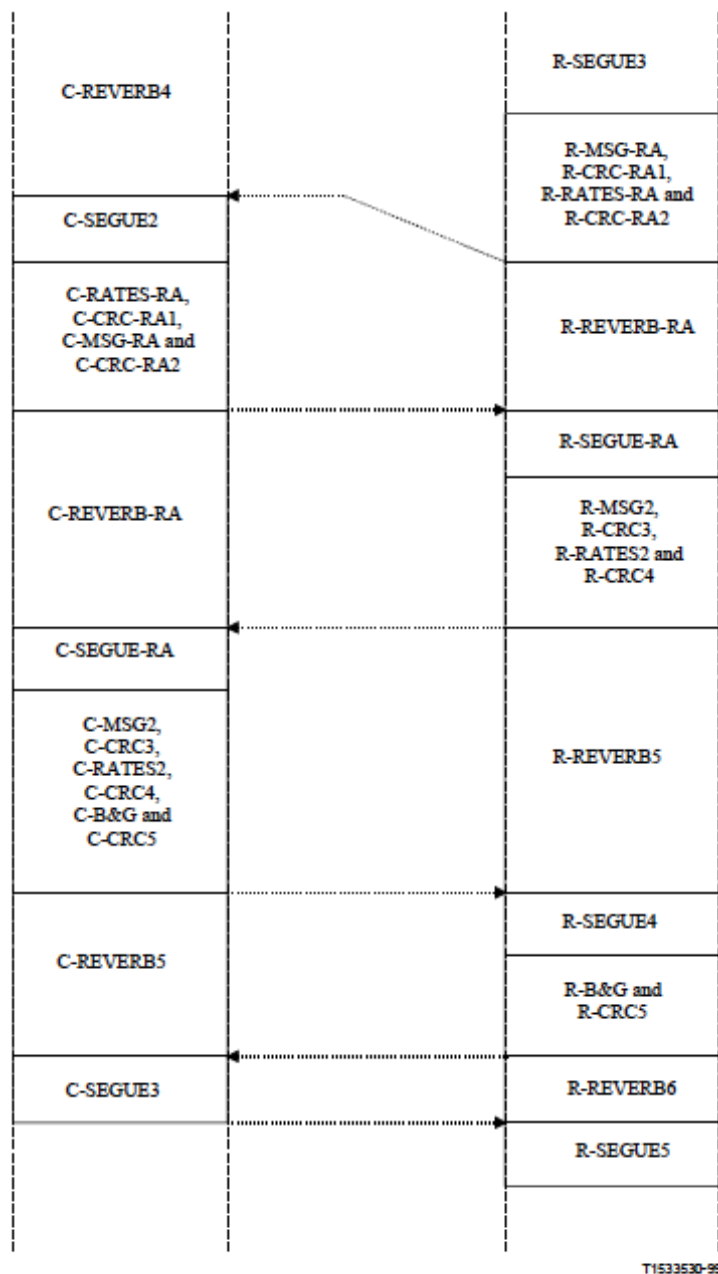


Figure 26/G.992.2 – Timing diagram of exchange

114. After assessing the channel, the ATU-R sends R-MSG-RA, which includes, among other things, a number of Reed-Solomon overhead bytes (R) and a number of Reed-Solomon payload bytes (K). G.992.2 at § 11.12.2. The ATU-R also sends R-RATES-RA, which indicates either (a) the option number of the highest data rate sent in C-RATES1 that can be supported based on the measured SNR in the downstream direction, (b) no option selection

was made but will be made later based on information in the C-RATES-RA signal the ATU-C will transmit, or (c) the ATU-R cannot implement any of the options received in C-RATES1. G.992.2 at § 11.12.4.

115. The ATU-C then transmits C-RATES-RA, which contains four new options for data rates and formats for both upstream and downstream transmission. G.992.2 at § 11.11.3. As in C-RATES1, each of the options includes downstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-C proposes to do for each option) and upstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-R will need to do for each of the options). G.992.2 at § 11.11.3.

116. In response to C-RATES-RA, the ATU-R transmits R-RATES2, which selects only the number of the option with the highest data rate that can be supported in the downstream direction based on the ATU-R's measurements of the channel. G.992.2 at § 11.12.10. The ATU-C then transmits C-RATES2, which indicates the final decision on the downstream and upstream options that will be used for the connection. G.992.2 at § 11.11.11. The ATU-C's decision combines the downstream option selected by the ATU-R with the option number with the highest upstream data rate that can be supported based on the ATU-C's measurements of the channel. G.992.2 at § 11.11.11.

4. G.993.1 (2004)

117. ITU-T Recommendation G.993.1 specifies aspects of very high-speed digital subscriber lines (VDSL) to permit the transmission of asymmetric and symmetric aggregate data rates up to tens of Mbit/s on twisted pairs. G.993.1 provides for use of a wider bandwidth than is used in ADSL, namely, up to 12 MHz. G.993.1 at § 1.

118. Among other things, G.993.1 specifies the use of FEC and interleaving in the transmitter. Figure 8-1 of G.993.1, copied below, illustrates the defined “slow” and “fast” paths. As shown, the “slow” path includes both FEC and interleaving, whereas the “fast” path includes FEC but not interleaving.

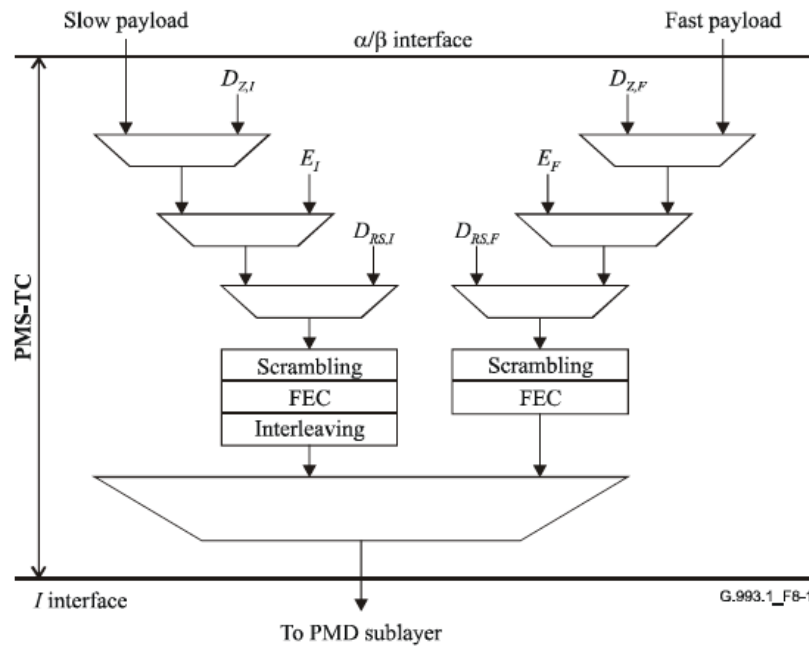


Figure 8-1/G.993.1 – Diagram of PMS-TC sublayer

119. G.993.1 specifies the use of “a standard byte-oriented Reed-Solomon code . . . to provide protection against random and burst errors” (G.993.1 at § 8.3) and interleaving “to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords.” G.993.1 at § 8.4.1. Specifically, “the codewords shall be interleaved before transmission to increase the immunity of RS [Reed-Solomon] codewords to bursts of errors.” G.993.1 at § 8.4.1. The interleave depth is programmable up to a maximum depth of 64 codewords when the codeword length is 255 bytes. *Id.* When the codeword is shorter than 255 bytes, the interleave depth can be larger than 64 codewords. *Id.*

120. G.993.1 specifies that “[i]t shall be possible to adjust the interleave depth via the management system to meet latency requirements.” *Id.* The interleaver “uses a memory in which a block of I octets is written while an (interleaved) block of I octets is read.” *Id.* G.993.1 teaches that the receiver requires the same size of memory for deinterleaving as the transmitter uses for interleaving. *Id.*

121. G.993.1 specifies an initialization procedure to allow the VTU-O and VTU-R to, among other things, exchange parameters such as Reed-Solomon settings and interleaver parameters. G.993.1 at § 12.4.1. Figure 12-7 of G.993.1, copied below, illustrates the timing of messages transmitted by the VTU-O and VTU-R during the channel analysis and exchange phase of VDSL initialization.

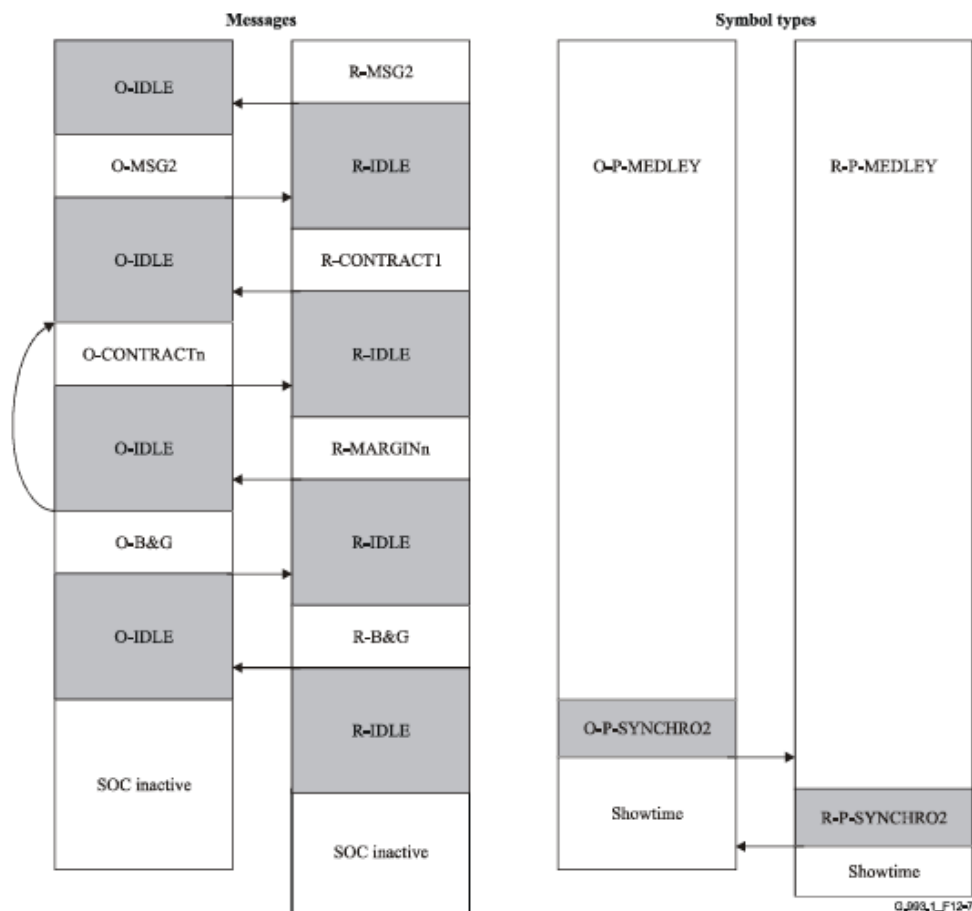


Figure 12-7/G.993.1 – Timeline of the channel analysis and exchange phase

122. During the channel analysis and exchange phase, the VTU-R sends a message called R-MSG2, which transfers, among other things, the Reed-Solomon capabilities of the VTU-R (e.g., whether it can support only mandatory settings or all settings), the interleaver settings supported by the VTU-R (e.g., whether it can support only mandatory settings, all settings, or a number of additional settings), and the “maximal interleaver memory” in bytes. *Id.* at § 12.4.6.1; § 12.4.6.3.1.1.

123. After receiving R-MSG2, the VTU-O sends a message called O-MSG2, which transfers, among other things, the Reed-Solomon capabilities of the VTU-O (e.g., whether it can support only mandatory settings or all settings), the interleaver settings supported by the VTU-O (e.g., whether it can support only mandatory settings, all settings, or a number of additional settings), and the “maximum interleaver delay” in milliseconds. *Id.* at § 12.4.6.1; § 12.4.6.2.1.1.

124. After receiving O-MSG2, the VTU-R sends a message called R-CONTRACT1, which contains “the proposed downstream contract based on the maximal number of bits in the slow channel based on the restrictions specified in O-MSG2 (i.e., as if only the slow channel will be used).” *Id.* at § 12.4.6.3.1.2. The proposed downstream contract specifies, among other things, the bit rate for the slow channel (a multiple of 64 kbit/s), the Reed-Solomon settings for the slow channel (i.e., the codeword length and number of redundancy bytes), and the interleaver setting (i.e., the interleaver depth and block length). *Id.* at § 12.4.6.3.1.2; § 12.4.6.2.1.2.

125. After receiving R-CONTRACT1, the VTU-O sends a message called O-CONTRACTn, which contains a proposed upstream and downstream contract that is based on the capabilities of the VTU-O and VTU-R. G.993.1 at § 12.4.6.2.1.2. The downstream portion of the contract is based on the information provided by the VTU-R in R-CONTRACT1 and,

ideally, is the same as the contract the VTU-R proposed in R-CONTRACT1. *Id.* Both the upstream and downstream portions of the proposed contract include, among other things, the bit rate for the slow channel (a multiple of 64 kbit/s), the Reed-Solomon settings for the slow channel (i.e., the codeword length and number of redundancy bytes), and the interleaver setting (i.e., the interleaver depth and block length). *Id.*

G. The Family 3 Patents

126. The Family 3 patents claim the benefit of U.S. provisional application No. 60/618,269, filed on October 12, 2004. They share a common written description and have the same drawings. Therefore, my references herein will be to the '882 patent.

127. The asserted claims of the Family 3 patents are generally directed to methods, systems, and apparatuses for allocating shared memory between transmitter and/or receiver latency paths. '882 patent at col. 4:1-3. The transmitter and receiver latency paths can share an interleaver/deinterleaver memory, which can be allocated to the transmitter's interleaver and to the receiver's deinterleaver. *Id.* at col. 4:5-9; col. 9:18-21. The allocation of the shared memory can be based on the data rate, latency, bit error ratio (BER), impulse noise protection requirements, or "any parameter associated with the communications system." *Id.* at col. 4:9-13; *see also id.* at col. 5:22-27. FIG. 1 of the Family 3 patents, copied below, illustrates, among other things, a transceiver with two latency paths in the transmit direction (210, 220), each including an interleaver (216, 226); two latency paths in the receive direction (310, 320), each including a deinterleaver (316, 326); and a shared memory (120). *Id.* at col. 4:41-56. The shared memory can be allocated to an interleaver and deinterleaver (*id.* at col. 5:33-39), to multiple interleavers in the transmitter (*id.* at col. 5:40-46), or to multiple deinterleavers in the receiver (*id.* at col. 5:47-53).

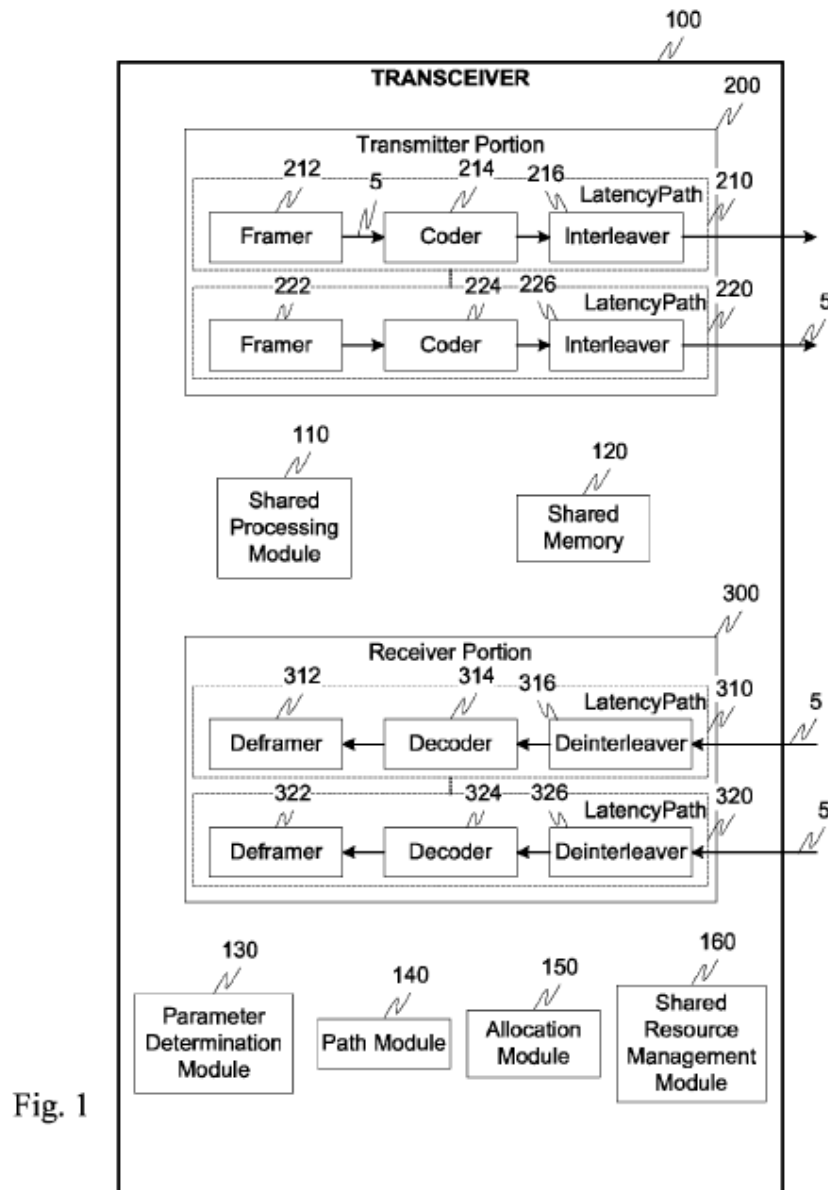


Fig. 1

128. Based on parameters such as data rate, impulse noise protection, bit error rate, or latency, the allocation module 150 allocates a portion of the shared memory 120 to the interleaver(s) and/or deinterleaver(s) in each of the latency paths. *Id.* at col. 5:62-6:3. After determining the memory allocation for each of the latency paths, “the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.” *Id.* at col. 6:4-11.

129. The Family 3 patents also disclose transmitting framing, coding, and interleaving information from one transceiver to another during initialization or thereafter. *Id.* at col. 7:50-59. In one embodiment, a first modem determines framing, coding, and interleaving parameters to meet application requirements such as latency, burst error correction capability, etc. *Id.* at col. 7:60-63. To do so, “the first modem must know what are the capabilities of a second modem.” *Id.* at col. 64-66. Specifically, “the first modem must know” (1) how many latency paths the second modem can support, (2) the maximum amount of interleaver memory for each transmitter latency path, and (3) the total shared memory for all transmitter latency paths. *Id.* at col. 7:66-8:5. The first modem uses this information to “choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.” *Id.* at col. 8:5-8.

130. The Family 3 patents provide an example in which a first transceiver sends a message to a second transceiver indicating the number of supported transmitter and receiver latency paths, the maximum interleaver memory for each of the latency paths, and the maximum total or shared memory for all of the latency paths. *Id.* at col. 8:9-19. The first transceiver then selects settings (i.e., Reed-Solomon parameter values N and R , and the interleaver depth, D) for each of the latency paths. *Id.* at col. 8:21-22.

131. FIG. 3 of the Family 3 patents, copied below, shows a method of exchanging shared resource allocations.

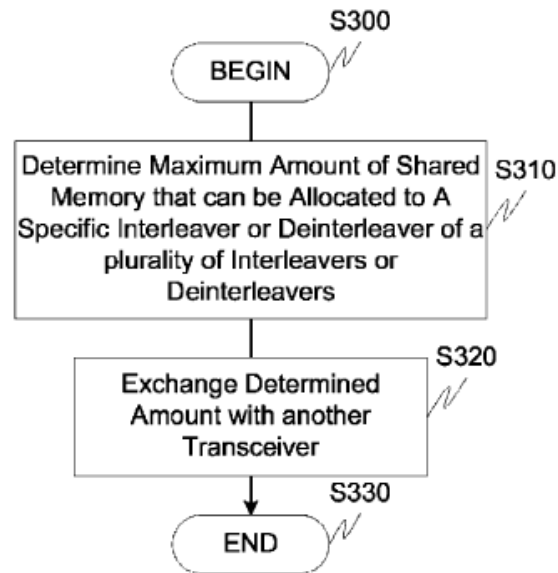


Fig. 3

At step S310, the “maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers and deinterleavers in a transceiver is determined.” *Id.* at col. 8:62-66. The determined maximum amount for one or more interleavers/deinterleavers is then transmitted to another transceiver in step S320. *Id.* at col. 8:66-9:1. The transceiver can also transmit and/or receive “messages containing additional information,” although the Family 3 patents do not provide any examples of such “additional information.” *Id.* at col. 9:1-3.

1. Asserted Claims Family 3 Patents

132. The asserted claims of the Family 3 patents are claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent. For convenience, I have given each of the claim elements an identifier, which I use through the rest of this report.

133. Claim 1 of the '048 patent recites:

- 1[a]. A system that allocates shared memory comprising:
- [b] a transceiver that is capable of:

[c] transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

[d] determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

[e] allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate,

[f] wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

[g] allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

[h] interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver,

[i] wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

As corrected by the certificate of correction⁵ issued on February 8, 2011, claim 5 of the '381 patent recites:

5[a]. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

[b] transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

⁵ As more particularly described below, following the issuance of both the '381 and '882 patents, the applicant requested and received Certificates of Correction pursuant to 35 U.S.C. § 235 as a result of typographical errors introduced by the applicant related to three limitations included in claims 5 and 13 of those patents, respectively. I have indicated the changes effected by the Certificates of Correction by using strike-through of the language as it appeared originally in the claims, and brackets for the language as corrected.

[c] determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

[d] allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ~~transmission~~ [reception] at a first data rate,

[e] wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

[f] allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes ~~received~~ [transmitted] at a second data rate; and

[g] deinterleaving the first plurality of RS coded data bytes within the ~~shared~~-[shared] memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver,

[h] wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

As corrected by the certificate of correction issued on May 3, 2011, claim 13 of the '882 patent recites:

13[a]. A system that allocates shared memory comprising:

[b] a transceiver that performs:

[c] transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

[d] determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

[e] allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ~~transmission~~ [reception] at a first data rate,

[f] wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

[g] allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes ~~received~~ [transmitted] at a second data rate; and

[h] deinterleaving the first plurality of RS coded data bytes within the ~~shared~~ [shared] memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver,

[i] wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

Claim 19 of the '473 patent recites:

19[a]. An apparatus comprising:

[b] a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path,

[c] the multicarrier communications transceiver being associated with a memory,

[d] wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and

[e] wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

2. Provisional Application

134. I reviewed the provisional application of which the Family 3 patents claim the benefit, namely U.S. provisional application No. 60/618,269 (“the ’269 provisional”), filed on October 12, 2004, to determine whether the asserted claims are entitled to a priority date of October 12, 2004. I concluded that they are not.

135. Claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 1 of the '048 patent all require shared memory, “wherein the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver].” I do not see any disclosure of this element in the '269 provisional, and therefore, in my opinion, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 1 of the '048 patent are not entitled to a priority date of October 12, 2004.

136. Claim 19 of the '473 patent requires that “the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.” I do not see any disclosure of this element in the '269 provisional. The '269 provisional discloses a receiver deciding how a transmitter will split interleaving memory between multiple interleavers (but not deinterleavers) and states that “an essential aspect of this invention [is] that prior to configuring the FCI blocks the transmitting modem must send a message to the receiving modem containing **information describing the total/shared memory of the transmit FCI blocks.**” '269 provisional at 5 (emphasis added). As an alternative approach, the '269 provisional describes the receiving modem sending a message to the transmitting modem to allow the transmitter to determine the transmit FCI configuration, in which case “it is an essential aspect of this invention that prior to configuring the FCI blocks the receiving modem must send a message to the transmitting modem containing **information describing the total/shared memory of the receive FCI blocks.**” '269 provisional at 5 (emphasis added). When it describes a transceiver sharing interleaver memory “between the transmitting and receiving portions of a single modem,” however, the '269 provisional does not disclose the transceiver performing any allocation of memory between an interleaving function and a deinterleaving function in accordance with a message received

during an initialization of the transceiver. '269 provisional at 5. Therefore, in my opinion, claim 19 of the '473 patent is not entitled to a priority date of October 12, 2004.

3. File History

137. The Family 3 patents claim priority to Provisional Application No. 60/618,629, filed on October 12, 2004. The applicant filed Utility Application No. 11/246,163 on October 11, 2005, which would eventually issue as the '890 patent, the first of the Family 3 patents. The application for the '890 patent originally included 45 claims, of which claims 37-42 are representative:

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:

information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes a interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

Application No. 11/246,163, at 28 (Oct. 11, 2005).

138. The Examiner rejected all 45 original claims, including claims 37-42, under 35 U.S.C. 102(e) as being anticipated by Fadavi-Ardekani (U.S. Patent No. 6,707,822). *See* 2/24/2009 Office Action. The applicant attempted to argue that Fadavi-Ardekani was not enabling and not anticipatory (*see* 8/21/2009 Remarks, at 8), but the Examiner rejected those arguments and maintained the rejection of all 45 claims as anticipated by Fadavi-Ardekani. *See* 12/9/2009 Office Action, at pp. 4, 14-15.

139. The Examiner found, for example, that Fadavi-Ardekani teaches methods and systems for “sharing resources in a transceiver” comprising “allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).” *Id.* at 14, 16, 18-19. The Examiner also found that Fadavi-Ardekani teaches transmitting or receiving “information that is used to determine a maximum amount of shared memory that can be allocated.” *Id.* at 15, 20. Finally, the Examiner found that Fadavi-Ardekani also teaches that the first latency path may include an interleaver and the second latency path may include either a second interleaver or a deinterleaver. *Id.* at 16, 19.

140. The Examiner and applicant then held an interview, and in an interview summary, the Examiner indicated that “[t]he examiner and applicant discussed an overview of the invention and explained features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth.” 12/16/2009 Examiner Interview Summary, at 4. The examiner suggested that the Applicant provide more details “such as type of memory, type of interleaving to distinguish from the prior art or memory art.” *Id.*

141. Thereafter, the applicant cancelled all 45 claims and introduced new claims 46-53, which the applicant stated “more particularly claim[] certain aspects of the invention,” including “a deinterleaver embodiment” reflected by independent claim 50. *See* 12/17/2009 Amendment and Response, at 4; 12/30/2009 Amendment and Response, at 5. The applicant then made one more amendment to both of the newly added independent claims 46 and 50 in order to “correct a typographical error,” which was directed to the use of the word “of” in new independent claims 46 and 50. 3/8/2010 Supplemental Amendment and Response, at 2, 3, 5.

142. The Examiner then issued a notice of allowance, which included an “Examiner’s Amendment.” The Examiner’s Amendment indicated that “authorization for this examiner’s amendment was given in a telephone interviews with Jason Vick (Reg. No. 45,285) on August 2 and 3, 2010,” and that “[s]hould the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312.” *See* 9/7/2010 Notice of Allowance, at 2-4. With respect to claim 50, the examiner noted it “identifies the distinct features of specifying a maximum number of bytes available to be allocated to a deinterleaver in a transmitted or received message, determining the amount of memory required to the deinterleaver wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message.” *Id.* at 5. The Examiner stated that “the closest prior art, Fadavi-Aredekani . . . discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, [but] fails to suggest limiting the memory allocated to the deinterleaver to a maximum number of bytes available that was specified in a transmitted or received messages.” *Id.*

143. After receiving the notice of allowance, on October 4, 2010, the applicant submitted comments on the Examiner’s stated reasons for allowance. The applicant stated that

“[w]hile the stated Reasons for Allowance may be a stated reason for allowing some independent claims, Applicant submits that some independent claims have a different reason for allowance and that some independent claims have other reasons for allowance. Specifically, the prior art fails to teach the specific combination of features as recited in the independent claims 46 and 50.” The applicant did not identify any error in the claims or contend that the allowed claims were defective. *See, e.g.*, 10/4/2010 Comments on Statement of Reasons for Allowance, at 1-2 (Application No. 11/246,163).

144. The applicant filed on April 16, 2010, August 9, 2010, and October 11, 2010 the three applications that matured into the '882 patent, the '381 patent, and the '048 patent, respectively. The '381 patent issued on November 16, 2010, and the '882 patent issued on November 30, 2010. The '048 patent did not issue until September 12, 2012.

145. On January 5, 2011, the applicant filed three requests for certificates of correction pursuant to 37 C.F.R. §§ 1.322 and 1.323 for claim 5 of the '890 patent, claim 13 of the '882 patent, and claim 5 of the '381 patent. The applicant stated that the corrections to the '890 patent were necessary due to “mistake[s] of both the Office and the Applicant,” specifically, the use of the words “transmission” and “received” in conjunction with the deinterleaving and interleaving functions of the transceiver, rather than “reception” and “transmitted.” *See, e.g.*, 1/5/2011 Request for Certificate of Correction of Patent for Office’s Mistake (37 C.F.R. § 1.322) and Applicant’s Mistake (37 C.F.R. § 1.323), at 1 (Application No. 11/246,163). A third word used in the claims, “shred,” also was corrected to be recited as “shared.” *See id.*

146. The requests for Certificates of Correction in the '882 and '381 patents also sought to correct “shred” and the use of the words “transmission” and “received” in connection

with, respectively, the deinterleaving and interleaving functions of the transceiver. The applicant admitted that the errors in the '882 and '381 patents were due only to mistakes of the applicant. *See, e.g.*, 1/5/2011 Request for Certificate of Correction of Patent for Applicant's Mistake (37 C.F.R. § 1.323), at 1 ('882 patent file history); 1/5/2011 Request for Certificate of Correction of Patent for Applicant's Mistake (37 C.F.R. § 1.323), at 1 ('381 patent file history).

147. Claim 5 of the '048 patent included the same use of the words "transmission," "received," and "shred" that had been the subject of Certificates of Correction for the '890 and '381 patents. In an initial office action dated January 6, 2012 rejecting all the claims, the examiner specifically called attention to the use of "shred," and objected to the claim due to that error. 1/6/2012 Non-Final Rejection, at 2. The examiner did not identify any other errors in the claim language, and in responding to rejection, the applicant did not suggest there were any. *See* 8/3/2012 Amendment and Response, at 6-7.

148. The examiner thereafter issued a Notice of Allowance, once again stating that "[t]he prior arts of record . . . fail to teach, singly or in combination, the claimed invention as whole, especially *transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver*." Notice of Allowance, at 4 (emphasis in original); *see also id.* at 5.

4. Claim Construction

149. I have reviewed the Court's Claim Construction Order for the Family 3 Patents, issued on December 28, 2017. A summary of the terms in the claims of the '882 patent, the '381 patent, the '048 patent, and the '473 patent for which the Court provided a construction is provided below:

Term or Phrase	Court's Construction
“transceiver”	“communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry”
“shared memory”	“common memory used by at least two functions, where a portion of the memory can be used by either one of the functions”
“amount of memory”	plain meaning
“the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]”	“the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory”
“latency path”	“transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay”
“wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message”	plain meaning
“portion of memory”	plain meaning
“memory is allocated between the [first] interleaving function and the [second interleaving / deinterleaving] function”	“an amount of the memory is allocated to the [first] interleaving function and an amount of memory is allocated to the [second interleaving / deinterleaving] function”

150. In my analysis, I have applied the Court's constructions. I have interpreted the remaining claim terms as they would have been understood by a person having ordinary skill in the art on the priority date of the Family 3 patents, considering the context of the claims themselves, the specification, the figures, the prior art, and the prosecution history. Consistent with these constructions and interpretations, I have considered the claims in light of the ordinary meaning of the claims based on the perspective of one of skill in the art and consistent with my experience in the field.

VIII. ANALYSIS OF INVALIDITY UNDER 35 U.S.C. § 112

A. 35 U.S.C. § 112, ¶ 2 – Indefiniteness

151. It is my opinion that claim 19 of the '473 patent is indefinite. Claim 19 recites the limitation “wherein at least a portion of the memory **may be** allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.” One of ordinary skill in the art would not have known with reasonable certainty whether a portion of the memory actually has to be allocated to an interleaving function at one time, and a deinterleaving function at another, or whether the mere possibility that some portion of the memory could possibly be allocated to the interleaving or deinterleaving function suffices to meet the claim language. I note that the Court determined that this language should have its plain meaning during claim construction.

152. The use of the permissive language “may be allocated” makes it impossible for a skilled artisan to determine with reasonable certainty whether the claim is infringed, because it is not clear, when reading the claims, specification, and file history, whether the memory actually has to be allocated in more than one way. Given the '473 patent's disclosure, one of ordinary skill in the art would have understood that, within the shared memory, a particular memory space may be allocated to the interleaver or the deinterleaver depending on the current demands of the system, and in turn, a message. It is not clear from the intrinsic record, however, whether this allocation actually has to happen, at some point, in order for a device to infringe. For example, a system could use a shared memory in such a way that it is theoretically possible that a portion of the memory is allocated to a deinterleaver or an interleaver, depending on the message, but it might not actually ever happen in practice. One of ordinary skill in the art would not have understood whether such a system would infringe claim 19 of the '473 patent.

B. 35 U.S.C. § 112, ¶ 1 – Written Description and Enablement

153. It is my opinion that the term “the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]” in claim 1 of the ’048 patent, claim 5 of the ’381 patent, and claim 13 of the ’882 patent lacks written description and enablement. I note that the Court construed this term to mean “the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory.” The specification, claims, and file history do not demonstrate to one of ordinary skill in the art that the inventors had possession of the claimed invention as of the filing date in accordance with the Court’s construction.

154. The specification describes sharing resources, such as memory and processing power, as well as ways of allocating those shared resources. It does not, however, describe or explain how shared memory that is allocated to an interleaver and a deinterleaver can be used at the same time, or even what “used at the same time” even means. Notably, the phrase “used at the same time” does not appear in the written description. One of ordinary skill in the art would not have understood that the inventor was in possession of this aspect of the invention when the application was filed.

155. It is also my opinion that the claim term “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message” in claim 19 of the ’473 patent lacks written description. I understand that the Court determined that this term should have its plain meaning.

156. One of ordinary skill in the art would not have understood the patentee to have been in possession of an apparatus wherein at least a portion of the memory may be allocated to a first interleaving function or a second interleaving function at any one particular time depending on the message. The specification describes ways of allocating shared memory between an interleaving function and a deinterleaving function, but it does not describe to one of ordinary skill in the art how at least a particular portion of the memory can be allocated to one function, and then be allocated to the other function at any one particular time.

C. Certificates of Correction

157. I was asked to opine on whether a person having ordinary skill in the art would have recognized certain terms in claim 5 of the '381 patent and claim 13 of the '882 patent, as they originally issued, to be "typographic errors" such that the changes made to these terms in the Certificate of Correction did "not materially affect the scope or meaning of the patent" as the applicant represented to the Patent Office in its requests for Certificates of Correction.

158. I believe that a person having ordinary skill in the art would have understood the word "shred" in the issued patents to be an obvious typographical error, particularly because it is followed by the word "memory," and the claims recite "shared memory" elsewhere.

159. I do not, however, believe that a person having ordinary skill in the art would have considered the terms "transmission" and "received" in claim 5 of the '381 patent and claim 13 of the '882 patent to be typographical errors. For example, as issued, both claims recited "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. . ." and "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate." As a skilled artisan would have understood, there is no reason why a

transceiver could not deinterleave a first plurality of Reed-Solomon coded data bytes and then transmit them at a first data rate, nor is there any reason why a transceiver could not receive a second plurality of Reed-Solomon coded data bytes at a second data rate and then interleave them. The Family 3 patents do not appear to foreclose either of these possibilities. Indeed, the Family 3 patents state that “it should be appreciated that this invention can be applied to any transceiver having any number of latency paths,” which a person having ordinary skill would have understood to include transceivers that allocate “a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate” and “a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate.”

160. Moreover, in my opinion, a person having ordinary skill in the art would have considered the changes made by the Certificates of Correction to materially affect the scope and meaning of the issued patents. A skilled artisan would have understood transmission and reception to be different, and that requiring transmission instead of reception, or vice versa, changes the required functionalities of the claimed transceivers. A skilled artisan would also have understood that a transceiver that did not infringe claim 5 of the '381 patent or claim 13 of the '882 patent as issued could infringe claim 5 of the '381 patent and claim 13 of the '882 patent as modified by the Certificates of Correction. In my opinion, this fact means that the changes made through the Certificates of Correction changed the scope and meaning of the '381 and '882 patents.

IX. ANALYSIS OF THE PRIOR ART

161. It is my opinion that each of the asserted claims of the Family 3 patents are rendered obvious by prior art as I describe below. In my analysis below, I opine on the claim language as corrected by the certificates of corrections filed by the applicant.

A. The Asserted Claims Are Obvious Over LB-031

162. ITU-T SG/15/Q4 Contribution LB-031 (“LB-031”), entitled “VDSL2 – Constraining the Interleaver Complexity,” was a contribution to the June 14-18, 2004 meeting of SG15/Q4, held in Leuven, Belgium. The first page of LB-031 indicates that it was a revision of a T1E1.4 contribution made in 2003 and numbered T1E1.4/2003-493.

163. It is my opinion that claim 1 of the ’048 patent, claim 5 of the ’381 patent, claim 13 of the ’882 patent, and claim 19 of the ’473 patent are rendered obvious by LB-031 in view of the knowledge of one of ordinary skill in the art. I have reviewed TQ Delta’s infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta’s interpretation of the claims, however, then LB-031 renders obvious the asserted claims of the Family 3 patents.

1. Public Availability of LB-031

164. LB-031 was made available to SG15/Q4 electronically via the SG15/Q4 document server at least by June 16, 2004.⁶ Per the SG15/Q4 operating rules, it should have been uploaded to the document server by at least June 7, 2004. *See, e.g.*, LB-004 (“Contributions for the ITU Rapporteur meeting should be uploaded to the ftp site one week prior to the start of the Rapporteur meeting. Generally, for a Monday Rapporteur meeting start,

⁶ See 00_doc_list.html, which was generated on June 16, 2004 by Steve Palm, one of the Associate Rapporteurs of SG15/Q4, and includes a link for LB-031; *see also* LB-000.txt, which lists the contributions to the Leuven meeting, including LB-031.

papers should be submitted by end of day on the prior Monday. Before presentation of a contribution, the electronic version of the paper shall be provided to the Rapporteur.”). Once uploaded to the document server, LB-031 would have been available to SG15/Q4 participants world-wide. *See, e.g.*, LB-004 (“The use of electronic document submission and distribution is a key factor in improving the efficiency of Q4/SG15 operation. The guidelines below will insure that all meeting attendees have advance capability to review contributions presented for Rapporteur meetings. The basic principals [sic] are that documents are posted on the ITU informal WEB site and access to the WEB is available world wide.”).

165. The VDSL issues list, used by SG15/Q4 to track work item status, open questions, and agreements, indicates that LB-031 was presented and discussed at the Leuven meeting, and three new open issues were added to the VDSL issues list based on the content and discussion of LB-031. *See* LB-U11R4, item 11.4 (adding questions “Should interleaver complexity be specified in terms of a time delay (ms), not in terms of an amount of memory or an interleaver depth?” and “Should interleaver delay in terms of octets be exchanged between the VTU-O and VTU-R; Should the delay in octets meet the minimum requirements in terms of the delay in time?” and “Should the upper limit on the number of codewords per unit time be constrained and scale with the data rate so that as the data rates increase, this upper limit on the number of codewords is also higher?”); *compare* LB-U11, item 11.4 (VDSL2 issues list at beginning of Leuven meeting did not include questions quoted above). Marcos Tzannes, a named inventor on the Family 3 patents, submitted contributions to the Leuven meeting. *See* 00_doc_list.html, LB-000.txt. I also encountered Mr. Tzannes at a number of other SG15/Q4 meetings that I attended. Mr. Tzannes served as Associate Rapporteur for the G.bond and G.test projects of SG15/Q4.

2. Brief Description of LB-031

166. LB-031 proposes to set particular restrictions on the interleaver to be specified for the VDSL2 standard being developed by SG15/Q4. LB-031 at 1. LB-031 begins with a tutorial on convolutional interleaving and derives equations to illustrate trade-offs between interleaver memory size, error correction capability, delay, and error burst separation. Denoting the block size as I and the interleaver depth as d , LB-031 explains that the end-to-end delay of the interleaver/deinterleaver pair, in octets (i.e., bytes) is given by

$$\text{interleaver delay} = (I - 1) \times (d - 1) \text{ octets} \quad (\text{Eq. 1})$$

and that “[t]he smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver.” *Id.* at 2. LB-031 teaches that the amount of memory used to implement the interleaver is typically approximately the same as the amount of memory used to implement the deinterleaver, and that the smallest possible amount of memory for either is given by:

$$\text{smallest possible (de)interleaver memory} = (I - 1) \times (d - 1)/2 \text{ bytes} \quad (\text{Eq. 2})$$

Id. LB-031 explains that “[i]n a typical implementation, slightly more memory is often required,” and “[t]he actual amount of required memory is implementation specific.” *Id.*

167. LB-031 teaches that “[t]he length of a burst that can be corrected by the combination of Reed-Solomon coding and interleaving/deinterleaving is dependent on the line data rate,” denoted in LB-031 as ldr , which is the bit rate of the Reed-Solomon encoded bits. *Id.* The line data rate ldr is higher than the net data rate, denoted as ndr , which is the user data rate. *Id.* LB-031 uses the notation $ldr_m\text{bit_s}$ to indicate when the line data rate is in Mbit/s and $ldr_k\text{bit_s}$ to indicate when the line data rate is in kbit/s. Denoting the Reed-Solomon codeword length as n and the number of Reed-Solomon redundancy bytes as r , LB-031 teaches that the line data rate and net data rate are related by the equation

$$ndr_kbit_s = ldr_kbit_s \times (n - r)/n - \text{overhead rate} \quad (\text{Eq. 3})$$

Id. As a person having ordinary skill in the art would have recognized as of the Family 3 patents' priority date, the "overhead rate" would include any additional bit rate consumed for the transmission of bits that do not convey user data (e.g., cyclic redundancy check bytes, messages transmitted to the far-end transceiver for operations, administration, and maintenance purposes, etc.).

168. LB-031 notes that the Reed-Solomon code can correct t bytes in error, where $t = r/2$. *Id.* It also explains that the Reed-Solomon codeword size n can be an integer multiple of the interleaver block size I , i.e., $n = I \times q$. *Id.* Consequently, the combination of Reed-Solomon coding and interleaving can correct a burst of errors up to $t \times d/q$ octets long. *Id.* By accounting for the line data rate, the maximum duration of a burst of errors that can be corrected can be determined. Converting to time, the duration of a burst of errors can be up to

$$\text{INP_min} = t \times \frac{d}{q} \times \frac{8}{ldr_mbit_s} \mu\text{s} \quad (\text{Eq. 4})$$

In equation 4, "INP_min" denotes the impulse noise correction, and the "8" in the numerator is the number of bits per byte to make the units of the quantity microseconds. *Id.* at 2, 5.

169. LB-031 provides an example using the equations for ADSL2 and ADSL2+, in which $q = 1$ (i.e., the interleaver block size is equal to the Reed-Solomon codeword length), the maximum value of t is 8 (corresponding to 16 redundancy bytes), the maximum value of the Reed-Solomon codeword length n is 255, and the maximum value of the interleaver depth d is 64 in the downstream direction and 8 in the upstream direction. *Id.* at 2. Assuming the maximum line data rate of 24.48 Mbit/s in ADSL2+, the use of Reed-Solomon coding plus interleaving can correct a burst of errors up to $8 \times 64/1 \times 8/24.48 = 167 \mu\text{s}$ in duration. *Id.*

170. LB-031 notes that the end-to-end interleaver delay, in milliseconds, is

$$(I - 1) \times (d - 1) \times 8/ldr_kbit_s \text{ (Eq. 5)}$$

Id. For the maximum line data rate and largest values of I and d in ADSL2+, the delay is

$$(255 - 1) \times (64 - 1) \times 8/24480 = 5.23 \text{ ms.}$$

171. LB-031 teaches that “[e]rror bursts must be separated in time so that each codeword corrects only one burst.” *Id.* The span (i.e., time over which a single codeword extends after interleaving) of a Reed-Solomon codeword of size n octets (bytes) and an interleaver depth of d is equal to

$$n \times d/q \times 8/ldr_kbit_s \text{ (Eq. 6)}$$

Id. Because $n = I \times q$, the span is nearly identical to the end-to-end interleaver delay given in Equation 5 for large codeword size n and depth d . *Id.* Using the ADSL2+ example from above, at the maximum codeword size, interleaver depth, and line data rate, each codeword spans $(255) \times (64) \times 8/24480 = 5.33 \text{ ms.}$ *Id.* at 3. Thus, in ADSL2+, at the maximum line data rate and codeword size, the combination of coding and interleaving can correct a burst of duration $167 \mu\text{s}$ every 5.33 ms. *Id.*

172. LB-031 observes that “[m]ore interleaver memory normally allows more error correction but leads to higher delays and a longer separation between error bursts.” *Id.*

Although “[s]ignificant error correction can be achieved by using shorter codewords requiring less memory, less delay, and shorter time between bursts,” shorter codewords “typically have lower net coding gain and higher computation requirements since there are more decoder operations required in the same amount of time.” *Id.* Thus, there is a trade-off between complexity, capability, and performance. *Id.*

173. LB-031 observes that “[t]he size of the interleaver memory will be a major source of complexity in VDSL2.” *Id.* ADSL2 specifies the smallest maximum interleaver

depth and the maximum number of Reed-Solomon codewords in a DMT symbol. *Id.* LB-031 points out two problems with adopting the same approach for VDSL2: (1) “it removes the flexibility of trading codeword size and interleaver depth to allow more error correction with the same amount of memory,” and (2) as the data rate increases, the end-to-end interleaver delay decreases, which leads to less error correction capability. *Id.*

174. Because the VDSL2 data rate requirements of different service providers extend over a large range, LB-031 suggests defining “the interleaver complexity requirements in a way that will allow those who want to deploy VDSL2 at lower speeds to do so at a reduced complexity with respect to higher speed implementations.” *Id.* Because the end-to-end interleaver delay in units of time is proportional to the interleaver depth and inversely proportional to the line data rate, as shown in Equation 5, LB-031 proposes to specify the interleaver complexity in terms of the end-to-end interleaver delay in units of time. *Id.* LB-031 suggests that requiring VDSL2 interleavers to support a delay of at least 5.23 ms (the value that results when ADSL2+ operates at the maximum line data rate, maximum interleaver delay, and maximum codeword size). *Id.*

175. LB-031 teaches:

For interoperability reasons, the VTU-O and VTU-R must exchange the interleaver delay in terms of octets. The requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate. If a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value. The VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities.

Id. LB-031 emphasizes again that “the actual amount of memory required is implementation specific.” *Id.*

176. As an example of the proposed approach, LB-031 uses Equations 1 and 5 to determine the minimum memory size required in each of the interleaver and deinterleaver for a VDSL2 line data rate of 44.5 Mbit/s and a minimum interleaver delay requirement of 5.23 ms. *Id.* at 4. From Equation 5, the value of $(I - 1) \times (d - 1)$ is 29092 bytes, and from Equation 1, the end-to-end delay of the interleaver in octets (bytes) is then also 29092. From Equation 2, the interleaver would need to have “at least 14546 octets” (bytes), although the amount actually used would be implementation-specific. *Id.* (emphasis in original). The VDSL2 transceiver would indicate, during the initialization procedure, that it can support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay. *Id.* LB-031 notes that if the line data rate ends up being much less than 44.5 Mbit/s, the delay using the entirety of the interleaver memory could be quite large, and “[t]his is why the maximum delay is still needed.” *Id.*

177. LB-031 proposes that SG15/Q4 agree that “interleaver complexity should be specified in terms of a time delay (ms), not in terms of an amount of memory or an interleaver depth,” and “interleaver delay in terms of octets should be exchanged between the VTU-O and VTU-R; the delay in octets should meet the minimum requirements in terms of the delay in time.” *Id.* at 6.

3. Claim 1 of the '048 Patent

178. It is my opinion that claim 1 of the '048 patent is obvious over LB-031 in view of the knowledge of one of ordinary skill in the art at the time of the alleged invention.

a. 1[a]. “A system that allocates shared memory”

179. It is my opinion that a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood LB-031 to disclose the preamble, limitation 1[a] of claim 1 of the '048 patent, to the extent that it is limiting. *See, e.g.*, LB-031 at p. 3.

180. LB-031 discloses allocating memory between an interleaver and a deinterleaver in a VDSL system. LB-031 identifies as an issue “tradeoffs between interleaver memory, error correction capability, delay, and burst separation.” *Id.* at p. 3. It then proposes that “the VTU-O and VTU-R must exchange the interleaver delay in terms of octets. The requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate.” *Id.* LB-031 goes on to provide an example of allocating memory between an interleaver and a deinterleaver, in which “[i]f the minimum interleaver delay requirement were 5.23 ms, then, from equation (5) and equation (1), this transceiver must support a delay of at least 29092 octets which corresponds to having an interleaver memory of *at least* 14546 octets according to equation (2).” *Id.* at 4 (emphasis in original). One of ordinary skill in the art on the priority date of the Family 3 patents would have understood this example to teach allocating memory for interleaving and deinterleaving.

181. In my opinion, one of ordinary skill in the art would have understood from the disclosures of LB-031 that the allocated memory can be a shared memory. I note that the Court construed “shared memory” as “common memory used by at least two functions, where a portion of the memory can be used by either one of the functions.” LB-031 describes how “[t]he size of the interleaver memory will be a major source of complexity in VDSL2.” *Id.* at 3. It further explains how VDSL2 has stated 100 Mbit/s as a stated goal for data rate, but that “a number of operators have stated their requirements at well below 100 Mbit/s.” *Id.* LB-031 further explains that the actual amount of memory required for interleaving and deinterleaving is implementation specific, and that a VDSL2 implementation can support a larger memory than is actually required. *Id.*

182. As I explained above in Section VII.C, it was well known by the priority date of the Family 3 patents that an interleaver and deinterleaver could share a memory, including in DSL implementations. *See, e.g.*, U.S. Patent Pub. No. 2005/0034046 by Berkman *et al.* at Abstract (disclosing a “combined interleaving and deinterleaving circuit” with “data memory (RAM) for temporary storage of the data to be interleaved and deinterleaved”); U.S. Patent No. 6,707,822 to Fadavi-Ardekani *et al.* at Abstract (disclosing an “Interleave/De-Interleave Memory” that “is shared by multiple ADSL sessions and by the transmit and receive processes within an individual session”); U.S. Patent No. 6,381,728 to Kang at col. 5:35-38 (disclosing “double buffering [that] allows the channel interleaver memory to be used, along with the app memory, as the turbo deinterleaver memory”); U.S. Patent No. 7,269,208 to Mazzoni *et al.* at Abstract (disclosing memory having “a first memory space assigned to the interleaver and a second memory space assigned to the deinterleaver” of a VDSL transceiver); U.S. Patent No. 5,751,741 to Voith *et al.* at col. 4:47-50 (disclosing external interleave/deinterleave memory used by both transmitter for interleaving and receiver for deinterleaving).

183. Consequently, a person having ordinary skill in the art as of the Family 3 patents’ priority date would understand that, by recognizing the negative effects of complexity and size of interleaver memory, LB-031 discloses the allocation of a “common memory used by at least two functions, where a portion of the memory can be used by either one of the functions” for the interleaver and deinterleaver.

b. 1[b]. “a transceiver that is capable of”

184. It is my opinion that LB-031 discloses limitation 1[b]. *See, e.g.*, LB-031, at pp. 3-4.

185. LB-031 describes that “[d]uring initialization, the VDSL2 transceiver would indicate” its capabilities. LB-031 at 4. LB-031 describes the use of a VDSL2 VTU-O and

VTU-R to allocate memory for interleaving and deinterleaving; one of ordinary skill in the art would have understood the VTU-O and VTU-R to be transceivers. *Id.* at 3. LB-031 also provides an example of calculating and allocating interleaver memory in a VDSL2 transceiver. *Id.* at 4.

186. I understand that the Court construed the term “transceiver” to mean “communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.” One of ordinary skill in the art would have understood that VDSL2 transceivers described in LB-031 both transmit and receive data (i.e., to be interleaved and deinterleaved), and share common circuitry such as a memory, in addition to other circuitry, such as, for example, an interface to the twisted pair.

c. **1[c]. “transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver”**

187. In my opinion, LB-031 discloses limitation 1[c]. *See, e.g.*, LB-031, pp. 3, 6.

188. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. The O-PMS message includes a parameter referred to as “max_delay_octet.” *See* G.993.2 (12/2011), § 12.3.5.2.1.3, Table 12-56. I do not agree that sending or receiving the O-PMS message meets this limitation. If the Court or other trier of fact interprets the claim such that sending or receiving the O-PMS message meets this limitation, however, then the message specifying interleaver delay in octets described in LB-031 discloses this limitation under such an interpretation of the claims.

189. LB-031 states that “[d]uring initialization, the VDSL2 transceiver would indicate” its capabilities, and that these capabilities include the maximum bit rate it can support, the maximum supported end-to-end delay in octets, and the maximum delay in ms. LB-031 at

pp. 4, 6. LB-031 also discloses that “[f]or interoperability reasons, the VTU-O and VTU-R must exchange the interleaver delay in terms of octets.” *Id.* at 3; *see also* 6 (“interleaver delay in terms of octets should be exchanged between the VTU-O and VTU-R, the delay in octets should meet the minimum requirements in terms of delay in time.”). LB-031 states that “[t]he requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate,” but that “[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value,” in which case “[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities.” *Id.* at 3.

190. LB-031 describes the relationship between the interleaver delay in octets and interleaver memory, noting that “the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver” and providing equations that describe that relationship, which I explained above at Section IX.A.2. *Id.* at 2. Thus, the information exchanged during initialization includes the maximum end-to-end interleaver delay in octets, which meets this limitation under TQ Delta’s interpretation of the claims.

d. **1[d]. “determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory”**

191. LB-031 discloses limitation 1[d], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4.

192. LB-031 describes, though a series of equations, the amount of delay imposed by a convolutional interleaver/deinterleaver pair, as well as how the “smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver.” *Id.* at 2 (equations (1) and (2) describing delay and total memory respectively). LB-031 also describes the relationship between Reed-Solomon coding

parameters and octets, and their respective effects on the end-to-end delay of an interleaver. *Id.* at 2 (equations (4) and (5)). Moreover, LB-031 describes trading codeword size and interleaver depth to achieve a desired level of error correcting capability. *Id.* at 3; *see also id.* at 4 (VDSL2 transceiver determines amount of memory to use for interleaving based on octets of memory available and maximum delay). One of ordinary skill in the art as of the Family 3 patents' priority date would have understood that LB-031 describes the VDSL2 transceivers determining an amount of memory required by an interleaver to interleave a first plurality of Reed Solomon coded data bytes within a shared memory.

e. **1[e]. "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate"**

193. It is my opinion that LB-031 discloses limitation 1[e]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6.

194. First, LB-031 discloses VDSL2 transceivers, a VTU-O and a VTU-R, which one of ordinary skill in the art would have understood to allocate a first number of bytes of shared memory to an interleaver (i.e., the VTU-O allocates shared memory to the interleaver for downstream transmission, and the VTU-R allocates shared memory to the interleaver for upstream transmission). *See* LB-031, at p. 3. The example at p. 4 of LB-031 indicates that during initialization, a VDSL2 transceiver indicates the maximum data rate and maximum delay it can support. As a person having ordinary skill in the art on the priority date of the Family 3 patents would have understood, based on the actual data rate, the VTU-O and VTU-R transmitters then allocate a first number of bytes of the memory to their interleavers.

195. Second, LB-031 discloses interleaving Reed-Solomon coded data bytes for transmission at a first data rate. For example, LB-031 explains the dependence of end-to-end

delay of the interleaver/deinterleaver pair on line rate, Reed Solomon codeword size, and other parameters. *Id.* at pp. 2-3; *see also id.* at p. 4-5 (discussing enhancing correction capability of Reed-Solomon code by using smaller codewords and larger interleaver depth). LB-031 also discloses that “the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver, and that “for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same.” *Id.* at LB-031 at p. 2. From these and other disclosures in LB-031, one of ordinary skill in the art would have understood that LB-031 discloses allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

f. **1[f]. “wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message”**

196. LB-031 discloses limitation 1[f], in my opinion, under TQ Delta’s interpretation of the claims. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6.

197. I have reviewed TQ Delta’s infringement contentions, and I understand that TQ Delta contends that the “maximum number of bytes in the message” is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta’s infringement position. To the extent that the Court or the trier of fact interprets the claim consistently with TQ Delta’s contentions, however, LB-031 discloses this limitation in my opinion.

198. As explained above, the example at p. 4 of LB-031 indicates that during initialization, a VDSL2 transceiver indicates the maximum data rate and maximum delay it can support. As a person having ordinary skill in the art as of the Family 3 patents’ priority date would have understood, the transceivers would exchange this information for both the

downstream and upstream directions. Based on the actual data rate and a specified maximum delay, each transmitter then allocates a first number of bytes of the memory to its interleaver. As a person having ordinary skill in the art on the Family 3 patents' priority date would have understood, neither transceiver would allocate interleaver memory to itself in a manner inconsistent with a message it transmitted in which it indicated its capabilities. Therefore, LB-031 discloses that the allocated memory for the interleaver does not exceed the maximum number of bytes in the message. *See, e.g.*, LB-031 at p. 4 (example of transceiver indicating support of delay of at least 29092 octets allocating up to 14546 octets to interleaver, which is less than 29092 octets indicated in message).

199. Furthermore, as described above, the equations in LB-031 describe tradeoffs between “interleaver memory, error correction capability, delay, and burst separation.” *Id.* at p. 3. LB-031 further specifies that “[t]he requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate.” *Id.* at p. 3. Given these constraints, LB-031 places limits on data rates, codeword sizes, levels of impulse noise protection to meet the constraints of interleaver delay, and in turn, available interleaver memory. *Id.* at 5 (“This does not mean that $n=85$ would be the largest or smallest codeword size allowed, it is simply used to guarantee a certain minimum level of impulse noise protection at a given minimum interleaver delay at a given maximum data rate. If the actual interleaver delay is higher or the data rate lower or the impulse noise protection lower, larger codewords can be used.”). One of ordinary skill in the art would have understood that because of these tradeoffs between interleaver memory and other parameters, a system according to LB-031 would not allocate more memory for its own interleaver than the maximum memory available according to the message.

200. LB-031 further provides a number of examples where the optimal interleaver or deinterleaver memory size does not exceed the amount of memory required by the delay and other parameters. *See id.* at 6.

g. **1[g]. “allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate”**

201. In my opinion, LB-031 discloses limitation 1[g]. *See, e.g.*, LB-031, pp. 2-3, 5, 6.

202. First, as I explained above, LB-031 discloses that the VTU-O and VTU-R exchange their capabilities regarding maximum data rate and maximum delay during initialization. *See, e.g.*, LB-031 at p. 4. As I also explained above, a person having ordinary skill in the art as of the Family 3 patents’ priority date would have understood that the transceivers would exchange this information for both downstream and upstream transmission (i.e., the information exchanged would relate to the VTU-O’s interleaver and deinterleaver and the VTU-R’s interleaver and deinterleaver). Based on this information, each transmitter then allocates a first number of bytes of its memory to its interleaver and a second number of bytes of its memory to its deinterleaver.

203. Second, as I also explained above, LB-031 discloses interleaving Reed-Solomon coded data bytes for transmission at a first data rate. LB-031 explains that the end-to-end delay of the interleaver/deinterleaver depends on line rate, Reed Solomon codeword size, and other parameters. *Id.* at pp. 2-3; *see also id.* at p. 4-5 (discussing enhancing correction capability of Reed-Solomon code by using smaller codewords and larger interleaver depth). LB-031 also discloses how “the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver, and that “for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same.” *Id.* at LB-031 at p. 2. From these and other disclosures in LB-031, one of ordinary skill in the art would have

understood that LB-031 discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate.

h. 1[h]. “interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver”

204. In my opinion, LB-031 discloses limitation 1[h]. *See, e.g.*, LB-031, p. 3.

205. I described above the process by which LB-031 allocates memory to the interleaver and to the deinterleaver above with respect to those sections. LB-031 also discloses a convolutional interleaver, which would operate to interleave RS coded data bytes at the transmitter. *Id.* at p. 2. As a skilled artisan would have understood, the receiver would include a corresponding convolutional deinterleaver, which would operate to deinterleave RS coded data bytes. Moreover, because LB-031 discloses a VDSL2 VTU-O and a VTU-R, one of ordinary skill in the art would have understood that the VTU-O (or VTU-R) would interleave the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver, and the deinterleaver would deinterleave the second plurality of RS code data bytes within the shared memory allocated to the deinterleaver.

i. 1[i]. “wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver”

206. It is my opinion that LB-031 discloses limitation 1[i]. *See, e.g.*, LB-031, p. 3.

207. I understand that the Court has construed the term “the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]” as “the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the

interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory.” LB-031 discloses interleaving and deinterleaving for VDSL transceivers. *See, e.g.*, LB-031 at pp. 1-3. As a person having ordinary skill in the art as of the priority date of the Family 3 patents would have understood, VDSL transceivers transmit and receive data at the same time (i.e., the VTU-O transmits data downstream and receives data upstream at the same time, and the VTU-R transmits data upstream and receives data downstream at the same time). This duplex transmission would require that the deinterleaver be able to read from, write to, or hold information for deinterleaving in the portion of memory allocated to the deinterleaver at the same time the interleaver is able to read from, write to, or hold information for interleaving in the portion of memory allocated to the interleaver. Thus, LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.⁷

4. Claim 5 of the '381 Patent

208. It is my opinion that each limitation of claim 5 of the '381 patent is obvious over LB-031 in view the knowledge of one of ordinary skill in the art.

a. 5[a]. “A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver”

209. To the extent that this preamble is limiting, it is my opinion that LB-031 discloses this limitation. *See, e.g.*, LB-031, p. 3.

210. LB-031 discloses the use of an interleaver pair in a VDSL2 VTU-O and VTU-R. *See id.* at p. 3. One of ordinary skill in the art would have understood that source code and

⁷ As I explain above at Section VIII.B, it is my opinion that this limitation is not enabled and lacks written description. To the extent that this limitation is described and enabled by the intrinsic record of the Family 3 patents, it is rendered obvious by the prior art as I describe here, and elsewhere within my report.

instructions for such transceivers could be stored on computer-readable information storage media, and could be executed by a processor, for example, as source or object code. I discuss how LB-031 discloses allocating shared memory in a transceiver above with respect to claim 1 of the '048 patent, which I incorporate here by reference. See Section IX.A.3.a. I describe how LB-031 discloses a transceiver above at Section IX.A.3.b, which I also incorporate by reference. Thus, LB-031 discloses this limitation.

b. 5[b]. “transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver”

211. In my opinion, LB-031 discloses limitation 5[b]. See, e.g., LB-031, pp. 3, 6.

212. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. The O-PMS message includes a parameter referred to as “max_delay_octet.” See G.993.2 (12/2011), § 12.3.5.2.1.3, Table 12-56. I do not agree that sending or receiving the O-PMS message meets this limitation. If the Court or other trier of fact interprets the claim such that sending or receiving the O-PMS message meets this limitation, however, then LB-031 discloses this limitation under such an interpretation of the claims.

213. Above at Section IX.A.3.c, I describe how LB-031 discloses transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver under TQ Delta’s interpretation of the claims, and I incorporate this discussion by reference.

214. LB-031 discloses that during initialization, the VTU-O and VTU-R exchange, among other things, the maximum delay supported, in octets (bytes). As I explained above, LB-031 indicates that the VTU-O and VTU-R exchange this information for both the downstream

and upstream directions of transmission. As a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood, the maximum delay is the end-to-end delay between one transceiver's interleaver and the other transceiver's deinterleaver.

215. Furthermore, LB-031 discloses that "[t]ypically, for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same." *Id.* at 2. One of ordinary skill in the art would have understood that the relationships described in LB-031 between delay, interleaver memory size, data rate and other transmission parameters are for an interleaver or a corresponding deinterleaver. Thus is it my opinion that LB-031 discloses this limitation under TQ Delta's interpretation of the claims.

c. **5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"**

216. LB-031 discloses limitation 5[c], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4.

217. Above at Section IX.A.3.d, I describe how LB-031 discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, and I incorporate my opinions by reference. LB-031 discloses the relationship between the memory required by an interleaver and a deinterleaver, as I described above with respect to the previous limitation. *See id.* at p.3. Accordingly, LB-031 discloses to one of ordinary skill in the art how to determine, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

d. **5[d] “allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate”**

218. In my opinion, LB-031 discloses limitation 5[d]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6.

219. Above at Section IX.A.3.e, I explain how LB-031 discloses allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. In addition, at Section IX.A.3.g above, I explain how LB-031 discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate. I incorporate both of these discussions by reference, and on that basis, it is my opinion that LB-031 discloses this limitation.

e. **5[e]. “wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message”**

220. In my opinion, LB-031 discloses limitation 5[e]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6.

221. I have reviewed TQ Delta’s infringement contentions, and I understand that TQ Delta contends that the “maximum number of bytes specified in the message” is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta’s infringement position. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta’s contentions, however, LB-031 discloses this limitation in my opinion.

222. Above at Section IX.A.3.f, I explain how LB-031 discloses “wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message,” and I incorporate that discussion by reference. In the same way that the VTU-

O or VTU-R of LB-031 would not allocate more memory for the interleaver than is specified in the messages that it exchanges during initialization, the transceiver would also not allocate more memory for the deinterleaver than is specified in the messages that it exchanges during initialization, in my opinion.

f. **5[f]. “allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate”**

223. LB-031 discloses limitation 5[f], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 5, 6.

224. Above at Section IX.A.3.e, I explain how LB-031 allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes transmitted at a second data rate. Also, at Section IX.A.3.g above, I explain how LB-031 discloses allocating a first number of bytes of the shared memory to an interleaver to interleave a first plurality of RS coded data bytes transmitted at a first data rate. I incorporate both of those sections herein by reference, and on that basis, it is my opinion that LB-031 discloses this limitation.

g. **5[g]. “deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver”**

225. LB-031, in my opinion, discloses limitation 5[g]. *See, e.g.*, LB-031, p. 3, 6.

226. Above at Section IX.A.3.h, I explain how LB-031 discloses interleaving a first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference. Though this limitation recites a first plurality being deinterleaved, and a second plurality of data bytes being

interleaved, in my opinion, there is no difference in how a transceiver would implement this limitation. It is my opinion that LB-031 discloses this limitation.

h. 5[h]. “wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver”

227. LB-031 discloses limitation 5[h], in my opinion. *See, e.g.*, LB-031, pp. 3, 6.

228. I explain above at Section IX.A.3.i that it is my opinion that LB-031 discloses wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference herein. In my opinion, one of ordinary skill in the art would have understood that there is no difference in these two limitations, i.e., they both require that the deinterleaver and interleaver memory be used at the same time. Accordingly, it is my opinion that this limitation is met by LB-031.

5. Claim 13 of the ’882 Patent

229. In my opinion, LB-031 discloses each limitation of claim 13 of the ’882 patent, as I explain below.

a. 13[a]. “A system that allocates shared memory”

230. To the extent that this preamble is limiting, LB-031 discloses a system that allocates shared memory. *See, e.g.*, LB-031, p. 3. This limitation is identical to the preamble of Claim 1 of the ’048 patent, and for the same reasons, it is my opinion that this limitation is disclosed by LB-031. *See* Section IX.A.3.a.

b. 13[b]. “a transceiver that performs”

231. In my opinion, LB-031 discloses limitation 13[b]. *See, e.g.*, p. 3, 4. This limitation is identical to the second limitation of Claim 1 of the ’048 patent, except that it recites “a transceiver capable of” additional steps. In my opinion, this limitation is met for the same

reasons that limitation 1[b] of the '048 patent is met, as I explain above at Section IX.A.3.b, and I incorporate my opinions herein by reference.

c. 13[c] through 13[i].

232. Limitations 13[c] through 13[i] of claim 13 of the '882 patent are substantially identical to limitations 5[b] through 5[h] of claim 5 of the '381 patent. *See* Appx. 3 (comparing limitations of claim 13 of the '882 patent to claim 5 of the '381 patent). I incorporate by reference my opinions with respect to those limitations set forth in Sections IX.A.3.c through IX.A.3.i (claim 1) and IX.A.5.b through IX.a.5.h (claim 5). For the same reasons, it is my opinion that those limitations are met by LB-031.

6. Claim 19 of the '473 Patent

233. In my opinion, LB-031 discloses each limitation of claim 19 of the '473 patent.

a. 19[a]. “An apparatus comprising”

234. To the extent that this preamble is limiting, LB-031 discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, LB-031, pp. 3, 4.

b. 19[b]. “a multicarrier communications transceiver”

It is my opinion that LB-031 discloses limitation 19[b]. *See, e.g.*, LB-031, pp. 3, 4. I understand that the Court has construed the term “transceiver” to mean “communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.”

235. LB-031 describes the use of a VDSL2 VTU-O and VTU-R to implement its equations and systems for allocating memory, which one of ordinary skill in the art would have understood to be VDSL2 transceivers. *Id.* at 3. LB-031 further provides an example of calculating and allocating interleaver memory in a VDSL2 transceiver. *Id.* at 4. One of ordinary skill in the art would have understood that VDSL2 transceivers described in LB-031

both transmit and receive data (i.e., to be interleaved and deinterleaved), and share common circuitry such as a memory in addition to other circuitry, such as, for example, an interface to the twisted pair.

236. LB-031 generally deals with VDSL2, which one of ordinary skill in the art would have understood to be a multicarrier communications system. *See, e.g.*, LB-U11R4, item 1.1 (indicating agreement in January 2004 “to develop a subsequent VDSL2 Recommendation that shall specify only DMT modulation, and shall be based on ITU Rec. G.993.1-2004 (VDSL) and ITU Rec. G.992.3 (ADSL2).”). Moreover, LB-031 describes the use of DMT symbols, which are used in multicarrier communications. *See, e.g.*, LB-031 at p. 4 (“Similar to the interleaver delay, we propose that the maximum number of codewords in a DMT symbol (or per unit time) also scale with the data rate. The higher the data rate, the more DMT codewords there can be in a fixed length DMT symbol.”). Therefore, it is my opinion that LB-031 discloses this limitation.

c. **19[c]. “that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path”**

237. In my opinion, LB-031 discloses limitation 19[c]. *See, e.g.*, LB-031, pp. 2-3.

238. LB-031 describes the use of VDSL2 transceivers, a VTU-O and a VTU-R. *Id.* at p. 3. LB-031 also discloses the use of an interleaver in a transmitter and a deinterleaver in a receiver. *Id.* at p. 2. One of ordinary skill in the art would have understood, therefore, that LB-031 discloses multiple latency paths within a VTU-O or VTU-R, namely, a downstream path and an upstream path in each. I understand that the Court has construed the term “latency path” to mean “transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay.” LB-031 further discloses that an interleaving function is associated with a first latency path, and a deinterleaving function is associated with a second latency path because

the VTU-O has an interleaver in the downstream latency path and a deinterleaver in the upstream latency path, and the VTU-R has an interleaver in the upstream latency path and a deinterleaver in the downstream latency path. LB-031 also describes that the operation of convolutional interleaver/deinterleaver pairs imposes a delay (or latency) on their respective latency paths, which may be different for the different latency paths. *Id.* at 2. Thus, LB-031 discloses that the VTU-O and VTU-R are both multicarrier communications transceivers that are configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path.

d. 19[d]. “the multicarrier communications transceiver being associated with a memory”

239. In my opinion, LB-031 discloses limitation 19[d]. *See, e.g.*, LB-031, p. 3.

240. LB-031 describes an interleaver memory associated with a VDSL2 transceiver. *Id.* at p. 3 (“The size of the interleaver memory will be a major source of complexity in VDSL2.”). LB-031 further explains that the amount of memory required is “implementation specific,” and provides examples of the amounts of delay and the amounts of memory required to support them. *Id.* at 3, 4. Therefore, LB-031 discloses that the multicarrier communications transceiver is associated with a memory.

e. 19[e]. “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”

241. LB-031 discloses limitation 19[e], in my opinion. *See, e.g.*, LB-031, pp. 3, 6.

242. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this

limitation, however, then LB-031 discloses this limitation under such an interpretation of the claims.

243. LB-031 states that “[d]uring initialization, the VDSL2 transceiver would indicate” its capabilities, and that these capabilities include the maximum bit rate it can support, the maximum supported end-to-end delay in octets, and the maximum delay in ms. LB-031 at pp. 4, 6. LB-031 states that “[t]he requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate,” but that “[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value,” in which case “[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities.” *Id.* at 3. LB-031 discloses that “[f]or interoperability reasons, the VTU-O and VTU-R must exchange the interleaver delay in terms of octets.” *Id.* at 3; *see also* 6 (“interleaver delay in terms of octets should be exchanged between the VTU-O and VTU-R; the delay in octets should meet the minimum requirements in terms of delay in time.”). One of ordinary skill in the art would have understood that this information would be exchanged as part of a message received during initialization, because the “interleaver delay” would be exchanged prior to the receivers entering Showtime and exchanging user data. *See also id.* at 4 (“During initialization, the VDSL2 transceiver would indicate that it could support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay.”).

244. It is my understanding that the Court construed the term “memory is allocated between the interleaving function and the deinterleaving function” to mean “an amount of memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function.” LB-031 also discloses how “the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the

interleaver/deinterleaver,” and that “for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same.” *Id.* at LB-031 at p. 2. LB-031 explains that the end-to-end delay of the interleaver/deinterleaver depends on line rate, Reed Solomon codeword size, and other parameters. *Id.* Given that the VTU-O and VTU-R in LB-031 receive a message containing the total delay of the interleaver/deinterleaver, one of ordinary skill in the art would have understood that LB-031 discloses allocating the memory between an interleaving function and a deinterleaving function, within TQ Delta’s interpretation of the claims.

f. **19[f]. “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

245. LB-031 discloses limitation 19[f] in my opinion. *See, e.g.*, LB-031, p. 3,

246. LB-031 discloses interleaving and deinterleaving for VDSL transceivers. *See, e.g.*, LB-031 at pp. 1-3. As a person having ordinary skill in the art as of the priority date of the Family 3 patents would have understood, VDSL transceivers transmit and receive data at the same time (i.e., the VTU-O transmits downstream and receives upstream at the same time, and the VTU-R transmits upstream and receives downstream at the same time). Thus, LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

B. **The Asserted Claims Are Obvious Over the Combination of LB-031 and Mazzoni**

247. To the extent it is determined that LB-031 does not render obvious claim 1 of the ’048 patent, claim 5 of the ’381 patent, claim 13 of the ’882 patent, or claim 19 of the ’473 patent, it is my opinion that these claims are obvious over LB-031 in combination with U.S. Patent No. 7,269,208 (“Mazzoni”). I have reviewed TQ Delta’s infringement contentions for

Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then LB-031 in combination with Mazzoni renders obvious the asserted claims of the Family 3 patents.

1. Brief Description of LB-031

248. I provided a brief description of LB-031 above in Section IX.A.2, which I incorporate by reference.

2. Brief Description of Mazzoni

249. Mazzoni describes a multicarrier transceiver with a shared memory that performs interleaving and deinterleaving and can be used in VDSL communication systems. *See, e.g.,* Mazzoni, at col. 1:8-15 (“the invention relates to sending and receiving digital data that can have different bit rates, and to choosing the capacity of memory means used by interleaving and deinterleaving processes effected within send/receive devices capable of processing different bit rates”); *id.* at col. 1:19-22 (“The present invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system, for example, though the invention may also be used in other applications”); *id.* at col. 1:54-58 (“Still another object of the invention is to provide such an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates.”); *id.* at col. 1:59-65 (“These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).”).

250. Mazzoni's multicarrier transceiver includes a channel coding/decoding stage that incorporates interleaving and deinterleaving functionality. *See, e.g.*, Mazzoni, col. 2:3-6. The interleaving and deinterleaving elements of the transceiver include a memory whose minimum size "is fixed as a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system)." *Id.* at col. 2:6-10. The memory assigns spaces to each of the interleaving and deinterleaving means, the sizes of which are set as functions of the bit rates that are processed. *Id.* at col. 2:6-15. Mazzoni recognizes that as a result of this configuration, it is "possible to considerably reduce the size of the memory means required for the interleaving and deinterleaving means implemented within a modem. . . ." *Id.* at col. 2:15-22; *see also id.* at col. 1:65-2:2 ("advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)," such that Mazzoni's invention "is capable of processing different bit rates from a group of predetermined bit rates").

251. Mazzoni notes that "the channel coding/decoding stage may include Reed-Solomon coding/decoding means of length N (where N=240 bytes, for example)." *Id.* at col. 2:37-39; *see also id.* at 2:25-27 ("The transmitted data stream may be protected from transmission channel noise by a Reed-Solomon coding algorithm, which is well known in the art"); *id.* at col. 2:27-37 (noting that the interleaving means may interleave the bytes temporally by modifying the order in which they are transmitted).

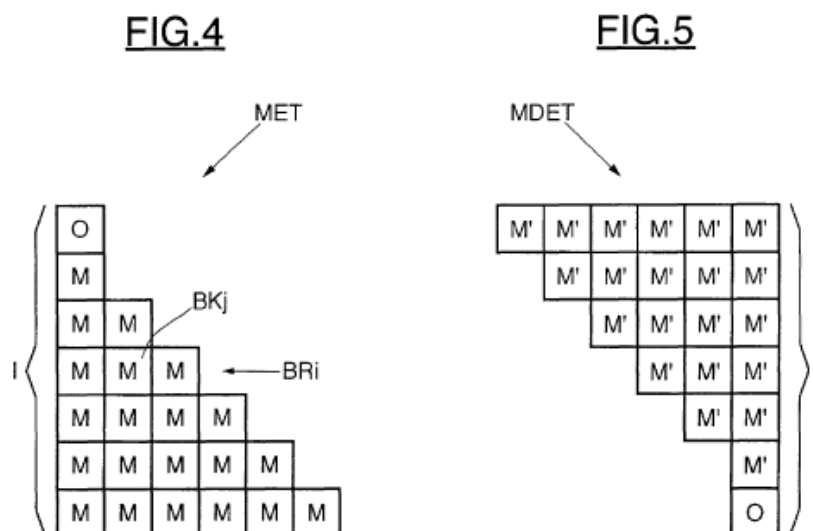
252. Mazzoni further describes how the capacity of the memory assigned to the interleaving/deinterleaving means "may need to be chosen in accordance with the maximum bit

rate of the services offered, here the bit rate of the highest asymmetrical service (service A6).”

Id. at col. 4:18-22. Mazzoni’s transceiver thus includes a channel coding unit “CC,” which includes Reed-Solomon (RS) coding means associated with the interleaving means. *Id.* at col. 4:36-41. The RS coding is applied individually to each of the data packets delivered to the input of the coding unit CC. *Id.* at col. 4:42-44.

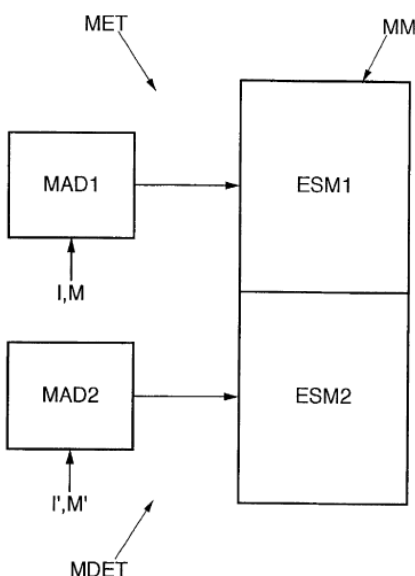
253. Mazzoni’s interleaving and deinterleaving functionality includes “I branches of i-1 blocks of M bytes for interleaving and I’ branches of I’-1 blocks of M’ bytes for deinterleaving,” and thus is capable of allocating the shared memory to the interleaver for use at the same time as the shared memory is allocated to the deinterleaver. *Id.* at col. 5:15-20; FIGS. 4-5. The parameters I, M, I’ and M’ define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means. *Id.* at col. 5:24-27. The allocation is accomplished “according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I’ and M’).” *Id.* at col. 5:27-30.

254. FIGS. 4 and 5 of Mazzoni, copied below, illustrate, respectively, the interleaving means and the deinterleaving means. *Id.* at col. 6:15-17.



255. FIG. 6 of Mazzoni, copied below, reflects the asymmetrical service, which produces an allocation of shared memory to the interleaver and deinterleaver in which I and I' and M and M' are generally different (*see id.* at col. 5:58-60).

FIG.6



The interleaving means and the deinterleaving means shown in FIG. 6 include common memory means MM, e.g., a dual-port random access memory, and the “memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 is assigned to the deinterleaving means MDET.” *Id.* at col. 5:61-67

256. Mazzoni’s parameters I, I', M and M' used for allocation of the shared memory can be determined from maximum and minimum memory size capacities that are easily calculable using downlink and uplink bit rates, the number of bits affected by noise, and RS error correction. *Id.* at col. 6:19-50. The size of the first memory space needed to implement triangular convolutional interleaving with I branches of i-1 blocks of M bytes is equal to $I \times (I-1) \times M / 2$. *Id.* at col. 6:38-41. Similarly, the size of the second memory space ESM2 required to

support the uplink bit rate is equal to $I \times (I' - I) \times M' / 2$, where I and I' are submultiples of the size N of the RS code. *Id.* at col. 6:41-44.

3. Claim 1 of the '048 Patent

257. It is my opinion that LB-031 in combination with Mazzoni discloses each limitation of claim 1 of the '048 Patent.

a. 1[a]. "A system that allocates shared memory"

258. It is my opinion that LB-031 in combination with Mazzoni discloses the preamble, limitation 1[a] of claim 1 of the '048 patent, to the extent that it is limiting. *See, e.g.*, LB-031 at p. 3; Mazzoni, col. 1:54-65; col. 2:3-21; col. 5:58-67.

259. LB-031 discloses allocating shared memory between an interleaver and a deinterleaver in a VDSL system, as I describe above in Section IX.A.3.a, which I incorporate by reference.

260. Mazzoni also discloses a system that allocates shared memory. I note that the Court construed "shared memory" as "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." Mazzoni explains that its disclosures can be applied to a VDSL environment or system. Mazzoni, col. 1:19-22 ("The present invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system, for example, though the invention may also be used in other applications."). In a VDSL environment, Mazzoni describes "an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates." *Id.* at col. 1:54-59. Mazzoni further discloses that it provides a memory that "can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive

device (modem).” *Id.* at col. 1:61-65. As Mazzoni further describes, “[t]he memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means.” *Id.* at col. 2:3-21; *see also id.* at col. 5:58-67 (describing “common memory means MM, e.g., a dual-port random access memory.”). Claim 13 of Mazzoni recites “[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: interleaving and deinterleaving the digital data; setting a minimum size of a shared memory based upon a maximum bit rate of the group of predetermined bit rates; assigning a first memory space of the shared memory for interleaving and a second memory space of the shared memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device; performing Reed-Solomon coding and decoding for a length N of the digital data; and the interleaving providing convolutional interleaving of I branches with $i-1$ blocks of M bytes, and the deinterleaving providing convolutional deinterleaving with I' branches of $i'-1$ blocks of M' bytes, with I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.”

261. Thus, Mazzoni in combination with LB-031 discloses common memory used by an interleaver and a deinterleaver, where a portion of the memory can be used by either one of the two functions.

b. 1[b]. “a transceiver that is capable of”

262. It is my opinion that LB-031 in combination with Mazzoni discloses limitation 1[b]. *See, e.g.*, LB-031, at pp. 3-4; Mazzoni, col. 1:8-27.

263. LB-031 describes the use of a VDSL2 VTU-O and VTU-R to implement its equations and systems for allocating memory, which one of ordinary skill in the art would have

understood to be VDSL2 transceivers, as described above at Section IX.A.3.b, which I incorporate by reference. *Id.* at 3.

264. Mazzoni similarly discloses its invention “may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system,” which a person having ordinary skill in the art would have understood to include VDSL transceivers. Mazzoni, col. 1:19-21. Mazzoni further discloses that its invention can transmit and receive data, as it “provides a device for sending/receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication systems).” *Id.* at col. 1:65-2:2. Mazzoni provides a depiction of two “send/receive devices TO and TU according to the invention.” *Id.* at col. 3:53-61, FIG. 1. One of ordinary skill in the art would have understood these devices to be transceivers.

265. Mazzoni also discloses that in its invention, at least some circuitry is shared between the transmit and receive portions, specifically, a common memory for interleaving and deinterleaving. *Id.* at col. 2:2-13 (“The device according to the invention may include a coding/decoding stage (generally referred to by those skilled in the art as a ‘channel coding/decoding stage including interleaving means and deinterleaving means. The interleaving and deinterleaving means include a memory whose minimum size is fixed as a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system). The memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means.”). The “memory” associated with the interleaving and deinterleaving means is common circuitry shared by the transmitter and receiver portions.

c. **1[c]. “transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver”**

266. In my opinion, LB-031 in combination with Mazzoni discloses limitation 1[c].
See, e.g., LB-031, pp. 3, 6; Mazzoni, col. 1:19-27.

267. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, or with TQ Delta’s infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then LB-031 in combination with Mazzoni discloses this limitation under such an interpretation of the claims.

268. LB-031 discloses that “the VTU-O and VTU-R must exchange the interleaver delay in terms of octets,” and the relationship between the interleaver delay in octets and the amount of interleaver memory needed. *Id.* at 3; see also 6 (“interleaver delay in terms of octets should be exchanged between the VTU-O and VTU-R, the delay in octets should meet the minimum requirements in terms of delay in time.”). I discuss how LB-031’s message meets this limitation above at Section IX.A.3.c, which I incorporate by reference.

269. In addition, Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that “can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).” Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that “the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means” are determined “according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I’ and M’).” *Id.* at col. 5:24-31. The system according to Mazzoni then divides the memory between the interleaving and deinterleaving means. *Id.* at col. 5:64-67 (“The

memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 in assigned to the deinterleaving means MDET.”). The size of the memory space is selected based on the bit rate. *Id.* at col. 6:26-30 (“The size of the memory space needed to store this maximum bit rate is then equal to $N \times n_{rs} / 2$, where N is the size of the Reed-Solomon code (here 240). The resulting memory space size is therefore equal to 24,960 bytes.”). One of ordinary skill in the art would have understood that the bit rate information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, as is described in LB-031. Thus, LB-031 in combination with Mazzoni discloses limitation 1[c] under TQ Delta’s interpretation of the claims.

d. **1[d]. “determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory”**

270. LB-031 in combination with Mazzoni discloses limitation 1[d], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4; Mazzoni, col. 1:46-2:2; col. 2:6-17; col. 2:25-36; col. 4:18-22; col. 5:21-30; col. 5:58-67; col. 6:19-50.

271. LB-031 describes how a transceiver can determine an amount of memory required by an interleaver to interleave Reed Solomon coded data bytes within the shared memory. I explain this in Section IX.A.3.d above, which I incorporate by reference.

272. Mazzoni also discloses this limitation. For example, Mazzoni explains that “the parameters I, M, I’ and M’ can be modified, e.g., by software, and are delivered by control means MCD,” and that “[t]hese parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means.” Mazzoni at col. 5:21-27. Claim 13 of Mazzoni recites “[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: . . . setting a

minimum size of a shared memory based upon a maximum bit rate of the group of predetermined bit rates. . . .”

273. Thus, LB-031 in combination with Mazzoni discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory.

e. **1[e]. “allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate”**

274. It is my opinion that LB-031 and Mazzoni disclose limitation 1[e]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 5:21-30; col. 5:61-67; col. 6:19-50; col. 10:22-42.

275. LB-031 describes allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. I explain this in Section IX.A.3.e above, which I incorporate by reference.

276. Mazzoni also discloses this limitation. For example, Mazzoni explains that “the parameters I, M, I’ and M’ can be modified, e.g., by software, and are delivered by control means MCD,” and that “[t]hese parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means.” Mazzoni at col. 5:21-27. The bytes to be interleaved are bytes of a Reed-Solomon codeword. *Id.* at col. 4:36-41 (“The channel coding unit CC includes Reed-Solomon coding means whose structure and function are known to those of skill in the art. The Reed-Solomon coding means are associated with the interleaving means. In conjunction with subsequent interleaving, the Reed-Solomon coding can correct bursts of errors introduced by the transmission channel. Reed-Solomon coding is applied

individually to each of the data packets delivered to the input of the coding unit CC.”); *id.* at col. 6:11-18 (“An example of the capacity of the memory MM and of the values chosen for the parameters I, M, I’ and M’ for an asymmetrical service A6 and an RS (240, 224) Reed-Solomon code with a correction power of 8 bytes/word may be as follows when the transmission lines are disturbed by an impulsive noise with a duration of 0.25 ms.”).

277. Mazzoni discloses implementing the interleaver using “I parallel branches BR_i (numbered from 0 to I–1, for example) which are implemented with a delay increment of M per branch (M represents the maximum number of bytes of a block BK_j with index j).” *Id.* at col. 5:31-35; *see also id.* at col. 6:19-30. The bytes are then interleaved, which means a first number of bytes of the shared memory to the interleaver were allocated to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. *See, e.g. id.* at col. 5:39-48.

278. Furthermore, claim 13 of Mazzoni recites “[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: . . . assigning a first memory space of the shared memory for interleaving and a second memory space of the shared memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device; performing Reed-Solomon coding and decoding for a length N of the digital data. . . .”

279. Therefore, LB-031 and Mazzoni disclose allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

f. **1[f]. “wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message”**

280. LB-031 in combination with Mazzoni discloses limitation 1[f], in my opinion.

See, e.g., LB-031, pp. 2-3, 4, 5, 6; Mazzoni, col. 1:19-27.

281. I have reviewed TQ Delta’s infringement contentions, and I understand that TQ Delta contends that the “maximum number of bytes specified in the message” is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta’s contentions or interpretation of the claims. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta’s contentions, however, LB-031 in combination with Mazzoni discloses this limitation in my opinion.

282. LB-031 discloses that the allocated memory for the interleaver does not exceed the maximum number of bytes in the message. I explain this in Section IX.A.3.f above, which I incorporate by reference.

g. **1[g]. “allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate”**

283. In my opinion, LB-031 and Mazzoni disclose limitation 1[g]. *See, e.g.*, LB-031, pp. 2-3, 5, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 5:21-30; col. 5:61-67; col. 6:19-50; col. 10:22-42; Fig. 3.

284. LB-031 discloses allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate. I explain this in Section IX.A.3.g above, which I incorporate by reference.

285. Mazzoni also discloses allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at

a second data rate. Specifically, Mazzoni discloses that “[t]he deinterleaving means . . . have a structure analogous to that which has just been described for the interleaving means,” but “the indices of the branches are reversed so that the longest interleaving time-delay corresponds to the shortest deinterleaving time-delay.” Mazzoni at col. 5:49-55. Mazzoni explains that “[t]he deinterleaving means MDET incorporated in the operator terminal TO have I' branches, the branch with index i' having a length equal to $i' \times M'$ bytes.” *Id.* at col. 5:55-57. Claim 13 of Mazzoni recites “[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: . . . assigning a first memory space of the shared memory for interleaving and a second memory space of the shared memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device; performing Reed-Solomon coding and decoding for a length N of the digital data;”

286. Therefore, it is my opinion that LB-031 and Mazzoni both disclose allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate.

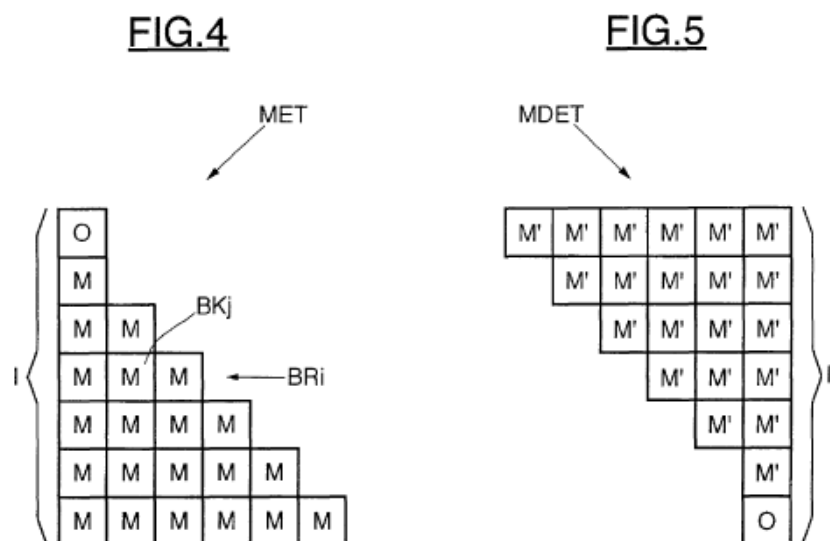
h. 1[h]. “interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver”

287. In my opinion, LB-031 and Mazzoni disclose limitation 1[h]. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 4:36-44; col. 6:51-8:10.

288. LB-031 discloses interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver. I explain this in Section IX.A.3.h above, which I incorporate by reference.

289. Mazzoni also discloses interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver. For example, Mazzoni discloses that the interleaver operates as follows: “The first block of M bytes (having the index 0, for example) is not interleaved and is delivered unmodified to the output of the interleaving means. The next block of M bytes (index 1) is delivered to the input of the branch BR1, and so on up to the seventh block of M bytes (index 6), which is delivered to the branch BR6. The cycle then begins again with the blocks of bytes with indices from 7 to 13. The preceding blocks of bytes are either delivered to the output of the interleaving means or moved forward by one block BKj in the branch concerned.” Mazzoni at col. 5:39-48; *see also id.* at FIG. 4. Mazzoni explains that the deinterleaver operates similarly. *Id.* at col. 5:49-57.

290. FIGS. 4 and 5 of Mazzoni, copied below, and the associated text illustrate the process of interleaving and deinterleaving.



291. In addition, claim 13 of Mazzoni recites “[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the

method comprising: interleaving and deinterleaving the digital data; . . . performing Reed-Solomon coding and decoding for a length N of the digital data; and the interleaving providing convolutional interleaving of I branches with $i-1$ blocks of M bytes, and the deinterleaving providing convolutional deinterleaving with I' branches of $i'-1$ blocks of M' bytes, with I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.”

292. Therefore, in my opinion, LB-031 and Mazzoni disclose interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

i. **1[i]. “wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver”**

293. It is my opinion that LB-031 and Mazzoni disclose limitation 1[i]. See, e.g., LB-031, p. 3; Mazzoni, col. 1:59-65; col. 6:21-30; col. 5:61-67; col. 10:22-42; col. 3:43-48; col. 6:51-8:10; Fig. 7, 8.

294. LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. I explain this in Section IX.A.3.i above, which I incorporate by reference.

295. Mazzoni also discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. I understand that the Court has construed the term “the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]” as “the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory.” Mazzoni

discloses that the shared memory is a dual-port memory. *See, e.g.*, Mazzoni at col. 2:57-58 (“The memory may be a random access memory, such as a dual-port memory, for example.”); *id.* at col. 5:58-67 (“the interleaving means and the deinterleaving means include common memory means MM, e.g., a dual-port random access memory. The memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 is assigned to the deinterleaving means MDET.”); claim 7 (“The device according to claim 1 wherein said memory comprises a dual-port memory.”); claim 12 (“The device according to claim 8 wherein said random access memory comprises a dual-port memory.”). As would have been appreciated by a person having ordinary skill in the art as of the Family 3 patents’ priority date, a dual-port memory is a memory that can be read from and written to at the same time. Through this disclosure, a skilled artisan would have understood Mazzoni to disclose that the shared memory allocated to the interleaver is read to, written from, or holds data at the same time as the shared memory allocated to the deinterleaver is read to, written from, or holds data.

296. In addition, claim 13 of Mazzoni recites “[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: interleaving and deinterleaving the digital data; . . . and the interleaving providing convolutional interleaving of I branches with $i-1$ blocks of M bytes, and the deinterleaving providing convolutional deinterleaving with I' branches of $i'-1$ blocks of M' bytes, with I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.”

297. Thus, LB-031 and Mazzoni both disclose that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

Consequently, the combination of LB-031 and Mazzoni discloses every limitation of claim 1 of the '048 patent.

4. Claim 5 of the '381 Patent

298. It is my opinion that claim 5 of the '381 patent is rendered obvious by LB-031 in combination with Mazzoni.

a. 5[a]. “A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver”

299. To the extent that it is limiting, it is my opinion that LB-031 discloses the preamble. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:8-27; col. 1:54-65; col. 1:59-65; col. 2:3-21; col. 5:58-67.

300. LB-031 discloses the use of an interleaver pair in a VDSL2 VTU-O and VTU-R. *See id.* at p. 3. Similarly, Mazzoni discloses a VDSL transceiver that includes a channel coder/decoder. *See* Mazzoni, col. 1:8-27; col. 2:3-19. One of ordinary skill in the art would have understood that source code and instructions for such transceivers could be stored on computer-readable information storage media, and could be executed by a processor, for example, as source or object code. I discuss how LB-031 in combination with Mazzoni discloses allocating shared memory in a transceiver above with respect to claim 1 of the '048 patent, which I incorporate here by reference. *See* Section IX.B.3.a. I describe how LB-031 in combination with Mazzoni discloses a transceiver above at Section IX.B.3.b, which I also incorporate by reference. Thus, LB-031 and Mazzoni disclose the preamble of claim 5.

- b. 5[b]. “transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver”

301. In my opinion, LB-031 in combination with Mazzoni discloses limitation 5[b].
See, e.g., LB-031, pp. 3, 4, 6; Mazzoni, col. 1:19-27.

302. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation. If the Court or other trier of fact interprets the claim such that sending or receiving the O-PMS message meets this limitation, however, then the combination of LB-031 and Mazzoni discloses this limitation under such an interpretation of the claims.

303. Above at Section IX.B.3.c, I describe how LB-031 in combination with Mazzoni discloses this limitation, and I incorporate this discussion by reference. Further, LB-031 discloses that “[t]ypically, for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same.” *Id.* at 2. One of ordinary skill in the art would have understood that the relationships described in LB-031 between delay, interleaver memory size, data rate and other transmission parameters are for an interleaver or a deinterleaver. In addition, Mazzoni notes that “everything just described here for the terminal TO applies to the terminal TU with deinterleaving means with I branches and interleaving means with I’ branches.” Mazzoni, col. 8:3-5. Thus its discussion of the process for allocating memory to an interleaver would be equally applicable to a deinterleaver. Thus is it my opinion that LB-031 in combination with Mazzoni discloses this limitation.

c. **5[c]. “determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory”**

304. LB-031 in combination with Mazzoni discloses limitation 5[c], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4; Mazzoni, col. 1:46-2:2; col. 2:6-17; col. 2:25-36; col. 4:18-22; col. 5:21-30; col. 5:58-67; col. 6:19-50.

305. Above at Section 269, I describe how LB-031 in combination with Mazzoni discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, and I incorporate my discussion and opinions by reference. LB-031 discloses the relationship between the memory required by an interleaver and a deinterleaver, as I described above with respect to the previous limitation. *See id.* at p. 3. Mazzoni discloses determining an amount of memory based on a data rate. Mazzoni, col. 4:18-22; col. 5:21-30. Accordingly, LB-031 in combination with Mazzoni discloses to one of ordinary skill in the art how to determine, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

d. **5[d]. “allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate”**

306. In my opinion, LB-031 in combination with Mazzoni discloses limitation 5[d]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 5:21-30; col. 5:61-67; col. 6:19-50, col. 10:22-42.

307. Above at Section IX.B.3.e, I explain how LB-031 and Mazzoni disclose allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. In

addition, at Section 282 above, I explain how LB-031 in combination with Mazzoni discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate. I incorporate both of these discussions by reference, and on that basis, it is my opinion that LB-031 in combination with Mazzoni discloses this limitation.

e. **5[e]. “wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message”**

308. In my opinion, LB-031 in combination with Mazzoni discloses limitation 5[e].
See, e.g., LB-031, pp. 2-3, 4, 5, 6; Mazzoni, col. 1:19-27.

309. I have reviewed TQ Delta’s infringement contentions, and understand that TQ Delta contends that the “maximum number of bytes specified in the message” is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta’s infringement position. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta’s contentions, however, LB-031 in combination with Mazzoni discloses this limitation in my opinion.

310. Above at Section IX.B.3.f, I explain how LB-031 discloses wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message, and I incorporate that discussion by reference. In the same way that the VTU-O or VTU-R of LB-031 and Mazzoni would not allocate more memory for the interleaver than is specified in the messages that it exchanges during initialization, the transceiver would also not allocate more memory for the deinterleaver than in specified in the messages that it exchanges during initialization, in my opinion.

- f. **5[f]. “allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate”**

311. LB-031 in combination with Mazzoni discloses limitation 5[f], in my opinion. See, e.g., LB-031, pp. 2-3, 5, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 6:19-50; col. 5:61-67; col. 10:22-42; Fig. 6.

312. Above at Section 282, I explain how LB-031 with Mazzoni allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes transmitted at a second data rate. Also, at Section IX.B.3.e above, I explain how LB-031 and Mazzoni disclose allocating a first number of bytes of the shared memory to an interleaver to interleave a first plurality of RS coded data bytes transmitted at a first data rate. I incorporate both of those sections herein by reference, and, on that basis, it is my opinion that the combination of LB-031 and Mazzoni discloses limitation 5[f].

- g. **5[g]. “deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver”**

313. LB-031 in combination with Mazzoni, in my opinion, discloses limitation 5[g]. See, e.g., LB-031, p. 3, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 4:36-44; col. 6:51-8:10.

314. Above at Section IX.B.3.h, I explain how LB-031 in combination with Mazzoni discloses interleaving a first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference. Though this limitation recites a first plurality being deinterleaved, and a second plurality of data bytes being interleaved, in my opinion, there is no difference in how a

transceiver would implement this limitation. It is my opinion that LB-031 in combination with Mazzoni discloses this limitation.

h. 5[h]. “wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver”

315. LB-031 in combination with Mazzoni discloses limitation 5[h], in my opinion. *See, e.g.*, LB-031, pp. 3, 6; Mazzoni, col. 1:59-65; col. 6:21-30; col. 5:61-67; col. 10:22-42; col. 3:43-48; col. 6:51-8:10.

316. I explain above at Section IX.B.3.i how it is my opinion that LB-031 and Mazzoni disclose wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference herein. In my opinion, one of ordinary skill in the art would have understood that there is no difference in these two limitations, i.e., they both require that the deinterleaver and interleaver memory be used at the same time. Accordingly, it is my opinion that this limitation is met by LB-031 and Mazzoni.

5. Claim 13 of the '882 patent

317. In my opinion, LB-031 in combination with Mazzoni discloses each limitation of claim 13 of the '882 patent, as I explain below.

a. 13[a]. “A system that allocates shared memory”

318. To the extent that this preamble is limiting, LB-031 in combination with Mazzoni discloses a system that allocates shared memory. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:54-65; col. 2:3-21; col. 5:58-67. This limitation is identical to the preamble of Claim 1 of the '048 patent, and, for the same reasons, it is my opinion that this limitation is disclosed by LB-031 and Mazzoni. *See* Section IX.B.3.a.

b. 13[b]. “a transceiver that performs”

319. In my opinion, LB-031 in combination with Mazzoni discloses limitation 13[b]. *See, e.g.*, p. 3, 4; Mazzoni, col. 1:8-27. This limitation is identical to the second limitation of Claim 1 of the '048 patent, except that it recites “a transceiver capable of” additional steps. In my opinion, this limitation is met for the same reasons that I explain above at Section IX.B.3.b, and I incorporate my discussion and opinions herein by reference.

c. 13[c] through 13[i]

320. Limitations 13[c] through 13[i] of claim 13 of the '882 patent are substantially identical to limitations 5[b] through 5[h] of claim 5 of the '381 patent. *See* Appx. 3 (comparing claim limitations of claim 13 of the '882 patent with claim limitations of claim 5 of the '381 patent). I incorporate by reference my opinions with respect to those limitations set forth in Sections IX.B.3.c through IX.B.3.i (claim 1) and Sections IX.B.4.b through IX.B.4.h (claim 5). For the same reasons, it is my opinion that limitations 13[c] through 13[i] are met by LB-031 and Mazzoni.

6. Claim 19 of the '473 Patent

321. In my opinion, claim 19 of the '473 patent is obvious over LB-031 in combination with Mazzoni.

a. 19[a]. “An apparatus comprising”

322. To the extent that the preamble is limiting, LB-031 and Mazzoni discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, LB-031, pp. 3, 4.

b. 19[b]. “a multicarrier communications transceiver”

323. It is my opinion that LB-031 in combination with Mazzoni discloses limitation 19[b]. *See, e.g.*, LB-031, pp. 3, 4; Mazzoni, col. 1:8-27.

324. LB-031 describes the use of a VDSL2 VTU-O and VTU-R to implement its equations and systems for allocating memory, which one of ordinary skill in the art would have understood to be VDSL2 transceivers. *Id.* at 3. LB-031 further provides an example of calculating and allocating interleaver memory in a VDSL2 transceiver. *Id.* at 4. I understand that the Court construed the term “transceiver” to mean “communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.” One of ordinary skill in the art would have understood that VDSL2 transceivers described in LB-031 both transmit and receive data (i.e., to be interleaved and deinterleaved), and share common circuitry such as a memory.

325. LB-031 generally deals with VDSL2, which one of ordinary skill in the art would have understood to be a multicarrier communications system. Moreover, LB-031 describes the use of DMT symbols, and one of ordinary skill in the art would have understood DMT to be a type of multicarrier communications system. LB-031 at p. 4 (“Similar to the interleaver delay, we propose that the maximum number of codewords in a DMT symbol (or per unit time) also scale with the data rate).

326. Mazzoni similarly discloses its invention “may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system,” which a person having ordinary skill in the art would have understood to include VDSL2 transceivers. Mazzoni, col. 1:19-21. Mazzoni further discloses that its invention can transmit and receive data, as it “provides a device for sending/receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication systems).” *Id.* at col. 1:65-2:2. Mazzoni provides a depiction of two “send/receive devices TO and TU according to the invention.” *Id.* at col. 3:53-

61, Fig. 1. One of ordinary skill in the art would have understood these devices to be transceivers.

327. Mazzoni also discloses that in its invention, at least some circuitry is shared between the transmit and receive portions, specifically, a common memory for interleaving and deinterleaving. *Id.* at col. 2:2-13 (“The device according to the invention may include a coding/decoding stage (generally referred to by those skilled in the art as a ‘channel coding/decoding stage’) including interleaving means and deinterleaving means. The interleaving and deinterleaving means include a memory whose minimum size is fixed as a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system). The memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means.”). The “memory” associated with the interleaving and deinterleaving means is common circuitry shared by the transmitter and receiver portions.

328. Mazzoni further discloses a VDSL system, which one of ordinary skill in the art would have understood to include a multicarrier communications transceiver.

c. **19[c]. “that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path”**

329. In my opinion, LB-031 in combination with Mazzoni discloses limitation 19[c]. *See, e.g.*, LB-031, pp. 2-3; Mazzoni, col. 3:62-4:25.

330. LB-031 describes the use of VDSL2 transceivers, a VTU-O and a VTU-R. *Id.* at p. 3. I understand that the Court has construed the term “latency path” to mean “transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay.” One of ordinary skill in the art would have understood that LB-031 discloses a multiple latency paths within a VTU-O or VTU-R, because a VTU-O transmits data downstream and receives

data upstream, and, similarly, a VTU-R transmits data upstream and receives data downstream. LB-031 describes that the operation of convolutional interleaver/deinterleaver pairs imposes an end-to-end interleaver delay (or latency) on their respective latency paths. *Id.* at 2. Thus, one of ordinary skill in the art would have understood LB-031 to disclose at least two latency paths, one downstream and one upstream.

331. Mazzoni discloses that “the VDSL communication system enables the operator to provide symmetrical services, typically six symmetrical services S1-S6.” Mazzoni, col. 3:62-64. Mazzoni also discloses that “the operator can also provide asymmetrical services A1-A6. These are services with different information bit rates in the user to operator direction (uplink direction) and in the operator to user direction (downlink direction).” *Id.* at col. 4:3-7. One of ordinary skill in the art would have understood the disclosure of asymmetrical and symmetrical services to require multiple latency paths (i.e., at least one latency path in the downstream direction and at least one latency path in the upstream direction), and, in turn, interleaving and deinterleaving functions for the respective latency paths.

d. 19[d]. “the multicarrier communications transceiver being associated with a memory”

332. In my opinion, LB-031 in combination with Mazzoni discloses limitation 19[c]. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:59-2:24; col. 2:37-48; col. 2:57-3:4; col. 5:9-20; Fig. 3, 4, 5.

333. LB-031 describes an interleaver memory associated with a VDSL2 transceiver. LB-031 at p. 3 (“The size of the interleaver memory will be a major source of complexity in VDSL2.”); *see also id.* at p 2 (“the smallest possible memory for either the interleaver or deinterleaver is [half of the overall delay of the interleaver/deinterleaver pair]”). LB-031 further explains that the amount of memory required is “implementation specific,” and provides

examples of delay constraints/requirements and the amounts of memory required to support them. *Id.* at 3, 4.

334. Mazzoni similarly discloses a memory associated with the multicarrier communications transceiver. Mazzoni, col. 2:6-10 (“The interleaving and deinterleaving means include a memory whose minimum size is a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system).”); col. 2:57-60 (“The memory may be a random access memory, such as a dual-port memory, for example. The interleaving means and the deinterleaving means may respectively include first addressing means and second addressing means.”); *see also id.* at Fig. 4, 5. Thus, Mazzoni in combination with LB-031 discloses this limitation.

- e. **19[e]. “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”**

335. LB-031 in combination with Mazzoni discloses limitation 19[e], in my opinion. *See, e.g.*, LB-031, pp. 3, 6; Mazzoni, col. 1:59-65; col. 2:3-18; col. 5:21-30.

336. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta’s infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then LB-031 in combination with Mazzoni discloses this limitation under TQ Delta’s interpretation of the claims.

337. LB-031 discloses that “the VTU-O and VTU-R must exchange the interleaver delay in terms of octets.” *Id.* at 3; *see also* 6 (“interleaver delay in terms of octets should be

exchanged between the VTU-O and VTU-R, the delay in octets should meet the minimum requirements in terms of delay in time.”). One of ordinary skill in the art would have understood that this information would be exchanged as part of a message received during initialization, because the “interleaver delay” would be exchanged prior to the receivers entering Showtime and exchanging user data. Furthermore, LB-031 discloses the VDSL2 transceivers indicating their capabilities during initialization. *See id.* at 4 (“During initialization, the VDSL2 transceiver would indicate that it could support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay.”).

338. It is my understanding that the Court construed the term “memory is allocated between the interleaving function and the deinterleaving function” to mean “an amount of memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function.” LB-031 discloses that “the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver, and that “for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same.” *Id.* at LB-031 at p. 2. LB-031 also explains the dependence of end-to-end delay of the interleaver/deinterleaver pair depends on line rate, Reed Solomon codeword size, and other parameters. *Id.* One of ordinary skill in the art would have understood that LB-031 discloses allocating the memory between an interleaving function and a deinterleaving function using the total delay of the interleaver/deinterleaver pair in the downstream direction and using the total delay of the interleaver/deinterleaver pair in the upstream direction.

339. In addition, Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that “can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).” Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses

that “the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means” are determined “according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I' and M').” *Id.* at col. 5:24-31. One of ordinary skill in the art would have understood that this information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, and that the memory would be allocated between the interleaving function and the deinterleaving function in accordance with that message.

f. **19[f]. “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

340. LB-031 in combination with Mazzoni discloses limitation 19[f] in my opinion. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:59-65; col. 2:3-18; col. 5:21-30.

341. LB-031 discloses interleaving and deinterleaving for VDSL2 transceivers. *See, e.g.*, LB-031 at pp. 1-3. As a person having ordinary skill in the art as of the priority date of the Family 3 patents would have understood, VDSL transceivers transmit and receive data at the same time (i.e., the VTU-O transmits downstream and receives upstream at the same time, and the VTU-R transmits upstream and receives downstream at the same time). Thus, LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

342. In addition, LB-031 discloses that the portion of the memory allocated to the interleaving function or the deinterleaving function at any one particular time is dependent on the message. *See, e.g.*, LB-031 at p. 3 (“the VTU-O and VTU-R must exchange the interleaver delay in terms of octets.”); *id.* at p. 4 (“During initialization, the VDSL2 transceiver would

indicate that it could support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay.”); *id.* at p. 2 (“the smallest possible memory for either the interleaver or deinterleaver is [half of the overall delay of the interleaver/deinterleaver pair]”).

343. Mazzoni also discloses a memory that can be shared between the interleaving and deinterleaving means. Mazzoni, col. 1:59-65 (“These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).”); col. 2:57-50 (“The memory may be a random access memory, such as a dual-port memory, for example. The interleaving means and the deinterleaving means may respectively include first addressing means and second addressing means.”). One of ordinary skill in the art would have understood that the interleaving means and the deinterleaving means would operate at the same time.

344. Mazzoni also discloses that the portion of the memory allocated to the interleaving function or the deinterleaving function at any one particular time is dependent on the message. For example, Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that “can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).” Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that “the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means” are determined “according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I' and M').” *Id.* at col. 5:24-31.

7. **Motivation to Combine LB-031 and Mazzoni**

345. As of the priority date of the Family 3 patents, a person having ordinary skill in the art would have been motivated to combine the teachings of Mazzoni with the teachings of LB-031 in the manner recited in the asserted claims.

346. First, both Mazzoni and LB-031 disclose VDSL transceivers. *See, e.g.*, LB-031 at p. 1 (Title) (“VDSL2 – Constraining the Interleaver Complexity”); *id.* at p. 4 (“During initialization, the VDSL2 transceiver would indicate that it could support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay.”); Mazzoni at col. 1:19-22 (“The present invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system, for example, though the invention may also be used in other applications.”).

347. Second, both Mazzoni and LB-031 are concerned with limiting the size of memory used for interleaving and deinterleaving. *See, e.g.*, LB-031 at p. 1 (“The interleaver is a major source of complexity in VDSL2. We propose that the interleaver delay in time be restricted rather than restricting the depth as in ADSL2. This allows . . . lower complexity implementations for profiles that do not require the full VDSL2 data rate.”); Mazzoni at col. 1:39-43 (“The processes of interleaving and deinterleaving data sent and received by a modem necessitates the use of memories. For a modem intended to operate at a predetermined bit rate, the memories must have a capacity that depends on that bit rate.”); *id.* at col. 1:47-49 (“An object of the invention is to provide a send/receive device (i.e., modem) architecture which requires a reduced quantity of memory.”).

348. To the extent that LB-031 does not explicitly disclose the use of shared memory to reduce interleaver complexity and cost, Mazzoni describes a method of implementing shared memory to reduce the amount of memory required. As of the priority date of the Family 3

patents, one of ordinary skill in the art would have been motivated to look to Mazzoni, in view of the teachings of LB-031, to reduce the complexity of an interleaver.

349. Mazzoni discloses that the amount of memory required for interleaving and deinterleaving, and therefore the “sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means,” depends on the downstream and upstream interleave depth (denoted in Mazzoni as I for the interleaver and I' for the deinterleaver), block length (denoted in Mazzoni as M for the interleaver and M' for the deinterleaver), and bit rates, which can be symmetric or asymmetric. Mazzoni at col. 5:21-30; *id.* at col. 2:19-24. *See also id.* at col. 2:13-15 (“The size of each of the two memory spaces is set as a function of the bit rate actually processed by the device.”). As a person having ordinary skill in the art would have understood, the parameters I , M , I' and M' would need to be chosen so as not to exceed the size of the shared memory given the bit rate processed by the transceiver.

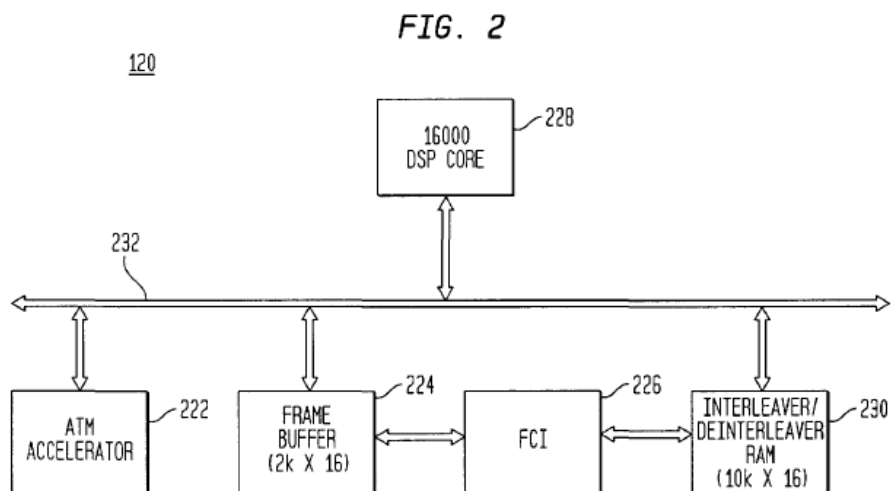
350. LB-031 teaches the VTU-O and VTU-R exchanging the interleaver delay in terms of octets for this exact reason, i.e., so that the VTU-O and VTU-R can then “select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities.” LB-031 at p. 3. Like Mazzoni, LB-031 also teaches that the amount of memory required for interleaving and deinterleaving depends on the line data rate. *Id.* at p. 4. Thus, a skilled artisan wishing to implement the VDSL transceiver of Mazzoni would have been motivated to include the initialization message of LB-031 so that the VTU-O and VTU-R of Mazzoni could choose values for the parameters I , M , I' and M' that would not exceed the size of the shared memory at the selected downstream and upstream bit rates.

C. The Asserted Claims Are Obvious Over Fadavi-Ardekani in Combination With ITU-T Recommendation G.993.1

351. It is my opinion that U.S. Patent No. 6,707,822 (Fadavi-Ardekani), in combination with either ITU-T Recommendation G.993.1 (“G993.1”) renders obvious each of claim 1 of the ’048 patent, claim 5 of the ’381 patent, claim 13 of the ’882 patent, and claim 19 of the ’473 patent. Furthermore, one of ordinary skill in the art would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.993.1, as I describe below in Section IX.C.7. I have reviewed TQ Delta’s infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions, and I do not agree with its infringement read. If the Court or other trier of fact does agree with TQ Delta’s interpretation of the claims, however, then Fadavi-Ardekani in combination with G.993.1 renders obvious the asserted claims of the Family 3 patents.

1. Brief Description of Fadavi-Ardekani

352. Fadavi-Ardekani describes a transceiver for asymmetric communication systems, such as ADSL, that implements a buffering and scheduling scheme to allow a single transceiver to synchronize data processing between multiple asynchronous ADSL sessions corresponding to different ADSL lines. Fadavi-Ardekani at Abstract; col. 2:47-67. FIG. 2 of Fadavi-Ardekani, copied below, shows an ADSL transceiver in accordance with Fadavi-Ardekani’s invention. *Id.* at col. 3:65-67.



353. The transceiver includes three functional elements (a DSP core, a framer/coder/interleaver (FCI), and an ATM accelerator) and two memories (a frame buffer (FB) and an interleave/deinterleave memory (IDIM)) coupled together. *Id.* at col. 3:5-7; col. 5:23-28. The DSP core generates a virtual clock signal that is used to synchronize the signal processing tasks of the transceiver, i.e., to control the operation of the ATM accelerator and the FCI. *Id.* at col. 3:7-8; col. 3:20-23; col. 6:27-29. The virtual clock signal has a frequency of approximately 4 kHz, which is the DMT symbol rate in ADSL. *Id.* at col. 3:20-23; col. 6:29-31. The DSP core controls operation of both the ATM accelerator and the FCI, and it manages the transfer of data to and from the FB and IDIM. *Id.* at col. 3:23-25.

354. The ATM accelerator “provides the network interface to multiple ATM channels for multiple asynchronous ADSL sessions.” *Id.* at col. 3:8-11. It “provides those functions that are responsible for data transport for a plurality of data streams communicated via twisted pair media.” *Id.* at col. 5:41-45. Among other things, the ATM accelerator assigns data to an appropriate bearer channel “as determined by the ADSL standard,” “subjects this framed data to various operations that calculate a plurality of complex numbers representing DMT tones,” and “subsequently transfers this DMT tone data on the twisted-pair media.” *Id.* at col. 5:45-54.

355. The FCI performs various processing tasks on the frame data that are required by the ADSL standards, including “framing/de-framing, cyclic redundancy check generation/checking (CRCing), scrambling/de-scrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving.” *Id.* at col. 6:11-16; col. 6:19-20. A preferred embodiment of the FCI is able to support approximately four T1.413 Issue 2 sessions (i.e., lines) or four G.992.2 sessions at one time. *Id.* at col. 6:20-23.

356. The FB provides a dual access memory used by the DSP core to transfer unframed bearer channel data between the ATM accelerator and the FCI. *Id.* at col. 5:57-60.

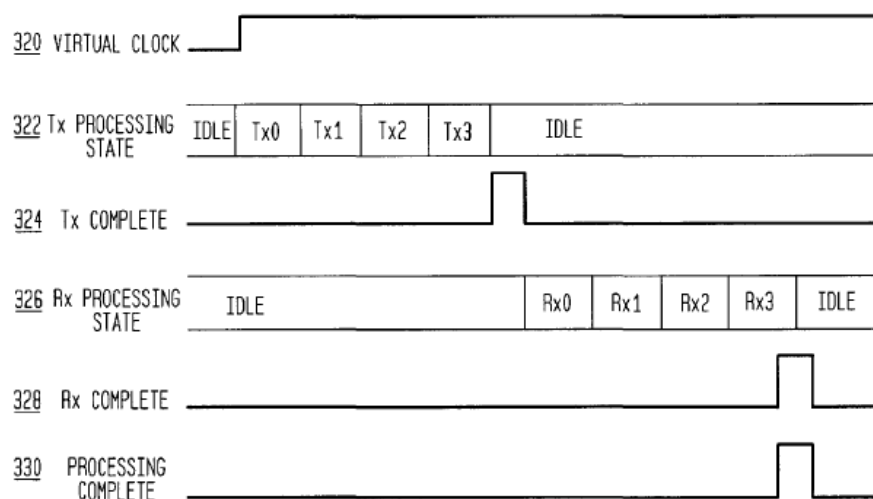
357. The IDIM provides a memory used by the DSP core to transfer data frames to and from the FCI for interleaving and deinterleaving. *Id.* at col. 6:55-60. In addition to storage for interleaving, the IDIM may include a dedicated area enabling the transfer of fast path data (i.e., non-interleaved data) between the FCI and the DSP core. *Id.* at col. 60-62. Fadavi-Ardekani teaches that “[t]he size of the IDIM and the interleave depth [of the ADSL sessions] may be varied so that a different number of sessions may be supported by the transceiver of the invention.” *Id.* at col. 7:3-5. In an “optimal implementation of the interleaver,” Fadavi-Ardekani teaches using “the same memory for receive data and transmit data” using a 20-kbyte IDIM, which is sufficient to support “a standard ADSL session at full interleave depth” or more than one session with each using a smaller interleave depth. *Id.* at col. 7:25-32.

358. Both the FB and IDIM are used in what Fadavi-Ardekani refers to as “a ping-pang fashion, based on the logic level of the virtual clock.” *Id.* at col. 3:13-17; col. 6:57-58. “Ping-pang fashion” means that “areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent.” *Id.* at col. 5:60-63. Fadavi-Ardekani explains that within a common memory, “[a]s one

area of memory is being used by a first agent, another area of memory can be used by a different agent,” and “[a]s long as different agents . . . access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors.” *Id.* at col. 5:63-6:1. At any given time, “an agent is allowed to access either a ping area of memory or a pang area of memory based on the logic level of the virtual clock signal.” *Id.* at col. 6:1-4.

359. In operation, during each virtual clock cycle, the transceiver completes a sequence that processes the data associated with however many lines are connected to the transceiver, including both the transmit (“TX”) data and the receive (“RX”) data. *Id.* at col. 7:46-53; col. 7:63-8:4. For interleaving and deinterleaving, “the DSP core needs to load one or more frames of RX [receive] data to the IDIM and read one or more frames of TX [transmit] data from the IDIM.” *Id.* at col. 7:46-53. As a person having ordinary skill would have understood on the Family 3 patents’ priority date, this disclosure means that during each of the virtual clock cycles (i.e., during each DMT symbol period), one frame of receive data for each connected line is loaded to the IDIM for deinterleaving by the FCI, and one frame of transmit data for each connected line is loaded to the IDIM for interleaving by the FCI.

360. FIG. 3 of Fadavi-Ardekani, copied below, illustrates the processing sequence enabling the transceiver to service four lines. *Id.* at col 4:1-2. As shown in FIG. 3, during each virtual clock cycle, “the transceiver first steps through ADSL lines, performing FCI transmit-processes for each active ADSL line and generating a control signal after completing all transmit-processes,” and “[t]he FCI then again steps through ADSL lines, processing receive-processes for all active ADSL lines and generating control signals indicating completion of receive processes and completion of all processing.” *Id.* at 26-35.

FIG. 3

361. The FCI processing is initiated by the transition of the virtual clock 320, shown as an upward transition in FIG. 3. The FCI begins each virtual clock cycle by processing the transmit data for each line in sequence (shown in the line of FIG. 3 labeled 322). *Id.* at col. 8:22-26. At the end of the TX processing cycle, one frame of transmit data for each line resides in the IDIM. *Id.* at col. 8:30-33. After completing the TX processing cycle (indicated by the pulse shown in the line of FIG. 3 labeled 324), and still within the same virtual clock cycle, the FCI processes the receive data. *Id.* at col. 8:34-35. The FCI steps through each line in sequence (shown in the line of FIG. 3 labeled 326). *Id.* at col. 8:35-37.

362. While the FCI is performing the TX processing during the first part of the virtual clock cycle, “the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory.” *Id.* at col. 8:62-65. Similarly, while the FCI block is performing the RX processing during the second part of the virtual clock cycle, “the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.” *Id.* at col. 8:67-9:3.

363. Fadavi-Ardekani was filed as an application on January 7, 2000, and was published when it issued on March 16, 2004. I understand that it is prior art to the Asserted Family 3 Patents.

2. Brief Description of G.993.1.

364. I provide a description of G.993.1 above at Section VII.F.4, which I incorporate here by reference.

365. I understand that G.993.1 was approved no later than June of 2004, although numerous prior versions of G.993.1 were in circulation and were made available to the relevant public before then. I understand that it is prior art to the Asserted Family 3 Patents.

366. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then G.993.1 renders obvious the asserted claims of the Family 3 patents when combined with other references as I explain below.

3. Claim 1 of the '048 Patent

367. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses each limitation of claim 1 of the '048 patent, as I describe below.

a. 1[a]. "A system that allocates shared memory"

368. To the extent that this preamble is limiting, Fadavi-Ardekani discloses a system that allocates shared memory, in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55:65; col. 7:25-30; col. 8:58-9:3.

369. Fadavi-Ardekani discloses an ADSL system that includes an Interleave/De-Interleave Memory (IDIM) and a framer/coder/interleaver (FCI) that uses the IDIM for interleaving and deinterleaving. Fadavi-Ardekani, Abstract ("A transceiver for an asymmetric

communication system is provided that implements a buffering and scheduling scheme that uses a virtual clock signal to synchronize processing of asynchronous frame data for multiple ADSL sessions The FCI also interfaces a Digital Signal Processing (DSP) core through an Interleave/De-Interleave Memory (IDIM). . . . IDIM holds DMT frames of data and may also be utilized in a ping-pang fashion. . . . Memory is shared by multiple ADSL sessions and for the transmit and receive processes within an individual session.”); *see also id.* at Fig. 2; col. 3:5-25. Fadavi-Ardekani explains that “‘ping-pang’ means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent,” so that within a shared memory, “[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent.” *Id.* at col. 5:60-65.

370. The FCI “supports multiple ADSL sessions,” and performs functions including “Reed-Solomon encoding/decoding.” *Id.* at col. 6:9-15. The FCI accesses the Interleave/De-Interleave Memory (IDIM), which “holds DMT frames of data and may be utilized in a ping-pang fashion . . . to transfer framed, coded and possibly interleaved data frames between the FCI core and the DSP Core.” *Id.* at col. 6:55-60. Fadavi-Ardekani explains that “the DSP core may load new DMT frames of [receive] data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory.” *Id.* at col. 8:62-65.

371. One of ordinary skill in the art would have understood the IDIM to be “shared memory.” I understand that the Court has construed this term to mean “common memory used by at least two functions, where a portion of the memory can be used by either one of the functions.” The IDIM of Fadavi-Ardekani meets this limitation because it “holds DMT frames

of data and may be utilized in a ping-pang fashion.” *Id.* at col. 6:57-58. According to Fadavi-Ardekani, “‘ping-pang’ means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of memory is being used by a first agent, another area of memory can be used by a different agent.” *Id.* at col. 5:60-65. When the memory is used in ping-pang fashion, “[a]s long as different agents . . . access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors.” *Id.* at col. 5:65-6:1. A clock signal governs whether “an agent is allowed to access either a ping area of memory or a pang area of memory.” *Id.* at col. 6:1-4. Thus, in my opinion, the IDIM described in Fadavi-Ardekani is a “shared memory.”

372. Fadavi-Ardekani further describes allocating the IDIM memory between transmit and receive functions. *Id.* at col. 7:25-30 (“An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path).”); col. 8:58-9:3 (“The IDIM may also be used in a ping-pang fashion by the FCI and the DSP core based on the virtual clock cycle. For example, between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX[receive] data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory. Between the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.”).

373. Thus, it is my opinion that Fadavi-Ardekani discloses the preamble.

b. 1[b]. “a transceiver that is capable of”

374. In my opinion, Fadavi-Ardekani discloses a transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67. I understand that the Court has construed the term “transceiver” to mean “communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.”

375. The central office ADSL transceiver of Fadavi-Ardekani is a communications device capable of transmitting and receiving data. Fadavi-Ardekani discloses “[a] transceiver for an asymmetric communication system . . . that implements a buffering and scheduling scheme that utilizes a virtual clock signal to synchronize processing of asynchronous frame data for multiple ADSL sessions.” *Id.* at Abstract; *see also id.* at col. 2:62-67. The central office ADSL transceiver is described as being “bi-directionally coupled” to a splitter and a digital network. *Id.* at col. 4:30-34. It includes, as shown in FIG. 2 of Fadavi-Ardekani, an ATM accelerator, which, among other things, “transfers [] DMT tone data on the twisted-pair media.” *Id.* at col. 5:52-54. FIG. 3 of Fadavi-Ardekani, shown above, “illustrates an exemplary processing sequencing for a case when four Transmit and Receive lines are enabled.” *Id.* at col. 4:1-2. One of ordinary skill in the art would have understood these disclosures to indicate that the transceiver is capable of transmitting and receiving data.

376. Fadavi-Ardekani further teaches that the transmitter and receiver portions share common circuitry, including the Asynchronous Transfer Mode (ATM) accelerator, frame buffer, framer/coder/interleaver, DSP core and interleave/deinterleave memory (IDIM). *Id.* at col. 5:23-40; *see also id.* at FIG. 2.

377. G.993.1 similarly discloses a transceiver, a VTU-O or VTU-R that is compliant with the G.993.1 standard. *See* G.993.1, §§ 5.2, 5.3, Fig. 5-2. Accordingly, it is my opinion that Fadavi-Ardekani and G.993.1 disclose this limitation.

c. **1[c]. “transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver”**

378. Fadavi-Ardekani in view of G.993.1 discloses limitation 1[c]. *See, e.g.*, G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.3.1.1.

379. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta’s infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then G.993.1 and Fadavi-Ardekani disclose this limitation under such an interpretation of the claims.

380. As explained above, the VDSL transceivers described in G.993.1 are capable of sending and receiving messages during initialization that specify communications parameters, including interleaver settings and capabilities. *See* G.993.1, § 12.4.1 (“Initialization of a VTU-O/VTU-R includes a variety of tasks. The set of tasks consists of: . . . exchange of parameters (RS settings, interleaver parameters, VOC settings, bit loading and energy tables . . .”). Initialization messages include R-MSG2, sent by the VTU-R, which “transmits information about [the connection’s] bit allocation capabilities and several other features,” including the “Maximal interleaver memory,” expressed in bytes. *Id.* at § 12.4.6.3.1.1; § 12.4.6.2.1.1 (Table 12-23). Thus, G.993.1 describes a transceiver, namely the VTU-R, transmitting a message during initialization (i.e., R-MSG2) specifying a maximum number of bytes of memory that are

available to be allocated to an interleaver (i.e., the VTU-R's interleaver). It also describes a transceiver, namely the VTU-O, receiving a message during initialization (i.e., R-MSG2) specifying the maximum number of bytes of memory that are available to be allocated to an interleaver (i.e., the VTU-R's interleaver).

381. Similarly, G.993.1 specifies that the VTU-O transmits the message O-MSG2. *Id.* at § 12.4.6 (Figure 12-7). O-MSG2 contains the field "Maximum interleaver delay," expressed in milliseconds. *Id.* at § 12.4.6.2.1.1 (Table 12-23). As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, the interleaver delay is a function of the bit rate and interleaver depth. Therefore, G.993.1 discloses a transceiver, namely the VTU-O, transmitting a message during initialization (i.e., O-MSG2) that meets this limitation under TQ Delta's interpretation of the claims. It also discloses a transceiver, namely the VTU-R, receiving a message during initialization (i.e., O-MSG2) that meets this limitation under TQ Delta's interpretation of the claims.

d. **1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory"**

382. Fadavi-Ardekani discloses limitation 1[d], in my opinion. *See, e.g.* Fadavi-Ardekani, col. 6:55-65; col. 6:66-7:33; col. 8:58-9:3; col. 6:10:15.

383. First, Fadavi-Ardekani discloses that the FCI performs Reed-Solomon coding on the data to be transmitted and decoding on received data. Fadavi-Ardekani, col. 6:10-15 ("The FCI Supports multiple ADSL sessions and performs various tasks on payload data including: framing/de-framing, cyclic redundancy check generation/checking (CRCing), scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving."). Second, Fadavi-Ardekani discloses that "[a]ll functionalities of the FCI are provided as per ADSL standards," which include G.992.2 and T1.413 Issue 2. *Id.* at col. 6:19-

23. As a skilled artisan would have understood as of the Family 3 patents' priority date, G.992.2 and T1.413 Issue 2 specify Reed-Solomon encoding.

384. Fadavi-Ardekani also discloses that the DSP core uses the IDIM to transfer frames to and from the FCI, (*see, e.g., id.* at col. 6:55-60), and that the IDIM is a shared memory. *See, e.g., id.* at col. 6:57-58 ("The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion."); col. 5:60-6:4 ("Ping-pang' means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of memory is being used by a first agent, another area of memory can be used by a different agent. As long as different agents . . . access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors. At any time, an agent is allowed to access either a ping area of memory or a pang area of memory based on the logic level of the virtual clock signal."); col. 8:58-9:3 ("The IDIM may also be used in a ping-pang fashion by the FCI and the DSP core based on the virtual clock cycle. For example, between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory. Between the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.").

385. Fadavi-Ardekani further discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory. *See, e.g., id.* at col. 6:55-65 ("The Interleave/De-Interleave Memory

(IDIM) 230 provides a memory through which the FCI 226 interfaces the DSP core 228. The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames between the FCI core and the DSP Core. In addition to interleave data storage, the IDIM may contain a dedicated area for the transfer of fast path data to the DSP Core. The IDIM may be organized as 16 bit words with byte write capability to allow beneficial performance of various interleave/de-interleave processes.”); col. 6:66-7:33 (“In a preferred embodiment of the invention, the IDIM is allocated as 10 K×16 (i.e., 20 K) Random Access Memory (RAM), which supports approximately four G.lite or approximately four standard ADSL session/s at less than full interleave depth. The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention. The size of the IDIM is derived as follows. A simple implementation of a transmit interleaver for G.lite communication requires 4 Kbytes per session for downstream processing, derived by multiplying the maximum codeword length by the maximum interleaver depth. The simple G.lite transmit interleaver also requires 2 Kbytes per session for upstream processing. Therefore, 24 Kbytes of RAM is required to support four G.lite sessions. Similarly, a simple implementation of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2 Kbytes per session for upstream processing, for a total of 72 Kbytes for four sessions. A fast path buffer is also required for fast path data in both the interleave and de-interleave processes and requires 256 bytes of RAM per session, or a total of 1 K bytes for four sessions. Since the smallest RAM block currently available is 1 K×16, 1 K×16 or 2 Kbytes must be allocated for the fast path buffer per direction. Therefore, a simple implementation of an interleaver would require 76 Kbytes for four standard ADSL sessions (64 K interleave +8 K de-interleave +4 K fast path).

An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path). With a lesser interleave depth, additional sessions may be supported with the same size buffer. With a larger buffer, additional session may be supported.”); *see also* col. 8:58-9:3.

386. Thus, it is my opinion that Fadavi-Ardekani discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory.

- e. 1[e]. “allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate”

387. It is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses limitation 1[e]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; col. 6:10-15; G.993.1, §§ 8.4.1.

388. As described above, Fadavi-Ardekani discloses the use of Reed-Solomon encoding. *See* Fadavi-Ardekani, col. 6:10-15. Fadavi-Ardekani also discloses that the FCI functions are in accordance with “ADSL standards,” such as G.992.2 and T1.413 Issue 2 (*id.* at col. 6:19-23), and that the “ADSL transceiver of the invention may alternatively incorporate other variations of DSL,” such as VDSL.

389. G.993.1 also discloses the transmitter interleaving the bytes of Reed-Solomon codewords. *See* G.993.1, § 8.4.1 (“Interleaving shall be used to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords. The interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255.”). The depth of the interleaver in G.993.1 is

adjustable, to meet latency requirements. *Id.* With respect to the memory needed for an interleaver and a deinterleaver, G.993.1 notes that “[t]he same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and de-interleaving at the receiver.” *Id.*

390. Fadavi-Ardekani discloses allocating a first number of bytes of a shared memory to an interleaver. Fadavi-Ardekani describes using the IDIM memory in a ping-pang fashion, where “[a]s one area of the memory is being used by a first agent, another area of the memory can be used by a different agent.” *Id.* at col. 5:60-63; col. 6:57-60 (“The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames the FCI core and the DSP core.”). A portion of the memory is then allocated to an interleaver to interleave a first plurality of Reed Solomon coded data bytes, by determining the size of the memory needed to interleave a certain amount of data. *Id.* at col. 7:3-33. And as Fadavi-Ardekani notes, “between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory,” and, similarly, “[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.” *Id.* at col. 8:60-9:3. As a person having ordinary skill in the art would have understood as of the Family 3 patents’ priority date, these disclosures indicate that a first number of bytes of the shared memory have been allocated to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate.

391. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses this limitation.

f. **1[f]. “wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message”**

392. In my opinion, Fadavi-Ardekani in view of G.993.1 discloses limitation 1[f].
See, e.g., G.993.1, §§ 8.4, 8.4.2, 12.4.1, 12.4.6.2.1.1.

393. I have reviewed TQ Delta’s infringement contentions, and I understand that TQ Delta contends that the “maximum number of bytes specified in the message” is met by the aggregate interleaver delay parameter and the O-PMS message. See G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta’s contentions or interpretation of the claims. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta’s contentions, however, G.993.1 in combination with Fadavi-Ardekani still discloses this limitation in my opinion.

394. As explained above, G.993.1 describes a transceiver, namely the VTU-R, transmitting a message during initialization (i.e., R-MSG2) specifying a maximum number of bytes of memory that are available to be allocated to an interleaver (i.e., the VTU-R’s interleaver). It also describes a transceiver, namely the VTU-O, receiving a message during initialization (i.e., R-MSG2) specifying the maximum number of bytes of memory that are available to be allocated to an interleaver (i.e., the VTU-R’s interleaver). It also describes a transceiver, namely the VTU-O, transmitting a message during initialization (i.e., O-MSG2) specifying a maximum number of bytes of memory that are available to be allocated to an interleaver (i.e., the VTU-O’s interleaver) according to TQ Delta’s infringement read. It also discloses a transceiver, namely the VTU-R, receiving a message (i.e., O-MSG2) during initialization specifying the maximum number of bytes of memory that are available to be

allocated to an interleaver (i.e., the VTU-O's interleaver) according to TQ Delta's infringement read.

395. Fadavi-Ardekani presents its disclosure in the context of G.992.2 and T1.413 Issue 2 but indicates that the transceiver may alternatively incorporate other variations of DSL, including VDSL, which a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood would include G.993.1. *See, e.g.*, Fadavi-Ardekani at col. 4:18-21. Thus, a person having ordinary skill in the art would have understood that the transceiver of Fadavi-Ardekani could implement G.993.1, including its initialization protocol.

396. As explained above, Fadavi-Ardekani discloses a single transceiver supporting multiple sessions (lines). In allocating memory for each of the lines, Fadavi-Ardekani discloses determining the amount of memory necessary to support different sessions required by the transceiver. *See* Fadavi-Ardekani, col. 7:3-33. The transceiver of Fadavi-Ardekani is a central office transceiver that, if implementing G.993.1, would implement the functions of one or more VTU-Os. Thus, the interleaver of claim 1 of the '048 patent is the VTU-O's interleaver. As of the Family 3 patents' priority date, a person having ordinary skill in the art would have understood, based on the disclosures of Fadavi-Ardekani, that the allocated memory for the interleaver for each of the supported lines, which would have been determined based on the content of the O-MSG2 message transmitted by the VTU-O corresponding to that line, would not exceed the requirements the VTU-O set for itself in O-MSG2.

397. Therefore, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

g. **1[g]. “allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate”**

398. In my opinion, Fadavi-Ardekani in view of G.993.1 discloses limitation 1[g]. See, e.g., Fadavi-Ardekani, col. 6:10-15; col. 5:57-6:6; col. 6:55-7:33; 8:58-9:3; G.993.1, § 8.4.1, 8.1.

399. As described above, Fadavi-Ardekani discloses the use of Reed-Solomon encoding and decoding, and interleaving and deinterleaving. See Fadavi-Ardekani, col. 6:10-15. G.993.1 also discloses the transmitter interleaving the bytes of Reed-Solomon codewords, which means that the receiver will need to deinterleave the bytes of the Reed-Solomon codewords to recover the transmitted data. See G.993.1, § 8.4.1 (“Interleaving shall be used to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords. The interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255.”). The depth of the interleaver is adjustable, to meet latency requirements. *Id.* With respect to the memory needed for an interleaver and a deinterleaver, G.993.1 notes that “[t]he same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and de-interleaving at the receiver.” *Id.*

400. As explained above, the transceiver of Fadavi-Ardekani would be the VTU-O(s) of G.993.1 if it implemented VDSL. Fadavi-Ardekani discloses allocating a second number of bytes of a shared memory to a deinterleaver, which would then deinterleave data received from the VTU-R(s) connected to the transceiver of Fadavi-Ardekani. Fadavi-Ardekani describes using the IDIM memory in a ping-pang fashion, where “[a]s one area of the memory is being used by a first agent, another area of the memory can be used by a different agent.” *Id.* at col. 5:60-63; see also *id.* at col. 6:57-65 (“The IDIM holds DMT frames of data and may be utilized

in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames the FCI core and the DSP core. In addition to interleave data storage, the IDIM may contain a dedicated area for the transfer of fast path data to the DSP Core. The IDIM may be organized as 16 bit words with byte write capability to allow beneficial performance of various interleave/de-interleave processes.”). Thus, a portion of the memory is allocated to a deinterleaver to deinterleave a first plurality of Reed Solomon coded data bytes, by determining the size of the memory needed to deinterleave a certain amount of data. *See, e.g., id.* at col. 7:3-33. And as Fadavi-Ardekani notes, “between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory,” and, similarly, “[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.” *Id.* at col. 8:60-9:3. As a person having ordinary skill in the art would have understood as of the Family 3 patents’ priority date, these disclosures indicate that a first number of bytes of the shared memory have been allocated to the deinterleaver to deinterleave a second plurality of Reed Solomon (RS) coded data bytes received at a second data rate.

h. 1[h]. “interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver”

401. It is my opinion that Fadavi-Ardekani and G.993.1 together disclose limitation 1[h]. *See, e.g.,* Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; col. 7:25-30; col. 8:58-9:3; G.993.1 at §§ 8.1, 8.4.1, Fig. 8-1.

402. G.993.1 discloses the VTU-O interleaving the first plurality of RS coded data bytes, and deinterleaving the second plurality of RS coded data bytes. See § 8.4.1 (“The same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and de-interleaving at the receiver.”); § 8.4.2.

403. As explained above, the transceiver of Fadavi-Ardekani would be the VTU-O(s) of G.993.1 if it implemented VDSL. Fadavi-Ardekani discloses interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver (i.e., prior to transmission to the VTU-R) and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver (i.e., after reception from the VTU-R). Fadavi-Ardekani discloses that “[a]n optimal implementation of the interleaver according to the method of the invention uses the same memory for receive data and transmit data . . .” Fadavi-Ardekani, col. 7:25-30. Fadavi-Ardekani further describes that the IDIM memory is used in a ping-pang fashion, in which “the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory.” *Id.* at col. 8:58-9:3. And as Fadavi-Ardekani notes, “between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory,” and, similarly, “[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.” *Id.* at col. 8:60-9:3. As a person having ordinary skill in the art would have understood as of the Family 3 patents’ priority date, these disclosures indicate that the

transceiver of Fadavi-Ardekani, acting as one or more VTU-Os, is interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

i. **1[i]. “wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver”**

404. It is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses limitation 1[i]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6, col. 6:55-65; col. 6:66-7:33; G.993.1, §§ 9.2.3.4.

405. I understand that the Court has construed this limitation to mean “the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory.” As described above, Fadavi-Ardekani discloses that the shared IDIM memory operates in a “ping-pang” fashion, where “areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of a memory is being used by a first agent, another area of memory can be used by a different agent.” Fadavi-Ardekani, col. 6:55-65. It further explains how “[a]s long as different agents access . . . different areas of a dual access memory, there are no memory address conflicts that could cause communication errors.” *Id.* at col. 5:65-67. Fadavi-Ardekani explains that “[a]n optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & deinterleave +4K fast path).” *Id.* at col. 7:25-30. Fadavi-Ardekani discloses that the shared

memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. Specifically, Fadavi-Ardekani discloses that “between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory,” and, similarly, “[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.” *Id.* at col. 8:60-9:3. As a person having ordinary skill in the art would have understood as of the Family 3 patents’ priority date, these disclosures indicate that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

406. Additionally, G.993.1 discloses that the interleaver memory and the deinterleaver memory are used at the same time, which G.993.1 refers to as Frequency Division Duplexing (FDD). G.993.1, § 6.1. In this mode, a “full-duplex” link is established between the VTU-O and VTU-R, over which data can be transmitted simultaneously in both directions. *Id.* at §§ 12.4.1, 9.2.3.4. One of ordinary skill in the art would have understood that the VTU-O would need to interleave and deinterleave data at the same time in this mode of transmission.

407. Therefore, it is my opinion that claim 1 of the ’048 patent is obvious over the combination of Fadavi-Ardekani and G.993.1.

4. Claim 5 of the ’381 Patent

408. It is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses each limitation of claim 5 of the ’381 patent.

a. **5[a]. “A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver”**

409. To the extent it is limiting, it is my opinion that Fadavi-Ardekani discloses the preamble. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67; col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; col. 7:34-43.

410. Fadavi-Ardekani describes how “the firmware required for performing processing tasks associated with the central office is resident on the single integrated circuit transceiver of the invention.” *Id.* at col. 7:34-37. Though Fadavi-Ardekani notes that functions implemented in hardware are generally faster, “similar functionality can be provided in a software implementation.” *Id.* at col. 7:37-43. I discuss how Fadavi-Ardekani discloses allocating shared memory in a transceiver above with respect to claim 1 of the ’048 patent, which I incorporate here by reference. *See* Section IX.C.3.a. I describe how Fadavi-Ardekani discloses a transceiver above at Section IX.C.3.b, which I also incorporate by reference. Thus, Fadavi-Ardekani discloses this limitation.

b. **5[b]. “transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver”**

411. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[b]. *See, e.g.*, G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.2.1.2, 12.4.6.3.1.1.

412. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta’s infringement read. If the Court or

other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then G.993.1 and Fadavi-Ardekani disclose this limitation under such an interpretation of the claims.

413. Above at Section IX.D.2.c, I describe how Fadavi-Ardekani in combination with G.993.1 discloses transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to allocated to a deinterleaver according to TQ Delta's apparent interpretation of the claims, and I incorporate that discussion by reference. Furthermore, G.993.1 discloses that "[t]he same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and deinterleaving at the receiver. The convolutional interleaving introduces an absolute read-to-write delay" G.993.1, § 8.4.1. Moreover, G.993.1 describes the similarities between the interleaver processing and the deinterleaver processing, stating that "[t]he deinterleaver is similar to the interleaver, but the branch indices are reversed so that the largest interleaver delay corresponds to the smallest deinterleaver delay." *Id.* at § 8.4.2, Table 8-1 (describing relationship between interleaver block depth, interleaving depth, "(De)interleaver memory size," and end-to-end delay). One of ordinary skill in the art would have understood that the discussions of allocating memory to an interleaver in Fadavi-Ardekani and G.993.1 apply equally to allocating memory to a deinterleaver. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses this limitation.

c. **5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"**

414. Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[c], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; 6:55-7:33; col. 8:58-9:3.

415. Above at Section 381, I describe how Fadavi-Ardekani in combination with G.993.1 discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, and I incorporate my discussion and opinions by reference. G.993.1 discloses the complementary relationship between the memory required by an interleaver and a deinterleaver, as I described above with respect to the previous limitation. See G.993.1, §§ 8.4.1, 8.4.2, Table 8-1. A person having ordinary skill in the art would have understood the disclosures of G.993.1 and Fadavi-Ardekani as disclosing that the transceiver determines an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

d. **5[d]. “allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate”**

416. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[d]. See, e.g., Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; col. 6:55-7:33; col. 8:58-9:3; G.993.1, §§ 8.1, 8.4.1, FIG. 8-1.

417. Above at Section IX.C.3.e, I explain how Fadavi-Ardekani in combination with G.993.1 discloses allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. In addition, at Section IX.C.3.g above, I explain how Fadavi-Ardekani in combination with G.993.1 discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate. I incorporate both of those discussions by reference, and on

that basis, it is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses this limitation.

e. **5[e]. “wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message”**

418. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[e]. *See, e.g.*, G.993.1, §§ 8.4, 8.4.2, 12.4.1, 12.4.6.2.1.1. I have reviewed TQ Delta’s infringement contentions, and understand that TQ Delta contends that the “maximum number of bytes specified in the message” is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. *See* G.993.2 (12/2011) at § 6.2.8. I do not agree with TQ Delta’s contentions or interpretation of the claims. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta’s contentions, however, the combination of Fadavi-Ardekani and G.993.1 discloses this limitation, in my opinion.

419. Above at Section IX.C.3.f, I explain how Fadavi-Ardekani in combination with G.993.1 discloses “wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message,” and I incorporate that discussion by reference. In the same way that the CO transceiver of Fadavi-Ardekani and G.993.1 would not allocate more memory for the interleaver than is specified in the messages that it exchanges during initialization, it would also not allocate more memory for the deinterleaver than is specified in the messages that it exchanges during initialization, in my opinion.

- f. 5[f]. “allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate”

420. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[f]. See, e.g., Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; G.993.1, §§ 8.1, 8.4.1, Fig. 8-1.

421. Above at Section IX.C.3.g, I explain how Fadavi-Ardekani allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes transmitted at a second data rate. Also, at Section IX.C.3.e above, I explain how Fadavi-Ardekani in combination with G.993.1 discloses allocating a first number of bytes of the shared memory to an interleaver to interleave a first plurality of RS coded data bytes transmitted at a first data rate. I incorporate both of those sections herein by reference. It is my opinion that, given this disclosure, Fadavi-Ardekani and G.993.1 disclose this limitation.

- g. 5[g]. “deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver”

422. Fadavi-Ardekani in combination with G.993.1, in my opinion, discloses limitation 5[g]. See, e.g., Fadavi-Ardekani, col. 5:57-6:6; col. 7:25-30; col. 8:58-9:3; G.993.1, §§ 8.1, 8.4.1, Fig. 8-1. Above at Section IX.C.3.h, I explain how Fadavi-Ardekani in combination with G.993.1 discloses interleaving a first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference. Though this limitation recites a first plurality being deinterleaved, and a second plurality of data bytes being interleaved, in my opinion, there is no difference in how a

transceiver would implement this limitation. It is my opinion that Fadavi-Ardekani and G.993.1 disclose this limitation.

h. 5[h]. “wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver”

423. Fadavi-Ardekani in combination with G.993.1 discloses that the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; G.993.1, §§ 6.1, 9.2.3.4, 12.4.1. I explain above at Section IX.C.3.i how it is my opinion that Fadavi-Ardekani in view of G.993.1 discloses wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference herein. In my opinion, one of ordinary skill in the art would have understood that there is no difference between these two limitations, i.e., they both require that the deinterleaver and interleaver memory be used at the same time. Accordingly, it is my opinion that this limitation is met by Fadavi-Ardekani in combination with G.993.1.

5. Claim 13 of the '882 patent

424. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses each limitation of claim 13 of the '882 patent, as I explain below.

a. 13[a]. “A system that allocates shared memory”

425. To the extent that the preamble is limiting, Fadavi-Ardekani discloses a system that allocates shared memory. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3. This limitation is identical to the preamble of Claim 1 of the '048 patent, and for the same reasons, it is my opinion that this limitation is disclosed by Fadavi-Ardekani. *See* Section IX.C.3.a.

b. 13[b]. “a transceiver that performs”

426. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses a transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67. This limitation is identical to the second limitation of Claim 1 of the '048 patent, except that it recites “a transceiver capable of” additional steps. In my opinion, this limitation is met for the same reasons that I explain above at Section IX.C.3.b, and I incorporate my discussion and opinions herein by reference.

c. 13[c] through 13[i]

427. These limitations are identical to the corresponding limitations of claim 5 of the '381 patent. *See* Appx. 3 (comparing limitations of claim 5 of the '381 patent with limitations of claim 13 of the '882 patent). For the same reasons, it is my opinion that these limitations are met by Fadavi-Ardekani in combination with G.993.1, and I incorporate by reference Sections IX.C.3.c through IX.C.3.i (claim 1) and Sections IX.B.4.b through IX.B.4.h (claim 5).

6. Claim 19 of the '473 Patent

428. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses each limitation of claim 19 of the '473 patent.

a. 19[a]. “An apparatus comprising”

429. To the extent that this preamble is limiting, Fadavi-Ardekani discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, Fadavi-Ardekani at Abstract; col. 1:12-14; col. 2:18-24; col. 2:62-67.

b. 19[b]. “a multicarrier communications transceiver”

430. It is my opinion that Fadavi-Ardekani discloses a multicarrier communications transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 1:12-14; col. 2:18-24; col. 2:62-67; G.993.1, §§ 5.2, 5.3, Fig. 5-2. I understand that the Court has construed the term “transceiver”

to mean “communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.”

431. The central office ADSL transceiver of Fadavi-Ardekani is a communications device capable of transmitting and receiving data. Fadavi-Ardekani discloses “[a] transceiver for an asymmetric communication system . . . that implements a buffering and scheduling scheme that utilizes a virtual clock signal to synchronize processing of asynchronous frame data for multiple ADSL sessions.” *Id.* at Abstract; *see also id.* at col. 2:62-67. The central office ADSL transceiver is described as being “bi-directionally coupled” to a splitter and a digital network. *Id.* at col. 4:30-34. It includes, as shown in FIG. 2 of Fadavi-Ardekani, an ATM accelerator, which, among other things, “transfers [] DMT done data on the twisted-pair media.” *Id.* at col. 5:52-54. FIG. 3 of Fadavi-Ardekani, shown above, “illustrates an exemplary processing sequencing for a case when four Transmit and Receive lines are enabled.” *Id.* at col. 4:1-2. One of ordinary skill in the art would have understood these disclosures to indicate that the transceiver is capable of transmitting and receiving data.

432. Fadavi-Ardekani further discloses using a “conventional ADSL transceiver.” *Id.* at col. 4:35-38. One of ordinary skill in the art would have understood that ADSL is a multicarrier communications system. Moreover, Fadavi-Ardekani discloses that ADSL uses “Discrete MultiTone (DMT), [which] is a multi-carrier technique that divides the available bandwidth of twisted-pair media connections into mini-subchannels or bins. In the ADSL standard, DMT may be used to generate up to 250 separate 4.3125 KHz subchannels from 26 KHz to 1.1 MHz for downstream transmission and up to 26 subchannels from 26 KHz to 138 KHz for upstream transmission.” *Id.* at col. 2:3-9.

433. Fadavi-Ardekani further teaches that the transmitter and receiver portions share common circuitry, including the Asynchronous Transfer Mode (ATM) accelerator, frame buffer, framer/coder/interleaver, DSP core and interleave/deinterleave memory (IDIM). *Id.* at col. 5:23-40.

434. G.993.1 similarly discloses a multicarrier communications transceiver, a VTU-O or VTU-R that is compliant with the G.993.1 standard and uses DMT. *See* G.993.1, §§ 5.2, 5.3, 8.5.1, Fig. 5-2. Accordingly, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

c. **19[c]. “that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path”**

435. Fadavi-Ardekani discloses limitation 1[c], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 6:66-7:33.

436. Fadavi-Ardekani discloses ADSL transceivers that include framer/coder/interleaver (FCI) blocks that perform interleaving and deinterleaving functions, and are associated with an Interleave/De-Interleave Memory (IDIM). *Id.* at col. 6:10-15. The IDIM is associated with multiple “sessions,” where, for example, “a simple implementation of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2Kbytes for upstream processing.” *Id.* at col. 13-17. I understand that the Court has construed the term “latency path” to mean “transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay.” One of ordinary skill in the art would have understood the sessions of Fadavi-Ardekani to take place over multiple latency paths, and that a session requiring “downstream processing” requires interleaving, and a session requiring upstream processing requires deinterleaving. These latency paths would have distinct latencies.

437. Similarly G.993.1 discloses at least one upstream path and one downstream path between a VDSL VTU-O and VTU-R, with each of these paths being associated with a latency. See G.993.1, § 5.1 (“The reference configuration provides two or four data paths with bit rate under the control of the network operator, consisting of one or two downstream and one or two upstream data paths. A single path in each direction can be of high latency (with lower BER expected) or lower latency (with higher BER expected). Dual paths in each direction provide one path of each type. The dual latency configuration is thought to be the minimum that is capable of supporting a sufficient full service set, although there are organizations supporting both the single latency model with programmable latency, and others requesting more than two paths/latencies.”), § 5.2. One of ordinary skill in the art would have understood that these upstream and downstream paths are associated with interleaving and deinterleaving functions. See, e.g., § 8.4.1 (“Interleaving shall be used to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords. . . . It shall be possible to adjust the interleave depth via the management system to meet latency requirements. The latency of the slow path is a function of the data rate and burst error correction capability. For data rates greater than or equal to 13 Mbit/s, the latency between the α and β interfaces shall not exceed 10 ms when the interleaver depth is set to the maximum. At lower data rates there is a trade-off between higher latency and decreased burst error correction ability. At any data rate, the minimum latency occurs when the interleaver is turned off.”).

438. Therefore, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

d. **19[d]. “the multicarrier communications transceiver being associated with a memory”**

439. In my opinion, the combination of Fadavi-Ardekani and G.993.1 discloses limitation 19[d]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; G.993.1 at § 8.4.1, Table 8-1, Table 8-2.

440. Fadavi-Ardekani describes an Interleave/De-interleave Memory (IDIM), which is associated with the transceiver. Fadavi-Ardekani, col. 6:55-65 (“The Interleave/De-Interleave Memory (IDIM) 230 provides a memory through which the FCI 226 interfaces the DSP core 228. The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion.”); col. 7:25-30 (“An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 kBytes to support a standard ADSL session at full interleave depth (16K interleave & deinterleave +4K fast path).”); *see also* Fadavi-Ardekani, col. 8:58-9:3.

441. Fadavi-Ardekani further describes that the “ADSL transceiver of the invention 120 is a single integrated circuit which has various component[s] including: an Asynchronous Transfer Mode (ATM) accelerator 222, a Frame Buffer (FB) 224, a Framer/Coder/Interleaver (FCI) 226, a Digital Signal Processing (DSP) core 228, and a Interleave/De-Interleave Memory (IDIM) 230.” *Id.* at col. 5:23-28. Because the IDIM is described and disclosed as being part of the ADSL transceiver, one of ordinary skill in the art would have understood it to be “associated with” the transceiver.

442. G.993.1 also discloses that the multicarrier communications transceiver is associated with a memory. *See, e.g.*, G.993.1 at § 8.4.1 (“The convolutional interleaver uses a memory in which a block of I octets is written while an (interleaved) block of I octets is read. . . . The same size interleaving memory (see Table 8-1) is needed for interleaving at the

transmitter and de-interleaving at the receiver.”); *see also* Table 8-1 (indicating interleaver and deinterleaver memory size is $(M - 1) \times (I - 1) / 2$ bytes); Table 8-2 (providing interleaver and deinterleaver memory sizes for a particular Reed-Solomon code).

443. Therefore, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

e. **19[e]. “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”**

444. Fadavi-Ardekani, in combination with G.993.1, discloses limitation 19[e], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.3.1.1.

445. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta’s infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then G.993.1 in combination with Fadavi-Ardekani discloses this limitation under TQ Delta’s interpretation of the claims.

446. Fadavi-Ardekani discloses allocating memory between an interleaving function and a deinterleaving function. Fadavi-Ardekani describes using the IDIM memory in a ping-pang fashion, where “[a]s one area of the memory is being used by a first agent, another area of the memory can be used by a different agent.” *Id.* at col. 5:60-63; col. 6:57-60 (“The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames the FCI core and the DSP core.”).

A portion of the memory is allocated to an interleaver by determining the size of the memory needed to interleave a certain amount of data. *Id.* at col. 7:3-33. And as Fadavi-Ardekani notes, “between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory,” and, similarly, “[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.” *Id.* at col. 8:60-9:3. It is my understanding that the Court construed the term “memory is allocated between the interleaving function and the deinterleaving function” to mean “an amount of memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function.” As a person having ordinary skill in the art would have understood as of the Family 3 patents’ priority date, these disclosures indicate that the memory is allocated between an interleaving function and a deinterleaving function.

447. As explained above, VDSL transceivers described in G.993.1 are capable of sending messages during initialization, specifying communications parameters, including interleaver and deinterleaver settings and capabilities. G.993.1 discloses transceivers that exchange initialization messages. See G.993.1, § 12.4.1 (“Initialization of a VTU-O/VTU-R includes a variety of tasks. The set of tasks consists of: . . . exchange of parameters (RS settings, interleaver parameters, VOC settings, bit loading and energy tables . . .”). Initialization messages include R-MSG2, sent by the VTU-R, that “transmits information about [the connection’s] bit allocation capabilities and several other features,” including the “Maximal

interleaver memory,” expressed in bytes. *Id.* at § 12.4.6.3.1.1; § 12.4.6.2.1.1 (Table 12-23).

Thus, G.993.1 describes a message during initialization (i.e., R-MSG2) that describes how interleaver memory can be allocated to an interleaver or a deinterleaver. It also describes how a VTU-O receives a message during initialization (i.e., R-MSG2) specifying parameters based on which the memory can be allocated (i.e., the VTU-R’s interleaver).

448. Similarly, G.993.1 specifies that the VTU-O transmits the message O-MSG2. *Id.* at § 12.4.6 (Figure 12-7). O-MSG2 contains the field “Maximum interleaver delay,” expressed in milliseconds. *Id.* at § 12.4.6.2.1.1 (Table 12-23). As a person having ordinary skill in the art would have understood as of the Family 3 patents’ priority date, because the interleaver delay is a function of the bit rate and interleaver depth, O-MSG2 specifies parameters that the VTU-O can use to allocate memory between an interleaver and a deinterleaver. It also discloses a transceiver, namely the VTU-R, receiving a message during initialization (i.e., O-MSG2) that the transceiver can use to allocate memory between an interleaver and a deinterleaver (i.e., the VTU-O’s interleaver).

f. **19[f]. “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

449. Fadavi-Ardekani, in combination with G.993.1, discloses limitation 19[f], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 8:58-9:3; G.993.1, §§ 8.4.1, 8.4.2.

450. As described above, Fadavi-Ardekani discloses that the shared IDIM memory operates in a “ping-pang” fashion used by multiple functions, where “[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent.”

Fadavi-Ardekani, col. 6:60-65. In operation, the shared memory disclosed in Fadavi-Ardekani

in which “the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory.” *Id.* at col. 8:58-9:3. The allocation of memory is based on the number of sessions supported by the transceiver and the interleave depth for each session. *See, e.g., id.* at col. 7:3-33.

451. As I explain above (see Section VII.F.4), G.993.1 discloses that the VTU-O and VTU-R exchange interleaver capabilities and requirements during initialization. Fadavi-Ardekani states that its transceiver may incorporate VDSL. Fadavi-Ardekani at col. 4:18-21. Thus, as a skilled artisan would have recognized as of the priority date of the Family 3 patents, the transceiver of Fadavi-Ardekani implementing VDSL as per G.993.1 would transmit and receive initialization messages regarding interleaving capabilities and requirements. Thus, at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

452. Additionally, G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time. G.993.1 uses Frequency Division Duplexing (FDD). G.993.1, § 6.1. In this mode, a “full-duplex” link is established between the VTU-O and VTU-R, over which data can be transmitted simultaneously in both directions. *Id.* at §§ 12.4.1, 9.2.3.4. One of ordinary skill in the art would have understood that data would need to be interleaved and deinterleaved at the same time in this mode of transmission, which would require that a portion of the memory be allocated to an interleaving function, and a portion of the memory would be allocated to a deinterleaving function.

453. Accordingly, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

7. **Motivation to Combine Fadavi-Ardekani and G.993.1**

454. In my opinion, one of ordinary skill in the art as of the Family 3 patents' priority date would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.993.1 in the manner claimed.

455. First, both references are in the telecommunications field and relate to DSL systems specifically. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:63-3:4; col. 4:9-21; col. 4:25:63 (describing an ADSL communication system); col. 4:65-5:40 (describing head-end ADSL transceiver); G.993.1, §§ 1 ("G.993.1 VDSL (Very high speed Digital Subscriber Line) permits the transmission of asymmetric and symmetric aggregate data rates up to tend of Mbit/s on twisted pairs."). In addition, Fadavi-Ardekani states that the disclosed transceiver may implement VDSL, which, as of the Family 3 patents' priority date, would have been understood by one of ordinary skill in the art to include G.993.1. *See, e.g.*, Fadavi-Ardekani, col. 4:18-21. For this reason alone, a skilled artisan would have been motivated to combine the teachings of G.993.1 with those of Fadavi-Ardekani.

456. Second, both references describe the need to allocate memory for interleaving and deinterleaving functions. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3, G.993.1 at § 8.4.1 (describing implementation of interleaver memory, and noting that "[t]he same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and de-interleaving at the receiver."). Thus, both Fadavi-Ardekani and G.993.1 relate to the problem to be solved identified by the Family 3 patents – allocating shared memory between interleaving and deinterleaving functions. *See, e.g.*, '048 patent, col. 1:48-59 ("One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to

provide error correcting capability.”). One of ordinary skill in the art naturally would have consulted Fadavi-Ardekani for its description of calculating memory needs and allocating memory between interleaver and deinterleaver functions when considering G.993.1 and its description of using interleavers and exchanging parameters relating to interleaving during initialization.

457. Third, as a skilled artisan would have understood on the Family 3 patents’ priority date, the memory requirements of VDSL transceivers, such as those described in G.993.1, contributed to the transceiver’s cost, power consumption, and size. The need to reduce size and power was known to be particularly acute for VDSL transceivers because the VTU-O was to be deployed in optical network units or cabinets, in which space was at a premium and heat dissipation mechanisms were limited. Thus, a skilled artisan would have sought implementations that would reduce the cost, size, and power consumption of the VTU-O. Fadavi-Ardekani discloses reducing the size and complexity of memory in a DSL transceiver. *See, e.g.*, Fadavi-Ardekani, col. 3:1-4 (“Utilizing this buffering and scheduling methodology, reductions in the design sizes of various transceiver components and the data flow complexity of the transceiver may be achieved.”). Fadavi-Ardekani faults prior art systems for being “excessively duplicative in terms of transceivers and memory in each transceiver, and thus more costly than necessary to provide the desired functionality.” *Id.* at col. 2:57-59. It also discloses the desirability of reducing the amount of memory needed. *Id.* at col. 3:43-47; col. 8:4-12; 9:20-23. To reduce memory, Fadavi-Ardekani discloses sharing one memory between the interleaver and deinterleaver. *See, e.g., id.* at Abstract; col. 3:39-41; col. 7:25-30; col. 9:18-20. Thus, a skilled artisan would have been motivated to combine the size- and cost-saving

approach of Fadavi-Ardekani with the transceivers of G.993.1 to reduce the cost, size, and power consumption of the VTU-Os that would be deployed in optical network units or cabinets.

458. Fourth, one of ordinary skill in the art, when considering Fadavi-Ardekani, would have naturally looked to G.993.1 to determine how to allocate shared memory. Fadavi-Ardekani explains that the amount of memory required by, and the allocation of memory between, the interleaver and deinterleaver depends on the services to be supported. Fadavi-Ardekani, col. 6:66-7:33 (“In a preferred embodiment of the invention, the IDIM is allocated as 10 K×16 (i.e., 20 K) Random Access Memory (RAM), which supports approximately four G.lite or approximately four standard ADSL session/s at less than full interleave depth. The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention.”). One of ordinary skill would have recognized that, in order to allocate memory between interleaver and deinterleaver functions in a useful way, the transceiver would need information about the amount of memory needed for the services that were to be supported by the transceiver.

459. As I described above, G.993.1 discloses that the transceivers share information about the services they will support, the latency requirements of those services, and the amount of available memory. *See, e.g.*, G.993.1, § 5.1 (“The reference configuration provides two or four data paths with bit rate under the control of the network operator, consisting of one or two downstream and upstream data paths. A single path in each direction can be of high latency (with low BER expected) or lower latency (with higher BER expected). Dual paths in each direction provide one path of each type. The dual latency configuration is thought to be the minimum that is capable of supporting a sufficient full service set, although there are organizations supporting both the single latency model with programmable latency, and other

requesting more than two paths/latencies. The model assumes that Forward Error Correction (FEC) will be needed for part of the payload and that deep interleaving will be required to provide adequate protection against impulse noise.”); § 8.5.2; § 12.4.6.2, § 12.4.6.3; Table I.39. One of ordinary skill in the art would have recognized that G.993.1, and the ability of transceivers to share information about their capabilities and requirements during the initialization procedure, provides a reliable and efficient way of implementing the advantageous single memory for interleaving and deinterleaving disclosed by Fadavi-Ardekani for a wide variety of services and applications such as those enabled by G.993.1.

D. The Asserted Claims Are Obvious Over Fadavi-Ardekani in Combination with G.992.2

460. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent. One of ordinary skill in the art would have been motivated, as of the Family 3 patents' priority date, to combine the teachings of Fadavi-Ardekani with the teachings of G.992.2, as I describe below in Section IX.D.6. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then Fadavi-Ardekani in combination with G.992.2 renders obvious the asserted claims of the Family 3 patents.

1. Brief Description of G.992.2

461. I provide a description of G.992.2 above at Section VII.F.3, which I incorporate herein by reference.

462. I understand that G.992.2 was approved and published no later than June 1999. I understand that it is prior art to the Asserted Family 3 Patents. I have reviewed TQ Delta's

infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then G.992.2 renders obvious the asserted claims of the Family 3 patents when combined with other references as I explain below.

2. Claim 1 of the '048 Patent

463. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 1 of the '048 patent, as I describe below.

a. 1[a]. "A system that allocates shared memory"

464. To the extent that this preamble is limiting, Fadavi-Ardekani discloses a system that allocates shared memory, in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55:65; col. 7:25-30; col. 8:58-9:3. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.a.

b. [1b]. "a transceiver that is capable of"

465. In my opinion, Fadavi-Ardekani discloses a transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67; G.992.2, §§ 4.1, 4.2, 5, Fig. 2. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.b.

466. G.992.2 similarly discloses a transceiver, an ADSL transceiver unit (ATU) that complies with the G.992.2 standard. *See* G.992.2, §§ 4.1, 4.2, Fig. 2. G.992.2 explains that "[t]he ATU shall transport a single duplex bearer channel," which would indicate to one of ordinary skill in the art that the ATU is capable of transmitting and receiving data. One of ordinary skill in the art would further have understood that the transmitter and receiver portions share some common circuitry, such as, for example, an interface to the twisted pair.

c. **1[c] “transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver”**

467. Fadavi-Ardekani in view of G.992.2 discloses limitation 1[c], in my opinion.

See, e.g., G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3.

468. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, nor do I agree with TQ Delta’s infringement read. If, however, the Court or other trier of fact interprets the claim such that the O-PMS message and sending max_delay_octet meets this limitation, then Fadavi-Ardekani and G.992.2 meet this limitation as well, in my opinion.

469. Transceivers such as those described in G.992.2 are capable of sending and receiving initialization messages that specify communication parameters for DSL systems. For example, G.992.2 teaches transceivers that exchange initialization messages that contain information about the channel as well as the transceiver and its processing requirements and capabilities. G.992.2, § 11.1.1 (“In subsequent parts of the initialization, in order to maximize the throughput and reliability of this link, ADSL transceivers shall determine certain relevant attributes of the connecting channel and establish transmission and processing characteristics suitable to that channel. During initialization each receiver can determine the relevant attributes of the channel through the transceiver training and channel analysis procedures.”). These messages include communicating to a far-end transceiver “the number of bits and relative power levels to be used on each DMT subcarrier, as well as any messages and final data rates information.” *Id.*

470. G.992.2 describes exchanging messages between the transceivers in an iterative process to establish transmission parameters such as data rates and formats for the ATU-R. The C-RATES1 message defined in G.992.2 is a signal sent from the ATU-C, whose purpose “is to transmit four options for data rates and formats to the ATU-R.” *Id.* at § 11.9.2. Each of the four options contains three fields, one of which is the RRSI field that “contains Reed-Solomon FEC and interleaver parameters.” The RRSI field contains ten entries, including the number of data frames (DFs) per Reed-Solomon codeword in the downstream direction, downstream interleave depth in codewords, the number of DFs per Reed-Solomon codeword in the upstream direction, and the upstream interleaver depth in codewords. *See id.*; *see also* Table 26, Table 27. One of ordinary skill in the art would have understood that these messages would meet this claim limitation, at least according to TQ Delta’s infringement read.

471. An additional initialization message is the C-RATES-RA message, which sends “four new options for transport configuration for both upstream and downstream. These options will, in general, be closer to the optimum bit rate for the channel than those in C-RATES1. . . .” G.992.2, § 11.11.3. Like the C-RATES1 message, the C-RATES-RA message contains ten entries, including the numbers of DFs per Reed-Solomon codeword in the downstream direction, downstream interleave depth in codewords, the number of DFs per Reed-Solomon codeword in the upstream direction, and the upstream interleave depth in codewords. *See id.*; *see also* Table 33, Table 34. As with the parameters in the C-RATES1 message, one of ordinary skill in the art would have understood that the information in the C-RATES-RA message would meet this limitation under TQ Delta’s interpretation of the claim.

472. In addition, the ATU-R transmits R-RATES2, which selects the number of the option in C-RATES-RA with the highest data rate that can be supported in the downstream

direction based on the ATU-R's measurements of the channel. G.992.2 at § 11.12.10. The ATU-C then transmits C-RATES2, which indicates the final decision on the downstream and upstream options that will be used for the connection. G.992.2 at § 11.11.11. The ATU-C's decision combines the downstream option selected by the ATU-R with the option number with the highest upstream data rate that can be supported based on the ATU-C's measurements of the channel. G.992.2 at § 11.11.11. A person having ordinary skill in the art would have understood that the information in the R-RATES2 and C-RATES2 messages meets this limitation, at least under TQ Delta's infringement read.

d. 1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory"

473. Fadavi-Ardekani in combination with G.992.2. discloses limitation 1[d], in my opinion. *See, e.g.* Fadavi-Ardekani, col. 6:55-65; col. 6:66-7:33; 8:58-9:3; 6:10:15; G.992.2, § 7.6. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section 381.

e. 1[e]. "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate"

474. It is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses limitation 1[e]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; col. 6:10-15; G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3.

475. As described above, Fadavi-Ardekani discloses the use of Reed-Solomon encoding. *See* Fadavi-Ardekani, col. 6:10-15. G.992.2 also discloses interleaving the bytes of Reed-Solomon codewords. *See* G.992.2, § 7.6 ("The Reed-Solomon codewords shall be convolutionally interleaved. The interleaving depth shall always be a power of 2."). The depth of the interleaver is adjustable, to meet different data rates and demands. *Id.*

476. As I explained above, Fadavi-Ardekani discloses allocating a first number of bytes of a shared memory to an interleaver. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.e. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation.

f. **1[f]. “wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message”**

477. In my opinion, Fadavi-Ardekani in view of G.992.2 discloses limitation 1[f]. *See, e.g.*, G.992.2, §§, 7.6, 11.1.1, 11.9.2, 11.11.3.

478. I have reviewed TQ Delta’s infringement contentions, and I understand that TQ Delta contends that the “maximum number of bytes specified in the message” is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta’s contentions or interpretation of the claims. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta’s contentions, however, G.992.2 in combination with Fadavi-Ardekani still discloses this limitation in my opinion.

479. First, one of ordinary skill in the art would have understood, given the disclosure of Fadavi-Ardekani, that the allocated memory for the interleaver would not exceed the requirements set forth by the transmitter. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.f.

480. Second, G.992.2 discloses the C-RATES1, R-RATES1, C-RATES-RA, R-RATES2, and C-RATES2 messages, which contain the RRSI field that contains values for the number of DFs in a Reed-Solomon codeword, and the interleaver depth in codewords in the upstream and downstream directions. *See, e.g.*, G.992.2, §§ 11.9.2, 11.11.3. G.992.2 also discloses that the interleaver depth is adjustable. *Id.* at § 7.6. The parameters in the C-

RATES1, R-RATES1, and C-RATES-RA messages can be used to allocate memory to implement each of the four options. The R-RATES2 and C-RATES2 messages can be used to allocate memory to implement the ATU-C's interleaver and to implement the ATU-R's interleaver. Based on this disclosure, one of ordinary skill in the art would have understood that the memory allocated for the interleaver does not exceed the number of bytes in the message.

g. **1[g]. “allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate”**

481. In my opinion, Fadavi-Ardekani in view of G.992.2 discloses limitation 1[g]. See, e.g., Fadavi-Ardekani, col. 6:10-15; col. 5:57-6:6; col. 6:55-7:33; 8:58-9:3; G.992.2, §§7.6, 11.1.1, 11.9.3.

482. As described above, Fadavi-Ardekani discloses the use of Reed-Solomon encoding. See, e.g., Fadavi-Ardekani, col. 6:10-15. G.992.2 also discloses interleaving the bytes of Reed-Solomon codewords. See G.992.2, § 7.6 (“The Reed-Solomon codewords shall be convolutionally interleaved. The interleaving depth shall always be a power of 2” and describing a rule for interleaver depth). The depth of the interleaver is adjustable, to meet different service requirements. See *id.* As a skilled artisan would have understood, the specification in G.992.2 that Reed-Solomon codewords shall be convolutionally interleaved by a transmitter means that the transceiver on the other side of the subscriber line would include a corresponding deinterleaver.

483. Fadavi-Ardekani discloses allocating a second number of bytes of a shared memory to a deinterleaver. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.g. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation.

h. 1[h]. “interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver”

484. It is my opinion that Fadavi-Ardekani and G.992.2 together disclose limitation 1[h]. See, e.g., Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; col. 7:25-30; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1, 11.9.3.

485. One of ordinary skill in the art would have understood that G.992.2 discloses interleaving a first plurality of RS coded data bytes, and deinterleaving a second plurality of RS coded data bytes. See § 7.6 (“The Reed-Solomon codewords shall be convolutionally interleaved. The interleaving depth shall always be a power of 2.”). Given G.992.2’s disclosure of a convolutional interleaver, and that each ATU supports both downstream and upstream transmission simultaneously (see, e.g., G.992.2 at §§ 4.2, 7.3, 7.10), one of ordinary skill in the art would have understood that an ATU would interleave data bytes to be transmitted and deinterleave received data bytes.

486. Fadavi-Ardekani discloses interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.h. It is my opinion that Fadavi-Ardekani and G.992.2 disclose this limitation.

i. 1[i]. “wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver”

487. It is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses limitation 1[i]. See, e.g., Fadavi-Ardekani, col. 5:57-6:6, col. 6:55-65; col. 6:66-7:33; G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3.

488. As described above, Fadavi-Ardekani discloses that the shared IDIM memory operates in a “ping-pang” fashion in which the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.i.

489. Additionally, one of ordinary skill would have understood that G.992.2 discloses that the interleaver memory and the deinterleaver memory are used at the same time. G.992.2 establishes a “single duplex bearer channel.” G.992.2, § 5. One of ordinary skill in the art would have understood that data is transmitted in both directions at the same time. As a result, the interleaver and deinterleaver would both have to be used at the same time, which in turn, would mean that the interleaver memory and deinterleaver memory were used at the same time. Accordingly, it is my opinion that G.992.2 also discloses this limitation.

3. Claim 5 of the '381 Patent

490. It is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 5 of the '381 patent.

a. 5[a]. “A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver”

491. To the extent that it is limiting, it is my opinion that Fadavi-Ardekani discloses the preamble. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67; col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; col. 7:34-43.

492. Fadavi-Ardekani describes how “the firmware required for performing processing tasks associated with the central office is resident on the single integrated circuit transceiver of the invention.” *Id.* at col. 7:34-37. Though Fadavi-Ardekani notes that functions

implemented in hardware are generally faster, “similar functionality can be provided in a software implementation.” *Id.* at col. 7:37-43. I discuss how Fadavi-Ardekani discloses allocating shared memory in a transceiver above with respect to claim 1 of the ’048 patent, which I incorporate here by reference. See Section IX.C.3.a. I describe how Fadavi-Ardekani discloses a transceiver above at Section IX.C.3.b, which I also incorporate by reference. Thus, Fadavi-Ardekani discloses this limitation.

b. **5[b]. “transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver”**

493. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[b]. See, e.g., G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3.

494. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta’s infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then G.992.2 and Fadavi-Ardekani disclose this limitation under such an interpretation of the claims.

495. Above at Section IX.D.2.c, I describe how Fadavi-Ardekani in combination with G.992.2 discloses transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to allocated to a deinterleaver, and I incorporate that discussion by reference. Furthermore, G.992.2 describes the relationship between the interleave depth of a convolutional interleaver and the memory required to interleave or deinterleave a certain amount of data. See G.992.2, § 7.6.

Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation under TQ Delta's interpretation of the claims.

c. **5[c]. “determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory”**

496. Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[c], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; 6:55-7:33; col. 8:58-9:3.

497. Above at Section IX.D.2.d, I describe how Fadavi-Ardekani in combination with G.992.2 discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, and I incorporate my analysis and opinions by reference. G.992.2 describes the relationship between the memory required by an interleaver and a corresponding deinterleaver, as I describe above with respect to the previous limitation. *See* G.992.2, § 7.6. This disclosure, combined with the disclosure of Fadavi-Ardekani, discloses to one of ordinary skill in the art how to determine, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

d. **5[d]. “allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate”**

498. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[d]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; col. 6:55-7:33; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1.

499. Above at Section IX.D.2.e, I explain how Fadavi-Ardekani in combination with G.992.2 discloses allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data

rate. In addition, at Section IX.D.2.g above, I explain how Fadavi-Ardekani in combination with G.992.2 discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate. I incorporate both of those discussions by reference, and on that basis, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation.

e. **5[e]. “wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message”**

500. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[e]. *See, e.g.*, G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3. Above at Section IX.D.2.f, I explain how Fadavi-Ardekani in combination with G.992.2 discloses wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message, and I incorporate that discussion by reference. In the same way that the CO transceiver of Fadavi-Ardekani and G.992.2 would not allocate more memory for the interleaver than is specified in the messages that it exchanges during initialization, the transceiver would also not allocate more memory for the deinterleaver than is specified in the messages that it exchanges during initialization, in my opinion.

f. **5[f]. “allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate”**

501. Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[f]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1.

502. Above at Section IX.D.2.g, I explain how Fadavi-Ardekani in combination with G.992.2 allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes transmitted at a second data rate. Also,

at Section IX.D.2.e above, I explain how Fadavi-Ardekani in combination with G.992.2 discloses allocating a first number of bytes of the shared memory to an interleaver to interleave a first plurality of RS coded data bytes transmitted at a first data rate. I incorporate both of those sections herein by reference, and, on that basis, it is my opinion that the combination of Fadavi-Ardekani and G.992.2 discloses this limitation.

g. 5[g]. “deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver”

503. Fadavi-Ardekani in combination with G.992.2, in my opinion, discloses limitation 5[g]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 7:25-30; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1.

504. Above at Section IX.D.2.h, I explain how Fadavi-Ardekani in combination with G.992.2 discloses interleaving a first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference. Though this limitation recites a first plurality being deinterleaved, and a second plurality of data bytes being interleaved, in my opinion, there is no difference in how a transceiver would implement this limitation. Therefore, it is my opinion that Fadavi-Ardekani and G.992.2 disclose this limitation.

h. 5[h]. “wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver”

505. Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[h]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1.

506. I explain above at Section IX.D.2.i how it is my opinion that Fadavi-Ardekani in view of G.992.2 discloses “wherein the shared memory allocated to the interleaver is used at the

same time as the shared memory allocated to the deinterleaver,” and I incorporate that discussion by reference herein. In my opinion, one of ordinary skill in the art would have understood that there is no difference between these two limitations, i.e., they both require that the deinterleaver and interleaver memory be used at the same time. Accordingly, it is my opinion that this limitation is met by Fadavi-Ardekani in combination with G.992.2.

4. Claim 13 of the '882 Patent

507. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 13 of the '882 patent, as I explain below.

a. 13[a]. “A system that allocates shared memory”

508. To the extent that this preamble is limiting, Fadavi-Ardekani in combination with G.992.2 discloses a system that allocates shared memory. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3.

509. This preamble is identical to the preamble of claim 1 of the '048 patent, and for the same reasons, it is my opinion that the preamble is disclosed by Fadavi-Ardekani in view of G.992.2. *See* Section IX.D.2.a.

b. 13[b]. “a transceiver that performs”

510. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses a transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67. This limitation is identical to the second limitation of claim 1 of the '048 patent, except that it recites “a transceiver that performs” additional steps. In my opinion, this limitation is met for the same reasons that I explain above at Section IX.D.2.b, and I incorporate my opinions herein by reference.

c. 13[c] through 13[i].

511. These limitations are identical to the corresponding limitations of claim 5 of the '381 patent that I discuss above at Sections IX.D.3.c through IX.D.3.i (claim 1) and Sections

IX.B.4.b through IX.B.4.h (claim 5), and I incorporate those opinions herein by reference. *See* Appx. 3 (comparing limitations of claim 5 of the '381 patent with limitations of claim 13 of the '882 patent). For the same reasons, it is my opinion that these limitations are met by Fadavi-Ardekani in combination with G.992.2.

5. Claim 19 of the '473 Patent

512. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 19 of the '473 patent.

a. 19[a]. "An apparatus comprising"

513. To the extent that the preamble is limiting, Fadavi-Ardekani discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, Fadavi-Ardekani at Abstract; col. 1:12-14; col. 2:18-24; col. 2:62-67. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.a.

b. 19[b]. "a multicarrier communications transceiver"

514. It is my opinion that Fadavi-Ardekani discloses a multicarrier communications transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67; G.992.2, §§ 4.1, 4.2, 5, Fig. 2. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.b.

515. G.992.2 similarly discloses a transceiver, an ADSL transceiver unit (ATU) that complies with the G.992.2 standard. *See* G.992.2, §§ 4.1, 4.2, Fig. 2. G.992.2 explains that "[t]he ATU shall transport a single duplex bearer channel," which would indicate to one of ordinary skill in the art that the ATU is capable of transmitting and receiving data. ADSL systems, such as G.992.2, would be recognized by one of ordinary skill in the art as being multicarrier communications systems. One of ordinary skill in the art would further have

understood that the transmitter and receiver portions share some common circuitry, such as, for example, an interface to the subscriber line.

c. **19[c]. “that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path”**

516. Fadavi-Ardekani in combination with G.992.2 discloses limitation 19[c], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 6:66-7:33. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.c.

517. Similarly G.992.2 discloses a duplex connection that includes both an upstream path and a downstream path. *See* G.992.2, § 5 (“The ATU shall transport a single duplex bearer channel. The bearer channel data rate shall be programmable in multiples of 32 kbit/s.”). The upstream path and the downstream path are associated with an interleaver and a deinterleaver. *See id.* at § 7.6, § 7.3.1 (“The framing is equivalent to the ‘reduced overhead mode with merged fast and sync bytes’ as defined in Recommendation 7.4.4.2/G.992.1 using only the ‘interleave buffer’ definition.”); § 7.3.3 (“A cyclic redundancy check (crc), scrambling, forward error correction (FEC) coding and interleaving shall be applied to the contents of the superframe.”). One of ordinary skill in the art would have understood that these upstream and downstream paths are associated with interleaving and deinterleaving functions.

518. Therefore, Fadavi-Ardekani in combination with G.992.2 discloses this limitation, in my opinion.

d. **19[d]. “the multicarrier communications transceiver being associated with a memory”**

519. In my opinion, Fadavi-Ardekani discloses limitation 19[d]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3. I incorporate by reference my

analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.d.

e. **19[e]. “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”**

520. Fadavi-Ardekani, in combination with G.992.2, discloses limitation 19[e], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.e.

521. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta’s infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then the combination of Fadavi-Ardekani and G.992.2 discloses this limitation under TQ Delta’s interpretation of the claims.

522. One of ordinary skill in the art would have understood that ADSL transceivers described in G.992.2 were capable of sending messages, including initialization messages, specifying communications parameters in ADSL systems. For example, G.992.2 teaches transceivers that exchange initialization messages that contain information about the channel as well as the transceivers and their capabilities and requirements. G.992.2, § 11.1.1 (“In subsequent parts of the initialization, in order to maximize the throughput and reliability of this link, ADSL transceivers shall determine certain relevant attributes of the connecting channel and establish transmission and processing characteristics suitable to that channel. During

initialization each receiver can determine the relevant attributes of the channel through the transceiver training and channel analysis procedures.”). This includes communicating to a far-end transceiver “the number of bits and relative power levels to be used on each DMT subcarrier, as well as any messages and final data rates information.” *Id.*

523. G.992.2 describes exchanging messages between the transceivers in an iterative process to establish transmission parameters such as data rates and formats for the ATU-R. The C-RATES1 message defined in G.992.2 is a signal sent from the ATU-C, whose purpose “is to transmit four options for data rates and formats to the ATU-R.” *Id.* at § 11.9.2. Each of the four options contains three fields, one of which is the RRSI field that “contains Reed-Solomon FEC and interleaver parameters.” The RRSI contains ten entries, including the number of DFs per Reed-Solomon codeword in the downstream direction, downstream interleave depth in codewords, the number of DFs per Reed-Solomon codeword in the upstream direction, and the upstream interleaver depth in codewords. *See id.*; *see also* Table 26, Table 27.

524. An additional initialization message is the C-RATES-RA message, which sends “four new options for transport configuration for both upstream and downstream. These options will, in general, be closer to the optimum bit rate for the channel than those in C-RATES1. . . .” G.992.2, § 11.11.3. Like the C-RATES1 message, the C-RATES-RA message contains ten entries, including the numbers of data frames (DFs) per Reed-Solomon codeword in the downstream direction, downstream interleave depth in codewords, the number of DFs per Reed-Solomon codeword in the upstream direction, and the upstream interleave depth in codewords. *See id.*; *see also* Table 33, Table 34. It is my understanding that the Court construed the term “memory is allocated between the interleaving function and the deinterleaving function” to mean “an amount of memory is allocated to the interleaving function and an amount of memory

is allocated to the deinterleaving function.” As with the parameters in the C-RATES1 message, one of ordinary skill in the art would have understood that the information in the C-RATES-RA message can be used to allocate memory between an interleaver and a deinterleaver function, at least within TQ Delta’s interpretation of the claims.

f. **19[f]. “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.”**

525. Fadavi-Ardekani, in combination with G.992.2, discloses limitation 19[f], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.f.

526. Additionally, one of ordinary skill would have understood that G.992.2 discloses that the interleaver memory and the deinterleaver memory are used at the same time. G.992.2 establishes a “single duplex bearer channel.” G.992.2, § 5. One of ordinary skill in the art would have understood that data is transmitted in both directions at the same time. As a result, the interleaver and deinterleaver are both used at the same time, which in turn, means that the interleaver memory and deinterleaver memory are used at the same time. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation.

6. **Motivation to Combine Fadavi-Ardekani and G.992.2**

527. One of ordinary skill in the art would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.992.2 in the manner claimed. First, both references are in the telecommunications field, and relate to ADSL systems specifically. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:63-3:4; col. 4:9-21; col. 4:25:63 (describing an ADSL communication system); col. 4:65-5:40 (describing head-end ADSL transceiver); G.992.2, §§ 1

(“The requirements of the Recommendation apply only to a single asymmetric digital subscriber line (ADSL).”); 4.1 (“The system reference model shown in Figure 1 describes the functional blocks required to provide ADSL service.”); FIG. 1, FIG. 2. In addition, Fadavi-Ardekani references G.992.2 a number of times, confirming that one of ordinary skill in the art would naturally consider the references together. *See, e.g.*, Fadavi-Ardekani, col. 6:19-23 (“All functionalities of the FCI are provided as per ADSL standards. In a preferred embodiment of the invention, approximately four G.lite (ITU G.992.2) or approximately four ADSL (ANSI T1.413-1998) sessions are supported by the FCI.”); col. 1:51-60 (“Many DSL technologies require that a signal splitter be installed at a remote end user location to split POTS service from the digital data transmission. However, the line split for an end user can be managed remotely from a central office using G.Lite (a/k/a DSL Lite, splitterless ADSL, and Universal ADSL), which is essentially a slower form of ADSL. Equipment installation costs are saved using G.Lite (ITU-T standard G-992.2), which provides a data rate of approximately 1.5 Mbps downstream and approximately 512 Kbps upstream.”); col. 4:59-63 (“An exemplary digital communication system employing G.lite is similar to FIG. 1, with splitters 130, 134 and 146 merely replaced by a hardware device providing a direct connection to ADSL transceivers 128, 136, and 148 respectively.”); col. 7:6-13 (“A simple implementation of a transmit interleaver for G.lite communication requires 4 Kbytes per session for downstream processing, derived by multiplying the maximum codeword length by the maximum interleaver depth. The simple G.lite transmit interleaver also requires 2 Kbytes per session for upstream processing. Therefore, 24 Kbytes of RAM is required to support four G.lite sessions.”). For this reason, one of ordinary skill in the art would naturally have looked to G.992.2 when considering Fadavi-Ardekani.

528. Second, both references describe the need to allocate memory between interleaving and deinterleaving functions. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3, G.992.2, §§ 7.6; 11.1.1. Thus, both Fadavi-Ardekani and G.992.2 relate to the problem to be solved identified by the Family 3 patents – allocating shared memory between interleaving and deinterleaving functions. *See, e.g.*, '048 patent, col. 1:48-59 (“One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability.”). One of ordinary skill in the art naturally would have consulted Fadavi-Ardekani for its description of calculating and allocating memory between interleaver and deinterleaver functions when considering G.992.2 and its description of using interleavers and exchanging parameters, such as interleaver parameters, relating to transceivers during initialization.

529. Third, one of ordinary skill in the art, when considering Fadavi-Ardekani, would have naturally looked to G.992.2, and specifically to determine how to allocate shared memory. Fadavi-Ardekani discloses reducing the difficulty of the interleaving/deinterleaving process as a goal. *See, e.g.*, Fadavi-Ardekani, col. 3:1-4 (“Utilizing this buffering and scheduling methodology, reductions in the design sizes of various transceiver components and the data flow complexity of the transceiver may be achieved.”). Fadavi-Ardekani faults prior art systems for being “excessively duplicative in terms of transceivers and memory in each transceiver, and thus more costly than necessary to provide the desired functionality.” *Id.* at col. 2:57-59. It also discloses that reducing the amount of memory needed is desirable. *Id.* at col. 3:43-47; col. 8:4-12; 9:20-23. To do so, Fadavi-Ardekani discloses sharing one memory for

both interleaving and deinterleaving. *See, e.g., id.* at Abstract; col. 3:39-41; col. 7:25-30; col. 9:18-20.

530. Fadavi-Ardekani further explains that the amount of memory required by, and the allocation of memory between, the interleaver and deinterleaver depends on the services to be supported. Fadavi-Ardekani, col. 6:66-7:33 (“In a preferred embodiment of the invention, the IDIM is allocated as 10 K×16 (i.e., 20 K) Random Access Memory (RAM), which supports approximately four G.lite or approximately four standard ADSL session/s at less than full interleave depth. The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention.”). One of ordinary skill would have recognized that, in order to allocate memory between interleaver and deinterleaver functions in a useful way, the transceiver would need information about the amount of memory needed for the services that were to be supported by the transceiver.

531. As I describe above, G.992.2 discloses that the transceivers share information about the relevant attributes of the channel between them and the parameters they will use for interleaving and deinterleaving. *See, e.g.,* G.992.2, §§ 7.6, 11.1.1, 11.9.2 (describing C-RATES1 message); 11.11.3 (describing C-RATES-RA message). One of ordinary skill in the art would have been motivated to look to the teachings of G.992.2 for ways of exchanging interleaver parameters, such that memory can be shared as described in Fadavi-Ardekani.

E. Claim 19 of the '473 Patent Is Obvious Over Voith in Combination with LB-031

532. It is my opinion that claim 19 of the '473 patent is obvious over U.S. Patent No. 5,751,741 (“Voith”) in combination with LB-031. I have reviewed TQ Delta’s infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta’s

interpretation of the claims, however, then Voith in combination with LB-031 renders obvious claim 19 of the '473 patent.

1. Brief Description of Voith

533. Voith describes an ADSL transceiver that transmits and receives data using discrete multi-tone (DMT) multicarrier communications. *See, e.g.*, Voith at Abstract; col. 1:25-50; col. 2:61-64. A transmit section of the transceiver performs rate adaptation using a single rate adaptation buffer, without the need for multiple frame buffering. *Id.* at col. 2:64-67.

534. FIG. 2 of Voith, copied below, illustrates an ADSL transceiver with a digital interface unit, and FIG. 3 of Voith, also copied below, illustrates the digital interface unit.

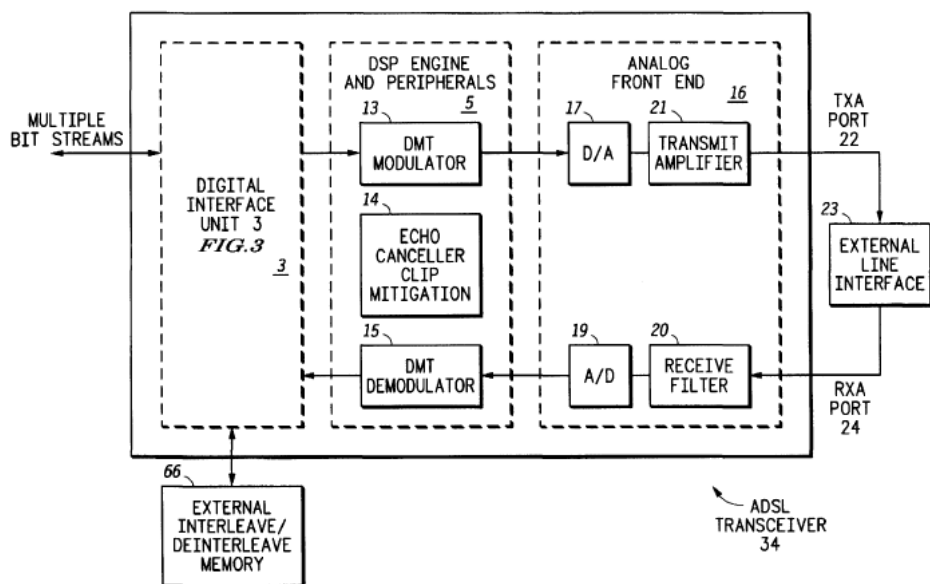


FIG. 2

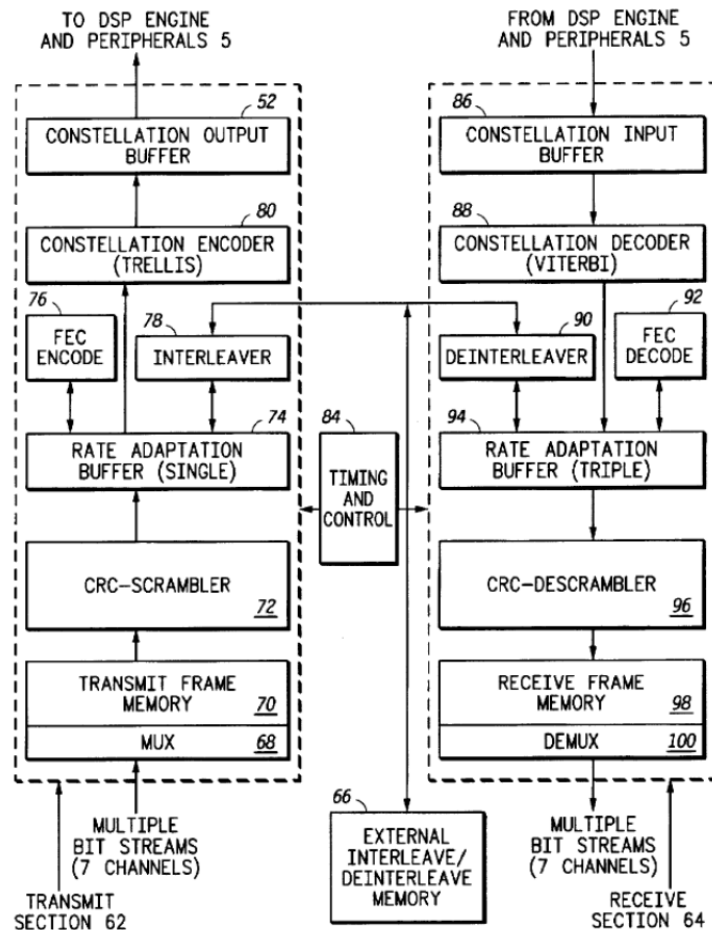


FIG. 3

The digital interface unit has a transmit section and a receive section, which respectively

“interleave[] transmit data and de-interleave[] receive data.” *Id.* at col. 4:30-32; col. 4:44-45.

Voith teaches that in order to accomplish the interleaving and deinterleaving, “ADSL transceiver 34 requires a large amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66.” *Id.* at col. 4:32-36.

535. The transceiver includes a common timing and control portion that coordinates the operation between the transmit and receive sections. *Id.* at col. 4:41-49; FIG. 3. A timing control block generates timing signals and also coordinates the activities of several modules in the transmit and receive paths so that their activities do not conflict. *Id.* at col. 4:50-55. The

timing control block also includes a memory arbitrator that arbitrates between the transmit and receive path for access to external interleave/deinterleave memory, “which is used by both transmit section 62 and receive section 64.” *Id.* at col. 4:47-50; col. 4:55-58.

536. The transmit section of Voith’s ADSL transceiver includes, among other things, an FEC encode block and an interleaver. *Id.* at col. 4:59-5:6; FIG. 3. The interleaver also has a bidirectional terminal connection to the external interleave/deinterleave memory. *Id.* at col. 5:6-8.

537. The receive section of Voith’s ADSL transceiver includes, among other things, a deinterleaver and an FEC decode block. *Id.* at col. 5:13-17; FIG. 3. Like the interleaver, the deinterleaver has a bidirectional terminal connection to the external interleave/deinterleave memory. *Id.* at col. 5:21-23.

538. The FEC encoder of Voith “performs a forward error correction encoding first on fast data and next on interleaved data in the frame and appends redundancy bytes to the frame and stores those in appropriate portions of the rate adaptation buffer.” *Id.* at col. 5:58-62. The interleaver operates only on the interleave portion of the frame, and both reads data out of and writes data back into the rate adaptation buffer. *Id.* at col. 5:62-65. Because the interleaving operation requires a large amount of memory, the interleaver uses a portion of the external interleave/deinterleave memory, and arbitrates with the deinterleaver so that only one external memory interface using common integrated circuit pins is required. *Id.* at 5:65-6:4. Voith’s memory thus is allocated between the interleaving function and the deinterleaving function, in which at least a portion of the memory may be allocated to the interleaving function or deinterleaving function at any one particular time.

539. In the receive section of Voith's transceiver, a deinterleaver performs a deinterleave operation on the interleaved portion of the received frame. *Id.* at col. 6:24-26. The deinterleaver "makes use of external interleave/deinterleave memory" and "arbitrates for usage thereof in a manner similar to" the interleaver. *Id.* at col. 6:26-29. The FEC decode "first performs an FEC decode operation on the fast portion of the frame data, and then performs an FEC decode operation on the interleaved portion of the frame data." *Id.* at col. 6:29-32. If the FEC decode detects an error in the frame data, it performs correction within the rate adaptation buffer. *Id.* at col. 6:32-34.

2. Claim 19 of the '473 Patent

540. In my opinion, Voith in combination with LB-031 discloses each limitation of claim 19 of the '473 patent.

a. 19[a]. "An apparatus comprising"

541. In my opinion, to the extent that the preamble is limiting, Voith in combination with LB-031 discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.,* Voith at Abstract; col. 1:25-50; col. 2:61-67; FIGS. 2-3.

b. 19[b]. "a multicarrier communications transceiver"

542. It is my opinion that Voith in combination with LB-031 discloses limitation 19[b]. *See, e.g.,* Voith, Abstract; col. 1:25-30; col. 2:61-3:9; Figs. 2, 3; LB-031, p. 3, 4.

543. One of ordinary skill in the art would have understood that Voith discloses a multicarrier communications transceiver because it discloses an ADSL transceiver that implements DMT, which is a type of multicarrier modulation. *See, e.g.,* Voith, Abstract (noting that transceiver can receive data at 4.05 kHz); col. 1:25-37 ("Discrete multi-tone (DMT) is a multi-carrier technique which divides the available bandwidth of twisted-pair copper media connections into mini-subchannels or bins. . . ."); col. 2:61-3:9; FIGS. 2-3.

544. I explained above in Section IX.A.6.b why, in my opinion, LB-031 discloses a multicarrier communications transceiver, namely a VTU-O and a VTU-R. *See* LB-031 at pp. 3, 4. I incorporate by reference my analysis and opinion from that section.

545. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

c. **19[c]. “that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path”**

546. In my opinion, Voith in view of LB-031, discloses limitation 19[c]. *See, e.g.*, Voith, col. 4:42-48; col. 4:59-5:12; col. 5:58-6:4; LB-031, pp. 2, 3.

547. Voith describes the signal processing in the transmit section as being “defined by the ADSL standard” and describes the framing of separate fast and interleaved data into DMT symbols for transmission. *See, e.g.*, Voith at col. 5:40-6:4 (“[S]even channels of payload data are then stored in corresponding portions of transmit frame memory 70. In addition, transmit frame memory 70 appends a FAST byte and a SYNC byte, defined by the ADSL standard, at the appropriate points in the frame. . . . CRC-scrambler 72 performs an 8-bit cyclic redundancy check first on the fast data and then on the interleaved data. The scrambler function of CRC-scrambler 72 also operates first on the fast data and next on the interleaved data. . . . FEC encode 76 performs a forward error correction encoding first on fast data and next on the interleaved data in the frame and appends redundancy bytes to the frame and stores those in appropriate portions of rate adaptation buffer 74. Interleaver 78 operates only on the interleave portion of the frame, and reads data out of rate adaptation buffer 74 and writes data back into rate adaptation buffer 74 after performing the interleaving operation. Because the interleaving operation requires a large amount of memory, interleaver 78 uses a portion of external interleave/deinterleave memory 66. Interleaver 78 arbitrates for use of external

interleave/deinterleave memory 66 with deinterleaver 90 so that only one external memory interface using common integrated circuit pins is required.”). I understand that the Court has construed the term “latency path” to mean “transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay.” As a skilled artisan would have understood as of the Family 3 patents’ priority date, the fast data and interleaved data are each associated with a separate latency path, each with a distinct latency. Therefore, the transmit section of Voith handles two latency paths, one of which is interleaved.

548. The receive section of Voith processes the received data similarly and also handles two latency paths, fast and interleaved. *See, e.g., id.* at col. 6:24-34 (in receive section, “[a] deinterleaver 90 performs a deinterleave operation on the interleaved portion of the received frame. Deinterleaver 90 makes use of external interleave/deinterleave memory 66 and arbitrates for usage thereof in a manner similar to interleaver 78. FEC decode 92 first performs an FEC decode operation on the fast portion of the frame data, and then performs an FEC decode operation on the interleaved portion of the frame data. If FEC decode 92 detects an error in the frame data, it performs correction within rate adaptation buffer 94.”). Thus, the receive section of Voith also handles two latency paths, one of which is interleaved, each of which has a distinct latency. Consequently, Voith discloses a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path (the interleaved path in the transmit direction) and perform a deinterleaving function associated with a second latency path (the interleaved path in the receive direction).

549. As I explained above in Section IX.A.6.c, LB-031 also teaches a transceiver that is configured to perform an interleaving function associated with a first latency path, and a

deinterleaving function associated with a second latency path. *See, e.g.*, LB-031 at pp 2, 3. I incorporate by reference my analysis and opinion from that section.

550. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

d. **19[d]. “the multicarrier communications transceiver being associated with a memory”**

551. In my opinion, Voith alone or in view of LB-031 discloses limitation 19[d]. *See, e.g.*, Voith, col. 4:21-40; col. 4:59-5:39; Fig. 3; LB-031, pp. 3, 4.

552. FIG. 3 of Voith illustrates a memory associated with the transceiver, an “external interleave/deinterleave memory 66, which is used by both transmit section 62 and receive section 64.” Voith, col. 4:49-50. Voith specifically notes that the “[i]nterleaver 78 also has a second bidirectional terminal connected to external interleave/deinterleave memory 66,” and that the “[d]e-interleaver 90 has a first bidirectional terminal, and a second bidirectional terminal connected to external interleave/deinterleave memory 66.” Voith, col. 5:5-7; 5:21-23; *see also id.* at col. 4:21-40; FIG. 3.

553. I explained above in Section IX.A.6.d why, in my opinion, LB-031 also teaches the multicarrier communications transceiver being associated with a memory. *See, e.g.*, LB-031 at pp. 3, 4. I incorporate by reference my analysis and opinion from that section.

554. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

e. **19[e]. “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”**

555. Voith, in combination with LB-031, discloses limitation 19[e], in my opinion. *See, e.g.*, Voith, col. 5:58-6:43; LB-031, at p. 3.

556. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then Voith in combination with LB-031 discloses this limitation under TQ Delta's interpretation of the claims.

557. Voith discloses allocating memory between the interleaving function and the dinterleaving function. *See, e.g.,* Voith, at col. 5:58-6:43. Voith specifically notes that "[b]ecause the interleaving operation requires a large amount of memory," the interleaver "uses a portion of external interleave/deinterleave memory 66." *Id.* at col. 5:65-6:1. Voith also discloses that its interleaver "arbitrates" with the deinterleaver for use of external the interleave/deinterleave memory. *Id.* at col. 6:1-4. Voith also discloses that a deinterleaver performs a deinterleave operation on the interleaved portion of the received frame. *Id.* at col. 6:24-26. Voith's deinterleaver "makes use of external interleave/deinterleave memory 66" and "arbitrates for usage thereof" in a manner similar to the interleaver. *Id.* at col. 26-29. It is my understanding that the Court construed the term "memory is allocated between the interleaving function and the deinterleaving function" to mean "an amount of memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function."

558. LB-031 teaches the well-known principle that the amount of memory required to meet a particular interleaver delay requirement depends on the line data rate. *See* LB-031 at p. 4. The line data rate, in turn, depends on the number of bits assigned to each subcarrier. Voith discloses that "[t]he bit allocation table is determined at initialization between the central office

and the remote terminal based on the characteristics of the transmission link.” Voith, col. 6:9-12. As a person having ordinary skill in the art would have understood as of the Family 3 patents’ priority date, the bit allocation table is determined during initialization by the receiving transceiver and communicated to the transmitting transceiver in a message sent during the initialization procedure. Therefore, Voith discloses that the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver, at least within TQ Delta’s interpretation of the claims in its infringement contentions.

559. I explained above in Section IX.A.6.e why, in my opinion, LB-031 also discloses allocating a memory between the interleaving function and the deinterleaving function. *See, e.g.*, LB-031 at p. 3. I incorporate by reference my analysis and opinion from that section.

560. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

f. **19[f]. “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

561. Voith, in view of LB-031, discloses limitation 19[f], in my opinion. *See, e.g.*, Voith, col. 4:50-58; col. 5:58-6:43; LB-031, p. 3.

562. Voith specifically explains that a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time. Voith, col. 5:65-6:4 (“Because the interleaving operation requires a large amount of memory, interleaver 78 uses a portion of external interleave/deinterleave memory 66. Interleaver 78 arbitrates for use of external interleave/deinterleave memory 66 with deinterleaver 90 so that only one external memory interface using common integrated circuit pins is required.”); *id.* at col. 4:50-58

(“Timing control block 84 generates timing signals which are necessary for the signal processing functions. Timing control block 84 also coordinates the activities of several modules in both the transmit and receive path so that their activities do not conflict. Furthermore, timing control block 84 includes a memory arbitrator that arbitrates between the transmit and receive path for access to external interleave/deinterleave memory 66.”); *id.* at col. 6:26-29

(“Deinterleaver 90 makes use of external interleave/deinterleave memory 66 and arbitrates for usage thereof in a manner similar to interleaver 78.”); *id.* at col. 4:35-41 (“in order to minimize the number of integrated circuit pins required to access external memory, the interleave and de-interleave buffers are also preferably implemented in the same physical memory and digital interface unit 3 preferably multiplexes between interleaving and de-interleaving operations.”); *id.* at col. 4:30-32 (“As part of the ADSL task, digital interface unit 3 also interleaves transmit data and de-interleaves receive data.”).

563. As noted above, Voith also discloses that memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver. *Id.* at col. 5:58-6:43. Consequently, at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

564. I explained above in Section 244 why, in my opinion, LB-031 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message. *See, e.g.*, LB-031 at p. 3. I incorporate by reference my analysis and opinion from that section.

565. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

3. Motivation to Combine Voith and LB-031

566. In my opinion, one of ordinary skill in the art would have been motivated to combine Voith and LB-031 for at least the following reasons. First, each is in the telecommunications field. Each discloses sharing memory for interleaving and deinterleaving to support various applications. *See, e.g.*, Voith, col. 4:29-58; col. 5:65-6:4; *see also* LB-031 at p. 2 (“The smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver [3]. Typically, for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same.”); *id.* at p. 3 (“The size of the interleaver memory will be a major source of complexity in VDSL2.”); *id.* at p. 4 (“Suppose a VDSL2 transceiver supports up to 44.5 Mbit/s as a line data rate. If the minimum interleaver delay requirement were 5.23ms, then, from equation (5) and equation (1), this transceiver must support a delay of at least 29092 octets which corresponds to having an interleaver memory of at least 14546 octets according to equation (2) (although this is actually implementation specific).”).

567. Thus, in my opinion, both Voith and LB-031 relate to the problem purportedly addressed by the ’473 patent—allocating memory for interleaving and deinterleaving to support various applications. *See, e.g.*, ’473 patent at col. 1:37-45; *id.* at col. 1:48-60. One of ordinary skill in the art would naturally have considered these complementary references together.

568. Furthermore, LB-031 explains that “[t]he interleaver is a major source of complexity in VDSL2,” (LB-031 at p. 1), and Voith discloses that efficiency in the use and management of memory is desirable. *See, e.g.*, Voith, at col. 2:26-28 (“[L]arge buffers consume a large integrated circuit area which adds to its cost.”); *see also id.* at col. 4:30-40 (“As part of the ADSL task, digital interface unit 3 also interleaves transmit data and de-interleaves receive data. In order to perform these complex functions, ADSL transceiver 34 requires a large

amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66. Also, in order to minimize the number of integrated circuit pins required to access external memory, the interleave and de-interleave buffers are also preferably implemented in the same physical memory and digital interface unit 3 preferably multiplexes between interleaving and de-interleaving operations.”). LB-031, meanwhile, discloses the desirability of balancing efficiency and performance. *See, e.g.*, LB-031 at p. 3 (“Equations (2), (4), (5), and (6) illustrate trade-offs between interleaver memory, error correction capability, delay, and burst separation. More interleaver memory normally allows more error correction but leads to higher delays and a longer separation between error bursts. Significant error correction can be achieved by using shorter codewords requiring less memory, less delay, and shorter time between bursts. However, small codewords typically have lower net coding gain and higher computation requirements since there are more decoder operations required in the same amount of time. Therefore, we make a trade-off between complexity, capability, and performance.”).

569. In my opinion, one of ordinary skill in the art would have naturally considered the advantages of each of these references, including their common goals of allocating memory for interleaving and deinterleaving operations, and would have been motivated to combine them. One of ordinary skill in the art considering Voith would have naturally looked to LB-031 to determine an effective and efficient way to allocate memory between interleaving and deinterleaving functions, including allocating memory at any one particular time depending on the message. One of ordinary skill in the art would have had a reasonable expectation that this combination would work and would be relatively straightforward to implement. There would have been substantial motivation to combine these references prior to the invention date.

F. Claim 19 of the '473 Patent is Obvious In View of Mazzoni and G.993.1.

570. It is my opinion that Mazzoni in combination with G.993.1 discloses each limitation of claim 19 of the '473 patent. I explain below at Section IX.F.4 why it is my opinion that one of ordinary skill in the art would have been motivated to combine Mazzoni and G.993.1. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then Mazzoni in combination with G.993.1 renders obvious claim 19 of the '473 patent.

1. Brief Description of Mazzoni

571. I provided a brief description of Mazzoni above in Section IX.B.2, which I incorporate by reference.

2. Brief Description of G.993.1

572. I provided a brief description of G.993.1 above in Section VII.F.4, which I incorporate by reference.

3. Claim 19 of the '473 Patent

573. In my opinion, Mazzoni in combination with G.993.1 discloses each limitation of claim 19 of the '473 patent.

a. 19[a]. "An apparatus comprising"

574. In my opinion, and to the extent that this preamble is limiting, Mazzoni in combination with G.993.1 discloses an apparatus, a multicarrier communications transceiver, as I describe below.

b. 19[b]. “a multicarrier communications transceiver”

575. It is my opinion that Mazzoni in combination with G.993.1 discloses a multicarrier communications transceiver. *See, e.g.*, Mazzoni, col. 1:8-27; G.993.1 §§ 4; 5.2, 6.7, 8.5.1, 9.2.1, Fig. 5-2.

576. As I explain above in Section IX.B.6.b, which I hereby incorporate by reference here, Mazzoni discloses that its invention “may advantageously applied to a very high rate digital subscriber line (VDSL) environment or system,” which a person having ordinary skill in the art would have understood to include VDSL transceivers according to G.993.1. *See* Mazzoni, col. 1:19-21. Similarly, I have also explained how G.993.1 discloses a VDSL transceiver, which employs multicarrier communications, at Section IX.C.6.b, which I also incorporate by reference here.

577. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

c. 19[c]. “that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path”

578. It is my opinion that Mazzoni in combination with G.993.1 discloses limitation 19[c]. *See, e.g.*, Mazzoni, col. 3:62-4:25; Fig. 3; G.993.1, §§ 8.4.1, 8.4.2.

579. I explain above at Section IX.B.6.c, which I hereby incorporate by reference here, how it is my opinion that Mazzoni discloses an interleaving function associated with a first latency path, and a deinterleaving function associated with a second latency path, by explaining that its VDSL communication system allows the operator to provide multiple symmetrical and asymmetrical services. In addition, I explain above that G.993.1 discloses transceivers that are configured to support multiple latency paths and perform interleaving and deinterleaving

functions using a convolutional interleaver associated with those latency paths (see Section IX.C.6.c). I incorporate my previous discussion and opinions by reference.

580. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

d. 19[d]. “the multicarrier communications transceiver being associated with a memory”

581. Mazzoni in combination with G.993.1 discloses limitation 19[d], in my opinion. *See, e.g.*, Mazzoni, col. 1:59-2:24; col. 2:37-48; col. 2:57-3:4; col. 5:9-20; Fig. 3, 4, 5; G.993.1, § 8.4.1.

582. It is my opinion, as I explain above at Section IX.B.6.d, which I hereby incorporate by reference, that this limitation is met by Mazzoni’s memory associated with an interleaving and deinterleaving means, which may be a RAM such as a dual-port memory. *See, e.g.*, Mazzoni, col. 2:57-60. In addition, G.993.1 discloses memory associated with an interleaver and deinterleaver pair, as I describe in Section IX.C.6.d, which I also incorporate by reference.

583. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

e. 19[e]. “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”

584. In my opinion, Mazzoni in combination with G.993.1 discloses limitation 19[e]. *See, e.g.*, Mazzoni, col. 1:59-65; col. 2:3-18; col. 5:21-30; G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.3.1.1.

585. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message

described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then Mazzoni in combination with G.993.1 discloses this limitation under TQ Delta's interpretation of the claims.

586. I previously explained that Mazzoni discloses how the memory allocation can be determined, and reconfigured, based on the bit rate processed by a modem, above at Section IX.B.6.e, which I incorporate by reference. *See* Mazzoni, col. 1:61-65; col. 5:24-31. G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver, as I explain above at Section IX.C.6.e, which I also incorporate by reference.

587. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

f. **19[f]. “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

588. It is my opinion that Mazzoni and G.993.1 disclose limitation 19[f]. *See, e.g.*, Mazzoni, col. 1:59-65; col. 2:3-18; col. 5:21-30; G.993.1, §§ 8.4.1, 8.4.2.

589. Above, I explain how Mazzoni discloses allocating distinct portions of a common memory to an interleaver and a deinterleaver, such that a portion is used by either function at any particular time, according to the message, at Section 339, which I incorporate by reference. G.993.1 similarly teaches that a portion of memory can be allocated to an interleaver and a deinterleaver, which I explain above at Section IX.C.6.f, and incorporate by reference.

590. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

4. **Motivation to Combine Mazzoni and G.993.1**

591. In my opinion, one of ordinary skill in the art would have been motivated to combine Mazzoni and G.993.1, as I explain below.

592. First, Mazzoni and G.993.1 are both specifically directed to VDSL and to VDSL transceivers. G.993.1 was the first of the ITU-T's specifications for VDSL transceivers, and the title of Mazzoni is "Device for Sending/Receiving Digital Data Capable of Processing Different Bit Rates, in Particular in a VDSL Environment."

593. Second, each of Mazzoni and G.993.1 discloses a need to allocate memory for interleaving and deinterleaving. *See, e.g.*, Mazzoni, col. 1:8-15 ("Moreover, the invention relates to sending and receiving digital data that can have different bit rates, and to choosing the capacity of memory means used by interleaving and deinterleaving processes effected within send/receive devices capable of processing different bit rates."); col. 1:54-65 ("Still another object of the invention is to provide such an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates."); G.993.1 at § 5.1, p. 5 ("The reference configuration provides two or four data paths with bit rate under the control of the network operator, consisting of one or two downstream and one or two upstream data paths. A single path in each direction can be of high latency (with lower BER expected) or lower latency (with higher BER expected). Dual paths in each direction provide one path of each type. The dual latency configuration is thought to be the minimum that is capable of supporting a sufficient full service set, although there are organizations supporting both the single latency model with programmable latency, and others requesting more than two paths/latencies."); §

8.4.1, p. 15 (“The same size interleaving memory... is needed for interleaving at the transmitter and de-interleaving at the receiver.”).

594. Thus, both references relate to the problem purportedly addressed by the ’473 patent—allocating memory for interleaving and deinterleaving to support various applications. *See, e.g.*, ’473 Patent at col. 1:37-45; col. 1:48-60. As a result, one of ordinary skill in the art would naturally have considered Mazzoni and G.993.1 together.

595. Mazzoni describes how sharing memory between interleaving and deinterleaving functions is advantageous, and that optimizing the size of the memory is advantageous. *See, e.g.*, Mazzoni, col. 1:54-65 (“Still another object of the invention is to provide such an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates. These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).”). Mazzoni discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See id.* at col. 6:51-61. As a person having ordinary skill in the art as of the ’473 patent’s priority date would have understood, Mazzoni’s table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers. One of ordinary skill in the art would have recognized that conveying interleaver parameters through the initialization message scheme of G.993.1 would avoid this limitation of Mazzoni’s table and would result in a more flexible solution.

G. **Claim 19 of the '473 Patent is Obvious In View of Voith and G.993.1, or, In the Alternative, In View of Voith, G.993.1 and Mazzoni.**

596. It is my opinion that Voith in combination with G.993.1 discloses each limitation of claim 19 of the '473 Patent. In the alternative, and to the extent that the combination of Voith and G.993.1 is not deemed to disclose each limitation of claim 19 of the '473 patent, it is my opinion that Mazzoni supplies the missing teachings, as I explain below at Section IX.G.4. I explain below why one of ordinary skill in the art would be motivated to combine Voith with G.993.1, and Voith and G.993.1 with Mazzoni, below at Sections IX.G.3 and IX.G.5, respectively.

597. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then Voith in combination with G.993.1, or Voith in combination with G.993.1 and Mazzoni, renders obvious claim 19 of the '473 patent.

1. **Brief Descriptions of Voith, G.993.1, and Mazzoni.**

598. I provide a brief description of Voith above at Section IX.E.1, G.993.1 at Section VII.F.4, and Mazzoni at Section IX.B.2. I incorporate each of those sections herein by reference.

2. **Claim 19 of the '473 Patent**

a. **19[a]. "An apparatus comprising"**

599. In my opinion, and to the extent that this preamble is limiting, Voith in combination with G.993.1 discloses an apparatus, a multicarrier communications transceiver, as I describe below.

b. 19[b]. “a multicarrier communications transceiver”

600. It is my opinion that Voith in combination with G.993.1 discloses a multicarrier communications transceiver. *See, e.g.*, Voith, col. 2:61-3:9; col. 1:44-50; G.993.1 §§ 4; 5.2, 6.7, 8.5.1, 9.2.1, Fig. 5-2.

601. As I explain above in Section IX.E.2.b, which I incorporate by reference, Voith discloses an ADSL multicarrier communications transceiver that employs DMT. Similarly, I have also explained how G.993.1 discloses a VDSL transceiver, which also specifies DMT, at Section IX.C.6.b, which I also incorporate by reference.

602. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

c. 19[c]. “that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path”

603. It is my opinion that Voith in combination with G.993.1 discloses limitation 19[c]. *See, e.g.*, Voith, col. 4:29-58; Fig. 3; G.993.1, §§ 8.4.1, 8.4.2.

604. I explain above at Section IX.E.2.c, which I incorporate by reference, how it is my opinion that Voith discloses an interleaving function associated with a first latency path, and a deinterleaving function associated with a second latency path. In addition, I explain above how G.993.1 discloses how transceivers are configured to support multiple latency paths, and perform interleaving and deinterleaving functions using a convolutional interleaver, associated with those latency patents at Section IX.C.6.c, which I also incorporate by reference.

605. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

d. **19[d]. “the multicarrier communications transceiver being associated with a memory”**

606. Voith in combination with G.993.1 discloses limitation 19[d], in my opinion. See, e.g., Voith, col. 3:55-65; col. 4:29-58; Fig. 2, 3; G.993.1, § 8.4.1.

607. It is my opinion, as I explain above at Section IX.E.2.d, which I incorporate by reference, that this limitation is met by Voith’s external interleave/deinterleave memory. In addition, G.993.1 discloses memory associated with an interleaver and deinterleaver pair, as I describe in Section IX.C.6.d, which I also incorporate by reference.

608. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

e. **19[e]. “wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver”**

609. In my opinion, Voith in combination with G.993.1 discloses limitation 19[e]. See, e.g., Voith, col. 5:65-6:4; G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.3.1.1.

610. I have reviewed TQ Delta’s infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta’s infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then Voith in combination with G.993.1 discloses this limitation under TQ Delta’s interpretation of the claims.

611. I explain how Voith discloses allocating the external interleave/deinterleaver memory, while using an arbitration procedure between the two functions to do so, above at

Section IX.E.2.e, which I incorporate by reference. G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver, as I explain above at Section IX.C.6.e, which I also incorporate by reference.

612. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

f. **19[f]. “wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message”**

613. It is my opinion that Voith and G.993.1 disclose limitation 19[f]. *See, e.g.*, Voith, col. 5:64-6:4; G.993.1, §§ 8.4.1, 8.4.2.

614. Above, I explain how Voith discloses allocating its memory to an interleaver and a deinterleaver, such that a portion is used by either function at any particular time depending on the message at Section IX.E.2.f, which I incorporate by reference. G.993.1 similarly teaches that a portion of memory can be allocated to an interleaver or a deinterleaver depending on the message, which I explain above at Section IX.C.6.f, which I also incorporate by reference.

615. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

3. **Motivation to Combine Voith and G.993.1**

616. In my opinion, one of ordinary skill in the art would have been motivated to combine Voith and G.993.1, as I explain below.

617. First, each of the references is in the DSL field, and each discloses a need to allocate memory for interleaving and deinterleaving. *See, e.g.*, Voith, col. 4:29-41 (“As part of the ADSL task, digital interface unit 3 also interleaves transmit data and de-interleaves receive

data. In order to perform these complex functions, ADSL transceiver 34 requires a large amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66. Also, in order to minimize the number of integrated circuit pins required to access external memory, the interleave and de-interleave buffers are also preferably implemented in the same physical memory and digital interface unit 3 preferably multiplexes between interleaving and de-interleaving operations. . . .”); col. 4:51-58; col. 5:65-6:4; G.993.1 at § 5.1, p. 5 (“The reference configuration provides two or four data paths with bit rate under the control of the network operator, consisting of one or two downstream and one or two upstream data paths. A single path in each direction can be of high latency (with lower BER expected) or lower latency (with higher BER expected). Dual paths in each direction provide one path of each type. The dual latency configuration is thought to be the minimum that is capable of supporting a sufficient full service set, although there are organizations supporting both the single latency model with programmable latency, and others requesting more than two paths/latencies.”); § 8.4.1, p. 15 (“The same size interleaving memory... is needed for interleaving at the transmitter and de-interleaving at the receiver.”).

618. Thus, both references relate to the problem purportedly addressed by the ’473 patent—allocating memory for interleaving and deinterleaving to support various applications. *See, e.g.*, ’473 Patent at col. 1:37-45; col. 1:48-60. As a result, one of ordinary skill in the art would naturally have considered these references together. Further, Voith discloses that efficiency in the use of memory is desirable. *See, e.g.*, Voith at col. 1:44-47; col. 2:26-35.

619. As discussed above, G.993.1 discloses how memory is allocated in accordance with a message received during initialization. One of ordinary skill in the art would therefore have recognized that the teachings of G.993.1 show a reliable and efficient way of enabling the

transceivers of Voith to partition the shared memory between the interleaver and deinterleaver. By exchanging information about their available memory, using messaging like that disclosed in G.993.1, the transceivers of Voith would be able to determine an appropriate allocation of the available memory to the interleaver and deinterleaver.

620. One of ordinary skill in the art would have had a reasonable expectation that this combination would work and would be relatively straightforward to implement. For example, adding G.993.1 messaging scheme to a transceiver according to Voith would be relatively simple, as one of ordinary skill in the art would have understood, particularly in view of Voith's reference to ADSL, which also uses messaging during initialization to enable the ATU-C and ATU-R to exchange information regarding their interleaving and deinterleaving requirements and capabilities.

4. **Mazzoni Supplies Any Disclosure Missing from G.993.1 and Voith**

621. To the extent that any limitations of claim 19 of the '473 patent are not disclosed by G.993.1 and Voith, it is my opinion that they are supplied by Mazzoni.

622. With respect to limitation 19[e], Mazzoni provides additional description on how memory is allocated between an interleaving function and a deinterleaving function. For example, Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I' and M')." *Id.* at col. 5:24-31. When combined with the disclosure of Voith and G.993.1, this discloses a

means of allocating the memory between the interleaving function and the deinterleaving function.

623. With respect to limitation 19[f], Mazzoni discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message. Mazzoni discloses a memory that can be shared between the interleaving and deinterleaving means. Mazzoni, col. 1:59-65 (“These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).”); col. 2:57-50 (“The memory may be a random access memory, such as a dual-port memory, for example. The interleaving means and the deinterleaving means may respective include first addressing means and second addressing means.”). One of ordinary skill in the art would have understood that the interleaving means and the deinterleaving means would operate at the same time and that a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

5. **Motivation to Combine Mazzoni with Voith and G.993.1.**

624. I explain above at Section IX.G.3, which I incorporate by reference, that one of ordinary skill in the art would have been motivated to combine Voith and G.993.1. Additionally, one of ordinary skill in the art would have been motivated to combine the teachings of Mazzoni with both of Voith and G.993.1.

625. Like Voith and G.993.1, Mazzoni is in the DSL field, and it describes a need to allocate memory for interleaving and deinterleaving. *See, e.g.*, Mazzoni, col. 1:8-15; col. 1:54-65. Mazzoni, like Voith and G.993.1, thus addresses the problem purportedly addressed by the

'473 patent – the allocation of memory for interleaving and deinterleaving to support different applications. *See, e.g.*, '473 patent, col. 1:37-45; col. 1:48-60.

626. Further, Voith discloses that efficiency in the use of memory is desirable. *See, e.g.*, Voith at col. 1:44-47; col. 2:26-35. Mazzoni, meanwhile, discloses that an adaptable architecture is advantageous, and that optimizing the size of memory is advantageous. *See, e.g.*, Mazzoni at 1:54-65. Mazzoni further discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See, e.g.*, Mazzoni at col. 6:51-61. One of ordinary skill would have recognized the inherent limitations of Mazzoni's table, namely that all services would need to be identified ahead of time so that the table could be created and stored in the transceiver.

627. As discussed above, G.993.1 discloses how memory is allocated in accordance with a message received during initialization. One of ordinary skill in the art would therefore have recognized that the teachings of G.993.1 show a reliable and efficient way of enabling the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the possible services to be defined in advance to create the table disclosed in Mazzoni. Instead, by exchanging information about their available memory, using messaging like that disclosed in G.993.1, the transceivers of Mazzoni would determine an appropriate allocation of the available memory to the interleaver and deinterleaver.

628. Thus, in my opinion that one of ordinary skill in the time of the invention would have been motivated to combine the teachings of Mazzoni with the teachings of Voith and G.993.1.

X. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

629. I understand that TQ Delta and its experts may present evidence relating to secondary considerations of non-obviousness, for example, while contending that the references

described above in my report do not render obvious the asserted claims of the Family 3 patents. I have reviewed TQ Delta's Supplemental Responses to Defendants' Joint Interrogatory Nos. 4, 8, and 12, which inquire about secondary considerations of non-obviousness.

630. If TQ Delta should present evidence regarding secondary considerations of non-obviousness in support of the non-obviousness of the Family 3 patents, whether in its responsive expert reports, or at a later date, I reserve the right to address this evidence in my reply report, or any supplemental reports thereafter.

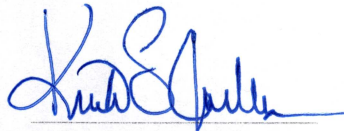
XI. CONCLUSION

631. In my opinion, based on my review of the Family 3 patents, the materials referenced herein, and my knowledge of what a person of ordinary skill in the art would have known at and before each of the Family 3 patents' priority dates about the technology at issue, a person of ordinary skill in the art would have understood all of the claim elements and limitations of claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent to be obvious over (a) LB-031; (b) LB-031 in combination with Mazzoni; (c) Fadavi-Ardekani in combination with G.993.1; and (d) Fadavi-Ardekani in combination with G.992.2. It is also my opinion that a person of ordinary skill in the art would have understood all of the claim elements and limitations of claim 19 of the '473 patent to be obvious over (a) Voith in combination with LB-031; (b) Mazzoni in combination with G.993.1; and (c) Voith in combination with G.993.1, or in the alternative, Voith in combination with G.993.1 and Mazzoni. I further opine that the asserted claims are invalid for indefiniteness, lack of enablement, and lack of written description as I explain above.

632. I reserve the right to supplement my opinions in the future to respond to any arguments or positions that TQ Delta or its experts may raise, taking account of new information as it becomes available to me.

Executed in Campbell, CA.

Date: November 28, 2018



Krista S. Jacobsen

APPENDIX A

Krista S. Jacobsen

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Experience

JACOBSEN IP LAW, Campbell, CA (February 2014 - present)

Attorney and Counselor at Law. Solo practitioner providing expert consultant, expert witness, patent litigation support, patent prosecution, and intellectual property (IP) counseling services.

SANTA CLARA UNIVERSITY SCHOOL OF LAW, Santa Clara, CA (January 2015 - present)

Lecturer in Law. Co-teaching Pretrial Litigation Techniques (Fall 2015, Fall 2016, Fall 2017, Fall 2018) and Law Practice Management (Spring 2015, Spring 2016, Spring 2017, Spring 2018).

DISRUPTIVE FORCE LLC, Campbell, CA (February 2015 - present)

Co-founder and CEO.

HEADWATER PARTNERS, Redwood Shores, CA (July 2011 - February 2014)

Head Counsel. Responsibilities included general counsel duties and patent prosecution.

COVINGTON & BURLING, LLP, Redwood Shores, CA (October 2009 - July 2011)

Associate. IP litigation.

HELLER EHRMAN, Menlo Park, CA (May-July 2008)

Summer Associate. IP litigation. Researched and drafted legal memoranda and briefs.

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, Sunnyvale, CA (June-August 2007)

Summer Associate. Patent prosecution. Composed responses to United States Patent and Trademark Office office actions and wrote portions of patent applications, including claims.

CONSULTANT (July 2004 - September 2007)

Responsibilities included assisting clients to determine and execute digital subscriber line (DSL) standardization and product strategies, writing simulations, generating and presenting technical tutorials, drafting and prosecuting patent applications, and helping with other patent issues. Clients included 2Wire, Inc., PMC-Sierra, Atheros Communications, and Beyer Law Group.

TEXAS INSTRUMENTS (TI) (formerly AMATI COMMUNICATIONS), San Jose, CA (January 1994 - May 2004).

Lead xDSL Standards Strategist (2001-04)

- Led TI's DSL standardization efforts, managed standards resources and budget, and communicated standards progress and status within TI.
- Developed and presented dozens of technical proposals for regional and international standards organizations, including ETSI TM6, ITU-T SG15/Q4, T1E1.4, and IEEE 802.3ah (Ethernet in the first mile).
- Wrote DSL white papers, technical reports, technical book chapters, and articles for external publications.
- Participated as a member of business unit patent committee and worked with TI legal department to ensure protection of intellectual property and to provide technical assistance.
- Wrote and ran DSL system simulations.
- Made presentations at industry conferences and events.

Previous roles with Amati/TI were *Project Manager, ADSL over ISDN* (2000-01), *Project Manager, VDSL* (1999-2000), *Senior Staff Engineer* (1998-99), *Staff Engineer* (1997-98), *Senior Systems Engineer* (1996-97), *Consultant* (1994-96).

ViTEL COMMUNICATIONS CORPORATION, Santa Clara, CA (August 1991 - May 1992).

Member of telecommunications group. Worked on a team that developed a video telephony transceiver.

Bar Memberships and Registrations

STATE BAR OF CALIFORNIA

Member No. 267868 (admitted December 7, 2009)

COLORADO STATE BAR

Registration No. 43,294 (admitted May 24, 2011 (currently inactive))

UNITED STATES PATENT AND TRADEMARK OFFICE

Registration No. 59,374 (registered October 11, 2006)

Krista S. Jacobsen

Education

SANTA CLARA UNIVERSITY SCHOOL OF LAW (Santa Clara, CA)

JD (*magna cum laude*), 2009

Honors and Awards

Santa Clara University School of Law Intellectual Property (IP) Fellowship (2006-09)

Dean's List (2006-09)

Order of the Coif (2009)

ABA-BNA Award for Excellence In the Study of Intellectual Property Law (Spring 2008)

CALI Award for Excellence In: Managing Complex IP Litigation (Fall 2008), IP Litigation Techniques (Spring 2008), Patent Prosecution (Spring 2008), Protection of IP (Spring 2008), Advocacy (Fall 2007), Contracts (Spring 2007)

Witkin Award for Excellence In: Opening Statements and Closing Arguments (Fall 2008), Pretrial Litigation Techniques (Fall 2008), Mass Communication (Fall 2007), Property (Spring 2007), Legal Analysis, Research and Writing, Section H (Spring 2007)

Grand Prize, First Annual San Francisco Intellectual Property Law Association Student Writing Competition (February 2009)

Selected to represent Santa Clara University in the Dean Jerome Prince Memorial Evidence Moot Court Competition (Spring 2009) and Constance Baker Motley National Moot Court Competition in Constitutional Law (Spring 2008)

Activities

Co-President, Santa Clara University Student Intellectual Property Law Association (2008-09)

Vice President, Alumni Relations, Santa Clara University Intellectual Property Association (2007-08)

Associate, Santa Clara Computer and High Tech Law Journal (2007-08)

STANFORD UNIVERSITY (Stanford, CA)

Ph.D. in electrical engineering, 1996

Dissertation: *Discrete Multi-Tone-Based Communications in the Reverse Channel of Hybrid Fiber-Coax Networks*

Adviser: John M. Cioffi (<http://www.stanford.edu/group/cioffi>)

MSEE, 1993

Digital communications specialization

Honors and Awards

IBM Graduate Fellowship (1994-95)

National Science Foundation Graduate Fellowship (1991-94)

IEEE Communications Society Scholarship (1993)

UNIVERSITY OF DENVER (Denver, CO)

BSEE (*summa cum laude*), 1991

Communications specialization

Honors and Awards

Winner, Denver Section IEEE Student Paper Contest (1991)

University of Denver Pioneer Award (1991)

University of Denver Distinguished Senior Woman Award (1990)

Phi Beta Kappa (1988)

University of Denver Honors Scholarship (1986-91)

Colorado Scholars Scholarship (1987-91)

Publications

LAW REVIEW AND JOURNAL PAPERS

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Krista S. Jacobsen

TECHNICAL BOOKS

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Cable Modems: Current Technologies and Applications (John Fijoleck, Michelle Kuska, Venkata C. Majeti, and Kotikalapudi Sriram, eds., IEEE Press, 1999): Co-author of Part II, section 3, entitled “Synchronized Discrete Multitone Modulation for Upstream Transmission on Cable Networks.”

Author of the definition of “broadband communication” in *World Book Encyclopedia* (2003).

TECHNICAL JOURNAL PAPERS AND MAGAZINE ARTICLES

K.S. Jacobsen. “Patents and Standardization, Part 3: Commitments to License Standard-Essential Patents Under Reasonable and Non-Discriminatory (RAND) Terms.” *IEEE Communications Magazine - Communications Standards Supplement*, September 2016, pp. 66-71.

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J.M. Cioffi *et al.* “Very-high-speed Digital Subscriber Lines.” In *IEEE Communications Magazine*, vol. 37, no. 4, April 1999, pp. 72-79.

TECHNICAL CONFERENCE PAPERS

K.S. Jacobsen. “Design and Performance of Synchronized DMT (SDMT) Modems for VDSL.” In *ICCE Conference Record*, Los Angeles, CA, June 1999.

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K.S. Jacobsen and J.M. Cioffi. “Achievable Throughput of Multicarrier-based Multipoint-to-point Networks Using a Reservation-based Channel Access Protocol.” In *Globecom '96 Conference Record*, London, U.K., November 1996.

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Krista S. Jacobsen

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K.S. Jacobsen and J.M. Cioffi. "High-performance Multimedia Transmission on the Cable Television Network." In *Proceedings 1994 International Conference on Communications*, New Orleans, LA, May 1994.

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K.S. Jacobsen, M.D. Agah, and B.R. Wiese. "Method to mitigate effects of ISDN off/on transitions in ADSL." U.S. patent number 7,184,467. February 2007.

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J.A.C. Bingham and K.S. Jacobsen. "Methods for coordinating upstream discrete multi-tone data transmissions." U.S. patent number 5,644,573. July 1997.

Prior Testimony

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Provided fact witness deposition testimony.

TQ DELTA, LLC v. 2WIRE, INC. (D. DEL., CASE NO.: 13-CV-1835-RGA)
Provided testimony at Markman hearing on behalf of defendant 2Wire.

IN RE MARRIAGE OF PRINCE (SUP. CT. CAL., COUNTY OF SANTA CLARA, CASE NO.: 2012-1-FL-163041)
Provided deposition and trial testimony on behalf of Petitioner, Jeffrey Prince.