UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

COMMSCOPE, INC.
Petitioner

v.

TQ DELTA, LLC
Patent Owner

U.S. Patent No. 7,836,381
Issue Date: November 16, 2010
Title: Computer Readable Medium With Instructions For Resource Sharing In A Telecommunications Environment

Case No. IPR2023-00066

PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,836,381

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Ex. 1010	Kernighan	B.W. Kernighan, D. M. Ritchie, *The C Programming Language*, 1998
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I. INTRODUCTION

Pursuant to 35 U.S.C. § 311 and 37 C.F.R. § 42.100 *et seq*., CommScope, Inc. ("CommScope" or "Petitioner") petitions the Board to institute inter partes review of claims 1, 2, 3, 4, 5, 6, 7 and 8 ("the Challenged Claims") of U.S. Patent No. 7,836,381 ("the '381 Patent," Ex. 1001) owned by TQ Delta, LLC ("TQ Delta" or "Patent Owner"). Petitioner's request is supported by the Declaration of Dr. Richard Wesel ("Decl.") (Ex. 1003) and other exhibits submitted herewith.

This Petition is a copycat to the Petition filed by Nokia of America Corporation in IPR2022-00665 and includes the exact same grounds. *Nokia of Am. Corp. v. TQ Delta, LLC*, IPR2022-00665, Paper 2 (PTAB Mar. 7, 2022) (the "Nokia IPR"). The Board found that the Nokia IPR presented "a compelling unpatentability challenge" and instituted trial on on October 3, 2022. *Nokia of Am. Corp. v. TQ Delta, LLC*, IPR2022-00665, Paper 10, at 7 (PTAB Oct. 3, 2022). In view of the Board's Institution Decision in the Nokia IPR, Petitioner hereby files this copycat petition with an accompanying motion for joinder.

Because (i) the Board instituted trial in the Nokia IPR, (ii) this is a copycat petition to the Nokia Petition; and (iii) CommScope will file an accompanying motion for joinder under 35 U.S.C. § 315(c), the time bar under § 315(b) does not apply to this IPR and the Board should institute trial, join CommScope to the Nokia

IPR, and permit CommScope to proceed in a "silent understudy" role in the Nokia IPR.

II. OVERVIEW OF CHALLENGES AND RELIEF REQUESTED

Pursuant to 42.22(a)(1) and 42.104(b)(1)–(2), Petitioner requests cancellation of the Challenged Claims pursuant to the grounds below. Additional support is provided in the Declaration of Dr. Richard Wesel (Ex. 1003).

Ground 1: Claims 1, 2, 3, 4, 5, 6, 7, and 8 are unpatentable under pre-AIA 35 U.S.C. § 103(a) over Mazzoni in view of VDSL1.

Ground 2: Claims 1, 2, 3, 4, 5, 6, 7, and 8 are unpatentable under pre-AIA 35 U.S.C. § 103(a) over VDSL1 in view of Fadavi-Ardekani.

III. BACKGROUND

The '381 Patent is directed to sharing a common memory and allocating that common memory between an interleaver and a deinterleaver in digital subscriber line ("DSL") technology. Ex. 1001, Abstract. The '381 Patent admits that interleaving and Reed-Solomon coding were known in the prior art but that the memory requirements were burdensome. *See id.*, 1:46-57. Accordingly, the '381 Patent explains that "an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver." *Id.*, 1:58–60.

At the time of the invention, Reed-Solomon coding was a well-known type of error control coding that protects a message against errors using additional bits or

symbols to produce a codeword that can withstand errors in the channel. Ex. 1003, ¶¶30-32. Interleaving was also a well-known type of error control, re-ordering symbols so that impairments that impact consecutively transmitted symbols, like impulsive noise bursts, will be spread out over multiple codewords after the symbols are deinterleaved. *Id.*, ¶¶33-40. Those symbols are then re-ordered back to the original order by a deinterleaver on the other end of a transmission. While each Reed-Solomon codeword is limited in the number of byte errors it can correct, interleaving the Reed-Solomon codewords allows for a long burst of errors to be spread over multiple Reed-Solomon codewords. For example, in the below figure, a sequence of interleaved Reed-Solomon coded data bytes suffers a noise burst, but, after those bytes are deinterleaved, the errored bytes are distributed across multiple codewords, and can thus be corrected. *Id.*, ¶¶35-40.

A sequence of Interleaved Reed-Solomon bytes suffers a noise burst of 14 bytes, shown as red squares.

After deinterleaving, the noisy bytes are distributed over multiple codewords so that they can be corrected.

Further, Reed-Solomon coding and interleaving on a shared memory was also a well-known concept at the time of the invention. *Id.*, ¶41. Indeed, computing

devices have long utilized common memory for at least two functions to overcome hardware constraints. *Id.*

The '381 Patent also contemplates an embodiment of the invention that relates to "configuring and initializing" the shared memory between the interleaver and deinterleaver. Ex. 1001, 1:63-64. But setting specific configurations by defining the parameters of two transceivers through an initialization process was a well-known concept at the time of the invention. Ex. 1003, ¶¶42-45. For example, for a communication link to function properly, the user transceiver and the operator transceiver must use the same parameters for the Reed-Solomon encoder/decoder pair and interleaver/deinterleaver pair. *Id.*, ¶43.

Here, the Board should institute review because there is at least a reasonable likelihood that Petitioner will prevail on at least one Challenged Claim.

A. '381 Patent Prosecution History

U.S. Patent Application No. 12/853,020 was originally filed on August 9, 2010. Ex. 1001. A Notice of Allowance was mailed on October 6, 2010, where the Examiner explained that the independent claims identify "the distinct features of specifying a maximum number of bytes available to be allocated to [a/an] [deinterleaver/interleaver] in a transmitted or received message, determining the amount of memory required by the [deinterleaver/interleaver], and then allocating the bytes of shared memory to the [deinterleaver/interleaver] wherein the bytes allocated

do not exceed the maximum number of available bytes specified in the message." *Id.* at 129-30. The Examiner explained that the "closest prior art, Fadavi- Ardekani" only "discloses sharing a memory between the interleavers and deinterleavers." *Id.*

The '381 Patent is a continuation of U.S. Patent Application 11/246,163, granted as U.S. Patent No. 7,831,890 (Ex .1024), which had all of its claims initially rejected under § 102 in view of Fadavi-Ardekani. Ex. 1025, 317-33. After canceling all rejected claims, Patent Owner presented new claims, which were allowed for the same reasons the claims of the '381 Patent were allowed. *Id.*, 74-82.

B. Priority Date

The '381 Patent claims priority to U.S. Provisional Application No. 60/618,269, filed on October 12, 2004. For purposes of this action Petitioner assumes (without determining) that the patent is entitled to a priority date of October 12, 2004. If Patent Owner disputes the prior art status of any of Petitioner's cited references, Petitioner reserves the right to challenge the priority date for the '381 Patent.

C. Prior Decisions by the District Court

The '381 Patent was previously considered by the United States District Court for the District of Delaware in *TQ Delta, LLC v. 2Wire, Inc.*, No. 13-cv-01835-RGA (D. Del.) (the "Delaware Litigation"); *TQ Delta, LLC v. Zhone Technologies, Inc.*, No. 13-cv-01836- RGA (D. Del.); *TQ Delta, LLC v. ZyXEL Communications, Inc.*,

No. 13-cv-02013- RGA (D. Del.); and *TQ Delta, LLC v. ADTRAN, Inc.*, No. 14-cv-00954-RGA (D. Del.). These four cases were consolidated into the lead case against *2Wire*.

The district court issued memoranda and orders construing multiple claim terms of the '381 Patent. Exs. 1018-21. The district court also addressed, on summary judgment, the invalidity of claim 5 of the '381 Patent as obvious in view of Mazzoni (Ex. 1005) over LB-031 (Ex. 1017), ultimately denying the motion because there was a dispute of material fact regarding the motivation to combine. Ex. 1022. Patent Owner also alleged certain references, including Fadavi-Ardekani (Ex. 1006), failed to disclose a "shared memory." The court granted Patent Owner's motion for no invalidity on this ground as a matter of law, reasoning that the Defendant failed to rebut Plaintiff's argument that Defendant had not proven inherency. *Id.* at 18.

A jury subsequently determined that LB-031 as understood by a POSA and LB-031 in combination with Mazzoni did not render claim 5 of the '381 Patent invalid as obvious. Ex. 1023. No ground on the basis of Mazzoni in view of VDSL1, or VDSL1 in view of Fadavi-Ardekani was presented to the jury.

D. Claim Construction (37 C.F.R. § 42.104(b)(3))

Claim terms are interpreted with the ordinary and customary meaning as understood by a person of ordinary skill in the art ("POSA") under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Certain terms of the '381 Patent were

construed in the Delaware Litigation. *See* Exs. 1018–21. Those claim terms are addressed in the table below. Any other terms should receive their respective plain and ordinary meaning.

Claim Term	**D. Del. Construction**
"transceiver"	"communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry"
"shared memory"	"common memory used by at least two functions, where a portion of the memory can be used by either one of the functions"
"amount of memory"	Plain meaning, i.e., that is not limited to number of bytes
"the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]"	"the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory"

1. "transceiver"

The district court improperly narrowed this term beyond what is contemplated in the specification. Relying on dictionary definitions, the district court concluded that "a POSA would understand the transmitter and receiver portions to share common circuitry or components." Ex. 1020 at 4. But, although the specification discloses sharing memory between a transmitter portion and receiver portion of a transceiver, Ex. 1001, 5:33-39—i.e., sharing common circuitry—it also discloses that "an exemplary transceiver can…allocate a first portion of shared memory 120 to a

first interleaver [] in the *transmitter* portion of the transceiver and allocate a second portion of the shared memory to a second interleaver [] in the *transmitter* portion of the transceiver," *id.*, 5:40-46. Thus, where only the transmitter portions are sharing a memory, the transmitter and receiver portions are **not** sharing a memory, i.e., do not share common circuitry. Narrowing the claim to require that the transmitter and receiver share common circuitry is inapposite to what is expressly disclosed in the specification and is thus inappropriate. *Summit 6, LLC v. Samsung Elecs. Co.*, 802 F.3d 1283, 1290 (Fed. Cir. 2015) (explaining that "[e]xtrinsic evidence may not be used to contradict claim meaning that is unambiguous in light of the intrinsic evidence" (internal quotation marks omitted)).

Petitioner therefore does not adopt the district court's construction and instead advances that the plain and ordinary meaning should control.

Irrespective, the unpatentability of the Challenged Claims in view of the grounds presented below does not turn on whether or not the transmitter and receiver portions of the claimed "transceivers" are required to share common circuitry.

2. "shared memory"

Petitioner does not adopt the narrow construction set forth by the district court and believes the claim term "shared memory" should be given its plain and ordinary meaning. Nowhere in the specification is a shared memory so narrowly defined, and it is improper to import such language from the specification into the claims.

SuperGuide Corp. v. DirecTV Enters., 358 F.3d 870, 875 (Fed. Cir. 2004). Nonetheless, the unpatentability of the Challenged Claims in view of the grounds below does not turn on whether the shared memory must include a portion of the memory that can be used by either one of the functions.

3. "amount of memory"

Petitioner does not adopt the construction set forth by the district court and believes the claim term should be given its plain meaning without limitation. Regardless, the unpatentability of the Challenged Claims in view of the grounds presented below does not turn on this construction.

4. "the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]"

For purposes of this petition, Petitioner adopts the district court's construction as recited *supra*.

IV. PRIOR ART REFERENCES

A. U.S. Patent No. 7,269,208 ("Mazzoni")

Mazzoni, which issued on September 11, 2007, derives from U.S. Patent Application No. 10/088,387, which was filed on July 11, 2001, and published as US2003/0021338 on January 30, 2003. Mazzoni thus qualifies as prior art under at least pre-AIA 35 U.S.C. § 102(e).

B. ETSI TS 101 270-2 Very High Speed Digital Subscriber Line ("VDSL1")

VDSL1 is technical specification ETSI TS 101 270-2 related to "Very High Speed Digital Subscriber Line (VDSL)" (hereinafter "VDSL1"). Ex. 1033. This technical specification was published online by ETSI on July 24, 2003. Dr. Hall-Ellis located VDSL1 at http://www.etsi.org, the website for the European Telecommunications Standards Institute (ETSI). *Id.*, ¶¶24-31. She confirmed that VDSL1 was cataloged and indexed and, thus, accessible by July 24, 2003. *Id.* She further states that a POSA would have located this document using reasonable diligence, either through common search terms or using the search engine on the ETSI website. *Id.* at 27–29. Dr. Wesel likewise states that a POSA would have looked to ETSI for a technical specification on VDSL. Ex. 1003, ¶18. Moreover, the Federal Circuit has previously confirmed that ETSI standards are publicly accessible. *See Kyocera Wireless Corp. v. ITC*, 545 F.3d 1340, 1350-51 (Fed. Cir. 2008). Thus, VDSL1 is prior art under at least pre-AIA 35 U.S.C. § 102(b).

C. U.S. Patent No. 6,707,822 ("Fadavi-Ardekani")

Fadavi-Ardekani was filed on January 7, 2000 and issued as a U.S. Patent on March 16, 2004. Fadavi-Ardekani is prior art under at least pre-AIA 35 U.S.C. § 102(a) and (e).

V. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSA") pertinent to the '381 Patent would have had at least a Bachelor's degree in electrical engineering, or a related field, and at least 6-7 years of experience in telecommunications or related field; a

master's degree in electrical or computer engineering, or the equivalent, and at least 3-4 years of experience in telecommunications or related field; or a Ph.D. in electrical or computer engineering, or the equivalent, with at least 1-2 years of experience in telecommunications or related field. Ex. 1003, ¶16. Additional experience may compensate for less education. *Id.*

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

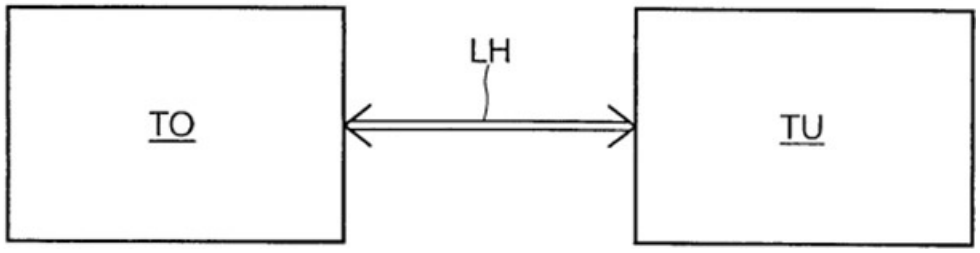
A. Ground 1: Claims 1-8 are Unpatentable Under 35 U.S.C. § 103 over Mazzoni in view of VDSL1

1. Overview of Ground 1

i. Mazzoni

Mazzoni teaches a transceiver in a VDSL environment that can send and receive digital data and that can determine the shared memory capacity used to interleave and deinterleave that data. Ex. 1005, 1:10-15. As shown in Figure 1 below, Mazzoni contemplates two send/receive devices (i.e., transceivers), TU and TO, that communicate by "a very high bit rate communication line LH." *Id.*, 1:60-61.

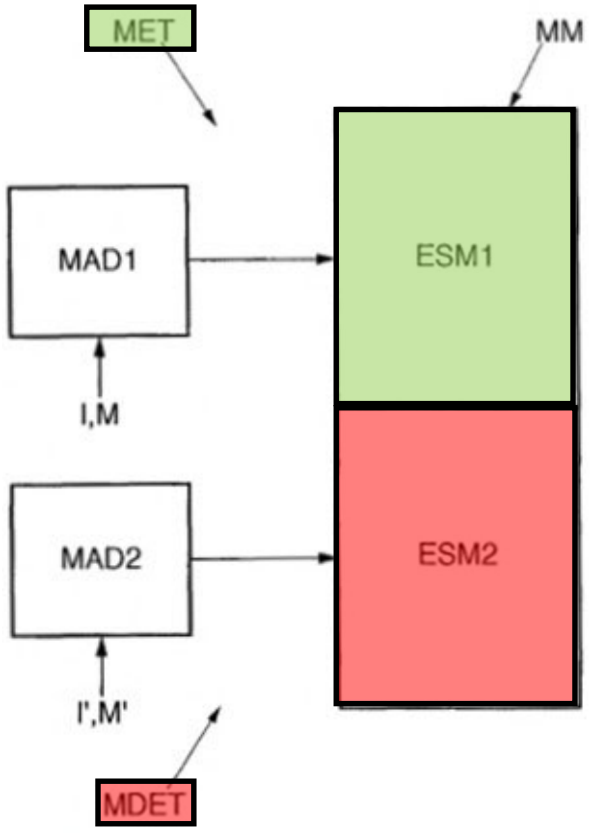
FIG.1



Id., Fig. 1.

Mazzoni further discloses a shared memory "MM" that resides in each transceiver, and that "can be shared between the interleaving means and the deinterleaving means." *Id.*, 1:59-65; 6:6-8. For example, annotated Figure 6 of Mazzoni, shown below, illustrates how the common memory, MM, is allocated to the interleaver (MET) as ESM1 (green, below) and deinterleaver (MDET) as ESM2 (red, below) on just one of the transceivers TO or TU.

FIG.6



Id., Fig. 6.

Mazzoni teaches how to determine the required memory allocations for the interleaver and deinterleaver (i.e., the memory size of ESM1 and ESM2) via triangular implementation of convolutional interleaving and deinterleaving.

Mazzoni further teaches using Reed-Solomon coding coupled to an interleaver to protect transmitted data. *Id.*, 2:25-30.

Thus, starting with downstream and upstream bit rates between the TO and TU that are disturbed by an impulsive noise, Mazzoni discloses calculating the number of data bits that are affected by an impulsive noise, the resultant errored bytes, the

number of Reed-Solomon codewords needed to correct those errored bytes, and the required interleaver or deinterleaver memory to hold those bytes. *Id.*, 6:11-36.

Relying on those calculations, Mazzoni also discloses determining the amount of memory required by the interleaver/deinterleaver to interleave/deinterleave the Reed Solomon coded data bytes using parameters I and M. *Id.*, 6:37-38. Mazzoni explains that parameters I and M can be applied to the equation I×(I−1)×M/2 to calculate "the size of the first memory space [ESM1]" for the interleaver, and parameters I' and M' can then be applied to the equation I'×(I'−1)×M'/2 to calculate "the size of the second memory space ESM2" for the deinterleaver. *Id.*, 6:38-44. Mazzoni explains that the common memory required (MM) is the sum of ESM1 and ESM2.

ii. VDSL1

VDSL1 is the technical specification for very high speed digital subscriber line transceivers put forth by ETSI. VDSL1 teaches incorporating VDSL onto transceivers VTU-O and VTU-R, and then determining the memory allocation for the interleaver and deinterleaver on each transceiver via triangular implementation of convolutional interleaving and deinterleaving. Ex. 1007, 13, 59-60.

Specifically, VDSL1 teaches that "[i]nterleaving shall be used to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords." *Id.*, 59. To determine the memory required to interleave or

deinterleave those bytes, VDSL1 teaches parameters I and M, which can be used to determine the "(De)interleaver memory size" with the equation MxIx(I–1)/2 (see Table 19 below). *Id.*, 60.

Table 19: Characteristics of triangular, convolutional interleaver

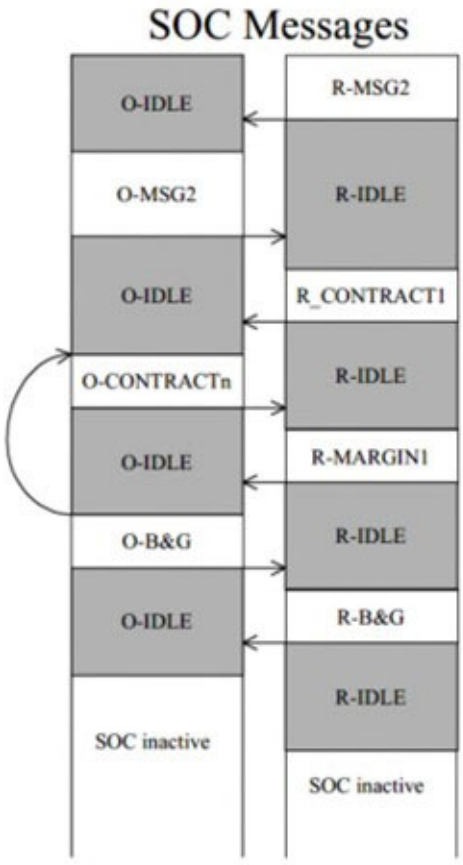
Parameter	Value
Interleaver block length	I octets (I must divide N)
Interleaving depth *D*	M x I + 1 octets
(De)interleaver memory size	M x I x (I–1)/2 octets
End-to-end delay	M x I x (I–1) octets
Correction capability	⌊t/q⌋ x M x (I+1) octets

VDSL1 then contemplates various "Interleaver Characteristics" in Table 27, including "Interleaver Memory Size," "Erasure Correction (E)," and "End-to-End Delay (DL)." *Id.*, 72.

Table 27: Interleaver Characteristics

Parameter	Value	Notes
Block Length (I)	$I = N/8$, $N/4$ or $N/2$, octets	$N = PS+19$, octets
Depth (D)	$D = M \times I + 1$, octets	$M = 0 \rightarrow 64$, programmable
Erasure Correction (E)	$E = \lfloor t \times I / N \rfloor \times (M \times I + 1)$, octets	$t = 8$ (RS error correction ability)
End-to-End Delay (DL)	$DL = M \times I \times (I - 1)$, octets	
Interleaver Memory Size	$MEM = M \times I \times (I - 1) / 2$, octets	
NOTE 1: The interleaver erasure correction *E* defines the maximum number of corrupted sequential octets could be corrected by RS algorithm when interleaving is applied. Correspondingly, the duration of noise pulses the system is protected from could be calculated as $E \times 8/R$, where R is the bit rate of the transmit signal over the line.		
NOTE 2: The ⌊ ⌋ symbols indicates the truncation of the value to the lower integer.		

VDSL1 also teaches initialization protocols between the VTU-O and VTU-R to set those I and M parameters, including the messages shown below. *Id.*, 127.



The first message, R-MSG2, describes the VTU-R's capabilities, including the maximal number of bytes available to be allocated to an interleaver. *Id.*, 132.

After the messages R-MSG2, O-MSG2, and R-CONTRACT1, the message O-CONTRACTn, contains a proposed upstream contract and a proposed downstream contract, including contract descriptors for each contract, including the parameters I and M for the upstream interleaver/deinterleaver and a distinct set of parameters I and M for the downstream deinterleaver/interleaver. *Id.*, 129.

iii. Motivation to Combine

Both Mazzoni and VDSL1 are directed to VDSL systems. Indeed, Mazzoni contemplates a transceiver for sending/receiving digital data, "*in particular in a VDSL environment*," Ex. 1005, and VDSL1 is the technical specification put forth by ETSI that "specifies requirements for transceivers that provide very high bit-rate digital transmission," i.e., VDSL, Ex. 1007, 9.

As explained *supra*, Mazzoni teaches a VDSL transceiver with a shared memory that determines an amount of memory required by an interleaver/deinterleaver to interleave/deinterleave Reed Solomon coded data bytes, that allocates those bytes of the shared memory to the interleaver/deinterleaver at a particular data rate, and that subsequently interleaves/deinterleaves those bytes.

Mazzoni does not, however, expressly disclose transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver or deinterleaver. A POSA would have understood that a transceiver as contemplated in Mazzoni, especially one implemented in a VDSL environment, would perform initialization protocols. Ex. 1003, ¶77. Thus, a POSA would have been motivated to look to the VDSL technical specifications available around the same time for those initialization protocols—here, the VDSL1 technical specification. *Id.*

VDSL1 disclosed initialization. Ex. 1007, 111 (disclosing "Initialisation" protocols for the transceiver pair VTU-O and VTU-R, including an "[e]xchange of

parameters"); *id.*, 127-34 (Disclosing a "channel analysis and exchange" state, which discloses the negotiation of interleaver/deinterleaver parameters, including R- MSG2, which specifies a maximum number of bytes of memory available to be allocated to an interleaver, and O-CONTRACTn, which describes the specific parameters I and M for each interleaver/deinterleaver pair. Once the O- CONTRACTn message is confirmed, these parameters indicate the agreed-upon memory allocation between interleaving and deinterleaving in the context of the triangular implementation of interleaving taught by VDSL1.).

A POSA thus would have been motivated to combine the initialization protocols of VDSL1 with the transceivers disclosed by Mazzoni using the parameter exchange protocol of the VDSL1 technical specification so as to perform initialization in a VDSL environment. Ex. 1003, ¶79. This simple incorporation would have achieved the known benefits of allowing the TO and TU transceivers of Mazzoni to communicate hardware capabilities and negotiate selection of parameters, thus allowing for increased flexibility in parameter selection and confirmation that the hardware is compatible with the executed parameters (e.g., that memory MM has enough storage capacity for the determined interleaver and deinterleaver size). *See, e.g.*, Ex. 1007, 111; Ex. 1003, ¶79.

There are several reasons to combine Mazzoni and VDSL1. First, Mazzoni expressly instructs that the invention "may advantageously be applied to a very high

rate digital subscriber line (VDSL) environment or system." Ex. 1005, 1:19-21. Thus, the POSA would have been motivated to combine Mazzoni's transceiver with a reference that provided the relevant implementation details that would have allowed it to operate in a VDSL environment—the technical specification. At the relevant time, a POSA looking to build a functioning transceiver that operated in a VDSL environment would have sought to comply with the VDSL1 technical specification. Ex. 1003, ¶80.

Second, the POSA would have understood that a VDSL transceiver would have had to perform initialization for the purposes of exchanging relevant information between the office transceiver and the remote transceiver. Ex. 1003, ¶81. For example, VDSL1 explains that one of the initialization tasks between the office and remote transceiver is defining "a common mode of operation," without which the office and remote transceivers would not be able to properly function. Ex. 1007, 111. As a result, the POSA would have been motivated to refer to the standard so as to follow the common and required mechanism for sharing such information between the office and remote. Ex. 1003, ¶81. Indeed, both Mazzoni and VDSL1 disclose additional requirements that would have been established during initialization, including impulse noise requirements, *compare* Ex. 1005, 6:11-18, *with* Ex. 1007, 71, latency requirements, *compare* Ex. 1005, 2:54-56, *with* Ex. 1007, 59,

and bit error rate requirements, *compare* Ex. 1005, 4:53-56, *with* Ex. 1007, 72. Third, the disclosure of Mazzoni explicitly suggests initialization protocols.

For example, in VDSL1, the parameters I, M, I', and M' result from the negotiation between the VTU-R and VTU-O transceivers during the "Channel analysis and exchange" phase, i.e., during initialization. Ex. 1007, 129; Ex. 1003, ¶82. Similarly, Mazzoni explains that "the parameters I, M, I', and M' can be modified, e.g., by software, and are delivered by control means MCD." Ex. 1005, 5:21-24. A POSA would have understood that initialization protocols would have preceded the delivery of M and I parameters by the MCD. Ex. 1003, ¶82. In reading Mazzoni, a POSA thus would have been motivated to look to the VDSL1 technical specification and had a reasonable expectation of success in doing so. *Id.* It is not significant that Mazzoni also discloses reading from a table of values for the parameters I, M, I', and M'. *See* Ex. 1005, 6:51-61. A POSA would have understood that initialization protocols could instruct which I, M, I', and M' parameters to select from said table, which would still provide the benefits of using initialization protocols as described above. Ex. 1003, ¶82. Alternatively, a POSA would have understood that initialization protocols could substitute for such a table—which is merely one contemplated method of delivering the I and M parameters—to allow for the benefits described above. *Id*.

In addition, because both Mazzoni and VDSL1 contemplate the same implementation of interleaving and deinterleaving—triangular implementation of convolutional interleaving—a POSA would have had a reasonable expectation of success in combining the two references. *Compare* Ex. 1005, 2:49-56, with Ex. 1007, 60, 152-53; Ex. 1003 ¶83. Particularly, both Mazzoni and VDSL1 contemplate the same parameters to define the interleaver and deinterleaver—I, M, I', and M'. *Compare* Ex. 1005, 6:37-44, with Ex. 1007, 59-60, 152-53. Likewise, both explain that to determine the interleaver or deinterleaver memory size—a critical element of the challenged claims—the parameters can be applied to the equation **I×(I−1)×M/2**." *Compare* Ex. 1005, 6:38-41, *with* Ex. 1007, 60. A POSA using ordinary creativity would know to implement a memory in the transceiver of Mazzoni of a size sufficient to enable the range of parameters contemplated in VDSL1. Ex. 1003, ¶83. Indeed, Mazzoni expressly instructs a POSA that its example is simply "[a]n application of the invention to a VDSL communication system," and that "the invention is not limited to this application." Ex. 1005, 3:53-55.

For at least these reasons, in reading Mazzoni, a POSA thus would have been motivated to look to the VDSL1 standard and had a reasonable expectation of success in doing so. Ex. 1003, ¶84.

2. Claim 1

i. Claim 1: [1.pre] A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

Petitioner does not agree that the preamble in this case is limiting. The language of the preamble does not recite essential structure or steps, nor is it necessary to give life, meaning, and vitality to the claim. *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002).

"Non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor" amounts to nothing more than "language extolling...features of the claimed invention," which "does not limit the claim scope without clear reliance on those benefits or features as patentably significant." *Id.* at 809. Because the limitations of the claim make no reference to—let alone clearly rely on—these features, the language cannot be deemed limiting.

To the extent it is argued that the language "a method for allocating shared memory in a transceiver" is limiting, a "conclusion that some preamble language is limiting does not imply that other preamble language, or the entire preamble is limiting." *Cochlear Bone Anchored Sols. AB v. Oticon Med. AB*, 958 F.3d 1348, 1355 (Fed. Cir. 2020).

As explained *supra*, Petitioner does not agree with the District of Delaware's construction of shared memory, but, under either construction, Mazzoni discloses this limitation.

To the extent it is argued that the preamble is entirely limiting, Mazzoni discloses this limitation. A POSA reading Mazzoni would understand that "the method for allocating shared memory in a transceiver" described in its specification would normally be implemented as a computer program or programmable logic, which would, as a matter of course, require a non-transitory computer-readable information storage media having stored thereon instructions. Ex. 1003, ¶94. For example, Mazzoni discloses a "send/receive device (i.e., modem)" with a memory, Ex. 1005, 1:47–49, as well as cites to a reference that discloses digital signal processors, which a POSA would understand requires the limitation as claimed. Ex. 1003, ¶94; Ex. 1026 (disclosing a "complete bit-true C model of the chip," which a POSA would understand to be instructions stored on a non-transitory computer-readable storage media, that when executed cause to be performed all the methods of the transceiver); *see also* Exhibit 1027.

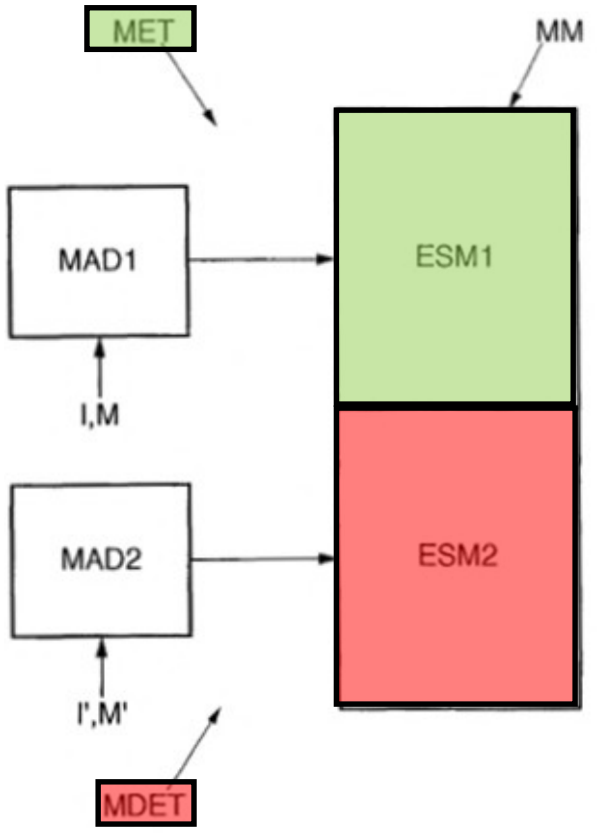
Further, Mazzoni discloses that the "memory may be a random access memory." Ex. 1005, 2:57–58. A POSA would understand memories such as Random Access Memories to be a "non-transitory computer-readable information storage media." Ex. 1003, ¶94. Mazzoni then explains that the modem "actually processe[s]" data, Ex. 1005, 1:59–65, which a POSA would understand to mean that the modem includes a processor that executes instructions stored in a memory. Ex. 1003, ¶94. Thus, Mazzoni discloses non-transitory-computer-readable information

storage media having stored thereon instructions for performing the claimed limitations in Claims 1-8 (see *infra*).

Mazzoni also discloses that when those instructions are executed by the processor, a method for allocating shared memory is performed, namely that a system with a common memory that is used by a first function (e.g., the interleaver) and a second function (e.g., the deinterleaver), where a portion of the memory (MM) can be used by either one of the functions. *See* Ex. 1003, ¶¶94-110. Specifically, Mazzoni discloses "a memory" that "**can be shared between the interleaving means and the deinterleaving means**, and whose memory allocation can be ***reconfigured*** in accordance with the bit rate actually processed by the send/receive device (modem)." Ex. 1005, 1:59–65; *see also id.*, 2:3–15.

Annotated Figure 6, shown below, illustrates how the common memory, MM, is allocated to the interleaver (MET), in green, and deinterleaver (MDET), in red.

FIG.6



Ex. 1005, Fig. 6. Mazzoni explains that, "the interleaving means and the deinterleaving means include **common memory means MM**, e.g., a dual-port random access memory." *Id.* at 5:61–64. "The memory space of the memory MM is then **divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 is assigned to the deinterleaving means MDET**." *Id.* at 5:64–67. *See also* Limitation [1.B] below, which discloses a dynamically allocable shared memory that can be used by either the interleaver or the deinterleaver.

Thus, Mazzoni discloses a common memory (e.g., MM) used by at least two functions (e.g., the interleaver and the deinterleaver), where a portion of the memory can be used by either one of the functions. Ex. 1003, ¶¶93-110.

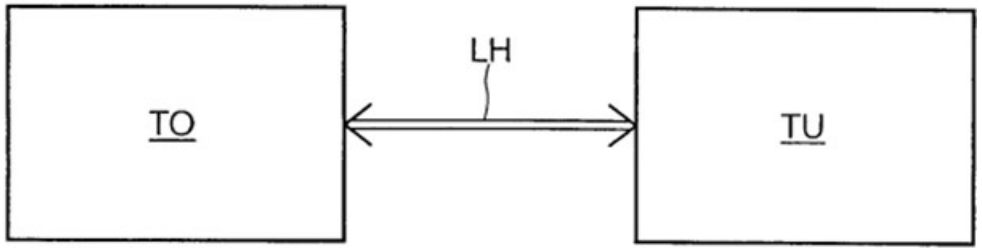
Mazzoni and VDSL1 further disclose a transceiver, as described in Limitation 1.A, *infra*.

ii. Claim 1: [1.A] transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

As explained *supra*, Petitioner does not agree with the District of Delaware's construction of transceiver, but, under either construction, Mazzoni discloses this limitation.

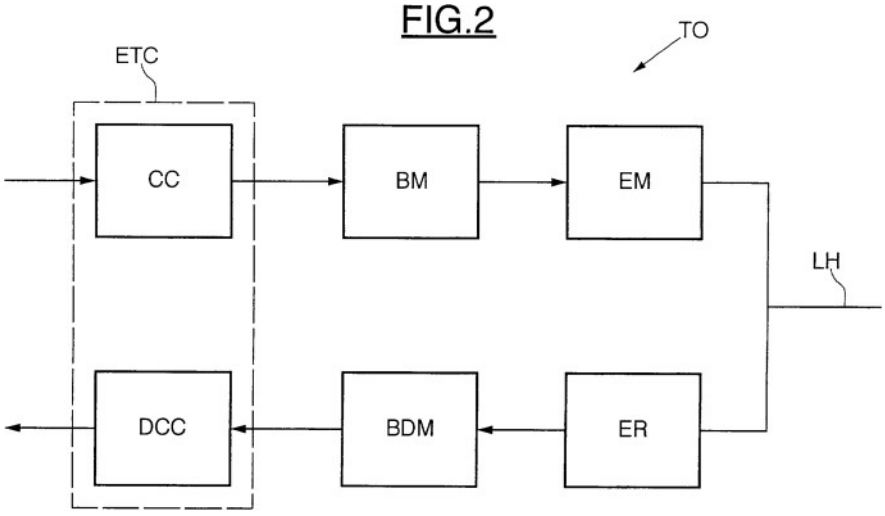
Mazzoni discloses a communication device capable of transmitting and receiving data (e.g., transceivers with "transmitters and receivers" for "sending and receiving digital data"). Ex. 1005, 1:8-15; Ex. 1003, ¶¶111-115. Specifically, as shown in Figure 1 below, Mazzoni contemplates two send/receive devices (i.e., transceivers), TU and TO, that communicate by "a very high bit rate communication line LH." Ex. 1005, 1:60-61.

FIG.1



Id., Fig. 1. As is shown in Figure 2, the terminal TO "includes a send system [i.e., transmitter] and a receive system [i.e., receiver] both connected to the transmission line LH." *Id.*, 4:30-32. Thus, the transmitter portion and receiver portion share at least some common circuitry. Ex. 1003, ¶¶112-114.

FIG.2



Mazzoni further discloses a shared memory "MM," wherein the "size of the memory MM is set by the maximum bit rate that the send/receive device can process." Ex. 1005, 6:6-8. The POSA would thus have understood the shared memory of Mazzoni is common circuitry between the "transmitters and receivers." Ex. 1003, ¶114.

Although Mazzoni does not expressly disclose that its transceiver performs transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that may be allocated to an interleaver, a POSA would have understood that, to implement the embodiments disclosed in Mazzoni, transmitting and receiving initialization messages setting parameters would have been necessary. Ex. 1003, ¶115.

To the extent it is argued that Mazzoni does not disclose this limitation, the VDSL1 standard does so explicitly. Specifically, VDSL1 discloses a message that is transmitted from the VTU-R transceiver and received by the VTU-O transceiver that specifies a maximum number of bytes of memory that are available to be allocated to an (de)interleaver at initialization. *See* Ex. 1007, 13, 132. A POSA would have been motivated to combine Mazzoni with VDSL1 for the reasons described *supra*. Ex. 1003, ¶116.

Similar to Mazzoni, VDSL1 discloses a communication device (e.g., defining "VTU" as "VDSL **Transceiver** Unit"). Ex. 1007, 13. VDSL1 also discloses that

each VTU is capable of transmitting and receiving data. For example, annotated Figure 4 shows how VTU-R transceivers (in purple) transmit and receive data to and from the VTU-O (in orange). Ex. 1007, 16.

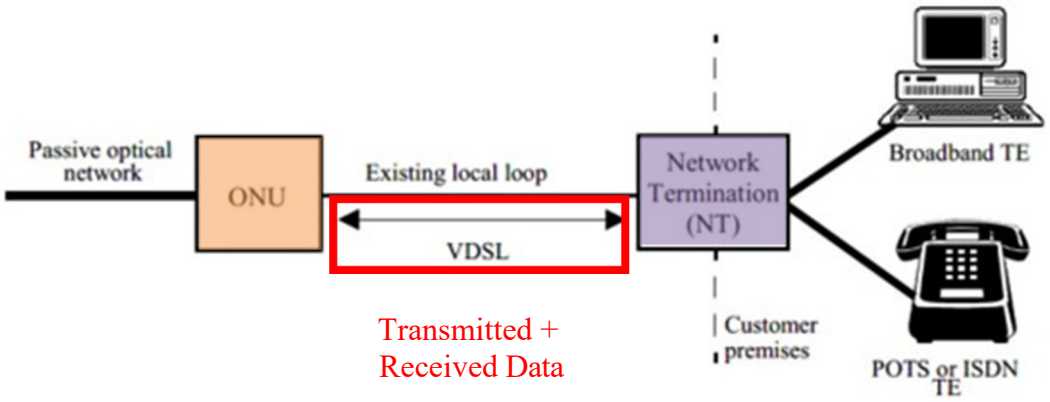
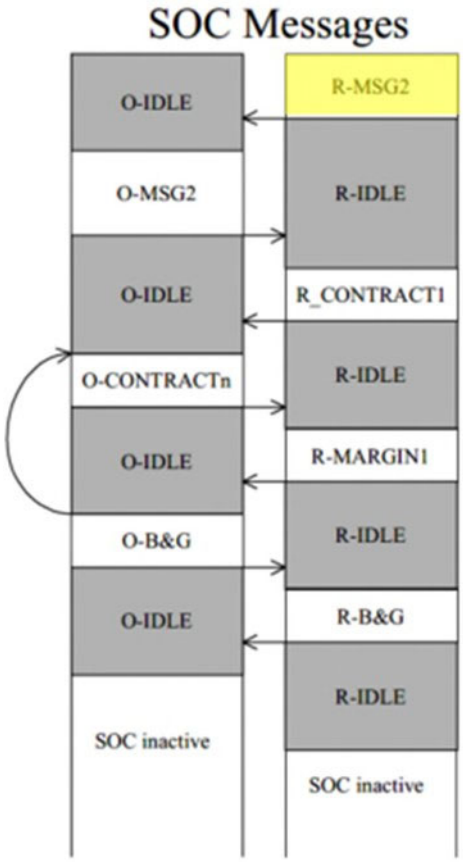


Figure 4: General fibre-to-the-node architecture for VDSL

As with Mazzoni, VDSL1 discloses that the transmitter and receiver portion of the VTU share at least some common circuitry (e.g., circuitry that provides power, circuitry that utilizes configuration messages, circuitry that controls timing, and, as in the case of the implementation disclosed by Mazzoni, circuitry of the common memory used for interleaving and deinterleaving). Ex. 1007, 20, 111; Ex. 1003, ¶118-120.

In addition to disclosing a transceiver, the VDSL1 standard discloses how each of its transceivers transmit or receive a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver in the "channel analysis and exchange state" of the "initialization

protocol." Ex. 1007, 63; Ex. 1003, ¶¶121-128. VDSL1 provides an overview of the "channel analysis and exchange state" wherein **R-MSG2** (below, highlighted) is communicated.



Ex. 1007, 77.

The VDSL1 technical specification describes the message **R-MSG2** in Table 82 as including the field "**Maximum interleaver memory**," which specifies the maximum number of bytes available to be allocated to an interleaver. *Id.*, 132; Ex.

1003, ¶125.

Table 82: Description of R-MSG2

Field	Field or macro-field type	Remark
Message descriptor	1 octet	See table 49
Maximum constellation size in upstream	1 octet	Maximum number of bits per tone
RS setting supported by VTU-R	1 octet	0x00: only mandatory settings 0xFF: all settings (see note 1)
Interleaver setting supported by VTU-R	1 octet	0x00: only mandatory settings 0xFF: all settings 0xNN: NN = number of settings (0x00 < NN < 0xFF)
Detailed interleaver setting description	0 octets if NN = 0x00 0 octets if NN = 0xFF NN x 4 octets otherwise	See table 74
Maximum power transmitted	1 octet	In units of 0,25 dBm
Maximum interleaver memory	3 octets	In octets (see note 2)
Maximum number of EOC octets per frame in upstream	1 octet	Number of EOC octets per frame
Maximum number of VOC octets per frame in upstream	1 octet	Number of VOC octets per frame
Support of express swapping	1 octet	0x00: Not supported 0xFF: Supported
j_{max}	1 octet	Maximum value of j_{max} supported by the VTU-R (see note 3)
NOTE 1: All settings means the values (for the redundancy) that are specified in clause 6.4.2. NOTE 2: The interleaver memory is computed as M×I×(I-1). NOTE 3: Specification of j_{max} = k means that all values from 0 to k are supported.		

The R-MSG2 message is one in a series of messages exchanged between the VTU-O and the VTU-R during initialization. Ex. 1007, 63; Ex. 1003, ¶¶125-127. Therefore, the combination of Mazzoni and VDSL1 discloses a transceiver (e.g., TO or TU in Mazzoni or the VDSL Transceiver Unit or VTU in VDSL1) that performs: transmitting or receiving a message (e.g., R-MSG2) during initialization (e.g., the channel analysis and exchange state) specifying a maximum number of bytes of memory that are available to be allocated to an interleaver (e.g., the parameter "Maximum interleaver memory"). Ex. 1003, ¶128-129.

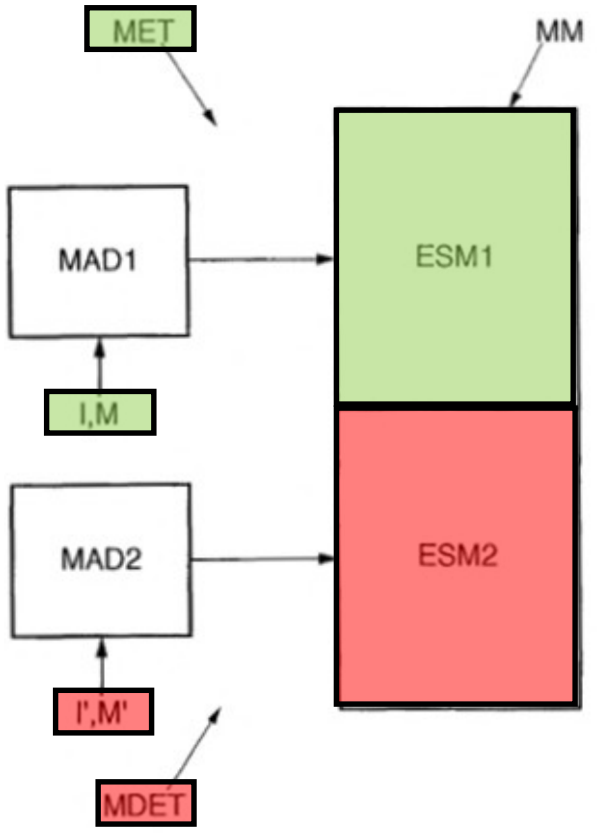
iii. Claim 1: [1.B] determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a

shared memory;

As explained *supra*, Petitioner does not agree with the District of Delaware's construction of amount of memory, but, under either construction, Mazzoni discloses this limitation.

Mazzoni discloses determining, at the transceiver (TO or TU), an amount of memory required by the interleaver (MET) in ESM1 (green, below) and the deinterleaver (MDET) in ESM2 (red, below). Ex. 1005, Fig. 6; Ex. 1003, ¶131-132. As described with respect to Limitation [1.pre], Mazzoni discloses memory shared between the interleaver and the deinterleaver.

FIG.6



Moreover, Mazzoni discloses that "Reed-Solomon coding means are associated with the interleaving means" and "[i]n conjunction with subsequent interleaving, the Reed-Solomon coding can correct bursts of errors introduced by the transmission channel." *Id.*, 4:38-41. Indeed, "Reed-Solomon coding is applied…to each of the data packets." *Id.*, 4:42-43.

Mazzoni discloses an example of determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon coded data bytes. In this example, the maximum downstream bit rate is set to 832x64 kbit/s and the

upstream bit rate is set to 32x64 kbit/s, which is "disturbed by an impulsive noise with a duration of 0.25 ms." Ex. 1005, 6:11-36.

To determine the number of Reed-Solomon coded data bytes, Mazzoni calculates the number of bits affected in the downstream by this 0.25ms impulsive noise by multiplying the transmitted bit rate (832x64 kbits/s) by the duration of the noise burst (0.25ms), resulting in 13,312 affected bits. *Id.*, 6:19-23. Next, Mazzoni determines the number of errored bytes by dividing the total number of affected bits by 8, the number of bits in a byte, resulting in 1,664 bytes. *Id.*

Mazzoni then determines the number of Reed-Solomon code words needed, explaining that that number is calculated by dividing the total errored bytes by "the correcting power of the Reed-Solomon code." *Id.*, 6:23-30. Mazzoni discloses "an RS(240,224)," which a POSA would have understood to mean a Reed-Solomon code that communicates 224 bytes of information using a 240-byte codeword, i.e., N=240, thus resulting in 16 *extra* bytes of redundancy, or a correcting power of 8. Ex. 1005, 6:11-26; Ex. 1003, ¶¶147-150. Thus, Mazzoni explains that the number of Reed-Solomon codewords needed to correct the errored bytes is the 1,664 errored bytes divided by 8, or 208 codewords. Ex. 1005, 6:23-26.

Mazzoni next determines the minimum size of memory required to hold the necessary number of RS codewords. Ex. 1005, 6:26-30; Ex. 1003, ¶¶151-163. Mazzoni explains that the "size of the memory space needed to store this maximum

bit rate is then equal to Nxnrs/2, where N is the size of the Reed-Solomon code (here 240)," and nrs is the number of RS codewords. Ex. 1005, 6:23-30. Accordingly, the resulting memory space size in the downstream is equal to 24,960 bytes. *Id.*

Applying the same methodology in the upstream, where the bit rate is 32x64, the number of bytes affected by the 0.25ms noise duration is 64 bytes (32 x 64 kbits is equal to 2,048,000 bits, multiplied by 0.25ms is 512 bits affected, and divided by 8 bits per byte is 64 bytes). Ex. 1005, 6:31-35; Ex. 1003, ¶¶151-163. The number of Reed-Solomon codewords needed to correct the errored bytes is the 64 errored bytes divided by 8, or 8 Reed-Solomon codewords. Ex. 1003, ¶¶151-163. Calculating the memory space size based on Nxnrs/2, it can be determined that the minimum required upstream memory is 960 bytes, although Mazzoni erred and calculated it to be 1,920 bytes.[1] Ex. 1003, ¶¶156, 162. Relying on Mazzoni's calculation, and

[1] Mazzoni improperly applies the equation Nxnrs/2 by failing to divide the number by 2. Ex. 1003 ¶156, 162. Such a minor error does not alter the effect of Mazzoni's disclosure, as a POSA reading Mazzoni would have understood how to modify the reference, i.e., by correcting a single math error applying the correctly disclosed equations, to determine the overall requisite memory between the upstream and downstream. *See Enplas Display Device Corp. v. Seoul Semiconductor Co.*, 909 F.3d 398, 405 (Fed. Cir. 2008); *Apple Inc v. Corephotonics, Ltd.*, 861 F. App'x 443,

adding the required memory from the downstream and the upstream, Mazzoni determines that the "minimum size of the memory MM is therefore 26,880 bytes." Ex. 1005, 6:29-30.

Finally, to determine the minimum amount of memory required by the *interleaver* to interleave a first plurality of Reed Solomon (RS) coded data bytes, Mazzoni explains that it is necessary to determine the parameters I, I', M, and M'. Ex. 1005, 6:37-38; Ex. 1003, ¶151-163. Mazzoni states that "parameters I, M, I' and M'...define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means." Ex. 1005, 5:21-27. Mazzoni explains that "**the size of the first memory space [ESM1]**...is equal to **I×(I−1)×M/2**." *Id.*, 6:38-41. Likewise, "**the size of the second memory space ESM2**...is equal to **I'×(I'−1)×M'/2**." *Id.*, 6:41-44. Mazzoni therefore explains that because **I×(I−1)×M/2** must be equal to the calculated downlink memory of 24,960 bytes, "it is possible to choose [parameters] I=40 and M=32." *Id.*, 6:45-48. Likewise, because **I'×(I'−1)×M'/2** must be at least equal to the calculated upstream memory of 1,920 bytes, "it is possible to choose [parameters] I'=24 and M'=7." *Id.* Because the required memory when I'=24 and M'=7 is 1,932 bytes, Mazzoni explains that the

450 (Fed. Cir. 2021) (explaining that modifications to fix an error in the prior art is permissible in an obviousness analysis).

common memory required (MM) is actually 26,892 bytes, with the ESM1 memory being equal to 24,960 bytes and the ESM2 memory being equal to 1,932 bytes. *Id*.

Mazzoni further teaches (de)interleaving Reed Solomon (RS) coded data bytes, Ex. 1005, 2:25-36 ("To make the Reed-Solomon coding more efficient, the coding means may be coupled to the interleaving means" wherein the "interleaving means may then interleave the [Reed-Solomon coded] bytes temporally by modifying the order in which they are transmitted"); *id.*, 5:7-8 (explaining that the embodiment "includes deinterleaving and Reed-Solomon decoding means"), and, as described with respect to Limitation [1.A], does so within a shared memory MM. Ex. 1003, ¶154.

Thus, Mazzoni explicitly discloses determining, at the transceiver (TO or TU), an amount of memory required by the interleaver (e.g., 24,960 bytes) to interleave a first plurality of Reed Solomon (RS) coded data bytes (e.g., at least 208 RS code words) within a shared memory (e.g., MM). *Id.*

Following the methodologies as disclosed by Mazzoni, and as described *infra* in Ground 2 Limitation [1.B], VDSL1 also discloses determining, at the transceiver (TO or TU), an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes. *Id.* ¶164.

iv. Claim1: [1.C] allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein

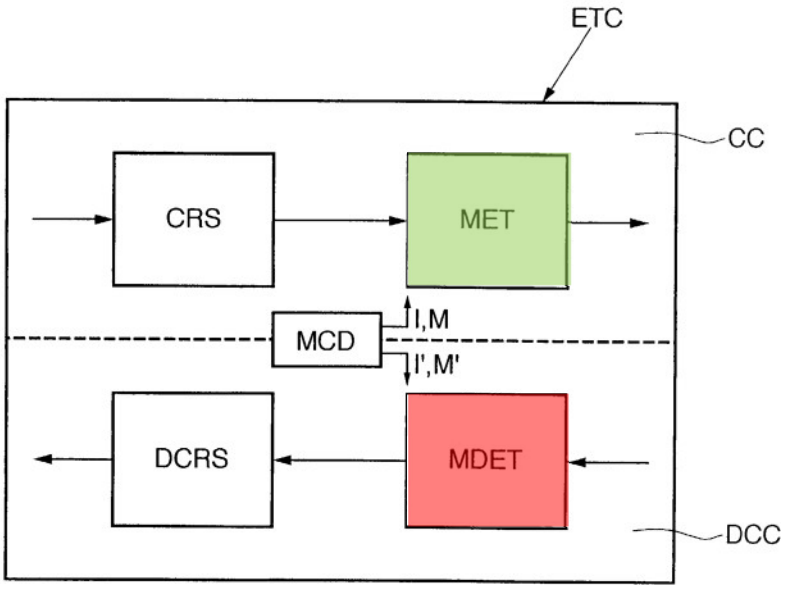
the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

The combination of Mazzoni and VDSL1 disclose this limitation for the same reasons as discussed in Limitations [1.A] and [1.B]. *See supra*. Specifically, Mazzoni discloses allocating, in the transceiver (TO or TU), a first number of bytes of the shared memory to the interleaver (in Mazzoni, as described *supra*, 24,690 bytes to ESM1 of shared memory MM) to interleave the first plurality of Reed Solomon (RS) coded data bytes (in Mazzoni, as described *supra*, at least 208 RS code words) for transmission at a first data rate (in Mazzoni, as described *supra*, 832x64 kbit/s in the downlink direction). Ex. 1003, ¶165.

In addition to *determining* an amount of memory required to interleave a first plurality of Reed-Solomon coded data bytes as described *supra*, Mazzoni discloses allocating the required amount to the interleaver. *Id.*, ¶166-181.

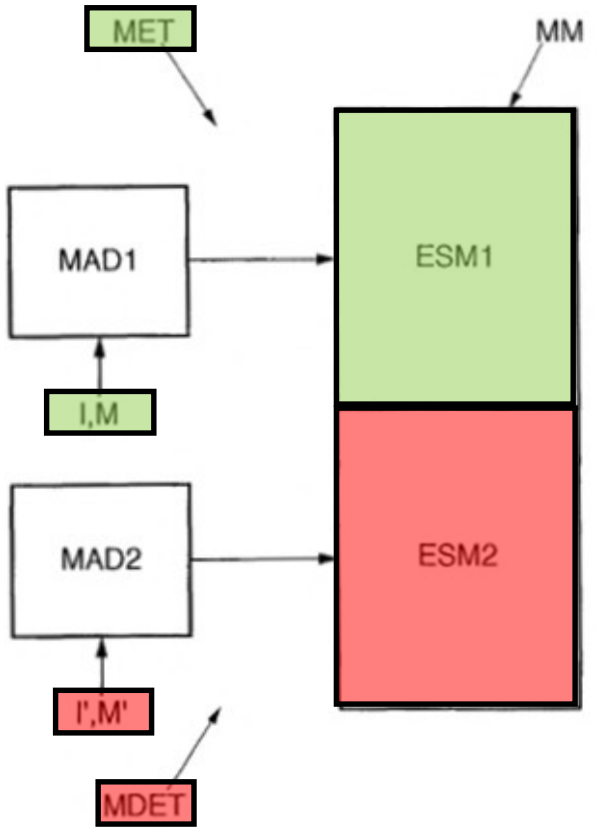
For example, Mazzoni explains that after the values of I, M, I', and M' are determined—which are the values that "define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means," Ex. 1005, 5:24-27—they are "delivered by control means MCD," *id.*, 5:21-24. As depicted in Figure 3, MCD delivers parameters I, M, I', and M' to "the interleaving means MET" and "deinterleaving means MDET." *Id.*, 5:64-67; Fig. 3.

FIG.3



As depicted in Figure 6, "memory space ESM1 [is] assigned to the interleaving means MET," and "memory space ESM2 [is] assigned to the deinterleaving means MDET." *Id.*, 5:64-67; Fig. 6.

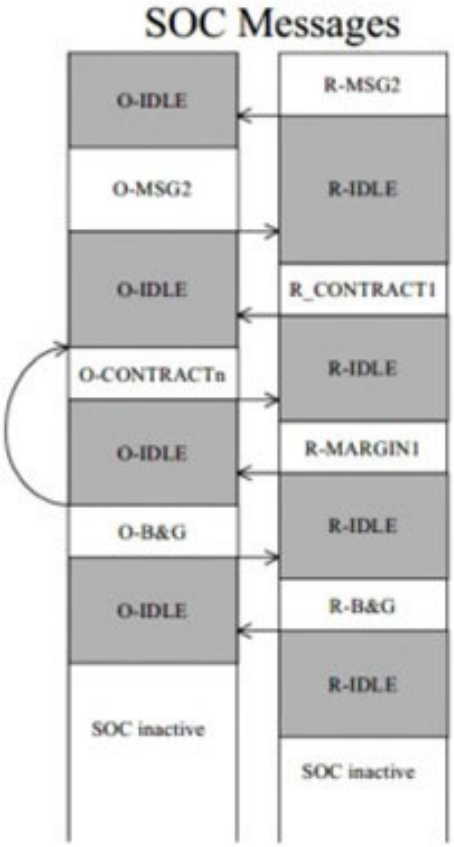
FIG.6



As to wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message, and as discussed in Limitations [1.A] and [1.B], a POSA would have understood that, to implement the embodiments disclosed in Mazzoni, transmitting and receiving initialization messages setting parameters would have been necessary. Ex. 1003, ¶172-173. Regardless, VDSL1 discloses a transceiver and a message that is transmitted from the VTU-R transceiver and received by the VTU-O transceiver that explicitly specifies a maximum number of bytes of memory that are available to be allocated to an (de)interleaver at

initialization. *See* Ex. 1007, 132; Ex. 1003, ¶174-180; *see also* [1.A] and [1.B], *supra*.

As explained *supra*, VDSL1 discloses that in the "initialization protocol," there is a "channel analysis and exchange state" whereby the modems "agree on a contract that thoroughly defines the communication link." Ex. 1007, 111; Ex. 1003, ¶¶175-176. As depicted in excerpted Figure 56, the "channel analysis and exchange state" includes a number of messages delivered between the VTU-O and VTU-R.



Ex. 1007, 127.

As explained *supra,* the VTU-R and VTU-O begin a series of negotiations to set the parameters for downstream and upstream interleaving and deinterleaving. Ex. 1003, ¶176. As depicted in Table 75, one of those messages, O-CONTRACTn, delivers a contract descriptor message for the downstream contract and upstream contract. Ex. 1007, 129; Ex. 1003, ¶177.

Table 75: Description of O-CONTRACTn

Field	Field or macro-field type
Message descriptor	Message code (1 octet)
Downstream contract	Contract Descriptor
Upstream contract	Contract Descriptor
EOC capacity	Number of EOC octets per frame (1 octet)
VOC capacity	Number of VOC octets per frame (1 octet)

As depicted in Table 76, the contract descriptor message for the downstream contract includes the parameters I and M for the interleaver (here, labeled "Interleaver setting"). Ex. 1007, 129; Ex. 1003, ¶178.

Table 76: Contract Descriptor

Field	Field or macro-field type	Remark
Rate in fast channel	2 octets	In multiple of 64 kbps
RS setting in fast channel	2 octets	b15 → b8: RS overhead b7 → b0: RS codeword length
Rate in slow channel	2 octets	In multiple of 64 kbps
RS setting in slow channel	2 octets	b15 → b8: RS overhead b7 → b0: RS codeword length
Interleaver setting	2 octets	b15 → b8: M (see note 1) b7 → b0: I
NOTE: The value *I* must be a divider of the RS codeword length.		

A POSA would have understood that the message delivered by the O-CONTRACTn message, which included the I and M parameters from which the memory will be determined, was the allocation of that memory. Ex. 1003, ¶177.

Indeed, having set the parameters I and M during initialization, VDSL1 discloses, in Table 19, that the interleaving and deinterleaving memory size may be determined, and subsequently allocated, based on the parameters I and M using equation **MxI×(I−1)/2**. Ex. 1007, 16; Ex. 1003, ¶177.

Table 19: Characteristics of triangular, convolutional interleaver

Parameter	Value
Interleaver block length	I octets (I must divide N)
Interleaving depth *D*	M x I + 1 octets
(De)interleaver memory size	M x I x (I–1)/2 octets
End-to-end delay	M x I x (I–1) octets
Correction capability	⌊t/q⌋ x M x (I+1) octets

VDSL1 further explains that the "VTU-R sends the R-MSG2 message to transfer information about its bit allocation capabilities." Ex. 1007, 127. A POSA would have understood that the upstream contract proposed by the VTU-O must comport with the limitations of the VTU-R, including the maximum interleaver memory as communicated in R-MSG2. Ex. 1003, ¶180. As such, a POSA would have understood that the O-CONTRACTn message confirms that the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the R-MSG2 message. *Id.*

The combination of Mazzoni and VDSL1 thus also discloses wherein the allocated memory for the interleaver (in VDSL1, set by message O-CONTRACTn) does not exceed the maximum number of bytes specified in the message (in VDSL1, set by message R-MSG2). Ex. 1003, ¶181.

v. Claim 1: [1.D] allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

Mazzoni discloses this limitation for the same reasons as discussed in Limitation [1.C]. Ex. 1003, ¶182. Particularly, Mazzoni discloses a "control means MCD," Ex. 1005, 5:21-24, that delivers parameters I, M, I', and M' to both "the interleaving means MET" and "*deinterleaving* means MDET," *id.*, 5:64-67; Fig. 3. Also, "memory space ESM1 [is] assigned to the interleaving means MET," and "memory space ESM2 [is] assigned to the *deinterleaving* means MDET." *Id.*, 5:64-67; Fig. 6.

Mazzoni thus discloses allocating, in the transceiver (TO or TU), a second number of bytes of the shared memory to a deinterleaver (in Mazzoni, as described *supra*, 1,932 bytes to ESM2 of shared memory MM) to deinterleave a second plurality of RS coded data bytes (in Mazzoni, as described *supra*, at least 8 RS code words) received at a second data rate (in Mazzoni, as described *supra*, 32x64 kbit/s in the uplink direction). Ex. 1003, ¶¶182-184.

vi. Claim 1: [1.E] interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

As is discussed in Limitations [1.B]-[1.D], *supra*, Mazzoni discloses interleaving the first plurality of RS coded data bytes (as described *supra*, at least RS 208 code words) within the shared memory allocated to the interleaver (as described *supra*, 24,690 bytes to ESM1 of shared memory MM) and deinterleaving the second plurality of RS coded data bytes (as described *supra*, at least 8 RS code words) within the shared memory allocated to the deinterleaver (as described *supra*, 1,932 bytes to ESM2 of shared memory MM). Ex. 1003, ¶¶183-188.

With respect to "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver," Mazzoni discloses this limitation. *Id.* As explained *supra*, Petitioner adopts the district court's construction for purposes of this petition.

Mazzoni explains that "the interleaving means and the deinterleaving means include common memory means MM, e.g., a dual-port random access memory." Ex. 1005, 5:61-65. A POSA would have understood that a dual-port random access memory has two ports that would allow the disclosed interleaver to read from or write to one port while the disclosed deinterleaver simultaneously reads from or

writes to a second port. Ex. 1003, ¶188. That is, by its disclosure of dual-port random access memory, Mazzoni discloses that the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory. *Id*.

Mazzoni further explains that memory MM is "divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 [] assigned to the deinterleaving means MDET." *Id.*, 5:64-67. By dividing the memory as disclosed, a POSA would have understood that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. Ex. 1003, ¶189. Finally, a POSA would further have understood that where there is a constant stream of data being transmitted and received, for example at 832x64 kbit/s, the deinterleaver would hold information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver holds information for interleaving in its respective allocation of the shared memory. *Id.*

Mazzoni thus additionally discloses wherein the shared memory allocated to the interleaver (e.g., ESM1) is used at the same time (e.g., via the dual-port random access memory) as the shared memory allocated to the deinterleaver (e.g., ESM2). *Id.*, ¶190.

3. Claim 2: The media of claim 1, wherein the determining is based on an impulse noise protection requirement.

The combination of Mazzoni and VDSL1 discloses claim 2. In determining the amount of interleaving or deinterleaving memory that must be allocated to an interleaver or deinterleaver, described *supra*, Mazzoni bases the determination on an impulse noise protection requirement—an impulsive noise with a duration of 0.25ms." Ex. 1005, 6:11-18; Ex. 1003, ¶192.

VDSL1 also discloses determining based on an impulse noise protection requirement. Ex. 1003, ¶¶193-195. Specifically, VDSL1 explains "[i]nterleaving improves the error-correcting power of the RS codes in the presence of impulse noise," and that the "value of interleaving depth D shall be chosen in [accordance] with the required impulse noise protection (erasure correction)." Ex. 1007, 71. VDSL1 further explains how to calculate "Erasure Correction" in Table 27 (below, highlighted) and adds that "the duration of noise pulses the system is protected from could be calculated as Ex8/R, where R is the bit rate of the transmit signal over the line." *Id.*, 72.

Table 27: Interleaver Characteristics

Parameter	Value	Notes
Block Length (I)	$I = N/8$, $N/4$ or $N/2$, octets	$N = PS+19$, octets
Depth (D)	$D = M \times I + 1$, octets	$M = 0 \rightarrow 64$, programmable
Erasure Correction (E)	$E = \lfloor t \times I / N \rfloor \times (M \times I + 1)$, octets	$t = 8$ (RS error correction ability)
End-to-End Delay (DL)	$DL = M \times I \times (I - 1)$, octets	
Interleaver Memory Size	$MEM = M \times I \times (I - 1) / 2$, octets	

NOTE 1: The interleaver erasure correction *E* defines the maximum number of corrupted sequential octets could be corrected by RS algorithm when interleaving is applied. Correspondingly, the duration of noise pulses the system is protected from could be calculated as *E×8/R*, where R is the bit rate of the transmit signal over the line.
NOTE 2: The $\lfloor \rfloor$ symbols indicates the truncation of the value to the lower integer.

Also, relying on the parameters considered in Table B.1 (below) it can be determined (see below) how the different amounts of memory are required by VDSL1 for different impulse noise, for different latencies, and for different bit rates. Ex. 1003, ¶¶195-196.

Table B.1: Interleaving depth Parameter values

Line Rate, Mb/s		1,62	3,24	6,48	12,96	25,92	51,84
Value of N/I		8					
250 µs of erasure correction	M, octets	2	4	8	16	32	64
	Delay, msec	5,9					
500 µs of erasure correction	M, octets	4	8	16	32	64	128
	Delay, msec	11,8					

Impulse noise burst time in ms	0.25 ms			0.5 ms		
Corresponding latency in ms	5.9 ms			11.8 ms		
Bit Rate in Mb/s	M	I (for N=240)	Memory (bytes)	M	I for (N=240)	Memory (bytes)
1.62 Mb/s	2	30	870	4	30	1740
3.24 Mb/s	4	30	1740	8	30	3480
6.48 Mb/s	8	30	3480	16	30	6960
12.96 Mb/s	16	30	6960	32	30	13920
25.92 Mb/s	32	30	13920	64	30	27840
51.84 Mb/s	64	30	27840	128	30	55680

4. Claim 3: The media of claim 1, wherein the determining is based on a latency requirement.

The combination of Mazzoni and VDSL1 discloses this claim. Mazzoni explains that "[l]atency is a primordial and decisive criterion for any VDSL communication system." Ex. 1005, 2:54-56; Ex. 1003, ¶197-202.

VDSL1 likewise explains that the "interleaver and de-interleaver shall be adjustable via the management system to meet latency requirements." Ex. 1007, 59.

It also explains that "[f]or data rates greater than or equal to 13 Mbps, the latency between the α and β interfaces shall not exceed 10 ms when the interleaver delay is set to the maximum." *Id.* VDSL1 further contemplates various interleaver parameters that affect the determination of the interleaver and deinterleaver memory allocation, including "End-to-end delay," i.e., latency (below,). Ex. 1007, 72. *See also* Claim 2 for calculations based on a latency requirement.

Table 27: Interleaver Characteristics

Parameter	Value	Notes
Block Length (I)	$I = N/8$, $N/4$ or $N/2$, octets	$N = PS+19$, octets
Depth (D)	$D = M \times I + 1$, octets	$M = 0 \rightarrow 64$, programmable
Erasure Correction (E)	$E = \lfloor t \times I / N \rfloor \times (M \times I + 1)$, octets	$t = 8$ (RS error correction ability)
End-to-End Delay (DL)	$DL = M \times I \times (I - 1)$, octets	
Interleaver Memory Size	$MEM = M \times I \times (I - 1) / 2$, octets	
NOTE 1: The interleaver erasure correction E defines the maximum number of corrupted sequential octets could be corrected by RS algorithm when interleaving is applied. Correspondingly, the duration of noise pulses the system is protected from could be calculated as $E \times 8/R$, where R is the bit rate of the transmit signal over the line.		
NOTE 2: The $\lfloor \rfloor$ symbols indicates the truncation of the value to the lower integer.		

5. Claim 4: The system of claim 1, wherein the determining is based on a bit error rate requirement.

The combination of Mazzoni and VDSL1 discloses this claim. Mazzoni discloses that "[e]rrors introduced by the channel, which often occur in bursts affecting several successive bytes and can therefore exceed the correction capacity of the Reed-Solomon code in isolation, may be distributed temporally," i.e., be based on a bit error rate requirement. Ex. 1005, 4:53-56; Ex. 1003, ¶203-207.

VDSL1 likewise discloses that the memory determination is based on a bit error rate requirement. Indeed, VDSL explains that bit error rate and latency are intertwined. Ex. 1007, 59 (explaining that the "latency of the slow path is a function

of the data rate and burst error correction capability" and that at "lower data rates there is a trade-off between higher latency and decreased burst error correction ability"). Thus, one is left balancing the latency requirements with bit error requirements. Ex. 1003, ¶204. *See also* Claim 2 for calculations based on a bit error requirement.

6. Claim 5

i. Claim 5: [5.pre] A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

See Limitation [1.pre].

ii. Claim 5: [5.A] transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

The combination of Mazzoni and VDSL1 discloses this limitation for the same reasons as described in Limitation [1.A]. It is not significant that claim 5 states that the message specifies a maximum number of bytes of memory allocated to a *deinterleaver* rather than an *interleaver* as in claim 1 because the claim states "transmitting or receiving." Ex. 1003, ¶209. For example, when the VTU-R *transmits* R-MSG2, which contains the "[m]aximal interleaver memory" to VTU-O, the VTU-O *receives* said message. Ex. 1007, 132. Because VTU-R was *transmitting* a message indicating the maximum interleaver memory on the VTU-R, the VTU-O was necessarily *receiving* a message indicating the maximum

deinterleaver memory on the VTU-O. Ex. 1003, ¶209. Such a result is because the deinterleaver in the upstream must necessarily have the same memory as the interleaver in the upstream, and the deinterleaver in the downstream must necessarily have the same memory as the interleaver in the downstream. *See* Ex. 1003, ¶209; *see also* Ex. 1007, 60 (disclosing calculating the "(De)interleaver memory size" using equation MxIx(I–1)/2); Ex. 1005, 8:3-5 ("Of course, everything just described here for the terminal TO applies to the terminal TU with deinterleaving means with I branches and interleaving means with I′ branches.").

iii. Claim 5: [5.B] determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

See Limitations [1.B] and [5.A].

iv. Claim 5: [5.C] allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

See Limitations [1.C] and [5.A].

v. Claim 5: [5.D] allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes [transmitted] at a second data rate; and

See Limitations [1.D] and [5.A].

vi. Claim 5: [5.E] deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the [shared] memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

See Limitations [1.E] and [5.A].

7. Claim 6: The media of claim 5, wherein the determining is based on an impulse noise protection requirement.

See claims 2 and 5.

8. Claim 7: The media of claim 5, wherein the determining is based on a latency requirement.

See claims 3 and 5.

9. Claim 8: The media of claim 5, wherein the determining is based on a bit error rate requirement.

See claims 4 and 5.

B. Ground 2: Claims 1-8 are Unpatentable Under 35 U.S.C. § 103 over VDSL1 in view of Fadavi-Ardekani

1. Overview of Ground 2

i. VDSL1

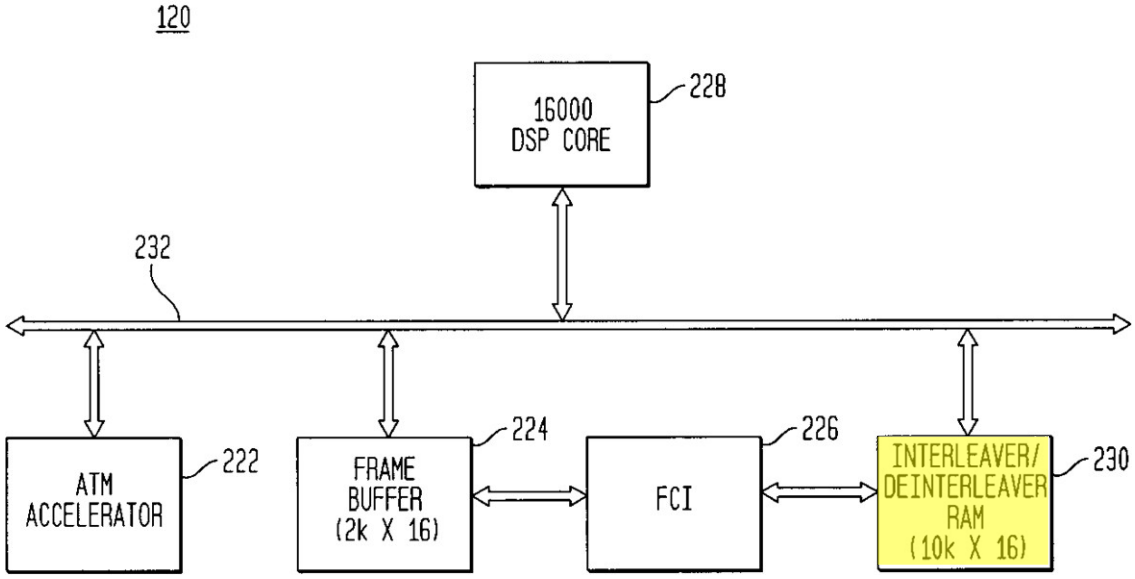
See overview of VDSL1 in Ground 1.

ii. Fadavi-Ardekani

Fadavi-Ardekani teaches a transceiver that may be implemented in a VDSL communication system with an interleaver and deinterleaver utilizing a shared memory. Ex. 1006, 4:19-21; Ex. 1003, ¶67. Fadavi-Ardekani discloses a "Framer/Coder/Interleaver" (FCI), which "performs…Reed-Solomon encoding/decoding, and interleaving/de-interleaving." *Id.*, 6:11-16. The memory that supports the FCI is the Interleave/De-Interleave Memory (IDIM), which "allow[s] beneficial performance of various interleave/de-interleave processes." *Id.*, 6:55-65.

Fadavi-Ardekani also teaches that the IDIM may be a shared memory between the interleaver and the deinterleaver. *Id.*, 6:55-58 (The "Interleave/De-Interleave Memory (IDIM)...may be utilized in a ping-pang fashion."); Ex. 1003, ¶68. Fadavi-Ardekani defines "ping-pang" to mean that "areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent" and that "[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent." *Id.*, 5:60-65. For example, Fadavi-Ardekani provides Figure 2, which identifies the interleaver and deinterleaver memory existing on a single RAM (highlighted, below).

FIG. 2



Fadavi-Ardekani teaches two implementations of shared memory: (1) a simple implementation where the memory has enough capacity to implement a session without using some bytes for both interleaving and deinterleaving for that session; and (2) an optimal implementation where the RAM is not large enough to execute a session without using at least some bytes for both interleaving and deinterleaving even for that particular session. *Id.*, 7:25-33. Both the simple and optimal implementations have the property that a portion of the memory can be used by either one of the functions of interleaving or deinterleaving. Ex. 1003, ¶69.

iii. Motivation to Combine

Both VDSL1 and Fadavi-Ardekani are directed to VDSL systems. Ex. 1007, Cover; Ex. 1006, 4:19-21; Ex. 1003, ¶75-92. Indeed, VDSL1 is the technical specification put forth by ETSI that "specifies requirements for transceivers that

provide very high bit-rate digital transmission," i.e., VDSL, and Fadavi-Ardekani contemplates that the transceiver of the invention may "incorporate other variations of DSL (i.e., xDSL), such as High bit-rate DSL (HDSL) and Very high bit-rate DSL (VDSL)." Ex. 1007, 9; Ex. 1006, 4:19-21.

As described in Ground 1, VDSL1 is a standards document that includes, among other things, initialization instructions. Ex. 1007, 111 (disclosing "Initialisation" protocols for the transceiver pair VTU-O and VTU-R, including an "[e]xchange of parameters)"); *id.*, 127-34 (disclosing a "channel analysis and exchange" state, which discloses the negotiation of interleaver/deinterleaver parameters, including R-MSG2, which specifies a maximum number of bytes of memory available to be allocated to an interleaver). In so doing, VDSL1 discloses various elements, such as a communication device (e.g., a transceiver). Ex. 1007, 13.

VDSL1 does not, however, expressly disclose use of a shared memory between the interleaver and deinterleaver. Ex. 1003, ¶87. A POSA would have understood that a transceiver as contemplated in VDSL1 would have implemented any efficiencies to meet those disclosed parameters. *Id.* Here, implementing a shared memory was one known efficiency. *Id.*

Fadavi-Ardekani disclosed shared memory between an interleaver and deinterleaver. Ex. 1006, 5:60-65; 6:55-58 ("The Interleave/De-Interleave Memory (IDIM) 230 provides a memory" and "may be utilized in a ping-pang fashion," meaning that "[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent").

A POSA thus would have been motivated to combine the shared memory of Fadavi-Ardekani with the transceivers disclosed by VDSL1 to create transceivers that are more efficient, which would provide the advantages of allowing each transceiver to support more sessions or sessions that are more data intensive and, thus, reduce costs. Ex. 1006, 8:4-17 (explaining that the memory savings of the invention reduces cost); Ex .1003, ¶89. This simple substitution would have achieved the known benefits of allowing the VDSL1 transceiver to implement a wider range of interleaver and deinterleaver parameters for a given size of memory or to implement more sessions for given size of memory or to support a given range of interleaver and deinterleaver parameters with less memory. Ex. 1003, ¶89.

There are several reasons to implement Fadavi-Ardekani's shared memory in the system disclosed by VDSL1. Ex. 1003, ¶90. First, VDSL1 describes determining the memory allocations for the interleaver and deinterleaver when using the triangular implementation of convolutional interleaving and deinterleaving but does not provide explicit instructions for the hardware that should or must be used to

implement the standard. *Id.* Fadavi-Ardekani, granted as a patent around the same time that the VDSL1 technical specification was published, provides the requisite hardware and instructs that its disclosure may beneficially be implemented with VDSL. Ex. 1006, 4:18-21; Ex. 1003, ¶90. As a result, the POSA would have been motivated to combine a reference that provides increased efficiencies to the memory of the transceiver in a VDSL environment with VDSL1's transceiver. Ex. 1003, ¶90.

Second, the POSA would have understood that implementing the VDSL1 standard supporting *both* asymmetric and symmetric downstream and upstream data streams for the numerous sessions and multiple lines that must be supported by an operator would be costly to implement because it may result in a larger number of transceivers and/or more memory in each transceiver. Ex. 1003, ¶91. As a result, the POSA would have looked to solutions that could provide the necessary functionality, without increased cost. *Id.* Fadavi-Ardekani provides such a benefit. Specifically, Fadavi-Ardekani explains that "the memory savings and corresponding reduction in buffer size permitted by the invention reduces integrated circuit area and ADSL transceiver cost," as well as, in a central office, results in requiring "a lesser number of ADSL transceivers than prior art ADSL communications systems." *Id.*, 8:8-17. Given the costs savings and reduction in integrated circuit area, the

POSA would have been further motivated to select the Fadavi-Ardekani solution. Ex. 1003, ¶91.

In addition, the POSA would have had a reasonable expectation of success in the combination because Fadavi-Ardekani expressly instructs that its disclosure can be implemented with VDSL, Ex. 1006, 4:18-21, and because both VDSL1 and Fadavi-Ardekani disclose transceivers that include Reed-Solomon encoding, an interleaver to interleave Reed-Solomon bytes, a deinterleaver to deinterleave Reed-Solomon bytes, and a memory to support the interleaving and deinterleaving functions. *Compare* Ex. 1007, 59-60; 71-72, *with* Ex. 1006, Abstract, 6:15-16; *see also* Ex. 1003, ¶92.

For at least these reasons, in reading VDSL1, a POSA thus would have been motivated to look to Fadavi-Ardekani and had a reasonable expectation of success in doing so. Ex. 1003, ¶92.

2. Claim 1

i. [1.pre]

As explained in Ground 1, Limitation [1.pre], *supra*, Petitioner does not believe the preamble is limiting. As further explained *supra*, Petitioner does not agree with the District of Delaware's construction of shared memory, but, under either construction, Fadavi-Ardekani discloses this limitation. Ex. 1003, ¶¶217-219.

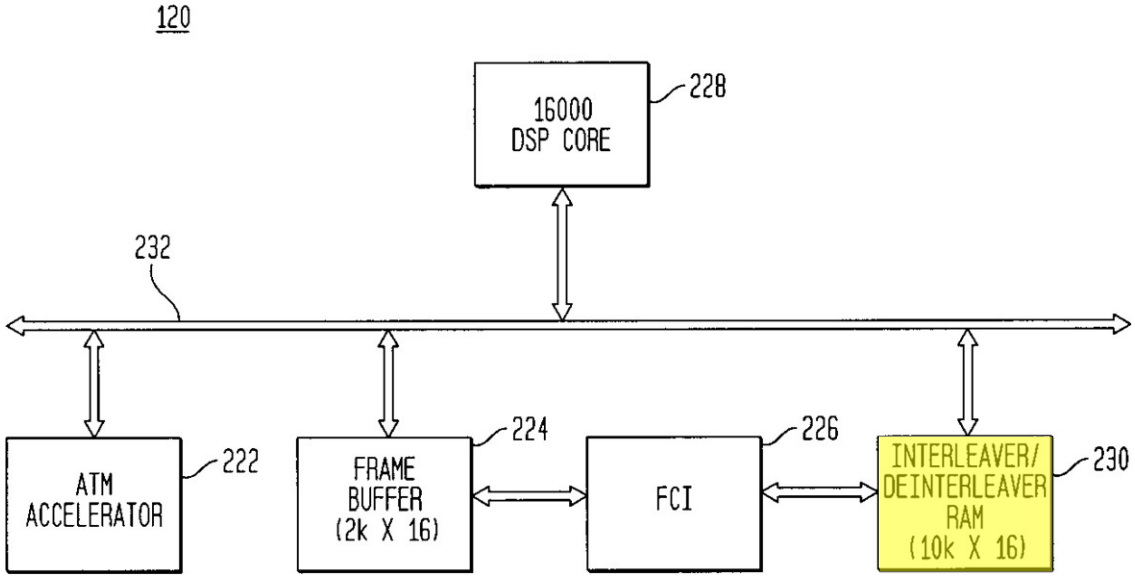
To the extent it is argued that the preamble is entirely limiting, Fadavi-Ardekani discloses this limitation. Fadavi-Ardekani discloses a "central office transceiver" that "includes various functional elements and memories coupled together with digital signal processing tasks synchronized by a virtual clock signal." Ex. 1006, 3:5–8. As explained *supra*, a POSA would understand such memories coupled to a DSP to be a "non-transitory computer-readable information storage media." Ex. 1003, ¶218. Fadavi-Ardekani next explains that in "the exemplary embodiment, the transceiver uses a Digital Signal Processor (DSP) core and is preferably implemented as a core of an DSP16K single chip DSP," and that "processing components of the transceiver communicate with the DSP core," Ex. 1006, 6:43–50, which a POSA would understand to mean that the transceiver includes a processor that executes instructions stored in a memory, Ex. 1003, ¶218. Thus, Fadavi-Ardekani discloses non-transitory computer-readable information storage media having stored thereon instructions for allocating memory.

Fadavi-Ardekani also discloses that when those instructions are executed by the processor, a method for allocating shared memory is performed, namely that a system with a common memory that is used by a first function (e.g., the interleaver) and a second function (e.g., the deinterleaver), where a portion of the memory (MM) can be used by either one of the functions. *See* ¶¶219-231*; see also* Claims 1-8, *infra*.

In the Delaware Litigation, the district court granted summary judgment of no invalidity determining that Fadavi-Ardekani did not directly disclose a shared memory as construed—namely, a shared memory *where a portion of the memory can be used by either one of the functions*—and that the Defendants failed to assert that such a shared memory was inherent in the disclosure. Ex. 1022, 17. This decision is inapplicable here because (1) Defendants in that case failed to particularly describe the embodiment—i.e., the "optimal implementation"—that expressly discloses this limitation; and (2) because Defendants in that case failed to assert that the embodiment it did identify inherently disclosed this limitation, both of which Petitioner does here.

Fadavi-Ardekani discloses this limitation. Ex. 1003, ¶220-231. Specifically, Fadavi-Ardekani discloses an "**Interleave/De-Interleave Memory (IDIM)**" that "provides a memory" and "may be utilized in a **ping-pang fashion**." Ex. 1006, 6:55-58. Fadavi-Ardekani defines "ping-pang" to mean that "areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent" and that "[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent." *Id.*, 5:60-65. Fadavi-Ardekani provides Figure 2, which identifies an "Interleaver/Deinterleaver RAM" (highlighted, below).

FIG. 2



Fadavi-Ardekani further teaches two implementations of allocating shared memory: (1) a "simple implementation"; and (2) an "optimal implementation." Ex. 1003, ¶¶224-226. In the simple implementation, Fadavi-Ardekani contemplates an ADSL session, which requires "16 Kbytes per session for downstream processing" and "2 Kbytes per session for upstream processing," thus requiring 18 Kbytes of RAM per session, or "72 Kbytes for four sessions." Ex. 1006, 7:13-17.

A POSA looking to Fadavi-Ardekani for a beneficial environment in which to implement VDSL would have understood that a dynamically allocable shared memory would be selected because support of both asymmetric and symmetric streams requires that the ratio of interleaver and deinterleaver sizes is *not fixed* and the flexibility to use a portion of the memory for interleaving or deinterleaving would necessarily be required to implement the full range of VDSL. Ex. 1006, 7:30-33;

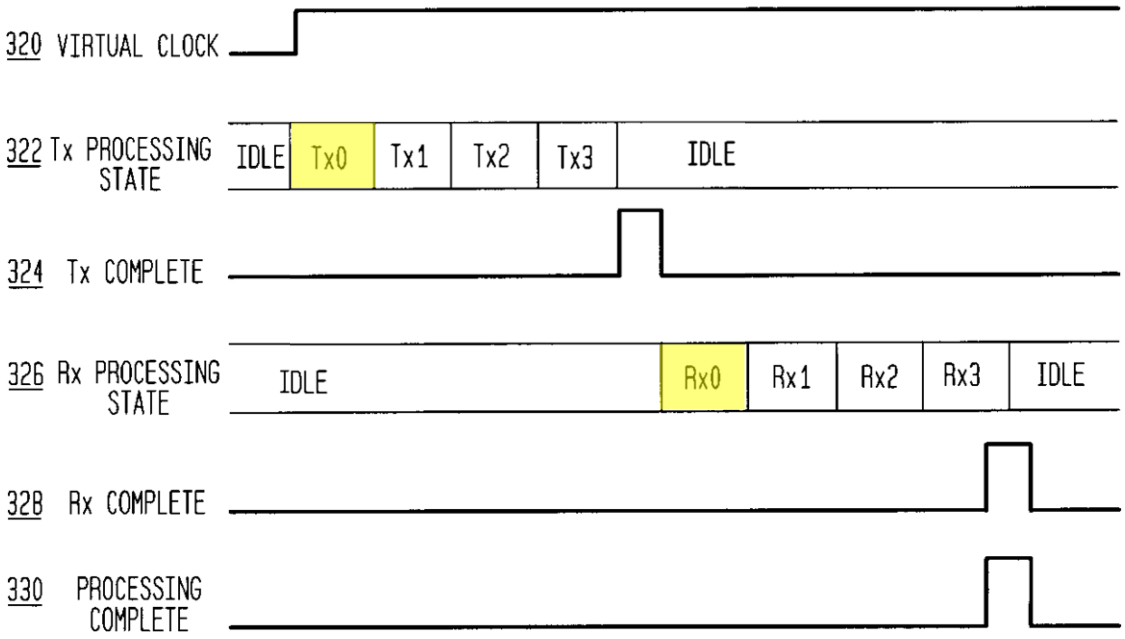
Ex. 1003, ¶227. Specifically, VDSL1 contemplates both symmetric and asymmetric systems, Ex. 1007, 37, meaning that, when using the full capacity of the RAM, there would be some bytes of memory used for interleaving in an asymmetric implementation and some bytes used for deinterleaving in a symmetric implementation, Ex. 1003, ¶227.

Regardless, in the "optimal implementation of the interleaver," Fadavi-Ardekani expressly discloses a *shared* memory where a portion of the memory can be used by either one of the functions. *Id.*, ¶228. Fadavi-Ardekani explains that the invention "*utilizes the same memory for receive data and transmit data*," and thus the interleaver/deinterleaver may be assigned only 16 Kbytes. Ex. 1006, 7:25-30. Because one ADSL session requires 16 Kbytes in the downstream and 2 Kbytes in the upstream—for a total of 18 Kbytes—and the RAM available to the interleaver/deinterleaver is only 16 Kbytes (after accounting for 4 Kbytes for the fast path buffer), a portion of the memory must be used by both the interleaver and deinterleaver to implement the disclosed session. Ex. 1003, ¶228.

Relying on Figure 3, below, Fadavi-Ardekani also discloses that the FCI "first processes TX data for each active ADSL line," which may include the 16 Kbytes of interleaved data (highlighted below, Tx0), and then "processes RX data for each active ADSL line," which may include 2 Kbytes of deinterleaved data (highlighted

below, Rx0), all in a single session that was originally only allocated 16 Kbytes of RAM. Ex. 1003, ¶229-230.

FIG. 3



Thus, Fadavi-Ardekani discloses a common memory (e.g., the IDIM) used by at least two functions (e.g., the interleaver and the deinterleaver), where a portion of the memory (e.g., 16 Kbytes of RAM) can be used by either one of the functions.

VDSL1 and Fadavi-Ardekani further disclose a transceiver, as described in Limitation 1.A, *infra*.

ii. [1.A]

As explained *supra*, Petitioner does not agree with the District of Delaware's construction of transceiver, but, under either construction, VDSL1 and Fadavi-Ardekani disclose this limitation.

As described *supra* in Ground 1, Limitation [1.A], the VDSL1 technical specification discloses a communications device, including a VDSL Transceiver Unit, Ex. 1007, 13, 17 (depicted below), capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.

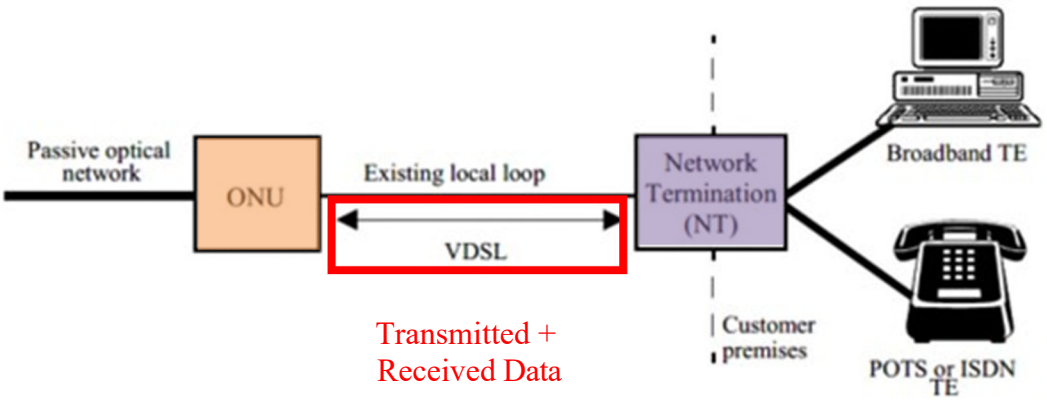


Figure 4: General fibre-to-the-node architecture for VDSL

Fadavi-Ardekani likewise discloses a transceiver, i.e., a communication device capable of transmitting and receiving data (e.g., a "transceiver for an asymmetric communication system"). Ex. 1006, Abstract. As described with respect to Limitation [1.pre], Fadavi-Ardekani further discloses a shared memory "IDIM," which is "bi-directionally coupled to [a framer/coder/interleaver (FCI)]." *Id.*, 9:49-55. The POSA would have understood the shared memory of Fadavi- Ardekani is common circuitry between the "transmitters and receivers." *Id.*, Abstract ("Memory

is shared by multiple ADSL sessions and by the transmit and receive processes within an individual session."); Ex. 1003, ¶246.

In addition to disclosing a transceiver, and as described *supra* in Ground 1, Limitation [1.A], the VDSL1 standard discloses how each of its transceivers transmit or receive a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver through R-MSG2. Ex. 1003, ¶247; *see also* Ground 1, Limitation [1.A], *supra*.

Therefore, the combination of VDSL1 and Fadavi-Ardekani discloses a transceiver (e.g., in VDSL1, the VDSL Transceiver Unit or VTU, and, in Fadavi-Ardekani, a transceiver for an asymmetric communication system) that performs: transmitting or receiving a message (e.g., R-MSG2) during initialization (e.g., the channel analysis and exchange state) specifying a maximum number of bytes of memory that are available to be allocated to an interleaver (e.g., the parameter "Maximum interleaver memory").

iii. [1.B]

As explained *supra*, Petitioner does not agree with the District of Delaware's construction of amount of memory, but, under either construction, VDSL1 and Fadavi-Ardekani disclose this limitation.

For example, VDSL1 explains that the "(De)interleaver memory size" at the transceiver can be determined from the equation **MxIx(I–1)/2** (see Table 19 below), wherein parameter I is the interleaver block length and parameter M is the interleaving depth parameter. *Id.*, 60.

Table 19: Characteristics of triangular, convolutional interleaver

Parameter	Value
Interleaver block length	I octets (I must divide N)
Interleaving depth *D*	M x I + 1 octets
(De)interleaver memory size	M x I x (I–1)/2 octets
End-to-end delay	M x I x (I–1) octets
Correction capability	⌊t/q⌋ x M x (I+1) octets

VDSL1 also contemplates interleaving Reed-Solomon codewords, explaining that "[i]nterleaving shall be used to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords," and "[w]hen the interleaver is on, the codewords shall be interleaved before transmission to increase the immunity of RS codewords to bursts of errors." *Id.*at 59. VDSL1 further requires that interleavers be supported for Reed-Solomon codes. *Id.*, 59-62. Specifically, VDSL1 explains that a "standard octet-oriented Reed-Solomon code shall be used to provide protection against random and burst errors," where a "Reed-Solomon code word contains *N=K+R octets*," and *(N,K)* must be one of (144,128) and (240,224). *Id.*, 59.

VDSL1 provides an implementation example based on Table B.1 (below), from which the (de)interleaver memory sizes may be calculated. *Id.*, 153; Ex. 1003, ¶¶252-253.

Table B.1: Interleaving depth Parameter values

Line Rate, Mb/s		1,62	3,24	6,48	12,96	25,92	51,84
Value of N/I		8					
250 µs of erasure correction	M, octets	2	4	8	16	32	64
	Delay, msec	5,9					
500 µs of erasure correction	M, octets	4	8	16	32	64	128
	Delay, msec	11,8					

Relying on the disclosed equation **MxIx(I–1)/2**, and applying that to the parameters contemplated in Table B.1, a POSA would have understood how to determine the "(De)interleaver memory size" as shown below. *See* Ex. 1003, ¶¶254-255.

Impulse noise burst time in ms	0.25 ms			0.5 ms		
Corresponding latency in ms	5.9 ms			11.8 ms		
Bit Rate in Mb/s	M	I (for N=240)	Memory (bytes)	M	I for (N=240)	Memory (bytes)
1.62 Mb/s	2	30	870	4	30	1740
3.24 Mb/s	4	30	1740	8	30	3480
6.48 Mb/s	8	30	3480	16	30	6960
12.96 Mb/s	16	30	6960	32	30	13920
25.92 Mb/s	32	30	13920	64	30	27840
51.84 Mb/s	64	30	27840	128	30	55680

A POSA would further make this determination on a shared memory—such as the shared memory disclosed in Fadavi-Ardekani, IDIM—as disclosed in [1.pre] for the benefits described *supra*. *Id.*

The combination of VDSL1 and Fadavi-Ardekani thus discloses determining, at the transceiver (e.g., VTU-O as disclosed in VDSL1), an amount of memory (e.g., **MxIx(I-1)/2** as disclosed in VDSL1) required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory (e.g., IDIM of Fadavi-Ardekani).

iv. [1.C]

The combination of VDSL1 and Fadavi-Ardekani disclose this limitation for the same reasons as discussed in Limitations [1.A] and [1.B]. *See supra*. Specifically, VDSL1 and Fadavi-Ardekani disclose allocating, in the transceiver (in VDSL1, VTU-O), a first number of bytes of the shared memory (in Fadavi-Ardekani, the IDIM) to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes (in VDSL1, as described *supra*) for transmission at a first data rate (in VDSL1, as described *supra*). *See also* Ground 1, Limitation [1.C].

In addition to *determining* an amount of memory required to interleave a first plurality of Reed-Solomon coded data bytes as described *supra*, VDSL1 in view of Fadavi discloses *allocating* the required amount to the interleaver. As explained *supra* in Ground 1, Limitation [1.C], VDSL1 discloses a message (O- CONTRACTn) that communicates the parameters I and M, which define the convolutional interleaver function. VDSL1 also discloses a specific triangular implementation that uses exactly Ix(I-1)xM/2 bytes of memory to implement the convolutional

interleaver or deinterleaver with parameters I and M, thus allocating the required amount of memory to the interleaver or deinterleaver based on parameters I and M. Ex. 1003, ¶256-265.

The combination of VDSL1 and Fadavi-Ardekani thus discloses this limitation, as well as wherein the allocated memory for the interleaver (in VDSL1, set by message O-CONTRACTn) does not exceed the maximum number of bytes specified in the message (in VDSL1, set by message R-MSG2).

v. [1.D]

VDSL1 and Fadavi-Ardekani disclose this limitation for the same reasons as discussed in Limitation [1.C]. *See also* Ground 1, Limitation [1.D]. Indeed, VDSL1 discloses various "*(De)*interleaver memory size[s]," indicative of the fact that a second number of bytes of the shared memory may be allocated, in the transceiver, to a deinterleaver when the first number of bytes was allocated to an interleaver. Likewise, to the extent it is argued that the second data rate must be different from the first data rate, VDSL1 discloses that the determination of memory to be allocated may be based on various parameters, including "different line rates." Ex. 1007, 153. A POSA would thus have understood that the allocation may be based on a second data rate. Ex. 1003, ¶¶266-268.

vi. [1.E]

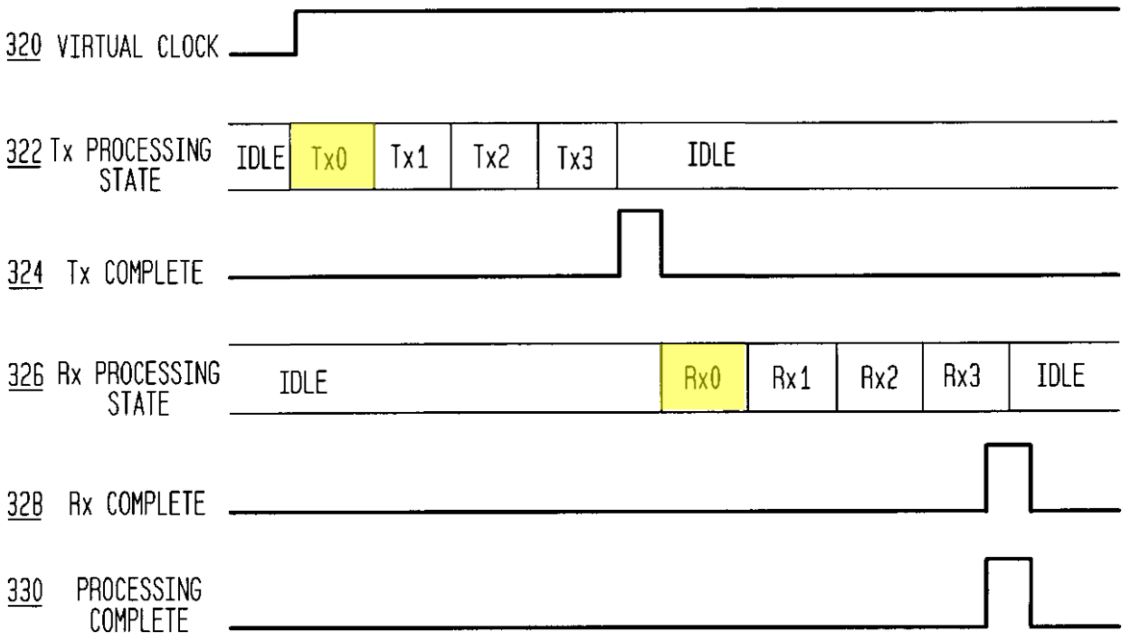
As is discussed in Limitations [1.B]-[1.D], *supra*, the combination of VDSL1 and Fadavi-Ardekani disclose interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

With respect to "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver," Fadavi-Ardekani discloses this limitation. As explained *supra*, Petitioner adopts the district court's construction for purposes of this petition.

Fadavi-Ardekani discloses an "Interleave/De-Interleave Memory (IDIM)" that "provides a memory" and "may be utilized in a **ping-pang** fashion." Ex. 1006, 6:55-58. Fadavi-Ardekani defines "**ping-pang**" to mean that "areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent" and that "**[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent**." *Id.*, 5:60-65. A POSA would have understood that use of the memory in a ping-pang fashion would allow the disclosed interleaver to read from or write to one port while the disclosed deinterleaver simultaneously reads from or writes to a second port. Ex. 1003, ¶271.

Likewise, in Figure 3, below, Fadavi-Ardekani also discloses that the FCI "first processes TX data for each active ADSL line," (i.e., writes to) and then "processes RX data for each active ADSL line," (i.e., reads from) all in a single session. Ex. 1006, 7:63-8:4.

FIG. 3



The combination of VDSL1 and Fadavi-Ardekani thus discloses this limitation, including wherein the shared memory allocated to the interleaver (e.g., in IDIM) is used at the same time (e.g., in a ping-pang fashion) as the shared memory allocated to the deinterleaver (e.g., in IDIM).

3. Claim 2:

The combination of VDSL1 and Fadavi-Ardekani discloses this claim at least because of the reasons identified in VDSL1 as was discussed in claim 2, Ground 1.

4. Claim 3:

The combination of VDSL1 and Fadavi-Ardekani discloses this claim at least because of the reasons identified in VDSL1 as was discussed in claim 3, Ground 1.

5. Claim 4:

The combination of VDSL1 and Fadavi-Ardekani discloses this claim at least because of the reasons identified in VDSL1 as was discussed in claim 4, Ground 1.

6. Claim 5

i. [5.pre]

See Limitation [1.pre].

ii. [5.A]

See Limitation [1.A] and Ground 1, Limitation [5.A].

iii. [5.B]

See Limitation [1.B] and Ground 1, Limitation [5.B].

iv. [5.C]

See Limitation [1.C] and Ground 1, Limitation [5.C].

v. [5.D]

See Limitations [1.D] and [5.C].

vi. [5.E]

See Limitation [1.E] and Ground 1, Limitation [5.E].

7. Claim 6:

See claim 2.

8. Claim 7:

See claim 3.

9. Claim 8:

See claim 4.

VII. DISCRETIONARY ISSUES

A. The Copycat Petition Does Not Present the Same References Addressed in Prosecution

Under *Advanced Bionics*, the Board should not deny institution under § 325(d). *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 7 (PTAB Feb. 13, 2020) (precedential).

The Board has held that the first prong of *Advanced Bionics* is not met where "neither [the combination references] nor similar prior art was before the examiner … the prosecution history does not include any overlapping arguments directed to this prior art." *Godbersen-Smith Constr. Co. v. Guntert & Zimmerman Const. Div., Inc*. IPR2021-00050, Paper 24 at 19-21 (PTAB May 7, 2021). All but one of the prior art references here was not cited during original prosecution and is not cumulative of any of the art considered by the Examiner during prosecution.

See III.A *supra*. Only Fadavi-Ardekani (one of two references at issue in Ground 2) appears on the face of the '381 patent, but the Petition relies on Fadavi-Ardekani for a limitation the Examiner agreed was disclosed.

Indeed, the Examiner stated that Fadavi-Ardekani "discloses sharing a memory between the interleavers and deinterleavers" but "fails to suggest the [other] claim elements." Ex. 1002 at 61. Here, the Petition relies on previously uncited VDSL1 as a base reference to teach those other claim elements. Because Petitioner relies on VDSL1 with respect to limitations that the Examiner alleged were not found in the art, there are material differences between the grounds herein and what was considered during prosecution. *Tianma Microelectronics Co.., v. Japan Display Inc.*, No. IPR2021-01058, Paper 16 at 31 (PTAB Jan. 5, 2022). Because the first prong is not met, the Board need not move to the second prong. *See id*. at 21; *Oticon Med. AB v. Cochlear Ltd*., IPR2019-00975, Paper 15 at 20 (PTAB Oct. 16, 2019).

Even if the Second Prong is reached, Petitioner has demonstrated a material difference between the grounds herein and what was previously considered by the Examiner by pointing out and explaining how the combination of VDSL1 and Fadavi-Ardekani teach the numerous limitations of the claims in combination. *See Tianma*, IPR2021-01058, Paper 16 at 31 ("Because Petitioner relies on [a new reference] with respect to a limitation that the Examiner determined was not found

in the art, there are material differences between the asserted art here and the art considered during examination.").

Because Fadavi-Ardekani was the only prior art reference addressed by the Examiner during prosecution, the majority of the grounds do not rely on the same or substantially the same prior art previously considered during prosecution. *Progenity, Inc. v. Natera, Inc.*, IPR2021-00279, Paper 12 at 44 (PTAB June 11, 2021). Therefore, the Board should not exercise its discretion under 35 U.S.C. § 325(d). *Adobe, Inc. v. Realtime Adaptive Streaming LLC*, IPR2019-00712, Paper 9 at 18 (PTAB Sept. 12, 2019).

For at least these reasons, the Board should not deny institution under § 325(d).

B. The Board Should Not Deny Institution Under *Fintiv*

The Board should not discretionarily deny this Petition under *Apple Inc. v. Fintiv, Inc*., No. IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). Patent Owner asserted the '381 patent against 2Wire, a company acquired by Petitioner in April 2019, in the Delaware Litigation. The '381 patent also is the subject of the following additional litigations: *TQ Delta, LLC v. ADTRAN, Inc.*, Case No. 1:14-cv-00954 (D. Del.) and *ADTRAN, Inc. v. TQ Delta, LLC*, Case No. 1:15-cv-0012 (D. Del.).

Critically, the Board instituted the Nokia IPR over Patent Owner's *Fintiv* arguments in view of the USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, 4–5 (June 21, 2022) finding that:

> As discussed in detail below, the evidence of record plainly shows that the Mazzoni and VDSL1 combination teaches the disputed limitations and that it would have been obvious to combine the cited teachings of Mazzoni and VDSL1…. Because the information presented at the institution stage presents a compelling unpatentability challenge, we decline to exercise our discretion under § 314(a) to deny the Petition.

IPR2022-00665, Paper 10, at 7 (PTAB Oct. 3, 2022). On this basis alone, the Board should reject any *Fintiv* argument that Patent Owner may make and institute this IPR because this copycat petition also presents a compelling unpatentability challenge, *i.e.*, the same challenge presented in the Nokia IPR.

In the Delaware Litigation, a jury found the asserted claims of the '381 Patent valid and infringed, but the court has not yet scheduled a trial regarding damages or any of 2Wire's affirmative defenses or counterclaims. (Ex. 1023). Thus, the date of a final judgment in the Delaware Litigation is speculative but is unlikely to occur for several years. Given the speculative nature of the schedule in the Delaware Litigation, resolving Petitioner's invalidity challenge to the '381 patent through the present petition promotes efficiency.

Accordingly, the Board should decline to exercise its discretion under *Fintiv* and institute inter partes review.

VIII. CONCLUSION

Petitioner respectfully requests cancellation of the Challenged Claims.

IX. MANDATORY NOTICES FOR INTER PARTES REVIEW – 37 C.F.R. § 42.8(A)(1).

A. Real Parties in Interest – 37 C.F.R. § 42.8(b)(1).

The real parties in interest are CommScope Holding Company, Inc., CommScope Inc., ARRIS US Holdings, Inc., ARRIS Solutions, Inc., ARRIS Technology, Inc., and ARRIS Enterprises, Inc.

B. Related Matters – 37 C.F.R. § 42.8(b)(2).

The '381 patent is the subject of the following litigations *TQ Delta, LLC v. 2Wire, Inc*., Case No. 1:13-cv-01835 (D. Del.); *TQ Delta, LLC v. ADTRAN, Inc*., Case No. 1:14-cv-00954 (D. Del.); *ADTRAN, Inc. v. TQ Delta, LLC*, Case No. 1:15- cv-0012 (D. Del.).

Petitioner is not aware of any other judicial or administrative matter that would affect or be affected by a decision in this IPR.

C. Lead and Backup Counsel – 37 C.F.R. § 42.8(b)(3); Service Information – 37 C.F.R. § 42.8(b)(4) & Power of Attorney.

Petitioner designates the following lead and backup counsel:

Lead Counsel	*Back-up Counsel*

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Pursuant to 37 C.F.R. § 42.8(b)(4), counsel agrees to service by mail as

detailed above, and to electronic service by email at the following addresses: sdutta@goodwinlaw.com; bschuman@goodwinlaw.com; aong@goodwinlaw.com; adiaw@goodwinlaw.com. A Power of Attorney executed by Petitioner accompanies this Petition.

X. CERTIFICATION OF GROUNDS FOR STANDING.

Petitioner certifies that the '381 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR.

XI. PAYMENT OF FEES – 37 C.F.R. § 42.15.

Petitioner authorizes the U.S. Patent & Trademark Office to charge Deposit Account No. 506989 for the fee set in 37 C.F.R. § 42.15(a) for this Petition and further authorizes any additional fees to be charged to this Deposit Account.

Date: November 1, 2022

Respectfully submitted,

By: /Sanjeet K. Dutta/

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CLAIMS APPENDIX

Claim	Recitation
1	A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising: transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver; determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.
2	The media of claim 1, wherein the determining is based on an impulse noise protection requirement.
3	The media of claim 1, wherein the determining is based on a latency requirement.
4	The media of claim 1, wherein the determining is based on a latency requirement.
5	A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising: transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of

Claim	**Recitation**
	memory that are available to be allocated to a deinterleaver; determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.
6	The media of claim 5, wherein the determining is based on an impulse noise protection requirement.
7	The media of claim 5, wherein the determining is based on a latency requirement.
8	The media of claim 5, wherein the determining is based on a bit error rate requirement.

CERTIFICATE OF COMPLIANCE

Petitioner certifies that the word count in this Petition is 13,540 words, as counted by the word-processing program (Microsoft Word for Office 365) used to generate this Petition, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, appendix of exhibits, and this certificate of word count. This Petition is in compliance with the 14,000-word limit set in 37 C.F.R. § 42.24(a)(1)(i).

Dated: November 1, 2022

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Lead Counsel for Petitioner

CERTIFICATE OF SERVICE ON PATENT OWNER

The undersigned certifies that the foregoing Petition for Inter Partes Review of U.S. Patent No. 7,836,381 and supporting Exhibits 1001 to 1033 were served on November 1, 2022 by Federal Express Next Business Day Delivery on the Patent Owner at the correspondence address of record for the '381 patent:

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver CO 80202

Courtesy copies of the foregoing Petition and Exhibits 1001-1033 were also served via Federal Express Next Business Day Delivery and email upon counsel of record for TQ Delta, LLC, the Patent Owner in IPR2022-00665:

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