UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY
Patent Owner

Patent No. 7,421,032

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,421,032

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner" or "Samsung") requests *inter partes* review of claims 1-8 and 10-22 ("challenged claims") of U.S. Patent No. 7,421,032 ("the '032 patent") (Ex. 1001) assigned to California Institute of Technology ("PO"). For the reasons below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc.

Related Matters: The '032 patent is at issue in the following matters:

- *California Institute of Technology v. Samsung Electronics Co., Ltd.*, No. 2-21-cv-00446 (E.D. Tex.) (alleging infringement of the '032 patent and also U.S. Patent Nos. 7,116,710; 7,916,781; and 8,284,833) ("E.D. Texas Litigation").
- *California Institute of Technology v. Microsoft Corp.*, No. 6-21-cv-00276 (W.D. Tex.).
- *California Institute of Technology v. HP Inc. f/k/a/ Hewlett-Packard Co.*, No. 6-20-cv-01041 (W.D. Tex.).

- *California Institute of Technology v. Dell Technologies Inc.*, No. 6-20-cv-01042 (W.D. Tex.).
- *California Institute of Technology v. Broadcom Ltd.*, No. 2-16-cv-03714 (C.D. Cal.).

The '032 patent has previously been at issue in the following matters:

- *Apple Inc. v. California Institute of Technology*, IPR2017-00700 ("Apple -700 IPR").
- *Apple Inc. v. California Institute of Technology*, IPR2017-00701 ("Apple -701 IPR").
- *Apple Inc. v. California Institute of Technology*, IPR2017-00728 ("Apple -728 IPR").
- *California Institute of Technology v. Hughes Communications, Inc.*, No. 2-15-cv-01108 (C.D. Cal.).
- *Hughes Communications, Inc. v. California Institute of Technology*, IPR2015-00060 ("Hughes -060 IPR").
- *California Institute of Technology v. Hughes Communications, Inc.*, No. 2-13-cv-07245 (C.D. Cal.).

Counsel and Service Information: Lead counsel: Robert A. Appleby (Reg. No. 40,897), and Backup counsel is Greg S. Arovas, P.C. (Reg. No. 38,818). Service information is Kirkland & Ellis, LLP, 601 Lexington Avenue, New York, NY

10022, Telephone: 212.446.4800, Facsimile: 212.446.4900, Email: Samsung_Caltech_IPR@kirkland.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 506092.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '032 patent is available for review and Petitioner is not barred/estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS

Claims 1-8 and 10-22 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1, 3-5, 7-8, 11-12, and 14-16 are unpatentable under pre-AIA 35 U.S.C. § 102(e) as anticipated by *Kobayashi* (Ex. 1005);

Ground 2: Claims 2, 6-7, 10, 13, and 17 are unpatentable under § 103(a) as obvious over *Kobayashi*; and

Ground 3: Claims 6, 13, and 18-22 are unpatentable under § 103(a) as obvious over *Kobayashi* and *McEliece* (Ex. 1006).[1]

The '032 patent issued from an application filed October 3, 2006, and claims priority to, *inter alia*, a provisional application filed May 18, 2000. Petitioner does not concede that the priority claim to the provisional application is proper, but for purposes of this proceeding, assumes the critical date for the '032 patent is May 18, 2000.

Kobayashi was filed April 28, 1997 and issued on February 22, 2000, and thus qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and 102(e).

McEliece is an article published in February 1998 in the *IEEE Journal on Selected Areas in Communications*. (Ex. 1006, Cover; *see also id.* (Library date stamp), 2 ("Copyright © 1998").) The Board has routinely held IEEE publications like *McEliece* as printed publications. For example, "[t]he Board has previously observed that 'IEEE is a well-known, reputable compiler and publisher of scientific and technical publications, and we take Official Notice that members in the scientific and technical communities who both publish and engage in research rely on the

[1] For the Grounds presented, Petitioner does not rely on any prior art reference other than those listed here. Any other references discussed are to show the state of the art.

information published on the copyright line of IEEE publications.'" *Power Integrations, Inc., v. Semiconductor Components Industries, LLC*, IPR2018-00377, Paper No. 10 at 10 (July 17, 2018) (quoting *Ericsson, Inc. v. Intellectual Ventures I LLC*, IPR2014-00527, Paper 41 at 11 (May 18, 2015)). Thus, *McEliece* qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(b).

These references were not considered during prosecution or prior IPRs. (*See generally* Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art at the time of the alleged invention ("POSITA") would have had a Ph.D. in mathematics, electrical or computer engineering, or computer science with an emphasis in signal processing, communications, or coding, or a master's degree in the above areas with at least three years of work experience in the field at the time of the alleged invention. (Ex. 1002, ¶¶21-22.)[2] Additional education would compensate for less experience, and vice versa. (*Id.*)

[2] Petitioner submits the declaration of Matthew C. Valenti, Ph.D., P.E. (Ex. 1002), an expert in the field of the '032 patent. (Ex. 1002, ¶¶3-20; Ex. 1003.)

VII. OVERVIEW OF THE '032 PATENT

The '032 patent relates to "serial concatenation of interleaved convolutional codes forming turbo-like codes." (Ex. 1001, Title; Ex. 1002, ¶¶36-39.) The '032 patent describes a "serial concatenated coder" that "includes an outer coder and an inner coder," where the "outer coder irregularly repeats bits in a data block according to a degree profile and scrambles the repeated bits," which are then "input to an inner coder, which has a rate substantially close to one." (Ex. 1001, Abstract.)

An exemplary embodiment of the alleged invention is disclosed by way of Figure 2. (*Id.*, 2:35.)

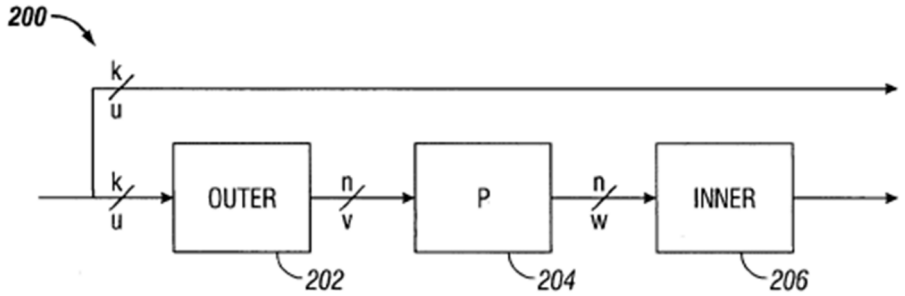


FIG. 2

(*Id.*, FIG. 2.; *see also id.* ¶¶23-35 (discussing technology background).)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Petitioner below provides proposed

constructions under the *Phillips* standard for certain terms recited in claims 1(c), 5(b), 7(b), 13(b)-(c), and 17 of the '032 patent. For purposes of this proceeding, Petitioner believes that other than the term(s) discussed below in Section VIII.A, no other special constructions are necessary to assess whether the challenged claims are unpatentable over the asserted prior art, and thus any remaining terms should be given their plain and ordinary meaning.[3] (Ex. 1002, ¶40.)

A. "repeat"

The term "repeat[]," as recited in claims 1(c), 5(b), 7(b), 13(b)-(c), and 17, should be construed to mean "generation of additional bits, where generation can include, for example, duplication or reuse of bits." (*See, e.g.*, Sections IX.A.1(c), IX.A.4(b), IX.A.5(b), IX.B.3(b), IX.B.5(b)-(c), IX.B.6, IX.C.2(b)-(c); Ex. 1002, ¶41.)

The Federal Circuit affirmed this construction of "repeat" in *California Inst. of Tech. v. Broadcom Ltd.*, 25 F.4th 976, 986 (Fed. Cir. 2022) ("*Broadcom* litigation"). The Federal Circuit agreed with the district court and PO that the claims simply require bits to be repeated and do not limit how the duplicate bits are

[3] Petitioner reserves all rights to raise claim construction and other arguments, including challenges under 35 U.S.C. §§ 101 or 112, in district court as relevant to those proceedings.

created/stored in memory. *Id.* Applying this construction, the Federal Circuit found that passing an input bit through an AND gate (when the other input was "1") was "repeating" within the context of the asserted claims. *Id.* at 986-88.

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: Claims 1, 3-5, 7-8, 11-12, and 14-16 Are Anticipated By *Kobayashi*

1. Claim 1

a) A method comprising:

To the extent the preamble of claim 1 is limiting, *Kobayashi* discloses the limitations therein. (Ex. 1002, ¶¶56-57; *see also id.*, ¶¶42-48.) For example, *Kobayashi* discloses a concatenated system with a transmitter that receives message bits and uses several encoders that perform an encoding "method" as claimed. (Ex. 1005, FIG. 8, 5:25-27, 7:5-8:34; Ex. 1002, ¶56; *see also* Sections IX.A.1(b)-(d).) In particular, *Kobayashi* discloses that the method (as shown in Figure 8 below) comprises receiving message bits from a source via a packet transmission system; encoding the sequence of message bits using the Hamming encoder, interleaver, and precoder to generate a sequence of parity bits; and transmitting the encoded sequence to the receiver via duobinary signaling. (Ex. 1005, 7:5-8:34; Ex. 1002, ¶57.)

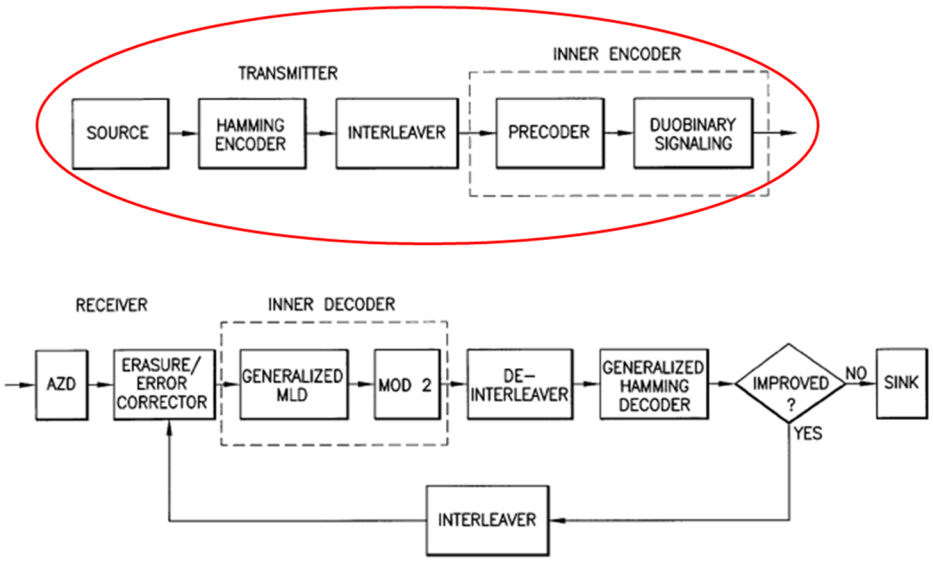


FIG.8

(Ex. 1005, FIG. 8 (annotated); *see also id.*, 5:17-24.)

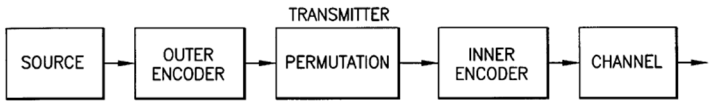


FIG.7A

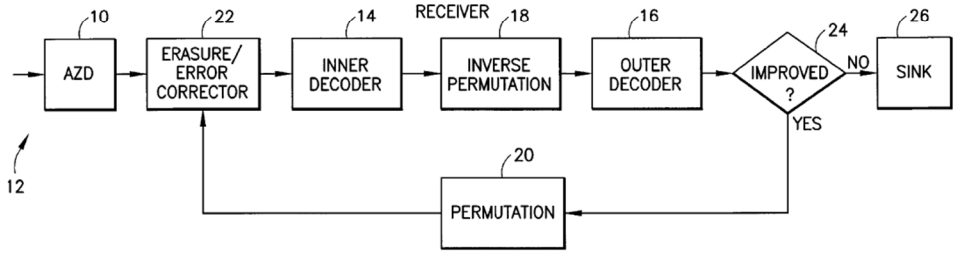


FIG.7B

(*Id.*, FIGS. 7A, 7B (showing generalized versions of Figure 8); Ex. 1002, ¶57.)

b) receiving a collection of message bits having a first sequence in a source data stream;

Kobayashi discloses these limitations. (Ex. 1002, ¶58.) For example, *Kobayashi* discloses that the transmitter receives a 28-message-bit sequence I_1 ("collection of message bits having a first sequence") in a source data stream (Ex. 1005, 7:46-49 (describing receipt of data via "a simple packet transmission system in which there are ***28 information bits in a packet***, an example of which is given by ***the stream: I_1=(0001001000110100010101100000)***.") (emphasis added).) *Kobayashi* depicts the source of the data stream in Figure 8 below.

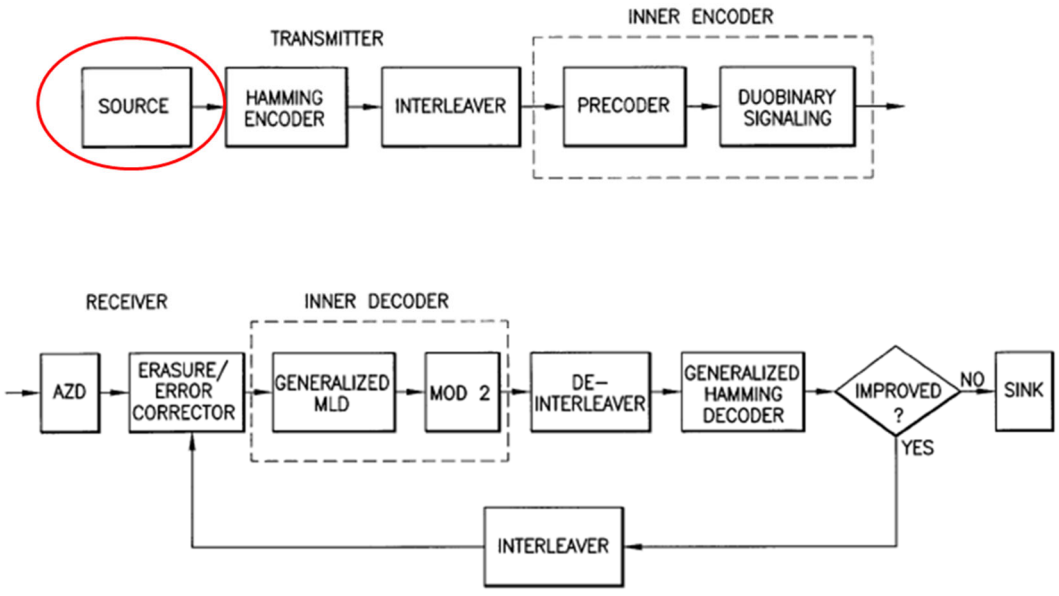


FIG.8

(Ex. 1005, FIG. 8 (annotated); Ex. 1002, ¶58.)

c) generating a sequence of parity bits, wherein each parity bit "x_j" in the sequence is in accordance with the formula $x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)a+i}$ where "x_{j-1}" is the value of a parity bit "j-1," and "$\sum_{i=1}^{a} v_{(j-1)a+i}$" is the value of a sum of "a" randomly chosen irregular

repeats of the message bits; and[4]

Kobayashi discloses these limitations. (Ex. 1002, ¶¶59-72.) *Kobayashi* discloses that the received 28-message-bit sequence I_1 is encoded in several steps, as shown below in Figure 8. (*Id.*, ¶59.)

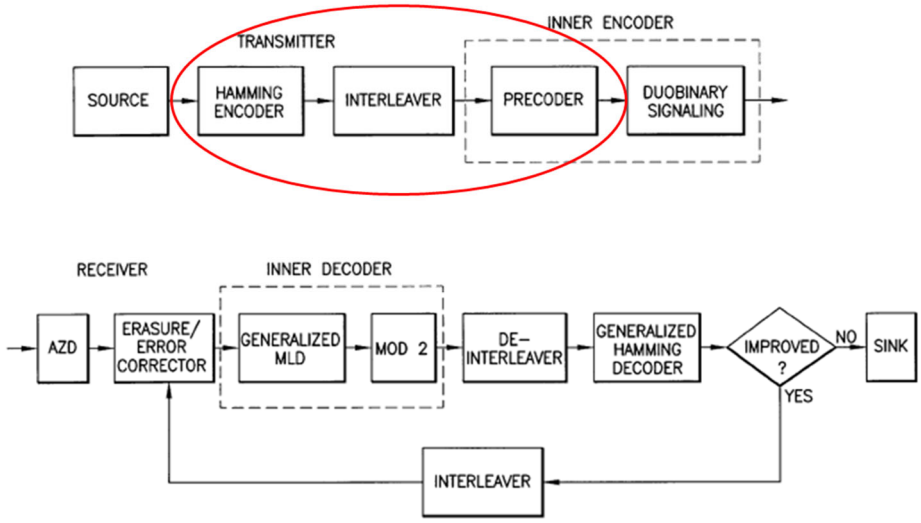


FIG.8

(Ex. 1005, FIG. 8 (annotated); Ex. 1002, ¶59.)[5] The 28-bit sequence I_1 is "first segmented into blocks of k=4 bits, and each block is then encoded to a codeword of length n=7, by using a (7, 4) Hamming code." (Ex. 1005, 7:50-53.) *Kobayashi*

[4] *See* Certificate of Correction (CoC) appended to the '032 patent.

[5] As discussed further for claim 1(d), *see infra* Section IX.A.1(d), *Kobayashi* discloses that duobinary signaling is a transmission technique for transmitting the sequence of parity bits to the decoder. (Ex. 1002, ¶59 n.4.)

discloses that the Hamming code's parity-check and generator matrices are represented in systematic form as follows:

$$H = \begin{bmatrix} 1 & 0 & 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$$

and

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix}$$

(*Id.*, 7:53-65.) After the Hamming encoder has been applied to all seven blocks of sequence I_1, "the Hamming encoder output is the following 49 bits (commas are placed between code words for clarity): I_2=(0001101, 0010111, 0011010, 0100011, 0101110, 0110100, 0000000)." (*Id.*, 7:66-8:2; Ex. 1002, ¶60.)

Kobayashi's method then uses a "7x7 block interleaver" to "perform a permutation action . . . which will store the above 49 bits [of I_2] row-wise in the following array structure."

$$\pi = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

(Ex. 1005, 8:3-15.) *Kobayashi* discloses that the "permutation output is obtained by "reading out the above array column by column as follows: I_3=(0000000, 0001110, 0110010, 1010100, 1100110, 0111100, 1101000)." (*Id.*, 8:16-20; Ex. 1002, ¶61.)

Kobayashi discloses that the sequence I_3 is the input to the precoder. (Ex. 1005, 8:18-27.) "The precoder output is obtained by taking the modulo-2 sum of the current input and the previous output (where 'modulo-2 summation' can be implemented by Exclusive OR: 0+0=0, 0+1=1, 1+0=1, 1+1=0)." (*Id.*, 8:21-24.) In other words, "[t]he precoder maps the input binary sequence into another binary sequence, based on the following rule: when the current input is 0, the output should remain in the previous value; and when the input is 1, the output changes its value from the previous one, i.e. either 0 to 1 or from 1 to 0." (*Id.*, 7:33-37.) The resulting encoded sequence is "I_4=(0000000, 0001011, 1011100, 1100111, 0111011, 1010111, 011000[0])." (*Id.*, 8:25-27; Ex. 1002, ¶62.)[6]

This generated sequence I_4 is a "sequence of parity bits" because the precoder can be represented as a (49, 49) nonsystematic linear block code. (Ex. 1002, ¶63.) In particular, the precoder operation is equivalent to multiplying the 1x49 vector I_3 by a 49x49 generator matrix $\mathbf{G}_A$ with "1"s both along and above the main diagonal and "0"s below the main diagonal, such as shown below, and obtaining 1x49 vector I_4 (*i.e.*, the sequence of parity bits) as a result. (*Id.*; *see also* Ex. 1009, 44 ("the

[6] The I_4 sequence contains a typographical error and is missing the 49th bit, which is a "0" bit. (Ex. 1002, ¶62 n.5.)

encoding operation [of a linear block code] is represented mathematically as **v = u · G**, where **v** is a vector of the encoded data bits, **u** is a vector of *k* information bits, and **G** is the *generator matrix*" (emphasis in original)), 45 (describing a nonsystematic code as one that does not contain a *k* x *k* identity matrix)[7].)

$$\mathbf{G}_A = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \\ 0 & 1 & 1 & \cdots & 1 \\ 0 & 0 & 1 & \cdots & 1 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \end{bmatrix}$$

(Ex. 1002, ¶63.) For such a nonsystematic linear block code, the bits of the codeword are parity bits. (*See* Ex. 1009, 45 (describing a nonsystematic code as having parity digits, and its corresponding generator matrix as being a matrix of parity-check coefficients); Ex. 1002, ¶63.)

Furthermore, "each parity bit 'x_j' in the sequence" I_4 is represented by "the formula $x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)a+i}$ where 'x_{j-1}' is the value of a parity bit 'j-1,' and '$\sum_{i=1}^{a} v_{(j-1)a+i}$' is the value of a sum of 'a' randomly chosen irregular repeats of the message bits." (Ex. 1002, ¶64.) As described above, in the precoder step, each parity bit of I_4 is generated by taking the mod-2 sum (which is implemented using an exclusive-OR 'XOR' operation) of the previous parity bit of I_4 and the current bit

[7] *See* n.1.

of I_3. (*Id.*) That is, the jth bit of I_4 ("x_j") equals the mod-2 sum of the "j-1"th bit of I_4 ("x_{j-1}") and the jth bit of I_3: $x_j = x_{j-1} + [jth\ bit\ of\ I_3]$. (*Id.*)

The jth bit of I_3 is equal to $\sum_{i=1}^{a} v_{(j-1)a+i}$, *i.e.*, "a sum of 'a' randomly chosen irregular repeats of the message bits." (*Id.*, ¶65.) As described above, in the first encoding step, each 4-bit block of I_1 is multiplied by generator matrix **G**, and this process comprises irregular repetition of the message bits under the claim construction of "repeat" affirmed by the Federal Circuit in the *Broadcom* litigation. (*See* Section VIII.A; Ex. 1002, ¶65.) As discussed *supra* Section VIII.A, the Federal Circuit found that passing an input message bit through an AND gate when the other input is a "1" bit comprises "repeating" the message bit. (Section VIII.A.) Multiplying a binary message bit by a "1" bit is equivalent to passing the message bit through an AND gate with a "1" bit, and thus under this construction of "repeat," multiplying an message bit by a "1" bit comprises "repeating" the message bit. (Ex. 1002, ¶65; *see also* Ex. 1009, 7-8 (disclosing that binary/modulo-2 multiplication is equivalent to a bitwise AND operation).) Accordingly, under this construction, any type of linear code using a non-zero generator matrix will "repeat" input bits because the process of multiplying a vector of message bits by the generator matrix will necessarily involve multiplying input bits by "1" bits. (Ex. 1002, ¶65.)

For example, as described above, *Kobayashi*'s Hamming encoder multiplies each 4-bit block of I_1 by the 4x7 generator matrix **G**, resulting in seven 7-bit

codewords. (*Id.*, ¶66.) This encoding step performs *repetition* of each and every message bit because the process of multiplying each 4-bit block by generator matrix **G** involves multiplying each input bits by at least one "1" bit (*i.e.*, repeating the input bits) and then summing the repeated bits to generate the codeword. (*Id.*) Moreover, the message bits are repeated irregularly such that message bits are repeated a different number of times. (*Id.*, ¶67.) The example below shows the first 4-bit block of sequence I_1 being multiplied by 4x7 generator matrix **G**, where c_1 through c_4 represent the first four message bits of I_1. (*Id.*) As shown, the first, second, and fourth bits of the block are "repeated" (multiplied by a "1" bit) three times because the first, second, and fourth rows of generator matrix **G** each have three "1"s (in blue). (*Id.*) However, the third bit of the sub-block is repeated *four* times because the third row of generator matrix **G** has four "1"s (in yellow). (*Id.*) The 7-bit codeword is comprised of seven sums of "a" irregular repeats of the message bits, where a=1 (first four bits) and a=3 (last three bits). (*Id.*)

$$[c_1 \quad c_2 \quad c_3 \quad c_4]\begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix} =$$

$$\begin{bmatrix} c_1(1)+c_2(0)+c_3(0)+c_4(0) \\ c_1(0)+c_2(1)+c_3(0)+c_4(0) \\ c_1(0)+c_2(0)+c_3(1)+c_4(0) \\ c_1(0)+c_2(0)+c_3(0)+c_4(1) \\ c_1(1)+c_2(0)+c_3(1)+c_4(1) \\ c_1(1)+c_2(1)+c_3(1)+c_4(0) \\ c_1(0)+c_2(1)+c_3(1)+c_4(1) \end{bmatrix}^T = \begin{bmatrix} c_1 \\ c_2 \\ c_3 \\ c_4 \\ c_1+c_3+c_4 \\ c_1+c_2+c_3 \\ c_2+c_3+c_4 \end{bmatrix}^T$$

(*Id.*)

When the full 28-bit sequence I_1 is encoded via the Hamming encoder, the 3rd, 7th, 11th, 15th, 19th, 23rd, and 27th bits are repeated four times, while the other 21 bits are repeated three times. (*Id.*, ¶68.) Each of the 49 bits of sequence I_2 is thus "a sum of 'a' . . . irregular repeats of the message bits," where a=1 (no highlighting)[8] or a=3 (green highlighting), as shown below. (*Id.*)

> I_1 = (c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}, c_{11}, c_{12}, c_{13}, c_{14}, c_{15}, c_{16}, c_{17}, c_{18}, c_{19}, c_{20}, c_{21}, c_{22}, c_{23}, c_{24}, c_{25}, c_{26}, c_{27}, c_{28})
>
> I_2 = (c_1, c_2, c_3, c_4, $c_1+c_3+c_4$, $c_1+c_2+c_3$, $c_2+c_3+c_4$, c_5, c_6, c_7, c_8, $c_5+c_7+c_8$, $c_5+c_6+c_7$, $c_6+c_7+c_8$, c_9, c_{10}, c_{11}, c_{12}, $c_9+c_{11}+c_{12}$, $c_9+c_{10}+c_{11}$, $c_{10}+c_{11}+c_{12}$, c_{13}, c_{14}, c_{15}, c_{16}, $c_{13}+c_{15}+c_{16}$, $c_{13}+c_{14}+c_{15}$, $c_{14}+c_{15}+c_{16}$, c_{17}, c_{18}, c_{19}, c_{20}, $c_{17}+c_{19}+c_{20}$, $c_{17}+c_{18}+c_{19}$, $c_{18}+c_{19}+c_{20}$, c_{21}, c_{22}, c_{23}, c_{24}, $c_{21}+c_{23}+c_{24}$, $c_{21}+c_{22}+c_{23}$, $c_{22}+c_{23}+c_{24}$, c_{25}, c_{26}, c_{27}, c_{28}, $c_{25}+c_{27}+c_{28}$, $c_{25}+c_{26}+c_{27}$, $c_{26}+c_{27}+c_{28}$)

The interleaver π permutes the sequence I_2 to result in sequence I_3, as shown below. (*Id.*, ¶69.) The interleaver does not otherwise alter the bits of I_2, and thus

[8] The specification admits "a" can be 1. (Ex. 1001, 4:42-45 ("IRA codes with a=1").)

each bit of I_3 is still "a sum of 'a' . . . irregular repeats of the message bits," where a=1 (no highlighting) or a=3 (green highlighting), as shown below. (*Id.*, ¶69.)

$$\pi = \begin{bmatrix} c_1 & c_2 & c_3 & c_4 & c_1+c_3+c_4 & c_1+c_2+c_3 & c_2+c_3+c_4 \\ c_5 & c_6 & c_7 & c_8 & c_5+c_7+c_8 & c_5+c_6+c_7 & c_6+c_7+c_8 \\ c_9 & c_{10} & c_{11} & c_{12} & c_9+c_{11}+c_{12} & c_9+c_{10}+c_{11} & c_{10}+c_{11}+c_{12} \\ c_{13} & c_{14} & c_{15} & c_{16} & c_{13}+c_{15}+c_{16} & c_{13}+c_{14}+c_{15} & c_{14}+c_{15}+c_{16} \\ c_{17} & c_{18} & c_{19} & c_{20} & c_{17}+c_{19}+c_{20} & c_{17}+c_{18}+c_{19} & c_{18}+c_{19}+c_{20} \\ c_{21} & c_{22} & c_{23} & c_{24} & c_{21}+c_{23}+c_{24} & c_{21}+c_{22}+c_{23} & c_{22}+c_{23}+c_{24} \\ c_{25} & c_{26} & c_{27} & c_{28} & c_{25}+c_{27}+c_{28} & c_{25}+c_{26}+c_{27} & c_{26}+c_{27}+c_{28} \end{bmatrix}$$

$I_3 = (c_1, c_5, c_9, c_{13}, c_{17}, c_{21}, c_{25}, c_2, c_6, c_{10}, c_{14}, c_{18}, c_{22}, c_{26}, c_3, c_7, c_{11}, c_{15}, c_{19}, c_{23}, c_{27}, c_4, c_8, c_{12}, c_{16}, c_{20}, c_{24}, c_{28}, c_1+c_3+c_4, c_5+c_7+c_8, c_9+c_{11}+c_{12}, c_{13}+c_{15}+c_{16}, c_{17}+c_{19}+c_{20}, c_{21}+c_{23}+c_{24}, c_{25}+c_{27}+c_{28}, c_1+c_2+c_3, c_5+c_6+c_7, c_9+c_{10}+c_{11}, c_{13}+c_{14}+c_{15}, c_{17}+c_{18}+c_{19}, c_{21}+c_{22}+c_{23}, c_{25}+c_{26}+c_{27}, c_2+c_3+c_4, c_6+c_7+c_8, c_{10}+c_{11}+c_{12}, c_{14}+c_{15}+c_{16}, c_{18}+c_{19}+c_{20}, c_{22}+c_{23}+c_{24}, c_{26}+c_{27}+c_{28})$

Each bit in sequence I_3 is also "a sum of 'a' *randomly chosen* irregular repeats of the message bits" because the message bits are irregularly repeated and permuted according to an arbitrary pattern, *i.e.*, the pattern implied by the combination of *Kobayashi*'s Hamming code and interleaver. (*See* Ex. 1002, ¶70 (explaining that "randomly chosen irregular repeats" encompasses irregularly repeated bits chosen according to a pseudo-random or arbitrary pattern in order for the decoder to properly function); *see also* Ex. 1001, 3:25-29 ('032 patent similarly disclosing interleaver 204 as performing a "pseudo-random permutation" of the irregularly repeated message bits), 3:52-55 (describing the "the arbitrary permutations" of "permutation block 310"—shown in Fig. 3 as "random permutation"—as "correspond[ing] to the scrambling performed by the interleaver 204").)

Thus, every bit of I_3 is equal to $\sum_{i=1}^{a} v_{(j-1)a+i}$, *i.e.*, "the value of a sum of 'a' randomly chosen irregular repeats of the message bits." (*Id.*, ¶71.) When the full "sequence of parity bits" I_4 is generated by using the I_3 sequence as input to the precoder operation, "each parity bit 'x_j' in the sequence is in accordance with the formula $x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)a+i}$," for a=1 and a=3, as shown below. (*Id.*)

$$Assuming\ x_0 = 0,$$

$$x_1 = x_0 + c_1$$

$$\vdots$$

$$x_{28} = x_{27} + c_{28}$$

$$x_{29} = x_{28} + (c_1 + c_3 + c_4)$$

$$\vdots$$

$$x_{49} = x_{48} + (c_{26} + c_{27} + c_{28})$$

Accordingly, *Kobayashi* discloses claim 1(c). (*Id.*, ¶72.)

d) making the sequence of parity bits available for transmission in a transmission data stream.

Kobayashi discloses these limitations. (Ex. 1002, ¶¶73-74.) For example, *Kobayashi* discloses that the encoded sequence of parity bits I_4 is made available for transmission, and transmitted via duobinary signaling, to a decoder.

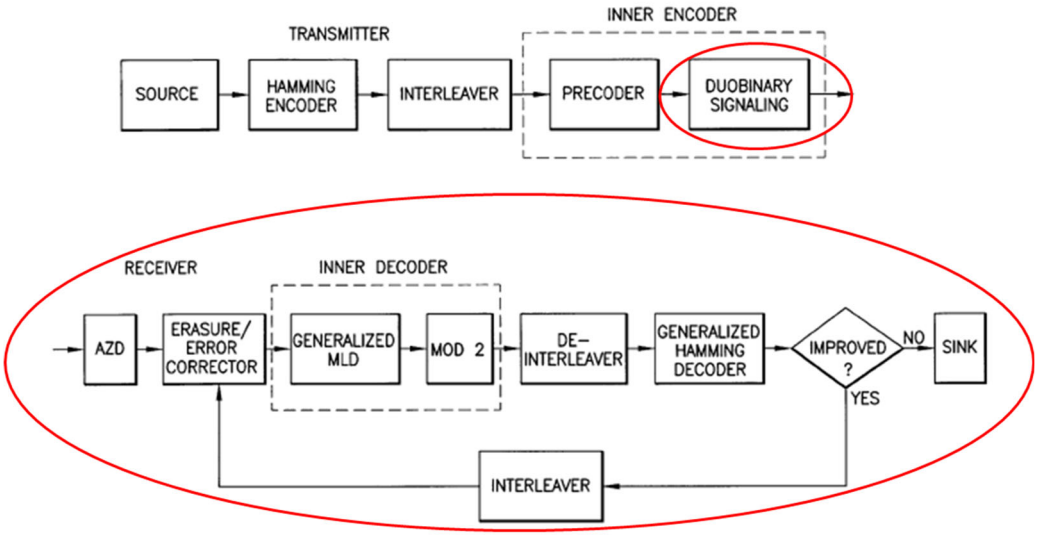


FIG.8

(Ex. 1005, FIG. 8 (annotated); Ex. 1002, ¶73.) Duobinary signaling, which is shown as part of the "inner encoder" in Figure 8 above, is described as the transmission technique for transmitting the sequence of parity bits I_4 to the decoder. (Ex. 1005, 8:25-32, 7:30-31, 7:43-45, 2:21-25; Ex. 1002, ¶73.) *Kobayashi* discloses that the decoder receives the transmission data stream in the form of a duobinary sequence "I_5=(0000000, 0001112, 2112210, 1210122, 1122112, 2111122, 1121000)" after it is transmitted to the decoder via duobinary signaling, but "[b]ecause of channel noise or interference, a received (and sampled) sequence will deviate from the sequence I_5." (Ex. 1005, 8:25-34.)

Accordingly, *Kobayashi* discloses claim 1(d). (Ex. 1002, ¶74.)

2. Claim 3

a) The method of claim 1, wherein the sequence of parity bits is generated is in accordance with "a" varying for different parity bits.

Kobayashi discloses these limitations. (Ex. 1002, ¶75.) As discussed for claim 1(c), the sequence of parity bits is generated in accordance with a=1 and a=3—that is, "a" varies for different parity bits. (Section IX.A.1(c).)

3. Claim 4

a) The method of claim 1, wherein generating the sequence of parity bits comprises performing recursive modulo two addition operations on the random sequence of bits.

Kobayashi discloses these limitations. (Ex. 1002, ¶76.) As discussed for claim 1(c), *Kobayashi* discloses that the precoder generates the sequence of parity bits I_4 by performing modulo-2 addition operations on the random sequence of bits in I_3 and previous parity bits in I_4. (Section IX.A.1(c).) The precoder operation is a recursive operation because it defines each parity bit x_j in terms of preceding bit x_{j-1}. (Ex. 1002, ¶76.)

4. Claim 5

a) The method of claim 1, wherein generating the sequence of parity bits comprises:

b) generating a random sequence of bits that repeats each of the message bits one or more times with the repeats of the message bits being distributed in a random sequence, wherein different fractions of the

message bits are each repeated a different number of times and the number of repeats for each message bit is irregular; and

Kobayashi discloses these limitations. (Ex. 1002, ¶77.) As discussed for claim 1(c), the *Kobayashi* method "generat[es] the sequence of parity bits" I_4 by generating at the conclusion of the interleaver step the permuted sequence I_3, which as discussed is a "random sequence of bits that repeats each of the message bits one or more times with the repeats of the message bits being distributed in a random sequence." (Section IX.A.1(c).) As also discussed for claim 1(c), prior to the interleaving step, the Hamming encoder produces a sequence I_2 of repeated bits, in which the 3rd, 7th, 11th, 15th, 19th, 23rd, and 27th message bits of I_1 are repeated four times, while the other 21 message bits of I_1 are repeated three times. (Section IX.A.1(c).) Thus, "the number of repeats for each message bit is irregular" because 1/4 of the message bits are repeated four times and 3/4 of the message bits are repeated three times (*i.e.*, "different fractions of the message bits are each repeated a different number of times"). (Ex. 1002, ¶77.)

c) XOR summing in linear sequential fashion a predecessor parity bit and "a" bits of the random sequence of bits.

Kobayashi discloses these limitations. (Ex. 1002, ¶¶78-80.) As discussed for claim 1(c), *Kobayashi* discloses that the precoder operation applies a sequential operation ("sequential fashion") that takes a mod-2 sum of the preceding parity bit

of I_4 ("a predecessor parity bit") and a current bit of I_3, which is the sum of "'a' bits of the random sequence of bits." (Section IX.A.1(c).) As further discussed, *Kobayashi* discloses that this precoder operation is implemented using an exclusive OR operation ("XOR summing"). (Section IX.A.1(c).) *Kobayashi* therefore discloses "XOR summing . . . in sequential fashion a predecessor parity bit and 'a' bits of the random sequence of bits." (Ex. 1002, ¶78.)

This precoder operation also XOR sums in "linear [] fashion" because it is a linear operation. (*Id.*, ¶79.) A POSITA would have recognized that a coder, such as *Kobayashi*'s precoder, operates in "linear [] fashion" if it is a linear transformation, *i.e.*, if its operation can be represented as a linear block code. (*Id.*) As explained for Ground 1, claim 1(c), the precoder's operation (*i.e.*, the XOR summing operation described above) can be represented as a (49, 49) linear block code and is thus a linear transformation. (Section IX.A.1(c).) In particular, the precoder's operation is numerically equivalent to a matrix multiplication operation in which the 1x49 vector I_3 is multiplied by a 49x49 generator matrix $\mathbf{G}_A$ below with "1"s both along and above the main diagonal and "0"s below the main diagonal, resulting in 1x49 vector I_4. (Ex. 1002, ¶79; *see also* Ex. 1009, 44 ("the encoding operation [of a linear block code] is represented mathematically as $\mathbf{v} = \mathbf{u} \cdot \mathbf{G}$, where **v** is a vector of the encoded data bits, **u** is a vector of *k* information bits, and **G** is the

generator matrix" (emphasis in original)).) Thus, the precoder's XOR summing operation occurs in a "linear [] fashion."

$$\mathbf{G}_A = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \\ 0 & 1 & 1 & \cdots & 1 \\ 0 & 0 & 1 & \cdots & 1 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \end{bmatrix}$$

(Ex. 1002, ¶79.)

Accordingly, *Kobayashi* discloses claim 5. (*Id.*, ¶80.)

5. Claim 7

a) The method of claim 5, wherein generating the random sequence of bits comprises:

b) producing a block of data bits, wherein different message bits are each repeated a different number of times in a sequence that matches the first sequence; and

Kobayashi discloses these limitations. (Ex. 1002, ¶81.) As discussed for claim 1(c), the first encoding step (Hamming code) involves repetition of each message bit in the first sequence to produce a block of data bits I_2, such that all message bits are repeated, and different message bits are each repeated a different number of times. (Section IX.A.1(c).)

c) randomly permuting the different bits to generate the random sequence.

Kobayashi discloses these limitations. (Ex. 1002, ¶82.) As discussed for claims 1(c) and 5(b), *Kobayashi*'s interleaver performs a permutation action to

generate a random sequence of bits that repeats each one of the message bits one or more times. (Sections IX.A.1(c), IX.A.4(b).) As further discussed, a POSITA would have understood random permutations of bits, as claimed, to encompass pseudo-random or arbitrary permutations of bits, such as performed by *Kobayashi*'s interleaver. (Sections IX.A.1(c), IX.A.4(b).) Accordingly, *Kobayashi* discloses claim 7(d). (Ex. 1002, ¶82.)

6. Claim 8

a) The method of claim 1, further comprising transmitting the sequence of parity bits.

Kobayashi discloses these limitations for the same reasons as explained for claim 1(d), which describes how the *Kobayashi* method both makes the sequence of parity bits available for transmission, and transmits the sequence of parity bits, to the decoder. (Section IX.A.1(d); Ex. 1002, ¶83.)

7. Claim 11

a) A device comprising:

To the extent the preamble of claim 11 is limiting, *Kobayashi* discloses the limitations therein. (Ex. 1002, ¶¶84-85.) For example, *Kobayashi* discloses a concatenated system with both transmitter and receiver portions, wherein the transmitter is "[a] device," as claimed, which receives message bits and encodes the bits using several encoders. (Ex. 1005, FIG. 8, 5:25-27, 7:5-8:34 (describing the transmitter device in the context of Figure 8); Ex. 1002, ¶84.) In particular,

Kobayashi discloses that the device (as shown in Figure 8 below) receives message bits from a source via a packet transmission system; encodes the sequence of message bits using the Hamming encoder, interleaver, and precoder to generate a sequence of parity bits; and transmits the encoded sequence to the receiver via duobinary signaling. (Ex. 1005, 7:5-8:34; Ex. 1002, ¶85.)

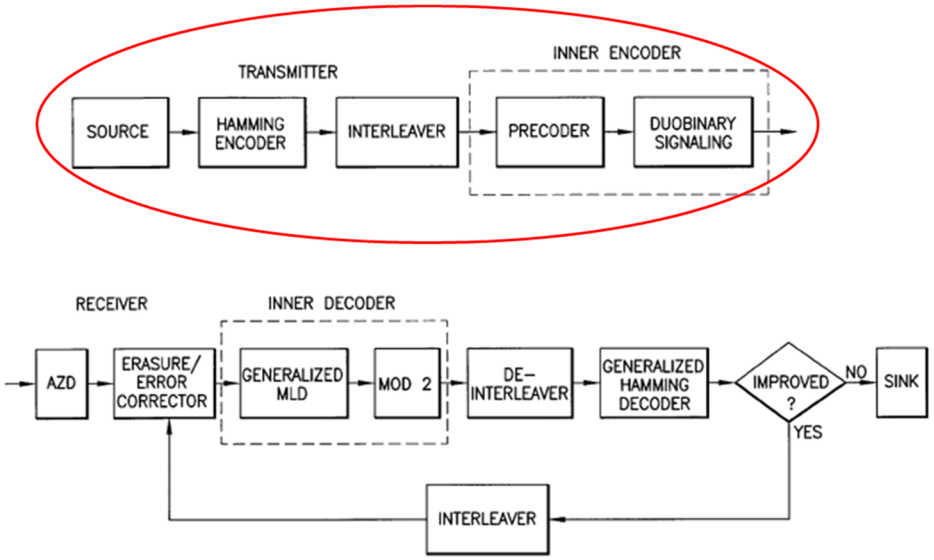


FIG.8

(Ex. 1005, FIG. 8 (annotated); *see also id.*, 5:17-24.)

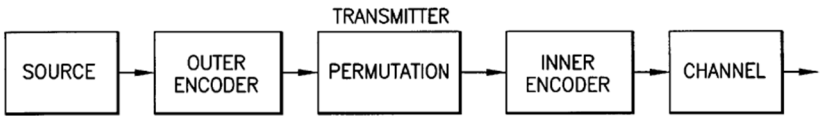


FIG.7A

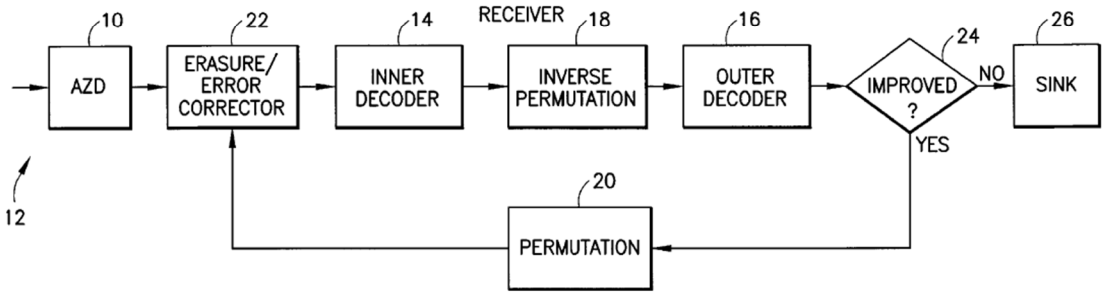
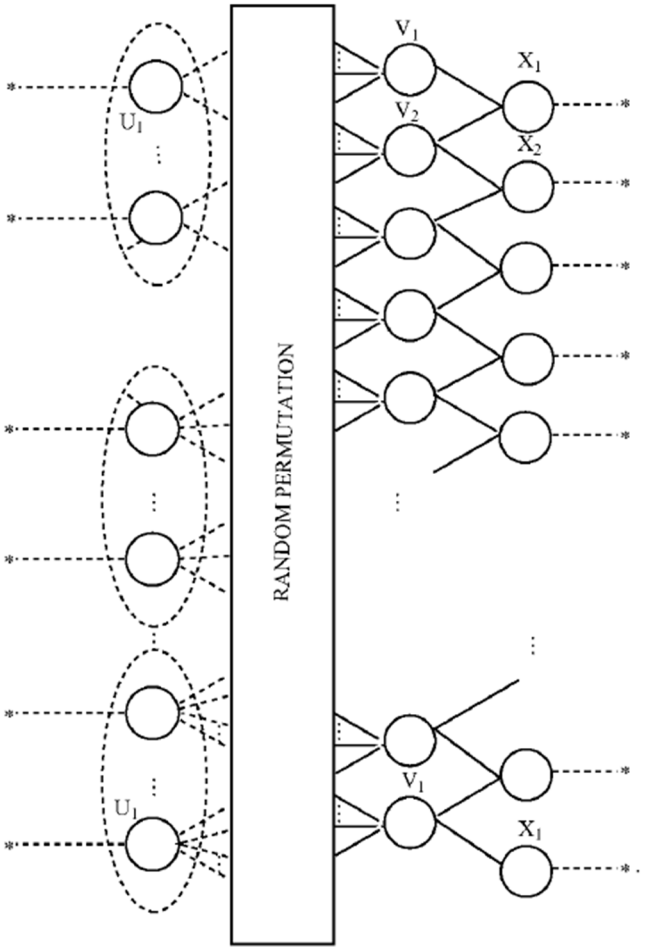


FIG.7B

(*Id.*, FIGS. 7A, 7B (showing generalized versions of the transmitter and receiver sides of Figure 8); Ex. 1002, ¶85.)

b) an encoder configured to receive a collection of message bits and encode the message bits to generate a collection of parity bits in accordance with the following Tanner graph:[9]

[9] Per the CoC appended to the '032 patent, the bottom U_1 of the Tanner graph should read U_k, the bottom V_1 should read V_r, and the bottom X_1 should read X_r. (*See* Ex. 1001.)



Kobayashi discloses these limitations for the same reasons as claim 1. (Ex. 1002, ¶¶86-92.) The '032 Patent explains that the tanner graph of Figure 3 (the same graph appearing in claim 11) "represents" the code expressed as the formula appearing in claim 1. Ex. 1001, 3:65-4:25. As discussed for claim 1(c), *Kobayashi* discloses that the transmitter has an encoding mechanism including a Hamming code, interleaver, and precoder (together, "an encoder" as claimed). (Section IX.A.1(c).) As discussed for claims 1(b) and 1(c), *Kobayashi*'s encoder is "configured to receive a collection of message bits" in the form of 28-bit sequence

I_1, and "encode the message bits to generate a collection of parity bits" in the form of 49-bit sequence I_4. (Sections IX.A.1(b)-(c).)

The encoder operates "in accordance with the [above] Tanner graph"[10] because *Kobayashi*'s Hamming code, interleaver, and precoder, together are an irregular repeat accumulate encoder that corresponds to the claimed Tanner graph. (Ex. 1002, ¶¶87-92.) As discussed for claim 1(c), the encoder irregularly repeats the message bits via a Hamming encoder so that subsets of message bits are repeated different numbers of times. (Section IX.A.1(c).) This irregular repetition corresponds to the dashed lines on the left side of the Tanner graph extending from the message bits (U_j) to the middle box. (Ex. 1002, ¶88.)

Kobayashi's Hamming encoder and interleaver apply a permutation action that randomly connects the irregularly repeated message bits to enforce constraints that determine the parity bits (I_4), which corresponds to the random permutation box and its connections with check nodes (V_j) in the middle of the Tanner graph. (Section IX.A.1(c); Ex. 1002, ¶89.) Indeed, the '032 Patent says the Tanner graph's node "connections correspond to the scrambling performed by the interleaver 204." (Ex. 1001, 3:50-55.)

[10] The '032 Patent states the Tanner graph represents both a "non-systematic" and "systematic" IRA code. (Ex. 1001, 4:19-25.)

Additionally, each parity bit (I_4) is determined as a function of both message/information bits and other parity bits in the same way shown by the configuration of nodes and edges of the right side Tanner graph (*i.e.*, the accumulator). (Section IX.A.1(c).) Specifically, as discussed for claim 1(c), Kobayashi's precoder accumulates the bits of 49-bit sequence I_3, resulting in 49-bit sequence I_4. (*See* Section IX.A.1(c).) This accumulation operation is achieved through the operation $\boldsymbol{x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)a+i}}$ where $\boldsymbol{x_{j-1}}$ is a previous parity bit and $\boldsymbol{\sum_{i=1}^{a} v_{(j-1)a+i}}$ is the output of parity check node V_{j-i} because it is the sum of a randomly chosen irregular repeats of the message/information bits, as shown above for claim 1. (Section IX.A.1(c).). Thus, the accumulation operation corresponds to the right-hand side of the Tanner graph, the accumulator. (Ex. 1002, ¶91.)

8. Claim 12

a) The device of claim 11, wherein the encoder is configured to generate the collection of parity bits as if a number of inputs into nodes v_i was not constant.

Kobayashi discloses these limitations. (Ex. 1002, ¶93.) As discussed for claim 11(b), "the encoder is configured to generate the collection of parity bits" for "a number of inputs into nodes v_i [that is] not constant" because the encoder operates in accordance with a Tanner graph in which the number of inputs equals either one (a=1) or three (a=3). (Section IX.A.7(b).)

9. Claim 14

a) The device of claim 12, wherein the accumulator comprises a recursive convolutional coder.[11]

Kobayashi discloses these limitations. (Ex. 1002, ¶¶94-95.) As discussed for claims 11 and 12, *Kobayashi*'s encoder includes a precoder that performs operations on encoded sequence I_3 by taking the modulo-2 partial sum of the current input of I_3 and the immediately previous output of I_4 (*i.e.*, the modulo-2 partial sum of all previous inputs up to the current input). (*See* Section IX.A.1(d).) The precoder is an "accumulator" that accumulates the bits in sequence I_3 and the precoder's accumulation operation is consistent with that disclosed by the '032 patent. (Ex. 1001, 2:66-3:24; Ex. 1002, ¶94.) The accumulator of the '032 patent is described as a "truncated rate-1 ***recursive convolutional coder*** with the transfer function 1/(1+D)." (Ex. 1001, 3:1-3 (emphasis added).) Accordingly, *Kobayashi*'s precoder is an "accumulator [that] comprises a recursive convolutional coder" as claimed (and is also a truncated rate-1 coder (claim 15) with transfer function 1/(1+D) (claim 16))

[11] There is no antecedent basis for an "accumulator" in claim 12, or in claim 11, from which claim 12 depends. Petitioner thus demonstrates how *Kobayashi* discloses that the "device of claim 12" includes an "accumulator [that] comprises a recursive convolutional coder," without conceding the claim complies with § 112. (Ex. 1002, ¶¶94-95, n.7.)

because the precoder operates in the same manner as the '032 patent's accumulator. (Ex. 1002, ¶95.)

10. Claim 15

a) The device of claim 14, wherein the recursive convolutional coder comprises a truncated rate-1 recursive convolutional coder.

Kobayashi discloses these limitations for the same reasons as explained for claim 14. (Ex. 1002, ¶96.)

11. Claim 16

a) The device of claim 14, wherein the recursive convolutional coder has a transfer function of 1/(1+D).

Kobayashi discloses these limitations for the same reasons as explained for claim 14. (Ex. 1002, ¶97.)

B. Ground 2: Claims 2, 6-7, 10, 13, and 17 Are Obvious Over *Kobayashi*

1. Claim 2

a) The method of claim 1, wherein the sequence of parity bits is generated is in accordance with "a" being constant.

Kobayashi discloses or suggests these limitations. (Ex. 1002, ¶¶98-102.) *Kobayashi*'s overall encoding mechanism is a nonsystematic code that generates 49 parity bits, where a=1 and a=3. (*See* Section IX.A.1(c).) However, it would have been obvious to implement the *Kobayashi* method using a *systematic* encoding mechanism, in which the 28 message bits appear directly in the codeword along with

the 21 parity bits following the 28 message bits. (Ex. 1002, ¶98; Ex. 1009, 45 (describing a "systematic code" as one in which the codeword "can be partitioned into two parts, with one part consisting of the *k*-bit information word and the other part consisting of the $n - k$ parity digits").) For example, the *Kobayashi* method would have been modified to use a systematic encoding mechanism by applying the precoder operation *only* over the last 21 bits of I_3 (highlighted in green below), and replacing the first 28 message bits of I_3 (highlighted in yellow below) with the 28 message bit sequence I_1 (in order, c_1 through c_{28}). (Ex. 1002, ¶99.)

> (unmodified) $I_3 = (c_1, c_5, c_9, c_{13}, c_{17}, c_{21}, c_{25}, c_2, c_6, c_{10}, c_{14}, c_{18}, c_{22}, c_{26}, c_3, c_7, c_{11}, c_{15}, c_{19}, c_{23}, c_{27}, c_4, c_8, c_{12}, c_{16}, c_{20}, c_{24}, c_{28}, c_1 + c_3 + c_4, c_5 + c_7 + c_8, c_9 + c_{11} + c_{12}, c_{13} + c_{15} + c_{16}, c_{17} + c_{19} + c_{20}, c_{21} + c_{23} + c_{24}, c_{25} + c_{27} + c_{28}, c_1 + c_2 + c_3, c_5 + c_6 + c_7, c_9 + c_{10} + c_{11}, c_{13} + c_{14} + c_{15}, c_{17} + c_{18} + c_{19}, c_{21} + c_{22} + c_{23}, c_{25} + c_{26} + c_{27}, c_2 + c_3 + c_4, c_6 + c_7 + c_8, c_{10} + c_{11} + c_{12}, c_{14} + c_{15} + c_{16}, c_{18} + c_{19} + c_{20}, c_{22} + c_{23} + c_{24}, c_{26} + c_{27} + c_{28})$
>
> (modified) $I_4 = (c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}, c_{11}, c_{12}, c_{13}, c_{14}, c_{15}, c_{16}, c_{17}, c_{18}, c_{19}, c_{20}, c_{21}, c_{22}, c_{23}, c_{24}, c_{25}, c_{26}, c_{27}, c_{28}$, [21 parity bits representing the precoder output applied over the last 21 bits of I_3])

The "sequence of parity bits" that is generated by the modified *Kobayashi* method would thus be comprised of the last 21 bits of I_4, rather than the entire sequence of I_4. (*See* Section IX.A.1(c).) As described for claim 1(c), a=3 for this entire 21-bit sequence (*i.e.*, "a" is constant). (Section IX.A.1(c); Ex. 1002, ¶100.)

There are only two types of codes—systematic and non-systematic—and thus a POSITA would have had a "finite number of identified, predictable solutions" and would have had "good reason" to pursue a modification with a systematic code. (Ex.

1002, ¶101.) *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 402 (2007). Moreover, using a systematic code would have been beneficial because the parity bits are merely appended to the sequence of message bits and thus the original input stream would not need to be decoded if the bits are received correctly. (Ex. 1002, ¶101; *see also* Ex. 1010, 54.) A POSITA would have also had the skill to implement, and expectation of success in achieving such a modification because it would have involved nothing more than an application of a known element (systematic code) to a known device (transmitter with concatenated encoders) to yield predictable results (provide an encoded output that includes not only parity bits, but also all of the message bits). (Ex. 1002, ¶102.) *KSR*, 550 U.S. at 416-418.

Accordingly, *Kobayashi* discloses or suggests claim 2. (Ex. 1002, ¶102.)

2. Claim 6

a) The method of claim 5, wherein generating the random sequence of bits comprises coding the collection of message bits using a low-density generator matrix (LDGM) coder.

Kobayashi discloses or suggests these limitations. (Ex. 1002, ¶¶103-113.) As discussed for claim 5(b), *Kobayashi* discloses "generating the random sequence of bits" via a (7, 4) Hamming code and an interleaver. (Section IX.A.4(b).) *Kobayashi* discloses that the (7, 4) Hamming code could be replaced with a different encoder—for example, with a different (n, k) Hamming code, or with a Reed-Solomon or BCH code—and incorporates other references such as the *Lin/Costello* text for further

details on those modified implementations. (Ex. 1005, 7:6-15 (citing the "Lin/Costello or Peterson/Weldon" texts for further details on (n, k) Hamming codes), 11:18-22; Ex. 1002, ¶103.)

A POSITA would have thus been motivated to consult the incorporated *Lin/Costello* reference and would have understood that an (n, k) Hamming code can be implemented for "any positive integer $m \geq 3$," where the code length is $n = 2^m - 1$, the number of information bits is $k = 2^m - m - 1$. (*See, e.g.*, Ex. 1005, 1:65-67 (providing citation to *Lin/Costello* text (Ex. 1010)); *see also* Ex. 1010, 79.) It would have thus been obvious to use a (255, 247) Hamming code (*i.e.*, m = 8) instead of using a (7, 4) Hamming code (*i.e.*, m = 3) as part of the "first encoding operation." (Ex. 1002, ¶104.) A POSITA would have recognized a benefit of making this modification to be an increase in the code rate, from a rate of 4/7 for the (7, 4) Hamming code to a rate of 247/255 for the (255, 247) Hamming code, and that such an increase in code rate translates to better spectral efficiency; *i.e.*, relatively more of the transmission corresponds to data and less of the transmission must be used on the overhead of transmitting parity bits. (*Id.*, ¶105.) A POSITA would have had the expectation of success in achieving such a modification because it would have involved an application of a known element ((255, 247) Hamming code) to a known device (*Kobayashi*'s transmitter that uses a (7, 4) Hamming code and interleaver to generate a random sequence of bits) to yield predictable results (generate a random

sequence of bits using a (255, 247) Hamming code and interleaver). (*Id.*) *KSR*, 550 U.S. at 416-418.

For this modified *Kobayashi* method, the systematic generator matrix **G** for a (255, 247) Hamming code is a 247x255 matrix comprised of two submatrices: a 247x247 identity matrix, and a 247x8 submatrix $\mathbf{Q}^T$ in which the 247 rows are the 247 nonzero *m*-tuples (eight-tuples) of weight 2 or more. (Ex. 1002, ¶106; Ex. 1010, 79-80 (disclosing that the generator matrix consists of a "$(2^m – m – 1)$ x $(2^m – m – 1)$ identity matrix" and the "transpose of **Q**" (*i.e.*, $\mathbf{Q}^T$), where "submatrix **Q** consists of $2^m – m – 1$ columns which are the *m*-tuples of weight 2 or more").) This generator matrix **G** has a density of approximately 2% because the 247x247 identity matrix has 247 "1"s, and because the transpose of **Q**, *i.e.*, the 247x8 matrix $\mathbf{Q}^T$, has rows consisting of the 28 eight-tuples of weight 2; 56 eight-tuples of weight 3; 70 eight-tuples of weight 4; 56 eight-tuples of weight 5; 28 eight-tuples of weight 6; 8 eight-tuples of weight 7; and 1 eight-tuple of weight 8. (Ex. 1002, ¶106.) A POSITA would have understood 2% to be low-density, and would have recognized that a Hamming code is a "generator matrix . . . coder." (*Id.*, ¶107.) Moreover, a density of 2% is within the density range that PO alleges corresponds to low-density generator matrices. (Ex. 1018, 40.)

With such a modification, the modified *Kobayashi* method would still operate according to the equation of claim 1(c), but with message bits irregularly repeated a

different number of times, and with a different value of "a." (*See* Sections IX.A.1(c), IX.A.4(b); Ex. 1002, ¶108.) As Dr. Valenti explains, such a modification would have still had "irregular repeats of the message bits," *see* Section IX.A.1(c), and would have still "repeat[ed] each of the message bits one or more times . . . wherein different fractions of the message bits are each repeated a different number of times and the number of repeats for each message bit is irregular," *see* Section IX.A.4(b). (Ex. 1002, ¶109.) The modified *Kobayashi* method would have also still met the equation of claim 1(c), but for a=1 and a=127. (Section IX.A.1(c); Ex. 1002, ¶¶110-111.) Furthermore, for claim 5(b), the modified *Kobayashi* method would have still "generat[ed] a random sequence of bits . . . with the repeats of the message bits being distributed in a random sequence" because the interleaver operation would still be applied. (Section IX.A.4(b); Ex. 1002, ¶112.)

Accordingly, *Kobayashi* discloses or suggests claim 6. (Ex. 1002, ¶113.)

3. Claim 7

a) The method of claim 5, wherein generating the random sequence of bits comprises:

b) producing a block of data bits, wherein different message bits are each repeated a different number of times in a sequence that matches the first sequence; and

Kobayashi discloses or suggests these limitations for the same reasons explained for Ground 1, claims 7(a)-(b). (Section IX.A.5(a)-(b); Ex. 1002, ¶¶114-

117.) To the extent it is argued that *Kobayashi* does not disclose that "different message bits are each repeated . . . *in a sequence that matches the first sequence*," it would have been obvious to implement the (7, 4) Hamming code, which performs the irregular repetition, using known methods for matrix multiplication to multiply the blocks of sequence I_1 by generator matrix **G**. (Ex. 1002, ¶114.)

For example, the below code fragment is an example of a matrix multiplication method known at the time of the alleged invention for implementing an (n, k) linear block code, such as *Kobayashi*'s (7, 4) Hamming code. (Ex. 1006, 44-45.)

```
/*****************************************/

for( i=0; i<n; i++){
     v[i] =0;
     for( j=0; j<k; j++ ) {
          v[i] = v[i] ^ (u[j] & g[j][i]);
          }
     }
/*  end of fragment  */
/*****************************************/
```

(*Id.*, 45[12]; Ex. 1002, ¶115.) The C code fragment reflects an "encoding operation" that may be "represented mathematically as $\mathbf{v} = \mathbf{u} \cdot \mathbf{G}$, where **v** is a vector of the encoded bits, **u** is a vector of *k* information bits, and **G** is the *generator matrix*," and

[12] *See* n.1.

where **v** is an *n*-bit vector, **u** is a *k*-bit vector, and **G** is a *k* x *n* generator matrix. (Ex. 1006, 44 (emphasis in original).)

The inner loop of the fragment increments j sequentially, and thus iterates sequentially over the sequence of message bits in order to generate the repeated bits. (Ex. 1002, ¶116.) Thus, when implementing *Kobayashi* method's Hamming code using a similar known matrix multiplication method, the "different message bits are each repeated a different number of times in a sequence that matches the first sequence" because the repeated bits are generated in an order corresponding to the order of the first sequence. (*Id.*) A POSITA would have had the skill to implement, and expectation of success in achieving such a modification because it would have involved nothing more than an application of a known method (matrix multiplication methods for linear block codes) to a known device (*Kobayashi*'s encoder that uses a linear block code (Hamming code)) to yield predictable results (provide an encoder that uses known matrix multiplication methods for linear block codes to implement the Hamming code). (*Id.*, ¶117.) *KSR*, 550 U.S. at 416-418.

c) randomly permuting the different bits to generate the random sequence.

Kobayashi discloses these limitations for the same reasons explained for Ground 1, claim 7(c). (Section IX.A.5(c); Ex. 1002, ¶118.)

4. Claim 10

a) The method of claim 8, wherein transmitting the sequence of parity bits comprises transmitting the sequence of parity bits as part of a systematic code.

Kobayashi discloses or suggests these limitations for the same reasons as explained for Ground 2, claim 2, which describes how a POSITA would have found it obvious to modify the *Kobayashi* method so that the sequence of parity bits is generated as part of a systematic code, and for Ground 1, claims 1(d) and 8, which describe how the method comprises transmitting the sequence of parity bits as part of a code. (Section IX.B.1; *see also* Section IX.A.1(d), IX.A.6; Ex. 1002, ¶119.) As another example, the information bits can simply be prepended to Kobayashi's 49 bit codeword, without modifying the encoding process for the parity bits, as was most commonly done in the prior art. (Ex. 1009, 45; Ex. 1005, 7:53-63; Ex. 1002, ¶119.)

5. Claim 13

a) The device of claim 11, wherein the encoder comprises:

b) a low-density generator matrix (LDGM) coder configured to perform an irregular repeat on message bits having a first sequence in a source data stream to output a random sequence of repeats of the message bits; and

Kobayashi discloses or suggests these limitations. (Ex. 1002, ¶120.) As discussed for Ground 2, claim 6, *Kobayashi* teaches using a "low-density generator

matrix (LDGM) coder to perform an irregular repeat on [the] message bits" of sequence I_1 and "output a random sequence of repeats of the message bits." (Section IX.B.2.) As discussed for Ground 1, claim 1(b), the "message bits hav[e] a first sequence in a source data stream." (Section IX.A.1(b).)

c) an accumulator configured to XOR sum in linear sequential fashion a predecessor parity bit and "a" bits of the random sequence of repeats of the message bits.

Kobayashi discloses or suggests these limitations. (Ex. 1002, ¶121.) As discussed for Ground 1, claim 5(c), the *Kobayashi* transmitter includes a precoder that "XOR sum[s] in linear sequential fashion a predecessor parity bit and 'a' bits of the random sequence of repeats of the message bits." (Section IX.A.4(c).) And as discussed for Ground 1, claim 14, *Kobayashi*'s precoder is an "accumulator." (Section IX.A.9.)

6. Claim 17

a) The device of claim 12, further comprising a second accumulator configured to determine a second sequence of parity bits that defines a second condition that constrains the random sequence of repeats of the message bits.[13]

Kobayashi discloses or suggests these limitations. (Ex. 1002, ¶122.) *Kobayashi* discloses that "[t]he invention can be extended to a concatenated system with three or more encoders." (Ex. 1005, 12:4-5.) A POSITA would have been motivated to add a second accumulator (in addition to the precoder (first accumulator), *see* Section IX.A.9) to the *Kobayashi* transmitter as a third encoder. (Ex. 1002, ¶122.) A POSITA would have appreciated the benefits of such an implementation because *Kobayashi* discloses that concatenating multiple error correcting codes may allow a receiver to "achieve a higher performance" in identifying errors in the received sequence. (Ex. 1005, 1:26-48.) An additional precoder provides the benefit of increasing error correcting performance without significantly increasing complexity of the encoder or decoder. (Ex. 1005, 7:30-32; Ex. 1002, ¶122.) Moreover, it would have been obvious to add another accumulator to the *Kobayashi* transmitter because *Kobayashi* provides examples of only two

[13] There is no antecedent basis for an "accumulator" in claim 12, or in claim 11, from which claim 12 depends. *See* n.11. (Ex. 1002, ¶¶122-123, n.10.)

types of encoders: a Hamming encoder, and an accumulator (the precoder). (Ex. 1002, ¶122; *see also* Ex. 1005, 7:46-8:27.) Accordingly, a POSITA would have had a "finite number of identified, predictable solutions" and would have had "good reason" to pursue a modification with a second accumulator. (Ex. 1002, ¶122.) *KSR*, 550 U.S. at 402.

A POSITA would have had a reasonable expectation of success in implementing such a modification because *Kobayashi* discloses that such a modification would have been both possible and beneficial. (Ex. 1002, ¶123.) A POSITA would have also had the skill to implement, and expectation of success in achieving such a modification because it would have involved nothing more than an application of a known element (accumulator) to a known device (*Kobayashi*'s transmitter with a Hamming code and accumulator) to yield predictable results (provide a concatenated system with an outer encoder comprising a Hamming code and an inner encoder comprising two accumulators). (*Id.*) *KSR*, 550 U.S. at 416-18.

C. Ground 3: Claims 6, 13, and 18-22 Are Obvious Over *Kobayashi* and *McEliece*

1. Motivation to Combine

A POSITA would have found it obvious to combine *Kobayashi* and *McEliece* in the manners discussed below.

First, it would have been obvious to modify the *Kobayashi* coding system so that the *Kobayashi* decoder is replaced with an iterative belief propagation decoder similar to that disclosed by *McEliece*. As explained for claim 1(a) *Kobayashi* discloses that its receiver is a decoder (shown below) which decodes the precoder's output. (Ex. 1005, 6:16-7:4 (describing the general decoding technique), 7:28-11:17.)

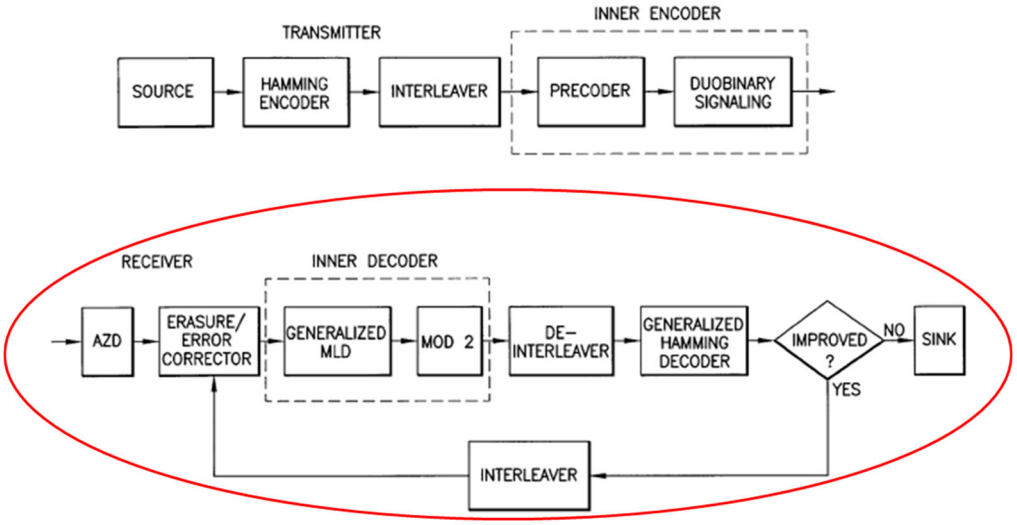


FIG.8

(*Id.*, FIG. 8 (annotated); Ex. 1002, ¶125.)

McEliece discloses a decoding algorithm called "Pearl's belief propagation algorithm," which "solves the probabilistic inference problem in many important special cases." (Ex. 1006, 144.) *McEliece* describes the probabilistic inference problem as follows. (*Id.*; Ex. 1002, ¶126.) "[L]et $X = \{X_1, X_2, \ldots, X_N\}$[5] be a set of N discrete variables, where X_i assumes values in the finite alphabet A_i." (Ex. 1006,

144.) *McEliece* defines the joint density function as shown below, *i.e.*, "a mapping from A_1 x … x A_N into the set of real numbers *R*." (*Id.*)

$$p(x) = p(x_1, x_2, \dots, x_N) \stackrel{\text{def}}{=} \Pr\{X_1 = x_1, \dots, X_N = x_N\}$$

(*Id.*) "[A]ssum[ing] that the marginal densities $p(x_i) \stackrel{\text{def}}{=} \Pr\{X_i = x_i\}$ are also known," then "[t]he marginal density function $p(x_i)$ represents our *a priori* 'belief' about the random variable X_i." (*Id.*) If "one or more of these random variables is measured or 'observed' . . . [then] there is a subset $J \subseteq \{1, 2, \dots, N\}$ (the evidence set) such that, for all $j \in J$, the random variable X_j is known to have a particular value, say a_j." (*Id.*) *McEliece* discloses "[t]he *evidence* is then defined to be the event $\mathcal{E} = \{X_j = a_j : j \in J\}$," and "[t]he fundamental *probabilistic inference problem* is to compute the *updated beliefs*, i.e., the *a posteriori* or conditional probabilities $p(X_i|\mathcal{E})$, for all $i \notin J$." (*Id.* (emphasis in original).)

A "'Bayesian belief network' approach . . . to the inference problem is to exploit any 'partial independencies' which may exist among the X_i's to simplify belief updating." (*Id.*) These "partial independencies can be described by a *directed acyclic graph*, or DAG," which is "a finite, directed graph, in which there are no directed cycles." (*Id.* (emphasis in original).) Suppose "*G* is a DAG, and . . . *X* is a set of random variables in one-to-one correspondence with the vertices of *G*." (*Id.*) Additionally, suppose that if *G* has a "directed edge $a \rightarrow b$, then *a* will be called a

'parent' of *b*, and *b* will be called a 'child' of *a*." (*Id.*) Then a "DAG, together with the associated random variables *X*, is called a *Bayesian belief network*, or *Bayesian network* for short." (*Id.*, 145 (emphasis in original); Ex. 1002, ¶127.)

McEliece discloses that "Bayesian networks can sometimes lead to considerable simplifications of the probabilistic inference problem," such as "Pearl's *belief propagation* algorithm." (Ex. 1006, 145 (emphasis in original).) *McEliece* further discloses that "Pearl's belief propagation algorithm is a decentralized 'message-passing' algorithm, in which there is a processor associated with each vertex of *G*" and "[e]ach processor can communicate only with its parents and children." (*Id.*, 146.) The general principle underlying Pearl's belief propagation algorithm is that "[w]hen a processor is activated, it 'reads' the messages received from each of its parents and children, updates its belief based on these messages, and then sends new messages back to its parents and children." (*Id.*) *McEliece* discloses that processors may also update their beliefs in parallel. (*Id.*, 148; Ex. 1002, ¶128.)

McEliece discloses advantageous uses of Pearl's belief propagation algorithm, which can be "used to derive effective iterative decoding algorithms for a number of . . . error-control systems, including . . . serially concatenated codes." (Ex. 1006, 140; Ex. 1002, ¶129.) *McEliece* describes these belief propagation ("BP") decoding algorithms as "remarkably effective" and notes that "belief propagation provides an attractive general method for devising low-complexity iterative decoding algorithms

for hybrid coded systems." (Ex. 1006, 140.) In particular, *McEliece* discloses that "decoding algorithms [for serially concatenated codes] can be derived routinely from a BP viewpoint, using the network of Fig. 12." (*Id.*, 149.)

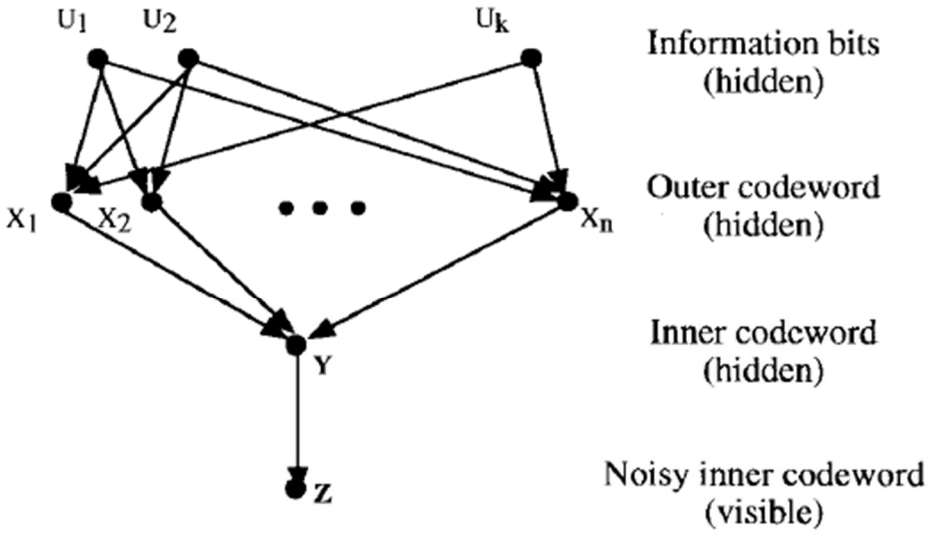


Fig. 12. Belief network for decoding a pair of serially concatenated codes.

(*Id.*, 150 (FIG. 12).)

It would have therefore been obvious to modify *Kobayashi*'s serially concatenated system to include a decoding technique similar to that disclosed by *McEliece*, rather than *Kobayashi*'s decoding technique, to take advantage of the belief propagation algorithms' benefits. (Ex. 1002, ¶130.) A POSITA would have had a reasonable expectation of success in implementing such a modification because *McEliece* discloses that such a modification would have been both possible and beneficial. (*Id.*) A POSITA would have also had an expectation of success in achieving such a modification because it would have involved nothing more than an

application of a known element (belief propagation decoder) to a known device (*Kobayashi*'s serially concatenated system with a decoder) to yield predictable results (provide a serially concatenated system with a belief propagation decoder). (*Id.*) *KSR*, 550 U.S. at 416-418.

Second, it would have been obvious to modify *Kobayashi* in view of *McEliece* to implement *Kobayashi*'s outer encoding step (*e.g.*, the Hamming encoder) using a low-density generator matrix transformation. (Ex. 1002, ¶124.) Both *Kobayashi* and *McEliece* relate to the design and implementation of linear, error-correcting codes. (Ex. 1002, ¶132.) A POSITA would have been motivated by the benefits of using a low-density generator matrix codes. For example, an LDGM achieves low-complexity encoding (due to its sparse graph), is able to be encoded in linear time, and requires fewer logic gates (or software operations) thus reducing cost of the encoder, especially when the desired coding rate is lower than 1/2. (*Ex. 1002, ¶132; Ex. 1011, 23.*) LDGMs were known to have good error correction performance—within 1 dB of channel capacity. (*Id.*) Indeed, a POSITA would have known LDGMs had similar results as alternative high performance prior art codes, LDPC and turbo coding, but with lower complexity. *Id.* LDGMs can also be decoded in a distributed parallel fashion, which can decrease decoding time and increase efficiency, making them "more suitable for practical applications." (*Ex. 1002, ¶132; Ex. 1011, 23.*)

McEliece further discloses that Pearl's belief propagation algorithm can be "used to derive effective iterative decoding algorithms for . . . the recently introduced low-density generator matrix codes." (Ex. 1006, 140; Ex. 1002, ¶131.) In particular, *McEliece* discloses using "BP decoding on certain systematic linear block codes with low-density *generator matrices*," and discloses a small number of options for the low-density generator matrix, including classes of block codes constructed by *MacKay* and *Cheng*. (Ex. 1006, 149 (emphasis in original); *see also, e.g.*, Ex. 1007 ("*MacKay*"); Ex. 1011 ("*Cheng I*"), Ex. 1012 ("*Cheng II*").)[14] A POSITA would have had a "finite number of identified, predictable solutions" and would have had "good reason" to pursue a modification with any of the solutions, such as, for example, *MacKay*'s low-density generator matrix code. (Ex. 1002, ¶131.) *KSR*, 550 U.S. at 402.

The *MacKay* paper derives an algorithm for inference problems in modulo-2 arithmetic and applies it to decoding systematic linear block codes with low-density generator matrices. (Ex. 1007, 179, 192; Ex. 1002, ¶132.) *MacKay* discloses the use of a random sparse generator matrix **A** where "[t]he first *N* lines of A were set to the identity matrix, and of the remaining bits, a fraction f_A were randomly set to

[14] Petitioner's reference to "*Cheng*" refers to the collective disclosures of *Cheng I* and *Cheng II* cited in *McEliece* to discuss the state of the art. *See* n.1.

1." (Ex. 1007, 185-86.) This low-density generator matrix "can be viewed as defining a systematic error correcting code in which the signal s is transmitted, followed by ($M - N$) sparse parity checks." (*Id.*, 185.) *MacKay* demonstrates results for vector length N set to 50; number of measurements M set to 500, 1000, and 2000; density f_A varying from 0.05 to 0.50; and varying noise levels. (*Id.*, 185-86.)

McEliece discusses the benefits of using low-density generator matrix codes along with a belief propagation decoder, noting that "[t]he decoding algorithm['s] . . . results were quite good, especially at high rates." (Ex. 1006, 149; Ex. 1002, ¶133.) Moreover, "these same ideas [were used] to construct a class of block codes which yield some remarkably efficient multilevel coded modulations." Figure 11 below "shows the belief network for low-density generator matrix codes." (Ex. 1006, 149.)

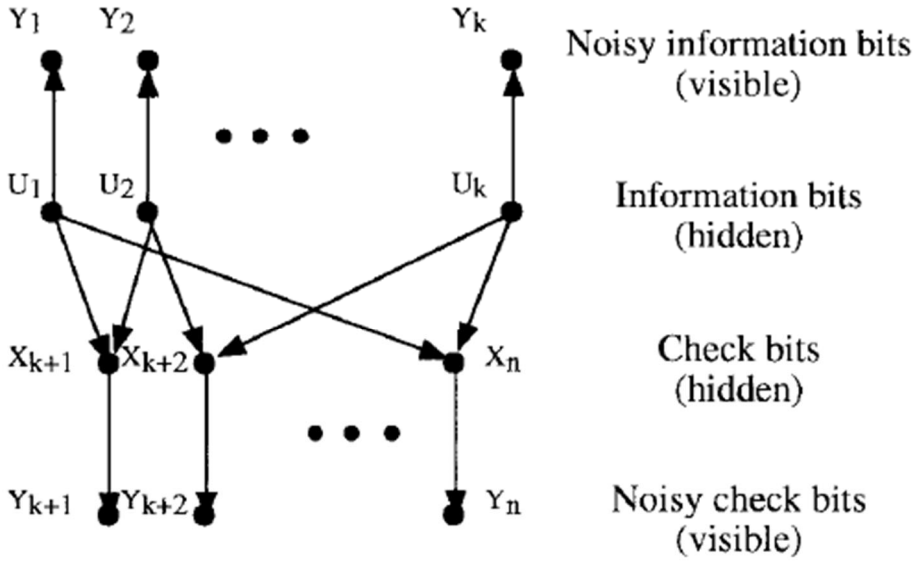


Fig. 11. Belief network for decoding systematic, low-density generator matrix codes.

(*Id.*, 149 (FIG. 11); Ex. 1002, ¶134.)

Given that the Hamming encoder of the *Kobayashi* is a systematic linear block code with a generator matrix, it would have been obvious to further modify the *Kobayashi-McEliece* method to use a systematic linear block code with a *low-density* generator matrix instead. (Ex. 1002, ¶135.) This would have allowed taking advantage of the benefits of LDGMS (including those disclosed by *McEliece*) and to further improve the concatenated system. (*Id.*) A POSITA would have had a reasonable expectation of success in implementing such a modification because *McEliece* discloses that such a modification would have been both possible and beneficial. (*Id.*) Such a modification would have involved nothing more than an application of a known element (systematic linear block code with a low-density generator matrix) to a known device (*Kobayashi*'s method that uses a systematic linear block code with a generator matrix as a first encoding step) to yield predictable results (*Kobayashi-McEliece*'s method that has a first encoding step comprised of a systematic linear block code with a low-density generator matrix). (*Id.*) *KSR*, 550 U.S. at 416-418.

2. Claim 6

a) The method of claim 5, wherein generating the random sequence of bits comprises coding the collection of message bits using a low-density generator matrix (LDGM) coder.

Kobayashi in view of *McEliece* discloses or suggests these limitations. (Ex. 1002, ¶¶124-141; *see also id.*, ¶¶49-55.) As discussed above, *Kobayashi* discloses "generating the random sequence of bits" via a (7, 4) Hamming code and an interleaver. (Section IX.A.4(b).) It would have been obvious to modify *Kobayashi* in view of *McEliece* to implement this encoding step using a *low-density* generator matrix transformation. (Section IX.C.1; Ex. 1002, ¶124.)

A POSITA would have understood that the *Kobayashi-McEliece* combination would have still operated according to the equation of claim 1(c), but with message bits irregularly repeated a different number of times, and with a different value of "a." (*See* Sections IX.A.1(c), IX.A.4(b); Ex. 1002, ¶136.) Because the low-density generator matrix disclosed by McEliece and MacKay is randomly created, as Dr. Valenti explains, the *Kobayashi-McEliece* combination would have still had "irregular repeats of the message bits," *see* Section IX.A.1(c), and would have still "repeat[ed] each of the message bits one or more times . . . wherein different fractions of the message bits are each repeated a different number of times and the number of repeats for each message bit is irregular," *see* Section IX.A.4(b). (Ex. 1002, ¶¶137-138.) Moreover, the value of "a" would vary for the same reason. (Ex.

1002, ¶139.) Furthermore, for claim 5(b), the *Kobayashi-McEliece* combination would have still "generat[ed] a random sequence of bits . . . with the repeats of the message bits being distributed in a random sequence" because the interleaver operation would still be applied. (Section IX.A.4(b); Ex. 1002, ¶140.)

Accordingly, the *Kobayashi-McEliece* combination discloses or suggests "generating the random sequence of bits comprises coding the collection of message bits using a low-density generator matrix (LDGM) coder." (Ex. 1002, ¶141.)

3. Claim 13

a) The device of claim 11, wherein the encoder comprises:

b) a low-density generator matrix (LDGM) coder configured to perform an irregular repeat on message bits having a first sequence in a source data stream to output a random sequence of repeats of the message bits; and

The *Kobayashi-McEliece* combination discloses or suggests these limitations. (Ex. 1002, ¶142.) As discussed for Ground 3, claim 6, a POSITA would have found it obvious to implement the *Kobayashi* transmitter using a "low-density generator matrix (LDGM) coder," such as that disclosed by *McEliece*, "to perform an irregular repeat on [the] message bits" of sequence I_1 and "output a random sequence of repeats of the message bits." (Section IX.C.1.) As discussed for Ground 1, claim 1(b), the "message bits hav[e] a first sequence in a source data stream." (Section IX.A.1(b).)

c) an accumulator configured to XOR sum in linear sequential fashion a predecessor parity bit and "a" bits of the random sequence of repeats of the message bits.

The *Kobayashi-McEliece* combination discloses or suggests these limitations for the same reasons as explained for Ground 2, claim 13(c). (Section IX.B.5(c); Ex. 1002, ¶143.)

4. Claim 18

a) A device comprising:

To the extent the preamble of claim 18 is limiting, *Kobayashi* discloses the limitations therein. (Ex. 1002, ¶144.) For example, *Kobayashi* discloses a concatenated system with both transmitter and receiver portions, wherein the receiver is "[a] device," as claimed, which performs the iterative decoding technique shown in Figure 8 below. (Ex. 1005, 6:16-7:4 (describing the general iterative decoding technique), 7:28-11:17 (describing the Figure 8 implementation of the general iterative decoding technique); Ex. 1002, ¶144.)

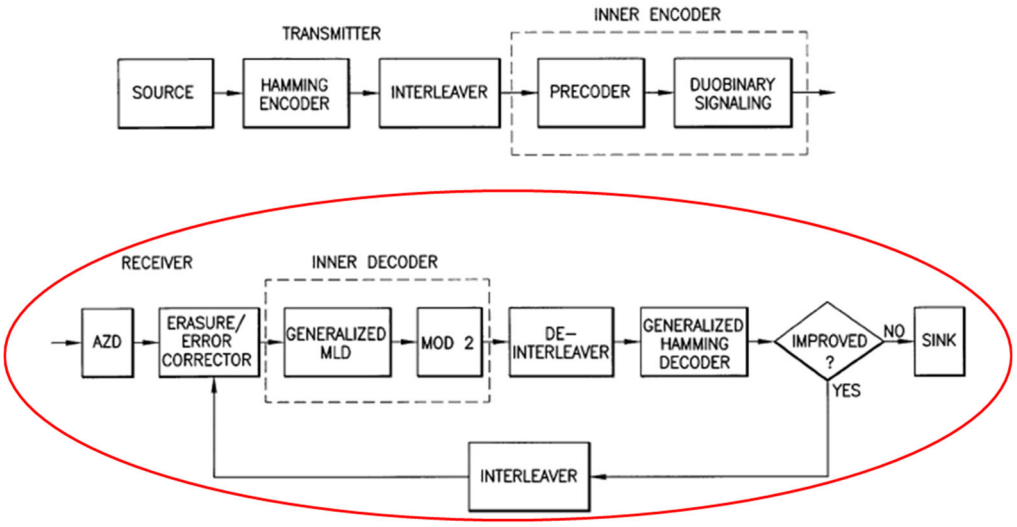
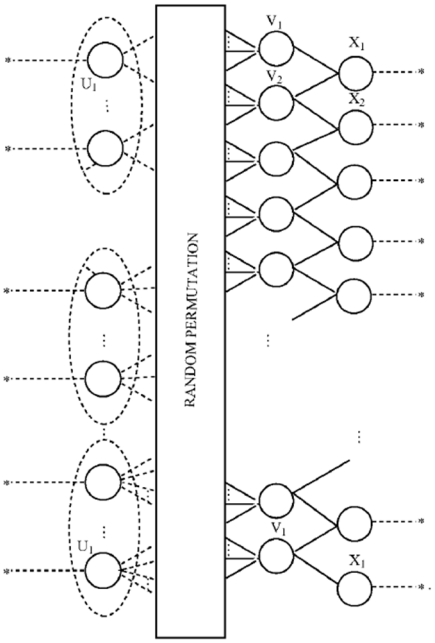


FIG.8

(Ex. 1005, FIG. 8 (annotated).)

b) a message passing decoder configured to decode a received data stream that includes a collection of parity bits, the message passing decoder comprising two or more check/variable nodes operating in parallel to receive messages from neighboring check/variable nodes and send updated messages to the neighboring variable/check nodes, wherein the message passing decoder is configured to decode the received data stream that has been encoded in accordance with the following Tanner graph:[15]

[15] Per the CoC appended to the '032 patent, the bottom U_1 of the Tanner graph should read U_k, the bottom V_1 should read V_r, and the bottom X_1 should read X_r. (*See* Ex. 1001.)



The *Kobayashi-McEliece* combination discloses or suggests these limitations. (Ex. 1002, ¶¶145-153.) As discussed for Ground 3, claim 6, it would have been obvious to modify the *Kobayashi* coding system so that the *Kobayashi* decoder discussed for Ground 3, claims 6 and 18(a) is replaced with a belief propagation decoder similar to that disclosed by *McEliece*. (*See* Section IX.C.1[16]; *see also* Section IX.C.4(a); Ex. 1002, ¶145 (citing the first modification at Ex. 1002, ¶¶124-130).)

As discussed for Ground 3, claim 6, the decoder of the *Kobayashi-McEliece* system is a "message passing decoder" because it uses Pearl's belief propagation

[16] While Section IX.C.1 discusses a second modification to implement a low-density generator matrix coder, such a modification is not necessary for claim 18(b).

algorithm, which is a decentralized, message-passing algorithm. (Section IX.C.1; Ex. 1002, ¶146.) The *Kobayashi-McEliece* decoder is also "configured to decode a received data stream that includes a collection of parity bits" because it is configured to decode the data stream sent by *Kobayashi*'s transmitter, which as discussed for Ground 1, claims 1(d) and 8, transmits a stream to the receiver device that includes a collection of parity bits. (Section IX.C.1; *see also* Sections IX.A.1(d), IX.A.6; Ex. 1002, ¶146.) As discussed for Ground 3, claim 6, the "message passing decoder compris[es] two or more check/variable nodes operating in parallel to receive messages from neighboring check/variable nodes and send updated messages to the neighboring variable/check nodes" because *McEliece*'s belief propagation decoder may have multiple nodes/processors operating in parallel to receive messages from neighboring nodes (parents and children), update the belief based on the messages, and send new messages to neighboring nodes (parents and children). (Section IX.C.1; Ex. 1002, ¶147.) The *Kobayashi-McEliece* decoder is also "configured to decode the received data stream that has been encoded in accordance with the . . . Tanner graph" above because it is configured to decode the data stream sent by *Kobayashi*'s transmitter, which as discussed for Ground 1, claim 11(b), encodes the message bits in accordance with the same Tanner graph. (Section IX.C.1; *see also* Section IX.A.7(b); Ex. 1002, ¶148.)

To the extent the *Kobayashi-McEliece* decoder, with the modifications described above, is found to not be "configured to decode the received data stream that has been encoded in accordance with the . . . Tanner graph," a POSITA would have found it obvious to implement the *Kobayashi-McEliece* combination such that its decoder decodes based on a Tanner graph representation of the encoder output, which is received by the decoder. (Ex. 1002, ¶149.) *McEliece* discloses that its belief propagation decoding algorithm for serially concatenated codes can decode an encoded data stream based on the belief network shown in Figure 12, reproduced below. (Ex. 1006, 149.)

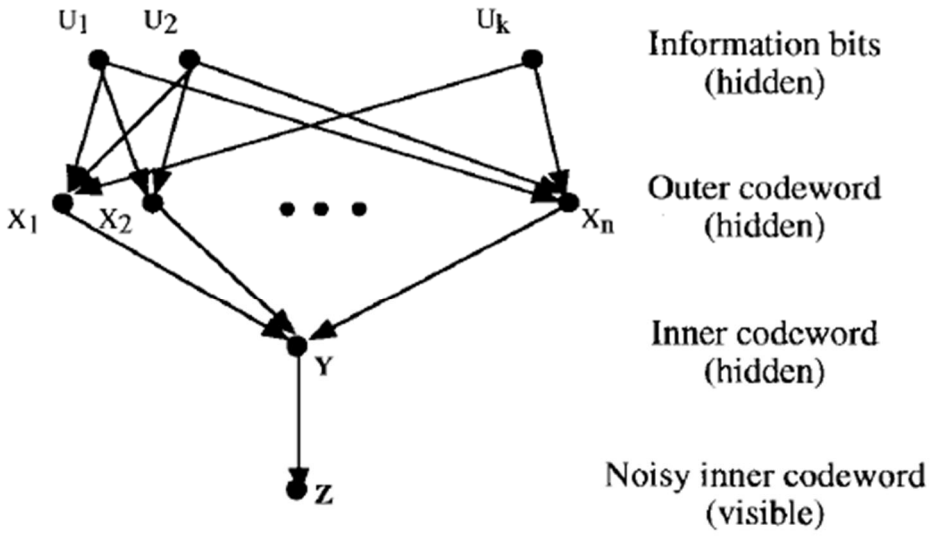


Fig. 12. Belief network for decoding a pair of serially concatenated codes.

(*Id.*, 150 (FIG. 12); Ex. 1002, ¶150.)

McEliece discloses that its other belief network diagrams are comparable to Tanner graph representations. (Ex. 1006, 145 n.9 ("Our Fig. 7 [belief network]

should be compared to Wiberg [67, Fig. 2.5], which describes the 'Tanner graph' of a turbo code.").) Moreover, *McEliece* discloses that, in the context of several variations on the belief propagation algorithm, both belief networks and Tanner graphs can be successfully used to yield the algorithm. (Ex. 1006, 150 ("If we were to apply Pearl's algorithm to the belief diagram of Fig. 13, we would obtain an iterative decoding algorithm for the tail-biting code. . . . Wiberg [67] has applied his algorithm to the Tanner graph of a tail-biting code with good success, and functionally, these two approaches yield virtually identical algorithms."); *see also id.*, 150 n.10 ("In this connection, we should note that Wiberg [67] has observed that his algorithm, when applied to a Tanner graph similar to Fig. 13 (less the tail-biting edge), also implies the BCJR algorithm."), 150 ("the BCJR algorithm . . . can be viewed as a kind of belief propagation"); Ex. 1002, ¶151.)

A POSITA would have found it obvious to modify the *Kobayashi-McEliece* coding system's decoder such that it decodes based on a Tanner graph representation, rather than a belief network representation, of Figure 12. (Ex. 1002, ¶152.) Decoding based on a Tanner graph representation was well known to a POSITA at the time of the invention, and *McEliece* discloses decoding using Tanner graph representations as a viable option for use with belief propagation decoding. (*Id.*) A POSITA would have also had the skill to implement, and expectation of success in achieving such a modification because it would have involved nothing

more than an application of a known method (belief propagation decoding based on a Tanner graph representation) to a known device (the *Kobayashi-McEliece* coding system's belief propagation decoder) to yield predictable results (provide a belief propagation decoder that decodes based on a Tanner graph representation). (*Id.*) *KSR*, 550 U.S. at 416-418.

Accordingly, the *Kobayashi-McEliece* combination discloses or suggests the limitations of this claim. (Ex. 1002, ¶153.)

5. Claim 19

a) The device of claim 18, wherein the message passing decoder is configured to decode the received data stream that includes the message bits.

The *Kobayashi-McEliece* combination discloses these limitations. (Ex. 1002, ¶154.) As discussed for Ground 3, claims 6 and 18(b), a POSITA would have found it obvious to implement the *Kobayashi-McEliece* device such that the "message passing decoder is configured to decode the received data stream" from *Kobayashi*'s transmitter. (Sections IX.C.1, IX.C.4(b).) A POSITA would have further found it obvious to implement *Kobayashi*'s transmitter (and thus the *Kobayashi-McEliece* decoder) such that the "received data stream . . . includes the message bits" for the same reasons as explained for Ground 2, claim 2, which discusses how a POSITA would have found it obvious to implement the *Kobayashi* transmitter using a systematic code. (Section IX.B.1.) Thus, the *Kobayashi-McEliece* combination

discloses or suggests that "the message passing decoder is configured to decode the received data stream that includes the message bits." (Ex. 1002, ¶154.)

6. Claim 20

a) The device of claim 18, wherein the message passing decoder is configured to decode the received data stream as if a number of inputs into nodes v_i was not constant.

The *Kobayashi-McEliece* combination discloses these limitations. (Ex. 1002, ¶155.) As discussed for Ground 3, claims 6 and 18(b), a POSITA would have found it obvious to implement the *Kobayashi-McEliece* device such that the "message passing decoder is configured to decode the received data stream" from *Kobayashi*'s transmitter. (Sections IX.C.1, IX.C.4(b).) As further discussed for Ground 1, claim 12, the *Kobayashi* transmitter is configured to encode message bits "as if a number of inputs into nodes v_i was not constant." (Section IX.A.8.) Thus, the *Kobayashi-McEliece* combination discloses or suggests that "the message passing decoder is configured to decode the received data stream as if a number of inputs into nodes v_i was not constant." (Ex. 1002, ¶155.)

7. Claim 21

a) The device of claim 18, wherein the message passing decoder is configured to decode in linear time at rates that approach a capacity of a channel.

The *Kobayashi-McEliece* combination discloses or suggests these limitations. (Ex. 1002, ¶¶156-160.) As discussed for Ground 3, claim 13, it would have been

obvious to further modify *Kobayashi* in view of *McEliece* to implement a low-density generator matrix coder. (Section IX.C.1.) As further discussed, *McEliece* discloses a small number of options for the low-density generator matrix, including classes of block codes constructed by *MacKay* (Ex. 1007) and *Cheng* (Ex. 1011, Ex. 1012), and thus a POSITA would have had good reason to pursue a modification with any of the solutions. (Section IX.C.1.) Thus, a POSITA would have had good reason to pursue a modification with *Cheng*'s low-density generator matrix code. (*See* Ex. 1006, 149 (citing Ex. 1011 (*Cheng I*), Ex. 1012 (*Cheng II*)); Ex. 1002, ¶156.)

Cheng discloses a class of low-density generator matrix codes whose corresponding Bayesian belief networks, such as shown below, may be decoded using a belief propagation algorithm. (Ex. 1012, 66; Ex. 1002, ¶157.)

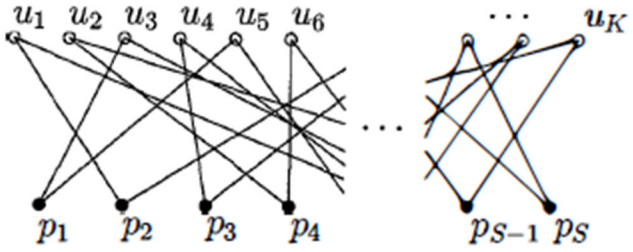


Figure 5.2 A random regular bipartite belief network.

(Ex. 1012, 66 (FIG. 5.2).) *Cheng* discloses that the random regular bipartite graph has "two partite sets as *K* and *S*," which are called "*systematic* nodes and *parity* nodes," and the vertices are labeled as "$u_1, u_2, \ldots, u_k$ and $p_1, p_2, \ldots, p_s$, respectively,

as shown in Fig. 5.2." (*Id.*, 67.) *Cheng* describes "G = [I | P]" as the "corresponding generator matrix of the new code, where *I* is a *K* x *K* identity matrix and *P* is a *K* x *S* matrix." (*Id.*) Because "[t]he entry P_{ij} of the matrix *P* will be 1 if and only if there is an edge connecting u_i and p_j, and 0 otherwise," the "class of codes is termed low-density generator matrix (LDGM) codes since G is sparse by this construction." (*Id.*) *Cheng* discloses that its class of LDGM codes encompasses both regular and irregular belief networks. (*Id.*, 67.) Given a code is either irregular or regular, and Koyabashi is already irregular, a POSITA would have been motivated to try the irregular type disclosed by *Cheng*. (Ex. 1002, ¶157.)

As discussed for Ground 3, claim 18(b), a POSITA would have found it obvious to modify the *Kobayashi-McEliece* coding system's decoder such that it decodes based on a Tanner graph representation, rather than a belief network representation, of an encoding mechanism. (Section IX.C.4(b).) Because *McEliece* and *Cheng* disclose belief network representations of LDGM codes, a POSITA would have therefore recognized that the *Kobayashi-McEliece* decoder, when implemented using *Cheng*'s LDGM (as taught by *McEliece*) and the belief propagation decoder disclosed by *McEliece* (*see* Section IX.C.1) would still meet the limitations of claim 18 for the reasons previously discussed for Ground 3, claim 18(b). (Section IX.C.4(b); Ex. 1002, ¶158.)

Cheng further discloses that its LDGM codes "can be encoded and decoded with complexity linear in the code length," and that "[t]he performances of these codes . . . are [within] 1 dB or so of the channel capacity." (Ex. 1011, 522; *see also* Ex. 1012, 65 (disclosing that *Cheng*'s class of LDGM codes "can be encoded and decoded in linear time" and "the performance of these new systems . . . approach the capacity of the Gaussian channel").) A POSITA would have thus understood that the *Kobayashi-McEliece* message passing decoder is also "configured to decode in linear time at rates that approach a capacity of a channel," as claimed. (Ex. 1002, ¶¶159-160.)

8. Claim 22

a) The device of claim 18, wherein the message passing decoder comprises a belief propagation decoder.

The *Kobayashi-McEliece* combination discloses or suggests these limitations. (Ex. 1002, ¶161.) As discussed for Ground 3, claim 18(b), the message passing decoder of the *Kobayashi-McEliece* combination is a belief propagation decoder. (Section IX.C.4(b).)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE HERE

A. The Board Should Not Use Its Discretion to Deny Institution Under *Fintiv*

The Board should decline to exercise its discretion to deny institution under 35 U.S.C. § 314(a). As explained below, the six factors set out in *Fintiv* do not

justify denying institution. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential).

As an initial matter, in light of Director Vidal's guidance on *Fintiv*, the Board should not rely on the *Fintiv* factors given this petition raises a compelling, meritorious challenge. *See* Memorandum on Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation issued by Director Vidal (June 21, 2022) ("Discretionary Denials Memorandum") at 2. The challenge here is particularly compelling and meritorious. For example, as discussed above, *Kobayashi* alone discloses or suggests all the limitations of the majority of the challenged claims. *See supra* Section IX. Unlike the prior IPRs filed by other petitioners (*see* Section II), PO cannot argue that the references being asserted here do not qualify as prior art, lack key claim features, or are premised on combinations that are unpredictable. *See, e.g.*, Hughes -060 IPR, Paper 18 at 14-15 (Apr. 27, 2015) (finding that petitioner did not meet burden to show the relied-upon reference is a printed publication); *id.* at 20-21 (finding that petitioner did not meet burden to show the relied-upon references teach the IRA claim features); Apple -700 IPR, Paper 67 at 21-27 (Aug. 2, 2018) (finding that petitioner did not meet burden to show that there was a reasonable expectation of success in the proposed combination); Apple -701 IPR, Paper 67 at 19-26 (Aug. 2, 2018) (same); Apple -728 IPR, Paper 63 at 22-28 (Aug. 21, 2018) (same); *see also infra* Section X.C. Thus, the evidence

supporting the challenges here, if unrebutted, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of evidence. *See* Discretionary Denials Memorandum at 4. Accordingly, the PTAB should institute this IPR regardless of the status of the parallel district court litigation. *Id.* at 2, 4.

But even if the other *Fintiv* factors are considered, they weigh in favor of institution.

For example, the **first *Fintiv* factor** is at best neutral, because Samsung has not yet moved to stay the district court proceedings pending IPR, and the PTAB will not infer how the district court would rule should a stay be requested. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

As to the **second *Fintiv* factor**, while trial is currently scheduled for September 11, 2023 (Ex. 1015, 1), the median time from the filing of a civil case to trial in the Eastern District of Texas is 24.5 months, placing the expected trial date in the parallel litigation around December 17, 2023 (Ex. 1016, 35). *See also* Discretionary Denials Memorandum at 8-9 (Director instructing Board to consider median time-to-trial statistics when evaluating second *Fintiv* factor).

And even if trial proceeds in September 2023, the above timing does not tip in favor of denying the petition in this case. *See also, e.g., Apple Inc. v. Koss Corp.*, IPR2021-00305, Paper 14 at 13 (June 3, 2021). This Petition is being filed in

October 2022. An institution decision should be issued within six months around April 2023. And a final written decision (FWD) should be issued in April 2024. Thus, the current trial date is only approximately seven months before the FWD (or four months before the FWD in consideration of the median time-to-trial statistics). PTAB cases analyzing similar schedules have weighed the second factor as neutral or, at most, slightly in favor of denial. *See, e.g., Sand Revolution II, LLC v. Cont'l Intermodal Grp–Trucking LLC*, IPR2019-01393, Paper 24 at 8–10 (June 16, 2020) ("*Sand*") (informative) (factor 2 favored institution despite trial preceding FWD deadline by five months); *Google LLC et al. v. Parus Holdings, Inc.*, IPR2020-00847, Paper 9 at 12 (Oct. 21, 2020) (trial scheduled for three months before FWD weighs "at best, neutral"). Nevertheless, even "an early trial date" is "non-dispositive" and simply means that "the decision whether to institute will likely implicate other factors," which, as explained, favor institution. *Fintiv*, 5, 9.

The **third *Fintiv* factor** weighs strongly against denial. First, the district court cases are in the early stages. Fact discovery just began. The parties have not taken any depositions or engaged in expert discovery. Nor have there been any substantive orders in the case. Claim construction is also at its very early stages with the parties having just exchanged claim terms. *See Skechers U.S.A., Inc. v. Nike, Inc.*, IPR2021-00160, Paper 10 at 12-13 (May 19, 2021) (finding this factor weighs against exercising discretion due to, in part, the lack of a *Markman* hearing or order); *see*

also Samsung Electronics Co. Ltd. v. Jawbone Innovations, LLC, IPR2022-00630, Paper 10 at 14-15 (Sep. 13, 2022) (similar); *Zhuhai Cosmx Battery Co., Ltd. v. Maxell, Ltd.*, IPR2022-00984, Paper 8 at 6-7 (Sep. 29, 2022) (finding this factor weighs against exercising discretion even though *Markman* hearing already held because much other work relating to invalidity remained).

Additionally, Petitioner filed its petitions almost two months before the statutory deadline to do so, and just seven months after being served with preliminary infringement contentions (PICs) on March 2, 2022, which identified the asserted claims.[17] In its complaint against Samsung, PO asserted four patents containing over 90 issued claims. Therefore, as the Board has found, it was reasonable for Petitioner to wait to file this Petition until after receiving and analyzing the contentions. *Facebook, Inc. v. USC IP P'ship*, *L.P.*, IPR2021-00033, Paper 13 at 13 (Apr. 30, 2021). Indeed, Samsung's diligence in filing its petition after receiving PO's preliminary infringement contentions and less than six months from the amended complaint (Ex. 1017) is also a "countervailing consideration" to any investment in the district court proceedings and weighs against exercising

[17] PO's PICs are insufficient as they do not address any actual accused product or even contend that any product necessarily infringes, but rather focus on a standard. (*See generally* Ex. 1018.)

discretion. *Tianma Microelectronics Co. Ltd. v. Japan Display Inc.*, IPR2021-01028, Paper 14 at 9-11 (Dec. 14, 2021) (instituting IPR when "[FWD] would issue approximately ten months after the start of trial" and IPR was filed within five months of receiving infringement contentions); *see also Coolit Systems, Inc. v. Asetek Danmark A/S*, IPR2021-01195, Paper 10 at 11-12 (Dec. 28, 2021) (instituting IPR when FWD would issue five months after the scheduled trial date and IPR was filed five months after receiving infringement contentions, noting petitioner's diligence in light of the litigation involving numerous patents). Accordingly, because the investment in the trial has been minimal and Petitioner acted diligently, this factor weighs against discretionary denial. *See, e.g., Hulu*, Paper 11 at 13.

The **fourth *Fintiv* factor** strongly favors institution. Petitioner may rely on invalidity grounds not asserted here in the district court litigation, including system art and prior art references and combinations not raised herein. Furthermore, the challenged claims include claims 1, 2, and 20 that are not asserted in the litigation. Thus, the validity of claims 1, 2, and 20 will only be adjudicated in this proceeding, not in district court. Therefore, any potential overlap between this proceeding and the district court is minimal and speculative at this time.

Moreover, Petitioner hereby stipulates that, if the IPR is instituted, Petitioner will not pursue the IPR grounds in the district court litigation. Thus, instituting trial here serves overall system efficiency and integrity goals by not duplicating efforts

and by resolving materially different patentability issues. *Sand*, Paper 24 at 12 (informative) (finding the fourth factor weighs in favor of institution due to petitioner's stipulation that it will not pursue the same grounds in district court despite trial preceding FWD deadline by five months). Thus, the fourth factor strongly favors institution.

Regarding the **fifth *Fintiv* factor**, the Board should give no weight to the fact that Petitioner and PO are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, Paper 16 at 11-13 (Apr. 14, 2021).

Thus, taken together holistically, the *Fintiv* factors strongly weigh against denial.

B. The Board Should Not Exercise Its Discretion Under *General Plastic*

This is not a serial petition under the factors set forth in *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper No. 19 at 16 (September 6, 2017). *General Plastic* concerns serial petitions filed by the same petitioner directed to the same claims of the same patent. *Id.* (first factor). Here, this is Petitioner's first petition directed to any claims of the '032 patent. Thus, the first factor favors institution.

The second through fifth factors have little to no bearing here given factor one favors institution. *Amneal Pharmaceuticals LLC et al. v. Almirall, LLC*, IPR2019-

00207, Paper 13 at 12–13 (May 10, 2019) (finding factor one dispositive); *Western Digital Corp. v. Spex Technologies, Inc.*, IPR2018-00084, Paper 14 at 17 (April 25, 2018). In any event, with respect to the second factor (*GP* at 16), the prior art combinations asserted in the instant Petition are different than the prior art combinations asserted in the prior IPRs filed by Apple and Hughes, which predated the Federal Circuit's claim construction of repeat.

With respect to the third factor (*GP* at 16), this Petition is being filed in light of PO's complaint against Samsung, which was filed well after its earlier complaints against Apple and Hughes. Thus, PO cannot argue that the timing of this IPR favors denial, as it would ignore its own conduct of serially asserting the same patents leading to the staggered IPR filings. *Western* at 18; *Echostar Corp. et al. v. Realtime Data LLC*, IPR2018-00612, Paper 10 at 20 (August 28, 2018)

The fourth and fifth factors (*GP* at 16) are inapplicable, or, if anything, favor institution, because this is Petitioner's first petition challenging any claims of the '032 patent and because there is no overlap between the grounds of this petition and those in the prior IPRs.

The sixth and seventh *General Plastic* factors (*GP* at 16) also favor institution, because there is no indication that the instant IPR would unduly burden the Board or impact the Board's duty to render a FWD in this IPR. *Cooler Master Co. Ltd. v. Aavid Thermalloy LLC*, IPR2019-00337, Paper 7 at 44-45 (June 12, 2019).

Accordingly, the Board should institute this Petition.

C. The Board Should Not Exercise Its Discretion Under Section 325(d)

The Board should not exercise its discretion under § 325(d), because neither *Kobayashi* nor *McEliece* were before the Office prior to this IPR. Nor are these references cumulative of references previously before the Office. For example, unlike prior references, *Kobayashi* expressly discloses the features involving the irregular repetition and accumulation of bits as set forth in some variation in, *e.g.*, claim 1(c). Section IX.A.1.c. Moreover, this petition presents new combinations of references that were not before the Office, including *Kobayashi* in view of *McEliece*. Thus, the Office erred in a manner material to patentability by not considering the teachings, arguments, obviousness combinations, and evidence presented in this Petition (Section IX).

XI. CONCLUSION

Accordingly, Petitioner requests institution of IPR for the challenged claims based on the specified grounds.

Respectfully submitted,

Dated: October 31, 2022 By: */Robert A. Appleby/*

Robert A. Appleby
Counsel for Petitioner
Reg. No. 40,897

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,421,032 contains, as measured by the word-processing system used to prepare this paper, 13,819 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: October 31, 2022 By: */Robert A. Appleby/*

Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on October 31, 2022, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,421,032 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center:

Bryan Cave Leighton Paisner LLP
1290 Avenue of the Americas
New York, NY 10104

By: */Robert A. Appleby*