

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION

Petitioner

v.

GREENTRHEAD, LLC

(record) Patent Owner

DECLARATION OF R. MICHAEL GUIDASH

Patent No. 11,316,014

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1. I, R. Michael Guidash, hereby declare as follows:

I. ENGAGEMENT AND COMPENSATION

2. I have been retained by Sony Group Corporation (“Petitioner”) as an expert in the *inter partes* review proceeding described above. I have been asked to provide my technical review, analysis, insights, and opinions regarding the references that form the basis for the grounds of unpatentability set forth in the Petition for *inter partes* review of U.S. Pat. No. 11,316,014 (the ’014 Patent). For this service, my billing rate is an hourly consulting fee of \$600/hour, and I am reimbursed for actual expenses. My compensation in no way depends on the outcome of this matter.

3. This declaration sets forth my analyses and opinions based on the materials I have considered thus far and the bases for my opinions. I understand that this declaration will be used in the above mentioned *inter partes* review. In forming my opinions, I have considered the following Exhibits:

Exhibit No.	Description
1001	U.S. Pat. No. 11,316,014 (“the ’014 patent”).
1004	U.S. Pat. No. 6,614,560 (“ Silverbrook ”).
1005	U.S. Pat. No. 6,420,763 (“ Yamashita ”).
1006	File History of U.S. App. Ser. No. 11/622,496 (issued as U.S. Pat. No. 8,421,195).
1007	File History of U.S. App. Ser. No. 17/371,839 (issued as the ’014 patent).

1008	U.S. Pat. No. 4,481,522 (“ Jastrzebski ”).
1009	Redline comparisons of claim 1 and claim 21
1010	U.S. Pat. Pub. 2004/0063288 A1 (“ Kenney ”).
1011	U.S. Pat. Pub. 2001/0032983 A1 (“ Miyagawa ”).
1012	Nishi, et al. (eds.) <i>Handbook of Semiconductor Manufacturing</i> , Marcel Dekker, Inc., New York (2000) (“ Nishi ”).
1018	U.S. Pat. App. Pub. 2003/0136982A1 (“ Rhodes ”).
1024	U.S. Pat. No. 6,483,176 (“ Noguchi ”).
1025	U.S. Pat. App. Pub. 2003/0063272A1 (“ Zaidi ”).
1026	U.S. Pat. App. Pub. 2003/0081463A1 (“ Bocian ”).
1027	U.S. Pat. App. Pub. 2003/0098419A1 (“ Ji ”).
1029	Excerpt from Pierret, <i>Semiconductor Fundamentals, Vol. I</i> , Addison-Wesley Publishing Company, Reading, MA, 1983.
1030	Excerpt from Grove, <i>Physics and Technology of Semiconductor Devices</i> , John Wiley & Sons, 1967.
1031	Excerpt from Sze, <i>VLSI Technology</i> , McGraw-Hill Book Company, 1983.
1032	Excerpt from Wolf and Tauber, <i>Silicon Processing for the VLSI ERA</i> , Lattice Press, Sunset Beach, CA, (2000).

II. SUMMARY OF OPINIONS

4. It is my opinion that claims 1-30 of the '014 patent are unpatentable for the following reasons (“Grounds”):

- **Ground 1:** Claims 1-15, 17, and 20-30 were obvious over Yamashita.
- **Ground 2:** Claims 1-30 were obvious over Silverbrook in view of

Yamashita.

- **Ground 3:** Claims 1-30 were obvious over Silverbrook in view of Yamashita and Nishi.

I. QUALIFICATIONS

5. I started my career with Eastman Kodak as a product engineer for Photometer ASIC's for Kodak film cameras after graduating with a Bachelor of Science in Electrical Engineering from the University of Delaware in 1981. In 1986, I transferred to the Kodak Research Laboratories and CCD wafer fabrication facility. During my time with the Kodak Research Laboratories and CCD wafer fabrication facility, I developed 2 μm and 1 μm CMOS processes, and a 30 V 4 μm Bipolar complementary metal-oxide-semiconductor (BiCMOS) process. These processes were used for gate arrays for many Kodak products and output driver ASICs for all of Kodak's copiers. During this time, I was also awarded entrance into the Special Opportunity Graduate Program that allowed me to obtain a Master's of Science in Electrical Engineering from the Rochester Institute of Technology. My Masters Thesis involved design and process integration of bipolar and CMOS transistors into an existing CCD (charge-coupled device) image sensor process. In this work I performed all of the transistor design, selected logic gate layouts, as well as simulated and implemented the process steps, location of the process steps in the existing CCD fabrication process, and attendant ion implants for formation of the

nMOS and pMOS transistors and NPN bipolar transistors. I also performed all of the transistor measurements to verify the transistor performance. These measurements included nMOS and pMOS transistor threshold voltage, punch-through voltage and current, subthreshold current, hot carrier immunity, and source/drain to substrate capacitance. Extensive testing of NPN bipolar transistor parameters was also performed. The results of this work were also published in the Proceedings of Seventh Annual IEEE International ASIC Conference and Exhibit in April 1994 (Ex. 1029).

6. In 1989, I transferred to the Smart Sensor Group which developed BiCMOS-CCD processes to provide fully integrated CCD systems on a chip. I also served as product engineer and yield enhancement engineer for Kodak's high volume CCDs. During this time, I led product delivery and technology development of all ASIC and smart sensor products. I developed a number of products during this time to include an interline CCD integrated with 2 μm CMOS on the same chip, the world's 1st pinned photodiode Active Pixel CMOS Sensor product, and linear CCD image sensor with on-chip timing and control. I also led and directed the CCD dark current and point defect reduction team.

7. In 1996, I formally started the CMOS Image Sensor group at Kodak. From 1996 to 2009, I managed the R&D and product development of CMOS Image Sensor (CIS) programs. As is further shown in my curriculum vitae, I was the

inventor or co-inventor of many key patents in the field of CMOS image sensors including pinned photodiode pixels, camera-on-a-chip architecture, and shared amplifier pixel architectures. During this time, I led the development of the world's 1st pinned photodiode CIS product, Shared amplifier CIS pixel product, and the world's first ½ inch optical format 1.3 megapixel CMOS image sensor into mass production, providing successful delivery to several compact digital camera products. I also led the development of one of the earliest 3D hybrid stacked BSI CIS architecture. This led to demonstration of very high performance, low dark current BSI prototype sensors with pixel sizes ranging from 0.9um to 5.0um.

8. In 2009, when Kodak closed its CMOS Image Sensor Business, I transitioned into a role as an intellectual property technologist and coordinator. This role included managing remaining image sensor patent applications and office actions, managing broad electronic components patent applications and office actions, and providing technical support for intellectual property sales and licensing teams.

9. I have since left Kodak and transitioned into a role of providing technical consulting services for CMOS image sensors. In this role I provide consulting services for processes, pixels, circuits, sensor architectures, systems and intellectual property to companies and clients.

10. My qualifications and publications are set forth more fully in my curriculum vitae, attached as Ex. 1003.

III. MY UNDERSTANDING OF THE RELEVANT LAW

A. Claim Construction

11. I understand that a claim term in an *inter partes* review is to be interpreted according to standards applied by district courts. First, the language of the claims themselves is of primary importance in the effort to determine precisely what it is that is patented. The terms used in a claim are generally given the ordinary and customary meaning that the terms would have to a person of ordinary skill in the art in question at the time of the alleged invention, unless the term is expressly defined in the patent. The person of ordinary skill in the art reads the claim in the context of the entire patent, including the specification. Next to the language of the claims, the specification is the single best source for interpreting the claim terms. The claims may also be interpreted using the record of correspondence between the patent applicant and the Patent Office, and also with reference to other sources of evidence that can help to define the meaning of terms to a person of ordinary skill in the relevant time frame. I define the relevant time frame in ¶70, below.

B. Anticipation

12. I understand that a claim in an issued patent can be invalid if it is anticipated. In this case, “anticipation” means that there is a single prior art reference that discloses every element of the claim, arranged in the way required by the claim.

13. I understand that an anticipating prior art reference must disclose each of the claim elements expressly or inherently. I understand that “inherent” disclosure means that the claim element, although not expressly described by the prior art reference, must necessarily be present based on the disclosure. I understand that a mere probability that the element is present is not sufficient to qualify as “inherent disclosure”.

C. Obviousness

14. I understand that a claim in an issued patent can be invalid if it is obvious. Unlike anticipation, obviousness does not require that every element of the claim be in a single prior art reference. Instead, it is possible for claim elements to be described in different prior art references, so long as there is motivation or sufficient reasoning to combine the references.

15. I understand that a claim is invalid for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the alleged invention was made to a person having ordinary skill in the art to which said subject matter pertains.

16. I understand, therefore, that when evaluating obviousness, one must consider obviousness of the claim “as a whole”. This consideration must be

from the perspective of the person of ordinary skill in the relevant art, and that such perspective must be considered as of the “time the invention was made”.

17. The level of ordinary skill in the art is discussed in ¶69 below.

18. The relevant time frame for obviousness, the “time the invention was made”, is discussed in ¶70, below.

19. I understand that in considering the obviousness of a claim, one must consider four things. These include the scope and content of the prior art, the level of ordinary skill in the art at the relevant time, the differences between the prior art and the claim, and any “secondary considerations”. I understand that these four things were specified by the U.S. Supreme Court in a case called *Graham v. John Deere*, and are therefore called the “*Graham* factors”.

20. I understand that “secondary considerations” include real-world evidence that can tend to make a conclusion of obviousness either more probable or less probable. For example, the commercial success of a product embodying a claim of the patent could provide evidence tending to show that the claimed invention is not obvious. In order to understand the strength of the evidence, one would want to know whether the commercial success is traceable to a certain aspect of the claim not disclosed in a single prior art reference (*i.e.*, whether there is a causal “nexus” to the claim language). One would also want to know how the market reacted to disclosure of the invention, and whether commercial success might be traceable to

things other than innovation, for example the market power of the seller, an advertising campaign, or the existence of a complex system having many features beyond the claims that might be desirable to a consumer. One would also want to know how the product compared to similar products not embodying the claim. I understand that evidence of commercial success should be reasonably commensurate with the scope of the claim, but that it is not necessary for a commercial product to embody the full scope of the claim.

21. Other kinds of secondary considerations are possible. For example, evidence that the relevant field had a long-established, unsolved problem or need that was later provided by the claimed invention could be indicative of non-obviousness. Evidence that others had tried, but failed to make an aspect of the claim might indicate that the art lacked the requisite skill to do so. Evidence of copying of the patent owner's products before the patent was published might also indicate that its approach to solving a particular problem was not obvious. Evidence that the art recognized the value of products embodying a claim, for example, by praising the named inventors' work, might tend to show that the claim was non-obvious.

22. I further understand that prior art references can be combined where there is an express or implied rationale to do so. Such a rationale might include an expected advantage to be obtained, or might be implied under the

circumstances. For example, a claim is likely obvious if design needs or market pressures existing in the prior art make it natural for one or more known components to be combined, where each component continues to function in the expected manner when combined (*i.e.*, when there are no unpredictable results). A claim is also likely invalid where it is the combination of a known base system with a known technique that can be applied to the base system without an unpredictable result. In these cases, the combination must be within the capabilities of a person of ordinary skill in the art.

23. I understand that when considering obviousness, one must not refer to teachings in the specification of the patent itself. One can, however, refer to portions of the specification admitted to be prior art, including the “Background” section. Furthermore, a lack of discussion in the patent specification concerning how to implement a disclosed technique can support an inference that the ability to implement the technique was within the ordinary skill in the prior art.

IV. TECHNICAL INTRODUCTION

A. Background

24. The '014 patent is directed to various structures for semiconductor devices.

25. Semiconductor devices have been prevalent in consumer electronic products for over four decades. Examples of semiconductor devices

include microprocessors, micro-controllers, memory, digital image sensors, signal processors, and smaller devices within these devices, such as transistors. The vast majority of such devices are fabricated using silicon, which is a semiconductor material. A semiconductor material is different from conductor materials, such as copper or aluminum, which have free carriers (electrons) that can conduct electricity without the need for thermal excitation. In contrast, without thermal or optical excitation, intrinsic semiconductor materials do not naturally have free carriers. Instead, engineers can create free carriers in a semiconductor material by adding impurities, called “dopants”. By adding different types and amounts of dopants to different parts of a piece of silicon, engineers can impart different electrical properties to different parts of silicon, creating complex devices known as “integrated circuits” or “chips”. Integrated circuits can have thousands to many millions of individual electronic devices, such as transistors, resistors, diodes, capacitors that are connected together as circuits.

26. Making a silicon integrated circuit begins with bulk silicon. Bulk silicon is often created from a melt, in a process that produces an ingot of silicon that is ideally a single crystal. The crystal ingot of silicon is then sawn into thin disks of silicon known as wafers. A wafer in 2004 was typically a round disk that could be several inches in diameter and slightly under a millimeter in thickness. The thickness of the wafer needed to be sufficient to allow for structural stability during

the “fabrication” process, that is, the process of forming electrical devices on the surface of a wafer.

27. The starting wafer itself typically had an initial and intentional concentration of dopants—the impurities discussed above that give silicon different electrical properties. Such “dopants” or “impurities” have two types: “n-type” or “p-type”. At a high level, dopants can be understood as making charge carriers more mobile. “N-type” dopants provide free negative charge carriers (electrons), while “p-type” dopants provide free positive charge carriers (a space where no electron is present, or a “hole”). The most common “n-type” dopant is phosphorous, although arsenic is also often used. The most common “p-type” dopant is boron, although boron difluoride is also sometimes used. Silicon that has n-type dopants is often called “n-type” silicon, whereas silicon that has p-type dopants is called “p-type” silicon. Undoped silicon is often called “native” or “intrinsic”. N-type dopants are often referred to as opposite type compared to p-type dopants and vice versa.

28. The concentrations of dopants in silicon is typically measured in the number of atoms per cubic centimeter. Typically, dopant concentrations might range from a low dopant concentration of 10^{13} atoms / cm^3 (which means 10,000,000,000,000 atoms of dopant per cubic centimeter of silicon) to a high dopant concentration of 10^{20} atoms / cm^3 . The more dopant that silicon has, the more free

carriers will be available to conduct current. Thus, highly-doped silicon is generally more conductive, *i.e.*, it has less resistance.

29. In undoped (“native”) silicon there are a low number of free carriers, giving undoped silicon a low electrical conductivity. In silicon that has n-type doping, there will be a higher number of free (mobile) electrons, allowing these electrons to more easily conduct electrical current. In this case, we say that electrons are the “majority” carriers, because they are relatively more abundant in n-type silicon. In n-type silicon, the positively-charged carriers, or “holes”, are the “minority” carriers. The situation is reversed in p-type silicon, where the holes are majority carriers, and the electrons are minority carriers.

30. Although bulk silicon wafers are typically doped, and could in theory be used to form devices such as transistors, it was common in the relevant timeframe to add a thin layer of silicon on the surface of the bulk silicon wafer, called an “epitaxial layer”. Such epitaxial layers were formed by different chemical or physical processes than those used to form the bulk wafer. The epitaxial processes were typically much slower (longer time to provide the same silicon thickness) than the process used to form the bulk silicon wafer, but could produce better crystal lattices and more precisely controlled doping concentrations. Thus, it was often expedient to form a relatively thicker wafer of silicon, needed for structural stability,

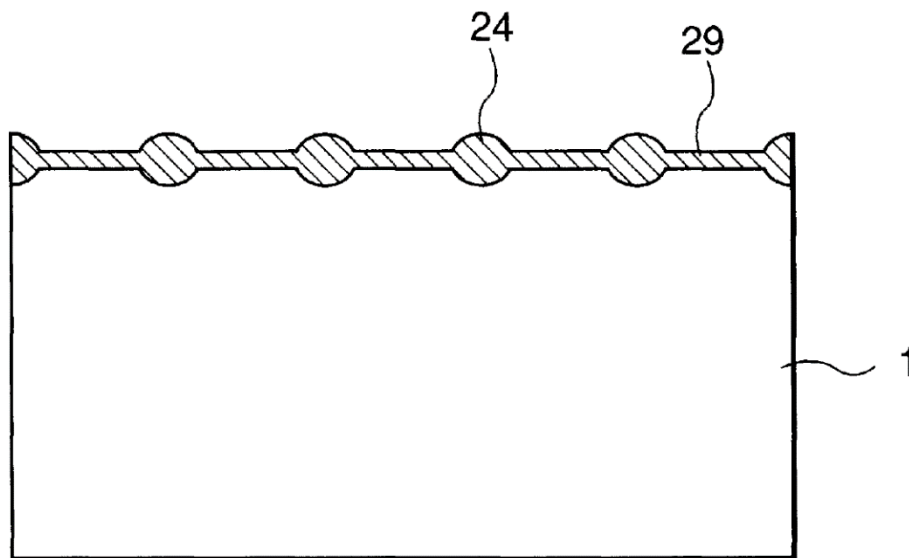
by pulling a crystal from a melt, and then to form a thinner epitaxial layer, with qualities more appropriate for devices, by slower epitaxial silicon growth processes.

31. To form devices such as transistors within the epitaxial silicon layer, a series of many processing steps are used. There were several types of steps used. These included:

- **Oxidation.** Oxidation converts silicon into silicon Dioxide (SiO_2). SiO_2 is an electrical insulator, and thus could be used to isolate electrical components from one another.
- **Masking.** Masking refers to the process of adding a photoresist layer (usually a polymer) to the surface of the wafer. The photoresist will harden in areas that are exposed to light (or for some resists, areas not exposed to light). A glass plate with patterns of light blocking material (a “mask”) could then be used to direct light onto the photoresist layer, which would harden the resist only in certain regions. The non-hardened regions could then be removed, exposing the surface of the silicon only in certain regions. This allows the selective application of various techniques to only certain regions of the device. The hardened portions of the photoresist layer can be later removed, and new masks used to form the desired patterns in other regions for subsequent process steps.
- **Deposition:** material such as insulators, metals or poly-crystalline silicon can be deposited and subsequently etched away (for example, in areas defined by a pattern in a resist layer) to form electrical interconnections.
- **Doping:** Dopants (as discussed above) can be added to silicon (beyond the dopants already in the bulk substrate or epitaxial layer). Dopants could be added in areas defined by a pattern in a photoresist layer.

32. An example of a semiconductor fabrication process is illustrated in Figs. 57-63 of the Yamashita prior art. (Ex. 1005, 22:29-32). This sequence of figures illustrates typical steps that can be used to fabricate semiconductor devices. Figure 57 of Yamashita begins with some processing already complete. Specifically, Fig. 57 shows a p-type silicon substrate 1, having a dopant concentration of $1 \times 10^{16} / \text{cm}^3$, that already has oxide portions 24 and 29 formed on its surface, as shown here:

FIG.57



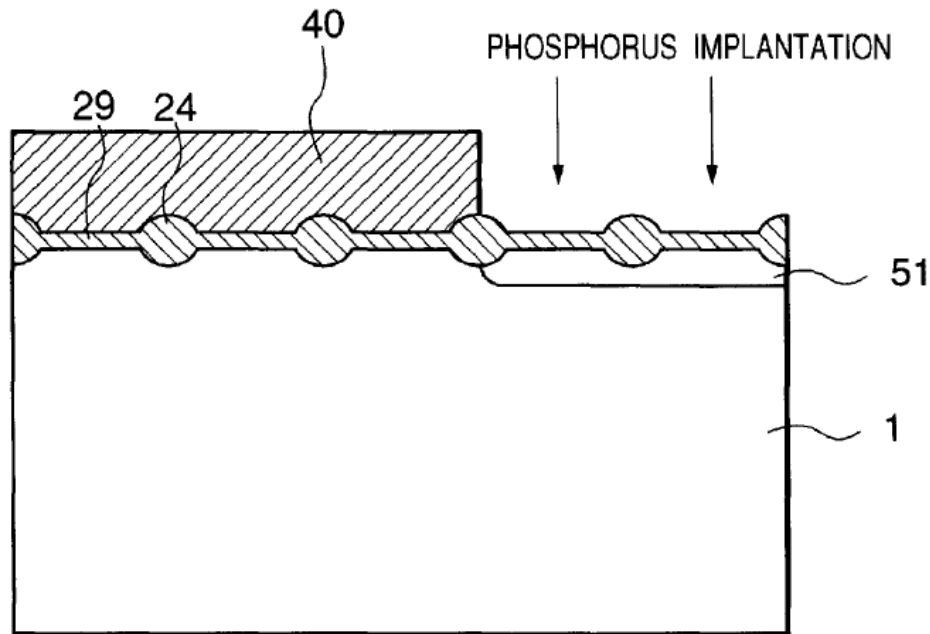
(Ex. 1005, Fig. 57, 22:32-39). Note that such drawings typically exaggerate the vertical dimension. A real device viewed in cross section would have a thickness that is dominated by the substrate, with typically only a very thin layer of devices at the top surface. These devices are typically formed by forming regions within the

existing substrate, chemically reacting the surface of the substrate, or depositing onto the substrate. The thickness of the structures produced by these operations are typically quite thin compared to the substrate.

33. Oxide portions 29 are thinner “gate oxide” regions in which active devices will be formed. (Ex. 1005, 22:32-39). The thicker oxide portions 24 are “field oxide” regions that are intended to separate and isolate active regions. (Ex. 1005, 22:32-39). These regions were likely formed with various masking and oxidation or deposition steps. (Ex. 1005, 22:32-39).

34. In the next figure, Fig. 58, Yamashita shows an example of masking and doping. Figure 58 is reproduced here:

FIG.58



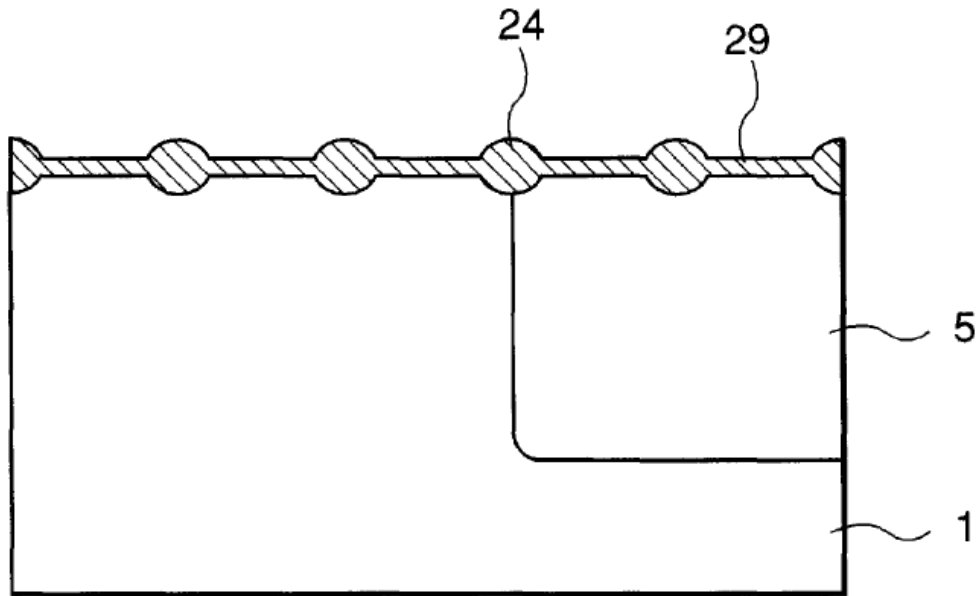
(Ex. 1005, Fig. 58).

35. In Fig. 58, a resist layer 40 has been formed selectively in a pattern having openings on the surface of the substrate. (Ex. 1005, Fig. 58, 22:39-45). An opening in the resist layer 40 on the right side of the figure allows for doping, in this case ion implantation (explained below), using phosphorous. (Ex. 1005, Fig. 58, 22:39-45). The patterned resist layer 40 blocks ion implantation on the left side of the diagram. In this area, the resist layer 40 is said to be “masking” a portion of the surface underneath the resist layer, thus protecting it from being affected by the current fabrication step (here, a phosphorous implantation). As a result, phosphorous atom dopants are not implanted underneath the resist layer 40, but

rather only added to the region 51 as shown in the Figure. (Ex. 1005, Fig. 58, 22:39-45). The depth of region 51 depends on several factors, including the energy with which the ions are implanted. The phosphorous is an “n-type” dopant, and is added to the low level of p-type dopants already present in the substrate. Because the phosphorous atoms are present in higher concentration than the p-type dopants, however, the region 51 becomes n-type, with electrons as the majority mobile carriers. (Ex. 1005, Fig. 58, 22:39-45).

36. In Fig. 59, shown below, Yamashita’s process has stripped off the resist layer 40, and has heated (“thermally annealed”) the substrate, causing the n-type dopants in region 51 to be positioned into the crystal lattice, (referred to as activated) and diffuse, to form a “low concentration n-type impurity layer 5”. (Ex. 1005, 22:45-49).

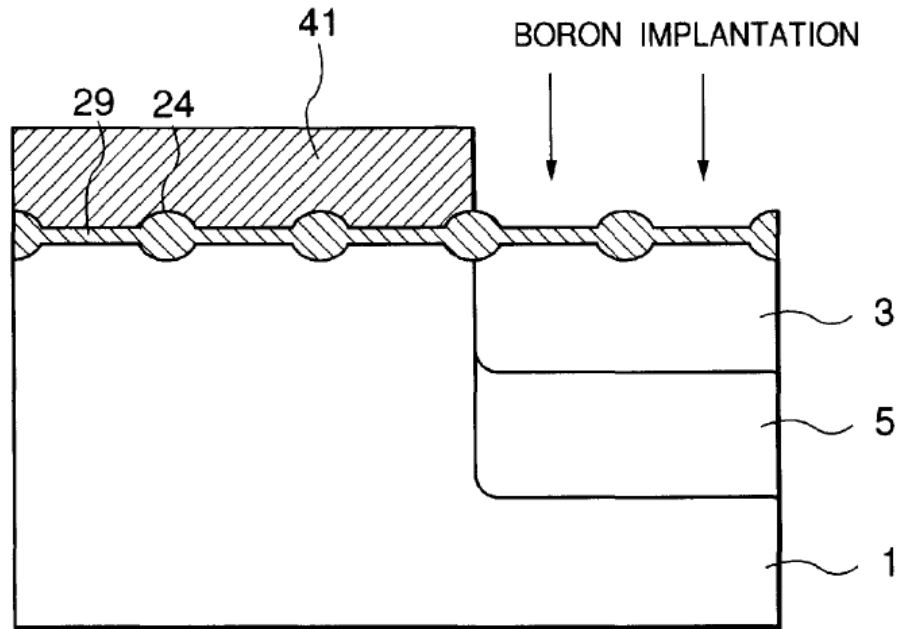
FIG.59



(Ex. 1005, Fig. 59).

37. Next, in Fig. 61, shown below, a surface layer of p-type doping is formed in the same region. (Ex. 1005, 22:57-63). This is accomplished by first using a patterned resist layer 41 with a similar opening as resist layer 40 in Fig. 58, above, and performing ion implantation of boron. (Ex. 1005, 22:57-63).

FIG.61

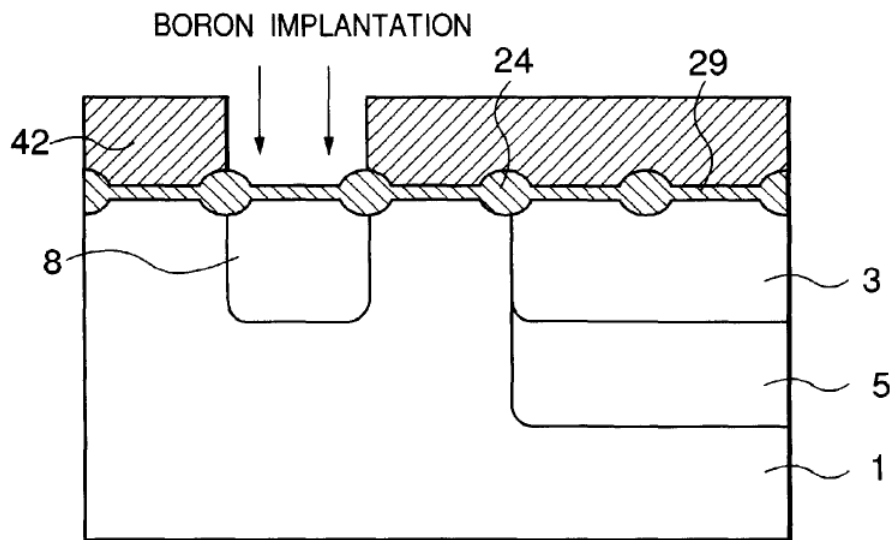


(Ex. 1005, Fig. 61).

38. The boron dopants are added to dopants already present from the p-type substrate and the n-type region 5. (Ex. 1005, Fig. 61, 22:57-63). The boron is a p-type dopant, and is implanted with sufficient concentration and energy to form a “retrograde p-well 3”. (Ex. 1005, Fig. 61, 22:57-63). The term “well” simply means a doped region of a substrate, while a “retrograde well” is a doped region in a substrate where the peak concentration of the dopant is physically deeper than that of the electrically active surface region of any device which may be eventually formed in the well. (Ex. 1018, ¶0045).

39. Figure 62 of Yamashita, shown below, has further steps, for which a different patterned resist layer 42 has been formed. (Ex. 1005, 22:64-23:3). The resist layer 42 has an opening that allows the formation of retrograde p-well 8, by the ion implantation of boron. (Ex. 1005, 22:64-23:3). The retrograde p-well will form the silicon material in which the channel of nMOS (n-channel) FET transistors are formed, with possible additional processing steps to the retrograde p-well 8. (Ex. 1005, Fig. 53, 21:20-24, 21:55-65). The boron atoms are added to dopants already present in the substrate.

FIG.62

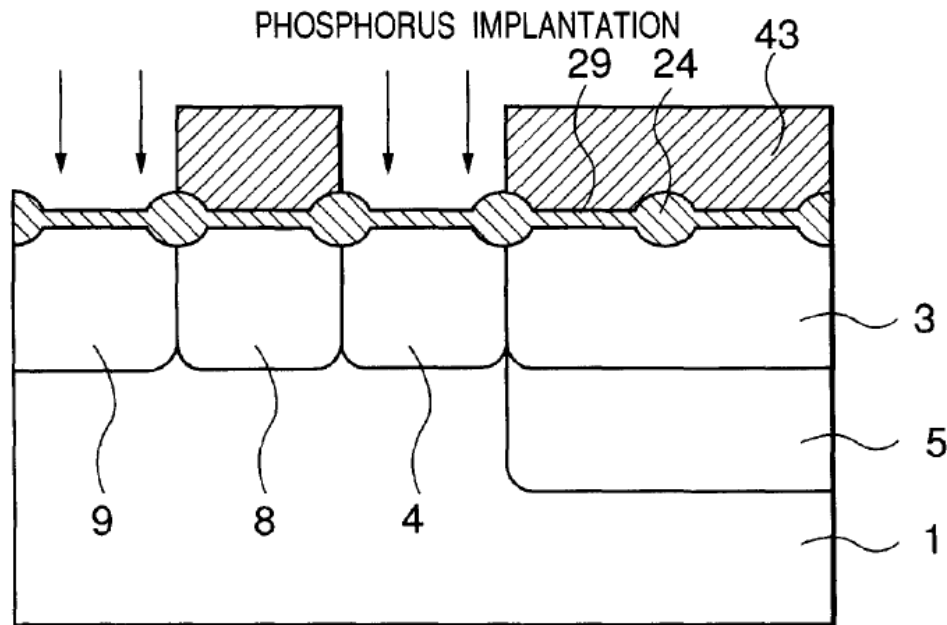


(Ex. 1005, Fig. 62),

40. In Figure 63, shown below, a new resist layer 43 is formed, with openings that allow the implantation of phosphorous to form retrograde n-wells 4

and 9. (Ex. 1005, 23:4-16). The phosphorous atoms are added to dopants already present in the substrate.

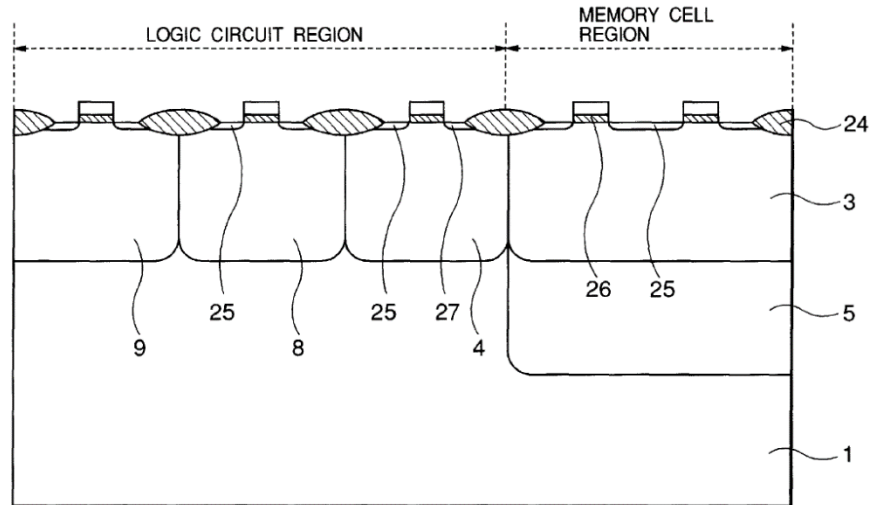
FIG.63



(Ex. 1005, Fig. 63).

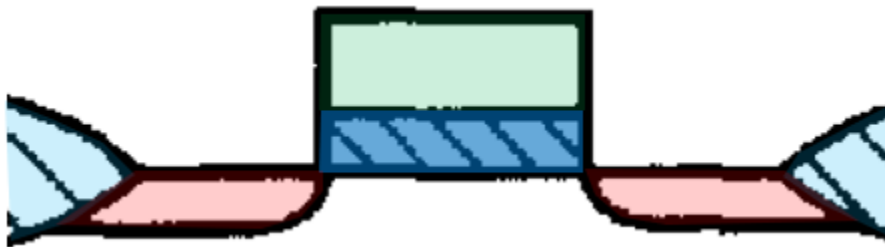
41. The retrograde n wells 4 and 9 will form the silicon material in which the channel of pMOS (p-channel) FET transistors are formed, with possible additional processing steps to the retrograde n-wells 4 and 9. (Ex. 1005, Fig. 53, 21:20-24, 21:55-65).

42. Further processing steps will be carried out to form individual electronic devices. For example, in Fig. 53 (shown below) Yamashita shows that FET (field-effect transistors) will be formed in the retrograde wells 9, 8, and 4:



(Ex. 1005, Fig. 53).

43. The FET transistors are visible, for example, as the following type of structure (magnified from retrograde n well 9 in Fig. 53 and with color added):



44. In the drawing above, the field oxide is visible on the extreme right and left edges, and has been shaded light blue. In the middle, shaded green, is a gate electrode. Underneath the gate electrode, shaded dark blue, is the gate oxide. Immediately underneath the gate oxide is the transistor channel, formed from the material of the retrograde n-well 9 in this case (in retrograde wells 8 and 4, the channel would be formed in the materials of those wells). To the right and left of the channel would be the source and drain of the transistor (shaded red). Because the

transistor well has n-type doping, the source and drain of the transistor will be p-type doped, and would typically be formed from additional applications of resist and boron implants (this will be the same in the retrograde n well 4, but will be the opposite in retrograde p well 8, that is, the source and drain of the transistors will have n-type doping). The source and drain can be structurally indistinguishable. Knowing which is which depends on how the transistor is connected in a larger circuit. The connection in a circuit is arbitrary, but each MOSFET transistor will have both a source and drain.

45. The transistor functions according to a voltage applied to the gate electrode. Normally, the channel region does not conduct electrical current, and thus the source and the drain region are electrically disconnected by the channel. However, in the case of a pMOS transistor, if a sufficiently negative voltage with respect to the source and n-well voltage is applied to the gate electrode (that is, a voltage lower than a so-called “threshold voltage” or V_T), it will attract positive charges to the area of the channel immediately underneath the gate oxide. The gate oxide will prevent the charges from reaching the gate electrode, and so the charges will remain in the channel region. This creates a path for current to flow from the source to the drain. When the negative voltage is removed from the gate electrode, the transistor will stop conducting. For transistors formed in a retrograde p well, such as neighboring retrograde p well 8, the considerations are the same, except that

the threshold voltage is positive. That means that a sufficiently large positive voltage with respect to the source and the p well (V_T) must be applied to the gate electrode, in order to attract electrons to the channel region.

46. The patent at issue here has particular concern for the processes of semiconductor doping, and in particular dopant gradients. To understand such gradients and their effects, it is important to understand the primary ways in which semiconductors are doped.

47. The main methods used for doping silicon wafers during the integrated circuit manufacturing process are (1) epitaxial silicon growth, (2) diffusion, and (3) ion implantation.

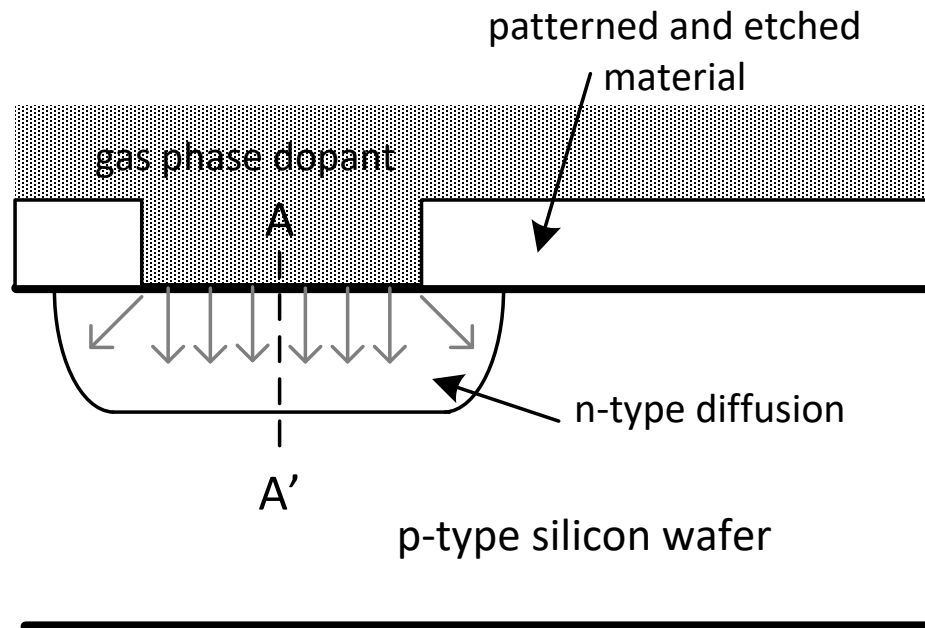
48. **Epitaxial silicon growth** (epitaxy) is a process used to grow a relatively thin, high quality crystalline layer of silicon on a silicon wafer. The base silicon wafers used in semiconductor manufacturing are several hundreds of microns thick, whereas the grown silicon epitaxial layer is typically a few to tens of microns thick. A key advantage of epitaxial deposition is precise control of the dopant concentration in the device regions. The epitaxial (epi) layer is doped as it is grown by introduction of gas phase dopants into the epi reactor. By making the gas dopant concentration static throughout the epi growth process, a layer with a uniform doping profile can be produced with the level of the silicon doping concentration controlled by the gas phase dopant concentration. By changing the gas phase dopant

concentration versus time during the epi growth process, graded doping profiles can be produced.

49. **Diffusion doping** is done by placing patterned silicon wafers into a diffusion furnace. The patterning creates openings in a masking material that is deposited on the silicon wafer. The masking material on the silicon wafer, (such as silicon dioxide) prevents diffusion of dopants into the silicon wafer. The furnace is brought to a specified temperature, and gas phase dopant is then pumped into the furnace and begins diffusing into the silicon wafers where there are openings in the material. The concentration of gas phase dopant, the time and temperature that the gas phase dopant is present, and the total time and temperature after the gas phase dopant is removed, determine the characteristics of the diffusion doping concentration versus depth into the silicon. The concentration versus depth is commonly called a “doping profile”.

50. An illustrative result of diffusion doping is shown in the figure below, which I created. The figure is a conceptual diagram of a cross-section of a portion of a silicon wafer during the diffusion doping process. The gas phase dopant diffuses into the silicon surface and continues to diffuse vertically (in a “depth” direction), and laterally. In this example, the dopant is phosphorous, and produces an isolated n-type region in the p-type substrate. The distance that the dopant

diffuses into the substrate increases with the temperature and time used in the diffusion process.



Cross section of doped region.

51. Figure 9-2 from Wolf and Tauber (Ex. 1032, p. 004), provided below, shows the doping profile, (logarithm of dopant concentration vs. depth in the silicon, for a single gas phase dopant concentration and temperature as a function of total diffusion time. One can see from Figure 9-2 from Wolf and Tauber that the doping concentration continuously decreases with increasing depth into the silicon, (*i.e.*, the profile is graded). A graded doping profile is characterized by having a doping density that is not uniform within the doped region, (*i.e.*, not constant).

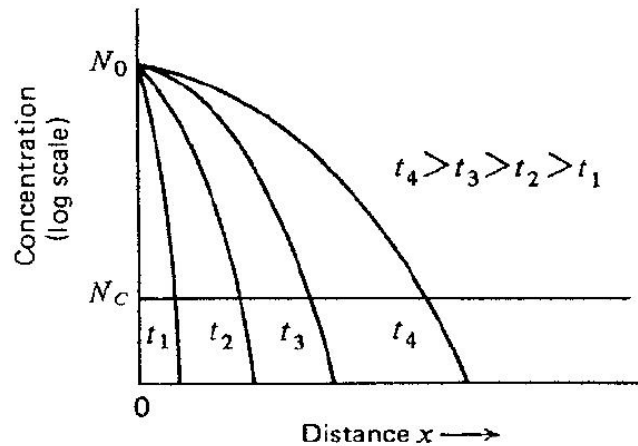
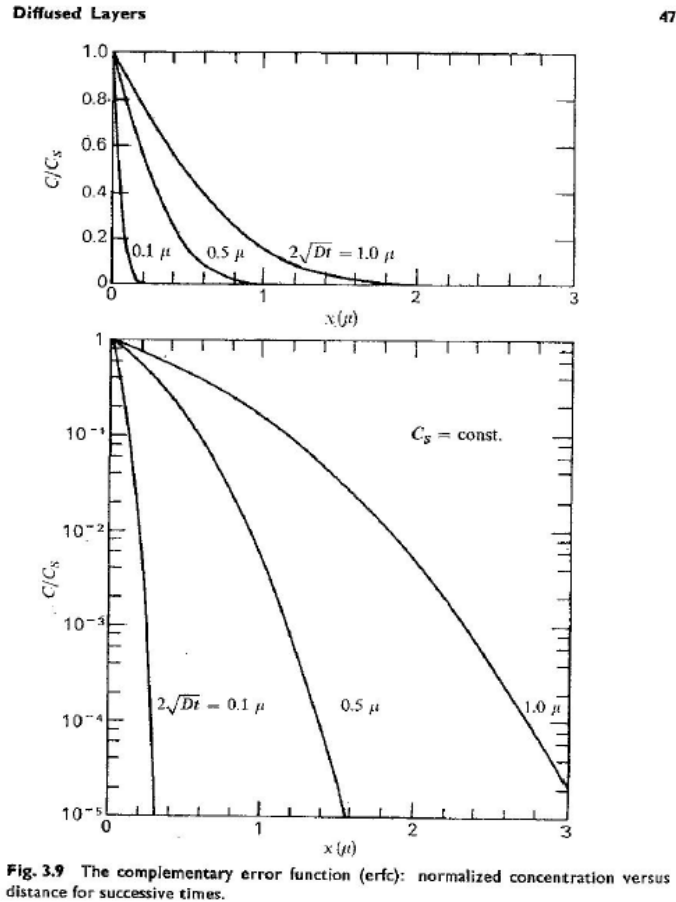


Fig. 9-2 Schematic representation of the diffusion profile for constant source diffusion (pre-deposition). Note the surface concentration remains constant with increasing diffusion time.⁷² From S.K. Ghandi, *VLSI Fabrication Principles*. Reprinted with permission of John Wiley & Sons.

from Wolf and Tauber, *Silicon Processing for the VLSI ERA*, © 2000.

52. Figure 3.9 from Grove (Ex. 1030, p. 003, reproduced below) shows the doping profile for a constant gas phase dopant concentration for various times, (two graphs, one with a linear axis for normalized dopant concentration, and one with a log axis like that in Fig. 9-2 from Wolf and Tauber). These are also graded doping profiles.



From A. S. Grove, Physics and Technology of Semiconductor Devices; © 1967.

53. **Ion implantation** doping is performed by implanting ionized atoms into patterned silicon wafers with enough energy to penetrate into the silicon at a desired depth. This is done by accelerating atomic ions with an electric field and directing them into the silicon wafer. This is analogous to shooting pellets (ionized atoms) into jello (silicon). The doping concentration is controlled by the number of ionized atoms implanted. The peak of the doping concentration is controlled by the energy of the ionized dopant atoms, (higher energy causes a peak concentration deeper from the surface). Implantation provides finer control over the dopant

concentration compared to diffusion doping, and has been the most common doping method (including in the relevant timeframe). After implantation, the dopants are activated by going through an anneal process at high temperature. The anneal process, as well as subsequent processing steps after the implantation that require high temperatures, cause some diffusion of the implanted dopant atoms, which is dependent on the length and temperature of the anneal process. The implant energy, implant dose (*i.e.*, the number of atoms implanted), and total time and temperature of annealing and other process steps after the implant was done, control the doping profile.

54. An illustrative result of ion implantation is shown in Fig. 5 from Sze (Ex. 1031, p. 005) below. Figure 5 shows the doping profile for boron implanted at a single implant dose for various implant energies prior to the anneal process.

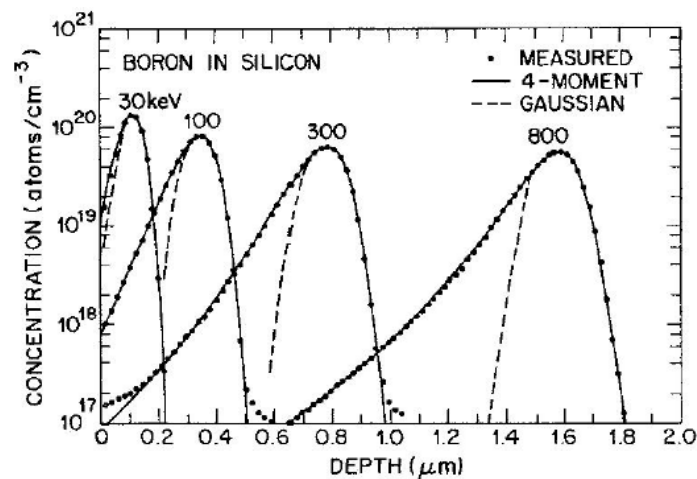


Fig. 5 Boron implanted atom distributions, with measured data points, and four-moment (Pearson-IV) and symmetric Gaussian curves. The boron was implanted into amorphous silicon without annealing. (After Hofker, Ref. 21.)

FIG.5: doping profiles formed by ion implantation; from Sze, VLSI Technology, ©

1983

55. One can see that the peak of the dopant concentration moves deeper into the silicon as the implant energy increases, and can be well-predicted, (*i.e.*, the measurements match theory). Figure 5 from Sze shows the doping profiles and free carrier profiles for boron implantations done at a single energy and dose, 30 Kilo-electron-Volts (KeV) and 10^{15} atoms per cm^2 respectively, with two different anneal temperatures. Anneals must be performed at a temperature that is high enough to activate the implanted dopant to produce free carriers. From Fig. 19 of Sze (Ex, 1031, p. 006, reproduced below), it is evident that annealing at 800 °C does not sufficiently activate all of the implanted boron atoms (free carriers are less than the boron concentration). Annealing at 900 °C is sufficient to activate all of the boron atoms, (free carriers match the boron concentration). It is evident from Figures 5 and 19 from Sze that the doping concentration continuously decreases (*i.e.*, there is a gradient) to either side of the peak dopant concentration. In some cases the peak is placed at or very near the surface of the silicon, producing a profile that continuously decreases with depth into the silicon, similar to that of a diffusion doping profile. These are all graded doping profiles.

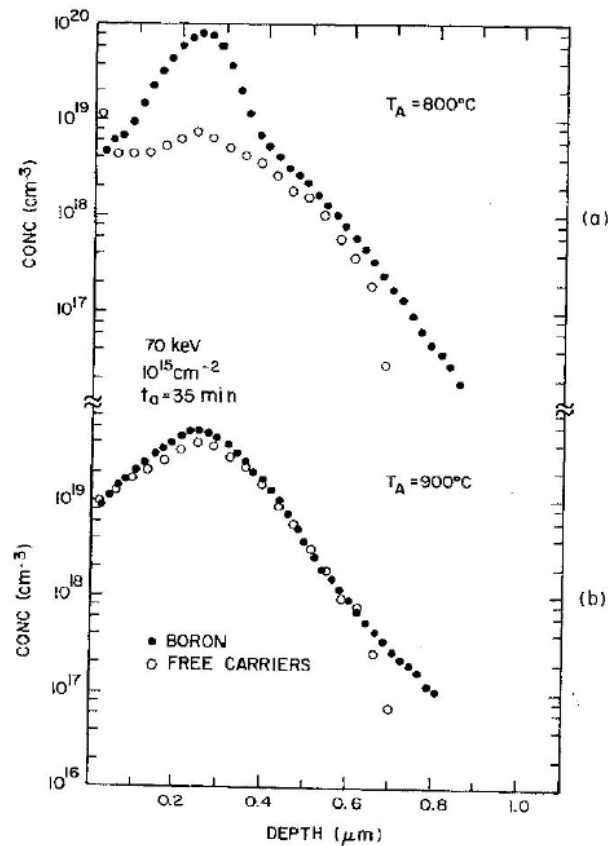


Fig. 19 Concentration profiles of boron atoms (SIMS—solid dots) and corresponding free-carrier concentrations (Hall data—open circles). (a) At 800°C and (b) at 900°C. (After Hofker, Ref. 21.)

Doping profiles and free carrier profiles from S.M. Sze, VLSI Technology. © 1983

56. Some examples of common and conventional dopant profiles for different types of semiconductor devices are shown in the Figures below. Figure 16-10 from Wolf and Tauber (Ex. 1031, p. 011, reproduced below) shows a conventional n-well that is used in p-type MOS transistors. This conventional n-well region has a graded doping profile. Figure 16-23 (Ex. 1032, p. 014, reproduced below) is a retrograde p-well used in n-type MOS transistors. This also has a graded doping profile. Fig. 1g from Sze (Ex. 1031, p. 008, reproduced below) is a doping

profile of various bipolar transistors, showing emitter, base and collector regions. One can see that the emitter, base, and collector regions all have doping profiles that are graded. Fig. 33 from Sze (Ex. 1031, p. 009) is a doping profile through the gate of n-channel (n-type MOS) and p-channel (p-type MOS) devices in conventional a CMOS semiconductor device. It is evident that the vast majority of semiconductor device regions can be characterized as having a graded dopant concentration.

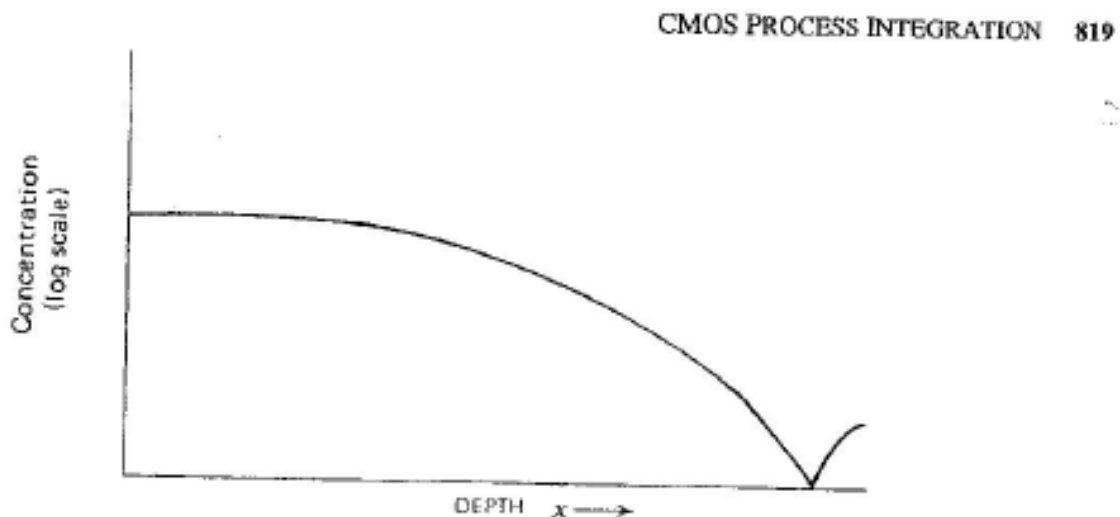


Fig. 16-10 Doping profile in a conventional well formed by a shallow implant and a drive-in step.

Conventional well implant doping profile; from Wolf and Tauber, Silicon Processing for the VLSI ERA, © 2000

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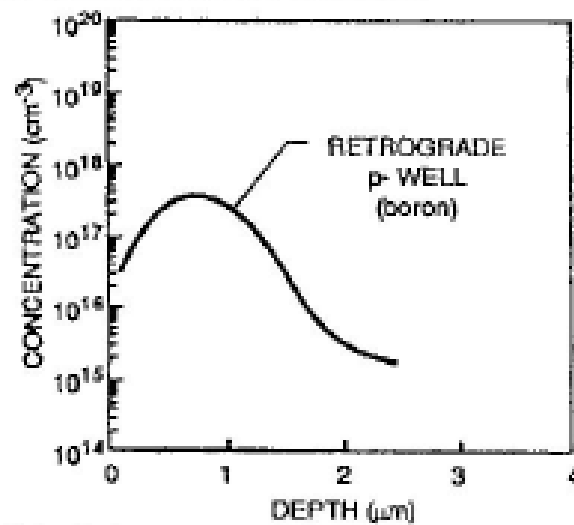


Fig. 16-23 Example of the doping profile of a retrograde *p*-well (boron) implant (400 keV).

Retrograde p-type well implant doping profile; from Wolf and Tauber, Silicon Processing for the VLSI ERA, © 2000

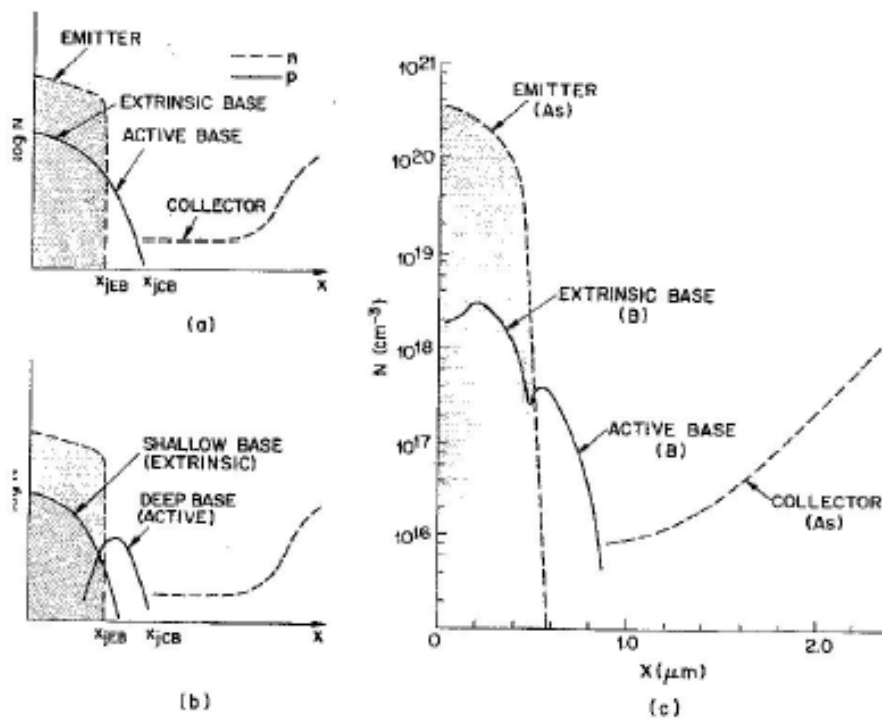
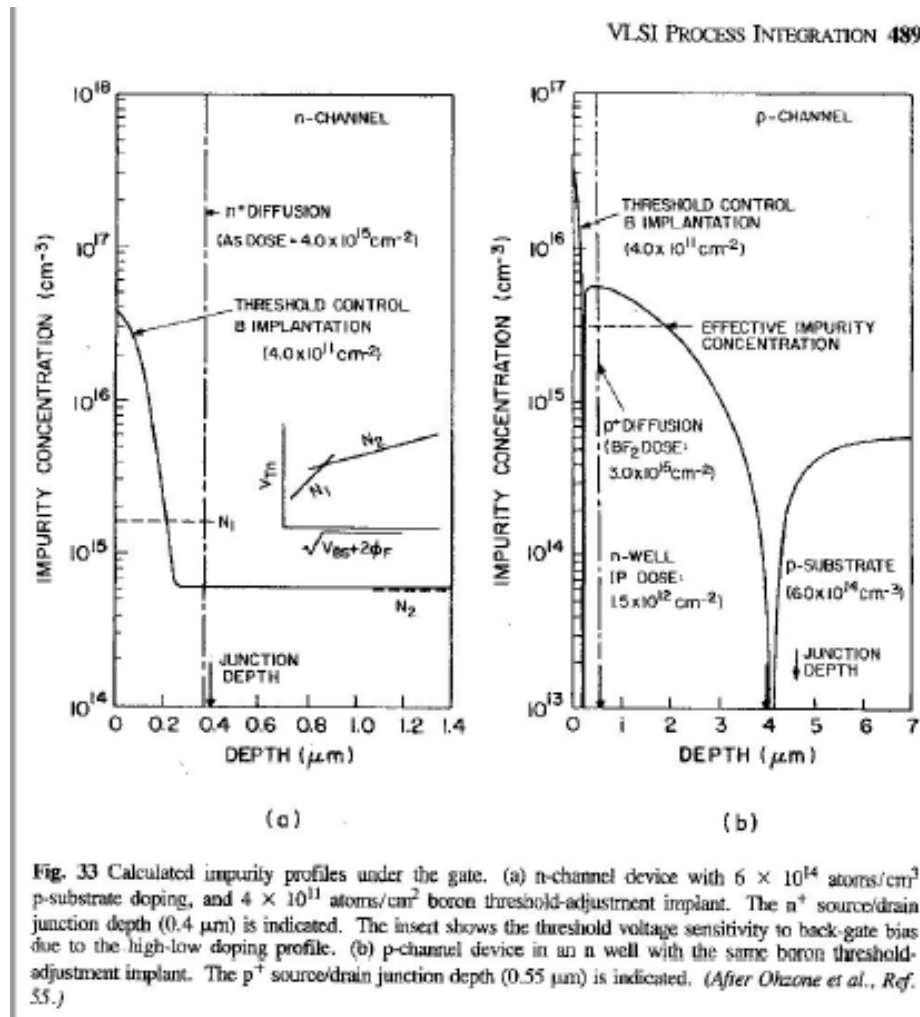


Fig. 4 n-p-n transistor doping profiles. (a) Single-base implant (schematic). (b) Double-base implant (schematic). (c) Single-base implant (actual).

Various bipolar transistor doping profiles; from S.M. Sze, VLSI Technology. © 1983



N-channel and p-channel MOS device doping profiles in a CMOS device; from S.M. Sze, VLSI Technology. © 1983

57. There is a known relationship between graded dopant profiles, the movement of charge carriers (electrons and holes), and electric fields that can be derived directly from the laws of physics. It has been well known for many decades that a region with a graded dopant concentration profile will produce an electric

field. The electric field produced is a function of the rate of change of the dopant concentration versus distance (depth into the silicon and/or laterally along the same depth of silicon). In order to illustrate the reasons for this, it is helpful to review energy band diagrams for semiconductor materials.

58. In general, materials can be characterized by energy bands. This is shown in Fig. 2.8 of Pierret below (Ex. 1029, p. 003). Materials have a valence band energy level (E_v) and a conduction band energy level (E_c). For energy levels below E_v , the energy states are occupied with electrons. In order to provide carrier transport (conduct electricity), the electrons must have sufficient energy imparted to them to be excited to the conduction band. The difference in E_c and E_v is referred to as the “bandgap”, or E_g . For insulator materials the E_g is very large and it takes a very large amount of energy for electrons to be excited to the conduction band. Therefore, insulators do not conduct electricity. For metal materials, E_v and E_c overlap, and therefore readily conduct electricity. Semiconductors have a small bandgap and therefore can conduct electricity if they are doped, or have sufficient energy (a much lower energy than an insulator) transferred to them, (*e.g.*, by heat or light). In a perfect silicon crystal, there are no energy states within the bandgap.

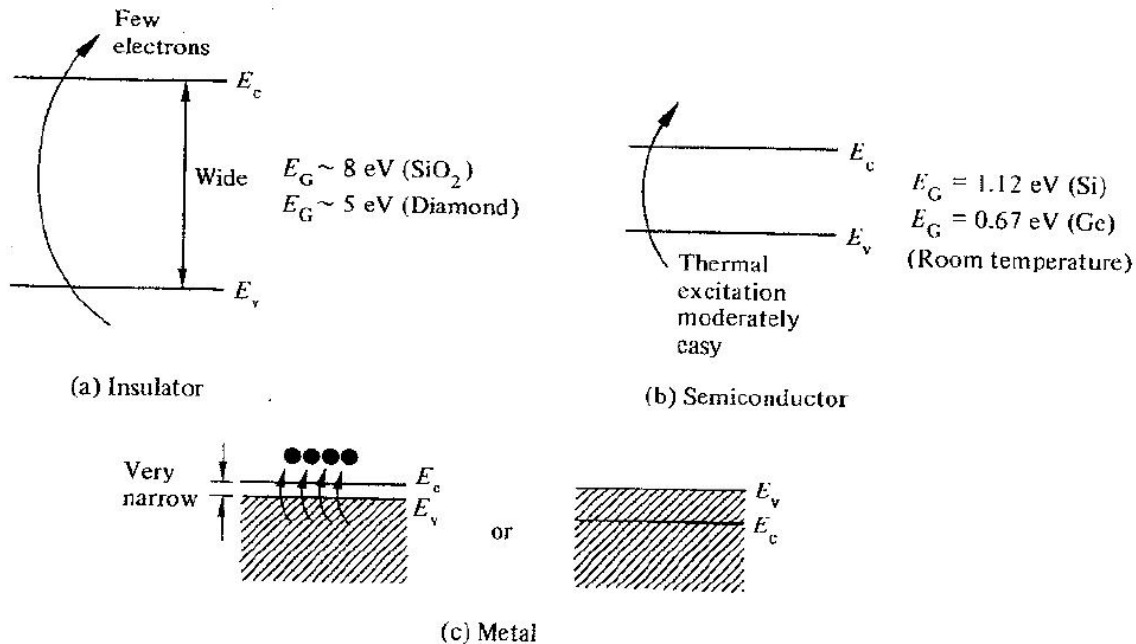


Fig. 2.8 Explanation of the distinction between (a) insulators, (b) semiconductors, and (c) metals using the energy band model.

59. By doping the silicon, (*i.e.*, adding an impurity to the silicon crystal), a new energy level is introduced within the bandgap. N-type dopants (donors) produce an energy level in the bandgap region that is close to E_c . P-type dopants (acceptors) produce an energy level that is close to E_v . Fig. 2.13 of Pierret (Ex. 1029, p. 006), shown below, illustrates the donor and acceptor energy states (E_D and E_A respectively) in the bandgap region. One can see that if a dopant is added, room temperature provides sufficient energy to move electrons (black filled circles) from the donor energy state to the conduction band where they provide carrier transport, (and similarly moved from the valence band to the acceptor energy state, leaving holes (white filled circles) behind in the valence band that provide carrier transport).

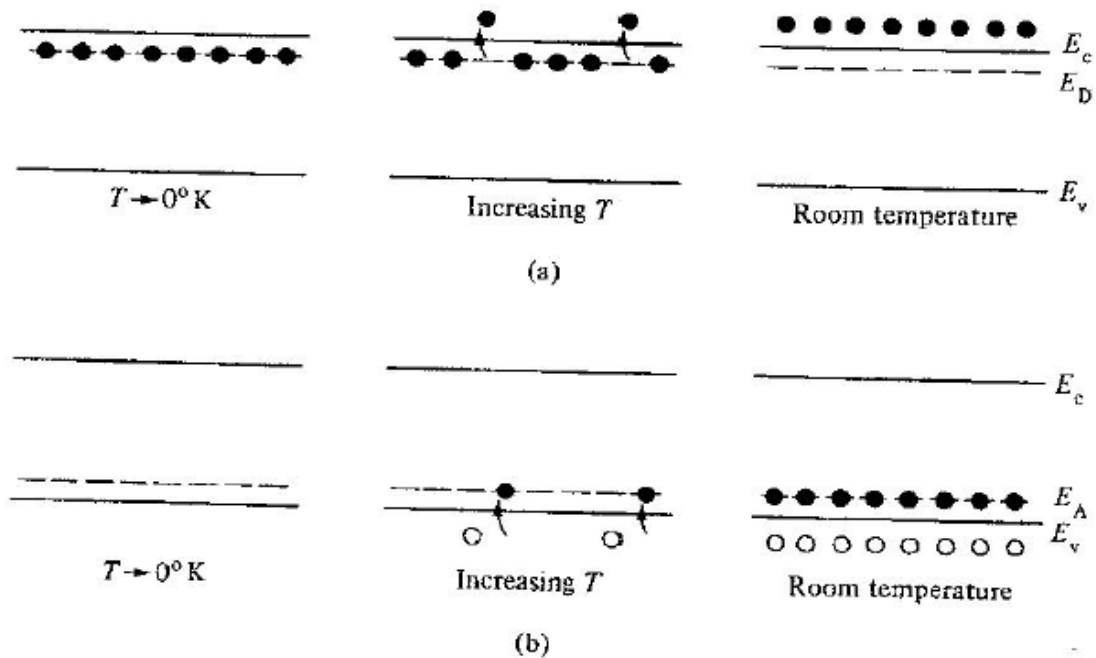


Fig. 2.13 Visualization of (a) donor and (b) acceptor action using the energy band model.

60. Another important detail in the energy band diagrams of material is the so-called Fermi energy level or Fermi-level. This is the energy state where the probability of being occupied by electrons is 50%. The Fermi level is situated at half the energy from E_v to E_c for undoped (intrinsic) silicon. As dopants are added the Fermi level shifts towards E_c for n-type dopants and towards E_v for p-type dopants. This is shown in Fig. 2.18 of Pierret (Ex. 1029, p. 009) below. The amount that the Fermi level is shifted also depends on the doping concentration as shown in Fig. 2.21 of Pierret (Ex. 1029, p. 010) below.

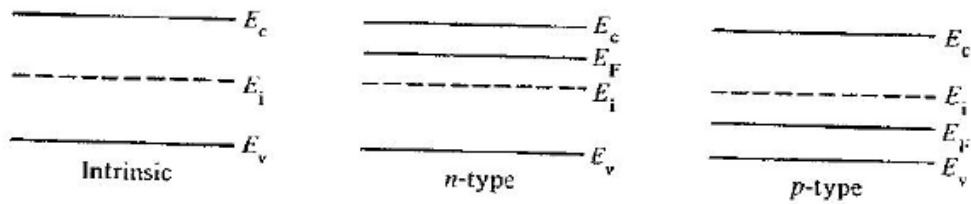


Fig. 2.18 "At a glance" representation of intrinsic (left), n -type (middle), and p -type (right) semiconductor materials using the energy band diagram.

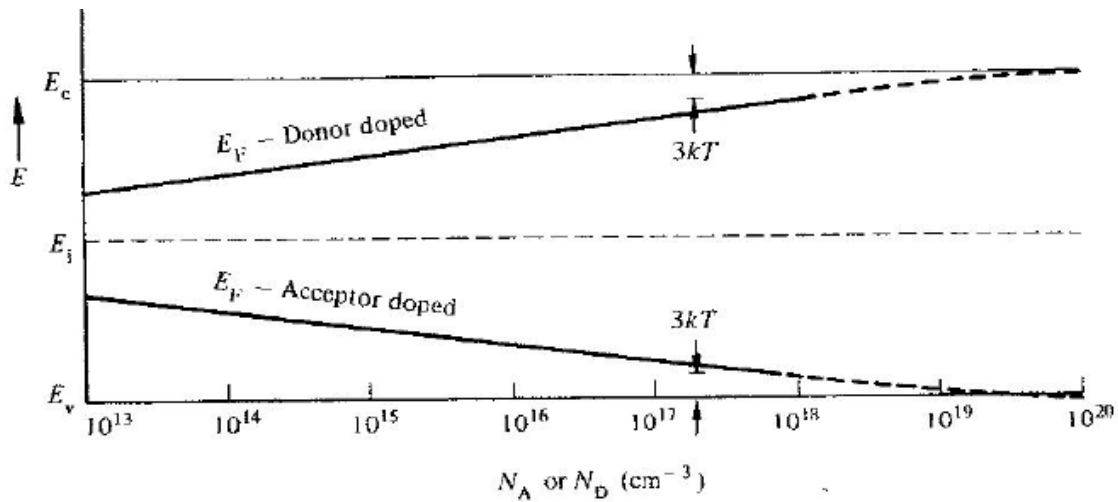


Fig. 2.21 Fermi level positioning in Si at room temperature as a function of the doping concentration. The solid E_F lines were established using Eq. (2.41) for donor doped material and Eq. (2.43) for acceptor doped material ($kT = 0.026$ eV, and $n_i = 10^{10}/\text{cm}^3$).

61. Since the Fermi level is defined by the probability of being occupied is 50%, it must be positionally continuous in a region of silicon with a positional variation in doping concentration. As a result, band bending of E_v and E_c occurs for graded dopant concentrations as shown in Fig. 3.13 of Pierret (Ex. 1029, p. 013) below. E_f is constant with respect to position or region in the silicon (*e.g.*, depth into), but E_c and E_v vary with position according to the doping concentration.

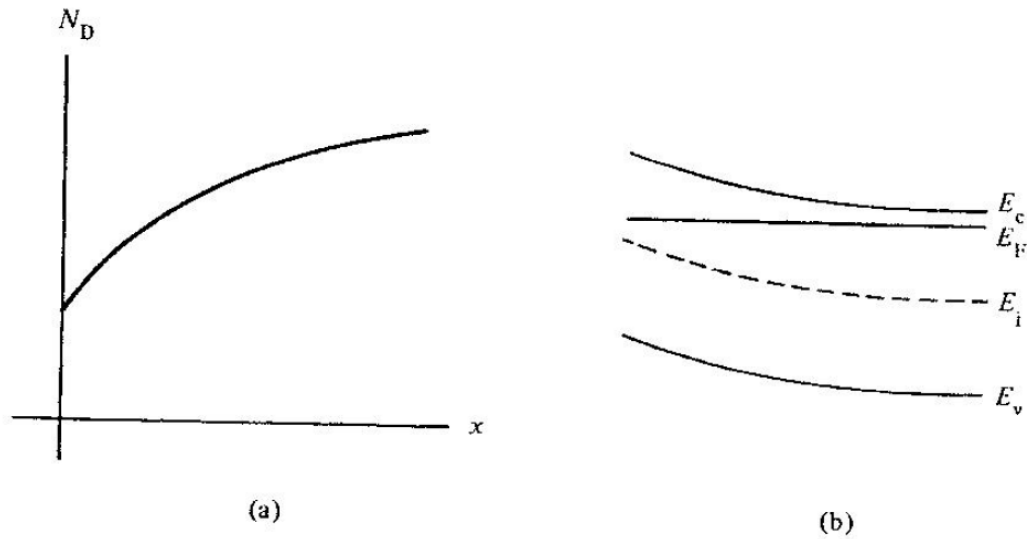


Fig. 3.13 Nonuniformly doped semiconductor: (a) assumed doping variation with position; (b) corresponding equilibrium energy band diagram.

The positional change in E_c and E_v produces an electric field. An electrical field is defined as the rate of change of an electrostatic potential, (*e.g.*, the positional rate of change in E_c and E_v energy level in electron-volts (eV)). This is illustrated in Fig. 3.9 of Pierret (Ex. 1029, p. 012), shown below. It was well-known that free carriers will be moved by an electric field, a process referred to as drift. An integral electric field (*i.e.*, present under zero bias and thermal equilibrium) can be produced by non-uniform doping versus position (*i.e.*, a graded dopant region) as has been described, or by applying an external voltage difference across a doped semiconductor.

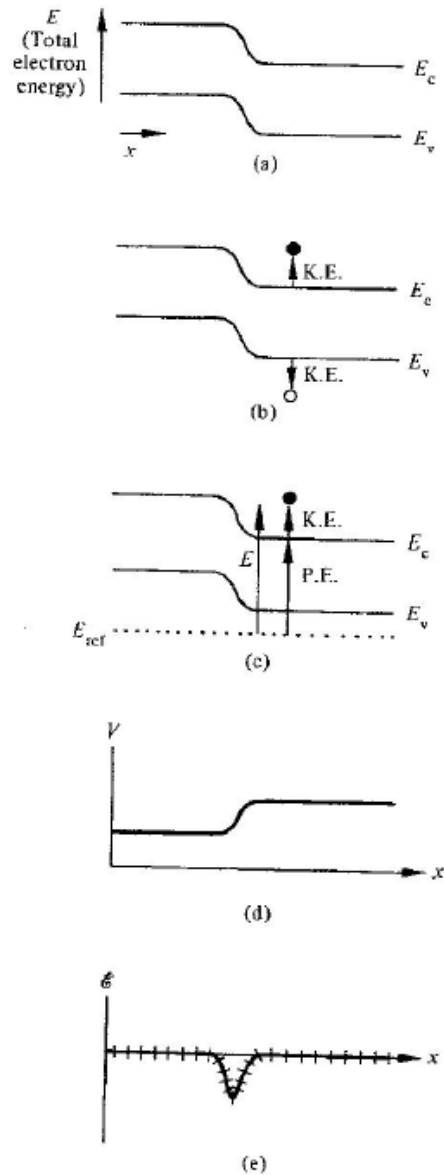


Fig. 3.9 Relationship between band bending and the electric field within a semiconductor: (a) sample energy band diagram; (b) identification of the carrier kinetic energies; (c) specification of the electron potential energy; (d) electrostatic potential and (e) electric field versus position dependence deduced from and associated with the part (a) energy band diagram.

62. It is well known that electrons (which have a negative charge) will move towards the more positive potential, and holes (which have a positive charge) will move towards the more negative potential. This is shown in Fig. 3.1 of Pierret (Ex. 1029, p. 011), below. Annotations are added to each Figure to show the

movement of electrons (majority carrier in n-type silicon, minority carrier in p-type silicon), and holes (majority carrier in p-type silicon and minority carrier in n-type silicon). It is clear that electrons and holes are aided in transport by an electric field in opposite directions due to their opposite charge.

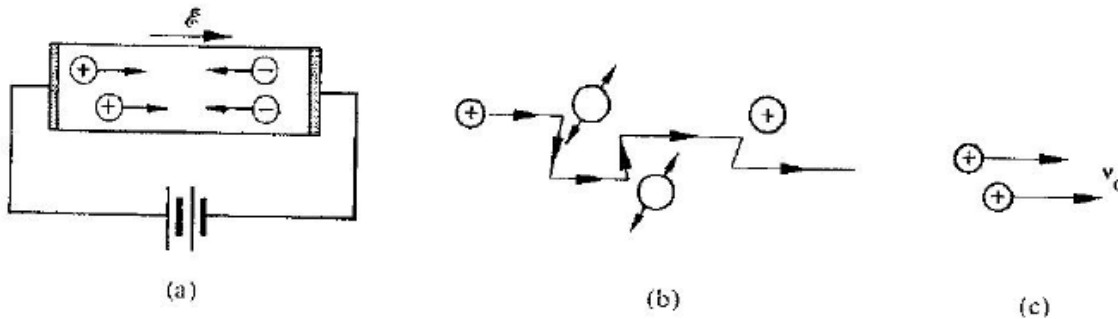
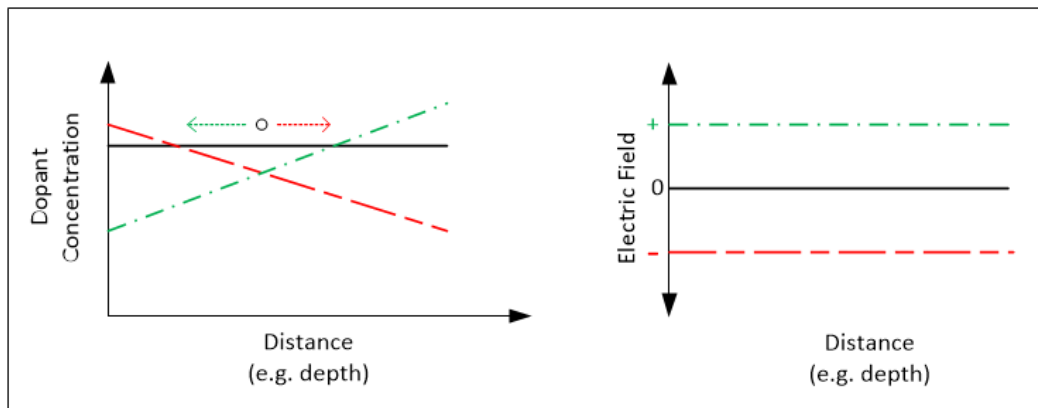


Fig. 3.1 Visualization of carrier drift: (a) motion of carriers within a biased semiconductor bar; (b) drifting hole on a microscopic or atomic scale; (c) carrier drift on a macroscopic scale.

63. This concept is illustrated in the Figure below, which I created. The Figure shows three different doping profiles, (1) a uniform or constant doping concentration, (2) a linearly decreasing doping concentration and (3) a linearly increasing doping concentration. The corresponding electric field vs depth is shown in the figure on the right.



Dopant concentration versus depth and corresponding electric fields.

64. The uniform profile (black solid line) has no change in doping versus distance and therefore the electric field is zero. Doping profile 2 (red dashed line) has a linearly decreasing dopant, therefore the electric field is the slope of profile which is a constant negative electric field. Doping profile 3 has a linearly increasing dopant (dash dot green line), therefore the electric field is the slope of profile which is a constant positive electric field. Analogous to a ball on physical topography, where the ball will move preferentially in a direction according to the slope of the topography, a free minority carrier (*e.g.*, an electron in semiconduction device region that is p-type) will move in the direction of decreasing p-type dopant concentration. This is shown by the circle in the Figure above, and the arrows corresponding to the increasing and decreasing dopant profiles.

65. This effect is described and utilized to improve the switching speed performance of a photodiode in a paper by A. G. Jordan et. al., "Photoeffect on Diffused P-N Junctions with Integral Field Gradients", IEEE Transactions on Electron Devices, October 1960. According to the summary shown below, the electric field produced by the impurity (dopant) distribution assists the transport of minority carriers.

Summary—A detailed analysis of a diffused junction photodiode is presented in which the illumination, monochromatic or broadband, is applied to the diffused face. The electric field produced by the impurity distribution, assumed exponential, assists the transport and collection of minority carriers created by photons absorbed in the graded region.

66. The device cross section and doping profile is shown below, (Figs. 3 and 4 from the paper).

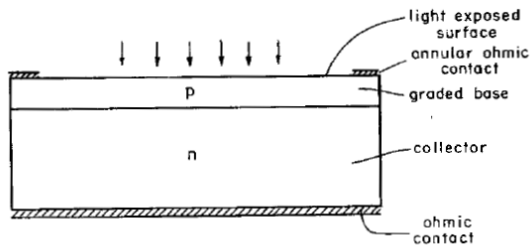


Fig. 3—Schematic diagram of a drift photodiode.

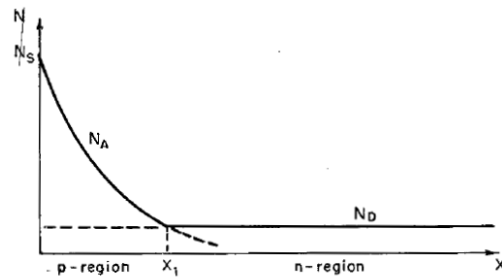


Fig. 4—Impurity profile of a graded base p - n photodiode.

67. The paper describes the electric field in terms of the doping profile, and that the electric field produced by the graded doping profile helps minority carriers move away from the surface (light exposed surface) towards the junction. Jordan states:

Since N_a is a function of x , the gradient of hole density produces a diffusion current $D_p dp/dx$, until the slight displacement of majority carriers which thus occurs creates an electric field E and an opposing and equal current $\mu_p pE$. Hence, in equilibrium,

$$E = \frac{D_p}{\mu_p} \frac{1}{p} \frac{dp}{dx}, \quad (5)$$

or from the Einstein relationship and (4)

$$E = \frac{kT}{q} \frac{1}{N_a(x)} \frac{dN_a(x)}{dx}. \quad (6)$$

Since the acceptor concentration decreases monotonically from the surface, its x range of change is negative, and therefore, the field is negative; that is, it points from the junction to the surface, helping the minority carriers, electrons, injected by the light to travel towards the junction.

68. It is clear from the material presented that graded dopant concentration profiles have been common in semiconductor devices for several decades. In addition, it has been known for several decades that graded dopant profiles create an electric field. It has further been well known for several decades that an electric field will assist in the movement of minority carriers, and majority carriers which move in the opposite direction of minority carriers in the presence of an electric field.

V. LEVEL OF ORDINARY SKILL IN THE ART

69. The level of ordinary skill in the art encompassed a person having a Bachelor's Degree in electrical engineering, microelectronics engineering or a related field and three years of experience relating to semiconductor device manufacturing, where a higher level of education may substitute for experience and vice versa.

VI. RELEVANT TIMEFRAME FOR DETERMINING OBVIOUSNESS

70. I understand that obviousness must be evaluated at the time the alleged invention was made. From the first and second page of the '014 patent (left column, field “[65] Related U.S. Application Data”), I understand that the earliest patent application was filed on September 3, 2004. I will assume for the purpose of this report that September 3, 2004, is the date the purported invention was made, with the understanding that my testimony will also be applicable to some time prior to September 3, 2004, approximately in the early-to-mid 2000s. I may refer to this time period as the “relevant time frame”, and my testimony concerning obviousness is directed to this timeframe, even if I occasionally do not explicitly use a past tense.

VII. DETAILED EXPLANATION OF THE REASONS FOR UNPATENTABILITY

Ground 1. Claims 1-15, 17, and 20-30 were obvious over Yamashita

71. In my opinion, claims 1-15, 17, and 20-30 were obvious under 35 U.S.C. §103(a) over U.S. Pat. No. 6,420,763 (“**Yamashita**”)(Ex. 1005).

A. Overview of the Combination

72. Yamashita teaches semiconductor devices for, *e.g.*, DRAM in integrated circuits. (Ex. 1005, 1:7-15). Yamashita, on its own, expressly teaches almost all elements of the claims. In my opinion, Yamashita nonetheless renders the claims obvious. First, to the extent the preamble of claims 1 and 21 are limiting,

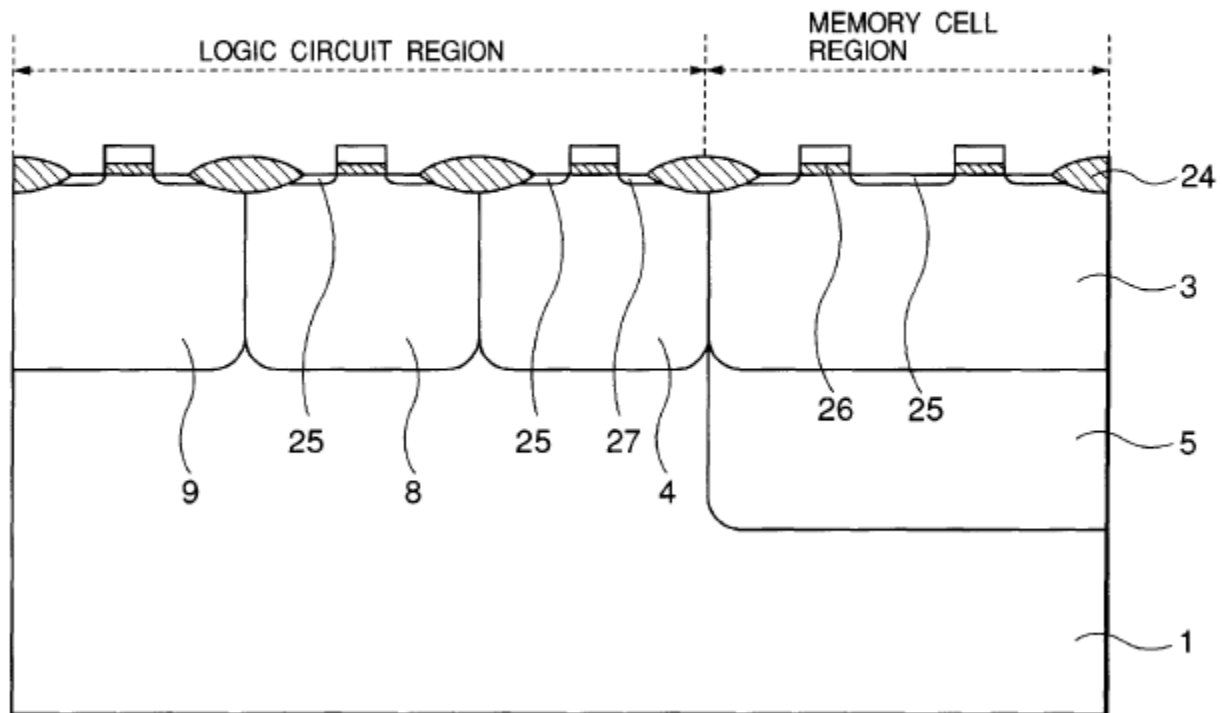
Yamashita renders obvious an “electronic device” by teaching semiconductor devices useful for memory. This Ground posits that it would have been obvious to use Yamashita in an electronic device. Second, Yamashita describes retrograde n-wells and retrograde p-wells. “Retrograde” wells are wells that have a dopant level peak below the surface. (Ex. 1005, Fig. 55, 21:35-41). While Yamashita expressly shows a dopant profile concentration having a graded dopant profile in a retrograde p-well, it does not illustrate the corresponding graded dopant concentration profile in a retrograde n-well, which would have been obvious. Third, Yamashita teaches that graded dopant profiles create potential gradients that aid carrier movement, and the ability to aid carrier movement in the specific Eighth Embodiment on which the Ground relies would have been obvious. Finally, it is my opinion that the dependent claims were obvious, as explained in detail in the claim mapping section where appropriate. The Rationale underpinning other obviousness grounds will be presented in the Claim Mapping section, under each claim element as appropriate.

B. Rationale (Motivation) Supporting Obviousness

73. In my opinion, it would have been obvious to use Yamashita’s devices in an electronic system.

74. Yamashita teaches semiconductor structures useful for memory (and in particular, DRAM) having both a logic circuit region and a memory cell region, as shown with respect to the Eighth Embodiment in Fig. 53, reproduced here:

FIG.53



(Ex. 1005, Fig. 53, 6:1-2, 21:19-34). Yamashita states:

“The semiconductor device is divided roughly into an element region (a memory cell region) for storing information of large-capacity mainly and an element region (a logic circuit region) for executing logical calculations while exchanging information of large-capacity with the memory cell region.”

(Ex. 1005, 21:27-33).

75. Yamashita renders obvious “electronic systems” because it teaches “semiconductor devices” (Ex. 1005, Title, Abstract, 21:19-24), which are themselves “electronic systems”.

76. Second, to the extent that an “electronic system” means something other than a “semiconductor device”, it was well-known in the relevant timeframe that semiconductor devices were used *within* electronic systems. For example, Yamashita expressly teaches the use of its circuits in memory. (Ex. 1005, Fig. 53, 21:20-34). It was well-known in the relevant timeframe that memory, including DRAM, was used in computers, appliances, and other types of electronic systems. It would have been obvious to use Yamashita’s circuits for logic and memory in memory devices, computers, and other systems because that was the purpose of computer memory in the relevant timeframe.

77. A person having ordinary skill in the art (“POSITA”) further would have found the combination obvious because Yamashita represents a known type of integrated circuit that required circuitry for DRAM and logic circuits, and would have been used for its known purpose in a predictable manner.

78. Other aspects of the Rationale supporting obviousness will be explained below in the Claim Mapping section, below, under the claim limitation to which the obviousness argument pertains.

C. *Graham* Factors

79. The **level of ordinary skill** is discussed above in ¶69.

80. The **scope and content of the prior art** are discussed throughout the Ground.

81. The **differences between the prior art and the claims** are discussed in the section entitled “Rationale (Motivation) Supporting Obviousness”, above, and in the claim mapping, below.

82. I am not aware of any **secondary considerations** that would make an inference of non-obviousness more likely.

D. Reasonable Expectation of Success

83. A POSITA in the relevant timeframe would have had a reasonable expectation of success in using the prior art in the manner I discuss herein. At the level of the claims of the '014 patent, the art was relatively predictable in the relevant timeframe (September 2004), with commercially-available sophisticated circuit design, process modeling and physics-based transistor modeling software tools available. A POSITA would have been able to make any necessary modifications to implement the Ground, and in particular would have been able to adjust doping gradients, electric fields created by dopant gradients and carrier movement to effect the purposes of Yamashita.

E. Analogous Art

84. Yamashita is analogous art because it is directed to the same field as the '014 patent (semiconductor devices). (Ex. 1001, claim 1, Abstract, 1:39-46)(Ex. 1005, Title, Abstract). Furthermore, the teachings of Yamashita would have been

reasonably pertinent to the problems facing the named inventors, *i.e.*, the improvement of memory function. (Ex. 1001, 3:48-4:1)(Ex. 1005, 1:12-3:22).

F. Claim Mapping

85. This section maps the challenged claims to the relevant disclosures of Yamashita, where the claim text appears in bold-italics, and the relevant mapping follows the claim text. There is added numbering and lettering in brackets (*e.g.*, 1[a], [1b]) to certain claim elements, to facilitate the discussion.

CLAIM 1

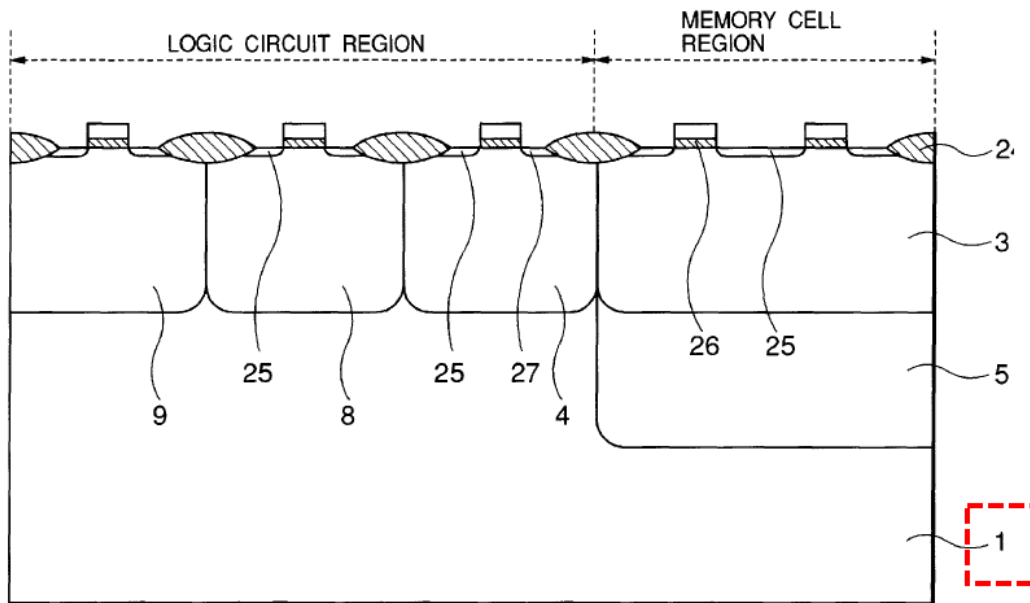
“1[a] An electronic system, the system comprising: at least one semiconductor device, the at least one semiconductor device including:”

86. Yamashita teaches and renders obvious an electronic system comprising at least one semiconductor device. Specifically, Yamashita teaches semiconductor devices (integrated circuits), which are also electronic systems that in turn contain smaller semiconductor devices, such as transistors and capacitors. (Ex. 1005, Title, 1:7-16, 2:63-67). As discussed above, it would have been obvious to include the semiconductor device of Yamashita in an electronic device for the reasons discussed in the section above entitled “Rationale (Motivation) Supporting Obviousness”.

“[1b] a substrate of a first doping type at a first doping level having a surface;”

87. Yamashita teaches **a substrate of a first doping type at a first doping level having a surface**. Yamashita teaches a semiconductor device having a **substrate 1**, as shown below in the reproduction of Fig. 53 of Yamashita, with an added, red-dashed box to show the reference numeral 1 of the substrate:

FIG.53



(Ex. 1005, Fig. 53, 6:1-2, 21:20-24, 22:19-24, 7:19-21).

88. The substrate 1 is “p type semiconductor substrate 1 containing boron of a concentration on the order of $1 \times 10^{16} / \text{cm}^3$ ”. (Ex. 1005, 6:1-2, 21:20-24, 22:19-24, 7:19-21). Thus, the substrate is **of a first doping type (p type) at a first doping level ($1 \times 10^{16} / \text{cm}^3$)**. (Ex. 1005, 8:13-14). The substrate is at a first doping level because it is doped to be p-type and is therefore doped to a specific level that

constitutes a first doping level. The substrate has a top **surface** (the top surface of the device shown in Fig. 53), as indicated in the figure.

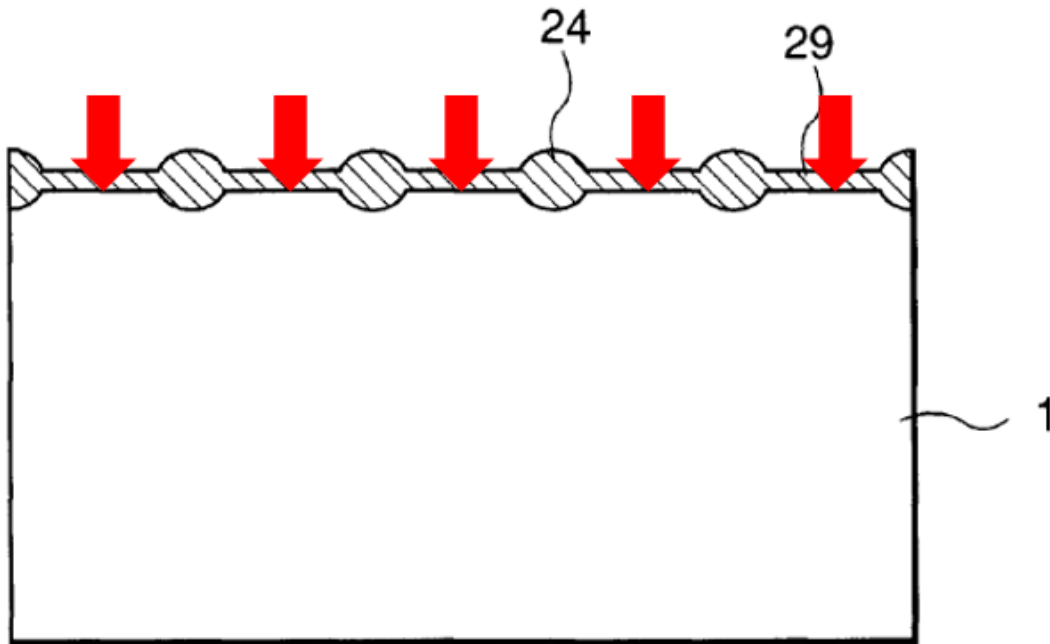
“[1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;”

89. Yamashita teaches a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type within which transistors can be formed. First, Yamashita teaches a series of active regions separated by separation regions:

“As shown in FIG. 57, the field oxide film 24 is formed on the separation region on the main surface of the p type semiconductor substrate 1 containing boron of concentration on the order of 1×10^{16} / cm^3 , **and the oxide film 29 for the gate oxide film 26 is formed on the active region.”**

(Ex. 1005, 22:33-37)(Emphasis added) Figure 57 of Yamashita (referenced in the quote above) is reproduced below, with the locations of the eventual active regions indicated with added red arrows:

FIG.57



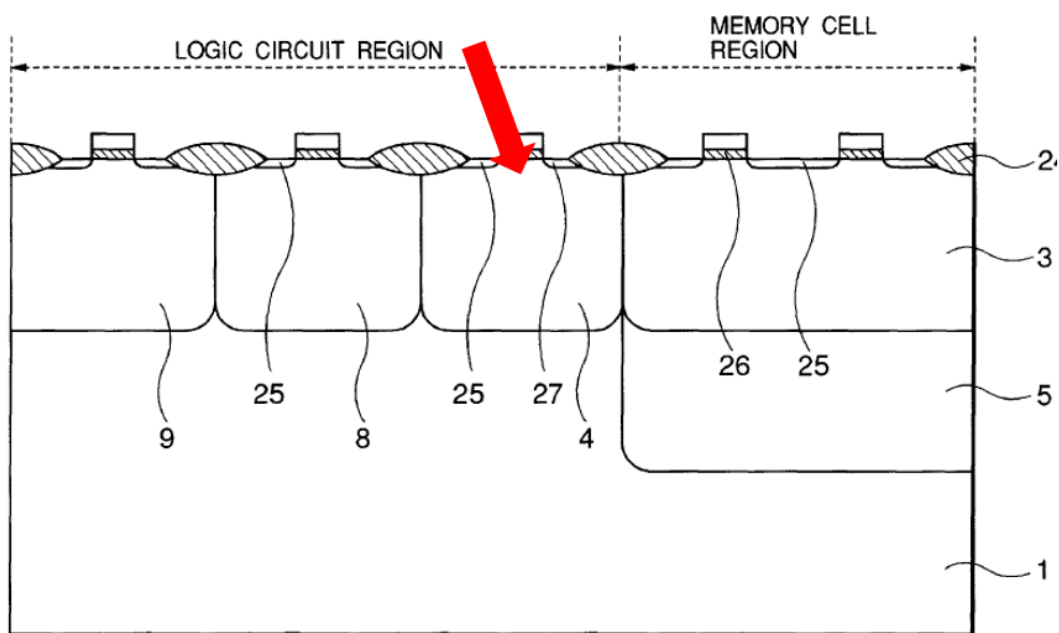
(Ex. 1005, 6:9-10, 22:29-39). The active regions at this stage in manufacturing are covered by a thin gate oxide, and separated by thick portions of field oxide 24. (Ex. 1005, 22:33-37). The field oxide has the function of isolating active regions from one another. (Ex. 1005, 22:33-37). The “gate oxide”, after later steps, will become the oxide that separates gate electrodes from transistor channels in MOSFET transistors.

90. The active regions are disposed **adjacent to the top surface of the substrate 1**. (Ex. 1005, Fig. 57, 22:33-37).

91. Yamashita teaches that certain active regions will have n-type doping, which is **a second doping type opposite in conductivity to the first doping**

type (which is p-type, as discussed above under claim limitation [1b]). (Ex. 1005, 23:4-16, 21:55-58, 21:66-22:1, 21:20-24, 22:7-9). The **first active region** with an n-type doping is indicated by the added red arrow in the reproduction of Fig. 53, reproduced below:

FIG.53



(Ex. 1005, 21:20-24).

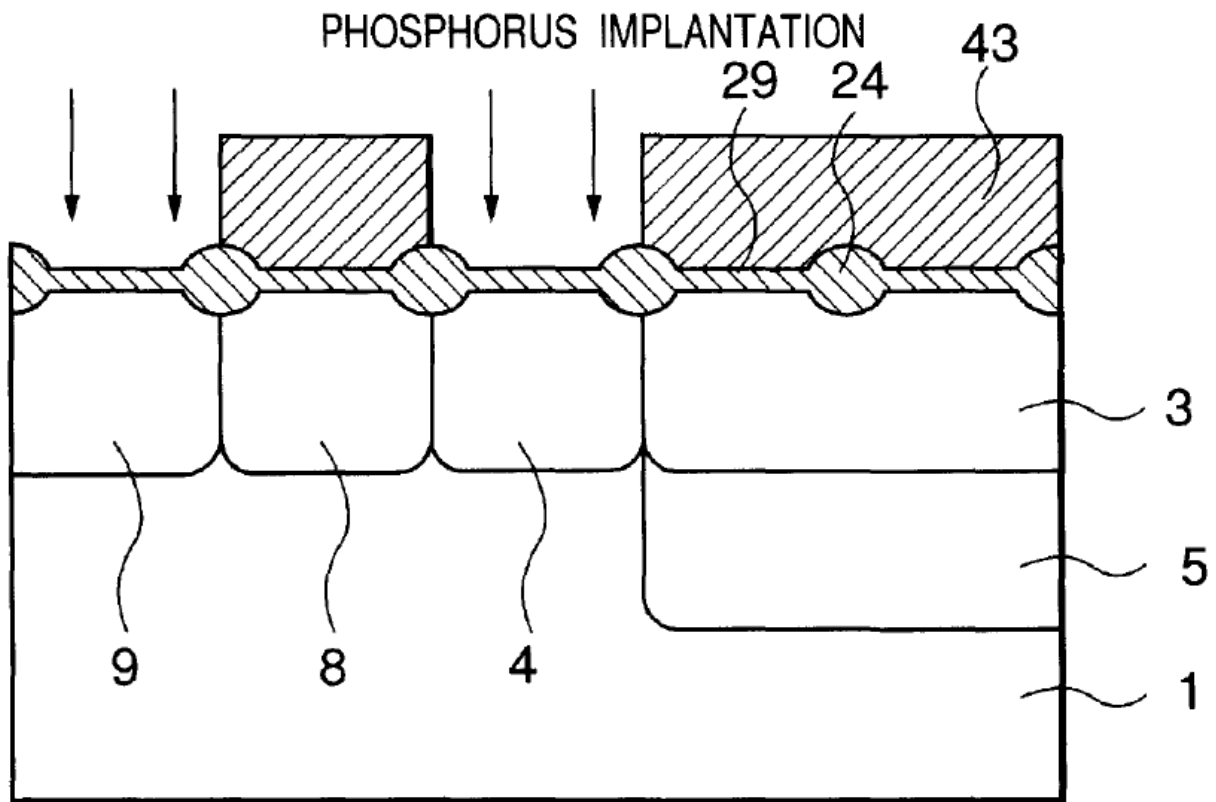
92. The **first active region** is formed by ion implantation of Phosphorous, producing a “retrograde n well 4” extending from the surface of the semiconductor to some depth. Yamashita explains:

“As shown in FIG. 63, a resist 43 is formed. The resist 43 has an opening portion on a formation region for the PMOSFET in the logic circuit region. **Phosphorus, which is a source of n type impurity**

ions, **is implanted** through the opening portion in the formation region by conditions of 300 keV – 2.5 MeV, $1 \times 10^{12} - 1 \times 10^{14} / \text{cm}^2$, and the **retrograde n wells 4, 9 are formed.**”

(Ex. 1005, 23:4-10)(Emphasis added). Figure 63, discussed in the quote above, is reproduced here:

FIG.63

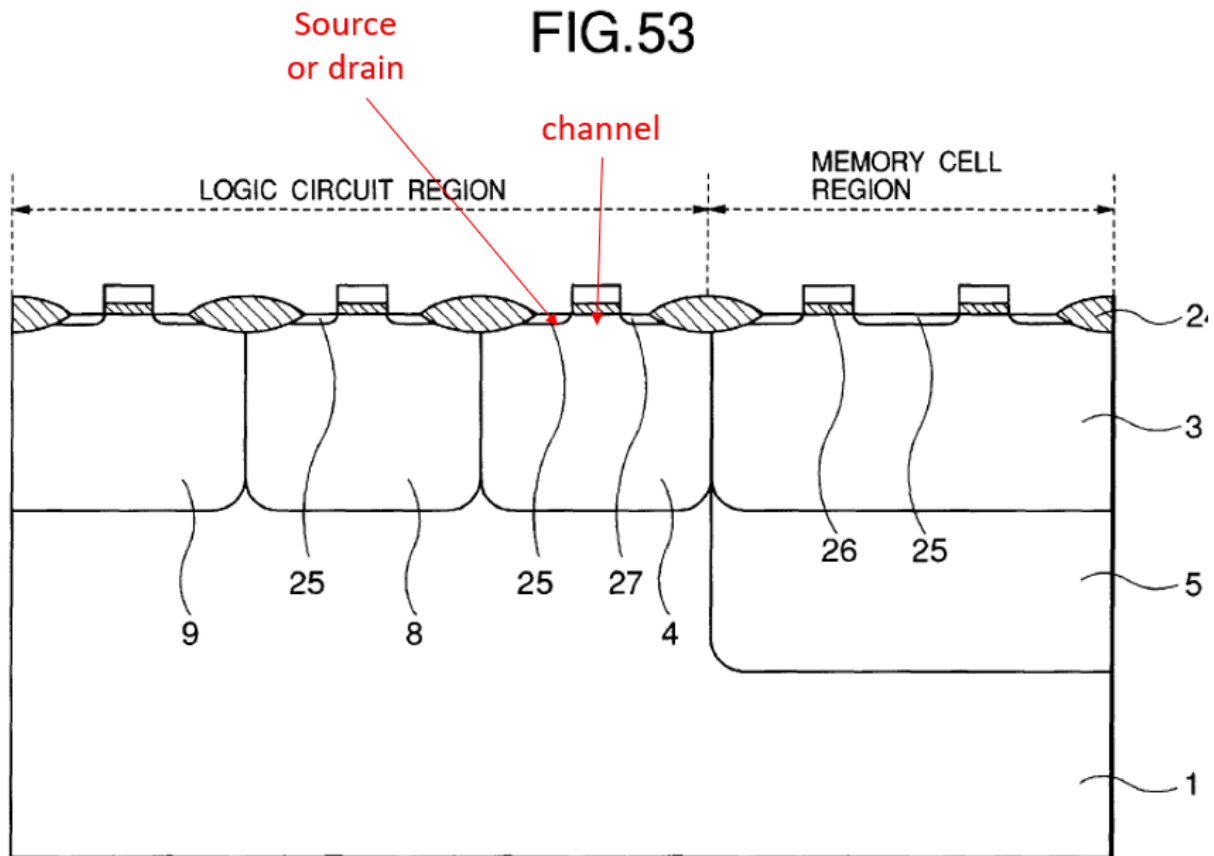


(Ex. 1005, Fig. 63).

93. The first active region is a region **within which transistors can be formed.** Figure 53, reproduced below with added labels and arrows, depicts the

source, drain and channel of a transistor, which meets the claim language under what

I understand to be the Patent Owner's interpretation:



(Ex. 1005, Fig. 53, 6:1-2, 21:55-58). Furthermore, Yamashita teaches that additional transistors can be formed in this same region:

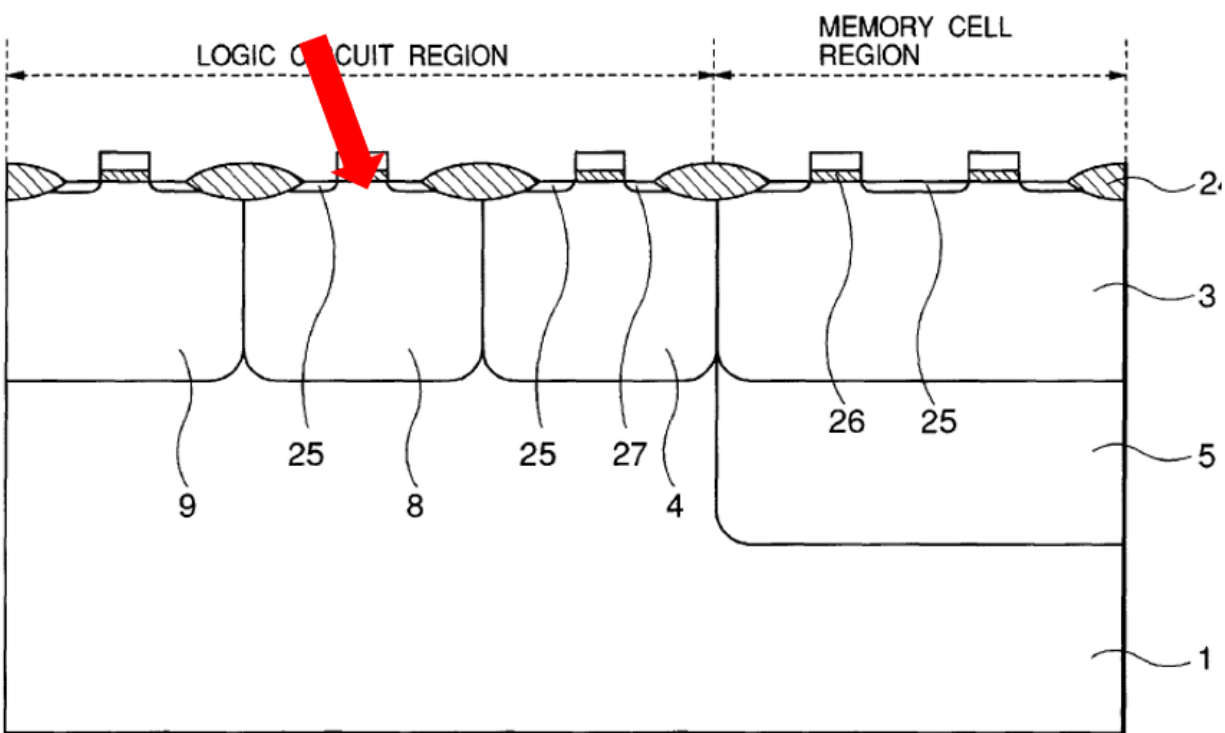
“A plurality of transistors or a single transistor is formed on the retrograde p well 8, the retrograde n well 4 and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region.”

(Ex. 1005, 21:55-58)(Emphasis added).

“[1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;”

94. Yamashita teaches a **second active region separate from the first active region disposed adjacent to the first active region** within which transistors can be formed. The second active region is shown in Fig. 53, reproduced below, with an added red arrow showing the **second active region**:

FIG.53



(Ex. 1005, Fig. 53). The second active region has a retrograde p well 8. (Ex. 1005, 21:20-23, 21:55-58, 22:64-23:3, 23:13-14). In the semiconductor arts, a substrate typically contains active regions, which can in turn contain or be contained in wells.

95. The second active region is **separate[d] from the first active region** by a “separation region”, which is comprised of an isolating field oxide layer 24, as explained above under element [1c]. (Ex. 1005, 22:33-37). The '014 patent also separates active regions by isolation regions. (*e.g.*, Ex. 1001, claim 6).

96. The second active region is also **adjacent to the first active region**, as shown in Fig. 53, above. This adjacent nature of the active regions was also obvious from the disclosure of CMOS logic. This is because in CMOS logic, logic gates (such as AND, OR and XOR) are formed using both n-channel and p-channel devices together in proximity with a common inputs and output, making it customary to place p-well and n-well portions adjacent to one another on an integrated circuit surface.

97. Finally, Fig. 53 depicts a transistor formed in the second active region, and Yamashita teaches that additional **transistors can be formed in the second active region**:

“A plurality of transistors or a single transistor is formed on the retrograde p well 8, the retrograde n well 4 and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region.”

(Ex. 1005, 21:55-58)(Emphasis added). This passage indicates that multiple transistors are formed in each well, which in turn is in an active region.

“[1e] transistors formed in at least one of the first active region or second active region;”

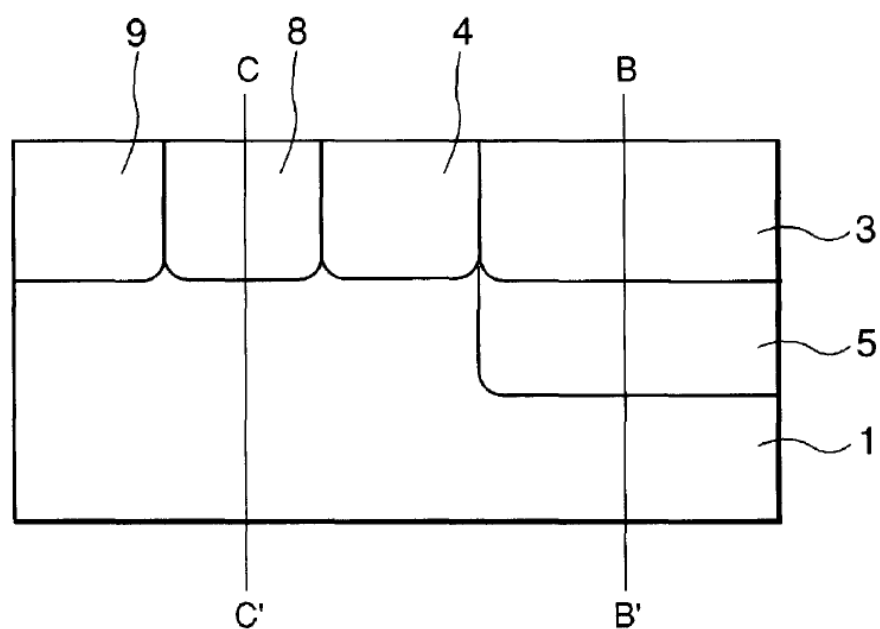
98. As explained above under elements [1c] and [1d], Yamashita teaches that transistors are formed in both the first and second active regions. (Ex. 1005, 21:55-58).

“[1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and”

99. Yamashita teaches that both the first and second active regions each have at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions. Specifically, the first active region contains a retrograde n well 4, and the second active region contains a retrograde p well 8. (Ex. 1005, 21:19-25, 22:7-9). As explained above in ¶38, a “retrograde well” is an area of a semiconductor device that has a dopant profile with a concentration peak (a local maximum dopant concentration) below the surface of the device.

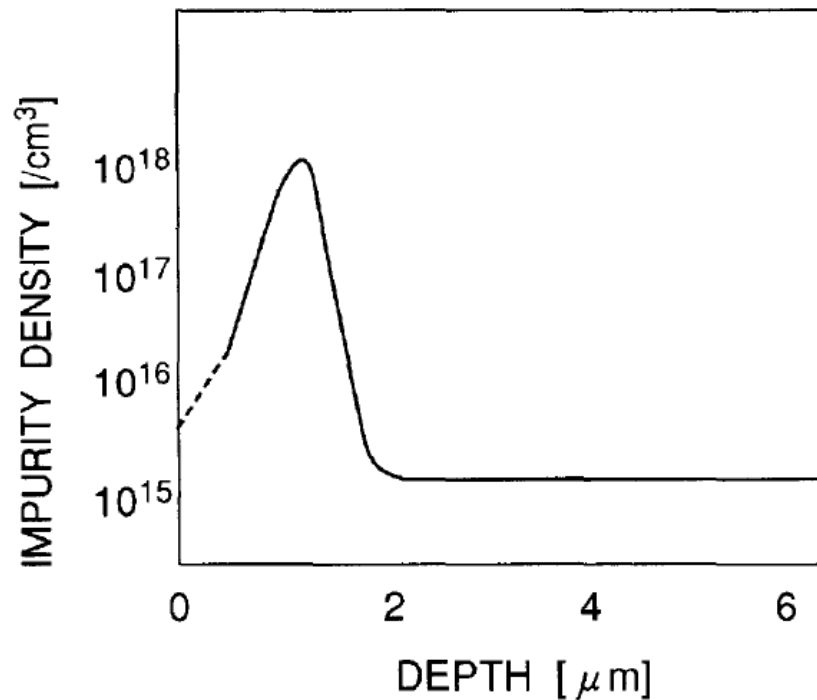
100. With respect to the second active region (which has a retrograde p well 8), Yamashita discloses a cross-section in Fig. 54. The cross-section in Fig. 54 is reproduced here:

FIG.54



(Ex. 1005, 6:3-4, 21:19-26). In Fig. 54, Yamashita shows, running through the second active region, a vertical axis C-C' toward the left-hand side. Along that axis, there is the dopant ("impurity") concentration profile shown in Fig. 55, reproduced here:

FIG.55



(Ex. 1005, 21:35-36, 6:5-6). The horizontal axis of Fig. 55 represents the depth from the top surface of the device, where the top surface is at depth zero on the left-hand side. The vertical axis represents the dopant concentration (called the “impurity density” here). As is visible from the figure, the **dopant concentration is graded**, because it increases from the surface, reaches a peak, and because it then decreases from the peak to a flatter portion at around a depth of two microns.

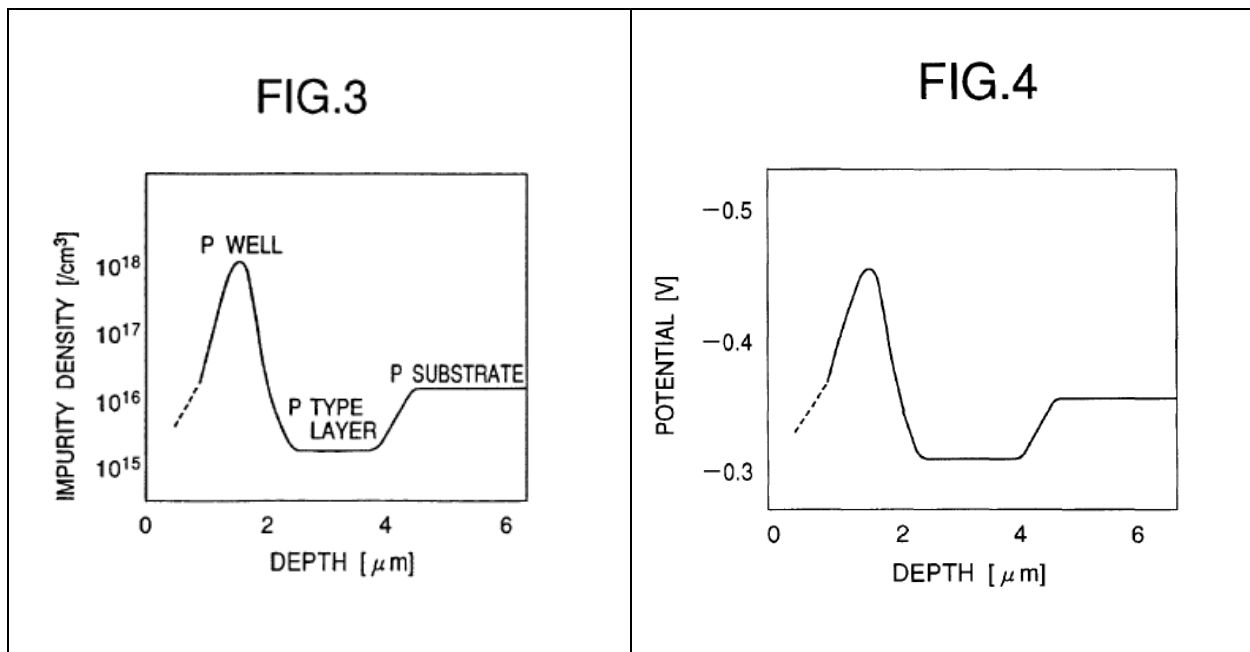
101. With respect to the first active region, although Yamashita does not provide a graph similar to the one shown in Fig. 55, Yamashita does disclose that

the well 4 is a “retrograde n well”. (Ex. 1005, 21:19-25, 21:55-22:1, 22:7-9, 23:4-17). This indicates that the n well 4 has a graded dopant concentration profile with a peak below the surface, similar to the one shown in Fig. 55. Furthermore, the ion implantation step described by Yamashita (Ex. 1005, 23:4-12, Fig. 63) would have produced a phosphorus (dopant) profile in the retrograde n well 4 similar to the dopant profile shown in Fig. 55 for boron. Thus, it would have been obvious based on the description of well 4 as a “retrograde n well”, the corresponding description of the dopant profile of the similarly-labeled retrograde p well 8, and the conditions under which the retrograde n well was created, that the first active region also had a dopant profile with a peak below the surface of the device, and thus a **graded dopant concentration**.

102. The graded dopant profiles would obviously have the effect of aiding carrier movement from the first and second active regions towards an area of the substrate where there are no active regions. I understand that the Patent Owner interprets the relevant claim limitation to require carrier movement to be aided in a downward direction. A dopant concentration that is graded from the top to the bottom of the device will produce an electric field that aids movement of carriers with one type of charge toward the bottom of the device (away from the surface), and carriers with the opposite charge toward the top of the device (toward the surface). *See above*, ¶¶56-68. The carriers that move toward the bottom of the

device (an area of the substrate where there are no active regions) are carriers that are aided from the first and second active regions towards an area of the substrate where there are no active regions under the Patent Owner's interpretation.

103. The obvious effect of Yamashita's graded dopant profiles is exemplified by Figs. 3 and 4 of Yamashita, shown side-by-side below. Fig. 3 shows a dopant profile concentration that has a peak between 1 and 2 microns' depth, similar to the peak shown in the dopant concentration profile of Fig. 55. That peak produces an electric potential function (the derivative of which is an electric field) as shown in Fig. 4 (right side):

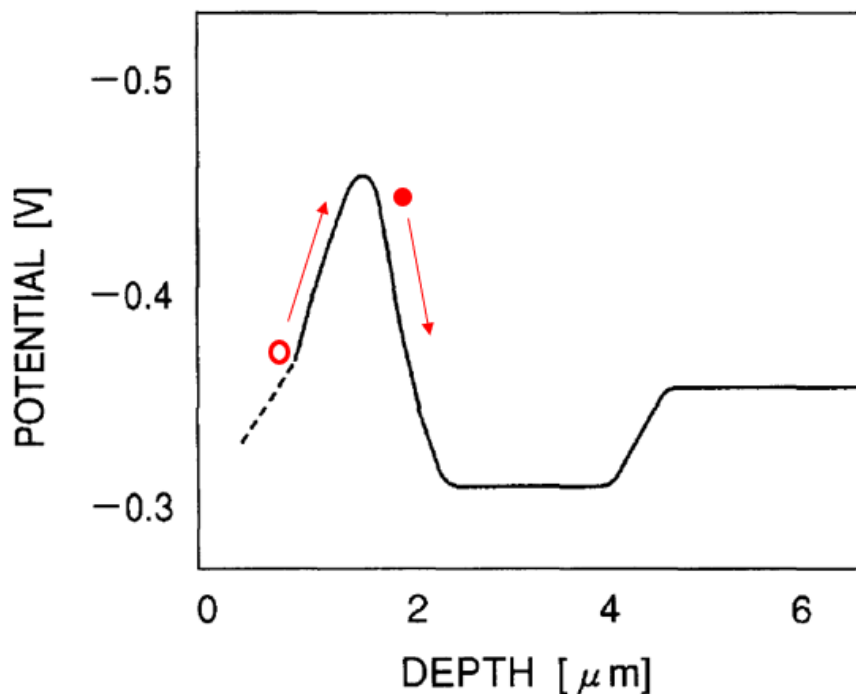


(Ex. 1005, 3:61-64, 7:32-8:5).

104. As shown in a version of Fig. 4 that I have annotated, below, the electric field produced by the retrograde p well causes negative carriers (electrons,

closed circles) to move down the slope to the right of the large negative potential peak, while positive carriers (holes, open circles) will move up the slope to the left of the positive potential peak, and thus both types of carriers are aided in their movement from the first and second active regions towards an area of the substrate where there are no active regions. (Ex. 1005, 7:32-8:5).

FIG.4



(Ex. 1005, Fig. 4).

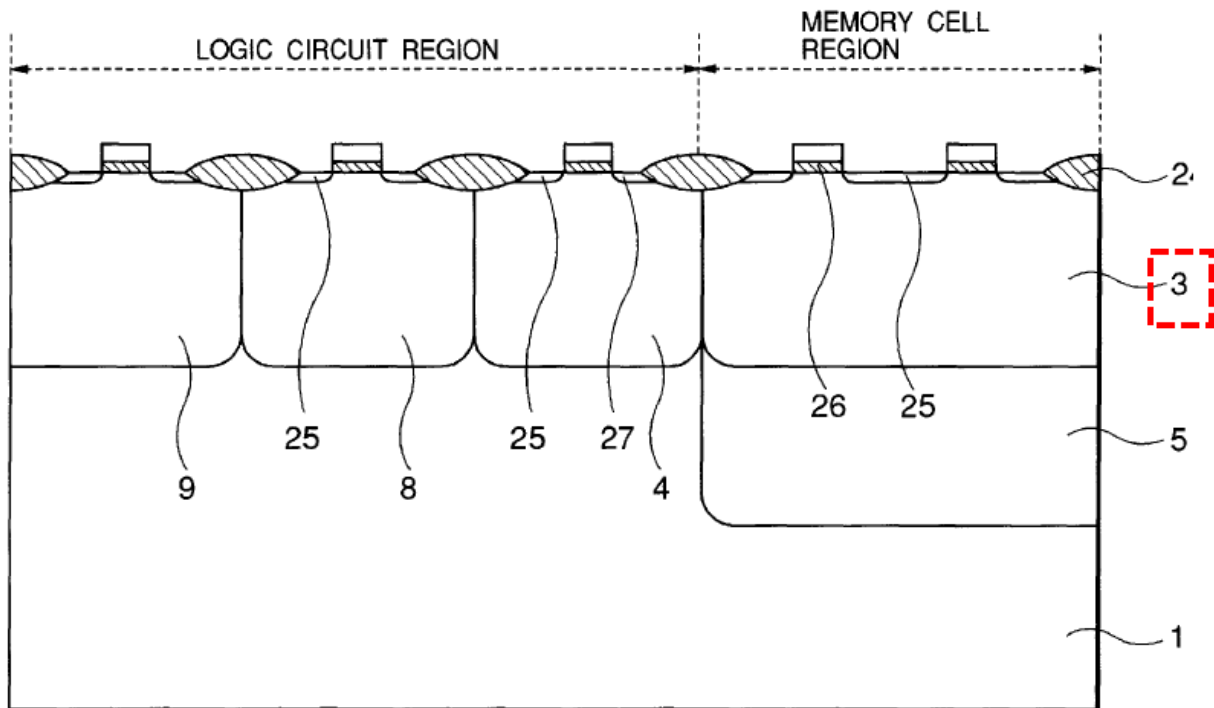
105. It would have been obvious to implement, in the Eighth embodiment of Yamashita, a potential gradient similar to the one in Fig. 4 from the surface to about 2.5 microns in depth using a graded dopant concentration. This was obvious

because of the similarity of the dopant concentration profiles between 0 and 2.5 microns depth in Figs. 3 and 55, and because the potential gradient of Fig. 4 would fulfill the function of the Eighth Embodiment of Yamashita, namely that “soft error based on electrons can be controlled” by aiding minority carriers toward the bottom of the device. (Ex. 1005, 23:17-26, 7:56-63).

“[1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions,”

106. Yamashita further teaches **at least one well region adjacent to the first or second active region**. The well region is “retrograde p well 3”, which is shown in Fig. 53. (Ex. 1005, 21:20-22, 21:51-54). Figure 53 is reproduced below with an added, red-dashed box around the reference numeral 3 on the right-hand side:

FIG.53

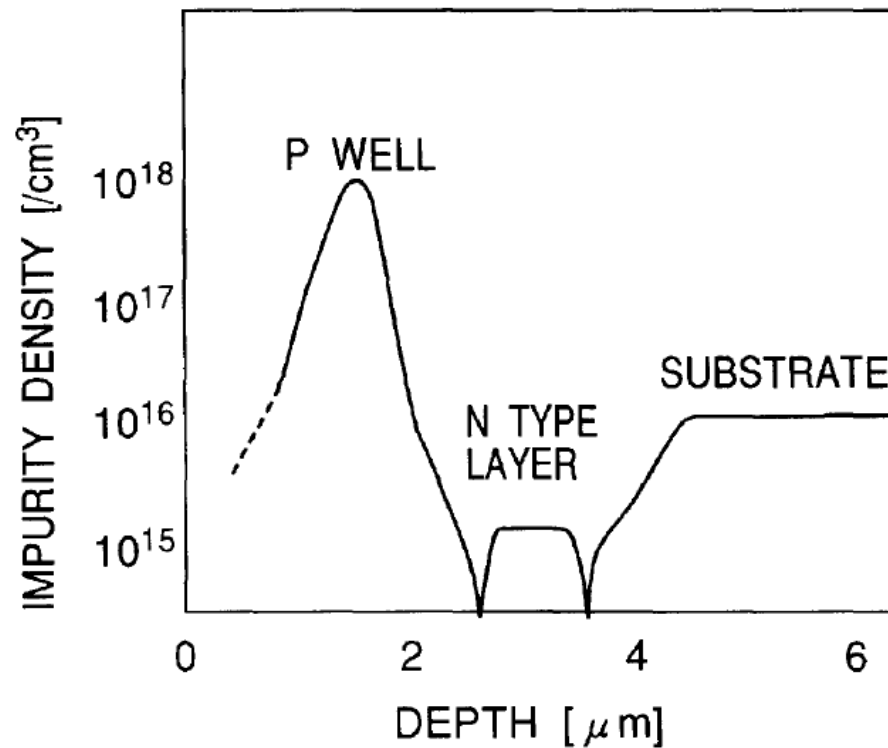


(Ex. 1005, Fig. 53, 21:42-54).

107. The retrograde p-well 3 is a **well region**. The well region is **adjacent to the first or second active region**, as shown in Fig. 53. It was also obvious to situate the well 3 adjacent to the first active region to have CMOS logic circuits adjacent to a memory area, as suggested by Yamashita. (Ex. 1005, Fig. 53, 21:27-32).

108. The retrograde p-well 3 further **contains at least one graded dopant region**. The dopant profile is shown in Fig. 10 of Yamashita (Ex. 1005, 21:36-41), reproduced here:

FIG.10

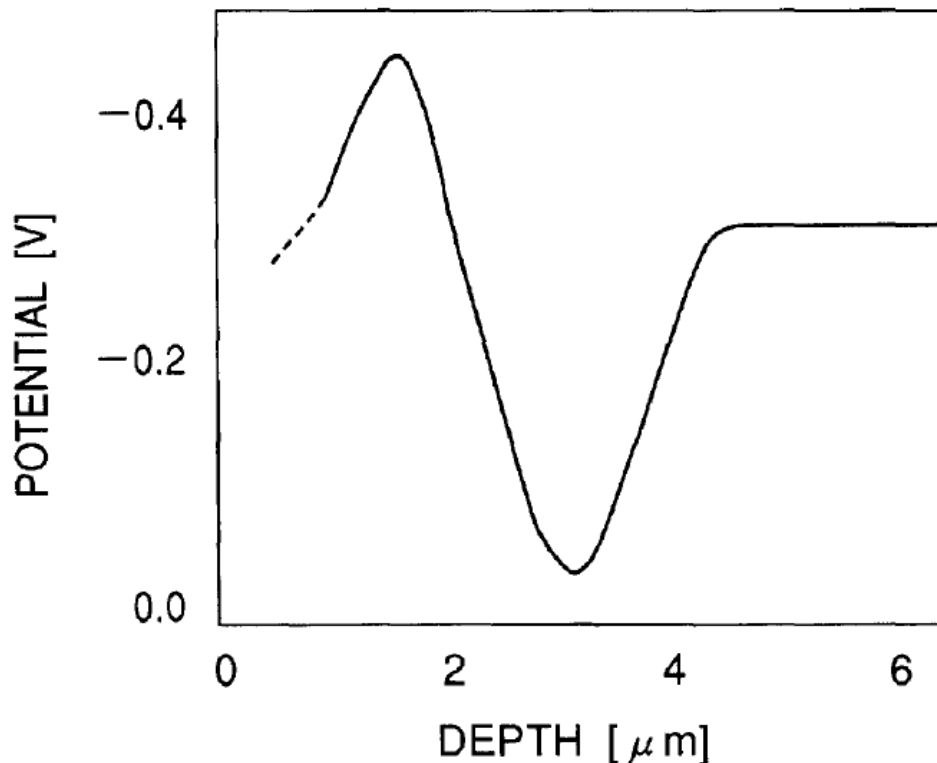


(Ex. 1006, 21:37-41, 22:10-19). Figure 10 shows a dopant concentration (“impurity density”) profile similar to the one discussed above under element [1f]. The region labeled “p well” corresponds to the retrograde p well 3 and the region labeled “n type layer” corresponds to n type layer 5. The Figure shows that the p well has a concentration peak with increasing dopant beginning at the surface and proceeding to a peak, followed by decreasing dopant concentration to a depth somewhat greater than two microns, where the p well contacts the n type layer below it. The well region thus has **at least one graded dopant region**.

109. The graded dopant region is to **aid carrier movement from the surface towards the area of the substrate where there are no active regions.** This is obviously the case for the same reasons discussed above under claim element [1f].

110. Furthermore, Yamashita teaches that the graded dopant concentration profile shown in Fig. 10 produces the potential profile shown in Fig. 11, reproduced here:

FIG.11



(Ex. 1005, Fig. 11, 4:14-15, 9:27-34). As shown in Fig. 11, the electrical potential (in Volts, in the vertical axis) varies in a manner corresponding to the dopant

concentration profile. The variation in potential is an electric field. The electric field causes movement of charged carriers in opposite directions (toward or away from the bottom of the device, depending on the charge of the carrier and the local direction of the field), and thus **aids carrier movement from the surface towards the area of the substrate where there are no active regions.**

111. For example, Yamashita teaches:

“According to the substrate structure of the memory cell region, as shown in FIG. 10, as in the second embodiment, soft error based on the electron can be controlled, because **the potential barrier of electrons**, generated by α -rays or the like in the p type semiconductor substrate 1, with respect to the upper side of the retrograde p well 3, becomes larger by the existence of the n type impurity layer 5, and **electron flow to the source/drain 25 on the retrograde p well 3 is interrupted.**”

(Ex. 1005, 22:10-19)(Emphasis added). The potential barrier interrupting electron flow to the source/drain 25 (at the top of the device) indicates that the potential barrier is **aiding** electron (carrier) **movement from the surface** towards the bottom of the device, which is **towards the area of the substrate where there are no active regions.**

“[1h] wherein at least some of the transistors form digital logic of the semiconductor device.”

112. Yamashita teaches that the **transistors** of the first and second active regions **form digital logic**. Yamashita states:

“A plurality of transistors or a single transistor is formed on the **retrograde p well 8**, the **retrograde n well 4** and the retrograde n well 9 (not shown), and a CMOS is formed on the **logic circuit region**.”

(Ex. 1005, 21:55-58)(Emphasis added). The logic circuit region is shown in Fig. 53, and encompasses both the first active region (discussed above under element [1c]) and the second active region (discussed above under element [1d]).]. (Ex. 1005, 21:55-65, 22:10-18, 22:32-39). CMOS logic is digital logic. As described above in the section entitled “Rationale (Motivation) for the Combination”, it would have been obvious to use Yamashita’s techniques in a logic device like DRAM and associated processing circuitry. In that way, the combination renders obvious that at least some of the transistors form digital logic of the semiconductor device.

CLAIM 2

“2. The system of claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.”

113. Yamashita teaches **the substrate is a p-type substrate**. (Ex. 1005, 22:10-14, 22:33-35).

CLAIM 3

“3. The system of claim 1, wherein the substrate of the at least one

semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.”

114. Yamashita teaches **substrates** that can have **epitaxial silicon**. Specifically, Yamashita teaches that the p type layer 2, as well as the n type layer 5, are “formed by epitaxial growth”. (Ex. 1005, 8:11-16, 8:50-54, 11:62-64, 12:27-28, 15:56-61, 16:53-57, 18:39-42, 21:20-24, 26:31-36). Silicon formed by epitaxial growth is **epitaxial silicon**. Furthermore, these layers are “formed on the p type semiconductor substrate 1”. (Ex. 1005, 8:11-15, 10: 50-54, 11:62-67, 21:20-24, Figs. 60, 53).

115. While Yamashita does not expressly state that the Eighth Embodiment epitaxial silicon is **on top of a nonepitaxial substrate**, this was common practice in the relevant timeframe, as I discuss above in ¶¶26 and 30. In general, epitaxial silicon layers are higher quality for device manufacturing, but slower to grow. Therefore, providing a thicker nonepitaxial substrate for handling and stability, topped by a higher-quality epitaxial substrate, made economic sense in the relevant timeframe.

CLAIM 4

“4. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.”

116. See above, claim 1, limitations [1c]-[1e] (discussing the formation of transistors in the first and second active regions, as well as their dopant types), limitation [1h] (discussing the transistors forming digital logic). The transistors in the first and second active region comprise both **p-channel and n-channel** devices. Specifically, transistors in the first active region comprise p-channel devices, because their channels are formed between p-type sources and drains in the n well 4, while the transistors in the second active region comprise n-channel devices, because their channels are formed between n-type sources and drains in the p well 8. (Ex. 1005, 21:42-65).

CLAIM 5

“5. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

117. See above, claim 4 (discussing p-channel and n-channel devices), claim 1, elements [1c] and [1d] (discussing the n-wells (e.g., n well 4) and p-wells (e.g., p well 8) respectively), and claim limitation [1f] (discussing the graded dopant regions in the retrograde n well 4 and the retrograde p well 8).

CLAIM 6

“6. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.”

118. Yamashita teaches that the **first active region and second active region are each separated by at least one isolation region**, specifically field oxide region 24. As discussed above under claim 1, element [1c], the active regions under gate oxide 29 in Fig. 57 are separated by “separation regions” in the form of field oxide 24. (Ex. 1005, 22:32-39, 22:57-23:17). These separation regions are visible between active regions, including after transistor construction, in Figs. 53 and 57-63. Field oxide regions are isolation regions.

CLAIM 7

“7. The system of claim 1, wherein the graded dopant is fabricated with an ion implantation process.”

119. Yamashita teaches that the **graded dopant is fabricated with an ion implantation process** in each of retrograde p wells 3 and 8, as well as retrograde n well 4. (Ex. 1005, 22:57-23:17).

CLAIM 8

“8. The system of claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.”

120. Yamashita teaches this claim. See above, claim 1, element [1c], which already requires that the *first* active region be “disposed adjacent to the surface”. The *second* active region, in turn, is disposed horizontally adjacent to the first active region (see above, claim 1, element [1d]), and is also **adjacent the first**

(top) **surface of the substrate**. See above, claim 1, element [1d]. To the extent that the word “formed” (as opposed to the word “disposed” in claim 1) requires a physical process, the first and second active regions are also “formed” where they are ultimately “disposed”. (Ex. 1005, 21:55-22:6, Fig. 53).

CLAIM 9

“9. The system of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.”

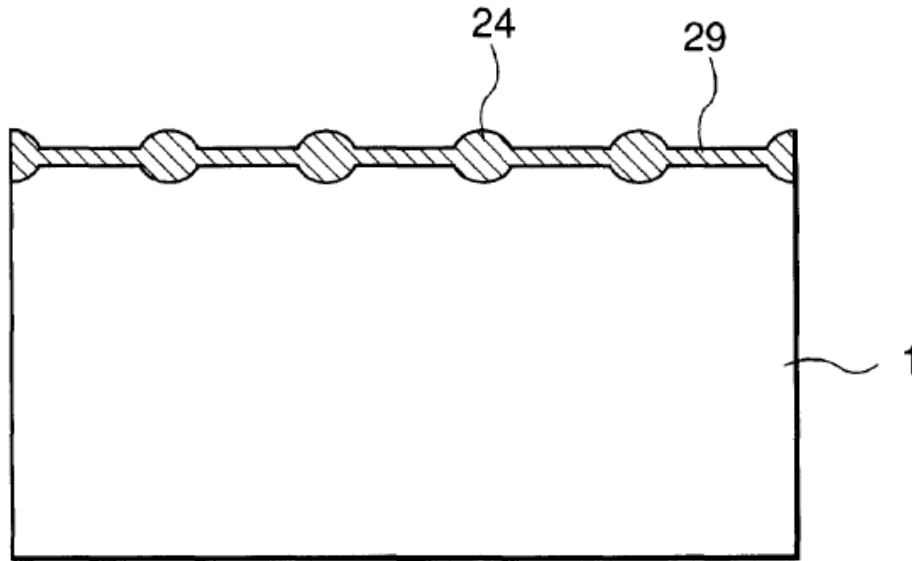
121. Yamashita teaches this claim. See above, claim 1, limitations [1c] and [1d] (discussing dopants of the first and second active regions) as well as limitation [1f], discussing the graded dopants.

CLAIM 10

“10. The system of claim 1, wherein dopants of the graded dopant concentration in the first active region of the at least one semiconductor device are both p-type and n-type.”

122. Yamashita teaches claim 10. As discussed above under claim 1, element [1b], Yamashita begins with a “p type semiconductor substrate 1 containing boron of a concentration on the order of $1 \times 10^{16} / \text{cm}^3$ ”. (Ex. 1005, 22:33-38, 6:1-2, 21:20-24, 22:19-24, 7:19-21). The substrate 1, at an earlier stage in the fabrication process, is shown in Fig. 57, reproduced here:

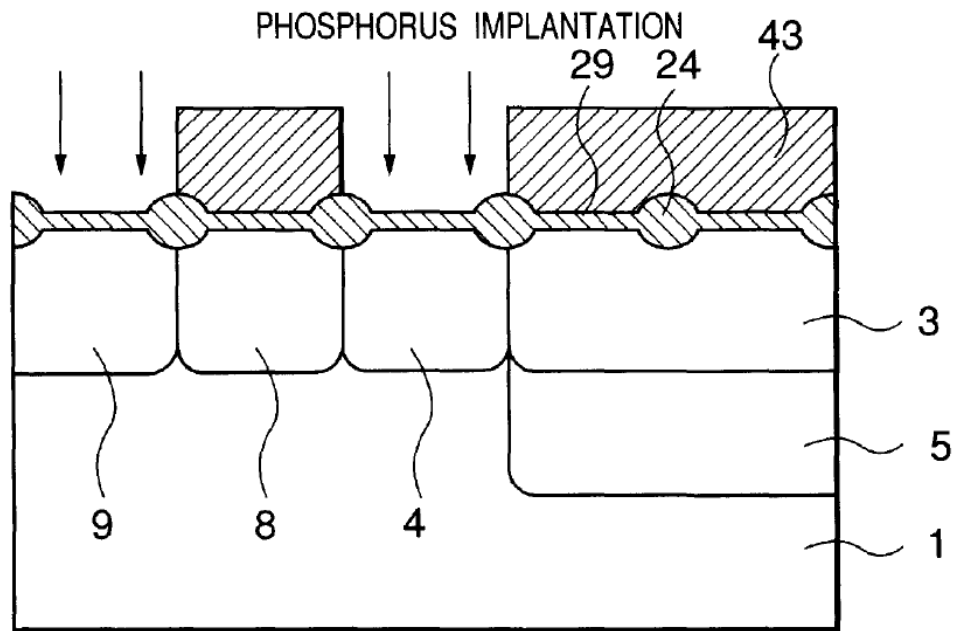
FIG.57



(Ex. 1005, Fig. 57, 22:33-38).

123. As discussed above under claim 1, element [1c], the **first active region** has a retrograde n well 4, which has a graded dopant concentration. The retrograde n well 4 is formed by the ion implantation of phosphorus ions, which are **n-type dopants**, into the already p-type substrate. (Ex. 1005, 23:4-12). This implantation is shown in Fig. 63, reproduced again here:

FIG.63



(Ex. 1005, Fig. 63, 23:4-12).

124. Because the n well 4 (which is in the first active region) is formed by the implantation of n-type dopants into substrate 1, which has p-type dopants, and because the implantation of n-type dopants does not remove p-type dopants, Yamashita teaches claim 10.

CLAIM 11

“11. The system of claim 1, wherein dopants of the graded dopant concentration in the second active region of the at least one semiconductor device are both p-type and n-type.”

125. The combination renders claim 11 obvious. As discussed above under claim 1, elements [1d] and [1f], the second active region of Yamashita

contains a retrograde p well 8, which has a **graded dopant region** containing **p-type dopants** (namely, boron). (Ex. 1005, 22:64-23:3).

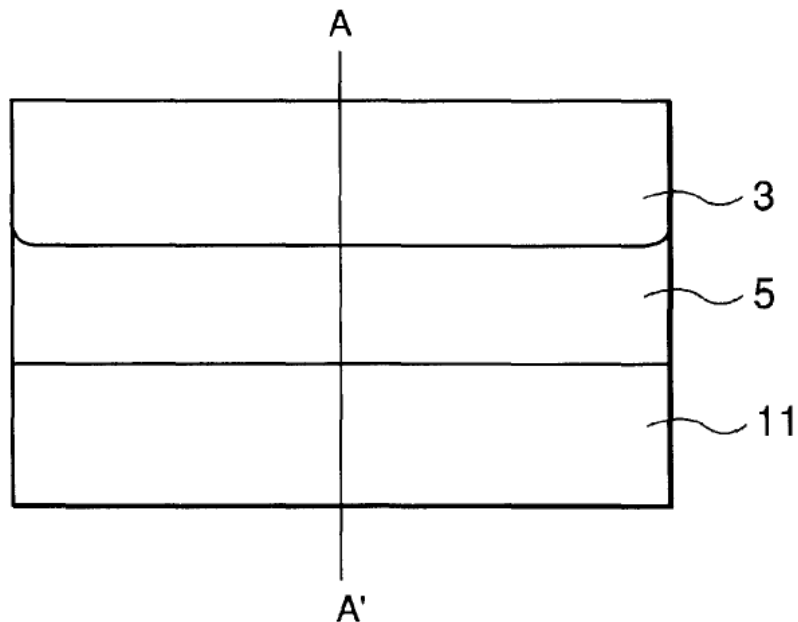
126. With respect to the required n-type dopants, it would have been obvious to use an n-type substrate, in which the retrograde p well 8 was implanted, thus providing both p-type and n-type dopants.

127. Specifically, Yamashita discloses, in the context of its Seventh Embodiment, an “n type semiconductor substrate 11”. (Ex. 1005, 19:57-20:7, 20:31-39, Fig. 48). The n type semiconductor 11 then has a p type impurity layer 2 and a retrograde p well 3. Yamashita states:

A substrate of the semiconductor device, as shown in FIG. 48, comprises the n type semiconductor substrate 11 containing phosphorus of concentration on the order of $1 \times 10^{16} / \text{cm}^3$, the n type impurity layer 5 containing phosphorus of concentration on the order of $1 \times 10^{15} / \text{cm}^3$ and the retrograde p well 3 containing boron of concentration on the order of $1 \times 10^{18} / \text{cm}^3$.”

(Ex. 1005, 20:1-7). The layers are shown in Fig. 48, reproduced here:

FIG.48



(Ex. 1005, Fig. 48).

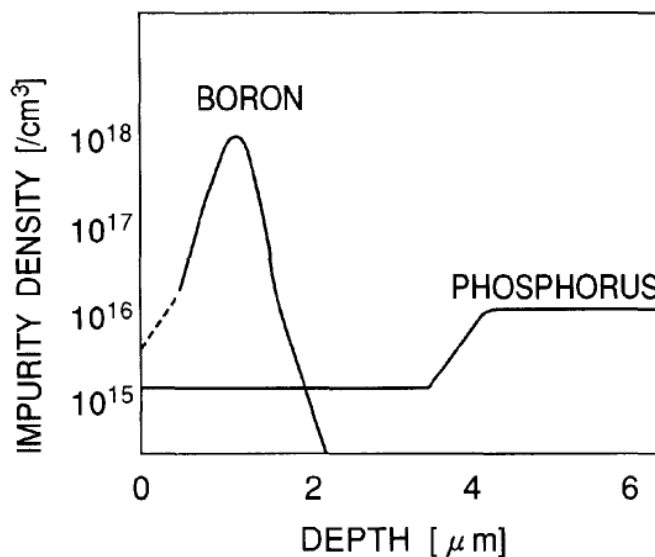
128. It would have been obvious to use an n-type substrate, as suggested by the Seventh Embodiment of Yamashita, in the Eighth Embodiment of Yamashita. A POSITA would have recognized that the Eighth Embodiment could have been used with a p type or an n type substrate without unpredictable results and with a reasonable expectation of success, as long as the appropriately doped well is implanted for each type of device. In the Seventh Embodiment, for example, a retrograde p well 3 is implanted near the surface, which is similar to the retrograde p well implanted for the second active region. (Ex. 1005, 20:1-7, 20:35-39, *compare* Figs. 50 and 54). In addition, Yamashita teaches that the structure of the Seventh Embodiment is advantageous, specifically because:

“As in the sixth embodiment, the semiconductor structure can improve pressure resistance, because the field between the retrograde p well 3 and the n type semiconductor substrate 11 is alleviated. Further, since the n type semiconductor substrate 11 has a high concentration and the retrograde p well 3 has a low impurity concentration surface for forming the transistor, degradation of transistor threshold voltage or the like can be reduced.”

(Ex. 1005, 20:31-39). A POSITA would thus have expected advantages in using the n type semiconductor substrate and structure of the Seventh Embodiment together with the Eighth Embodiment of Yamashita.

129. With the n type semiconductor substrate of the Seventh Embodiment, the substrate has a dopant concentration, as required by claim 1, specifically phosphorus of concentration on the order of $1 \times 10^{16} / \text{cm}^3$. (Ex. 1005, 18:59-65). The dopant concentration profile along the line A – A’ in Fig. 48 is shown in Fig. 50, reproduced here:

FIG.50



(Ex. 1005, Fig. 50, 5:60-62, 19:65-67). The profile of Fig. 50 is similar to the profile in the second active region (shown in Fig. 54), as discussed above under claim 1, element [1f], except that in Fig. 50, the n type dopant (Phosphorous) is present from the n type substrate.

130. As can be seen from the Figure, the p type dopant (boron) and n type dopant (Phosphorous) overlap in the region of graded dopant profile. Thus, both dopant types obviously would contribute to the dopant level, meaning that **dopants of the graded dopant concentration in the second active region are both p-type and n-type.**

CLAIM 12

“12. The system of claim 1, wherein dopants of the graded dopant region in the well region of the at least one semiconductor device

are both p-type and n-type.”

131. Yamashita teaches claim 12. As discussed above under claim 1, element [1g], the well region with a graded dopant concentration is the p well 3. The p well 3 is formed by boron implantation, and thus has **p-type dopants**. (Ex. 1005, 22:57-63, Fig. 53). The p well 3, however, is formed after the ion implantation and diffusion of phosphorous, which is an n-type dopant, forming layer 5. (Ex. 1005, 22:39-63, Figs. 58-61). Because the p well 3 is formed by the implantation of p-type dopants into n type layer 5, which has n-type dopants, and because the implantation of p-type dopants does not remove n-type dopants, Yamashita teaches claim 12.

CLAIM 13

“13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.”

132. Yamashita teaches that **the transistors which can be formed in the first and second active regions are CMOS digital logic transistors**. The first and second active regions, and their transistors, are discussed above under claim 1, elements [1c]-[1e]. Yamashita states that the transistors can form CMOS digital logic. Yamashita states:

“A plurality of transistors or a single transistor is formed on the retrograde p well 8, the retrograde n well 4 and the retrograde n well 9 (not shown), and a **CMOS** is formed on the logic circuit region.”

(Ex. 1005, 21:52-58)(Emphasis added). A POSITA would have understood (*see, e.g., ¶96, above*) from this description that pMOS transistors are formed in the n well 4, and nMOS transistors are formed in the p well 8, and that these transistors together form CMOS digital logic, and are thus **CMOS digital logic transistors**. The MOSFET transistors in Yamashita have sources, drains, channels, and gates. (Ex. 1005, 21:55-65, 22:32-39).

CLAIM 14

“14. The system of claim 1, wherein the at least one semiconductor device is a dynamic random access memory (DRAM).”

133. Yamashita renders claim 14 obvious. Specifically, as explained above under the Rationale (Motivation) Supporting Obviousness, Yamashita already renders obvious using its semiconductor devices in **a dynamic random access memory (DRAM)**. (Ex. 1005, Fig. 53, 21:20-34).

CLAIM 15

“15. The system of claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.”

134. Yamashita renders claim 15 obvious. *See* above, claim 13 (addressing CMOS) and claim 3 (addressing the nonepitaxial substrate).

CLAIM 17

“17. The system of claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.”

135. Yamashita renders claim 17 obvious. Yamashita renders obvious DRAM, which has individual cells that store individual bits of information as charge in a **capacitor**. (Ex. 1005, 1:12-15). Yamashita also expressly teaches forming capacitors. (Ex. 1005, 23:10-12). Yamashita likewise teaches **digital logic**, as discussed above under claim 1, element [1h].

CLAIM 20

“20. The system of claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.”

136. See above, claim 1, elements [1c] and [1d]. The first and second active regions laterally next to one another. (Ex. 1005, Fig. 53).

CLAIM 21

137. Claim 21 is similar to claim 1. A comparison (redline) of differences between claims 1 and 21 is provided in Ex. 1009 (p. 1).

“21[a]. An electronic system, comprising: at least one semiconductor device, the at least one semiconductor device including:”

138. See discussion above, claim 1, element 1[a], which has the same language. (Ex. 1009, p. 1).

“[21b] a substrate of a first doping type at a first doping level having a surface;”

139. See discussion above, claim 1, element [1b], which has the same language. (Ex. 1009, p. 1).

“[21c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;”

140. See discussion above, claim 1, element [1c], which has similar language (Ex. 1009, p. 1). The present element [21c] specifies that the “surface” is the “surface of the substrate”, and that transistors can be formed “in the surface” of the first active region. These differences in language do not affect the mapping of the prior art onto the claim, because the transistors in Yamashita’s first and second active regions are formed at the surface of the substrate, which is also the surface of the active region. See above, claim 1, element [1e].

“[21d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;”

141. See discussion above, claim 1, element [1d], which has similar language (Ex. 1009, p. 1). The present element [21d] specifies that transistors can be formed “in the surface” of the second active region. This difference in language does not affect the mapping of the prior art onto the claim, because the transistors in

Yamashita's first and second active regions are formed at the surface of the substrate, which is also the surface of the active region. *See above, claim 1, element [1e].*

“[21e] transistors formed in at least one of the first active region or second active region;”

142. *See discussion above, claim 1, element [1e], which has the same language. (Ex. 1009, p. 1).*

“[21f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions;”

143. *See discussion above, claim 1, element [1f], which has similar language. (Ex. 1009, p. 1). The present claim element [21f] specifies that carrier movement is aided “from the surface” instead of “from the first and second active regions”, but this does not affect the mapping of the prior art to the claim, because the first and second active regions are aligned with the surface [of the substrate]. *See above, claim 1, element [1c]-[1d].**

“[21g] and at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and”

144. *See discussion above, claim 1, element [1g], which has similar language. (Ex. 1009, p. 1). The present claim element [21g] changes the word*

“towards” to “to”, but this does not affect the mapping of the prior art to the claim.

See above, claim 1, element [1g]. (Ex. 1006, p. 100)(Ex. 1017, pp. 12-13, 22-23).

“[21h] wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.”

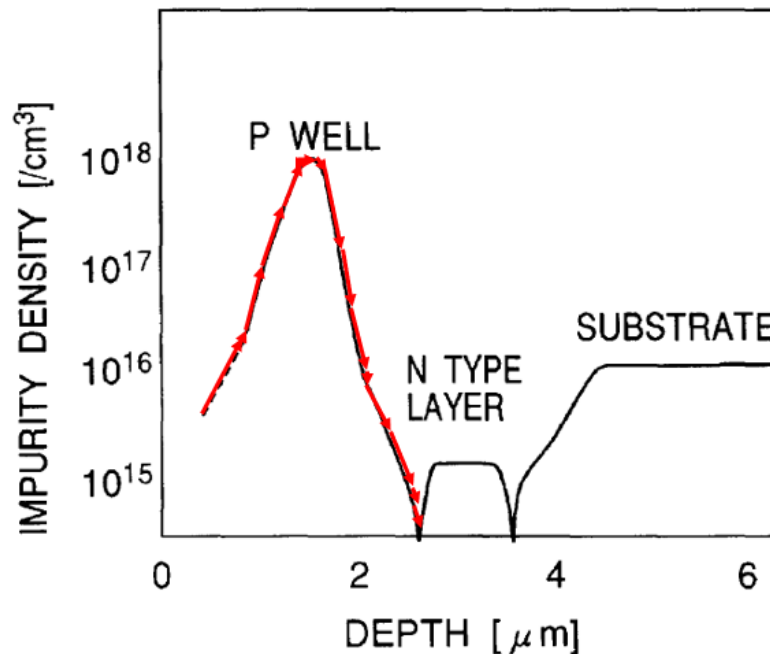
145. It was obvious from Yamashita’s disclosure of the graded dopant concentration in the p well 3 (see above, claim 1, element [1g]) that the concentration profile was linear, **quasilinear, error function, complementary error function, or any combination thereof.**

146. First, the p well 3 was formed by ion implantation, which was obviously followed by annealing and the consequent diffusion (see above, ¶¶53,36). Such would obviously have resulted in the claimed mathematical profile. Ion implantation yields a dopant concentration profile that can be modeled using four moment gaussian profiles. (Ex. 1012, p. 108). For example, a typical ion implantation profile is shown above in Fig. 5 from Sze (Ex. 1031, p. 005), as discussed above in ¶54. Subsequent annealing and other thermal steps would obviously have produced diffusion of the implanted dopants and result in a dopant profile that is well-modeled with complementary error functions, as described in Grove Fig. 3.9 (Ex. 1030, p. 003), as discussed above in ¶52. The present claim element does not specify the value of constants used, and allows for use “in any combination”, thus accounting for any departures from the ideal distributions. For

example, if a complementary error function yielded values that were slightly too high, it could be multiplied by a constant, or have another error function, or linear function, subtracted from it. This process can be continued with an arbitrary number of functions (*e.g.*, quasi-linear or piece-wise linear) until an acceptable match occurs, and still fall within the scope of claim 21.

147. Furthermore, the clause of the claim that permits “any combination thereof” would cover the dopant profiles of Yamashita. Choosing a sequential combination of piece-wise linear functions having tangents to the dopant profiles of Yamashita would allow for a nearly exact reproduction of those profiles. This is shown, for example, in the reproduction of Fig. 10 below, which has red arrows added to show a series of linear functions that, when combined, match the profile of Fig. 10. The match between the actual dopant profile and the one formed from tangent lines can be improved to an arbitrary degree, simply by shortening the tangent lines (in the figure, by using a greater number of shorter arrows):

FIG.10



(Ex. 1005, Fig. 10). Thus, it would have been obvious from the combination that the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

CLAIM 22

“22. The system of claim 21, wherein the substrate of the at least one semiconductor device is an n-type substrate.”

148. See above, claim 11, discussing that it would have been obvious to use an n type substrate with the Eighth Embodiment of Yamashita.

CLAIM 23

“23. The system of claim 21, wherein the substrate of the at least

one semiconductor device is a p-type substrate.”

149. See above, claim 2.

CLAIM 24

“24. The system of claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.”

150. See above, claim 3.

CLAIM 25

“25. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.”

151. See above, claim 4.

CLAIM 26

“26. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

152. See above, claim 5.

CLAIM 27

“27. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.”

153. See above, claim 6.

CLAIM 28

“28. The system of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.”

154. See above, claim 9.

CLAIM 29

“29. The system of claim 21, wherein dopants of the graded dopant concentration in the first active region of the at least one semiconductor device are both p-type and n-type.”

155. See above, claim 10.

CLAIM 30

“30. The system of claim 21, wherein dopants of the graded dopant concentration in the second active region of the at least one semiconductor device are both p-type and n-type.”

156. See above, claim 11.

Ground 2. Claims 1-30 are obvious over Silverbrook in view of Yamashita.

157. Claims 1-30 were obvious under 35 U.S.C. §103(a) over U.S. Pat. No. 6,614,560 (“**Silverbrook**”)(Ex. 1004) in view of Yamashita. Yamashita was discussed above under Ground 1.

A. Overview of the Combination

158. As discussed above under Ground 1, Yamashita teaches semiconductor devices for, e.g., DRAM in integrated circuits. (Ex. 1005, 1:7-15).

Yamashita teaches on its own almost all elements of the claims. To the extent Yamashita does not itself render obvious an “electronic system” comprising a semiconductor device, Silverbrook teaches an electronic system using an integrated circuit (called an “Image Capture and Processing Chip” or “ICP”) having DRAM, a CPU, an image sensor, in which it is appropriate to use Yamashita’s devices. (Ex. 1004, 6:42-55, Fig. 15). This Ground posits that it would have been obvious to use Yamashita in an electronic system having chip like Silverbrook’s ICP. This Ground also posits obviousness for a variety of minor reasons that are apparent from Yamashita alone, as explained in detail in the claim mapping section where appropriate.

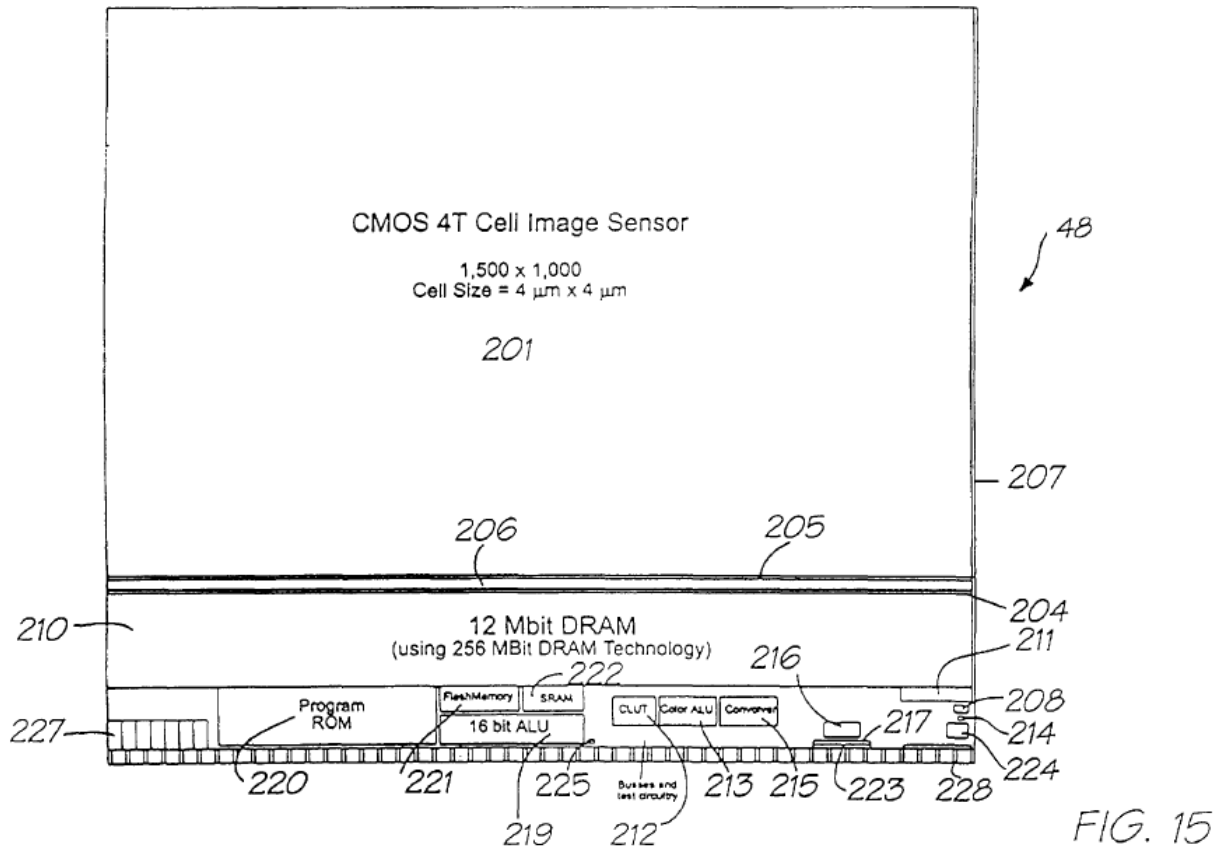
B. Rationale (Motivation) Supporting Obviousness

159. It would have been obvious to use Yamashita’s devices in an electronic device and integrated circuit like Silverbrook’s ICP.

160. As discussed above under Ground 1, Yamashita teaches semiconductor structures useful for memory (and in particular, DRAM) having both a logic circuit region and a memory cell region, as shown with respect to the Eighth Embodiment in Fig. 53. (Ex. 1005, Fig. 53, 21:20-34).

161. Silverbrook teaches a camera system (an electronic device) having an Image Capture and Processing Chip (ICP) that employs DRAM and logic

circuitry. (Ex. 1004, Abstract, 6:42-10:23). The layout of the ICP is shown in Silverbrook's Fig. 15, reproduced here:



(Ex. 1004, 6:42-10:23). As seen at the bottom of Fig. 15, the ICP has DRAM and a logic circuit region for executing logical calculations (*e.g.*, the 16 bit ALU 219, the Color ALU 213, and the Convolver 215). (Ex. 1004, 6:46-48, 7:1-27, 10:9-50).

162. Silverbrook does not teach the low-level semiconductor structure of devices that form the DRAM and logic devices, but does state that they “can be vendor-supplied cores” (7:28-30). A POSITA would have understood Silverbrook

to be teaching that the exact semiconductor techniques used for the DRAM and logic circuit can be obtained from other prior art.

163. A POSITA further would have found it obvious to use the techniques of Yamashita in Silverbrook. Yamashita teaches that its techniques can be used to achieve the advantages of:

“provid[ing] a semiconductor device having a substrate impurity structure that has both soft error resistance and latch up resistance and that prevents faulty circuit operation when the semiconductor device is formed with a fine structure.”

(Ex. 1005, 3:15-18 *see also* 23:17-25). A POSITA thus would have found the combination obvious based on the advantages of Yamashita.

164. A POSITA further would have found the combination obvious because Silverbrook represents a known type of integrated circuit that required circuitry for DRAM and logic circuits, and would have been ready for improvement using the known techniques in a predictable manner.

C. *Graham* Factors

165. The ***Graham*** factors are discussed above under Ground 1.

D. Reasonable Expectation of Success

166. A POSITA in the relevant timeframe would have had a reasonable expectation of success in using the prior art in the manner discussed in this Ground. As I have explained, the art was relatively predictable in the relevant timeframe

(September 2004), with commercially-available sophisticated circuit design, process modeling and physics-based transistor modeling software tools available. A POSITA would have been able to make any necessary modifications to implement the Ground, and in particular would have been able to use Yamashita's techniques in Silverbrook, and to adjust doping gradients, electric fields created by dopant gradients and carrier movement to effect the purposes of Yamashita.

E. Analogous Art

167. Yamashita is analogous art as described under Ground 1. Silverbrook is analogous art because it is directed to the same field as the '014 patent (semiconductor devices). (Ex. 1001, claim 1, Abstract, 1:39-46)(Ex. 1004, Title, 1:9-11, 2:10-16). Furthermore, the teachings of Silverbrook would have been reasonably pertinent to the problems facing the named inventors, including the production of integrated circuits including CMOS image sensors and memory. (Ex. 1001, 3:48-4:1)(Ex. 1004, Title, Fig. 15, 6:41-8:17, 11:14-30).

F. Claim Mapping

168. The claim mapping for this ground is the same as the claim mapping for Ground 1, except that, in the present Ground, Silverbrook's camera system is the "electronic system" recited in the preambles of claims 1 and 21. (Ex. 1004, Abstract, 1:10-12, Fig. 1, 3:32-45). The electronic system contains a semiconductor device,

in the form of Silverbrook's ICP. (Ex. 1004, 6:42-44). It would have been obvious to use Yamashita's techniques in Silverbrook's ICP and camera, as described above.

169. Furthermore, the combination alters the mapping for claims 14-19, as shown below.

CLAIM 14

“14. The system of claim 1, wherein the at least one semiconductor device is a dynamic random access memory (DRAM).”

170. The combination renders claim 14 obvious. Specifically, Silverbrook teaches that its chip has DRAM, and is thus a dynamic random access memory (DRAM). (Ex. 1004, 11:13-30, 11:47-49, Fig. 15).

CLAIM 15

“15. The system of claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.”

171. The combination renders claim 15 obvious. See above, claim 13 (addressing CMOS) and claim 3 (addressing the nonepitaxial substrate).

CLAIM 16

“16. The system of claim 1, wherein the at least one semiconductor device is a flash memory.”

172. The combination renders claim 16 obvious. Specifically, Silverbrook teaches that its chip has flash memory, and is thus a flash memory. (Ex. 1004, 11:55-57, 11:66-12:1, Fig. 15).

CLAIM 17

“17. The system of claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.”

173. The combination renders claim 17 obvious. Yamashita and Silverbrook teach DRAM, which has individual cells that store individual bits of information as charge in a capacitor. (Ex. 1004, 11:13-30, 11:47-49)(Ex. 1005, 1:12-15). Yamashita also expressly teaches forming capacitors. (Ex. 1005, 23:10-12). Yamashita and Silverbrook likewise teach digital logic, as discussed above under claim 1, element [1h].

CLAIM 18

“18. The system of claim 1, wherein the at least one semiconductor device is a central processing unit.”

174. The combination renders claim 15 obvious. Specifically, Silverbrook teaches that its chip has a central processing unit, and is thus a central processing unit. (Ex. 1004, 11:54-55, 11:65-67, Fig. 15).

CLAIM 19

“19. The system of claim 1, wherein the at least one semiconductor device is an image sensor.”

175. The combination renders claim 19 obvious. Specifically, Silverbrook teaches that its chip has an image processor, and thus is an image sensor. (Ex. 1004, Title, 6:39-67, 7:6, 7:28-30, Fig. 15).

Ground 3. Claims 1-30 were obvious over Silverbrook, Yamashita, and Nishi

176. In my opinion, claims 1-30 were obvious over Silverbrook and Yamashita (Grounds 1 and 2) in further view of the Nishi, et al. (eds.) *Handbook of Semiconductor Manufacturing*, Marcel Dekker, Inc., New York (2000)(Ex. 1012).

177. Nishi is a well-known textbook in the field of semiconductor fabrication. It is the kind of publication that experts in this field would reasonably rely on, including for its publication date. The publication date of Nishi is provided by its copyright date, which is the year 2000. (Ex. 1012, p. 004). I myself was aware of Nishi at approximately the time it was published. Nishi was repeatedly cited in the years between 2000 and 2004, for example, in Ex. 1024, p. 001, Ex. 1025, ¶0006, Ex. 1026, ¶0112, Ex. 1027, ¶0004.

A. Overview of the Ground

178. In my opinion, it would have been obvious to provide for additional graded dopant profile portions to the retrograde wells 4 and 8 of Yamashita, as taught by Nishi.

179. Nishi teaches a “modulated retrograde well” dopant profile—applicable to CMOS transistors—in its Fig. 11 and surrounding text. (Ex. 1012, p. 086). Figure 11 of Nishi is reproduced below, and shows a dopant concentration profile with depth, where the surface of the substrate is on the left side of the figure:

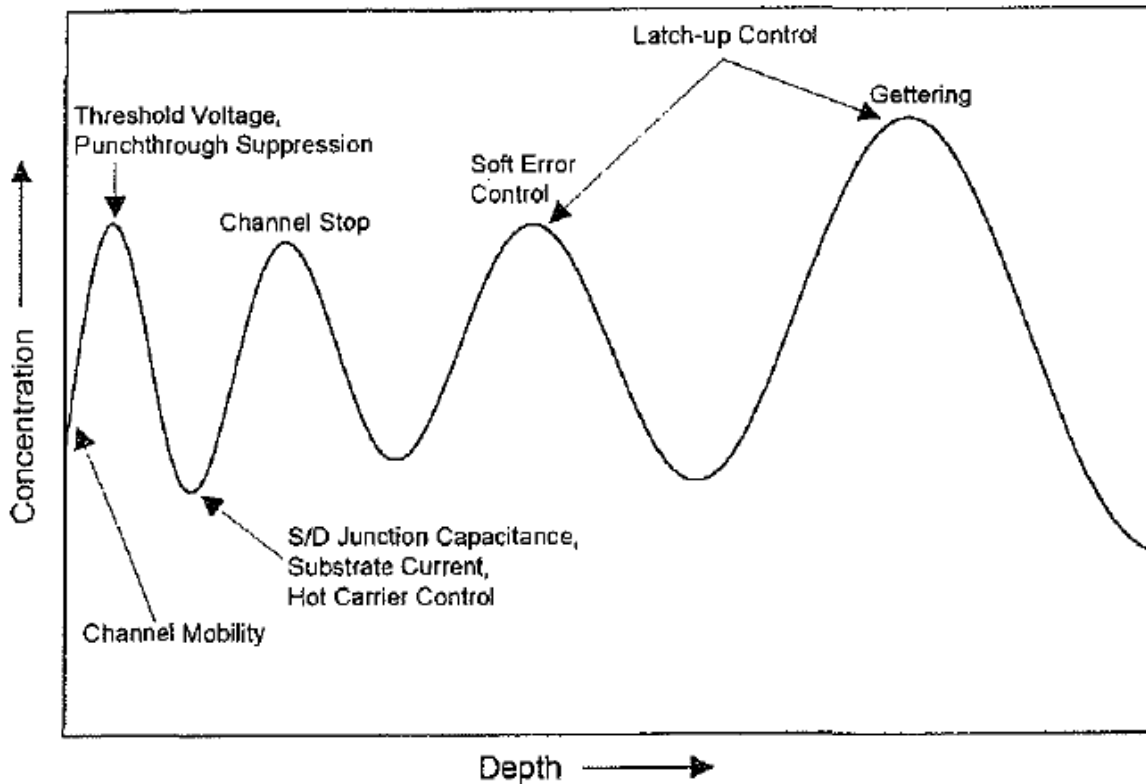
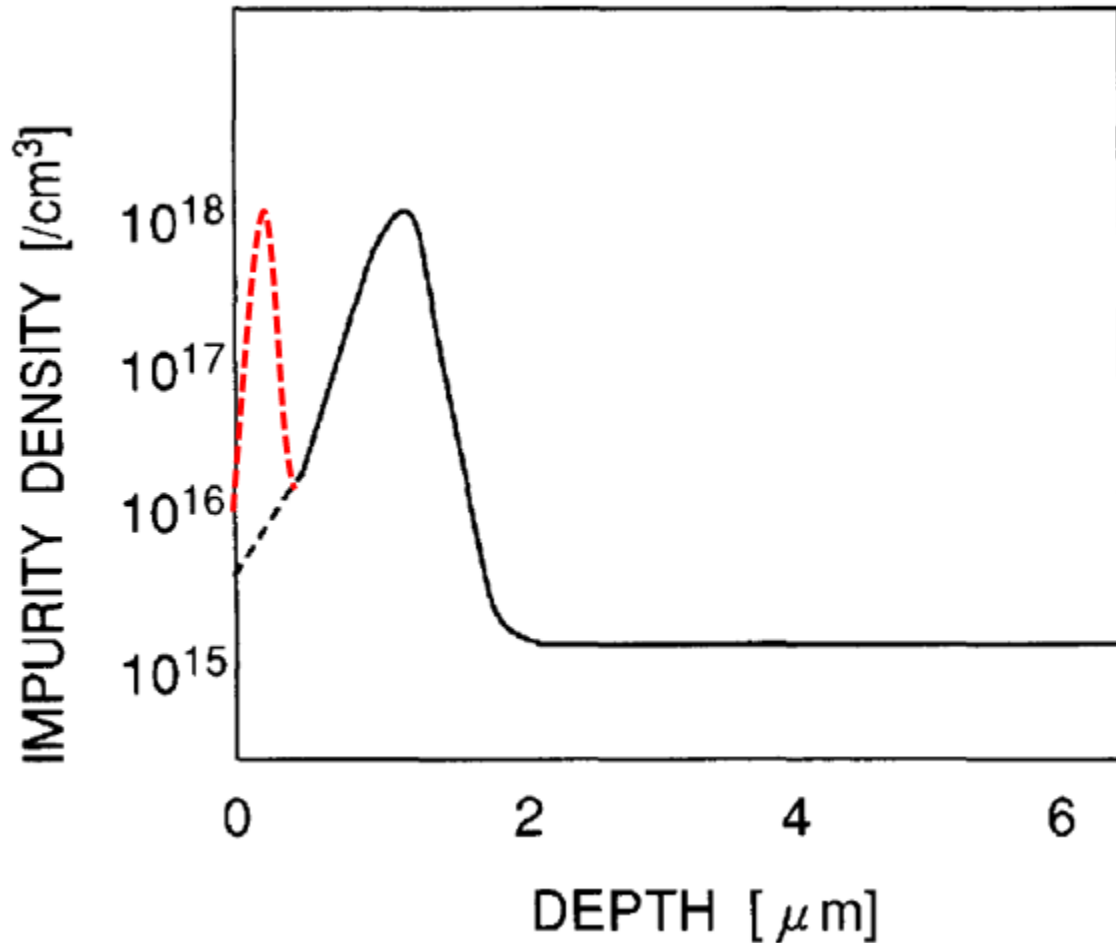


Figure 11 Doping profile of a modulated retrograde well structure, showing the device parameters affected by the doping level at each depth. Adapted from references [40,41].

(Ex. 1012, Fig. 11, p. 086).

180. In my opinion, it would have been obvious to provide for at least the left-most peak in the Nishi Fig. 11 profile (labeled with “Threshold voltage, Punchthrough Suppression” at the peak and “Channel Mobility” at the left shoulder”) in Yamashita’s retrograde wells 4 and 8. (Ex. 1012, p. 086). This would have provided for a graded dopant profile that is very close to the surface of the device in Yamashita, and within the transistor channel. A modified version of Fig.

55 of Yamashita, showing the additional peak from Nishi, is provided below, with an added, red-dashed line indicating the peak from Nishi provided for punch-through suppression and threshold voltage, with adjacent valleys for channel mobility and hot carrier control:



181. A similar modification would be made to the dopant profiles in both wells 4 and 8, using n-type and p-type dopants, respectively.

B. Rationale (Motivation) Supporting Obviousness

182. In my opinion, the modification would have been obvious.

Yamashita already suggests such a modification, stating:

“A plurality of transistors or a single transistor is formed on the retrograde p well 8, the retrograde n well 4 and the retrograde n well 9 (not shown), and a CMOS is formed on the logic circuit region. **In this case, in the retrograde wells, the channel implantation layer for punch-through prevention and threshold control is formed at the depth of 0-0.2 μm from the substrate as needed.**”

(Ex. 1005, 21:55-61)(Emphasis added). This expressly suggests forming an implantation in the transistor channel region, which would result in a peak of dopant concentration at a depth between 0 and 0.2 μm . Furthermore, the purpose of this implantation is for “punch-through prevention and threshold control”, which are exactly the purposes shown in Fig. 11 of Nishi for the left-most (shallowest) dopant concentration peak. This implantation would make sense in Yamashita’s device, the transistors of which are potentially susceptible to deterioration by hot carriers and may have required adjustment of the threshold voltage.

183. Furthermore, Yamashita teaches that the transistors in the Logic Circuit Region (*see* Fig. 53) are MOSFET transistors in a CMOS process. (Ex. 1005, 21:34). Nishi teaches that the modulated retrograde well is particularly effective for

such transistors, and had, by 2000, replaced other standard well processes. (Ex. 1012, p. 086). Nishi explains:

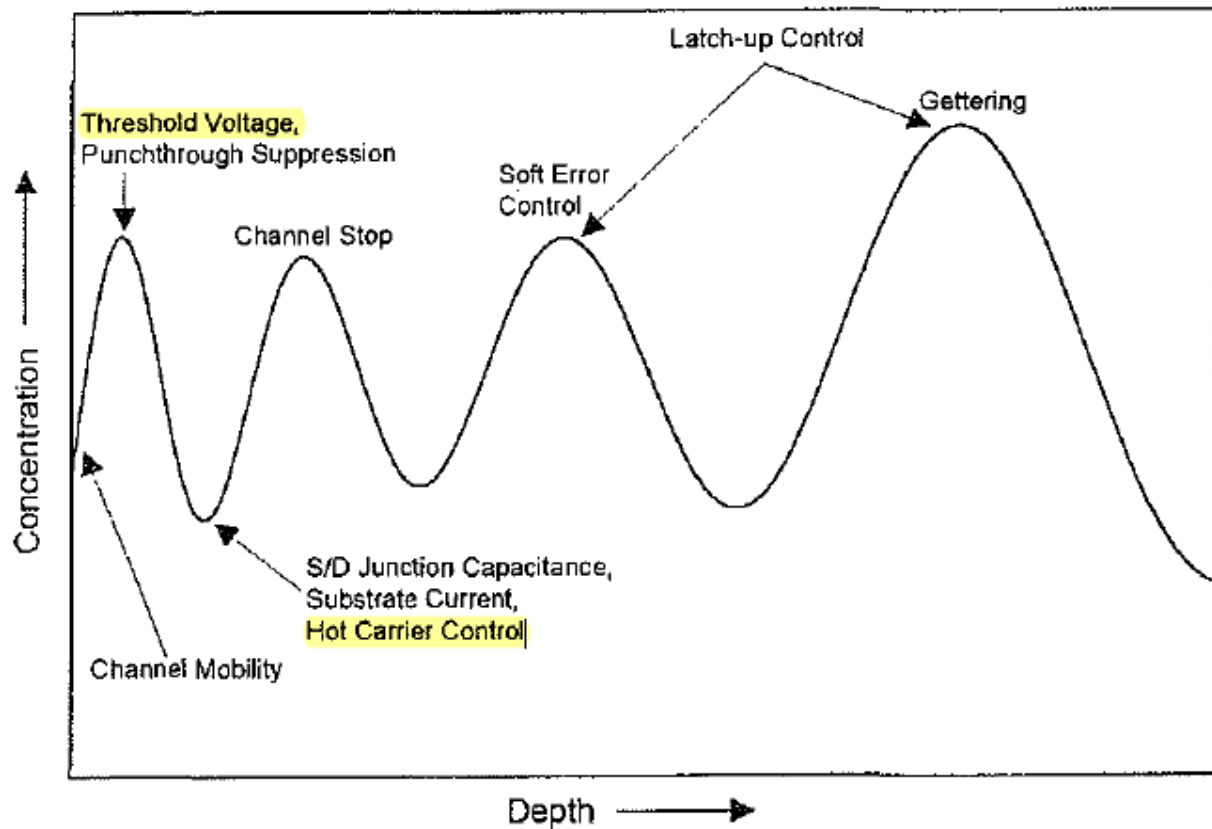
“Ion implantation is essential for fabricating the twin tub (both p-well and n-well implants) CMOS process. **The modulated well structure (Fig. 11) has replaced the older diffused well process, due to its higher processing flexibility and lower cost.** Since the well forms the MOSFET’s ‘back gate’, the well doping will fundamentally affect the transistor's electrical performance. **Engineering the well with multiple implants and minimal thermal diffusion** allows independent control of dopant levels throughout the depth of the well, and thus **independent optimization of key MOSFET performance characteristics** (Fig. 11). Device speed (carrier mobility, S/D capacitance), inter-device leakage currents, **V_T control, punchthrough suppression**, parasitic transistor effects, and soft error and latch-up resistance can be optimized almost independently by carefully positioned dopant peaks and valleys [41,42]. **Low surface doping levels increase mobility and decrease capacitance.** Heavier doping below the surface (retrograde doping) reduces minority carrier collection by reducing depletion widths, thus reducing soft errors and latch-up susceptibility [43-46]. This degree of design flexibility is not possible with diffused wells.”

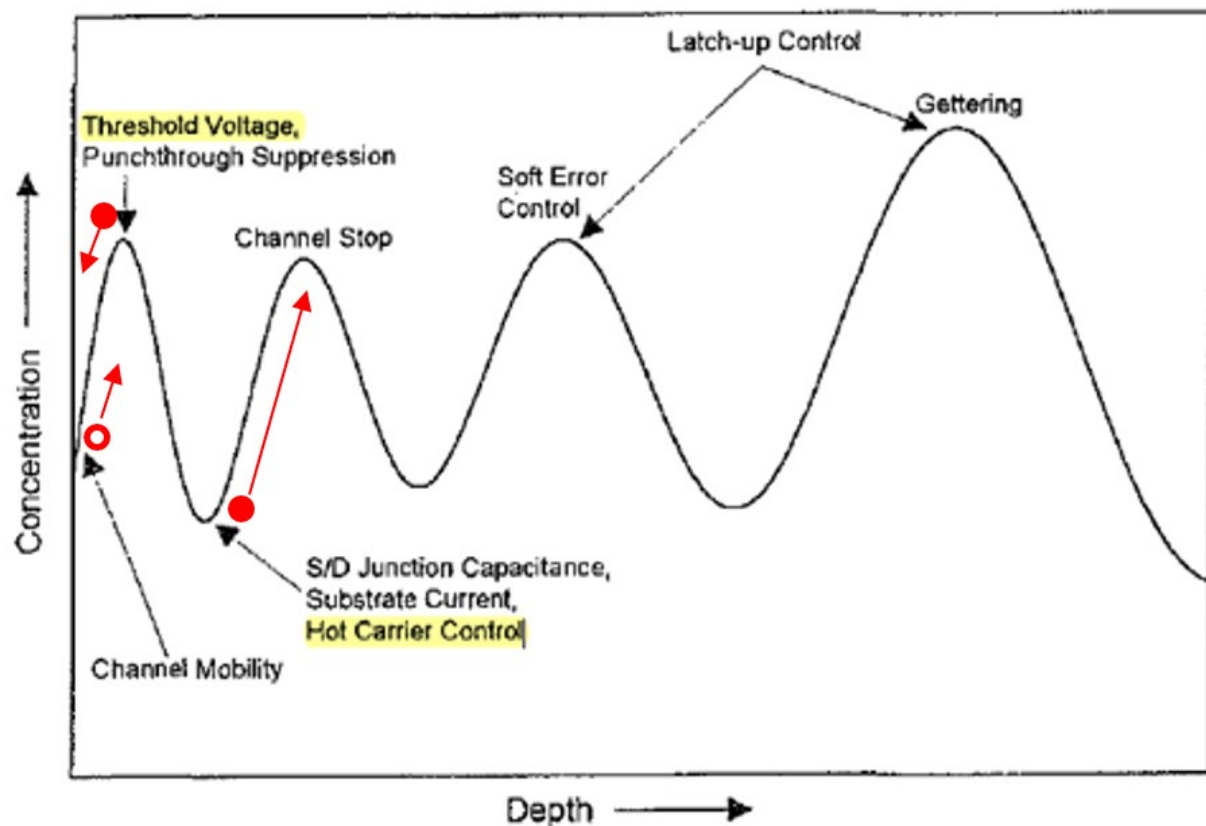
(Ex. 1012, p. 086)(Emphasis added). Nishi thus teaches to engineer wells “with multiple implants and minimal thermal diffusion”, which results in multiple peaks in the dopant profile concentration, as shown in Fig. 11. (Ex. 1012, p. 086). Among

other things, this allows better control of the threshold voltage of the transistor (“ V_T ” in the quote above), allows for punch-through suppression, and allows for hot carrier control, as shown in Nishi Fig. 11 and (as to V_T and punch-through suppression) taught expressly by Yamashita. (Ex. 1005, 21:55-61)(Ex. 1012, p. 086). Nishi further teaches that having a lower dopant concentration at shallower depths in the transistor channel “increase[s] mobility and decrease[s] capacitance”, while “[h]eavier doping below the surface (retrograde doping) reduces minority carrier collection....” (Ex. 1012, p. 086). To the extent desired, a POSITA could have used all four peaks shown in Nishi Fig. 11 in an obvious manner. These advantages (the ability to better control the transistor threshold voltage, punch-through suppression, hot carrier control and increased transistor channel mobility, decreased minority carrier collection and decreased capacitance) would have been seen as valuable by a POSITA in the relevant timeframe, and would have rendered the combination obvious.

184. Furthermore, it would have been obvious to arrange the doping peak of Nishi in Yamashita specifically to aid the movement of carriers from the first and second active regions towards an area of the substrate where there are no active regions. I again note that I understand that the Patent Owner interprets the relevant claim limitation to require carrier movement to be aided in a downward direction. This would have been obvious to a POSITA in order to achieve the threshold voltage

control and hot carrier control, as shown in Fig. 11 of Nishi, reproduced again here with highlighting added in the first version of the figure, and with highlighting and carriers with arrows added in red in the second version:





(Ex. 1012, Fig. 11, p. 086). Threshold voltage and punchthrough voltage control can be provided by the gradient in the doping profile. A lower doping is preferred at the surface to have the desired threshold voltage. A higher doping is preferred slightly deeper than the surface in order to prevent the punch-through (effectively an electrical shorting of the transistor). The doping level required to provide punch-through suppression is too high to provide the desired threshold voltages, (typically in the range of 0V – 0.6V). Engineering of the implanted doping profile of the first peak from the surface can provide the desired threshold voltage and punch-through voltage. In addition, the graded doping profile will aid the movement of majority

carriers (holes shown in open red circles) away from the surface toward the substrate (up the left-side slope of the first peak), and it will aid the movement of minority carriers (electrons shown in solid red circles) toward the surface, thus providing an increase in the device switching speed. As I discuss above in ¶45, FET transistors work by applying a potential to a gate electrode. The potential will create a voltage that draws minority carriers into the region under the gate electrode. By grading dopant concentration underneath the gate electrode, the ability of carriers to be drawn into the channel will be affected, thus increasing the speed at which minority carriers can move to the surface, and majority carriers can move away from the surface, while maintaining a lower surface doping to set the desired level of potential required to be placed on the gate to activate the transistor. Thus, the use of the shallow peak as shown in Fig. 11 of Nishi allows the designer a way to influence threshold voltage that is less coupled to the punchthrough voltage. (Ex. 1012, 086). Such independent control over design parameters is an express goal of Nishi's modulated well. (Ex. 1012, p. 086). Furthermore, hot carriers are controlled by the right-hand slope of the first peak in Fig. 11. Hot carriers are carriers that have high energy, which can be emitted from a depletion region and migrate to a transistor gate oxide region, where they can damage the gate oxide. The graded dopant region shown in Fig. 11 of Nishi aids such carriers (electrons in this case) away from the surface toward the substrate, where they cannot damage the transistor. Thus it would

have been obvious to arrange the graded dopant profile in order **to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions** under the Patent Owner's claim construction.

185. Finally, the technique suggested by Nishi was, in the relevant timeframe, a well-known (indeed, textbook) technique for improving exactly the type of transistors taught by Yamashita, and could have been used in Yamashita with no unpredictable results, and was thus obvious.

C. *Graham* Factors

186. The Graham factors are the same as discussed under Grounds 1 and 2, with the exception that the relationship of the prior art to the claims is altered in this Ground.

D. Reasonable Expectation of Success

187. In my opinion, a POSITA in the relevant timeframe would have had a reasonable expectation of success in implementing the transistor channel peak (and any other of Nishi's peaks in Fig. 11, as desired). The dopant profiles shown in Nishi were accomplished by ion implantation, which was a standard, predictable technique in the relevant timeframe.

E. Analogous Art

188. Nishi is analogous art because it is in the same field as the '014 patent (semiconductor devices) and as a handbook on manufacturing such devices,

would have been highly relevant to the problems purportedly facing the named inventors.

F. Claim Mapping

189. The claim mapping is the same as described in Ground 2, except that the first and second active regions would have one (or more, if desired) additional **at least one graded dopant concentration to aid carrier movement**. These graded regions would be the additional peak as discussed above, present in the channels of transistors formed in both the retrograde p-well 8 and retrograde n-well 4. This peak is a **graded dopant profile** in each active region, which would have obviously and necessarily been **to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions** (claim limitations [1f] and [21f]), as explained above in the section entitled Rationale (Motivation) Supporting Obviousness. The mapping for other elements of the independent or dependent claims does not change. In particular, the mapping for claims 9-12 and 28-30 (the language of which pertains to the graded dopant concentration) does not change if the graded region is at shallower depth.

VIII. OATH

190. This declaration and my opinions herein are made to the best of my knowledge and understanding, and based on the material available to me, at the time of signing this declaration. I declare under penalty of perjury under the laws of the United States of America that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon.

December 9, 2022

Date



R. Michael Guidash