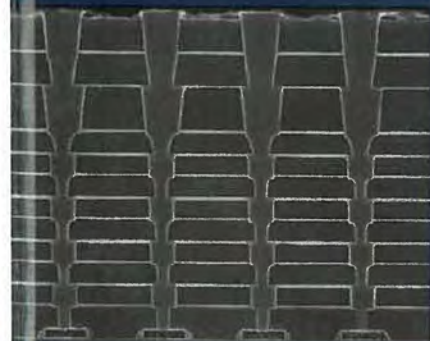
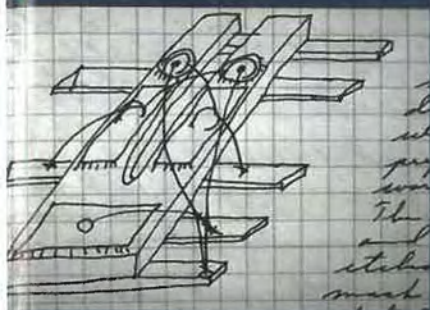




Handbook of Semiconductor Manufacturing Technology

edited by
Yoshio Nishi
Robert Doering

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Foreword

In 1958, the year of the invention of the integrated circuit, a single silicon transistor sold for about \$10. Today, it is possible to buy more than 50 million transistors for that price. Today you receive not only the transistors but at least an equal number of passive components and a set of interconnections permitting the devices to function as a dynamic random access memory. This cost reduction is unprecedented.

This progress has been the work of tens of thousands of very capable engineers working around the world. Every step of the fabrication process, from preparation of pure silicon materials to the final packaging operations, has been carefully examined, reinvented, and improved. Highly automated equipment has been developed for the manufacturing processes. This book provides an overview of the current status of this work, and a look at the progress to be expected in the future.

These cost reductions have tremendously expanded the field of electronics. In 1958, the most common electronic products were radios and television sets, and the semiconductor market represented about \$218 million. Today, semiconductors are found in everything from automobiles to x-ray machines, and the worldwide market exceeds \$150 billion. The story is not over, and more progress can be expected.

*Jack S. Kilby, M.S.E.E.
Texas Instruments Inc.
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Preface

The primary purpose of this book is to serve as a reference for practitioners and developers of semiconductor manufacturing technology. It contains many graphs, tables, and formulas that experts in each subfield should find useful to have close at hand. However, unlike a "mostly numbers" handbook, we have embedded the compact reference information into a basic description of current and anticipated practice in integrated-circuit manufacturing. Although not as tutorial as might be found in a textbook, this description attempts to make each chapter very readable to specialists in the subfields covered by the other chapters. Thus, we hope that the book will be useful to a broad audience involved in the development and manufacturing of semiconductor products. To this end, we have also included some overview chapters, each of which serves to introduce a section of closely-related chapters that together cover a more general topic such as interconnect. Most of the chapters deal with individual process, equipment, material, or manufacturing control/support/infrastructure technologies. Note that the book is intended to address only silicon-based manufacturing, although many of the topics are at least partially applicable to building devices with other semiconductor substrates. We have also asked the authors to include generous reference lists and bibliographies pointing the readers to more detailed sources.

Our editorial philosophy has been to give the authors considerable freedom in addressing their topics. Thus, you may notice a breadth of approaches, as well as styles, across the chapters. Some have provided more history, others, more prognostication. There are chapters that stick pretty closely to the traditional basics, and others that emphasize the current and future R&D challenges in the area. We trust that this flexibility has provided each author with the opportunity to create a chapter that reflects his personal perspective and sense of excitement about what is important today in that area. Of course, semiconductor manufacturing technology has become so specialized that many of the chapter subjects required the collaboration of several experts to cover the topic, which also serves to widen the perspective.

It's definitely a challenge to provide up-to-date reference books in a field as broad and rapidly changing as semiconductor manufacturing technology. Just look at both the growth in book length and the technology acceleration found in the *National and International Technology Roadmap for Semiconductors* editions published from 1992 through 1999! We have tried to anticipate what will be most relevant to readers now and in the future. Fortunately, we were able to enlist the support of many distinguished technologists from industry and academia, who are presently advancing the state of the art, to author chapters on their areas of expertise. Some of these areas have become more recognized as distinct specialties (e.g., with dedicated manufacturing and R&D staff) only within the last few years and would not have been treated as such in earlier books. The continued scaling and evolution of device construction has also resulted in new issues and perspectives that have influenced the topics and their treatments and relationships within this book. Our authors have responded to this challenge with an

excellent job of collaborating and coordinating between and within chapters. Of course, this would have been significantly more difficult a few years ago, especially across such a geographically dispersed group. But today, we can take great advantage of the personal and global interconnectivity that our silicon technology has enabled. We also work together in an increasingly global industry, with many more partnerships, consortia, program committees, and "roadmap working groups," in addition to the traditional professional societies, to help us meet colleagues and exchange ideas. As always, it's an exciting time to be in the semiconductor industry, and we appreciate this opportunity to share the technical knowledge and experience of our authors/colleagues with the reader.

In addition to thanking our authors, we would especially like to acknowledge the very many important contributions of Tim Wooldridge, our Assistant Editor, and the excellent work of Kristie Conner, who helped with numerous editorial activities. We have all enjoyed working on this project and hope that you find the book interesting as well as useful.

Robert Doering
Yoshio Nishi

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Handbook of Semiconductor Manufacturing Technology

Silicon Materials

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I. INTRODUCTION

Silicon is the major semiconductor material used in solid state electronics. Silicon in the form of a single crystal wafer is the basic building block for the integrated circuit (IC) fabrication. To keep pace with the growth in IC processing technology, chip size and circuit complexity, silicon crystal and wafers have to be prepared with continued increases in diameter and improvements in perfection. Modern Ultra Large Scale Integration (ULSI) ICs, fabricated with design rules approaching 100 nm, have to depend on the availability of highly perfect single crystals, which are prepared exclusively from silicon pulled from the melt by the Czochralski (CZ) technique. The CZ silicon material prepared today must meet the challenges imposed by the stringent requirements of the starting materials for current and future design rule generations, as guided by the Starting Materials Road Map of the National Technology Roadmap for Semiconductor (NTRS).

The purpose of this chapter is to review the fundamental aspects of silicon technology and to discuss the advances in understanding of the science and engineering of this technology with respect to the challenges in the material requirements for ULSI fabrication.

II. SILICON CRYSTAL GROWTH PROCESSES

A. Float Zone Silicon Growth

The float zone method (FZ) is based on the zone-melting principle [1] and was invented by Theuerer [2]. Figure 1 shows a schematic of the FZ process. A polysilicon rod is mounted vertically inside a growth chamber under vacuum or an inert atmosphere. A needle-eye coil provides radio frequency power to the rod causing it to melt and maintain a narrow, stable molten zone by balancing the surface tension and gravitational forces. The levitation effect of the radio frequency field helps to support a large molten zone. As the molten zone is moved along upward the polysilicon rod, the molten silicon solidifies into a single crystal and, simultaneously, the material is purified. To initiate the growth, in the bottom-seed FZ, the seed crystal (~10 mm in diameter) is brought up from below to make contact with the drop of melt formed at the tip of the poly rod. A necking process is carried out to establish dislocation-free feature before the "neck" is allowed to increase in diameter to form a taper and to reach the desired diameter for steady-state body growth. During this process,

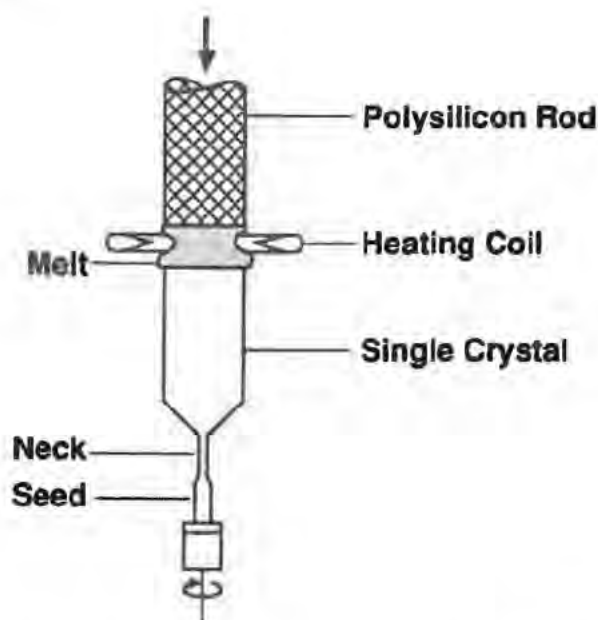
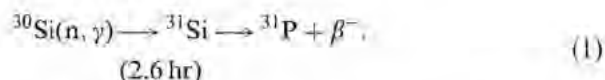


Figure 1 Schematic of a float zone silicon growth arrangement.

the shape of the molten zone and crystal diameter are monitored by infrared sensors and are adjusted by the rf power input to the coil and travel speed. Details of FZ technology are discussed by Keller and Muhlbauer [3]. Current FZ technology can produce high quality FZ silicon up to 150 mm in diameter in production quantities.

FZ crystals are doped by adding the doping gas phosphine (PH_3) or diborane (B_2H_6) to the inert gas for n - and p -type, respectively. Polysilicon rods for FZ growth may also be doped in the gas phase and dopant redistribution by zone melting. Since the doping is by gas phase interaction with the molten silicon, axial dopant uniformity is achieved. However, due to the very nature of FZ growth configuration, the small "hot zone" lacks thermal symmetry. As a result, temperature fluctuations, remelting phenomenon and dopant segregation cause FZ silicon to display more microscopic dopant inhomogeneity, or dopant striations than observed in CZ silicon. Severe dopant micro-inhomogeneity can be circumvented for n -type FZ via neutron transmutation doping (NTD) [4]. In NTD, high purity FZ crystal is subjected to thermal neutron bombardment, causing some of the silicon isotope ^{30}Si ($\sim 3.1\%$ of Si) to form the unstable isotope ^{31}Si , which decays to form the stable phosphorus iso-

tope ^{31}P , such that



Since neutron bombardment (both thermal and fast neutrons) induces radiation damages, the irradiated crystal must be annealed at about 700°C for defect annihilation and to restore resistivity due to the phosphorus doping. In the FZ silicon with NTD, the dopant striations are greatly reduced. However, the NTD method is only feasible for high resistivity, phosphorus doped FZ. Low resistivity doping of FZ by NTD would require excessively long irradiation (more lattice damages) and is not feasible. The NTD process for p -type doping is not available.

Unlike CZ growth, the silicon molten zone in FZ growth is not in contact with any substances except the ambient gas, which may contain doping gas. Therefore, the FZ silicon can easily achieve much higher purity and higher resistivity (resistivity ranges from a few tens to a few thousands ohm-cm) than the CZ silicon (generally, < 50 ohm-cm). A large volume of FZ silicon is used in the fabrication of semiconductor power devices and infrared sensors. However, its application in the microelectronic IC fabrications is rather limited. The main reason is FZ's low interstitial oxygen content. The oxygen content of FZ crystal is in the range of 10^{16} atoms/ cm^3 [5], which is two orders of magnitude below that of conventional CZ silicon and is far below the solid solubility limit at IC's thermal processing temperatures. Consequently, FZ silicon lacks the ability of oxygen precipitation and associated internal gettering potential. Furthermore, the "residual level" of oxygen in FZ also results in lower mechanical strength than the CZ in terms of its ability to withstand thermal stress and to suppress slip, wafer bow and warp during high temperature processing [6,7]. The presence of "sufficient" interstitial oxygen in CZ silicon appears to have strain hardening effects in the silicon lattice and serves as obstacles for dislocation initiation/propagation. Numerous studies [8,9] have shown that the difference in mechanical strength can be attributed to the difference in the oxygen content and associated defects. These are the main reasons that CZ silicon is almost exclusively used for IC processing. In order to overcome FZ's shortcomings, oxygen [10] and nitrogen [11] doping during FZ growth have been reported. It was shown that doping concentrations of $1\text{--}1.5 \times 10^{17}$ / cm^3 for oxygen or 1.5×10^{15} atoms/ cm^3 for nitrogen can significantly increase FZ's strength.

Nitrogen doped FZ proves useful in microelectronics device fabrication where oxygen-free material is desirable [12].

B. Czochralski Silicon Growth

Czochralski pulling method (CZ) is named after J. Czochralski [13]. However, the pull-from-melt method widely employed today was developed by Teal and Little [14]. Small diameter CZ silicon crystals were first used in the early 1960s for IC fabrication (and earlier for discrete Ge and Si transistor fabrication). The development of the dislocation-free growth technique and automatic diameter control in the late 1960s led to a rapid growth in silicon crystal diameter and charge/grower size during the last two decades. Today, 200 mm silicon crystals, weighing over 80 kg are not uncommon; the 300 mm diameter silicon growth is in pre-production and 450 mm era is already under development. In the ULSI era, the emphasis on the CZ silicon crystals for ICs are the uniformity of dopant and oxygen incorporation and microdefect control. Significant research and development efforts are devoted to these aspects in order to satisfy the stringent requirements of IC processing for sub 250 nm ICs. The CZ silicon growth process is controlled by many variables. It involves aspects of heat transfers and material phase transitions. Modern CZ silicon growth equipment transformed the "art" of crystal growth into an engineering discipline. Although most of the steps in the growth process can be monitored and controlled by a computer/microprocessor, many critical steps nevertheless still require the judgement and attention of an experienced operator. Therefore, significant differences can still exist in the properties of the crystals grown from different grower designs and growth processes.

Figure 2 shows a schematic of a typical modern CZ grower for large diameter silicon growth. Major components include the so-called hot zone, crystal-pull/rotation and crucible-lift/rotation mechanisms, diameter and temperature sensing devices. The puller is operated under a reduced pressure inert ambient (typically 18–20 torr). CZ silicon growth consists of three major processes: (1) seeding and necking, (2) body growth, and (3) tang growth/termination. The necking process is one of the most critical steps in dislocation-free CZ growth; the body growth can not be initiated without a successful necking process. The necessity of the procedure and principles of necking are given below and are also common to the FZ growth discussed in the previous section.

A CZ growth process begins with the melting of polysilicon nuggets and doping element or alloy contained in a silica crucible. Temperature adjustments and stabilization follow the melt-down such that the melt surface temperature is slightly supercooled. A crystal seed (~12 mm in diameter) attached to the end of a steel cable is dipped into the melt. If the crystal-melt contact forms a smooth meniscus, the "necking" process based on Dash's [15] technique may begin. The reason for necking is as follows: The growth of dislocation-free silicon has to be "extended" from a dislocation-free silicon crystal. Although the seed crystals used in CZ are usually dislocation-free, upon contacting the melt, dislocations are generated due to thermal shock. These dislocations must be eliminated before the full diameter crystal growth can begin. Necking is a procedure to out-grow dislocations. During necking, the seed crystal is gradually decreased in diameter by increasing the pull speed and appropriate temperature adjustment. The goal is to reach a steady state neck growth condition with a neck diameter of 3–4 mm and a pull rate of 4–6 mm/min. The dislocation-free crystal is usually achieved after a few centimeters of growth. Two phenomena may occur during the necking. When the seed diameter is large in the early stage of necking, the thermal stress cause dislocation movements by glide, cross slip and climb mechanisms, since the temperature is above the "plastic" temperature ($>900^{\circ}\text{C}$). In the growth of $\langle 111 \rangle$ and $\langle 100 \rangle$ crystals, the growth axes are oblique or perpendicular to $\{111\}$ slip planes. The dislocations can therefore glide out of the crystal surface after sufficient time. For $\langle 110 \rangle$ growth, because $\langle 110 \rangle$ is contained in a $\{111\}$ plane, the seed has to be oriented a few degrees off the pulling axis toward the direction perpendicular to the $\langle 111 \rangle$ plane, to facilitate dislocation eliminations. When the neck is 3–4 mm in diameter under high speed pulling, the stress is relatively small, causing slow or no movement of the prevailing dislocations. When dislocation movements are slower than the advancing solid-liquid interface, dislocation-free growth is obtained. Typically, the dislocation-free status is accompanied by the growth of strong ridges ($\langle 100 \rangle$ crystals) or "flats" ($\langle 111 \rangle$ crystals) on the crystal's symmetry positions, which are actually due to prominent $\{111\}$ facet growth at these positions [17].

Once the dislocation-free growth is achieved through necking, the diameter may be expanded by "shoulder" growth until it reaches the desired diameter. The body growth is under automatic diameter control (ADC), in which the pull rate is slaved

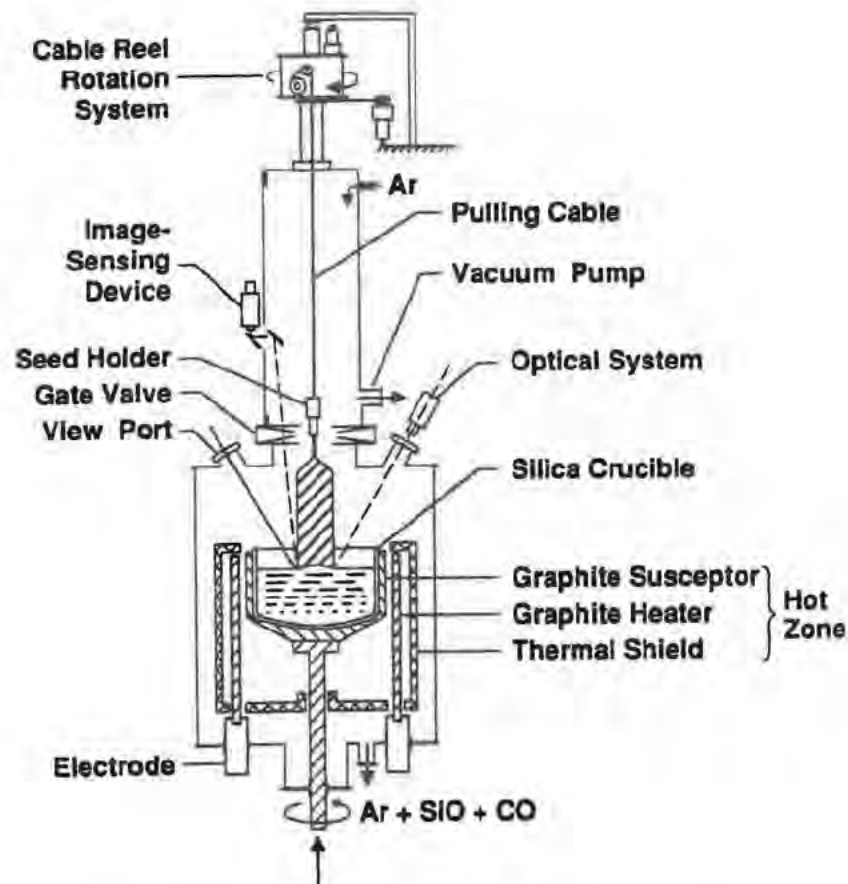


Figure 2 Schematic of a typical Czochralski silicon growing system. (From Ref. 15.)

by optically monitoring crystal diameter variations. The ADC is also assisted by minor temperature adjustments slaved by the long-term pull rate changes. The crystal growth process is terminated by a gradual decrease from full diameter to zero in a low pull speed in order to minimize thermal stress by the diameter change and associated slip generations. After the heater power is off, the crystal usually stays in the grower for a period of time for cooling before it is removed from the grower. The total dwell time and temperatures the crystal experiences during crystal growth and cool down constitute the so-called "thermal history" of the silicon crystal. The thermal history of CZ silicon determines the state of nuclei for oxygen precipitation unique to that crystal growth process and is an important consideration, as is oxygen concentration, in oxygen precipitation kinetics. The heart of a CZ puller is the hot-zone. The design of heater and heat shields, for example, determines the

radial and vertical thermal gradients in the melt. These thermal characteristics are intimately related to the growth characteristics, such as interface shape and related thermal stress generation [18]. Although this concept is fundamental to large-diameter silicon growth, little is known about the correlation between the crystal growth system hot-zone design factors and growth characteristics. For a given growing system an empirically observed optimum growth condition is usually obtained by modifying hot-zone components and/or by varying the growth parameters by trial and error. Hot zone thermal characteristics impact many aspects of silicon crystal properties including oxygen incorporation behavior and the thermal history of the grown crystal. Since hot zone design varies from one crystal grower to another, the crystals grown from different growers are expected to differ in these properties. Thermal convection and forced convection conditions are also important

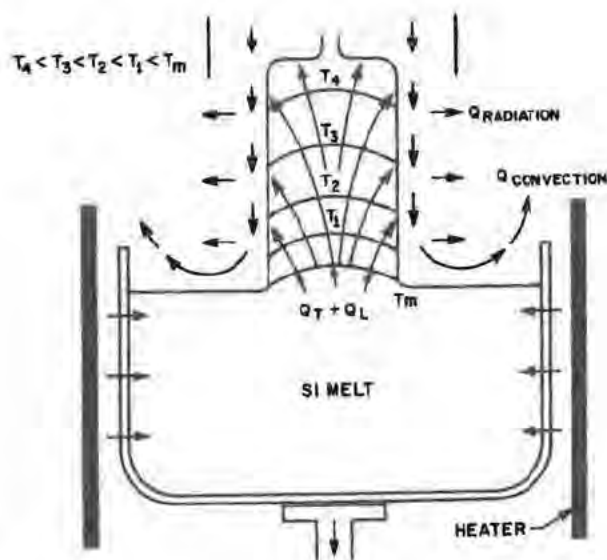


Figure 3 Schematic heat flow in a CZ growth arrangement; Q_L is latent heat and Q_T is heat transfer to the crystal. (From Ref. 18.)

controlling factors for CZ crystal properties and will be discussed in the following section.

III. CHARACTERISTICS OF CZOCHRALSKI SILICON GROWTH

A. Thermal Characteristics for Dislocation-Free Growth

In the growth of large diameter silicon crystals, the thermal characteristics of the growing system are the most important consideration. The structural morphology, perfection, and other properties of large-diameter crystals are determined by the nature of the heat flow balance near the melt-crystal interface. Figure 3 shows the heat flow pattern in a CZ growing system. There is a balance of heat flow about the interface during the steady state growth, i.e., $Q_C + Q_R = Q_L + Q_T$. The interface shape and neighboring isotherms in the growing crystal are controlled by the crystal cooling conditions and melt radial temperature gradient, as well by the solidification rate of the crystal. The crystal cools by radiation and gas convection at the crystal surface, while the melt radial temperature gradient is determined by the melt aspect ratio and heater geometry.

When the crystal diameter is small, the crystal may be considered as a one-dimensional conductor. The surface cooling rate would, at best, affect the growth rate. As the diameter increases, the shape of the interface and isotherms in the crystal becomes highly dependent on the surface cooling rate, the melt radial temperature gradient, and the growth rate. Excessive surface cooling, a shallow radial temperature gradient, or a high growth rate can result in highly concave interfaces and nearby isotherms. This configuration corresponds to a high thermal stress condition [19], which can generate slip dislocations when the thermal stress exceeds the critical resolved shear stress [20]. This usually occurs in the region above the growing interface where the temperature is in the plastic deformation range ($>900^\circ\text{C}$). Once dislocations are generated, they are propagated toward the interface, and continued growth will not be dislocation-free. More often than not, through dislocation multiplication, the growing crystal eventually turns into polycrystalline silicon. Thermal stress-induced perfection loss is usually accompanied by a highly concave interface. Figure 4 is a cross-section of a 150 mm diameter silicon crystal grown under unfavorable thermal conditions. The growth experiments show that increasing the melt radial temperature gradient reduces the curvature of the interface and thus the thermal stress. The thermal stress in a CZ crystal can be modeled and the distribution of the total resolved shear stress on each slip system can be calculated, as was done by Jordan et al. [21] Their model predicts slip dislocations, which are typically detected in poor-quality crystals.

The melt radial thermal gradient also has a profound impact on the crystal shape of large diameter crystals. For example, during the growth of $\langle 111 \rangle$ crystals, flat regions develop on the crystal periphery in the $\langle 211 \rangle$ directions. That is, the lateral growth is retarded in the $\langle 211 \rangle$ directions (see Fig. 5(a)). The flats shown in Figure 5(a) result from excessive supercooling, which is caused by a small radial temperature gradient in the melt or a high convective heat loss at the meniscus. In severe cases the cross-section tends to be triangular. A steeper thermal gradient has been found to minimize such preferential growth.

It should be noted that the aforementioned shape problem due to flat formation is common in lightly doped $\langle 111 \rangle$ silicon growth. In the growth of heavily doped $\text{N}^+ \langle 111 \rangle$ crystals (such as those doped with antimony in the concentration range of $10^{18}/\text{cm}^3$) the situation is quite different. The preferred growth in this case is in the $\langle 211 \rangle$ direction, and facet growth

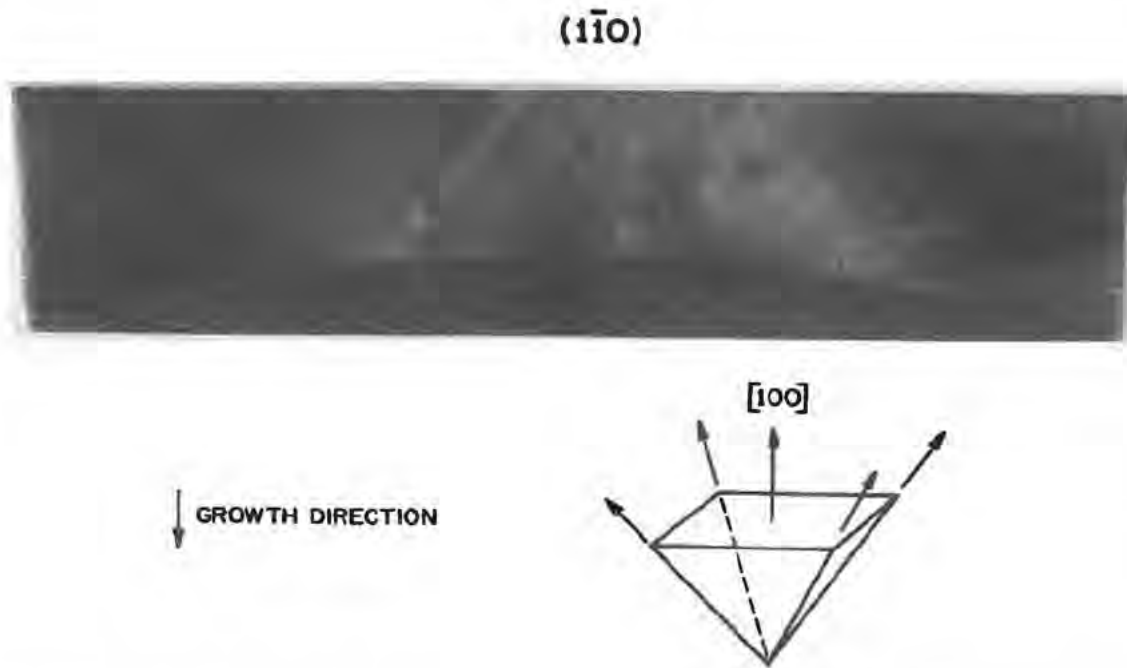


Figure 4 Etched longitudinal cross-section of a silicon crystal of 150 mm in diameter showing stress-generated slip dislocations from an instantaneous interface (curved demarcation) and its propagation above the interface. (From Ref. 18.)

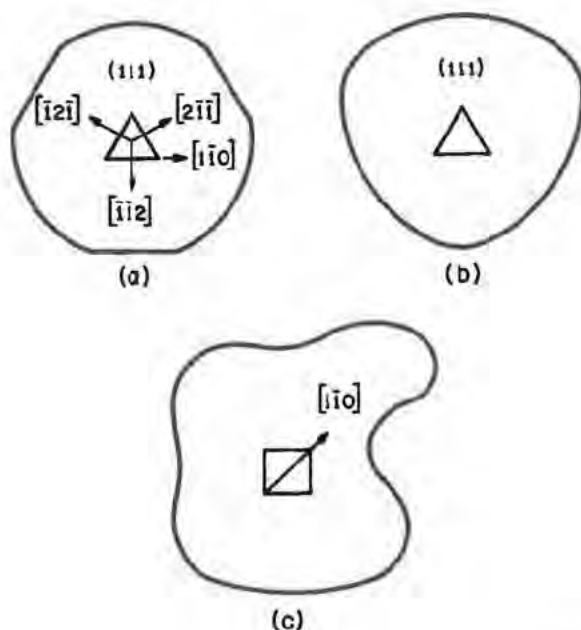


Figure 5 Cross-section shapes of crystals grown under unfavorable thermal conditions: (a) lightly doped *p*-type (111); (b) heavily Sb doped (111); (c) lightly doped (100). (From Ref. 18.)

is retarded. The result is a cam-shaped crystal cross-section, as shown schematically in Figure 5(b). A theoretical model that predicts the effect of dopant type and concentration on silicon growth habit has not been developed. The radial thermal gradient also affects the shape of (100) crystals. Small gradients can cause preferred lateral growth in the $\langle 110 \rangle$ directions, resulting in a rectangular or square cross-section (Fig. 5(c)). The preferential growth is very sensitive to the thermal conditions, and the shape of the crystals can be used as a measure of the thermal conditions of a growing system. This is especially true for lightly doped (111) crystals.

In growing crystals of large diameter, the main concern is the thermal stress build-up due to massive latent heat of solidification at the interface and longer path for heat dissipation during crystal growth. To maintain the heat balance at the interface for dislocation-free growth discussed above, the growth rate has to be reduced as the crystal diameter is increased. This trend has been observed in the development of 300 mm and 400 mm diameter crystal growth, as will be discussed in a later section. From thermal stress considerations, there will be a practical upper limit for the diameter in CZ silicon crystal growth.

B. Impurity Incorporation

1. Axial Dopant Distribution

In the growth of silicon crystals from large melts using ADC mechanisms involving pull rate and/or temperature changes slaved to optical diameter measurements, the axial dopant distributions follow the normal freezing behavior [22],

$$C_s(x) = C_0 k (1 - x)^{1-k} \quad (2)$$

where C_s , k and x are crystal dopant concentration, dopant segregation coefficient and fraction of melt solidified, respectively. C_0 is the initial dopant concentration of the melt. Complete mixing takes place in the melt by vigorous thermal convection and the segregation coefficient of the dopant assumes the equilibrium value k_0 in most instances. In the reduced pressure growth of heavily doped silicon involving dopants with high vapor pressure, such as antimony, the k value can deviate significantly from the equilibrium value (k assumes a value greater than k_0 but less than unity). Due to dopant segregation, there is a spread in dopant concentration along a CZ crystal. The degree of the spread depends on the value of the dopant. The smaller the k value, the larger the spread in concentration. The segregation effect of the dopants often limit the "yield" of the CZ silicon crystals. Non-standard CZ methods, such as double crucible method [17,23] and continuous growth method [24] have been used to eliminate the effect due to segregation (see Fig. 6). The axial microscopic uniformity is controlled by the microscopic growth rate. Thermal convection, thermal asymmetry, and pull-rate fluctuations are sources of microscopic growth fluctuations. The nature of the microinhomogeneity of impurity in CZ crystals will be discussed following the discussion of melt convection flows and effective segregation coefficient.

2. "Unintended Dopants"

Impurities in the crucible material or the vapor above the melt can be incorporated into the melt and into the silicon during crystal growth. Oxygen and carbon are the major impurities incorporated into CZ silicon. Their concentrations in CZ crystals are on the order of 10^{18} atoms/cm³ and 10^{16} atoms/cm³ for oxygen and carbon, respectively. The silica crucible is an infinite source for oxygen. Molten silicon dissolves the silica and absorbs oxygen. Unlike normal dopants, oxygen in the silicon melt is a dynamic system and the oxygen distribution is not homogeneous in the

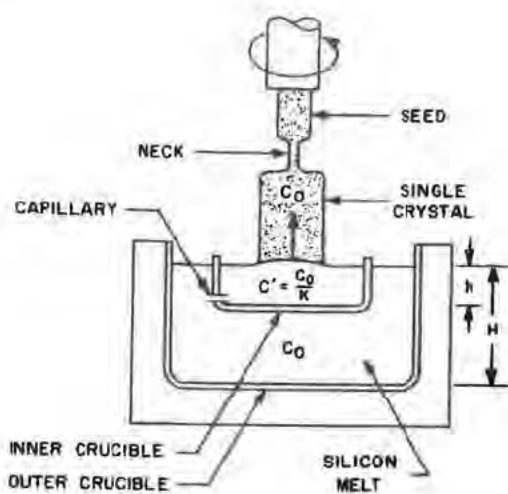
melt. The oxygen concentration incorporated into the crystal is a result of complex interactions between the crucible dissolution rate and the nature of the melt flow (which determines how the oxygen-rich melt is transported). Therefore, the axial oxygen profile of a silicon crystal is not the result of normal freezing behavior and the concentration profile can vary widely depending on the grower thermal characteristics and growth parameters used.

The source of the carbon is the graphite material making up the hot zone of the crystal grower. The silicon monoxide evaporated from the melt surface interacts with hot graphite components and is reduced to carbon monoxide before reentering the melt following:

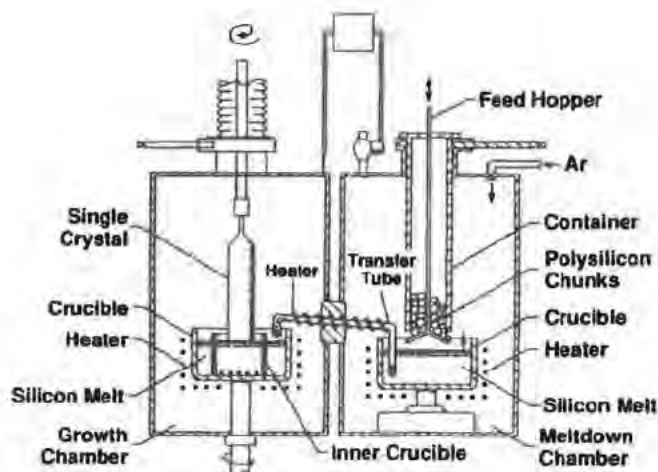


The introduction of CO into the melt is a continuous process. The incorporation from the vapor phase and residual carbon content in the starting polysilicon (<0.2 ppma) results in a normal-freezing-type carbon concentration profile in CZ silicon (carbon has a small segregation coefficient, $k_0 = 0.07$). Carbon in silicon has not been shown to affect IC characteristics. Carbon concentration of up to 4 ppma did not directly change DRAM performance or yield [26]. However, carbon in silicon has been observed to enhance oxygen precipitation. To utilize this property for oxygen precipitation enhancement, one must grow silicon with controlled carbon concentration and uniformity. Such silicon growth process has not been reported. For ULSI applications, it is a common practice to keep carbon at minimum levels (<0.5 ppma).

Besides carbon and oxygen, metal atoms can also be incorporated into the growing crystal. Metallic elements, especially transition metals, are among the most undesirable contaminants in silicon material for IC processing due to its role as lifetime killers. They are also fast diffusers in silicon at elevated temperatures and even at 700°C. Fortunately, due to the small values of their segregation coefficients (10^{-4} – 10^{-6}) [27], no significant metal can be grown into silicon crystals when the melt is contaminated with metals [28]. However, transition metals transported in the vapor phase can condense and diffuse through the silicon crystal surface at high temperatures and rapidly into the bulk. The diffusion of metal contaminants is most "effective" at the grown crystal surface above the melt. The metal contaminants can be evaporated from an overheated metal or alloy surface of grower components. An example is the stainless steel



(a)



(b)

Figure 6 (a) Schematic representation of a double crucible growth arrangement, (b) Continuous liquid-feed Czochralski growth furnace. (From Refs. 25,26.)

shaft/cable for crystal pull and rotation, which is usually not water-cooled. Overheating of these parts occur when they are too close to the hot zone. The use of an extended seed chuck (seed holding device attached to the bottom of the steel shaft/cable, made of ceramic materials or graphite) would minimize the overheating of the steel shaft/cable. Contaminated graphite for fabrication of hot zone parts, such as heater, susceptor and heat shields is another possible source of metal contamination. Metal evaporated from the graphite parts can contaminate the grown silicon via solid phase diffusion [29].

3. Macroscopic and Microscopic Inhomogeneity

a. *Effective Segregation Coefficient, k_{eff} and Interfacial Boundary Layer.* The degree of incorporation of an impurity at the freezing front is controlled by its segregation coefficient. When the solidification rate is low, or the impurity concentration is dilute, the segregation coefficient assumes a value very close or identical to the equilibrium value. In CZ silicon growth with finite or higher growth rate, the dopant ($k_0 < 1$) incorporation behavior was found to result in a k value which deviated from the equilibrium value, for example, the k was observed to increase with increasing growth rates [30]. This behavior is due to the finite diffusivity of the dopant in the crystal that

can not equalize the concentration change at the solidification front quickly. Because the concentration of impurities is higher at the solidification front, a larger number of impurity atoms is incorporated into the crystal than would be expected from the concentration in the bulk melt outside the diffusion-controlled layer. This results in a higher degree of impurity incorporation and an effective segregation coefficient k_{eff} which is larger than the equilibrium value, k_0 . Burton, Prim and Schlichter (BPS) [31] extended the plain rotating disc treatment [32] for the diffusion boundary layer for crystal growth and showed that the degree of incorporation, or the effective segregation coefficient of an impurity, is related to the diffusion boundary layer thickness, δ , and growth rate f as

$$k_{\text{eff}} = \frac{k_0}{k_0 + (1 - k_0)\exp(-\delta f/D)} \quad (4)$$

where D and k_0 are the diffusion coefficient and equilibrium segregation coefficient of the impurity, respectively. The thickness of the diffusion boundary layer δ depends on the diffusivity of the impurity, kinematic viscosity ν of the melt and crystal rotation rate ω as,

$$\delta = 1.6 D^{1/3} \nu^{1/6} \omega^{-1/2} \quad (5)$$

From expressions (4) and (5), it is seen that the instan-

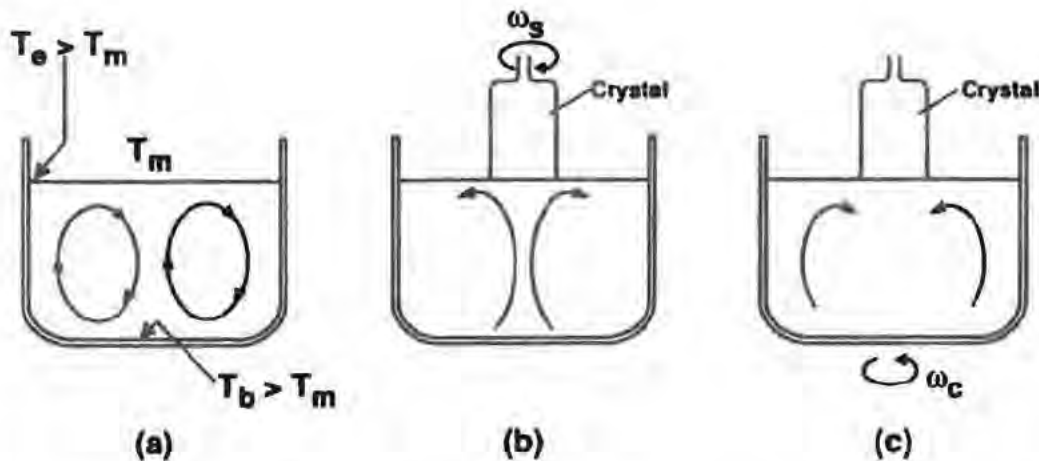


Figure 7 Convection patterns in a Czochralski melt due to (a) thermal convection; (b) crystal rotation; and (c) crucible rotation. (From Ref. 143.)

taneous incorporation rate is microscopic growth rate-controlled. The growth rate fluctuations are the source of microscopic inhomogeneity in the crystal. On the other hand, at any given interface, the uniformity of the boundary layer thickness across the interface controls radial uniformity. The CZ crystal's radial and microscopic impurity uniformity will be discussed later in terms of the BPS equation.

b. Convection Flows in Czochralski Melt. The major convective fluid flows in the CZ melt that impact the growth are thermal convection flows due to the existence of a non-vertical temperature gradient, and forced convection induced by crystal and crucible rotation as shown in Figure 7 (other convection flows are caused by crystal pulling and surface tension). The basic thermal convection flow generated in a melt can be symmetrical or asymmetrical, with the hot melt rising along the crucible wall and descending at the crucible center as is shown in Figure 7(a). The basic flow pattern is determined by the crucible geometry, aspect ratio (height to diameter ratio of the melt), and thermal boundary conditions. The driving force is given by the dimensionless Grashof number N_{Gr} :

$$N_{Gr} = g\alpha\Delta T R^3 / \nu^2 \quad (6)$$

where g is the acceleration due to gravity, α is the melt thermal expansion coefficient, ΔT is the temperature difference across the crucible diameter R and ν the kinematic viscosity of the melt. From this expression, it is clear that as the crystal grower is scaled up in

charge size (so is the crucible diameter), a stronger thermal convection is generated due to the direct contribution of the third power of R and increasing temperature gradient in the melt. Melt turbulence associated with strong thermal convection cause temperature fluctuations in the melt and contribute to microinhomogeneity in dopant and oxygen incorporation.

It is a common practice in CZ growth to use crystal rotation to override the deleterious effects of thermal convection discussed above. The effects of crystal rotation are two-fold. Similar to a rotation disc, the crystal rotation induces a uniform hydrodynamic boundary layer across the interface. Burton et al. [31] extended the plain rotating disc treatment for the diffusion boundary layer for crystal growth, Eq. (5). Secondly, the rotating crystal draws a uniform flow from the central region of the melt, perpendicular to the interface over the radius and spins it outward radially near the surface, Figure 7(b). As a result, the convection flow by the crystal rotation has the effect to counter and reduce the thermal convection flow and the convection flow induced by the crucible rotation (has same general flow pattern as thermal convection, see Fig. 7(c)). The magnitude of the flow induced by the crystal rotation is characterized by the dimensionless Reynolds number N_{Re} :

$$N_{Re} = \omega r^2 / \nu \quad (7)$$

where ω is the crystal rotation rate and r is the crystal radius.

While forced convection, i.e. the crystal rotation, has the effect of overriding the harmful thermal convection, the net effect depends on the relative magnitude of the two components. The relative effect of the two components may be expressed by the ratio, N_{Re}^2/N_{Gr} . If $N_{Re}^2 > N_{Gr}$, the crystal rotation will effectively isolate the segregation process at the growth interface from the thermal convection in the melt [33]. Therefore, small melt and high crystal rotation would suppress the effect of thermal convection.

c. *Macroscopic Radial Impurity Uniformity.*

In the silicon growth from a homogeneous melt, the radial uniformity is controlled by the uniformity of boundary layer thickness across the interface. In Eq. (3), if the growth rate is assumed to be uniform across the interface, then the radial uniformity of the impurity is determined by the variation in boundary layer thickness. It may be shown [34], in the case of dopant in silicon, that the rate of change in k_{eff} with respect to the variation in diffusion boundary layer thickness is very sensitive in the range of layer thickness encountered in the silicon CZ growth. The effect is greater for *n*-type than for the *p*-type dopant in silicon. The relevance of the melt convection condition to the radial impurity incorporation is the following. In the absence of thermal convection, the result of the crystal rotation would be a uniform diffusion boundary layer over the crystal radius at the interface. Hence, if the crystal rotation is the only source of convection, no radial segregation will result from the fluid flow effect and impurity incorporation is uniform across the crystal radius. In real crystal growth, however, the thermal convection flows form a general pattern in the crucible as rising streamlines along the crucible wall which fall in the center following a gradually curved path (see Fig. 7a). This path results in a stagnation point near the center of the crystal interface. Therefore, when thermal convection is strong compared to forced convection, the diffusion boundary layer thickness at the outer region of the interface may be reduced by the thermal convection velocity while the effect is small in the region near the center of the interface. Thus thermal convection flow causes a radial variation in boundary layer thickness. If the segregation coefficient of the dopant involved, k_0 , is smaller than unity, one finds a significant radial variation in impurity incorporation; it is high in the center and low in the outer region of the crystal. The greater the k value deviates from unity, the greater the radial variations. By the same principle, increased crucible rotation can cause variations in the

boundary layer thickness and radial gradient in incorporation. As discussed above, harmful thermal convection effects can be suppressed by increased crystal rotation and by small melt growth. Lin and coworkers [17,23] have demonstrated such effects by using a double crucible arrangement (see Fig. 6(a)). The use of a smaller diameter and low aspect ratio inner crucible reduced the effect of thermal convection. The improvements on radial dopant uniformity and random dopant concentration fluctuations, characteristic of the thermal convection, were observed for As, P, Sb and oxygen for which the segregation coefficients deviated significantly from unity.

d. *Microscopic Inhomogeneity.* In general, the microscopic inhomogeneity of impurity in CZ silicon crystals is a result of growth-rate fluctuations and impurity segregation during crystal growth. The growth-rate fluctuations cause variations in the impurity incorporation levels. The lattice strain associated with local impurity concentration variations give rise to the so-called "striations," which are revealed by chemical etching or x-ray topography. Severe microscopic dopant inhomogeneity corresponds to a large variation in carrier concentration and is not desirable in silicon materials used for device fabrication, especially when such variation is comparable to the device feature size. This is an important consideration in VLSI/ULSI fabrication. Large oxygen striations can result in preferential precipitation, often observed as concentric ring patterns in etched wafers following thermal processing. In CZ silicon growth there are several sources of microscopic growth rate variations which are discussed below.

Noncentrosymmetric Thermal Distribution in the Silicon Melt. In large-melt silicon growth, finite thermal asymmetry exists about the center of the melt. During crystal growth, as the crystal is rotated about the growth axis, the interface experiences slightly different temperatures at different positions in the melt. Therefore, the growth rate of a given crystal element parallel to the crystal axis fluctuates periodically, as illustrated schematically in Figure 8. In general, the fluctuation is most pronounced in the crystal elements furthest from the crystal center. The periodicity of the fluctuation is determined by the average growth rate, f , and crystal rotation rate ω , as f/ω . The variations in the impurity incorporation level that correspond to the growth-rate variations are commonly referred to as "rotational striations". When the equilibrium segregation coefficient (k_0) of the element

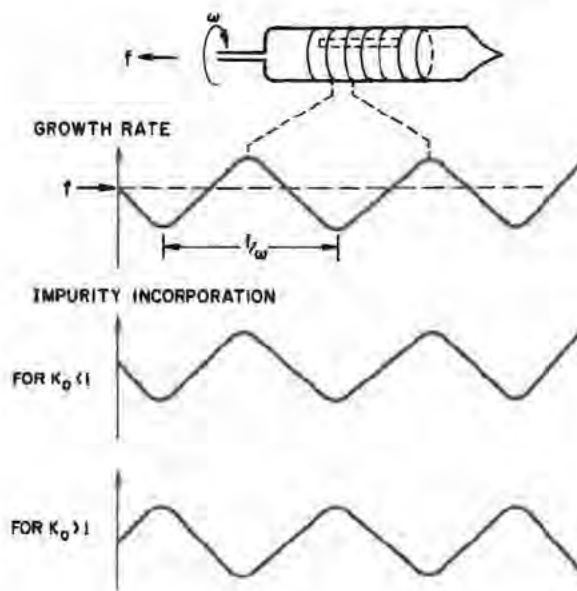


Figure 8 Schematic illustration of growth-rate fluctuation and its relationship with microscopic Impurity fluctuations in CZ crystal. Here, f and ω are growth rate and crystal rotation rate, respectively. (From Ref. 53.)

involved is less than unity, the fluctuation in impurity incorporation level is in phase with the growth rate fluctuation. If $k_0 > 1$, the fluctuations will be out of phase (see Fig. 8). The relationship may be realized readily by examining the Eq. (4).

Thermal Convection-Related Temperature Fluctuations. Growth rate fluctuations caused by thermal convection related temperature variations are mostly random in nature, and etched striations are characteristically aperiodic. When thermal convection is significant, the microstriations bear the signature of high-frequency fluctuations on the order of tens of hertz.

Automatic Diameter Control-Induced Perturbation. Growth-rate fluctuation can be further perturbed by the automatic diameter control mechanism (ADC) commonly employed in silicon crystal growth. The crystal pull-rate is slaved by optically monitored crystal diameter variations in order to maintain a preset diameter. The pull-rate adjustments are both "instantaneous" (a few seconds) and "long term" (minutes). The long term pull-rate adjustment determines the average growth rate. The instantaneous pull-rate adjustment imposes modifications on the

microscopic growth-rate fluctuations resulting from thermal asymmetry and thermal convection. The net effect is to smear the periodic nature of the impurity fluctuation resulting from the melt thermal asymmetry.

4. Oxygen Incorporation and Segregation in Czochralski Silicon Growth

a. *Incorporation Mechanism.* Unlike most intended dopants in silicon CZ crystal growth, which show "normal freezing" behavior under normal growth conditions, oxygen is an unintended dopant that enters the silicon melt continuously by dissolving the silica crucible. The incorporation behavior of oxygen into silicon is the result of complex interplay among crucible dissolution, surface evaporation, thermal convection and forced convection, as shown in the Figure 9. In a side-heated CZ hot zone, the dissolution of the silica crucible is the highest at the side wall of the crucible. The silicon melt dissolves SiO_2 and absorbs its oxygen. The oxygen-rich silicon melt would rise along the crucible wall, following the thermal convection flow pattern to near the melt surface, and then to the melt center where it is drawn toward the crystal for incorporation by the forced convection induced by the crystal rotation. When the oxygen-rich melt is near the surface, a great portion of the oxygen is evaporated through the free surface. The oxygen concentration incorporated into the growing crystal, therefore, is proportional to the oxygen concentration in the melt adjacent to the growing crystal. During steady-state growth, there exists a dynamic equilibrium of oxygen between the four controlling factors in the system. Due to the difference in thermal characteristics of different hot-zone designs, the oxygen incorporation behavior varies from one grower design to another. The major oxygen-controlling factors are discussed in the following.

Effect of Surface Evaporation and Crucible Dissolution. In the absence of thermal and forced convection (a hypothetical case), the melt oxygen concentration is proportional to the ratio of melt-crucible contact area to the available free surface area. In such a case the transport of oxygen would depend entirely on diffusion. This ratio constantly decreases as the aspect ratio is reduced during the growth. The variation of this ratio is the basic characteristic of the axial oxygen profile of CZ silicon, in which the concentration is observed to gradually decrease from the seed end toward the tang end (for

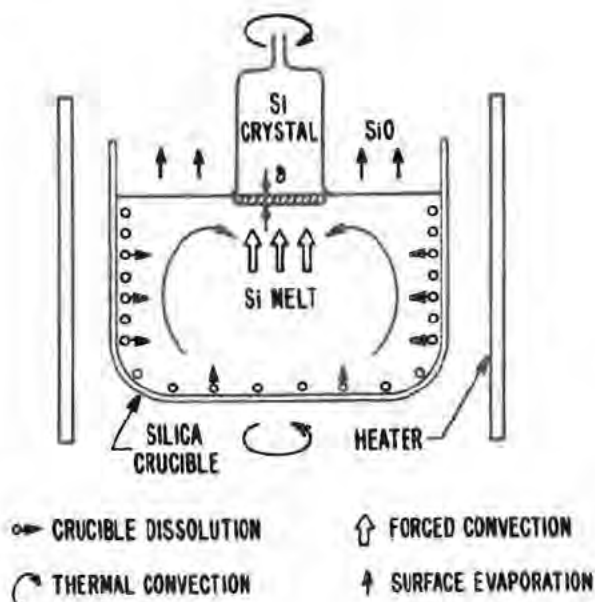


Figure 9 Schematic of a silicon Czochralski growth system showing relationship among oxygen-controlling factors. (From Ref. 23.)

example, see Fig. 15). However, the dependence of concentration on this geometric ratio is influenced by the crucible dissolution rate and ambient pressure. The dissolution rate of the silica is material density and temperature dependent. Therefore, using crucible with an inner wall made of "porous silica," for example, would enhance the dissolution rate. Increasing the melt-crucible contact area by using corrugated inner surface will obviously serve similar purpose. Mathematical modeling of the observed oxygen incorporation behavior based on dissolution and evaporation, as carried out by Carlberg et al. [35], is merely a first-order approximation. In actual silicon growth, oxygen incorporation and uniformity are greatly affected by thermal convection and forced convection. No modeling effort thus far accurately takes these factors into account.

A study of oxygen evaporation from the melt surface was made using "shoulder" growth of a 300 mm diameter crystal from a 350 mm diameter crucible. In this experiment, the effect of the free melt surface evaporation on the oxygen level during crystal crown growth was examined. Figure 10 plots oxygen concentration variation in the grown silicon as the melt surface is covered by the growing "shoulder". The relationship between oxygen concentration and available surface is not linear. When the crystal shoulder

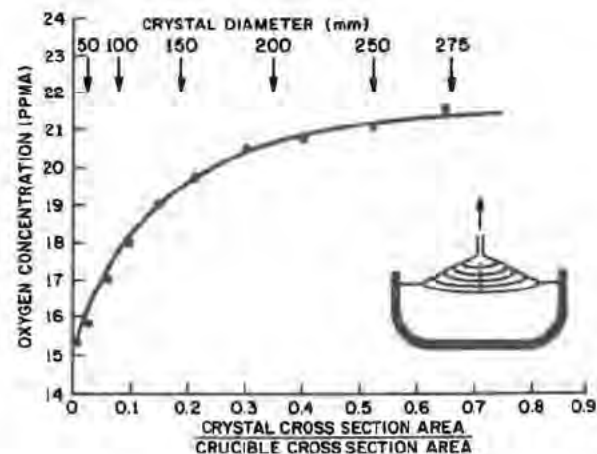


Figure 10 Oxygen concentration measured as a function of fraction of melt surface being covered by the growing crystal during crown growth. The crystal crown accounts for less than 10% of the initial charge. (From Ref. 18.)

diameter is small (<125 mm), the oxygen evaporation (and therefore the oxygen concentration of the growing crystal) is very sensitive to the diameter change. When the majority of the surface is covered with the crystal, the evaporation seems to remain nearly constant. By extrapolating the curve in Figure 10, the oxygen concentration corresponding to a very small and to a maximum size of crystal (when the melt is fully covered) may be obtained. The maximum oxygen evaporation accounts for about 30% of the available dissolved oxygen. This value is much lower than generally conceived, that over 90% of the dissolved oxygen from crucible is evaporated from the melt surface [36]. More discussion of the oxygen incorporation behavior on the 300 mm diameter crystal growth will be made in a later section.

Lin and Hill [17] studied the effect of ambient pressure on the oxygen distribution in the melt and grown crystal via crystal growth experiments. Based on the experimental evidence, physical models of oxygen distributions in large silicon melts were proposed and are shown schematically in Figure 11. It is shown that thermal convection is the main oxygen transport mechanism when the melt aspect ratio is high in a large melt growth. The oxygen-rich flow conforms with the suggested thermal convection pattern shown in Figure 7(a). Experimental results also showed that under atmospheric pressure, the oxygen distribution is not uniform near the melt center, where a stagnant region of low oxygen concentration exists. The nature of this nonuniformity is displayed in crystals' radial oxygen

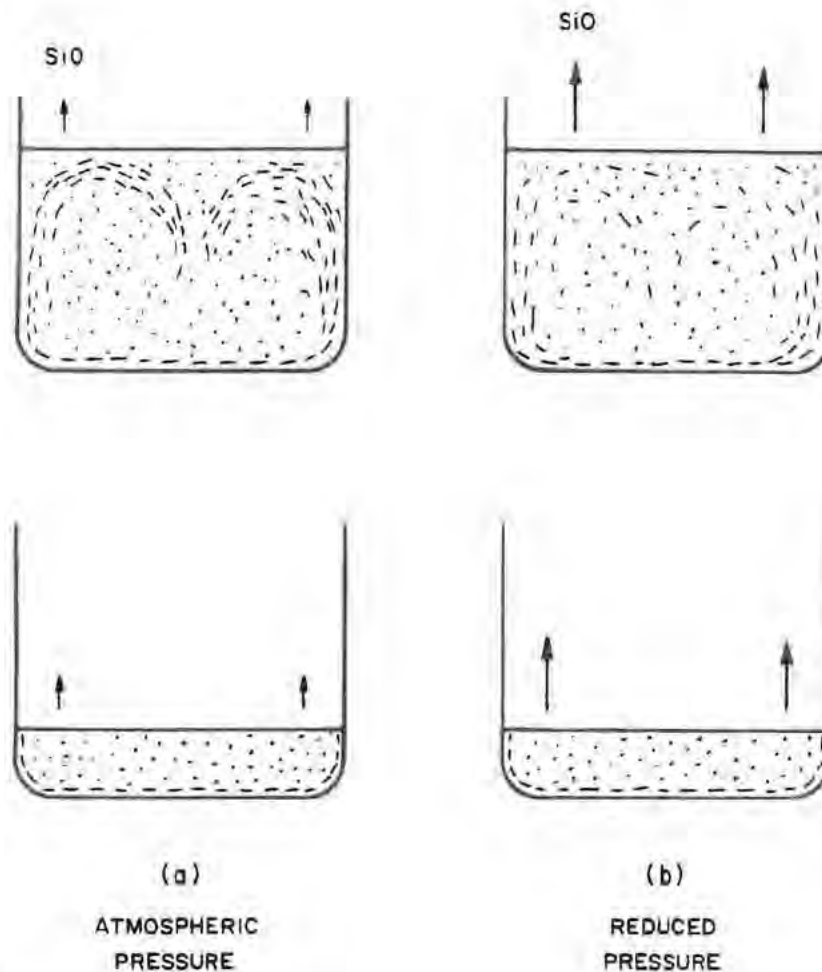


Figure 11 Schematic representations of oxygen distribution in silicon melt at high and low melt level configurations. The dots and lines represent oxygen concentration. (a) At reduced pressure, (b) At atmospheric pressure. (From Ref. 17.)

profiles near the seed end, Figure 12(a). However, as the crystal growth progresses, the forced convection due to crystal rotation modulates the oxygen distribution and results in local mixing, and the gross nonuniformity near the stagnant region is largely diminished. On the other hand, under the reduced pressure, Figure 12(b), the oxygen distribution in the melt is more uniform near the surface of the melt. The grown crystal possesses better radial oxygen uniformity. When thermal convection is not significant, as in the case of a low aspect ratio configuration, the melt oxygen is both diffusion rate- and crucible dissolution rate-dependent. The melt tends to be uniform in oxygen. Both enhanced forced convection and ambient pressure have little effect on the oxygen uniformity.

Effect of Crystal and Crucible Rotations. For a given system, i.e., fixed starting melt geometry and hot zone thermal distribution, etc., the parameters that can significantly alter the oxygen incorporation are crucible and crystal rotations and growth rate variations. The effect of crystal/crucible rotation on the fluid flow patterns were studied in the past by simulation using fluid of similar viscosity as that of silicon melt at room temperature [37]. Figure 13 shows the fluid flow patterns due to various combination of crystal and crucible rotations. In the real crystal growth, however, the flow patterns can be significantly altered by the presence of thermal convection. The results of the simulations provide very useful information on the effect of rotational parameters. Kakimoto et al. [38,39] observed thermal and forced

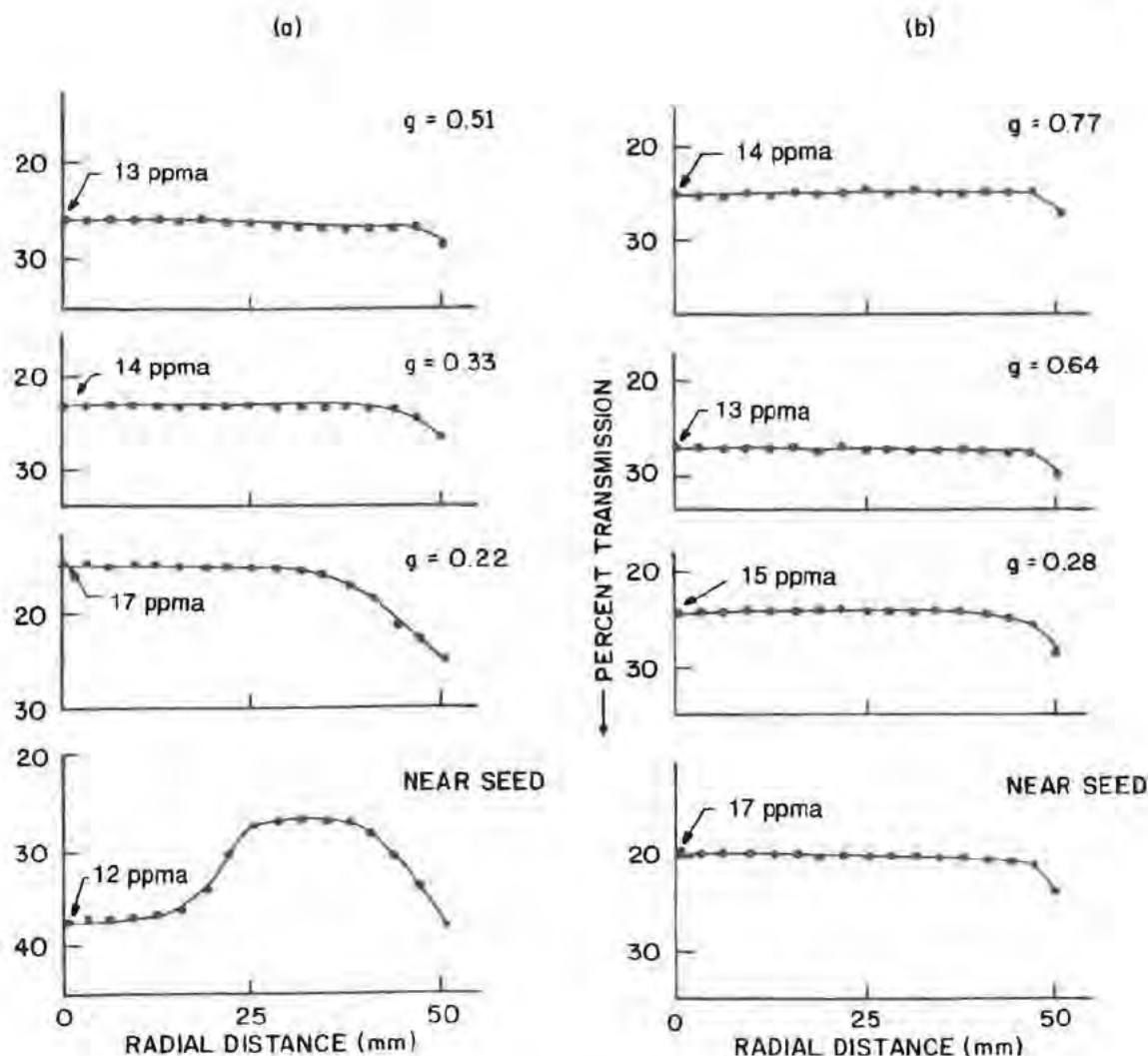


Figure 12 Radial profiles of $9\ \mu\text{m}$ IR transmission at various stages: g =fraction solidified, (a) At atmosphere, (b) At reduced pressure (18 torr). Oxygen concentration is computed in accordance with ASTM F121-80. (From Ref. 17.)

convection flows of silicon melt directly during Czochralski growth using x-ray radiography with solid tracers, for various crystal and crucible rotation speeds. The effect of non-axial symmetrical temperature distributions on the thermal convection flows was clearly observed. The suppression of thermal convection by crystal rotation-induced forced convection was also evidenced. One way to gain information on the flow properties of a growing system is to analyze grown crystals following parametric growing experiments. One finds that forced convection is effective in controlled oxygen incorporation.

As discussed previously, crystal rotation rate determines the magnitude of the upward melt flow. This

flow can serve as oxygen transport from crucible bottom to the growing interface. The net effect on the overall flow pattern and oxygen incorporation depends on its magnitude and rotational direction relative to the crucible rotation. Figure 14 shows an "uncommon" oxygen profile of silicon grown under high crystal rotation (30 rpm) with crucible in iso-rotation mode (2 rpm). At about 30% of melt solidified, the oxygen incorporation underwent a mode change and sharply increases to a very high concentration level (~ 25 ppma). This behavior indicates that as the melt aspect ratio is reduced during the crystal growth, at some transition point, the strong forced convection takes over as the dominant transport mech-

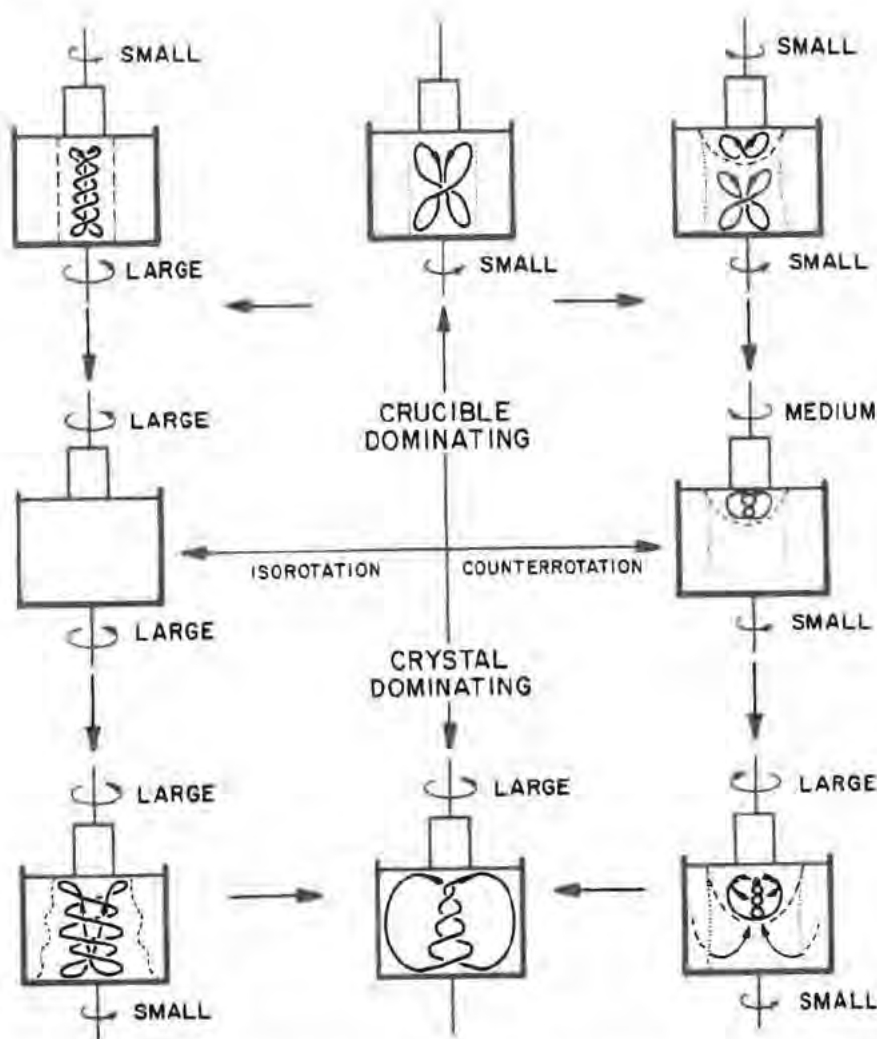


Figure 13 The variation of Czochralski flow patterns with relative directions and magnitudes of crystal and crucible rotations. (From Ref. 37.)

anism which draws oxygen-rich melt from the crucible bottom to the growing interface.

Crucible rotation develops radial pressure gradients which enhance the thermal convection flow arising from non-vertical temperature gradient as shown in Figure 7(c). Therefore, fast crucible rotation helps the transport of oxygen from near the crucible wall to the growing crystal and enhances incorporation. Figure 15 shows the effect of crucible rotation on the incorporation level. Fast melt flow also results in a thinner melt-crucible boundary diffusion layer, a condition that will enhance crucible dissolution. Figure 16 shows several axial oxygen concentration profiles of silicon grown with several combinations of crystal/crucible rotation rates, under both counter-

and iso-rotation conditions in the same grower and a reduced pressure. These results show that the forced convection induced by crystal/crucible rotations has very significant effects on the melt flow pattern, even in the presence of thermal convection. The bulk of the incorporation behavior is consistent with, and can be interpreted from, the simulated flow patterns (see Fig. 13).

Incorporation in p^+ and n^+ Silicon Crystal Growth. Degenerately doped n - and p -type silicon, in the concentration range of 10^{18} – 10^{19} atoms/cm³, are common substrate materials for n/n^+ and p/p^+ epitaxial structures for CMOS ICs. Unlike the lightly doped silicon, oxygen precipitation behavior in

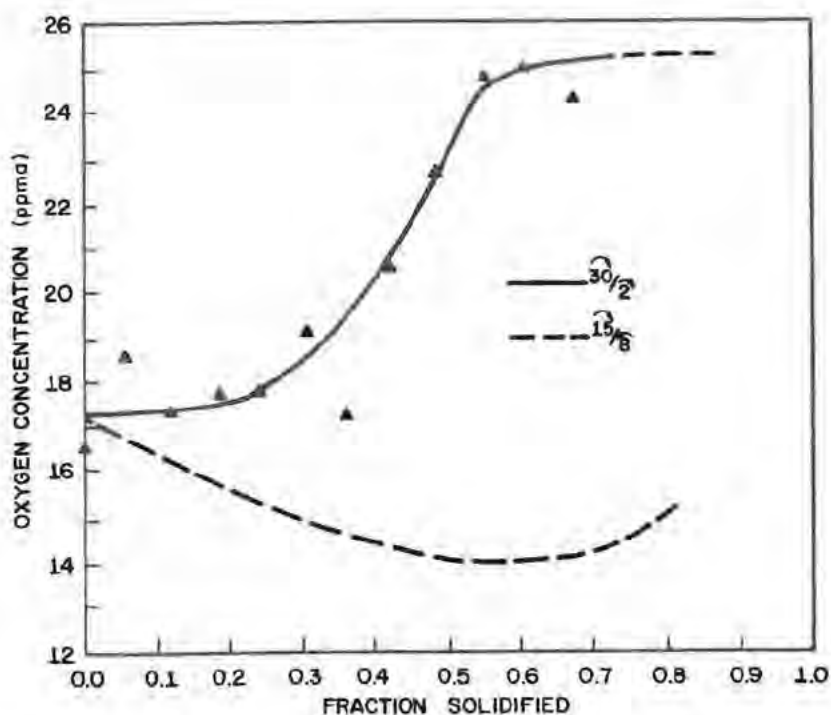


Figure 14 Axial oxygen profile of silicon grown with crystal rotation of 30 rpm and crucible rotation of 2 rpm (in iso-rotation). The dashed line represents profiles due to normal growth.

degenerately doped silicon is drastically different depending on the conductivity type [41]. In this resistivity range (0.005–0.02 ohm-cm), oxygen precipitation is retarded in Sb-doped silicon while the kinetics are at their peak for p -type, boron doped silicon. The possible sources of differences in precipitation kinetics in p^+ and n^+ were investigated. Oxygen diffusion mechanism was found not to be affected by the presence of heavy Sb or light boron [42]. The nucleation mechanisms for oxygen precipitates have been thought to be different in p^+ and n^+ . Experimentally, the oxygen incorporation in n^+ and p^+ have been found to be different from the lightly doped silicon [43].

Figure 17 shows the axial oxygen distribution in 100 mm diameter p^+ (0.005–0.01 ohm-cm) and n^+ (0.02–0.08 ohm-cm) crystals as measured by SIMS, compared to the distribution band of p^- (8–20 ohm-cm) grown with the same conditions. It is seen that on the average, the p^+ crystals exhibit about 25% higher incorporation rate than n^+ crystals (with p^+ contents higher than p^- , while n^+ are lower). Other studies [44,45] also show the dependency of oxygen incorporation on doping level, but to different degrees. In considering the oxygen incorporation mechanism, it would not be a surprise to find that the dependency

obtained would vary somewhat depending on the melt size, melt aspect ratio, etc. used in the crystal growth experiments. Several possible mechanisms behind the dependency of oxygen incorporation on the dopant concentration have been suggested [46–48]. Some data indicate that the reduced oxygen incorporation into heavily Sb-doped silicon is due to Sb_2O_3 evaporation from the melt, thus reducing oxygen concentration in the melt [46]. Others explain the lower oxygen incorporation observed in heavily Sb-doped silicon as due to accelerated SiO evaporation from the melt caused by simultaneous evaporation of elemental antimony [48]. In the case of p^+ crystal growth, the enhanced oxygen incorporation is speculated as due to enhanced crucible dissolution by heavily boron doped silicon melt. It is pointed out here that the difference in oxygen incorporation level can not account for the difference observed in precipitation kinetics in p^+ and n^+ . The difference in the nucleation mechanism probably plays a significant role.

b. *Oxygen Segregation and Microscopic Inhomogeneity.* Solute segregation during the solidification of a binary system is determined by the nature of its phase diagram near the solvent's melting

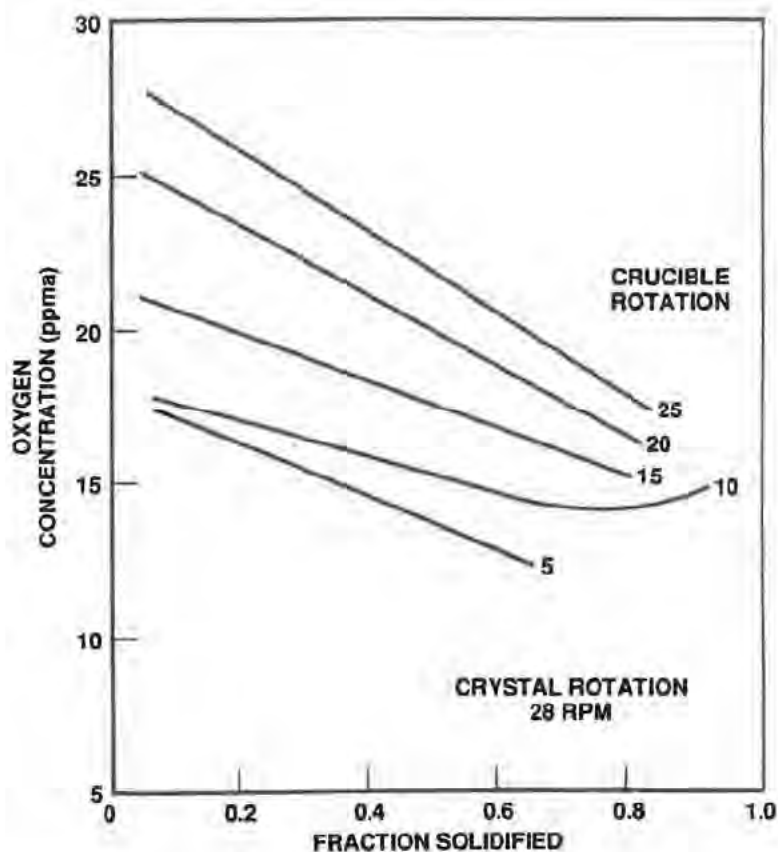


Figure 15 Oxygen profiles at various crucible rotation rates, with crystal rotation rate held at 28 rpm. (From Ref. 40.)

temperature. The equilibrium segregation coefficient of the solute is a physical constant and is related to the slopes of the liquidus and solidus immediately adjacent to the melting temperature, above the primary phase of the equilibrium phase diagram as is shown in Figure 18. The equilibrium segregation coefficient, k_0 can be smaller or greater than 1 and can be deduced readily when the equilibrium phase diagram near the primary phase is established. In practice, when the solidification is not under equilibrium condition, the liquidus and solidus will shift in positions and segregation coefficient will deviate from k_0 . Solute segregation phenomenon can be demonstrated by a controlled directional solidification of a binary alloy, in which the solute concentration along the direction of solidification will follow Eq. (1). If the solution is in good mixing condition and solidification rate is small, the k value can approach k_0 .

In the growth of CZ silicon, the dopant segregation behavior is similar to the solute in the directional solidification of a binary alloy, the dopant distribution

along the grown crystal will follow Eq. (1). If the dopant is non volatile, such as boron or phosphorus, and melt is in complete mixing, the k value approaches the equilibrium value. However, in the case of oxygen, the incorporation behavior is quite different from the dopant element. The crucible dissolution rate, the oxygen transport mechanisms (thermal and forced convection) used and surface evaporation rate determine the melt oxygen concentration near the growing interface for incorporation [23]. Therefore, the oxygen in the silicon melt during CZ growth is a dynamic system. Depending on the growth parameters employed, the oxygen concentration and its profile along the grown crystal can be drastically different from those expected from a "normal freezing" behavior of the dopant element. Figure 16 shows oxygen concentration profiles from several CZ crystals grown using different parameters but with the same grower and setup. From these profiles, it appears that there is no common "segregation" behavior for oxygen displayed by these CZ silicon crystals. In fact, these

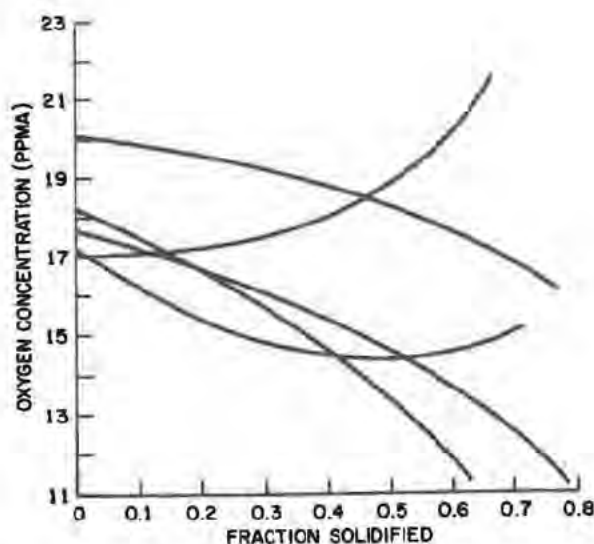


Figure 16 Axial oxygen profiles of silicon crystal grown with several combinations of crystal and crucible rotation rates.

axial oxygen distributions are not the results of oxygen segregation during silicon solidification. One can certainly fit the power function of Eq. (1) to any of the profiles in Figure 16 and obtain a “ k ” value. But the k value so obtained does not describe the segregation behavior of oxygen during silicon freezing, but merely represent the characteristics of the oxygen concentration change in the melt near the growing interface in a particular growing process. Therefore, it is inappropriate and incorrect to assign the “ k ” value so obtained as a “segregation coefficient” of oxygen. More importantly, it must be emphasized that the k value so obtained has absolutely no relationship with the equilibrium segregation coefficient of oxygen, which is a physical constant.

Although oxygen segregation is not visualized readily at the macro level, it is realized at the micro level at the growing interface in CZ silicon growth. In general, the degree of impurity incorporation (i.e., the effective segregation coefficient) at the growing interface is determined by the crystal growth rate f , at the interface, the boundary layer thickness δ (a function of crystal rotation) and equilibrium segregation coefficient k_0 , as may be described by the Burton, Prim, Slichter (BPS) expression, Eq. (2). In the BPS expression, the k_0 and diffusion coefficient D are material constants, and f and δ are crystal growth parameters. If the crystal and crucible rotations are maintained constant, then the only parameter can

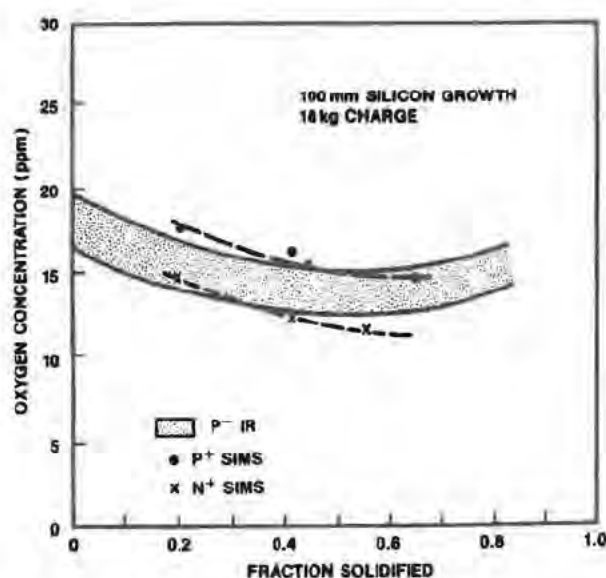


Figure 17 A comparison of oxygen incorporation levels of lightly doped p and heavily doped p and n (p^+ and n^+) silicon crystals grown under identical conditions. (From Ref. 43.)

SOLUTE SEGREGATION

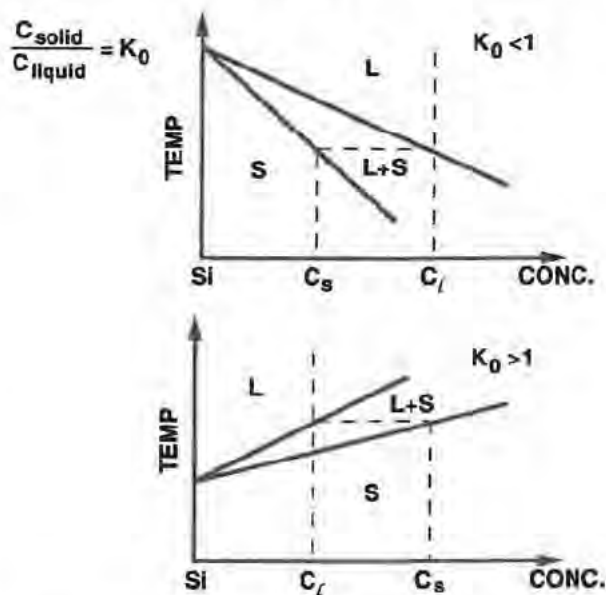


Figure 18 Schematic showing relationship between k_0 of solute and slopes of liquidus and solidus in a binary system. (From Ref. 56.)

cause variation in oxygen incorporation rate is the growth rate. An analysis of the Eq. (2) shows that the conditions listed in Table 1 are true. It is clear from the table that the impurity incorporation rate can fluctuate with the changing growth rate, unless the equilibrium segregation coefficient k_0 is unity. However, $k_0=1$ is not consistent with the phase rule [49]. Further more, it is also realized that the change in k_{eff} is greater when k_0 is further deviated from unity. In large diameter CZ silicon crystals, non-uniform oxygen incorporation in the form of so called oxygen striations are usually observed. The striations are results of impurity segregation due to fluctuations in the microscopic growth rate. The existence of oxygen striations in CZ silicon is evidence that **oxygen in silicon does segregate** and that k_0 for oxygen is not unity.

Equilibrium Segregation Coefficient, k_0 , of Oxygen. The k_0 value of oxygen defines the basic segregation characteristics, and therefore the effective incorporation rate during the silicon growth. The k_0 has been of interest to researchers in order to understand the microscopic oxygen incorporation and resulting precipitation characteristics in silicon. However, the details of the phase equilibrium of the Si—O system for the Si-rich alloys have not been extensively studied. Many investigations for the k_0 value of oxygen have only been carried out in the last three decades. The efforts can be divided into two categories. The first is a direct method, by oxygen concentration analysis on quenched oxygen-silicon alloys, as is commonly done in phase diagram studies. The second approach is to deduce the k_0 value from the silicon crystal growth experiments. One major factor affecting the k_0 determination is the accuracy of the oxygen concentration analysis. In this regard, infrared absorption using single crystal is more accurate and less uncertain than oxygen analyses on quenched samples using other methods such as differential thermal analysis. Due to the variety of methods used and accuracy of the oxygen concentration determination, the k_0 values reported over the years certainly do not show a great consensus. A range of k_0 values have been reported by various authors [27, 50–55], ranging from greater to less than unity and including unity.

Among the various k_0 studies, the use of crystal growth experiments and analysis via the BPS relation has been considered a very accurate and repeatable approach. Lin and Hill [52] first applied the approach by growing a small diameter (14 cm) crystal in a large

Table 1 Directions of incorporation rate change in response to crystal growth rate changes for $k_0 < 1$ and $k_0 > 1$. There is no response in incorporation rate with growth rate change when $k_0 = 1$.

Equilibrium segregation coeff k_0	Crystal growth rate f	Impurity incorporation rate k_{eff}
>1	$\downarrow$	$\uparrow$
>1	$\uparrow$	$\downarrow$
<1	$\downarrow$	$\downarrow$
<1	$\uparrow$	$\uparrow$
$=1$		$k_{\text{eff}} = k_0$

system in a controlled experiment. The oxygen incorporation level was observed to change with a change in crystal growth rate and it shows that oxygen does segregate during silicon solidification. From such an experiment, an equilibrium segregation coefficient of ~ 0.25 was deduced. Similarly, Lin and Stavola [53] studied the origin of microscopic oxygen inhomogeneity and its effect on oxygen precipitation using large-spacing oxygen striations prepared by a manually controlled crystal growth. The periodic nature of the oxygen profile shown in Figure 19 is a result of growth rate fluctuations and oxygen segregation. With $k_0 < 1$, the oxygen fluctuations and growth rate fluctuations are “in phase” (i.e. the maxima and minima of the oxygen fluctuations coincide with the microscopic growth rate fluctuations) see Table 1. The growth rate fluctuations are due to asymmetrical temperature distribution in a large silicon melt. These results again show that oxygen segregates significantly which corresponds to a nonunity equilibrium segregation coefficient. The phase analysis [53] showed that $k_0 < 1$ for oxygen and that oxygen behaves similarly to arsenic in silicon (i.e. $k_0 \sim 0.3$). More recently, Iino et al. [55] used a similar approach to study the k_0 of oxygen by analyzing oxygen striations in comparison with that due to phosphorus. They obtained k_0 values between 0.13 and 0.37 (averaged to 0.21). The range of values obtained are in good agreement with the values obtained by Lin et al. [52,53].

Microscopic Inhomogeneity and Oxygen Precipitation. Oxygen segregation produces inhomogeneity when there is a perturbation in the growth rate. The thermal treatment experiments of silicon containing microfluctuations in oxygen concentration show that the precipitation is not uniform. Figure 19 bottom is a micrograph after the sample was heat treated at

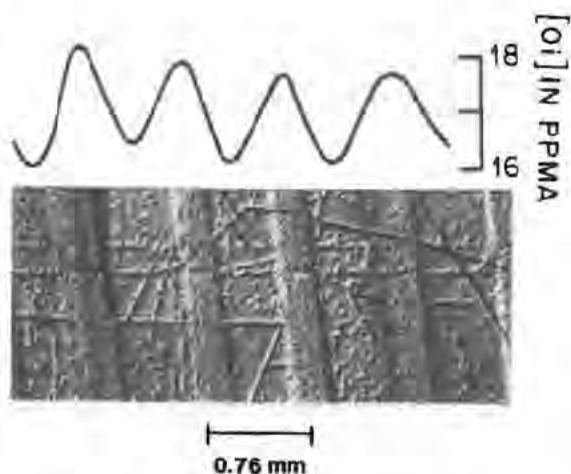


Figure 19 Top: IR 9 μm profile parallel to crystal axis showing periodic oxygen fluctuations. Bottom: Micrograph of etched silicon after heat treatment showing precipitation bands corresponding to high oxygen regions of the fluctuations (top). (From Ref. 56.)

1050°C for 5 h following chemical etching. It shows heavy precipitate bands corresponding to high concentration regions of oxygen in the fluctuations. The precipitation density in the low oxygen region appears to be insignificant. The difference in the precipitation densities in the high and low oxygen regions, however, cannot be accounted for by the difference in their [O], $\sim 9\%$ (concentration fluctuation is $\sim 4.5\%$ about the mean). Furthermore, the fact that the precipitation occurs at the sample surface suggests that no denudation takes place. Apparently, the oxygen outdiffusion near the sample surface is suppressed by a fast nucleation/growth mechanism in the high oxygen band regions while the precipitation kinetics at the low oxygen regions seem retarded. These preferential precipitation bands correspond to concentric ring patterns often observed in the oxidized or heat treated wafers following chemical etching. An example is shown in Figure 20.

The oxygen precipitation kinetics in CZ silicon with microfluctuations is not strictly proportional to oxygen concentration. It is likely that the preferential precipitation of oxygen in the high [O] regions reflects the large number of nuclei available in the same regions. It is reasonable to postulate that the mechanism for inhomogeneous precipitation behavior involves the preferred nucleation of the precipitates at microdefect centers introduced during crystal growth. Such defects, ranging from several hundred angstroms to tenths of a



Figure 20 X-ray topography of heat treated CZ wafer showing concentric oxygen precipitation bands at high oxygen regions of the concentration fluctuations. (From Ref. 57.)

micron in size, have been related to temperature fluctuations and remelting phenomenon at the growing interface.

The grown-in microdefects in CZ silicon have been extensively studied in recent years. Basically, as in the FZ silicon, two types of microdefects may be formed during crystal growth [58]; D defects are vacancy agglomerates in nature and their formation and density are growth rate dependent. The D defects form when growth rate is above a critical value, below which the A-defects formation are favored. The A defects are clusters of silicon self-interstitials in the form of dislocation loops. In a crystal's "D defect region", where the vacancy concentration is excessive (greater than the equilibrium value), defects such as crystal originated pits (COP), flow pattern defects (FPD) and laser scattering tomography defect (LST) have been observed and they have been shown to cause degradation of MOS devices (mainly gate oxide integrity) [59]. Further discussion on grown-in microdefects and their relevance to crystal growth parameters will be made later in this chapter. Nakajima et al. [60] studied the distribution of as-grown D defects in the silicon crystal in relation to microscopic growth rate fluctuations on large striated silicon crystals. The study revealed that LST defects occur at the maxima of the growth rate fluctuations while FPD defects occur at the minima (see Fig. 21). This result means that the LST defects occur at the high oxygen concentration regions of the [O] fluctuations. The LST defects have been speculated as oxygen precipitates in nature (they can be annihilated by high temperature anneal in hydrogen) [61]. It is assumed

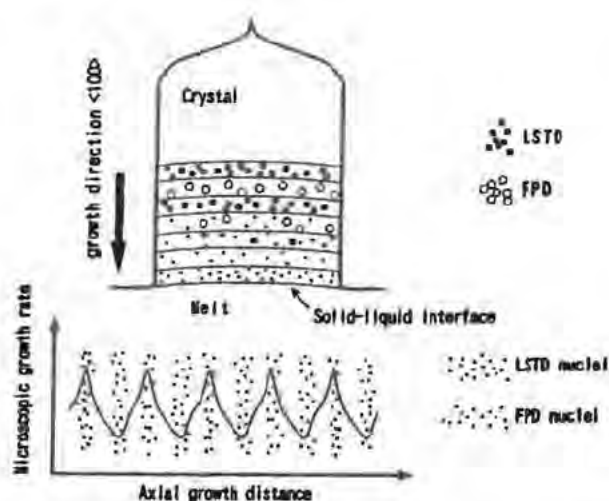


Figure 21 Schematic showing the occurrence of LST and FPD defects at maxima and minima of the growth rate fluctuations, respectively, of the CZ growth. (From Ref. 60.)

that its formation may be the result of either (a) nucleation of oxygen precipitates on vacancy clusters or (b) direct interaction of oxygen atoms with non-clustered point defects. The existence of LST defect centers (a current crystal as shown in Figure 19 was growth with a growth rate of 1.5 mm/min) suggests there are far more nuclei available in the high oxygen regions than in the low oxygen regions. When subjected to precipitation heat treatment(s), as the oxygen precipitation progresses in the bands of high nuclei density, self-interstitials are ejected and flood the neighboring low oxygen regions, where the precipitation has not started. The supersaturated self-interstitials would raise the nucleation barrier in the low oxygen regions of the fluctuations and retards its precipitation process [62].

In the current discussion, the occurrence of the microdefects in the high oxygen regions may be a major factor in the formation of observed preferential precipitation. It would be interesting and useful to conduct a similar experiment with a crystal grown with microfluctuations in oxygen but without D defects by using a low growth rate. Such an experiment would clarify the role of microdefects in the observed preferential oxygen precipitation.

c. Controlled Oxygen Silicon Crystal Growth

Normal Czochralski Growth. For ease of discussion, oxygen concentrations in silicon crystals for integrated circuit applications may be conveniently

classified into high, medium and low concentration ranges. If we designate 14–17 ppma (ASTM F121-80) as the medium range, the concentrations above and below this range are referred to as high and low concentrations, respectively.

From previous discussions, it is seen that forced convection is an effective tool for controlling oxygen incorporation. In order to achieve a desired oxygen level with axial uniformity in a silicon crystal, the following procedure may be carried out. Experimentally, for a given crystal growing system, one can establish oxygen incorporation profiles as a function of crystal/crucible rotation rates via studies such as shown in Figure 15. Using selected rotational parameters at different stages of crystal growth, one can develop and tailor the growth processes to grow crystals of desired oxygen concentration with substantial axial and radial uniformity. Figure 22 shows an example of using variable crucible rotation rates to change the oxygen incorporation levels during the growth, while the crystal rotation rate is maintained constant. It shows that the crucible ramping to a higher rotation rate effectively raises the oxygen level and changes the oxygen concentration profile. The incorporation level can be further enhanced when alternate ramping-up and -down of crucible rotation at medium and high rates are employed, as shown in the Figure 22. Presumably, the action causes local "disturbance" and thinning of the boundary layer between the crucible and the melt, thus increases crucible dissolution. The example in Figure 22 demonstrates the usefulness of forced convection in the enhancement or retardation of oxygen incorporation. With the proper use of forced convection, including the use of alternate ramping-up and -down of the crucible rotations, the increased uniformity in axial incorporation for high and medium ranges of oxygen can be achieved. Concentration profiles **a** and **b** of Figure 23 are oxygen profiles using variable crucible rotations for high and medium oxygen concentration levels.

In the crystal growing systems where the forced convection alone can not achieve the level/uniformity desired, additional sources of oxygen may be added by increasing the melt-crucible contact surface. Methods such as sand-blasting of the crucible surface [63] and the addition of an extra quartz rod/ring placed at strategic locations [64] have been used. Figure 24 shows a crucible design with its bottom surface fabricated in a corrugated configuration. It is shown that the additional contact sources uniformly increase the incorporation level, curve **b** of Figure 25, as may be compared with curve **c**, grown with a normal

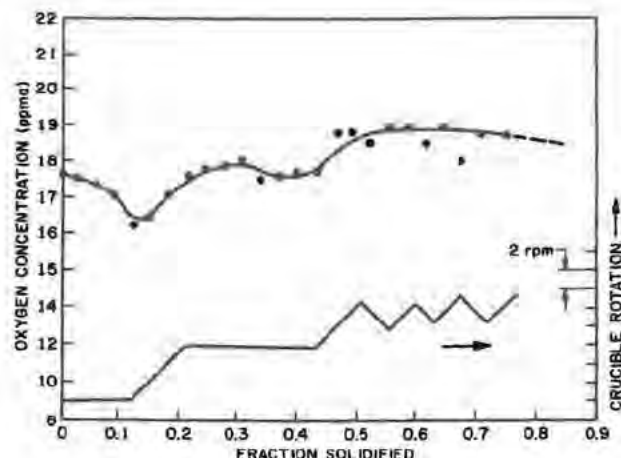


Figure 22 Axial oxygen profile of a silicon crystal showing the effect of crucible rotation rate on oxygen incorporation level. (From Ref. 18.)

crucible. Curve *a* shows an oxygen profile resulting from silicon growth with extra quartz material adhered to the crucible bottom surface as an added oxygen source under normal growth conditions. It is pointed out that profiles *a*, *b*, and *c* are obtained for a fixed set of crystal and crucible rotations. When variable forced convection parameters are applied, the concentration profiles may be tailored to improve axial uniformity as is shown in Figure 23. Curve *a* of Figure 23 is the result of using variable crucible rotation on crystal growth with additional quartz material adhered to the crucible bottom.

While thermal convection, crucible and crystal rotations all have effects on the oxygen incorporation level, these parameters also have great impact on the radial oxygen gradient. The relevance of these parameters to radial impurity uniformity has been discussed in Section 3 B.3.c. of this chapter. In order to achieve radial oxygen uniformity, the melt flows causing the radial non-uniformity in diffusion boundary layer thickness have to be suppressed. For example, when using a high crucible rotation rate to enhance oxygen incorporation, the radial oxygen uniformity is degraded unless a high crystal rotation in the opposite direction is used. As discussed earlier, the crucible rotation creates a fluid flow in the same general direction as the thermal convection (see Fig. 7). Such flow will cause the diffusion boundary layer to be thinner at the edge than at the center of the interface. Consequently, more oxygen is incorporated at the center than at the edge of the crystal. Increased crystal rotation suppresses the effect of crucible

rotation and thermal convection flows and results in a thinner diffusion boundary layer. Thickness variations in the thinner boundary layer would cause less radial gradient in oxygen incorporation. Faster crystal rotation also results in more mixing in the melt adjacent to the growing interface and tends to improve the melt concentration uniformity. It should be mentioned that there exists a drastic decrease in oxygen concentration in the CZ crystal's radial oxygen profiles near the crystal's periphery region. This is due to oxygen out-diffusion during crystal growth following solidification.

In large melt growth, the controllability for low level oxygen incorporation is more limited than that for the medium and high incorporation levels due to the domination of thermal convection function as the transport of oxygen-rich melt. This is enhanced for the growth of the crystal portion near the seed end. The curve *d* in Figure 25 represents a typical range of concentration profiles in the low oxygen range (11–14 ppma) that may be obtained with the experimental hot zone used. In this range, further uniformity of the profile can be obtained by increasing the incorporation level of the lower concentration portion of the profile using crucible ramping. However, suppressing the seed-end oxygen incorporation by forced convection is usually not an efficient process. It often results in degradation in the oxygen radial gradient and other disadvantages in growth conditions and crystal properties.

From the above discussion, one realizes that in normal CZ growth, the small and/or low-aspect-ratio melt configurations facilitates the incorporation of low-levels of oxygen due to the reduction of thermal convection. Such a growth environment may be obtained by growing silicon from a small/shallow inner crucible in a double-crucible type set-up. Axial uniformity as well as concentration control using a double-crucible set-up has been demonstrated [65]. Although such an apparatus is more involved than a normal CZ growth, as the CZ charge size continues to increase, the concept of a small/shallow melt growth in a double-crucible is capable of extension to continuous CZ growth, to be discussed later in this section. For silicon materials requiring low oxygen and low microdefect density, however, the most effective method is growth under an applied magnetic field. For very low level oxygen incorporation (a few ppma), crucibles made of non-oxygen containing materials, such as Si_3N_4 , have been used for silicon crystal growth [66,67]. In this case, the source of oxygen is from the silica beads added in the silicon melt. The oxygen

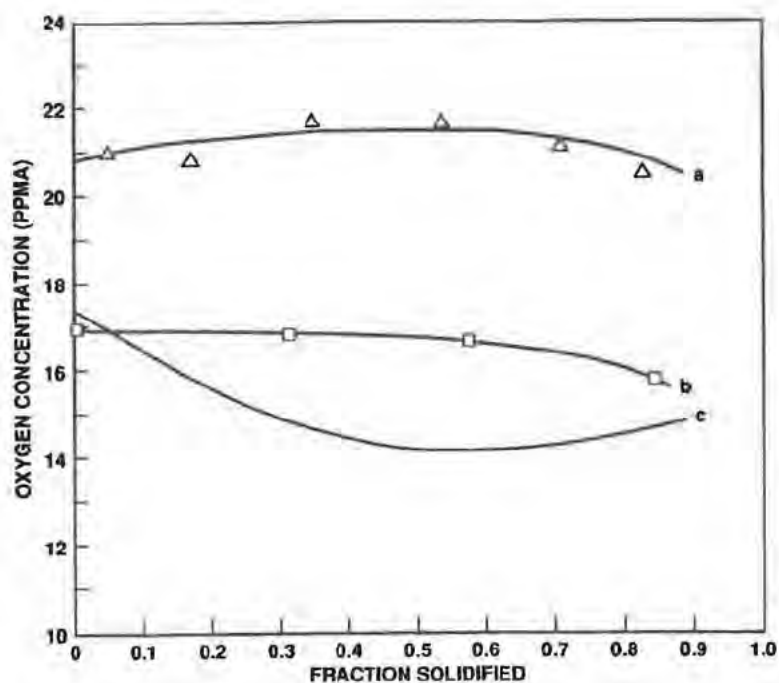


Figure 23 Uniform axial oxygen profiles of silicon crystals using variable crucible rotation rates during growth (curve **a** and **b**), as compared with that due to normal growth (curve **c**). (From Ref. 143.)

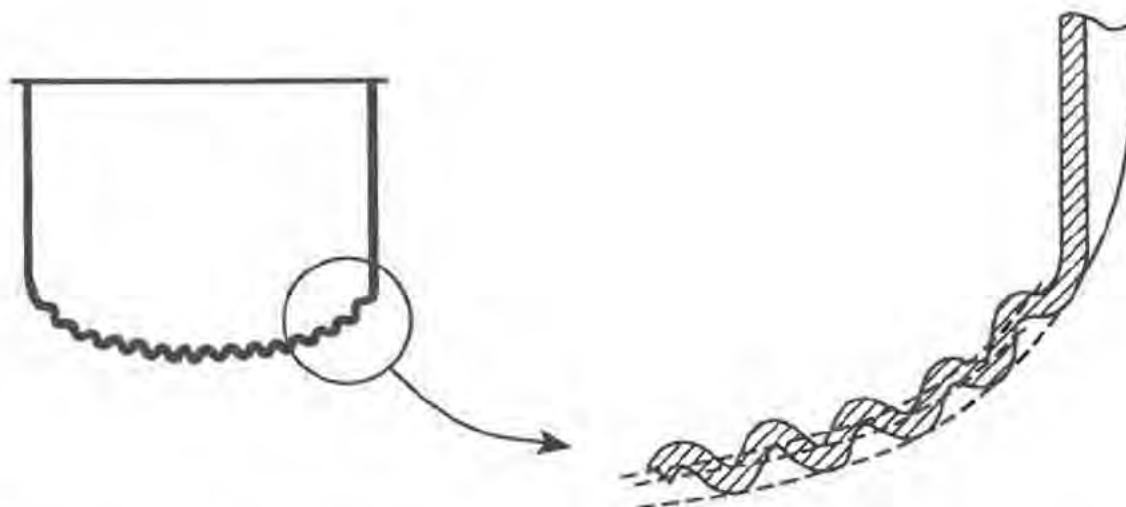


Figure 24 Schematic of the cross-sectional view of the crucible design with corrugated crucible bottom.

incorporation is controlled by the ratio of the surface area of the SiO_2 beads to the free melt surface. In general, the oxygen incorporation in normal CZ silicon growth from a large melt can be controlled to within ± 1.5 ppma of the normal concentration range of interest.

Magnetic Field Applied Czochralski Growth (MCZ). From the previous discussion, it is clear that thermal convection in a large silicon melt plays a major role in determining many aspects of the crystal quality of CZ silicon. In particular, oxygen concentration as well as dopant and oxygen uniformity are of con-

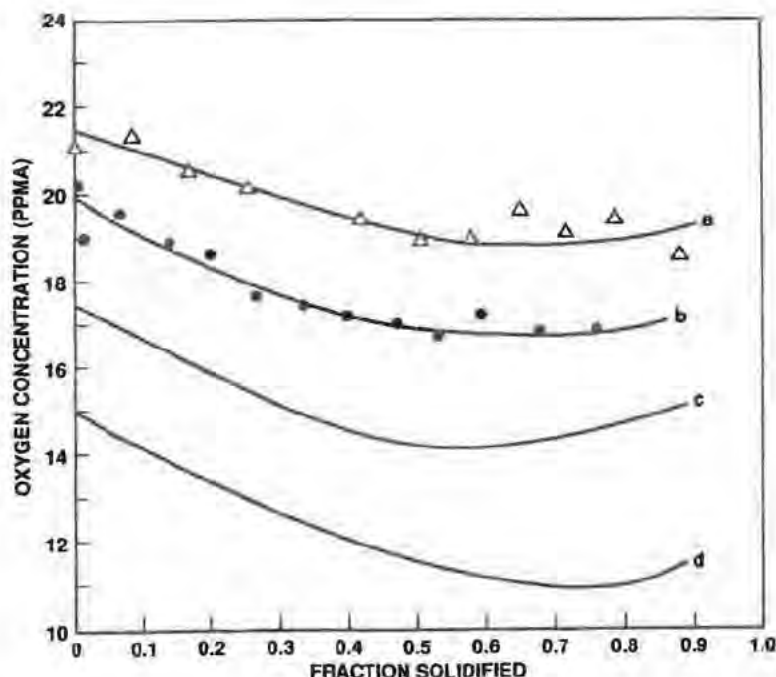


Figure 25 Axial oxygen profiles showing enhanced incorporation by (a) extra quartz adhered to crucible bottom and (b) corrugated crucible bottom. Curve (c) is due to normal growth and curve (d) is due to the use of forced convection conditions for low-oxygen incorporation. (From Ref. 143.)

cern. The ability of a magnetic field to suppress the thermal convection in electrically conducting fluids was demonstrated in the 1960s in crystal growth experiments [68]. In 1970, a transverse magnetic field was applied for the same purpose in CZ growth of indium antimonide [69]. The application of a magnetic field across an electrically conductive melt increases the effective kinematic viscosity of the melt [70] and thus suppresses the thermal convection and related temperature fluctuations in the melt.

Hoshi et al. [71] first reported CZ silicon crystal growth under an applied transverse magnetic field. Aside from a reduction/elimination of impurity striations, MCZ displayed the potential for growing low-oxygen, low-microdefect and higher resistivity CZ silicon for applications in power devices and imaging devices such as CCD. Since 1980, various types of magnetic field configurations [72,73] in terms of field directions (VMCZ for vertical, HMCZ for horizontal and cusp magnetic field) and the magnet types used (normal conductive or superconductive), have been developed and crystal growth studies have been carried out. Figure 26 shows a comparison of

the magnetic field direction/distribution of the three MCZ methods.

In general, both VMCZ and HMCZ growth have been shown to reduce temperature fluctuation related growth rate fluctuations, resulting in reduced impurity striations. However, the magnetic field effects on impurity incorporation behavior vary widely depending upon the field direction with respect to the growth axis, and field strength. For example, increased field strength enhances oxygen concentration under a vertical field [74], whereas oxygen incorporation is retarded under an increased transverse magnetic field [75]. Therefore, a transverse magnetic field facilitates the incorporation of low ($<5 \times 10^{17}$ atoms/cm³) to medium ($5\text{--}10 \times 10^{17}$ atoms/cm³) oxygen concentrations, whereas a vertical field facilitates the growth of silicon with medium to high ($>10^{18}$ atoms/cm³) oxygen concentrations. In fact, extremely high oxygen concentrations, near or above the solubility limit, can be incorporated under certain growth conditions with vertical magnetic fields [74,76]. Forced convection induced by crystal and crucible rotations can also perturb the oxygen incorporation

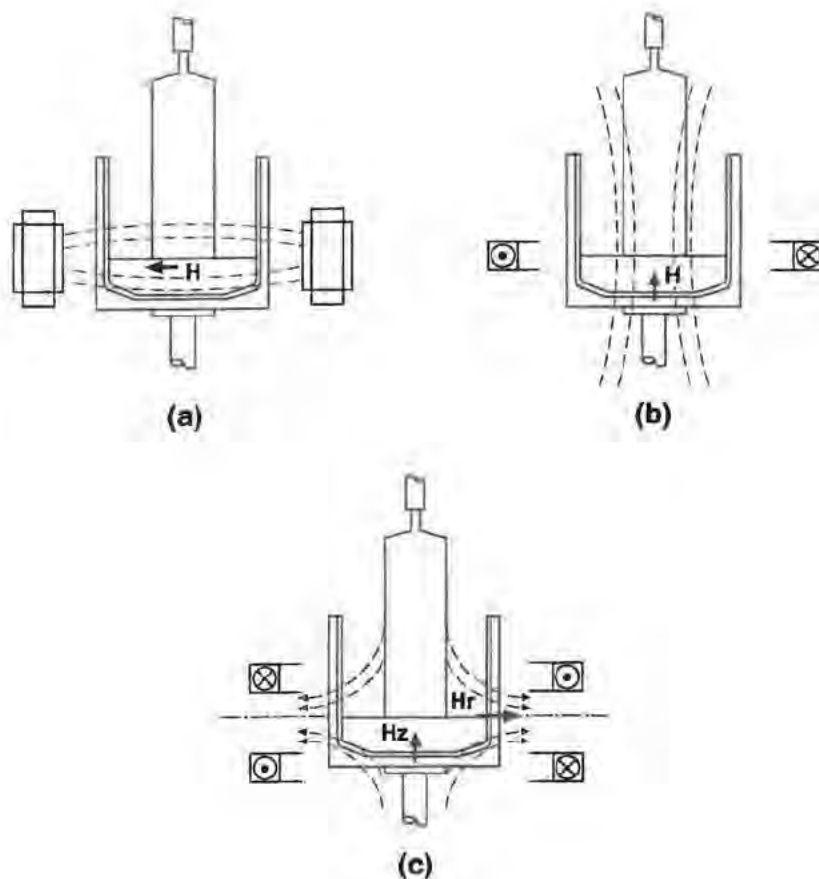


Figure 26 Schematics showing arrangements for magnetic Czochralski; (a) horizontal magnetic field; (b) vertical magnetic field, and (c) cusp magnetic field. The arrows indicate field directions.

under a magnetic field. Several large diameter MCZ crystal growth experiments from large melts have provided information on the difference in oxygen incorporation behavior between HMCZ and VMCZ. For example, Ohwa et al. [76] made a comparison of oxygen incorporation behavior between VMCZ and HMCZ using the same puller, as is shown in Figure 27. In the HMCZ mode, a low level of oxygen concentration (~ 4 ppma) is incorporated in a horizontal magnetic field of 0.25 Tesla (2500G) with good axial uniformity. The crystal rotation shows no effect on the incorporation level under this condition. However, it is shown in another study [75] that, under HMCZ, an increase in crucible rotation increases the oxygen incorporation level. As in the normal CZ, high crucible rotation often results in some degradation in radial uniformity. In such an instance, the use of a higher crystal rotation rate would help to reduce the oxygen radial gradient. Figure 27 also shows that, in VMCZ

mode, higher oxygen concentration may be incorporated using a magnetic field strength 1/3 of that for HMCZ. Unlike HMCZ, the oxygen incorporation level in VMCZ is a strong function of crystal rotation and the incorporation switches to a much higher level through a sharp transition during the crystal growth. Both the incorporation level and the transition point are clearly a function of crystal rotation, indicating that under VMCZ mode the crystal rotation induced forced convection acts as a major transport mechanism.

Figure 28 shows models proposed by Hoshi et al. [77] for the magnetic damping of the melt flow for VMCZ and HMCZ. In view of the model for VMCZ, the melt flow from outer to center regions of the melt (flow perpendicular to the vertical magnetic flux) are retarded. Under this condition, the forced convection induced by the crystal rotation is an effective transport for the oxygen-rich melt from the crucible

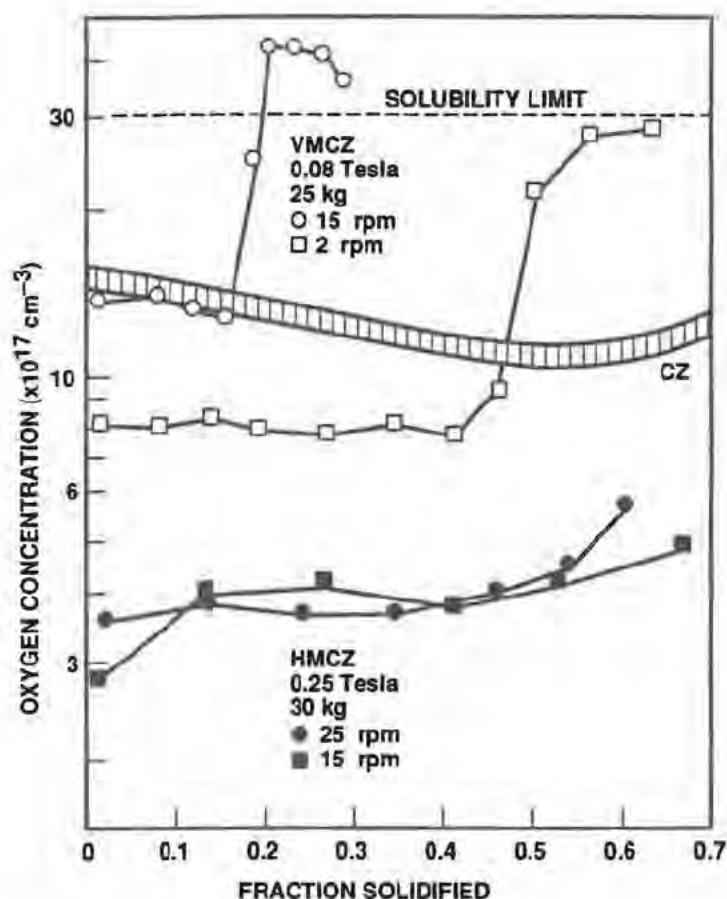


Figure 27 Oxygen profiles of silicon crystals grown under horizontal and vertical applied magnetic fields under the conditions indicated. (From Ref. 76.)

bottom to the growing crystal. As the melt aspect ratio is reduced during the crystal growth, at some transition point, the forced convection would take over as the dominant transport mechanism and the incorporation level is sharply increased. The occurrence of this "transition" seems to depend on the crystal rotation used; the higher the crystal rotation, the sooner this transition occurs during the growth. It is interesting to note that the observed "transition" in incorporation level for the VMCZ growth is similar to that discussed earlier for normal CZ growth under high crystal rotation (30 rpm) with the crucible in iso-rotation mode (2 rpm) (see Fig. 14). In both cases, the behavior is attributed to strong crystal-rotation-induced convection. In the case of HMCZ, the model of Hoshi et al. shows that the transverse magnetic flux damps the vertical melt flow near the wall due to thermal convection and crucible rotation, resulting in retarded

oxygen transport and therefore, a low level of oxygen incorporation. The forced convection induced by the crystal and crucible rotations are more effective in the transverse direction, parallel to the magnetic flux. Thus, the increased crucible rotation would help crucible dissolution and transport of the oxygen-rich melt follow flow path delineated in the model.

The results by Ohwa et al. discussed above and other large-diameter, large-melt VMCZ growth indicate that oxygen incorporation (and other growth characteristics) in VMCZ is affected by many variables and is not easily controlled. Furthermore, impurity segregations were observed to depend on the vertical field strength [78,79]. The segregation coefficient of the impurity (such as phosphorus, gallium, carbon and oxygen) tends to increase (toward unity) as the magnetic field increases. However, the radial uniformity of these impurities is significantly degraded

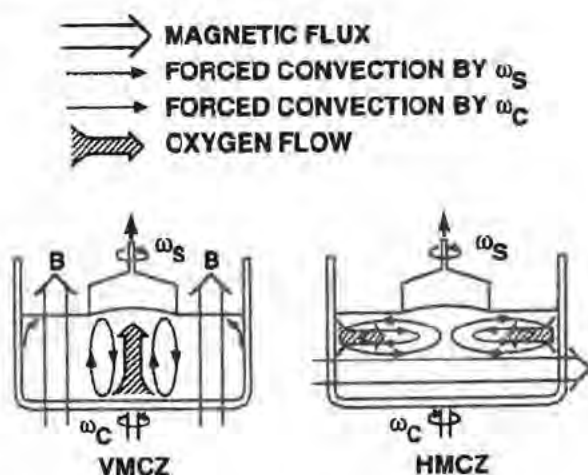


Figure 28 The effect of vertical and horizontal magnetic field on damping melt flow in Czochralski crucible. (From Ref. 77.)

in a vertical field [74]. For example, the radial oxygen gradient in a 100 mm diameter silicon crystal can reach 30–50% when grown in a high vertical field. These properties are not desirable. The change in segregation and severe degradation of the radial gradient found for growth in VMCZ have not been reported for HMCZ growth. From considerations of growth control ability and crystal properties, HMCZ is the preferred approach for MCZ growth. The HMCZ method can grow large diameter silicon with oxygen levels ranging from a few ppma to over 20 ppma with axial concentration uniformity.

The CZ crystal growth under an applied cusp magnetic field was designed to minimize the undesirable characteristics of VMCZ discussed above [80,81]. A CZ growing system with cusp magnet field uses two sets of coils (often superconducting) co-axially with the crystal, which are energized in opposing directions, as shown in Figure 26(c). In this arrangement, the crystal-melt interface is located in the symmetry plane between the two coils and is maintained in this position throughout the growth by adjusting the crucible height. The resulting magnetic field distribution in the growing system is represented by the dotted lines in Figure 26(c). Essentially, the major, and significant magnetic components are vertical magnetic field orthogonal to the crucible bottom, H_z , and the radial field orthogonal to the side walls of the crucible, H_r . The melt free surface has no orthogonal magnetic field component. As discussed earlier, the crucible erosion rate and evaporation rate

at the melt free surface are factors determining the oxygen concentration in the bulk melt, and therefore the incorporation level. The erosion rate at the side wall is believed to be under diffusion control. The orthogonal components of the magnetic field at the side wall and bottom have the damping effect on melt flows parallel to the crucible surface (such as thermal convection flows), resulting in thicker diffusion boundary layer, and thus a lower erosion rate. At the melt free surface, on the other hand, the boundary layer controlling the oxygen evaporation is determined by the radial melt flows, such as Marangoni flows and centrifugal flows pumped outwards from the crystal by the crystal rotation induced forced convection. But these flows are not damped since there is no orthogonal magnetic field components at the melt free surface. Thus, the oxygen level can be reduced by retarding the crucible erosion while leaving surface evaporation unaffected. The degree of oxygen level reduction is proportional to the applied field strength generated by the two coils. However, when the melt surface is located away from the symmetry plane of the cusp magnetic field, the melt surface will be subjected to the effect of orthogonal magnetic components, resulting in reduced oxygen evaporation and increased oxygen level [79].

In general, the main application of cusp magnetic field applied CZ growth is in the low oxygen incorporation in addition to the usual advantages of magnetic CZ, such as reduced temperature fluctuations in the melt, etc. The orthogonal components acting on the melt surface and on the crucible walls can be controlled independently. Thus, the controllability of the magnetic field is the main benefit such that the desired incorporation level with good axial uniformity can be achieved. The crystals so grown are without degradation in radial properties and abnormal segregation behavior of the dopant experienced by the VMCZ incorporation. However, it is essential to optimize the crystal and crucible rotation condition to match the applied field strength and fraction of solidification during the growth in order to achieve radial and axial uniformity of oxygen and dopant [83].

C. Grown-in Microdefects

1. Relevance to Growth Parameters

Microdefects are formed in normal “dislocation-free” melt-grown silicon crystals due to condensation or agglomeration of excess point defects at or near the growing interface. In the 1970s, the so-called A and B defects were observed in FZ crystals [84]. The A defects were identified as small “extrinsic” dislocation

loops and B defects the embryos for the A defects as characterized by TEM. The defects are the result of condensation of Si self-interstitials and they can be electrically active when decorated as may be revealed by EBIC (electron beam induced current) [85]. Fast growth rates were found to eliminate the A, B defects [84]. The other type of defects, termed "D" defects in FZ crystals were attributed to the condensations of excess vacancies. In recent years, the microdefects in as-grown CZ silicon have been studied extensively. Defects similar to D and A defects found in FZ silicon have been observed in CZ silicon [86]. The major findings and their relevance to crystal growth are discussed in the following.

In a CZ silicon growth with a "normal" growth rate, the cross section can often be divided into two regions: the inner region is vacancy-rich and the outer concentric region is silicon self-interstitial rich. The two regions are separated by a concentric ring border that can be characterized by populations of oxidation induced stacking faults (OSF) upon oxidation of the wafer as is shown in the schematic in Figure 29. Empirically, it has been found that the diameter of the "OSF ring" is reduced when the growth rate is reduced and vice versa. The microdefects have been observed inside the OSF-ring by several detection methods; COPs as revealed by repeated standard SC-1 cleans of the wafer surface (as small scattering centers)

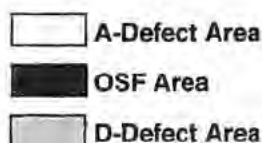


Figure 29 Schematic showing a ring region (oxidation induced stacking faults region upon oxidation) separating A-defect-rich and D-defect-rich areas.

[87] (see Fig. 30), FDPs as delineated by the Secco etch of the wafer surface without agitation [88], LST defects [89] or by an optical precipitate profiler (OPP). Their respective defect densities have been correlated with crystal growth rate (Fig. 31) and with the defect densities of the GOI measurements (Fig. 32). Furthermore, from the correlation such as shown in Figure 33, it was speculated that the defects detected inside the OSF-ring by different methods have a common origin, i.e. they are agglomerates of vacancies

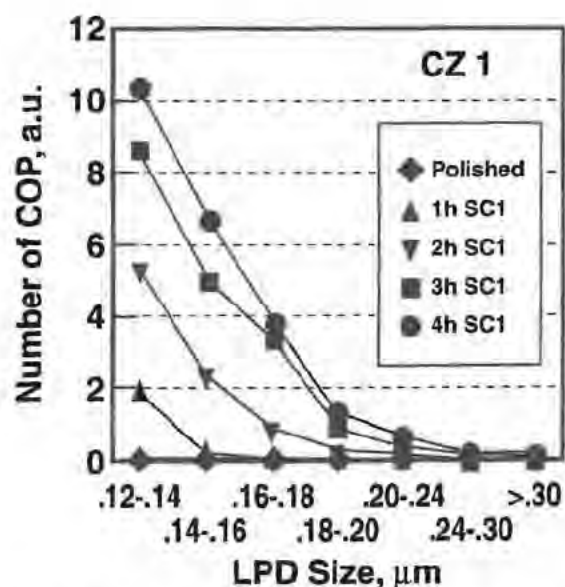


Figure 30 Light scattering point counts due to COP defects as a function of length of SC1 clean solution treatment and "particle size." (From Ref. 97.)

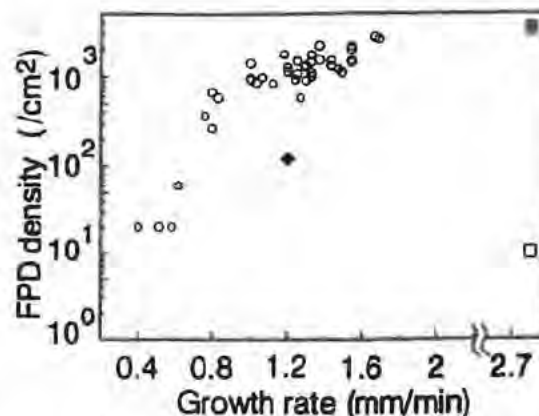


Figure 31 Flow pattern defect density as a function of CZ crystal growth rate. (From Ref. 58.)

in nature, and are referred to as "D" defects. Systematic studies have found that COPs, FPDs and LSTs are same defects revealed by different detection methods [90]. The defects in the region outside the OSF-ring are referred to as "A" defects which have been shown not to affect GOL, but degrade DRAM performance and yield. "A" defects are normally observed as "large pits" following Secco etch of the wafer surface.

Due to the harmful effect of the D defects on the gate oxide quality and A defects on DRAM, it is desirable to minimize the formation of clusters of either of these point defects but to achieve a nominally low level of each type. In the extreme case, the diameter of the OSF-ring shrinks to zero and whole wafer is free of D defect. Experimentally, the OSF-ring diameter

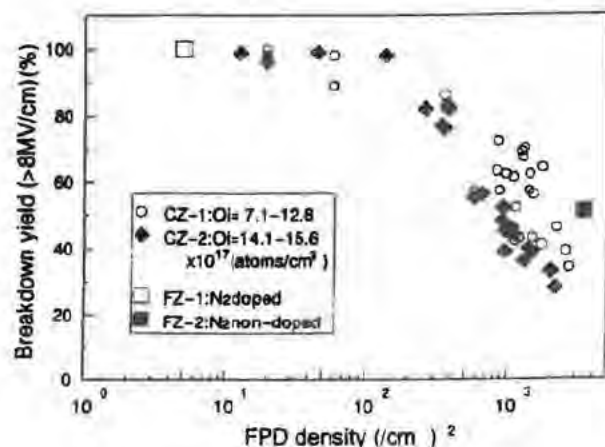


Figure 32 C-mode oxide break yield as a function of flow pattern defect density. (From Ref. 58.)

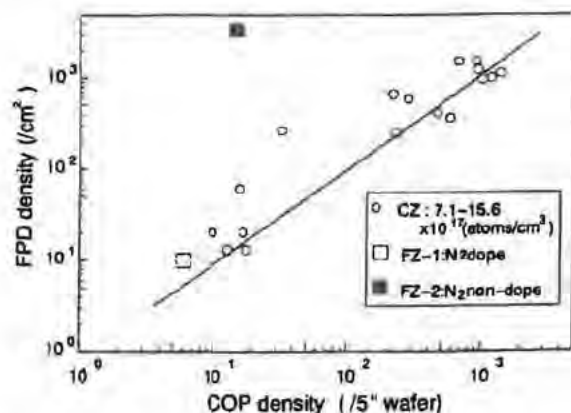


Figure 33 Correlation between COPs and FPDs. (From Ref. 58.)

was found to increase as the growth rate is increased. However, the dependence of the ring diameter on the pull rate behave remarkably different for different crystal diameters or when the surface cooling condition is changed via, for example, an added radiation shield [91]. A radiation shield serves to isolate the crystal surface from the radiation heat from the heater and silicon-melt surface, resulting in an increase in surface cooling rate and therefore an increase in axial thermal gradient in the crystal near the liquid-solid interface. The net effect depends on the heat shield design. Crystal growth experiments with various designs of heat shields show that the OSF-ring diameter, and therefore the fraction of the silicon wafer containing D defects, depends not only on the crystal growth rate, but also the axial thermal gradient in the crystal at the growing interface. Based on experiments, von Ammon et al. [91] found that there exists a constant critical value of $V/G(r) = C_{crit} = 1.3 \times 10^{-3} \text{ cm}^2 \text{ min}^{-1} \text{ K}^{-1}$ which allows a calculation of the radial position r of the OSF-ring if the pull rate V and radial variation of the axial temperature gradient $G(r)$ are known [91,92]. The empirical formula can be explained based on Voronkov's theory [93,94] which predicted a change from vacancy to Si interstitial type defects at a critical value of V/G . Based on the empirical equation, Figure 34 shows computed dependence of OSF ring diameter on the crystal pull rate for various crystal diameters. It shows that the larger the crystal diameter, the slower the pull rate is required to completely eliminate the vacancy type defects [95]. At 100 mm diameter, a pull rate of 0.65 mm/min is required for vacancy defect-free growth, while a much lower pull rate, 0.35 mm/min, is required to eliminate the vacancy defects for the

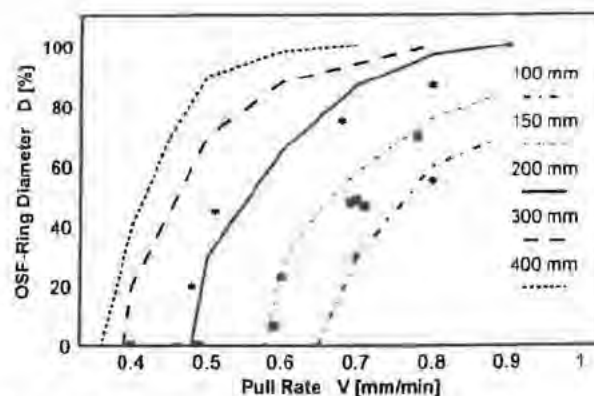


Figure 34 OSF-ring diameter as a function of crystal pull rate for different crystal diameters. (From Ref. 95.)

300 mm diameter crystal. Too low a pull rate, however, presents a problem in maintaining a stable and steady growth rate, which is essential for dislocation-free growth.

The above discussions on the occurrence of the "D" defects are for lightly doped silicon crystal growth. The defect formation mechanism is apparently different for heavily doped boron silicon. It is found that the diameter of OSF ring [95], and COP density [96,97], decrease dramatically with increasing boron concentration (for resistivity <20 m ohm-cm, Fig. 35). This effect was attributed to Fermi-level effects of boron-vacancy pairs [98]. The other probable explanation was based on the modification of the generation mechanism and/or diffusivity of the intrinsic defects in the strained silicon lattice induced by the high concentration of smaller-sized boron atoms compared to silicon.

2. Defect Structures

Although the microdefects in CZ silicon have been detected for quite sometimes by various methods as mentioned above, only recently have the detailed structures have been revealed by transmission electron microscopy (TEM) and meaningfully correlated to the features detected by other methods. Modern day bulk defect detection methods such as IR Laser Scattering Tomography and precision thinning/etching tools such as FIB (Focused Ion Beam) make it possible to isolate bulk defects in a small thin sample to be studied by TEM. Since the most significant impact of the microdefects in silicon is on the GOI

failures, the defects were first observed by TEM as voids by Parks et al. [99] as the origin of oxide defects. The octahedral voids were also observed to exist under the dielectric breakdown sites of thermal oxide films by the Cu decoration method [100], (see Fig. 36). The TEM also identified the LST defects in the silicon bulk as octahedral voids [101–103]. In general, the TEM findings on the D defects can be summarized as voids bounded by {111} planes having a structure of two inverted pyramids (see Figs. 37 and 38). The analyses by the energy dispersive x-ray spectroscopy (EDXS) indicated that there are no other signals except silicon. The silicon signal is weaker inside the defect than its surrounding, an evidence of a cavity. Their typical size is 0.1–0.2 μm and they often appear as twins or triplets, although the individual defect is usually an incomplete octahedron (some tops of the octahedrons are cut to result in complex polyhedral). The side walls of the octahedron are lined with an oxide layer; EDXS and Auger spectroscopy analyses suggested that the oxide is SiO_2 and is ~ 2 nm thick (see Fig. 37b). The void structure with oxide linings in the side walls make it unique as a CZ crystal defect, since CZ crystal growth incorporate significant amount of interstitial oxygen. The formation mechanism of the octahedron void defects is not clear. It involves complex interplays between several crystal growing factors. The temperature fluctuations at the growing interface, the growth rate (and axial thermal gradient in the crystal) and dwell time at a critical temperature range (Several temperature ranges have been proposed in between 900–1100°C [104,105] in the post-freezing crystal all play a role. Several models have been proposed [106].

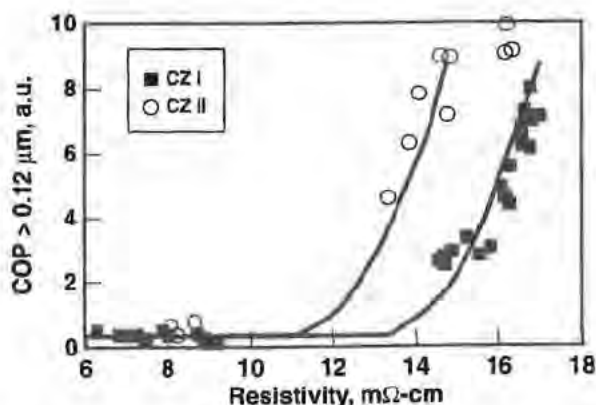


Figure 35 COP density as a function of crystal resistivity, showing that the crystal is essentially COP-free when the resistivity is less than 10 m ohm-cm. (From Ref. 97.)

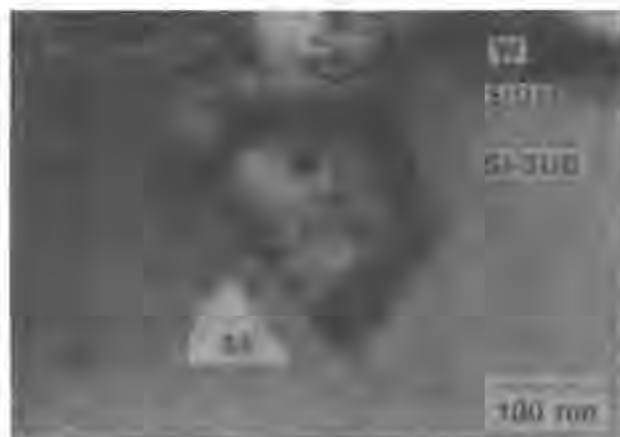
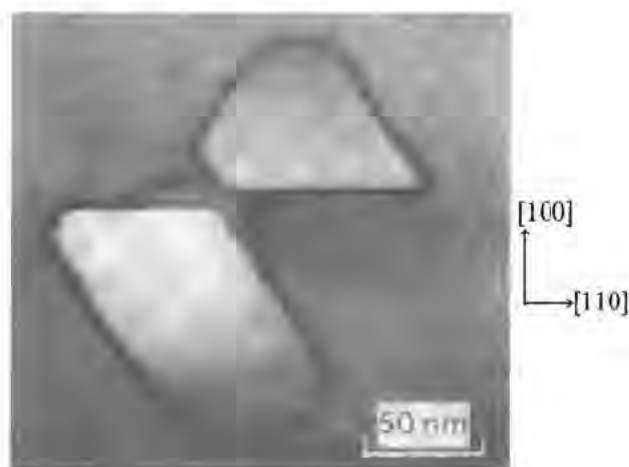
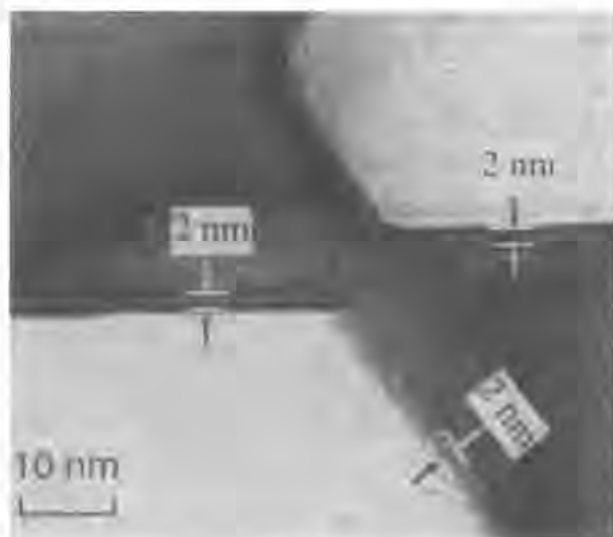


Figure 36 Cross-sectional TEM observation of an oxide defect. (From Ref. 102.)



(a)



(b)

Figure 37 Cross-sectional TEM view of LST defects. (From Ref. 102.)

IV. TRENDS IN LARGE DIAMETER SILICON GROWTH

A. Evolution in Crystal Diameter

As semiconductor technology continues to advance, the IC design rule is approaching 100 nm by 2006, if not earlier. In parallel with the design rule decrease, the increased circuit design complexity results in increased chip size. This has been the major driving

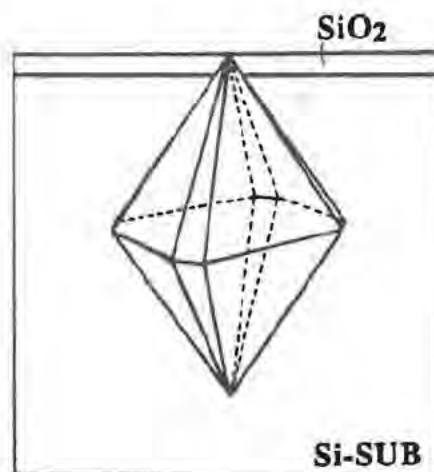


Figure 38 Schematic representation of an octahedral defect structure. Bottom photo is an enlarged view of the top showing oxide layer at void-crystal interface. (From Ref. 102.)

force for increased wafer diameter for the last 25 years, that is, to increase the required number of ICs per wafers in order to reduce IC manufacturing cost. Figure 39 shows the wafer diameter evolution in the industry since wafer diameter was about 1" in 1960. Today, 200 mm is the main stream, which was initiated in the late 1980s. In 1995, the development of 300 mm wafer was initiated, targeting for IC manufacture in the 0.25 μm /0.18 μm design rule generation. Concurrently, Japan has launched a project for development of the 400 mm wafer era technology. In the up-scaling of the wafer diameter, in the 300–450 mm diameter range, the most significant technical challenges are in the crystal growth. The growing process is far more complex than in the past. Unlike small diameter crystals, the dislocation-free as-grown yield will dominate the cost of the manufacturing of 300–450 mm diameter wafers.

To economically produce large diameter silicon crystals, one needs to employ large charge size for growing a long crystal. A charge greater than 200 kg for 300 mm diameter crystal growth or 400 kg for a 400–450 mm crystal is justified. At this melt size, thermal convection is severe. The temperature fluctuations associated with the thermal convection will make initial thin neck growth more difficult. The thermal convection would also result in higher oxygen incorporation in the crystal. It is common to apply an external magnetic field, such as a cusp magnetic field, to the large melt to reduce the thermal

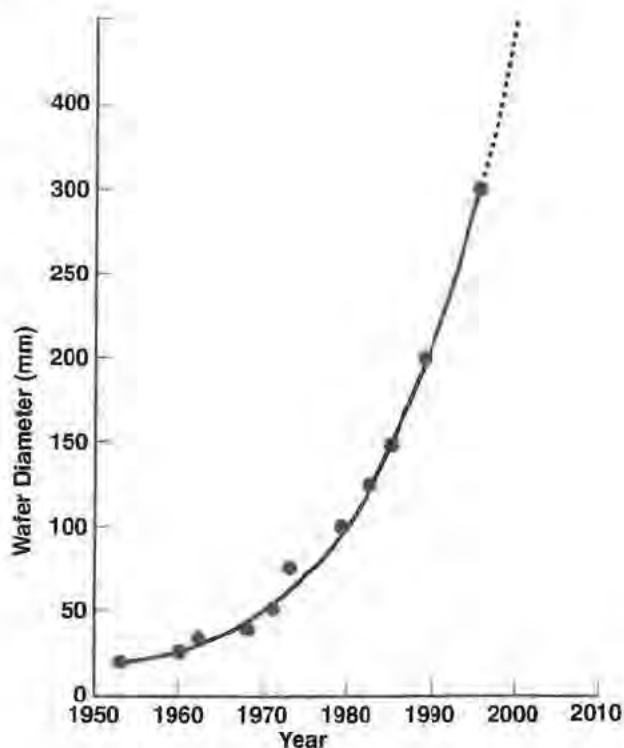


Figure 39 Evolution of silicon crystal diameter.

convection effect and to reduce the melt-crucible interaction. When growing a CZ crystal weighing 150 kg or more employing a thin neck growth to achieve the initial dislocation-free seed, one must consider the risk of fracturing of the thin neck due to the crystal weight exceeding the fracture strength of silicon. An estimate based strictly on fracture strength in tensile mode [107] predicts that the crystal weight limit is about 200 kg when the smallest neck is ~ 4 mm in diameter (a targeted neck diameter commonly used for necking). However, for 400–450 mm diameter growth, the crystal weight needs to be in the range of 400–500 kg to be comparable with the 200 mm crystals in production economics. At this weight level and to avoid neck fracture, the “Dash Neck” diameter needs to be larger than 6 mm, a diameter that is difficult to achieve dislocation free structure in the necking process. One of the solutions is to devise a “crystal suspending system” to help support the crystal weight through a “subsidiary cone” grown following the dislocation-free neck is established [108]. An example of such a proposed device is shown in Figure 40. Another crystal weight related problem is the “creep” phenomenon at the high stress concentration region at the “plastic temperature”, $>900^\circ\text{C}$. The

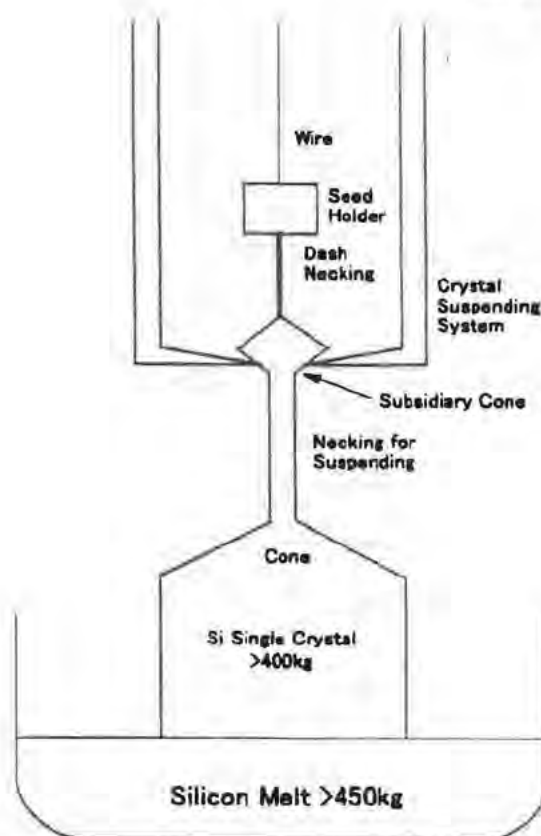


Figure 40 Schematic of a suspending system for weight support of large diameter growing crystal. (From Ref. 108.)

intersection of the crystal neck and “crown” is such a region [109]. When the stress from the crystal weight (plus the meniscus column and surface tension in the melt) exceeds the critical resolved shear stress for slip, slip dislocations will be generated and propagate down the crystal, along the slip systems, $\{110\}/\{111\}$. Two possible consequences may result. If the slip exits the crystal, the dislocation-free growing process will not be interrupted, but the crystal length above this point will not be useful. If the dislocation reaches the growing solid-liquid interface, the continued growth will not be dislocation-free. The latter case occurs when the crystal length, L , is less than $L=R \cdot \tan 54.74^\circ$, where R is the radius of the growing crystal.

Besides weight related problems, the large diameter silicon requires growth rate reduction as well. As the crystal diameter is increased, dissipation of the massive latent heat of solidification from the freezing interface becomes more difficult, since the heat transfer

paths are longer. This can be understood from the heat balance shown in Figure 3. In silicon crystal growth, a sufficiently high growth rate is essential to maintain a steady crystal growth in order to maintain the dislocation-free structure. One can enhance the growth rate by enhancing the heat transfer rate via increased crystal surface cooling. Radiation shields have been used to reduce the radiation effect from the melt and from the heater [91]. However, by doing so, the thermal gradient is increased resulting in more curved isotherms and interface shapes, enhancing the condition for higher thermal stress. The stress induced slip can occur causing structure loss. In the severe case, the high thermal stress can cause crystal cracking. Eventually, the growth rate issue may be a limiting factor in determining the maximum diameter for CZ silicon.

The increase in diameter has a profound effect on the crystal's cooling rate and, therefore, the microdefect formation. If the growing crystal's V/G is above the critical value, D defects are generated within part of, or all the radius. It is now understood that the formation of D defects (vacancy clusters), such as COPs, FDPs and LSTs, the defect density is a function of the dwell time in the temperature range of 900–1100°C [104,105]. Slow cooling reduces GOI defect density. As the crystal diameter is increased, the crystal cooling rate decreases, and the dwell time at 900–1100°C increases. It was estimated that for the 300 mm crystal, the dwell time in this temperature range is 50% longer than that of the 200 mm, 100% for the 400 mm case [95]. Therefore, the diameter increase causes the reduction in D defect density. The D defects on wafer surface cause oxide thinning and its density is directly correlated with the defect density in the GOI test. Therefore, it appears that the diameter increase certainly has a positive effect on the microdefect density.

If the diameter increase requires a decrease in the growth rate, then V/G may be in the region that the entire crystal is Si interstitial rich. The defects are in the form of small dislocation loops (A, B defects). From the available reports, it appears the A, B defects have no effect on the GOI, but may cause junction leakage in devices such as charge storage in DRAM, as crystallographic defects, especially if decorated with metallic, are potential recombination centers. The Si self-interstitial-rich silicon also does not favor oxygen precipitation, as SiO_2 induces excess Si atoms in the crystal. Therefore, oxygen precipitation in such silicon may be impeded. This factor plus the fact that large diameter crystals are low in oxygen (most are grown with MCZ) will require sig-

nificant research to assure internal gettering in these materials.

It appears that large diameter crystals grown today and in the foreseeable future will contain either vacancy or self-interstitial type microdefects, or both. A crystal growth process for growing defect-free materials is not yet available. In the CMOS processing employing thin gate oxides, <5 nm, and shallow junctions, clusters of vacancy-type or interstitial-type defects are undesirable. Therefore, IC makers may resort to epitaxial wafers or hydrogen annealed wafers [110]. The epitaxial silicon layer has higher quality than the melt grown bulk silicon. The layer is essential free of interstitial oxygen, carbon and microdefects, and lower in surface particle and metal contamination than the bulk wafer. The DRAM manufacturing group has been the largest user of the polished wafers. The microdefect problem associated with the bulk wafer may drive a significant fraction of the DRAM manufacturers to switch to epitaxial wafers. Two possible epi structures exist: p/p^+ and p^-/p^- . The former has also been popular with the microprocessor and ASIC manufacturers, the advantages including improved gate oxide quality, internal gettering, latch-up immunity, etc. The p^-/p^- approach is useful to "mask" the microdefect problems in the polished p^- wafers. The microdefects, neither dislocation loops or voids are not found to extend into the epitaxial layer during the epitaxial growth [110].

B. Continuous Czochralski Silicon Growth

The idea of continuous CZ growth came about due to the fact that as the silicon diameter continues to increase, the maximum grown crystal length of the batch CZ process is limited by the charge size. The initial motivation of the approach of the continuous growth was for the increased crystal length, and thus improved throughput and operation cost of the CZ grower. A continuous CZ growth based on a two-container system was first demonstrated by Fiegl [24]. In addition to increased crystal length, many other desirable crystal properties were also demonstrated such as improved axial uniformity of both dopant and oxygen concentrations. In particular, the arrangement affords the use of a small and shallow-melt CZ set-up in the growing container. In many ways, the two-container arrangement with crystal pulling from a constant melt volume is the same as the double-crucible operation. Figure 41 is a generalized two-container system reconfigured from a constant-volume double-crucible, where V_1 and

V_2 are the melt volumes in the outer and inner crucibles, respectively, in a double-crucible set-up. The reconfigured arrangement facilitates the addition of polysilicon and dopant. Only the outer crucible (the feeder) needs to be lifted or adjusted for the melt level control for constant volume/melt level in the growing crucible. The system offers the same advantages as the double crucible in axial uniformity in dopant and oxygen and the benefit of a small melt effect. Figure 42 shows the uniform axial oxygen profile

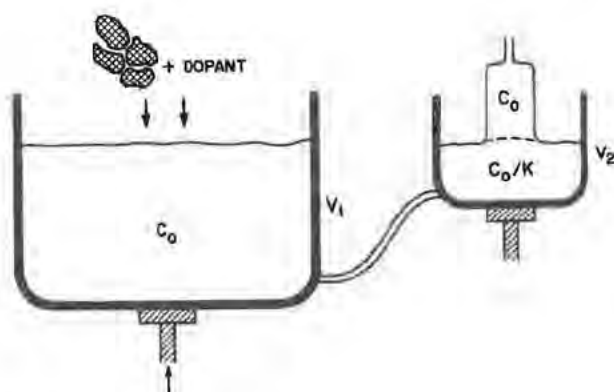


Figure 41 Schematic showing a generalized two-container arrangement for crystal growth from a constant volume melt by continuous feed. (From Ref. 18.)

obtained due to "constant volume" growth. The uniform axial dopant profile at concentration C_0 is obtained when the initial doping of the growing crucible is C_0/k and the feeding crucible concentration is maintained at C_0 . The incorporation behavior of impurities in the feed material is similar to one-pass zone leveling [22] with the "zone width" being equivalent to the melt volume in the growing crucible, V_2 . In the continuous growth mode, V_1 is the total melt volume passing from the feeding (outer) crucible to the growing crucible before V_2 is consumed and reduced. The oxygen concentration level is determined by the volume and aspect ratio of the melt in the growing crucible (see Fig. 43).

While the continuous "feed-and-pull" system with two containers appears straightforward, many engineering challenges remain to be solved or improved for the method to be practical. Among the problems to be solved are the liquid melt transfer and establishment of thermal stability and radial thermal symmetry in the melt while receiving replenishment melt from an external source. In recent years, with the availability of high-purity, small-diameter silicon beads (~ 0.1 – 1 mm) from the fluidized bed process, "feed-and-pull" may be carried out in a double-crucible arrangement as illustrated in Figures 44(a) and 44(b). In case of configuration in Figure 44(a), the partition between the inner and outer crucibles can be inserted

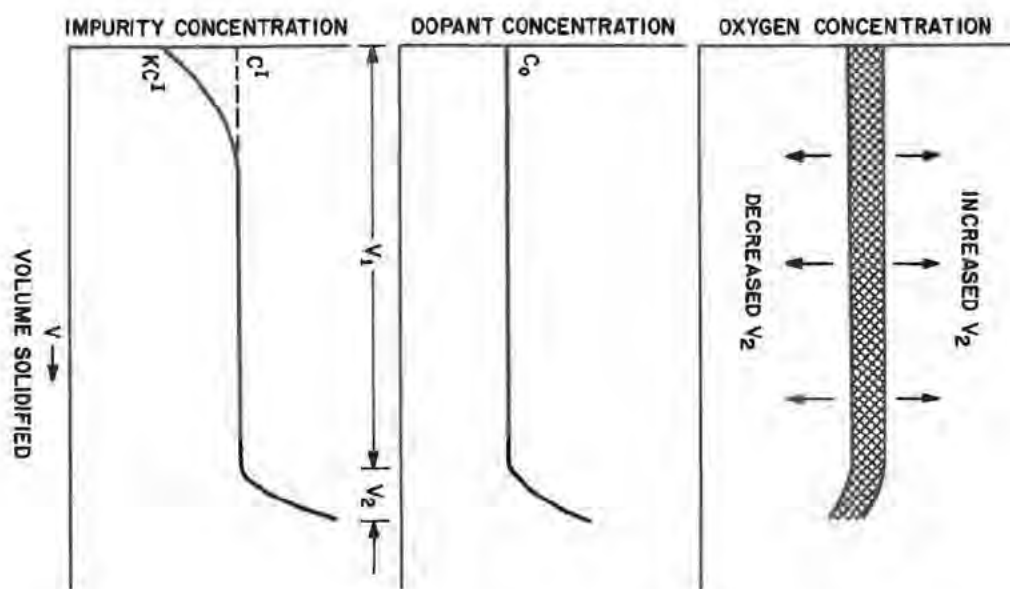


Figure 42 Axial oxygen, dopant and impurity concentrations along the crystal grown from the arrangement shown in Figure 41. The oxygen concentration level can be adjusted by changing the melt volume. (From Ref. 18.)

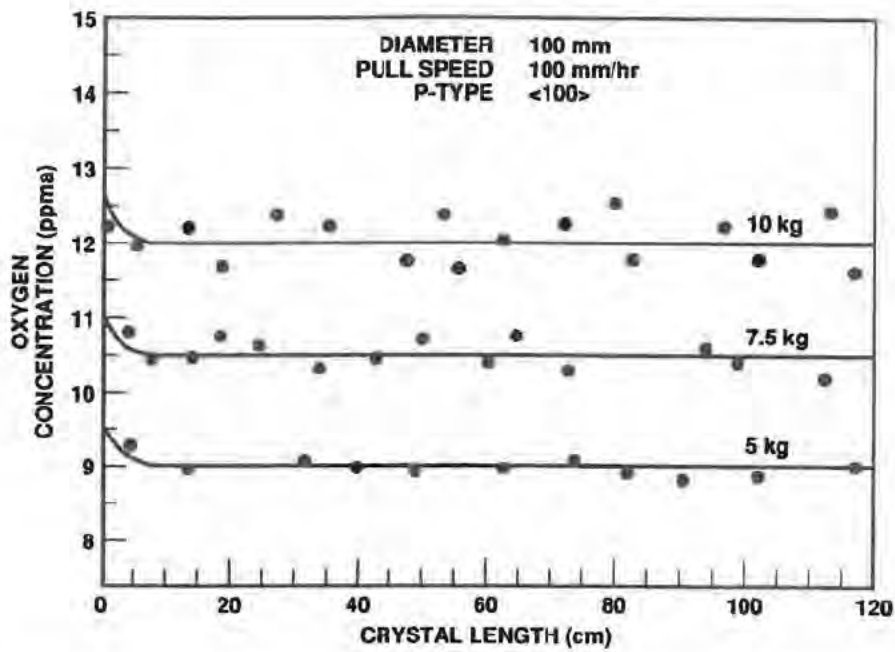


Figure 43 Uniform axial oxygen distributions from “constant volume” continuous-feed silicon growth. The oxygen level is shown to depend on the melt size. (From Ref. 24.)

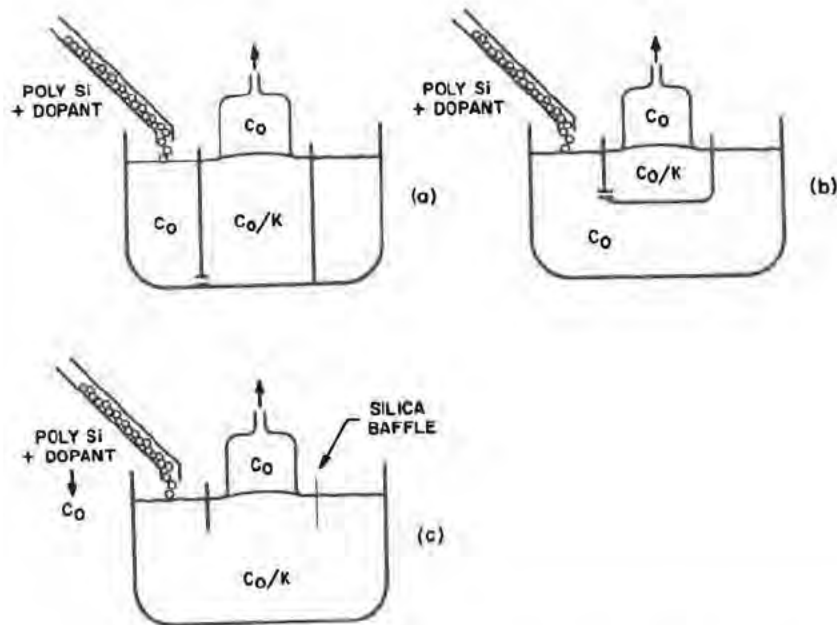


Figure 44 Crystal growth from double-crucible arrangements with (a) constant melt level or (b) constant inner melt volume, maintained by continuous-feed (c) crystal growth from a single container equipped with a circular silica baffle. Melt level is kept constant by continuous feed. The melt concentration is maintained at C_0/k . (From Ref. 18.)

after the polysilicon charge is completely melted, before the seeding begins [112]. Crystal length of 2 meters grown under such continuous "feed and pull" mode was demonstrated. If the total melt volume is kept constant, the partition separating the two melt concentrations becomes unnecessary. The resulting "one melt" growth retains the advantages of double-crucible arrangements (see Fig. 41(c)). In this arrangement, the oxygen concentration level is controlled, as in the two-container case, by the melt volume and aspect-ratio. However, the application of forced convection for additional oxygen incorporation control is more restricted than for standard batch processes. Furthermore, in this design, the single crucible contains a physical barrier to prevent unmelted silicon particles from reaching the growing crystal and a baffle that reduces thermal convection. One may also view the continuous feed mechanism as playing the role of the outer crucible which supplies silicon with dopant concentration C_0 (the intended concentration in the crystal). The small-diameter polysilicon beads add a new dimension to the development of continuous "feed-and-pull" silicon growth. Shiraish et al. [113] uses liquid-feed for continuous crystal growth of large diameter silicon (150 and 200 mm diameter crystals). In this approach, the polysilicon rods are melted into liquid silicon immediately above the growing melt, inside the growing chamber, and continuously fed into the CZ melt. The continuous-mode growth provides flexibility where the melt volume and aspect ratio of the growing crucible can be adjusted for oxygen incorporation level. This is especially important for the low oxygen incorporation, which can not be easily attained in the standard CZ growth with a melt size of 80 kg or larger.

V. WAFER PREPARATION

Silicon semiconductor devices are mostly fabricated on polished wafers or epitaxial wafers. Thus, the first step in device fabrication is the preparation of mirror polished, clean and damage-free silicon surfaces in accordance with the specifications. As the design rule of device fabrication advances into the deep sub-micron region, the device processing and performance are more sensitive to starting material's characteristics. The requirements of the geometrical tolerance of the polished wafers as well as their bulk characteristics are becoming more stringent. The polished wafers are prepared through the complex sequence of shaping, polishing and cleaning steps after a single crystal ingot

is grown. Although the detailed shaping processes vary depending on the manufacturer, the processes described below are generic in nature. Newly introduced processing technologies will be discussed where appropriate. Figure 45 is a flow chart showing a generic wafer shaping process.

The single crystal ingot is first evaluated for crystal perfection and resistivity before it is surface ground to a cylindrical shape of a precise diameter. Flat(s) or a notch with preferred crystallographic orientations are ground on the ingot surface parallel to the crystal axis. The primary flat or notch, for example, is positioned perpendicular to a (110) direction on a (100) wafer, is used for alignment of the wafer in the device processing with automated handling equipment. The primary flat, or notch, also serves as an orientation reference for chip layout, since devices fabricated on wafers are crystallographically oriented. The existence of secondary flat on the wafer, shorter than the primary, is used to identify the wafer surface orientation and conductivity type [114].

A. Slicing

The slicing operation produces silicon slices from the ground ingot. Slicing defines the critical mechanical aspects of a wafer, such as thickness, taper, warp, etc. The slicing is commonly carried out by an inner diameter (ID) circular saw (see Fig. 46(a)), after the ingot is rigidly mounted to maintain an accurate crystallographic orientation as previously determined by x-ray diffraction. The ID saw uses a thin stainless steel blade bonded with diamond particles on the inner edge of the blade. Recently, the development of multiple-wire saws has enabled the silicon slicing to result in high throughput and superior mechanical properties such as significantly reduced bow and warp. Figure 46(b) shows a schematic of a multiple-wire saw. In this arrangement, parallel, equally spaced and properly tensioned stainless steel wires spun across two pulleys are part of a single stainless steel wire winding through a complex set of pulleys. Cutting of multiple slices results when the ingot is pressed against the traveling wires under injection of slurry. Although the cutting rate is much slower than the ordinary ID saw (ordinary ID saw is 80–100 times higher rate), as many as 300 slices can be produced simultaneously. Besides higher throughput, the multiple-wire saw has other major advantages over the ID saw. Slicing by the multi-wire is actually the result of low speed grinding/lapping action by the slurry. Improved bow, warp, TTV, and taper are much easily obtained than

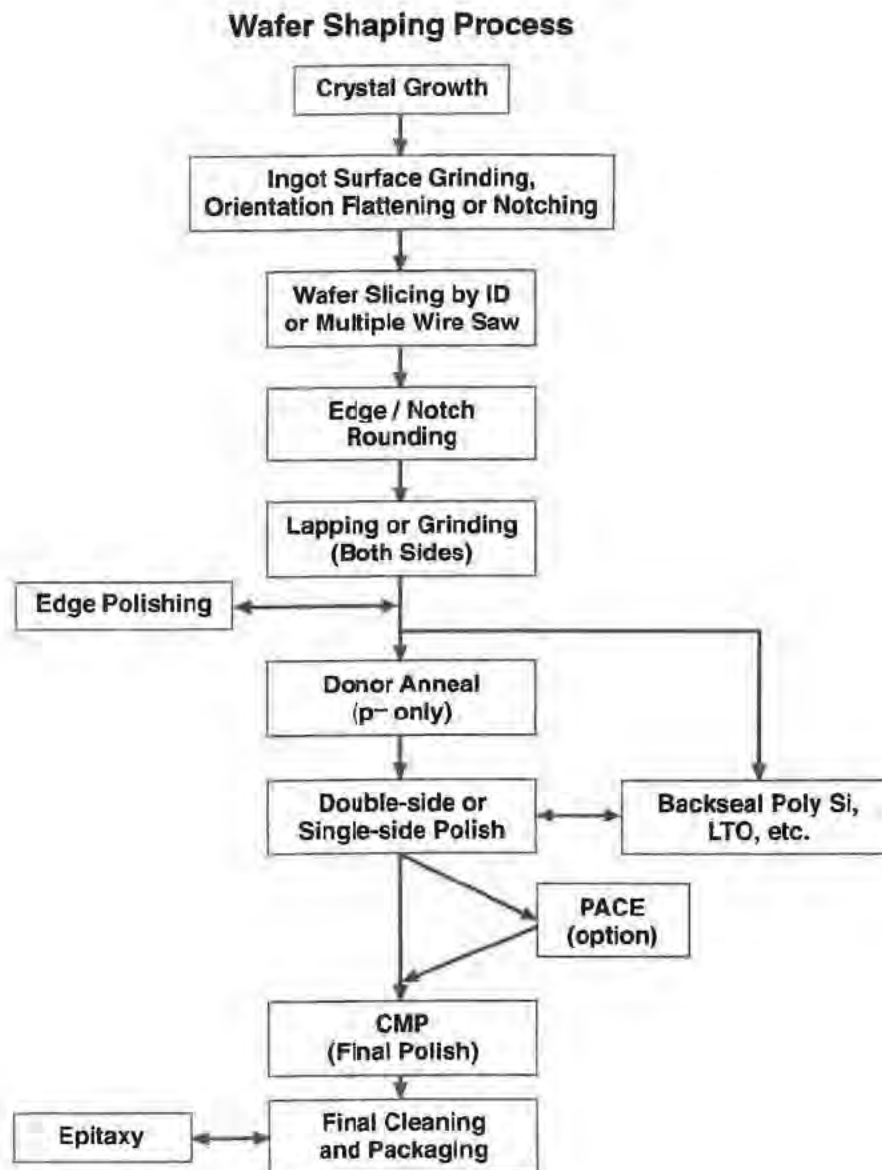
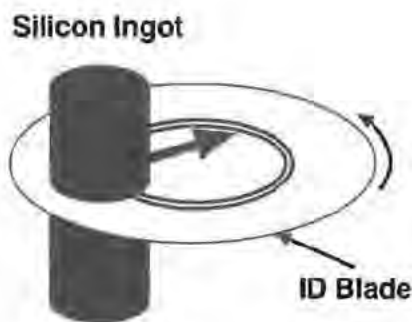


Figure 45 Flow chart describing generic steps involved in wafer preparation employing modern technologies.

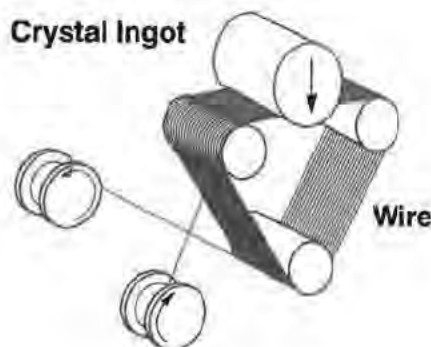
with the ID saw. In addition, the slow lapping action by the moving wire results in small kerf loss which affords more slices per inch of ingot. It is shown that the kerf size loss is very close to the diameter of the wire used. The multiple-wire saw offers material savings (reduces kerf loss by 30% compared to the ID saw), increased productivity and improved wafer mechanical properties. It has been used for slicing 200 mm and 300 mm diameter wafers and is expected to be used for the future "diameter generations".

B. Chemical Etching

Chemical etching of the slices is done to remove mechanical damage induced during the previous shaping steps—ingot surface grinding and slicing. The etching can be carried out by either an acidic solution or a caustic etchant. The acidic system is mostly based on HNO_3 -HF system (or with modifiers such as acetic acid [115]). The surface material removal is the result of two-step reactions. The Si surface is first oxidized



ID Saw



Multiple Wire Saw

Figure 46 Schematics showing the traditional ID saw and recently developed multiple-wire saw for silicon wafer slicing.

by HNO_3 to form SiO_2 , followed by its removal by HF . The acid etch produces a smooth and shiny surface. However, since the reaction is exothermic, temperature control is critical in order to maintain uniform etching. Caustic etching uses an alkaline solution [116], such as KOH , with certain stabilizers. The KOH etch offers a uniform etching rate, but produces a rougher surface than the acid etch, since KOH etching rate is crystallographic orientation dependent. Chemical etching of the slice may be repeated after subsequent mechanical operations such as edge rounding and lapping/surface grinding to remove mechanical damage.

C. Edge Rounding

The square edge of sliced silicon wafers is rounded by an edge grinder. The rounded-edge wafers greatly reduce mechanical defects, such as edge chips and cracks induced by wafer handling. Edge chips and cracks can serve as stress raisers which facilitate the onset of wafer breakage or plastic deformation and slip dislocations during thermal processing. In addition, the rounded edge eliminates occurrence of epitaxial crown (thicker epitaxial layer at the wafer edge) in the epitaxial deposition process and pile-up of the photoresist at the wafer edge. The shape of the rounded edge usually follows an industrial standard (i.e. SEMI standard) in which the edge profile fits within the boundary of a standard template. However, variations from the "standard" exist. In some applications, the rounded edge is modified to be more "blunt" in order

to facilitate the chemical mechanical polishing (CMP) operation for inter-level dielectric planarization. In this case, the "blunt" edge supposedly prevents the wafer from slipping out of the template during polishing. Other applications require more "rounded" edge shapes for increased strength. Often, a compromise on the edge profile is required.

D. Lapping/Grinding

The lapping of the silicon slice surface takes place when the slice is ground between two counter rotating cast iron plates in the presence of an abrasive slurry, usually a mixture of micro-sized alumina or silicon carbide particles suspended in a solution. The purpose of lapping operation is to remove the non-uniform damage left by slicing, and to attain a high degree of parallelism and flatness, both global and local. In fact, post-lapping slices possess the best mechanical characteristics in the entire shaping process flow. The subsequent mirror-polishing operation generally degrades the flatness characteristics attained by the lapping operation. However, lapping with slurry also introduces fresh damage to the silicon surface which requires subsequent chemical etching and chemical-mechanical polishing for removal. Chemical etching and CMP of the silicon surface degrades the wafer flatness. To circumvent this situation, surface grinder (with a precision grinder bonded with diamond particles) on both sides of the wafer is employed to achieve surface flatness with reduced surface damage. With reduced surface damage, the need for chemical etching

and CMP is also reduced and good mechanical properties may be retained.

E. Polishing

Polishing is accomplished by a chemical-mechanical polishing process involving a polishing pad and a slurry. The polishing slurry is usually an alkaline colloidal solution containing micron-sized silica particles. While CMP is used to remove surface damage and to produce a mirror-finished surface, it also degrades the wafer flatness achieved by lapping/grinding. Therefore, it is essential to optimize operational parameters so as to minimize the polishing time and flatness degradation. Double-side polishing (CMP on both front and back surfaces simultaneously) has been found to result in superior flatness than the single side polishing arrangements. The combination of surface grinding (on both sides of the wafer) and double-side CMP has shown to result in superior total indicator reading (TIR), total thickness variation (TTV) and local flatness. Such an approach is becoming a standard manufacturing process for large diameter wafers (≥ 300 mm) preparation.

The wafer preparation via mechanical methods (i.e. grinding, CMP etc.) has its limits in the degree of flatness that it can achieve. To supplement and to fine tune the local topography for further improvement in local flatness, tools such as plasma assisted chemical etching (PACE) [117] have been developed. Such a tool employs a spatially confined plasma with a scanning mechanism to allow material removal to be controlled as desired over the wafer surface. The PACE utilizes low energy neutral ions (i.e. $\ll 1$ eV) rather than energetic ions which are involved in reactive ion etching. Therefore, PACE produces minimum or no subsurface damage.

F. Cleaning

Wafer surface contamination can affect electronic device performance. The contaminants can be attached to the wafer surface physically or chemically. Cleaning of the wafers is necessary at many steps in device fabrication processes as well as during the wafer shaping processes. The silicon wafer must be free of contamination before it is shipped to the device fabrication line. The cleaning process for removal of surface contaminants during wafer shaping and polishing processes is discussed below.

In general, the contaminants can be classified as molecular, ionic or atomic. Typical molecular contaminants include waxes, resins and oil used in polishing and sawing operations, and material from the plastic containers used for slice transport and storage. Molecular contaminants are absorbed on the wafer surface by weak electrostatic forces. They should be removed before subsequent cleaning involving chemical reactions. The ionic contaminants, such as Na^+ , Cl^- , F^- , are present after wafer treatments in HF-containing or caustic solutions. They are attached to the wafer surface by chemical absorption. The atomic contaminants of concern are due to transition metal atoms such as Fe, Ni, and Cu. The transition metals and ionic species can cause degradation in device performance.

Chemical cleaning is an effective method to remove contaminants on wafer surface. Many chemical cleaning processes have been developed. The process that is widely used in the semiconductor industry is the so-called "RCA Clean" [118] which consists of two consecutive cleaning solutions including $\text{H}_2\text{O}-\text{H}_2\text{O}_2-\text{HN}_4\text{OH}$ (Standard clean 1, SC1) and $\text{H}_2\text{O}-\text{H}_2\text{O}_2-\text{HCl}$ (Standard clean 2, SC2). The SC1 clean, with volume ratios typically 5 : 1 : 1, is to remove organic contaminants by both the solvating action of NH_4OH and strong oxidizing action of H_2O_2 . The NH_4OH can also form soluble complexes with some metals such as gold, copper, nickel and cobalt. The SC2 clean, with typical volume ratios of 6 : 1 : 1, removes transition and alkali metals from wafer surface and prevents re-deposition from the solution by forming soluble metal complexes (with Cl^-). The SC1 can also remove particles physically attached to wafer surface by etching effect of NH_4OH which detaches the particles from the wafer surface. The repulsion effect of the opposite charges transferred from the electrolyte NH_4^+ and OH^- to the wafer surface and detached particle, respectively, prevent the particles from redepositing on the wafer surface. A modified RCA Clean [119], by adding a brief etch in diluted HF solution after SC1 was designed to eliminate the thin oxide layer grown on silicon surface due to the SC1 process. The thin oxide resulted from the SC1 was thought to hinder surface for cleaning by the SC2. Many modifications of the "RCA clean" exist (published and unpublished). Most of the modifications are on the volume ratios. For example, in order to reduce silicon surface roughness, there is a trend to greatly reduce the volume fraction of the NH_4OH in SC1 from the original formula. The effect of surface roughness of silicon surface on the gate

oxide integrity has been reported as significant when the oxide thickness is thinner than 5 nm, although the literature is often not consistent, probably due to different process conditions. Other chemical cleaning solutions/processes, such as piranha ($\text{H}_2\text{SO}_4\text{--H}_2\text{O}_2\text{--H}_2\text{O}$), ozonated water, etc. have also been shown to be effective. However, the "RCA clean" and its modified versions have been the most popular cleaning processes used by the semiconductor silicon manufacturers.

VI. EPITAXIAL WAFER

An epitaxial silicon wafer refers to a structure where an epitaxial layer is grown on a single crystal silicon substrate by chemical vapor deposition (CVD), normally at a high temperature. The CVD process usually involves the hydrogen reduction of high purity silicon tetrachloride (SiCl_4), trichlorosilane (SiHCl_3) or dichlorosilane (SiHCl_2) to form solid silicon. An added source gas in the reaction, such as diborane (B_2H_6) or arsine (AsH_3) provides dopant atoms for n - or p -type electrical carriers, respectively, in the epitaxial layer. The primary purpose of the epitaxial growth is to create a layer with a different, usually lighter, concentration of electrically active dopant than the substrate. Depending on the IC characteristics, the epi layer must meet a set of specifications for thickness, electrically active dopant concentration, sharpness of the epi-substrate interface, defect density and contamination.

The epitaxial layer was initially applied to bipolar devices. Typically, a lightly doped layer is grown over a substrate containing a pattern (often referred to as sub-collector) of opposite type impurity by diffusion or ion implantation. The structure allows a vertical transistor to be built with a minimum of collector

resistance and readily permits junction isolation between devices (see Fig. 47). The most common application of the epitaxial layer in complementary metal-oxide-silicon (CMOS) device processing involves a lightly doped layer over a heavily doped substrate of the same conductivity type, i.e. either p/p^+ or n/n^+ structure. The p/p^+ is by far the dominant universal epitaxial structure. It has been used by CMOS-based logic, microprocessor and ASIC manufacturers, and application of p/p^+ for DRAM is growing as the device design rules shrink to 0.18 μm . Figure 48 is a schematic of a CMOS structure built on p^- layer of the p/p^+ wafer.

It is realized today that p/p^+ wafer has many advantages over the bulk p^- wafers. The initial motivation for using such structure was to reduce the MOS device's leakage current. Since the lightly doped substrate has higher concentration of minority-carriers, the carriers can diffuse hundreds of micrometers to space-charge layers and are collected as reverse-bias leakage currents. This minority-carrier diffusion current can dominate over leakage current generated within the space-charge layers, especially at higher operating temperatures ($\geq 40^\circ\text{C}$) [120]. A technique that can circumvent this problem is to form a p^- layer ($\sim 10^{15}$ atom/ cm^3) as an epi layer grown on a heavily doped substrate ($\sim 10^{19}$ atom/ cm^3) [121,122]. The p^+ substrate has few minority carriers (electrons), so the minority carriers are only generated from the thin epi layer. Thus, the diffusion current from the substrate is suppressed, even though the minority-carrier diffusion lengths are long. This is especially important in preserving holding times in dynamic nodes (e.g. DRAM) [120].

Since its initial application in CMOS, many added beneficial functions have been found to be associated with the p/p^+ structure. The major ones include its effects in minimizing soft errors, preventing latch-up

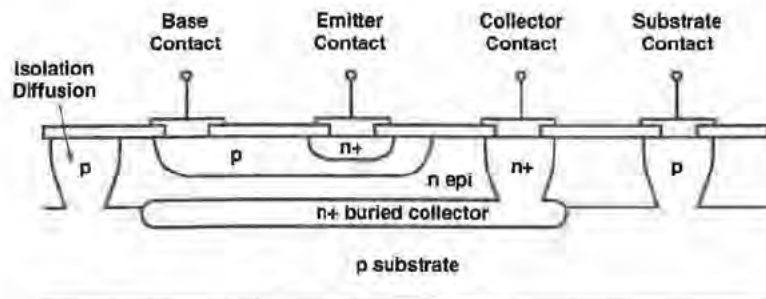


Figure 47 The role of epi layer in a bipolar device.

of the device and providing sites gettering of harmful impurities. From the device design view point, using p/p^+ structure for CMOS fabrications is the best solution for avoiding latch-up without resorting to circuit design modifications, such as adding "guard rings", etc. The latch-up is due to the turn-on of a parasitic 4-terminal, n - p - n - p lateral transistor between neighboring NMOS and PMOS transistors, as shown in Figure 48. However, if the formation of a vertical parasitic p - n - p is favorable with the presence of p^+ substrate, the turn-on of the lateral 4-terminal device may be suppressed. In a first approximation, in order to suppress the lateral p - n - p - n device, the effective epi thickness (taking into account the boron up-diffusion after device processing) must be smaller than the separation of two neighboring n - p transistors. Latch-up simulators are available to provide information for designing latch-up-free design layout, from which an appropriate epi thickness may be estimated.

P^+ substrates in p/p^+ wafers have been found to serve as excellent intrinsic gettering sites. Two effects have been observed. The first is the gettering effect due to p^+ silicon's high efficiency in generating oxygen precipitates-dislocation complexes. The oxygen precipitation in p^+ , with resistivity around 10 m ohm-cm, has fast kinetics and can result in a precipitate density which is more than an order of magnitude higher than in p^- (10 ohm-cm) under a Lo-Hi annealing condition [41]. Much of the oxygen precipitation behavior is discussed in Section 7. The second gettering effect by the p^+ silicon is due to the "segregation" effect which drives metallic impurities to the p^+ region from the p^- epi layer under a "segregation" annealing [123]. The p^+ , like other highly doped (degenerately doped)

silicon regions, such as diffused phosphorus layers, source/drain regions in the CMOS structure, have long been observed to getter metal impurities and perceived as due to an enhanced solubility effect. The segregation effect of the impurities (such as Fe) was proposed to be due to the difference in the Fermi levels of p^+ and p^- silicon [124].

One of the unique features associated with the p/p^+ structure is the possible existence of misfit dislocations at the epi-substrate interface (see Fig. 49). These dislocations can act as gettering sites as well. It is well known that doping with boron causes the silicon crystal lattice to contract (~ 0.014 Å/at% boron added) [125]. The vast difference in the boron doping levels in p/p^+ ($\sim 10^{19}$ atom/cm³ in the substrate while the epi layer is doped with 10^{15} atom/cm³) results in a lattice mismatch between the epitaxial layer and the substrate during CVD deposition [126]. Under this condition, the epitaxial growth is accompanied by lattice stress, tensile on the epi layer side and compressive on the substrate side. The misfit stress increases as the layer continues to grow, until the local stress exceeds the elastic limit at the deposition temperature, at which time the stress is partially relaxed by forming misfit dislocations at the epi-substrate interface. The onset of misfit dislocation formation during epi deposition is a function of the degree of lattice mismatch, deposition temperature and deposition thickness. The unrelaxed misfit stress will contribute to both wafer bow and warp. It should be reminded that the misfit dislocations formed on the (100) p/p^+ epi structure are contained in the (100) interface, with a Burger's vector of the form $b=a/2$ [110] [127]. Since the (100) plane is not a glide plane in the silicon lattice,

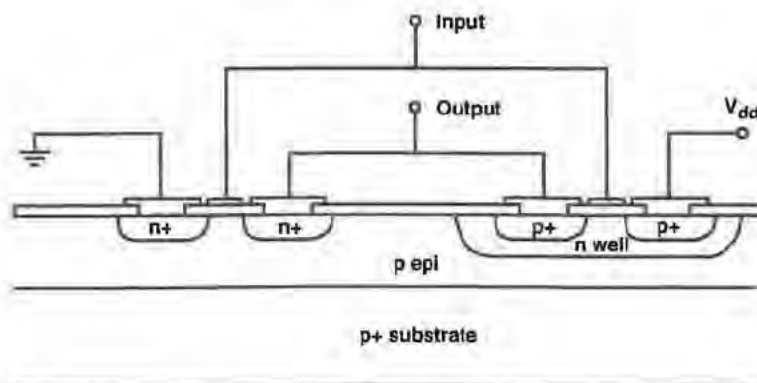


Figure 48 The role of epi layer in a complementary MOS device.



Figure 49 (110) cross-sectional view of an etched p/p^+ epi wafer, showing etched dislocation pits at the epi-substrate interface due to misfit dislocations. (From Ref. 123.)

the dislocation is immobile; it is "locked" [128] in the interface. Furthermore, the dissociation of such a dislocation into two mobile dislocations in two inclined $\{111\}$ slip planes is energetically unfavorable. However, it is possible to move misfit dislocations in silicon by a 'climb' mechanism under high stress conditions. Experimental evidences [126] shows that the movement is toward the substrate side, i.e., the side with the smaller lattice constant. The misfit dislocations so formed are stable and could contribute to gettering effect. They present no harmful effect to the epi layer structure.

Perhaps the most fundamental difference between the polished bulk wafer and p^- layer of the p/p^+ wafer is that CVD silicon is superior in quality. The epi layer is free of oxygen and carbon incorporation. The incorporation of dopant is uniform and free of local fluctuations (such as striations in CZ materials discussed in Section 3A3). In general, CVD epitaxial silicon have been recognized as superior materials for GOI in device processing than bulk CZ silicon, (see Fig. 50). More significantly, in the era of thin-gate-oxide/sub-0.18 μm -design-rule technologies, CVD silicon epitaxial material is of vital importance in the gate oxide integraty. CVD epitaxial silicon layer is also free of grown-in microdefects stemming from the agglomerations of point defects

encountered in melt grown silicon (CZ) Grown-in "D" defect (such as COPs, LSTs and FDPs) density in CZ silicon have been correlated with the oxide defect density. The issue of grown-in defects is discussed in Section 3C. However, the defects due to agglomeration of point defects in CZ growth tend not to extend into the epitaxial layer during CVD deposition. It has been demonstrated that as thin as 0.3 μm of epitaxial layer, grown on a CZ substrate containing COPs can mask the harmful effect of COPs [111]. In consideration of the impact of grown-in microdefects on device yield and reliability, many device manufacturers will be prompted to switch from bulk CZ wafers to p^-/p^+ or even p/p^- epitaxial wafers.

VII. OXYGEN BEHAVIOR IN SILICON PROCESSING

A. Oxygen Precipitant Kinetics

Oxygen in silicon tends to precipitate upon heat treatment when the oxygen concentration exceeds its solid solubility limit via homogeneous or heterogeneous nucleation mechanisms. The precipitation kinetics of oxygen at a given temperature can be described by a "time-temperature-transformation" (TTT) curve,

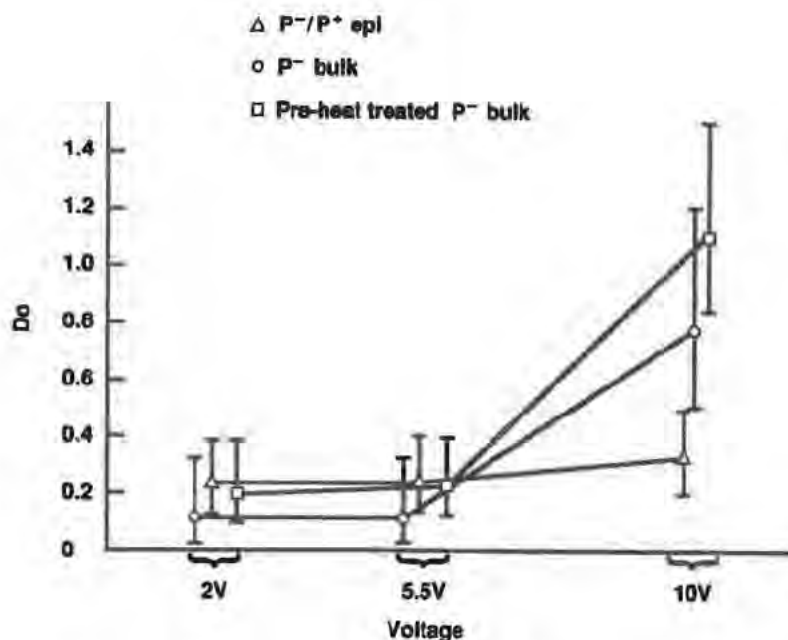


Figure 50 Defect density (D_0) extracted from voltage measurements on thin oxide grown on three different silicon surfaces. (From Ref. 141.)

such as that shown in Figure 51 for p^+ silicon where the precipitation density is plotted as a function of annealing time at 1050°C . Although various models have been proposed to describe the basic nucleation/growth mechanism [129], no simple model can take into account the effect of all the factors involved, such as crystal thermal history, oxygen, dopant and carbon concentrations, point defect concentrations and grown-in microdefects, as well as the detailed IC processes and sequence. Indeed, most of the understanding of the precipitation behavior has been based on experiments with mostly a few controlled parameters.

One of the most important factors affecting nucleation is the grown-in microdefects. Although “dislocation-free” CZ silicon grown with today’s technology is considered highly perfect, crystal lattice imperfections may be formed at, or behind, the freezing interface during growth. Microdefects, such as A, B and C type defects [84] provide sites for oxidation induced stacking faults at the wafer surface and oxygen precipitation in the bulk silicon upon subsequent heat treatment. Experiments have shown [131] that during a high temperature anneal (without a previous low-temperature nucleation anneal), a heterogeneous nucleation mechanism dominates and microdefects play as important a role in nucleation as the

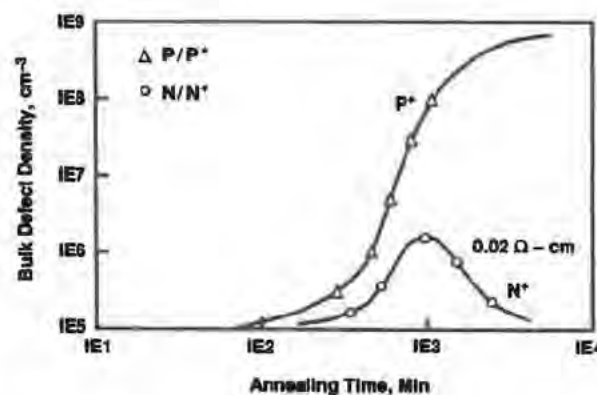


Figure 51 A comparison of oxygen precipitation kinetics in n^+ and p^+ annealed at 1050°C after epi deposition at 1150°C . (From Ref. 137.)

post-crystal growth “thermal history” experienced by the silicon. In this condition, precipitation in CZ silicon lacking microdefects would be retarded. On the other hand, when a two-step anneal containing a low-temperature nucleation step initially is used, the homogeneous nucleation mechanism dominates, and the impact of grown-in microdefects on precipitation is diminished.

Oxygen precipitation kinetics at a given temperature is primarily a function of oxygen concentration. In the ASTM standard test methods [132] for the oxygen precipitation ability of *n*- and *p*-type CZ silicon, a high temperature (1050°C, 16 hr, Method A) and a low-high (750°C, 4 hr+1050°C 16 hr, Method B) thermal cycles are utilized. The combined A and B tests reveal the state of thermal history and microdefect density of the wafers under test, when compared with a reference precipitation behavior. Figures 52 and 53 show the oxygen precipitation as a function of oxygen concentration under test methods A and B respectively, for wafers from several sources [133]. In this case, the wafers from different sources/suppliers have similar behavior.

Although it is well established that carbon in silicon has the benefit of oxygen precipitation, the precise control of carbon incorporation in a range of a few ppma during crystal growth has not been developed. While the control of carbon incorporation and uniformity are still issues of silicon growth, the carbon concentration in CZ crystals is usually kept to a minimum to avoid its influence.

The CVD deposited polysilicon film on the wafer backsurface was found to serve as a good extrinsic gettering sink because of its ability to generate dislocations and stacking faults at the backsurface. It was found that the backsurface deposited polysilicon also enhanced oxygen precipitation, which added to the efficiency of "backside polysilicon gettering". The precipitation enhancement effect was thought to be a nucleation effect due to the polysilicon deposition thermal cycle. Shirai et al. [134] have shown that a

polysilicon layer at the wafer backsurface causes localized oxygen precipitation near the backsurface. The enhancement effect was attributed to the absorption of silicon self-interstitials by the polysilicon, which causes an increase in vacancy concentration in the near-by silicon wafer, since $(I)(V)=\text{Const.}$ at equilibrium. Vacancies were considered to be effective nucleation sites.

B. Oxygen Precipitation in p^+ and n^+

In recent years, the use of *n/n*⁺ and *p/p*⁺ epitaxial structures in the VLSI/ULSI ICs has significantly increased, due to the structure's potential in reducing latch-up susceptibility in CMOS and alpha particle-induced soft error in memory devices. There is no distinguished difference in oxygen precipitation kinetics between *n*- and *p*-type silicon in lightly doped silicon (typically, 10^{15} cm^{-3}). However, as the dopant is increased to the degenerately doped region of interest (0.005–0.02 ohm-cm), the behavior is drastically different depending on the conductivity type. In this range, oxygen precipitation is retarded in Sb-doped silicon while the kinetics are at their peak for *p*-type boron doped silicon. Due to these properties, the p^+ substrate provides good internal gettering while Sb-doped n^+ leads to reduced microdefect formation and intrinsic getting during silicon processing. Figure 51 compares oxygen precipitation kinetics in p^+ and n^+ wafers under isothermal anneal at 1050°C, after an epitaxial deposition at 1150°C (without pre-epi heat treatment). The possible

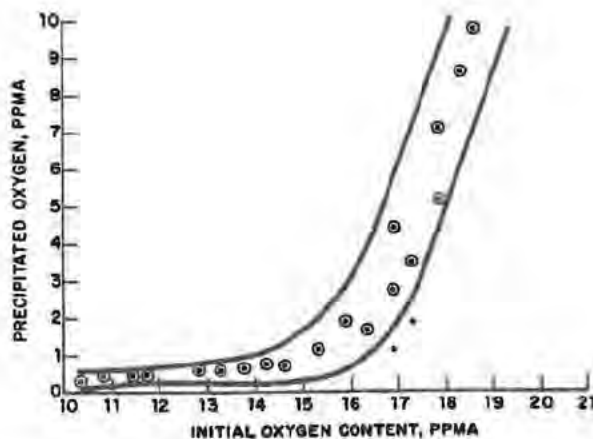


Figure 52 Oxygen precipitation after 1050°C, 16 hr anneal. Data represent wafers from six sources. (From Ref. 133.)

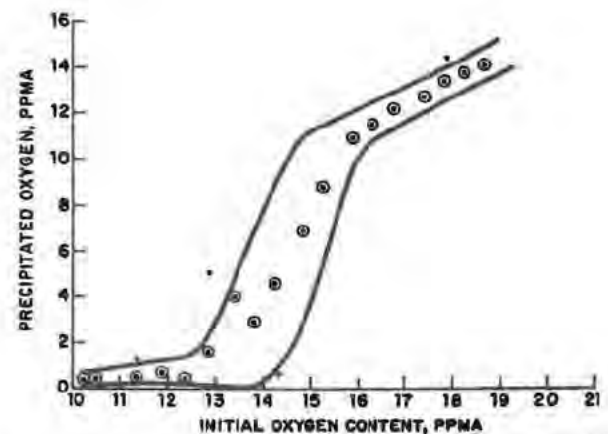


Figure 53 Oxygen precipitation after 750°C, 4 hr+1050°C, 16 hr anneal. Data represent wafers from six sources. (From Ref. 133.)

sources of differences in the precipitation kinetics in p^+ and n^+ silicon include oxygen incorporation, oxygen diffusivity, grown-in microdefect density and nucleation mechanism.

It is now established that oxygen incorporation into silicon crystals depends on the type and concentration of dopant [43]. On the average, p^+ crystals exhibit about 25% higher incorporation rate than n^+ crystals (with p^+ contents higher than n^+ , while n^+ are lower). The difference in oxygen incorporation can not account for the difference observed in precipitation kinetics in p^+ and n^+ . The diffusion mechanism of oxygen in n^+ was found to be the same as in p^- silicon [42]. The difference between the precipitation behavior in p^+ and n^+ appears to reside in the nucleation mechanism. Various models of precipitation mechanisms have been proposed in order to explain the kinetics in p^+ and n^+ . Early models [135,136] were based on the assumption that Si self-interstitials are responsible for heterogeneous nucleation; complexing of Sb^+I^- would reduce the nucleation centers in n^+ . Later models favored nucleation mechanisms based on vacancies as nucleation centers, V-O complexes [41,47,137,138]. Suppression of precipitation in n^+ was suggested as due to reduction of V^- by the formation of a high concentration of V^-Sb^+ complex [47,137]. The enhancement effect p^+ may be due to the formation of B^-I^+ complexes and increasing V^- [47], since $I^+V=Cont.$

C. Effects of Oxygen Precipitation on Device Processing

Oxygen precipitation is generally considered beneficial for its impurity gettering function in silicon processing. However, uncontrolled or untimely precipitation can result in adverse effects. In the following, the ill-effects of uncontrolled oxygen precipitation are discussed in terms of defect generation, both for epitaxial and bulk wafers.

Fast precipitation kinetics of oxygen in p^+ silicon is difficult to control. One such consideration is during pre-epitaxial deposition thermal treatments of p^+ substrates for film growth, or deposition for wafer backseal (to minimize autodoping), or external gettering purposes. For example, a two-hour, 800°C thermal treatment can induce significant precipitation in the case of a high oxygen e.g., 19 ppma (ASTM F121-80), p^+ wafer without the formation of a precipitate-free region (denuded zone). Such fast precipitation can generate a configuration where precipitates and bulk stacking faults would intersect

the polished wafer surface. Subsequent silicon epitaxial growth on such defected surfaces will generate a unique crystallographic defect structure appearing as pairs of etch pits, or "viper pits", on the p^-/p^+ epitaxial wafer surface, after preferential etching [139]. The pairs of pits correspond to the two dislocations, initiated from a single strain center, an oxygen precipitate (or related dislocation loops), at the epitaxial-substrate interface.

One can avoid unwanted oxygen precipitation in the pre-epi thermal processing by using low-oxygen p^+ silicon and/or shorter, lower temperature thermal cycles. However, it is desirable that precipitation occurs during the epitaxial deposition. Some precipitation during epitaxial deposition can add gettering ability and reduce nucleation centers for stacking faults, and saucer pit density in the epitaxial layer. For the same reason, oxygen precipitations is desired in the critical thermal steps following epitaxial deposition in the IC processing, such as gate oxidation. Therefore, in an ideal situation, the p^+ substrate shall be tailored such that (a) there is little or no precipitation as result of pre-epi thermal treatment; (b) some precipitation occurs during epitaxial deposition, to provide internal gettering; and (c) full precipitation occurs early in the device fabrication steps. This is illustrated in Figure 54. in p/p^+ wafers for conventional CMOS applications, the formation of a denuded zone (DZ) in p^+ substrate beneath the epi layer is not a critical feature. In principle, no harm can result even $DZ=0$, so long as it is formed after epi deposition. However, in some ULSI designs with trench structures fabricated on thin p/p^+ epi, the large-aspect-ratio trench structures usually extend beyond the epi layer and into the p^+ substrate. In these applications, a DZ is required so that trenches can be fabricated in the defect-free p^+ region. For device processing based on lightly doped silicon n - or p -type, oxygen precipitation kinetics are much slower than in p^+ . Depending on the oxygen level and thermal cycle sequence, the precipitate distribution in the wafer cross-section can be classified into four categories, as shown schematically in Figure 55.

The configuration in Figure 55(a) is ideal, where significant precipitation occurs along with a sufficient defect-free region for device fabrication. This situation can occur during the IC processing thermal cycles or it may be brought about by added pre-IC processing thermal cycles, such as HI-Lo-Hi or Hi-Lo thermal treatment schemes. In the latter case, "full precipitation" usually occur as a result of pre-heat treatments at the early stage of device processing.

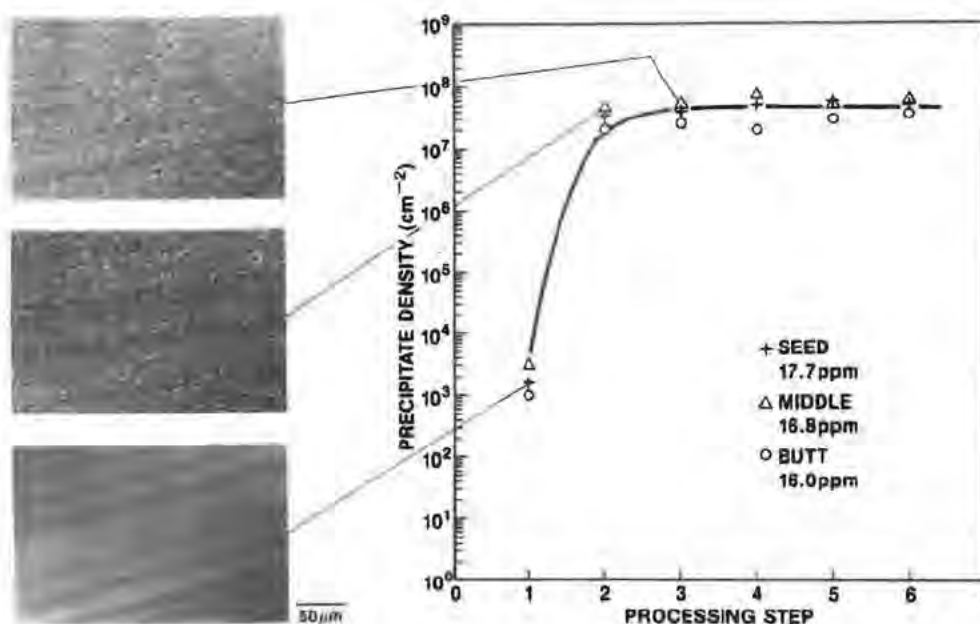


Figure 54 Oxygen precipitation density in p^+ silicon after thermal cycles due to backseal (step 1) epi deposition (step 2) and 1st four steps if Twin-Tub V process technology. (From Ref. 139.)

In the cases where precipitation getting is important, steps for enhanced precipitation are often used. However, care must be taken to avoid over-precipitation, which would "drain" interstitial oxygen from the silicon crystals. The reduction of interstitial oxygen resulting in significant oxygen precipitation lowers the wafer yield strength and makes it more susceptible to plastic deformation when subjected to thermal gradients. The net results are wafer warpage and the generation of slip dislocations into active device regions. It has been shown [140] that at least 10 ppma of interstitial oxygen should be retained to prevent the onset of slip dislocations during processing of a bipolar device. The configuration in Figure 55(b) is the result from non-perfect DZ formation, due to local precipitation enhancement caused by grown-in microdefects or micro-oxygen concentration fluctuations. This results in oxygen precipitations/bulk stacking faults near the active region of the wafer surface layer, causing emitter-collector shorts, source-drain shorts transistor junction leakage and DRAM storage or capacitance related yield problems. The configuration in Figure 55(c) corresponds to uniform oxygen precipitation where oxygen out-diffusion is impeded, resulting in no DZ formation and the possibility that precipitates/bulk stacking faults would intersect the wafer

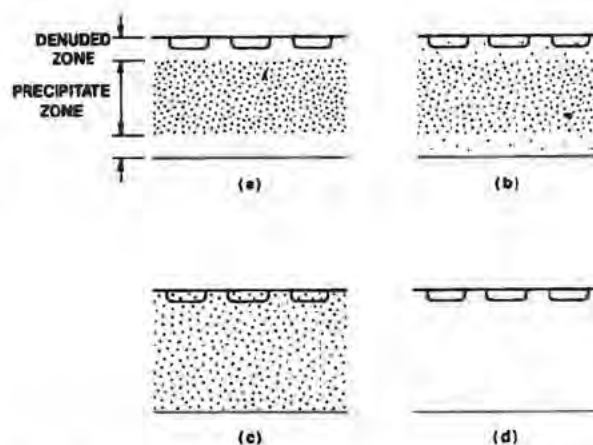


Figure 55 Schematics of wafer cross-sections showing four categories of DZ/precipitation distributions during IC process. (From Ref. 139.)

surface. The situation stems from a gross oxygen concentration-process thermal cycle-mismatch, or the use of a dominant Lo-Hi type process cycle at the beginning of the thermal processing. When oxygen precipitates intersect the wafer surface, it can cause oxide defects and poor breakdown characteristics.

The reliability effect of thin gate oxides grown on a silicon surface containing a high density of oxygen precipitates and bulk stacking faults induced by heat treatment has been investigated [141]. Both voltage-ramp and time dependent dielectric breakdown (TDDB) results indicate that oxygen precipitates cause significant gate oxide degradation. Figure 50 shows the defect density (D_0) extracted from the voltage measurements, illustrating the "heat treated" wafers have larger D_0 than "normal" bulk wafer and p/p^+ epitaxy for $V > 5$ volt.

Figure 55(d) represents a situation where the wafer's oxygen content is below the threshold of oxygen precipitation for the thermal cycles used and no precipitation is formed. However, some precipitation can be triggered near the wafer back surface for gettering by pre-processing wafer backside polysilicon film deposition via mechanism discussed above. In the era of sub-0.5 μm technology using 200 mm diameter-wafers, there has been a trend to use lower oxygen concentrations [142] for "soft internal gettering", with targeted bulk precipitation density to be about 5×10^5 per cm^3 and denuded zone width of approximately 15 μm . The main advantage of using low oxygen silicon is the decrease in the possibility of microdefect formation near the wafer's active region. Microdefects are critical in memory devices. Furthermore, the possibility of wafer warpage and slip dislocation generation induced by over-precipitation of oxygen is also reduced. It is believed that the trend for lower oxygen is likely to continue in view of the advancements made in IC contamination control in IC fabrication lines; class one or better environments, cleaner process equipment, and improvements in the purity of process chemicals and materials. The potential for heavy metal contamination is accordingly reduced and so is the IC's dependence on internal gettering by oxygen precipitates. When additional gettering capability is needed, an external gettering method may be added, such as backside polysilicon deposition.

The foregoing discussions and examples on silicon processing of both epitaxial and bulk wafers illustrate the importance of oxygen control in silicon, whether or not precipitation gettering is wanted. Uncontrolled precipitation can result in precipitate-induced defects during epitaxial growth, electrically sensitive defects in the device active regions and inferior gate oxides. In these situations, the harmful effects of oxygen can outweigh its beneficial aspects. In the coming era of 300 mm, 0.18 μm IC fabrication, it is essential to "engineer" oxygen precipitation to occur at the optimal locations and at the right time through tight

control of wafer oxygen concentration and/or strategically tailoring of the thermal processes. Alternatively, one can positively avoid the ill effects of oxygen precipitates by utilizing silicon with a sufficiently low oxygen concentration for "soft" or no precipitation. In either case, the control of oxygen with a narrow concentration distribution and minimization of growth-in microdefects in silicon are necessary.

VIII. SUMMARY

Modern Ultra Large Scale Integration (ULSI) ICs, fabricated with design rules approaching 100 nm, depend on the availability of highly perfect silicon single crystals, which are prepared exclusively by the CZ crystal growth method. The silicon material prepared today, polished wafer or epitaxial wafer, must meet the challenges imposed by the stringent requirements of the starting materials for current and future design rule generations, as guide by the Starting Materials Road Map of the National Technology Roadmap for Semiconductors (NTRS).

In parallel with the design rule decrease, both chip size and circuit complexity increase. There is a continued push for increased wafer diameter in order to reduce IC manufacturing cost. In the up-scaling of the wafer diameter, in the 300–450 mm range, the most significant technical challenges are in the crystal growth. The major issues include crystal weight support, reduced growth rate and growing long crystals from "ultra-large" charge capacity and continuous growth. The dislocation-free as-grown yield will dominate the cost of manufacturing 300–450 mm diameter wafers. Furthermore, the grown-in microdefects have vital impacts on the GOI and proper function of memory devices. The microdefect-free crystal growth processes (i.e. for crystals free of D and A defects) present major challenges and require continued efforts in research and development. To circumvent the microdefect problem in polished wafers, there is an increasing trend to use epitaxial wafers, either p^-/p^+ or p^-/p^- for IC fabrication. MCZ is the growth method for large-capacity, large diameter silicon crystals growth for reducing thermal convection and better control of oxygen. Consequently, the interstitial oxygen contents of the large diameter silicon (≥ 300 mm) are generally lower than the smaller diameter silicon grown with normal CZ. Lower oxygen content makes it difficult, if not impossible, to exercise internal gettering by oxygen precipitation under the low

thermal budget of sub-0.18 μm design rule device processing.

As the design rule reduces, the requirements for wafer mechanical dimension control, particulate, as well as metal contamination, become more stringent. To achieve improved flatness for sub-0.18 μm IC fabrication, new techniques in wafer shaping and polishing have been implemented, these include surface grinding in conjunction with reduced chemical etching, double-side polishing and plasma assisted chemical etching. Finally, for improved wafer contamination control, purer starting raw material, process chemicals, proper equipment maintenance and wafer handling are essential.

REFERENCES

1. WG Pfann. *Trans Am Inst Min Metall Eng* 194: 747-753, 1952.
2. HC Theuerer. 1962, US Patent 3, 060, 123.
3. K Keller, A Muhlbauer. *Floating zone silicon*. New York: Marcel Dekker, 1981.
4. JM Meese. ed. *Neutron transmutation doping in semiconductors*. New York: Plenum, 1979.
5. M Bullis. In: F Shimura. ed. *Oxygen in silicon*. New York: Academic Press, 1994, pp 121.
6. B Leroy, C Plougonven. *J Electrochem Soc* 127: 961-970, 1980.
7. S Takasu, H Otsuka, N Yoshihiro, T Oku. *Jpn J Appl Phys Suppl* 20(1): 25, 1981.
8. JR Patel, AR Chaudhuri. *J Appl Phys* 33: 2223, 1963.
9. I Yonenaga, K Sumino, K Hoshi. *J Appl Phys* 56: 2346-2350, 1984.
10. K Sumino, I Yonenaga, A Yusa. *Jpn J Appl Phys* 19: L763, 1980.
11. T Abe, K Kikuchi, S Shirai, S Muraoka. In: HR Huff, RJ Kriegler, Y Takeishi. eds. *Semiconductor Silicon 1981*. New Jersey: Electrochem Soc Princeton, 1981, pp 54-71.
12. L Jastrzebski, GW Cullen, R Soydan, G Harbeke, J Lagowski, S Vecrumba, WN Herry. *J Electrochem Soc* 134: 466, 1987.
13. J Czochralski. *Metalle Z Phys Chem* 92: 219-221, 1918.
14. GK Teal, JB Little. *Phys Rev* 78: 647, 1950.
15. T Abe. In: NG Einspruch, HR Huff. eds. *VLSI electronics microstructure science*. New York: Academic Press, Vol. 12, pp 3-61.
16. WC Dash. *J Appl Phys* 29: 736-737, 1958.
17. W Lin, DW Hill. In: *Silicon processing*, ASTM STP 804, 1983, pp 24-38.
18. W Lin, KE Benson. *Annual review of materials science*, 17: 273-298, 1987.
19. E Billig. *Proc R Soc London Ser A* 235: 37-55, 1956.
20. LH Van Vleck. *Elements of materials science and engineering*. 3rd ed. Reading, MA: Addison-Wesley, 1975.
21. AS Jordan, R Caruso, AR Von Neida. *Bell Syst Tech J* 59: 593-673, 1980.
22. WG Pfann. *Zone Melting*. 2nd ed. New York: John Wiley & Son, 1966.
23. KE Benson, W Lin, EP Martin. In: HR Huff, RJ Kriegler, Y Takeishi. eds. *Semiconductor silicon 1981*. New Jersey: Electrochem Soc Princeton, 1981, p 33-48.
24. G Fiegl. *Solid State Technol.* August, 1983, pp 121-131.
25. RE Lorenzini, A Iwata, K Lorenz. *US Patent* 4, 036, 595, 1977.
26. RA Craven, WE Baily, JW Moody, RJ Falster, LW Shive. *Mat Res Soc Symp Proc* 59: 359, 1986.
27. FA Trumbore. *Bell Sys Tech J* 39: 205, 1960.
28. KG Barraclough, PJ Ward. *Electrochem Soc Meet Ext Abstr.* 167th 1983, p 474.
29. D Gilmore, T Arahori, M Ito, H Murakami, SI Miki. In: CL Claeys, P Raj-Choudhury, P Stallhofer, JE Maurits. eds. *High purity silicon IV*. New Jersey: Electrochem. Soc. Pennington, 1996, pp 102-114.
30. H Kodera. *Jpn J Appl Phys* 2: 212, 1963.
31. JA Burton, RC Prim, WP Slichter. *J Chem Phys* 21: 1987-1996, 1953.
32. WG Cochran. *Proc Cambridge Phil Soc* 30: 365, 1934.
33. JR Carruthers, AF Witt, RE Reusser. In: HR Huff, E Sirtl. eds. *Semiconductor silicon 1977*. New Jersey: Electrochem Soc Princeton, 1977, pp 61-71.
34. JR Carruthers. *J Electrochem Soc* 114: 959, 1967.
35. T Carlberg, TB King, AF Witt. *J Electrochem Soc* 129: 189-, 1982.
36. K Hoshikawa, H Hirata, H Nakanishi, K Ikuta. In: HR Huff, E Sirtl. eds. *Semiconductor silicon 1981*. New Jersey: Electrochem Soc Princeton, 1981, pp 101-.
37. JR Carruthers, K Nassau. *J Appl Phys* 39: 5205-5214, 1968.
38. K Kakimoto, M Eguchi, H Watanabe, T Hibiya. *J Cryst Growth* 88: 356-, 1988.
39. K Kakimoto, M Eguchi, H Watanabe, T Hibiya. *J Cryst Growth* 89: 412-, 1989.
40. JW Moody. In: HR Huff, T Abe, B Kolbeson. eds. *Semiconductor silicon 1986*. New Jersey: Electrochem Soc Pennington, 1981, pp 100-116.
41. H Tsuya, Y Kondo, M Kauamori. *Jpn J Appl Phys* 22: L16, 1983.
42. AS Oates, W Lin. *Appl Phys Lett* 53: 2659-2660, 1988.
43. AS Oates, W Lin. *J Cryst Growth* 89: 117-123, 1988.
44. H Walitzki, HJ Roth, J Refflw, S Pahlke, M Blatte. In: HR Huff, T Abe, B Kolbeson. eds. *Semiconductor silicon 1986*. New Jersey: Electrochem Soc Pennington, 1986, pp 86-99.

45. T Nozaki, Y Itoh, T Masui, T Abe. *J Appl Phys* 59: 2562-, 1986.
46. Y Itoh, T Nozaki, T Masui, T Abe. *Proc 31st Appl Phys Conf. Kawasaki, Japan, 1984*, pp 609-.
47. F Shimura, W Dyson, JW Moody, RS Hockett. In: MW Bullies, S Broydo. eds. *VLSI science and technology 1985*. New Jersey: Electrochem Soc Pennington, 1985, pp 507-516.
48. KG Barraclough, RW Series. In: R Reif, ed. *Reduced temp proc for VLSI*. New Jersey: Electrochem Soc. Pennington, 1986, pp 452-463.
49. LS Darken, RW Gurry. *Physical metallurgy of metals*. New York: McGraw Hill, 1953, pp 287-294.
50. W Kaiser, PH Keck, CF Lange. *Phys Rev.* 101: 1264, 1956.
51. T Yatsurugi, N Akiyama, Y Endo, T Nozaki. *J Electrochem Soc* 120: 975-979, 1973.
52. W Lin, DW Hill. *J Appl Phys* 54: 1082-1085, 1983.
53. W Lin, M Stavola. *J Electrochem Soc* 132: 1412-1416, 1985.
54. H Harada, T Itoh, N Ozawa, T Abe. In: MW Bullies, S Broydo. eds. *VLSI science and technology 1985*. New Jersey: Electrochem Soc Pennington, 1985, pp 526-535.
55. E Iino, K Takano, I Fusegawa, H Yamagishi. In: HR Huff, W Bergholz, K Sumino. eds. *Semiconductor silicon 1994*. New Jersey: Electrochem Soc Pennington, 1994, pp 148-155.
56. W Lin. In: M Umeno. ed. *Proc. of 2nd Inter Symp on Adv Science of Silicon Materials*. Kono, 1996, pp 288-293.
57. F Shimura. *Semiconductor silicon technology*, Academic Press, 1989, p 258.
58. H Yamagishi, I Fusegawa, K Takano, E Iino. In: HR Huff, W Bergholz, K Sumino. eds. *Semiconductor silicon 1994*. New Jersey: Electrochem Soc Pennington, 1994, pp 124-135.
59. J-G Park, S-P Choi, GS Lee, Y-K Jeong, Y-S Kwak, C-K Shin, S Han, WI Smith, P Mascher. In: CR Helms, BE Deals. eds. *The physics and chemistry of SiO₂ and the Si-SiO₂ interface II*. Plenum Publishing Co, 1993, pp 168-179.
60. K Nakajima, J Furukawa, H Furuya, T Shingyouji. In: HR Huff, W Bergholz, K Sumino. eds. *Semiconductor Silicon 1994*. New Jersey: Electrochem Soc Pennington, 1994, pp 168-179.
61. H Nishikawa, Y Komatsu, M Hourai, M Sano, T Shigematsu. In: *Proceedings of the 45th symposium on semiconductor and integrated circuits technology*, Jpn Electrochem Soc 1993, p 100.
62. BPR Marioton, U Gosele. *J Appl Phys* 63:4661, 1988.
63. WJ Patrick, SJ Scilla, WA Westdrop. *US Patent* 4,010,064.
64. F Secco d'Aragona. 1985, *US Patent* 4, 545, 849.
65. W Lin, CW Pearce. *J Appl Phys* 51: 5540-5543, 1980.
66. M Watanabe, T Usami, H Muraoka, S Matsuo, Y Imanishi, H Nagashima. In: HR Huff, RJ Kriegler, T Takeishi. eds. *Semiconductor silicon 1981*. New Jersey: Electrochem Soc Pennington, 1981, pp 126-137.
67. M Watanabe. *ASTM Symp on Semiconductor processing, Abstract*, San Jose, 1984.
68. HP Utech, MC Flemings. *J Appl Phys* 37: 2021, 1966.
69. AF Witt, CJ Herman, HC Gatos. *J Mater Sci* 5: 822, 1970.
70. S Chandrasekhar. *Philos Mag* [7] 43: 501-, 1952.
71. K Hoshi, T Suzuki, Y Okubo, N Isawa. *Electrochem Soc Meet Ext Abstr.* 157th, 1980, p 811.
72. S Takasu, S Takahasi, M Ohwa, O Suzuki, T Higuchi. In Huff HR, Barraclough KG, Chikawa J-i. eds. *Semiconductor silicon 1990*. New Jersey: Electrochem Soc Pennington, 1990, pp 45-57.
73. RW Series, KG Barraclough, DTJ Hurle, GJ Rae. *Electrochem Soc Meet Ext Abstr* 167th, p 396.
74. TT Braggins, RN Thomas. *Electrochem Soc Meet Ext Abstr.* 169th, 1986, p 351.
75. K Hoshi, N Isawa, T Suzuki, Y Okubo. *J Electrochem Soc* 132: 693-700, 1985.
76. M Ohwa, T Higuchi, E Toji, M Watanabe, K Homma, S Takaku. In: HR Huff, T Abe, B Kolbesen. eds. *Semiconductor silicon 1986*. New Jersey: Electrochem Soc Pennington, 1986, pp 117-128.
77. K Hoshi, N Isawa, T Suzuki. *ULSI*, August 1986, p 51.
78. Series, KG Barraclough, DTJ Hurle, DS Kemp, GJ Rae. *Electrochem Soc Meet Ext Abstr.* 167th, 1985, p 396.
79. TT Braggins, RN Thomas. *Electrochem Soc Meet Ext Abstr.* 169th, 1986, p 354.
80. H Hirata, K Hoshikawa. *J Cryst Growth* 96: 47-755, 1989.
81. H Hirata, K Hoshikawa. *J Crystal Growth*: 98:777-781, 1989.
82. RW Series. *J Cryst Growth* 97:92-98, 1989.
83. K Hoshikawa, H Hirata. In: M Umeno. ed. *Proc of 2nd Inter Symp of Adv Science of Silicon Mater* Kono. 1996, pp 85-94.
84. AJR de Kock. In: H Huff, E Sirtl. eds. *Semiconductor silicon 1977*. New Jersey: Electrochem Soc. Princeton, 1977, pp 508-520.
85. RB Marcus. In: SM Sze. ed. *VLSI Technology*. New York: McGraw-Hill, 1983, p 543.
86. AJR de Kock, WM van de Wijgert. *J Cryst Growth* 49: 719, 1980.
87. J Ryuta, E Morita, T Tanak, Y Shimanuki. *J Appl Phys* 29: L1947, 1990.
88. H Yamagishi, I Fusegawa, N Fujimaki, M Katayama. *Semicond Sci & Techn* 7: A135, 1992.
89. P Gall, JP Fillard, J Bonnafe, T Rakotomavo, H Rufer, H Schwenk. In: K Sumino. ed. *Defect Control in Semiconductors*. Amsterdam: North Holland, 1990, pp 255.

90. S Umeno, M Okui, M Hourai, M Sano, H Tsuya. *Jpn J Appl Phys.* 36: L591, 1997.
91. W von Ammon, E Dornberger, H Oelkrug, H Weidner. *J Cryst Growth* 151: 273-, 1995.
92. E Dornberger, W von Ammon. *J Electrochem Soc* 143:1648, 1996.
93. VV Voronkov. *J Crystal Growth*, 59: 625, 1982.
94. VV Voronkov, R Falster, JC Holzer. In: BO Kolbeson, P Stallhofer, C Claeys, F Tardiff. eds. *Crystalline Defects and Contamination: Their Impact and Control in Device Manufacturing II*. New Jersey: Electrochem Soc. Pennington, 1997, p 3.
95. W von Ammon. In: M Umeno, ed. *Proceeding of 2nd Int Symp on Adv Sci and Tech of Silicon Materials*. Kono, 1996, pp 233-241.
96. M Suhren, M Graf, U Lambert, P Wagner. In: CL Claeys, P Rai-Choudhary, P Stallhofer, JE Mauritis. eds. *High Purity Silicon IV*. New Jersey: Electrochem Soc. Pennington, 1996, pp 132-139.
97. P Wagner, D Graf, R Schmolke, M Suhren. In: M Umeno, ed. *Proc of 2nd Intern Symp of Adv Sci and Tech of Silicon Materials*. Kono, 1996, pp 101-106.
98. W Wijaranakula, S Archer. *J Electrochem Soc* 143: 1636, 1996.
99. JG Park, H Kirk, C Cho, HK Lee, CS Lee, GA Rozgonyi. In: HR Huff, W Bergholz, K Sumino. eds. *Semiconductor Silicon 1994*. New Jersey: Electrochem Soc Pennington, 1994, pp 370-378.
100. M Isumi, H Akiya, T Ueki, M Tomita, M Yamawaki. *J Appl Phys* 78:5984, 1995.
101. N Ueki, M Isumi, T Takeda. *Int Conf On Solid State Devices and Materials*, Yokohama, LA-1, 1996, pp 862.
102. M Isumi, H Akiya, M Tomita, T Ueki, M Yamawaki. In: M Umeno, ed. *Proc of 2nd Int Symp on Adv Sci and Tech of Silicon Material*. Kono, 1996, pp 270-275.
103. H Takeno, M Kato, Y Kitagawara. In: M Umeno, ed. *Proc of 2nd Int Symp on Adv Sci and Tech of Silicon Materials*. Kono, 1996, pp 294-301.
104. D Dornberger, W von Ammon, D Graf, U Lambert, A Miller, H Oelkrug, A Ehlert. In: CL Claeys, P Rai-Choudhury, P Stallhofer, JE Mauritis. eds. *High Purity Silicon IV*. New Jersey: Electrochem Soc Pennington, 1996, pp 140-146.
105. M Hourai, T Nagashima, E Kajita, S Miki, T Shigematsu, M Okui. *J Electrochem Soc* 142: 3193, 1995.
106. K Tanabashi, N Inoue, Y Mizokawa. In: M Umeno, ed. *Proc of 2nd Int Symp on Adv Sci and Tech of Silicon Materials*. Kono, 1996, pp 51-58.
107. KM Kim, P Smetana. *J Cryst Growth* 100:527, 1990.
108. H Yamagishi, H Minami, M Imai, T Misawa, K Takada. In: M Umeno, ed. *Proc 2nd Intern Symp on Adv Tech of Silicon Materials*. 1996, p 59.
109. HD Chiou, TYT Lee, S Teng. *J Electrochem Soc* 144:2881-1886, 1997.
110. H Kubota, M Numano, T Amai, M Miyashita, S Samata, Y Matsushita. In: HR Huff, W Bergholz, K Sumino. eds. *Semiconductor silicon 1994*. New Jersey: Electrochem Soc Pennington, 1994, pp 225-231.
111. Shimizu, Y Sugino, N Suzuki, S Kiyota, K Nagasawa, M Fujita, K Takeda, S Isomae. *Jpn J Appl Phys* 36:2565-2570, 1997.
112. Y Araï, M Kida, N Ono, N Abe, N Machida, H Furuya, K Sahira. In: H Huff, W Bergholz, K Sumino. eds. *Semiconductor silicon 1994*. New Jersey: Electrochem Soc Pennington, 1994, pp 180-191.
113. Y Shiraishi, S Kurosaka, M Imai. *J Cryst Growth* 166: 685-688, 1996.
114. SEMI International standards, materials volume. Mountain View, CA: SEMI International, 1994.
115. Robbins, B Schwartz. *J Electrochem Soc* 107: 108-111, 1960.
116. JA Moreland. In: NG Einspruch, HR Huff, eds. *VLSI Electronic microstructure science*, Vol 12. New York: Academic Press, 1985, pp 63-87.
117. D Bollinger, CB Zarowin. In: *Advances in fabrication and metrology for optical and large optics*, Vol. 966. Bellingham, WA: Soc of Photo-Optical Instrumentation Engineers. 1988, pp 82-90.
118. W Kern, DA Puotinen. *RCA Rev* 31: 187-206, 1970.
119. W Kern. *Semicond International*, April 1984, pp 94-99.
120. RC Sun, JT Clemens. In: *Proc IEEE Int Electron Device Meet*, Washington, DC 1977, pp 254.
121. JT Clemens, DA Metha, JT Nelson, CW Pearce, RC Sun. US Patent No. 4216489.
122. JW Slotboom, HA Harwig, MJM Pelgrom. In: *Proc IEEE Int Electron Device Meet*, Washington, DC 1981, pp 667.
123. Aoki, Itakura T, Sasaki N. *J Appl Phys* 66: 2709-2711, 1995.
124. JL Benton, PA Stolk, DJ Eaglesham, DC Jacobson, JY Cheng, JM Poate, NT Ha, TE Haynes, SM Myers. *J Appl Phys* 80: 3275-3284, 1996.
125. FH Horn. *Phys Rev* 97:1521, 1955.
126. W Lin, DW Hill, CL Paulnack, MJ Kelly, KE Benson, RR Bushert. In: M Bullis. ed. *Defect in Silicon II*. New Jersey: Electrochem Soc Pennington, 1991, pp 161.
127. J Washburn, G Thomas, JH Queisser. *J Appl Phys* 42: 2612, 1964.
128. J Weertman, JR Weertman. *Elementary Dislocation Theory*, MacMillan, New York: 1965, p 54.
129. See for example, K Wada, N Inoue. In: HR Huff, ed. *Semiconductor silicon 1986*. New Jersey: Electrochem Soc. Pennington, 1986, p 778.
130. PM Petroff, AJR DeKock. *J Cryst Growth* 30:117, 1975.
131. W Lin, AS Oates. *Appl Phys Lett* 56: 128, 1990.

132. ASTM Standard F1239-89.
133. R Swaroop, N Kim, W Lin, M Bullis, L Shive, A Rice, E Castel, M Crist. *Solid State Technology*, March 1987, p 85.
134. H Shirai, A Yamaguchi, F Shimura. *Appl Phys Lett* 54: 1748, 1989.
135. AR de Kock, WM van de Wiggert. *J Cryst Growth* 49: 718, 1980.
136. AR de Kock, WM van de Wiggert. *Appl Phys Lett* 38: 888, 1981.
137. W Wijaranakula, J Matlock, H Mollenkopf. In: D Gupta. ed. *Semiconductor fabrication*, ASTM STP 990. Philadelphia: ASTM, 1989, p 371.
138. CW Pearce. *Mat Res Soc Symp Proc* 36:231, 1985.
139. W Linn. In: HR Huff, KG Barraclough, J-i Chikawa. eds. *Semiconductor silicon 1990*. New Jersey: Electrochem Soc Pennington, 1990, pp 569-584.
140. W Lin, KG Moerschel. In: R Reif. ed. *Reduced temperature processing for VLSI*. New Jersey: Electrochem Soc Pennington, 1986, p 438.
141. KC Boyko, RL Feiller, W Lin, unpublished.
142. M Watanabe. *Solid state technology*, April, 1991, p 133.
143. W Lin. In: F Shimura. ed. *Oxygen in silicon*. Academic Press, 1994, pp 1-52.

Ion Implantation

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I. INTRODUCTION

Over the last two decades ion implantation has played a steadily increasing role in production processes for leading-edge integrated circuit fabrication, due to its flexibility in the selection of dopant species, their spatial location within the device, and in subtle control of the concentration profile. This flexibility allows additional degrees of freedom in processing, as well as easy adaptation to the changes required by other process advances, enabling rapid introduction of new integrated process technology. Significant advances in implanter hardware technology have allowed ion implantation to keep pace with the rigid requirements for fabricating 180 nm devices. These include advances in beam current capability, dose control, energy range, energy purity, wafer charging control, beam angle control, and reduction of metallic and particulate contamination.

II. ION IMPLANTATION SCIENCE

A. An Overview of Ion Implant Physics and Materials Science

Ion implantation is a process whereby energetic dopant ions are made to impinge on a silicon or other target, resulting in the penetration of these ions below the target surface and thereby giving rise to controlled, predictable dopant distributions. Low implant energies

produce dopant distributions near the surface such as are required for MOS source and drain regions, or bipolar emitter regions, and high energies produce deeply implanted dopant profiles such as are required for CMOS retrograde wells, and buried layers. The provision of wafer cooling during implant allows the use of photoresist masks to laterally control the location of dopant regions, an important feature for the production of CMOS devices. Similarly, topographical features of the device, such as a gate stack, may be used to effect implant masking, thereby allowing for the production of cost- and yield-effective, self-aligned doping regions.

A quantitative understanding of the atomic interactions between these energetic ions, target atoms and masking layers is required for the prediction of the depth and lateral doping profiles produced by the ion implantation process. These interactions depend on the relative mass of ion and target atom, the ion energy, the ion angle of incidence, and the target crystal orientation and perfection. The implanted ions cover a large atomic mass range, including species such as boron, phosphorus, arsenic, indium and antimony, and a wide range of implantation energies from <2 keV to >3 MeV. Ion implantation equipment allows ion incidence angle ranges from 0° (normal incidence) to $\approx 60^\circ$.

The ion-atom interactions which occur during ion implantation produce collateral damage, which can take the form of a non-equilibrium excess of vacant lattice sites (vacancies) and interstitial atoms

(interstitials), vacancy clusters, interstitial clusters, dopant-interstitial and dopant-vacancy clusters, and locally amorphized regions of the crystalline silicon target. Iso-valent ions such as Si, Ge, or Sn are sometimes implanted to intentionally take advantage of this collateral damage. The annealing of this damage requires that the implanted target receive a subsequent heat treatment. The as-implanted defect configurations evolve during post-implant thermal processing, giving rise to transient enhanced dopant diffusion, and the formation of relatively stable dislocation arrays, which if present in active device regions can lead to degradation of electrical performance. An understanding of all of these phenomena is therefore crucial to the design of the implant recipe, and to the post-implant thermal treatment. The following reviews the underlying physics and materials science needed for such understanding.

B. Electronic and Nuclear Stopping and Collision Cascades

It is now well established that energetic ion stopping occurs through interactions between the electrons of the target and projectile ion (electronic stopping), and through atomic collisions (nuclear stopping) between the projectile and target atoms. These interactions slow the energetic ion until it eventually comes to a halt. The statistical distribution of the stopping points for many ions (typically 10^{11} to 10^{15} ions/cm² are implanted) constitutes a concentration versus depth profile. The prediction of such doping profiles is a central issue that underlies the interest in the stopping process. Stopping is characterized by an energy loss per unit length of travel, and is described by the following equation:

$$(dE/dx)_{\text{Total}} = S_n(E) + S_e(E) \quad (1)$$

where $S_n(E)$ and $S_e(E)$ are respectively the nuclear and electronic stopping components. Both stopping components are a function of the ion energy, atomic number, and mass, and also the target atomic number, mass, and packing density. The ion range results from the apportionment of the incident projectile energy over these stopping components.

Electronic stopping results in excited target electronic states that decay without producing atomic displacements. On the other hand, nuclear stopping results from momentum and energy transfer between the projectile and target atoms, which may result in the generation of energetic knock-on target atoms,

which may then produce secondary, tertiary and higher order knock-on displacements. The resulting damage chain, known as a collision cascade, leaves behind a trail of vacant lattice sites, along with implanted atoms and displaced target atoms in substitutional and interstitial positions. The collision-induced defects are predominantly produced as vacancy-interstitial pairs known as Frenkel defects, but can interact on the time-scale of the collision cascade (10^{-11} s) to recombine or agglomerate into more complex defect configurations. Also because of the initial momentum of the impinging projectile ions, the centroid of the interstitial distribution lies deeper in the target than the vacancy distribution.

1. Electronic Stopping

Electronic stopping is similar to the drag on a particle in a viscous medium, and involves excitation of the electrons of both target and projectile. It may also involve electron capture or loss from the bound states of the moving projectile ion. These processes determine the charge state and effective electronic stopping power of the ion as it moves through the solid. At high velocities, $v \gg Z_1 v_0$ (where Z_1 is the ion atomic number, and v_0 , the Bohr velocity = 2.2×10^8 cm/sec) the ion is stripped of its bound electrons. Here stopping can be calculated using the Bethe-Bloch [2,3] theory. Such stopping is rarely encountered in ion implantation where the energy ranges used predicate that even the lightest ions typically have velocities in the range $\sim 0.1 v_0$ – $5 v_0$. At low ion velocities ($v < v_0$) such as are typically encountered in the energy range of 2–400 keV, the projectile ions are essentially neutral and stopping is proportional to the ion velocity [4] giving the relationship:

$$S_e(E) = k_e(E)^{1/2} \quad (2)$$

The proportionality constant is a periodic function of the atomic number of the projectile ion.

Equation (2) is no longer valid when the projectile velocity approaches the average orbital electron velocity (given by $v \approx Z^{2/3} v_0$), when the projectile can become partially stripped of some electrons.

Here, the stopping power is determined through proportion with the known stopping of a proton in the target at the same velocity through a proportion constant, known as the stopping power effective charge, Z_1^* [5]:

$$(Z_1^*)^2 = S_{Z1}/S_p \quad (3)$$

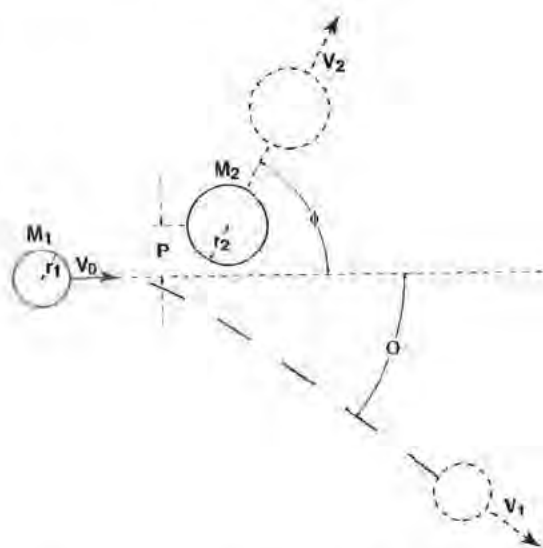


Figure 1 Schematic illustration of a binary collision between a projectile having mass M_1 and initial velocity v_0 and a stationary target atom having mass M_2 .

where S_{Z1} is the desired stopping power of the partially stripped ion, S_p is the proton stopping power. A knowledge of Z_1^* therefore allows for the calculation of the ion stopping power from published values of the proton stopping power. Z_1^* in turn depends on the degree of ionization of the projectile, and as well on the degree of inter-penetration of the target electrons, and the remaining bound electrons moving with the projectile. Z_1^* is therefore greater in magnitude than the degree of ionization. The solution of the stopping problem therefore involves first a determination of the velocity dependent degree of ionization, and then from this the calculation of the stopping power effective charge Z_1^* . Reference [6] summarizes the computations used in these determinations, including the methods utilized by Ziegler, Biersak, and Littmark for inclusion in the TRIM Monte-Carlo program for the determination of implantation profiles [7]. These issues are important for ion implantation of boron, phosphorus, and arsenic in the range of ≈ 600 –4000 keV, where projectiles have velocities in the range between v_0 and $5 v_0$. Reference [8] gives a recent review of electronic stopping for all ion energy ranges.

2. Nuclear Stopping

Most models of nuclear stopping treat the problem as a binary collision event between the target and projectile particles. The presence of the other atoms in the crystal

lattice is accounted for through the interaction potential between target and projectile ions, a displacement energy, a binding energy, and the above described electronic stopping processes. This approach is valid over a broad range of ion energies. At low energies (<5 keV) the approach fails and a more general Molecular Dynamics scheme for broadly calculating the interactions with the ion and an ensemble of nearby target atoms is required. These methods are extremely computer intensive. Figure 1 depicts the binary collision event that results in nuclear stopping. Here, a projectile ion of mass M_1 approaches the target atom of mass M_2 . The path of the projectile ion is offset from the center of the target atom by the impact parameter, p . A value of $p=0$ signifies a head-on collision, whereas non-zero values of p signify a glancing blow. For p values greater than $r_1 + r_2$ of the respective atomic radii, the projectile ion "misses" the target atom and no collision ensues. The projectile ion approaches the target atom with velocity V_0 , and after colliding moves off with velocity V_1 , deflected through an angle θ with respect to its initial direction. The struck target atom acquires velocity V_2 at an angle ϕ , with respect to the direction of the incoming projectile. Conservation of energy requires that the initial kinetic energy of the projectile be greater than or equal to the post-impact kinetic energy, and that therefore $V_1 \leq V_0$. The energy loss of the projectile is directly related to the deflection angle, which in turn is related to the impact parameter and the interaction potential which arises as the projectile particle approaches the target particle, and interactions ensue between the atomic nuclei and the bound electrons of particle and target. The determination of nuclear stopping therefore requires that this interaction potential be known and related to the variety of deflection angles representative of the random values assumed by the impact parameter.

The relationship between energy transfer and deflection angle is most conveniently determined using a center of mass coordinate system [9–12]. The determination of the interaction potential requires that the screening effect of the electrons surrounding the target and projectile nuclei be accounted for, and as well that the quantum mechanical interactions between their overlapping electron clouds be determined. Various approximations of these interactions have been attempted, the most accurate of which involve Hartree-Fock models of the atom. Such calculations are computer intensive, and are used primarily as benchmarks to establish the accuracy of simpler approaches. Reference [7] reviews the status of these

theoretical approximations and gives numerically fitted functions which best describe these interaction potentials. The numerically fitted functions are known as ZBL potentials, which are used in several current Monte Carlo programs used to simulate the implant process. Currently, these interaction potentials have been refined to the point where predictions agree within several percent of experimentally determined values.

C. Models of Implantation Profiles Prediction

Lindhard, Sharff, and Schiott [13] combined the effects of nuclear and electronic stopping to arrive at an analytical means of predicting the statistical distribution of large numbers of implanted ions. Their efforts yielded a general analytical solution to Eq. (1), which assumed the ion velocity dependent electron stopping described by Eq. (2), and nuclear interaction potentials derived from the Thomas-Fermi model of the atom. These efforts yielded mean range, R , and standard deviation of ranges (called straggle, ΔR_p). The mean range determination also allowed for the determination of the mean *projected* range R_p , which is the mean distance below the target surface in the direction determined by the initial incidence trajectory of the projectile ion. The final ion distribution profile was then determined by assuming the distribution to be Gaussian with the mean value, R_p , and Standard deviation, ΔR_p . The work is applicable only to amorphous targets, and does not yield results of sufficient accuracy for semiconductor device simulation, but was crucial to advancing stopping physics state of knowledge. However, it is still common practice to approximate implant profiles using the Gaussian approximation, using R_p and ΔR_p determined by alternate means such as are available from the TRIM program. The Gaussian depth-concentration profile is determined from Eq. (4):

$$n(x) = \frac{\phi}{\sqrt{2\pi}\Delta R_p} \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right] \quad (4)$$

where ϕ is the important dose in atoms/cm². The peak concentration for such a distribution is given by Eq. (5):

$$n(x = R_p) = \frac{\phi}{\sqrt{2\pi}\Delta R_p} \cong \frac{0.4\phi}{\Delta R_p} \quad (5)$$

Current methods of profile prediction makes use of Monte Carlo programs which are computer intensive,

and with the appropriate selection of electron and nuclear stopping algorithms, can yield very accurate results. The results of these models are then used to describe the implant profile as a statistical distribution function. Since the Gaussian distribution is described by only two moments, the mean and variance, it is usually inadequate for such fitting. Accurate profile description requires that four statistical moments be used. These are the mean range, variance, skewness, and kurtosis. The Pearson distribution function has demonstrated suitable fitting [14] for amorphous targets. In crystalline targets, it has been found that ion channeling, described below, can result in a bi-modal profile, the fitting of which requires a Dual Pearson model [15].

Two Monte Carlo simulation programs are readily available and useful for the computationally intensive simulation of the implant process. These models are also useful in providing significant insight into the physics of the implant process. These are the programs TRIM, available from IBM [16], and UT-Marlowe, available from the University of Texas [17]. Both programs use the binary collision approximation to describe nuclear stopping, and both use the ZBL approximation [7] to describe the interatomic potentials. TRIM is very convenient in that it will operate on a personal computer in the Windows® operating environment, and provides tabulated outputs which can readily be incorporated into spreadsheets for numerical analysis and graphing. TRIM is limited to "amorphous" target materials. UT-Marlowe requires a workstation platform and intrinsically accommodates the single crystal target environment. UT-Marlowe continues to receive the support needed to evolve and adapt the program to the ever-expanding species, energy, dose, and angle regime encountered with modern ion implantation practice. The UT-Marlowe program is also able to model ion implant damage [18].

D. Amorphous versus Crystalline Targets and Ion Channeling

The main difference between amorphous and single crystal silicon targets resides in the fact that in an amorphous target, the atoms are assumed to be randomly distributed in a way which conforms to the overall packing density, local atomic coordination, and atom size constraints, whereas in single crystal silicon the atoms are packed in a long range, ordered, diamond cubic arrangement. The result of this symmetry is that the crystal target has "channels", or open

directions where an ion can travel long distances without encountering a target atom. In silicon, the $\langle 100 \rangle$, $\langle 111 \rangle$, and $\langle 110 \rangle$ directions provide such paths. In addition, there are highly symmetric planar directions which also provide ion channeling opportunities. An appropriately oriented ion beam will either be directly aligned along such channel directions, or will allow a high fraction of incident ions to be scattered into a channel. Channeled ions will penetrate deeply into the silicon since overall stopping is determined primarily by the electronic stopping component, and in the mid-energy regime, ion penetration will scale with the ion velocity as predicted in Eq. (2). In addition, the propensity for ions to be scattered into, and remain captured in a channel is a function of incident angle, ion mass, and energy [19]. Ion implant practice usually orients the silicon wafers to avoid such channels since for channel oriented wafers, slight differences in beam orientation across the wafer result in radically different implant profiles. It has been shown that channel avoidance requires that the wafer be rotated about two axis with respect to the beam direction [20], and ion implantation equipment is configured to provide such wafer "Tilt" and "Twist". In general, wafers that are appropriately oriented by proper choice of tilt and twist angles will behave essentially as amorphous targets. It is important to note, however, that at lower energies the angle range for acceptance into a channel broadens considerably, thereby allowing a significant fraction of incident ions to either directly enter a channel, or be scattered into a channel, making the amorphous target assumption increasingly risky.

E. Crystal Damage and Amorphization

It has been observed that crystalline target materials that are exposed to energetic ion doses show progressively less channeling and, at some critical dose, will spontaneously transform to the amorphous state. Various theories have been proposed to explain this phenomenon. One theory suggests that when the local concentration of point defects rises to the point where the free energy of the defected crystal state is equal to that of the amorphous, then spontaneous amorphization will occur. For silicon this suggests that amorphization will take place when the vacancy atom fraction exceeds the range ~ 0.04 – 0.2 . The degree to which this atom fraction must be exceeded depends upon spontaneous crystal annealing, which occurs during implantation. Another view suggests that when the local energy deposited by nuclear stopping exceeds that required to melt the crystal, then local

amorphization will take place. A review article by J. F. Gibbons [21] provides a comprehensive treatment of this subject. Ultimately, both the defect and local melting model require that a critical displacement energy density be imparted to the crystal target. Based upon these considerations, it has been suggested [22] that the transition occurs when the energy density exceeds a critical energy density E_C given by the equation:

$$E_C \approx f(10^{24}) \text{ eV/cm}^3 \quad (6)$$

where the factor, f , varies from 0.1 to 0.5, with the smaller value typical of moderate energy large mass ion, and the 0.5 factor typical of light species implantation. It is noted that both the vacancy model and the energy density models postulate a range of values. This range arises because spontaneous defect annihilation or damage annealing occurs during the transient time period ($\sim 10^{-11}$ s) when target atoms and electrons associated with the collision cascade are in an excited state. For this reason, the crystalline-amorphous transition occurs within a range of energy density values, dependent upon the species, dose rate, projectile energy, and target temperature. Also, since the accumulation of displacement damage and the crystalline-amorphous transition disrupts ion channeling, these dependencies can induce subtle changes in dopant profiles. Quantitative modeling of these phenomena requires quantification of the incident ion energy apportionment between electronic stopping and nuclear stopping. It further requires that the nuclear stopping be apportioned between collisions which produce target atom displacements, as opposed to leaving the non-displaced target atom in an excited state of vibration. It also requires a quantitative knowledge of displacement damage as a function of target depth.

F. Energy and Depth Dependent Electronic and Nuclear Stopping for Important Implant Species

Figures 2 and 3 give values of nuclear and electronic stopping for several common implanted species [24]. Figure 2 shows the monotonic increase in electronic stopping versus energy, as would be expected from (2). Figure 3, which is derived from the ZBL potentials, shows that nuclear stopping increases with atomic number, and that arsenic and antimony exhibit maxima at energy values of, respectively, ≈ 70 keV and ≈ 160 keV. Although not shown, the nuclear

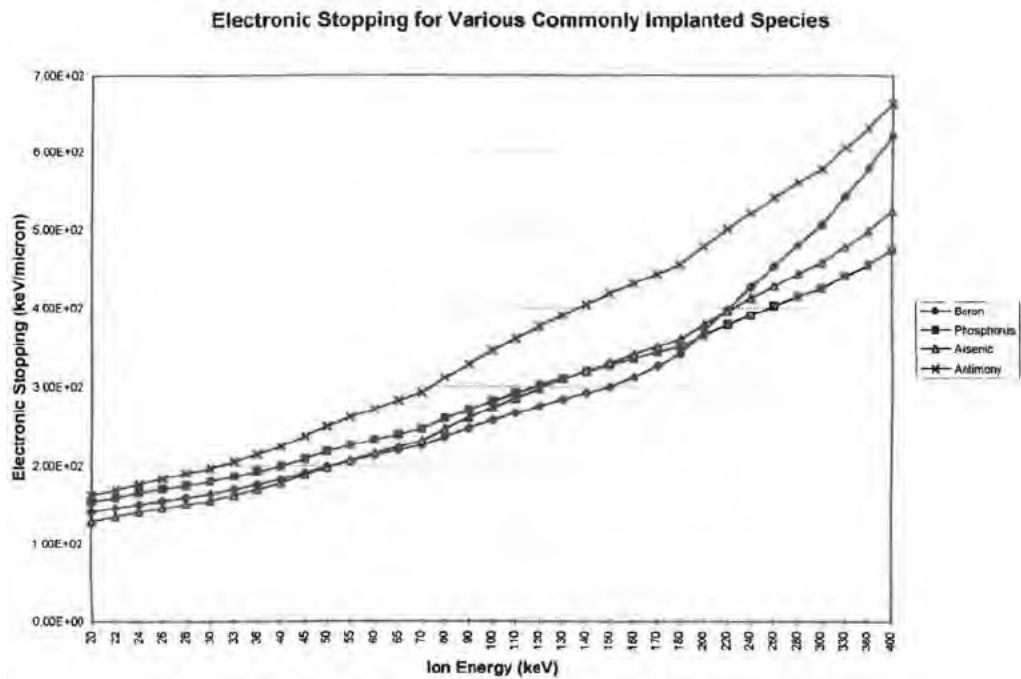


Figure 2 Electronic stopping in silicon for various commonly implanted ions (from TRIM).

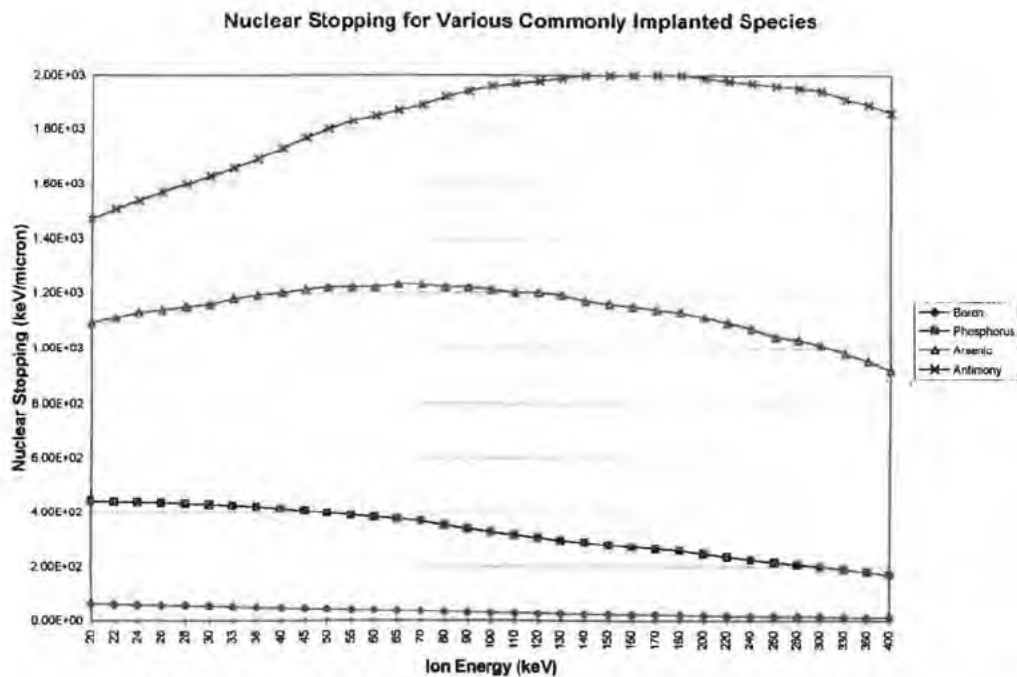


Figure 3 Nuclear stopping in silicon for various commonly implanted ions (from TRIM).

stopping values of phosphorus and boron also exhibit maxima at ion energies of, respectively, ≈ 17 and ≈ 3 keV. The monotonic decrease in nuclear stopping at high ion energies results from the fact that the ion scattering depends in part on the interaction time between projectile and target [10,12,18], which leads to smaller scattering cross-section as ion velocity (and energy) is increased. A second consequence of this velocity-cross section dependence is that at higher ion velocities, a greater fraction of nuclear stopping results from low angle scattering events which do not cause the displacement of target atoms. Therefore, displacement collisions become less probable as the projectile velocity increases. The theoretical work of Kinchin and Pease [25] provides a quantitative framework for the velocity (energy) apportionment of nuclear stopping between displacement and non-displacement events, and the theoretical work of Brice [26] quantifies the depth dependence of displacement collision events. Kinchin and Pease [26] suggest that when the ion energy is sufficiently low, then the number of target displacements produced by a primary recoil is given by:

$$N_d = E/E_d \quad (7)$$

where E is the energy of the recoil atom, and E_d is the target displacement energy, usually taken to be 15 eV. The upper energy boundaries for Eq. (6) validity are respectively 7 keV, 31.4 keV, and 480 keV for boron, silicon, and antimony. Equation (6) estimates the damage produced by the silicon knock-on atoms. Also, since the equation is linear, the total displacements produced by the primary ion and its knock-ons, may be estimated by from Eq. (7) by taking E to be the incident ion energy, provided that this value is below the aforementioned upper boundary. For energy values above the boundary, a progressively smaller amount of recoil energy results in displacement events and therefore:

$$N_d = fE/E_d \quad (8)$$

where f ranges in value from $\frac{1}{4}$ to $\frac{1}{2}$.

From the foregoing, it may be concluded that when an ion initially impinges on the target at high energy, stopping is predominantly comprised of electronic and non-displacement nuclear stopping. However, as the ion is slowed through these non-damaging processes, an energy is reached where target displacement collisions become predominant, and significant target damage is produced. After further slowing, the ion has lost sufficient energy so that only collisions with

low impact parameter can produce displacements. One might therefore expect that damage will maximize at some intermediate depth, which is more shallow than that location where the ion eventually comes to rest. The theoretical work of Brice [26] confirms this behavior.

G. Ion Stopping and Damage Viewed from the Monte-Carlo Model Perspective

As previously mentioned, nuclear stopping in the TRIM and UT-Marlowe Monte Carlo models is viewed as a series of binary collision events between a target lattice atom, and a energetic projectile which may be either the primary ion or an energetic knock-on silicon atom. All fast particles lose energy by electronic stopping between these binary collision events. The binary collision can result in three possible outcomes:

1. If both participants have a post-collision energy greater than a "displacement energy" E_d , then the target atom will be knocked out of its site, and the projectile ion will leave the site as well, leaving behind a vacant lattice site. A vacancy-interstitial pair (Frankel defect) is produced. The knock-on target atom leaves the site with the energy delivered by the projectile impact minus the displacement energy. It may have sufficient energy to create further knock-ons. The initial projectile may also have sufficient post-collision energy to create further knock-ons. For silicon, the displacement energy is usually taken to be 15 eV. After the collision event, some of the displacement energy is dissipated in the way of lattice vibration (phonon energy). However, some residual energy remains, associated with the vacancy-interstitial pair. This energy is known as the "binding energy" E_b , since it will be dissipated if the vacancy and interstitial recombine and mutually annihilate to restore the perfect lattice site. For silicon, the binding energy is usually taken as 2 eV, although the energy of a Frenkel defect derived from silicon self-diffusion studies indicates that an energy of 7–8 eV would be more appropriate [23]. The dopant and damage profiles yielded by Marlowe and TRIM are relatively insensitive to the choice of the binding energy.

2. If the post-collision energy of the target atom is $< E_d$, then it remains in its lattice site in an excited vibration state. The projectile leaves the site with its energy reduced by the excitation energy imparted to the target atom. This is the aforementioned non-displacement nuclear stopping.

3. If the post-collision energy of the projectile atom is $< E_d$ but the target atom is $> E_d$, then the projectile

Table 1 Summary results of TRIM simulations of commonly implanted ions

	Results of TRIM simulations of commonly implanted ions (99,999 ions counted)											
	10 keV Boron			28 keV Phosphorus			68 keV Arsenic			110 keV Antimony		
Backscattered Ions	2/34			101			0			0		
Longitudinal Mean Project												
Range, Rp	391 Å			405 Å			501 Å			567 Å		
Longitudinal Straggle, ΔRp	167 Å			171 Å			174 Å			162 Å		
Radial Projected Range	226 Å			181 Å			163 Å			150 Å		
Radial Straggle	113 Å			103 Å			94 Å			83 Å		
Vacancies/Ion TRIM 97	126.5			464.7			1212.4			1903.4		
Vacancies/Ion (Kinchin and Pease, (18))	98			355			921			1449		
Energy Loss (%)	Ions	Recoils	Total	Ions	Recoils	Total	Ions	Recoils	Total	Ions	Recoils	Total
Electronic Stopping	48.21	22.27	70.48	23.80	38.19	61.99	12.52	46.84	59.36	12.66	47.82	60.48
Target Vacancies	0.50	2.00	2.50	0.29	3.01	3.30	0.20	3.34	3.54	0.16	3.27	3.43
Phonon	1.72	25.31	27.03	0.76	33.95	34.71	0.44	36.65	37.09	0.33	35.76	36.09
Total	50.43	49.58	100.01	24.85	75.15	100.00	13.16	86.83	99.99	13.15	86.85	100
Energy Loss (keV)	Ions	Recoils	Total	Ions	Recoils	Total	Ions	Recoils	Total	Ions	Recoils	Total
Electronic Stopping	4.82	2.23	7.05	6.66	10.69	17.36	8.51	31.85	40.36	13.93	52.60	66.53
Target Vacancies	0.05	0.20	0.25	0.08	0.84	0.92	0.14	2.27	2.41	0.18	3.60	3.77
Phonon	0.17	2.53	2.70	0.21	9.51	9.72	0.30	24.92	25.22	0.36	39.34	39.70
Total	5.04	4.96	10.00	6.96	21.04	28.00	8.95	59.04	67.99	14.47	95.54	110.00

atom replaces the target atom in the lattice site. Such collisions are termed "replacement collisions". The struck target atom leaves the site with the energy of the projectile atom, minus the displacement energy. Collisions of this type tend to be more common near the end of the projectile path, where its energy has been reduced through prior collisions and electronic stopping. They leave the projectile in an interstitial site, but do not result in the creation of a vacancy.

The TRIM and UT-Marlowe programs track the individual paths of the incident ion and all the knock-ons, recording the various collision events until all energetic particles come to rest. In TRIM, no attempt is made to incorporate models for vacancy-interstitial recombination, whereas in UT-Marlowe, vacancy interstitial pairs which are within a "capture radius" are assumed to recombine and annihilate. The UT-Marlowe recombination model is limited in accuracy, which is currently under study to provide a model which better accounts for recombination, and is, as well, consistent with the dopant distribution profile.

H. TRIM Implant and Damage Profiles for Boron, Phosphorus, Arsenic, and Antimony

TRIM modeling was used to further elucidate the ion stopping process and ensuing target damage. Tables

1 and 2 summarize the results of this modeling for boron, phosphorus, arsenic and antimony. In all cases, 99,999 ions were counted, and displacement energy and binding energies of respectively 15 eV and 2 eV were assumed. Given the velocity dependence of electronic as well as nuclear stopping, ion energies were chosen to give equal initial ion velocities, to better clarify the effects of ion mass and atomic number. For boron, phosphorus, arsenic and antimony, these energies corresponded to respectively 10 keV, 28 keV, 68 keV and 110 keV. Further analyses were done to compare 110 keV boron with 110 keV antimony to elucidate the effects of ion energy and mass. These results are given in Table 2.

Figures 4-8 give some of the depth profiles from this modeling. Figure 4(a), 5(a), 6(a), 7(a), and 8(a) each provide dopant atom probability versus depth distribution, and a normalized vacancy versus depth distribution. The dopant distribution, when multiplied by the ion implant dose (with appropriate conversion of length and area units to cm and cm²) give the dopant concentration (in atom/cm³) versus target depth. The vacancy profile has been normalized by dividing by the overall vacancy/ion yield given in Tables 1 and 2 for each of the respective ions. For example, from Figure 4 it may be observed that for 10 keV boron ions, the normalized vacancy profile

Table 2 Summary of TRIM simulations demonstrating the effects of ion energy and ion mass

Results of TRIM simulations of illustrating the effects of ion energy and mass differences									
	110 keV Antimony			110 keV Boron			10 keV Boron		
Backscattered Ions	0			186			2134		
Longitudinal Mean Projected Range, Rp	567 Å			3669 Å			391 Å		
Longitudinal Straggle, ΔRp	162 Å			828 Å			167 Å		
Radial Projected Range	150 Å			1288 Å			226 Å		
Radial Straggle	83 Å			634 Å			113 Å		
Vacancies/Ion TRIM 97	1903			535.4			126.5		
Vacancies/Ion (Kinchin and Pease, (18))	1449			417			98		
Energy Loss (%)	Ions	Recoils	Total	Ions	Recoils	Total	Ions	Recoils	Total
Electronic Stopping	12.7	47.82	60.48	78.01	10.61	88.62	48.21	22.27	70.48
Target Vacancies	0.16	3.27	3.43	0.14	0.83	0.97	0.50	2.00	2.50
Phonon	0.33	35.76	36.09	0.45	9.96	10.41	1.72	25.31	27.03
Total	13.2	86.85	100	78.60	21.40	100.00	50.43	49.58	100.01
Energy Loss (keV)	Ions	Recoils	Total	Ions	Recoils	Total	Ions	Recoils	Total
Electronic Stopping	13.93	52.60	66.53	85.81	11.67	97.48	4.82	2.23	7.05
Target Vacancies	0.18	3.60	3.77	0.15	0.91	1.07	0.05	0.20	0.25
Phonon	0.36	39.34	39.70	0.50	10.96	11.45	0.17	2.53	2.70
Total	14.47	95.54	110.00	86.46	23.54	110.00	5.04	4.96	10.00

exhibits a maximum of 0.00225 at a target depth of 220 Angstrom. This figure, when multiplied by the vacancy/ion yield of 126.5 given in Table 2 gives the value of 0.284 Vacancies/Ion/Angstrom. This latter figure, when multiplied by dopant dose, yields the maximum vacancy concentration. This approach may be applied to all points on the normalized vacancy profile to yield a vacancy concentration versus depth profile. For the example cited above, one calculates that at the 220 Angstrom depth, a implant dose of 1(E) 14 ions/cm² yields a vacancy concentration 2.85(E)21 vacancies/cm³. It is noted that in the TRIM model, no vacancy/interstitial recombination is assumed, so the above value is a measure of the number of vacancies created by displacement collision events, and the depth value is the point in depth where the vacancies have been created. The vacancy profile therefore serves as a measure of displacement damage versus depth. It is noted that in all cases, that displacement damage peaks at some depth beneath the target surface, as expected by Brice's [25] theoretical predictions. Note also that the damage peak is more shallow than the dopant profile peak, also as would be expected from theoretical considerations.

Figures 4(b), 5(b), 6(b), 7(b), and 8(b) show the net excess of vacancies or interstitial atoms versus target depth. Here, the comparison is between the local con-

centration of vacancy generation cites, and local interstitial concentration, with no recombination assumed. As expected, regions of excess interstitial concentration lie deeper in the target than vacancies. Regions of excess interstitials are of particular interest, since these excess interstitials if present in a sufficiently high concentration may coalesce into extrinsic stacking faults or "311 rods" and eventually, upon further annealing coalesce into dislocation loops. During the transient period where such coalescence takes place, there exists a net non-equilibrium excess of interstitial atoms, which gives rise to enhanced dopant diffusivity. This transient enhanced diffusivity (TED) is of major current interest since it makes difficult the achievement of very shallow implanted junctions, such as are required for CMOS source/drain contacts and drain extensions. There exists extensive current literature related to boron TED. Reference [26] by P. A. Stolk et al, provides an excellent review of the current literature.

Figures 4(c), 5(c), 6(c), 7(c), and 8(c) show the displacement damage versus target depth for a dopant dose of 1(E) 15/cm². This damage-depth behavior is again consistent with the foregoing discussion and the theoretical work of Brice. Reference to Eq. (6) indicates that amorphization of the silicon target may be expected for displacement damage in the range of 1(E) 23 eV/cm³ for heavy ions such as antimony, to

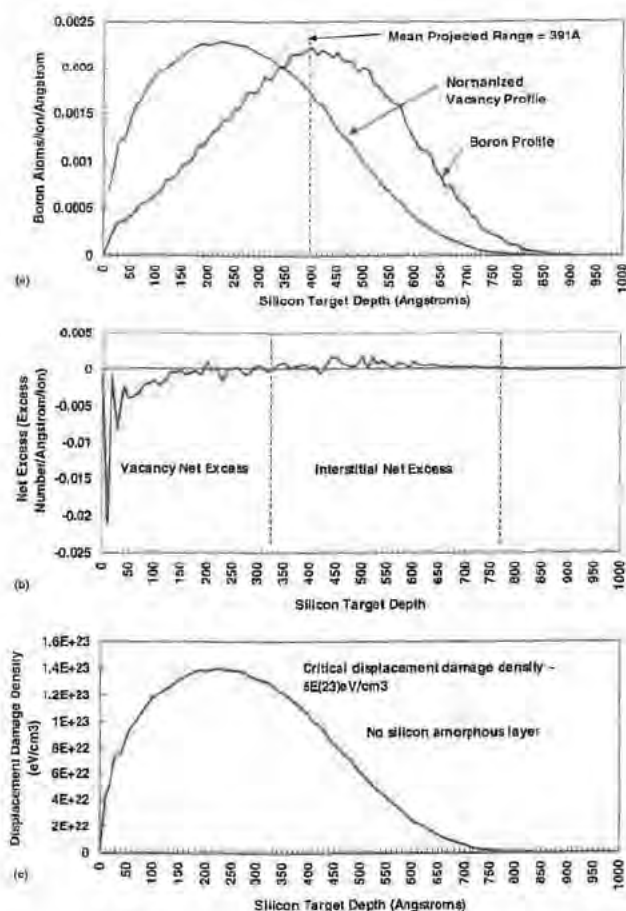


Figure 4 TRIM simulation results for 10 keV boron ions implanted into silicon (99,999 ions counted). (a) Normalized vacancy profile and boron dopant profile. (b) Net excess vacancy and interstitial profile. (c) Displacement damage profile for $1\text{E}15/\text{cm}^2$ boron dose.

5(E) 23 for light ions such as boron. From the figures it may be expected that at this dose, boron ion implantation will produce no amorphized region, phosphorus will possibly produce a buried amorphized layer in a region on the shallow side of the dopant profile peak, arsenic will produce a continuous amorphous layer which is also centered on the shallow side of the dopant profile peak, and antimony will produce a very substantial continuous amorphous layer which encompasses virtually all of the implanted dopant profile. It is also noted that for 110 keV boron, Figure 8(c), the peak damage density is one-half the peak damage density produced by the 10 keV boron implant. This somewhat counter-intuitive result derives from the fact that high energy implants tend to produce collision cascades which are more broadly

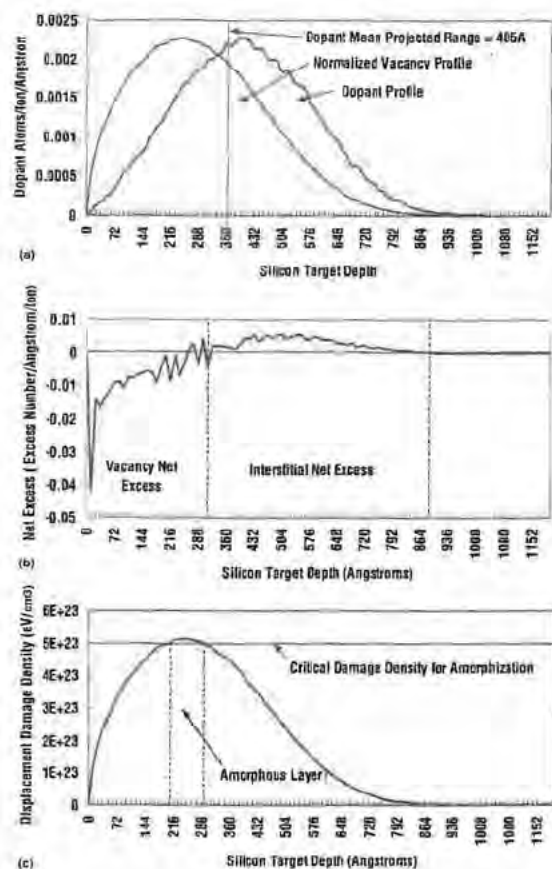


Figure 5 TRIM simulation results for 28 keV phosphorus ions implanted into silicon (99,999 ions counted). (a) Normalized vacancy profile and phosphorus dopant profile. (b) Net excess vacancy and interstitial profile. (c) Displacement damage profile for $1\text{E}15/\text{cm}^2$ phosphorus dose.

dispersed, and where a greater fraction of stopping is apportioned to electronic stopping and non-displacement nuclear stopping.

Referring to Table 1, it is noted that the longitudinal mean projected range of all ions as having the same velocity is roughly the same, ranging from a value of 391 Angstroms ($1\text{ Angstrom} = 10^{-10}\text{ meter}$) for 10 keV boron, to 567 Angstroms for 110 keV antimony. Notice as well that the longitudinal straggle is also approximately the same. On the other hand, the radial straggle and radial projected range monotonically decrease with increasing ion mass. This implies that, for the large mass ions, there will be less encroachment of the dopant profile under a mask edge. Notice as well that there is a dramatic increase in the number of vacancies produced per incident ion,

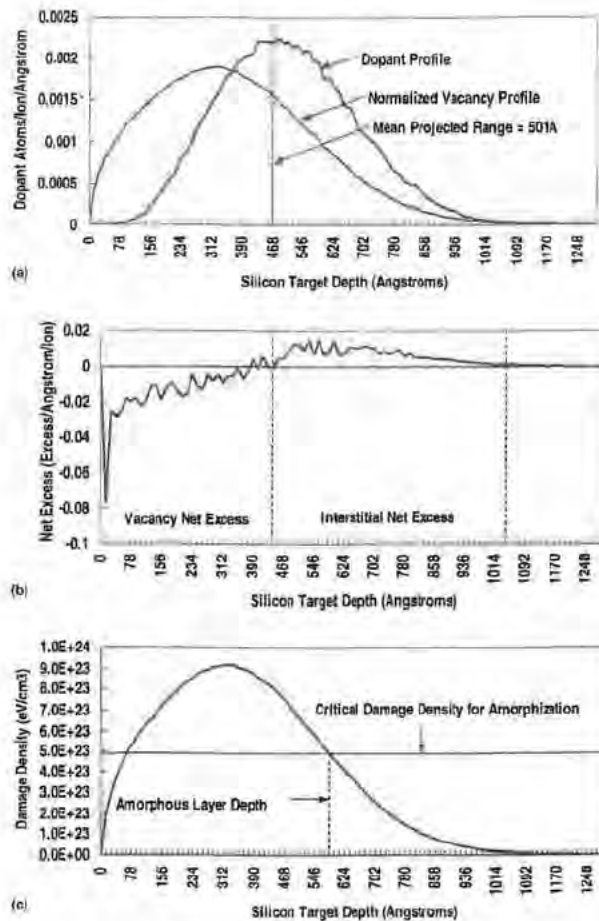


Figure 6 TRIM simulation results for 68 keV arsenic ions implanted into silicon (99,999 ions counted). (a) Normalized vacancy profile and arsenic dopant profile. (b) Net excess vacancy and interstitial profile. (c) Displacement damage profile for $1\text{E}15/\text{cm}^2$ arsenic dose.

increasing from a low of 126.5 vacancies per ion for 10 keV boron, to 1903.4 vacancies per ion for 110 keV antimony. Since the depth profiles are roughly the same, this implies a significantly higher concentration of displacement damage for the antimony implant as compared with the boron implant. Notice as well that for 10 keV boron, of the nominal 100,000 ions counted, 2134 ions are back-scattered and recoil off the target surface, a consequence of the low ion mass relative to the silicon target atom, whereas for the large mass ions the back-scattered fraction drops to zero. In comparison, 110 keV boron (Table 2) shows the back-scattered yield dropping to 186 ions with the dopant profile is skewed toward the surface, indicating that back-scattering continues to take place but that the

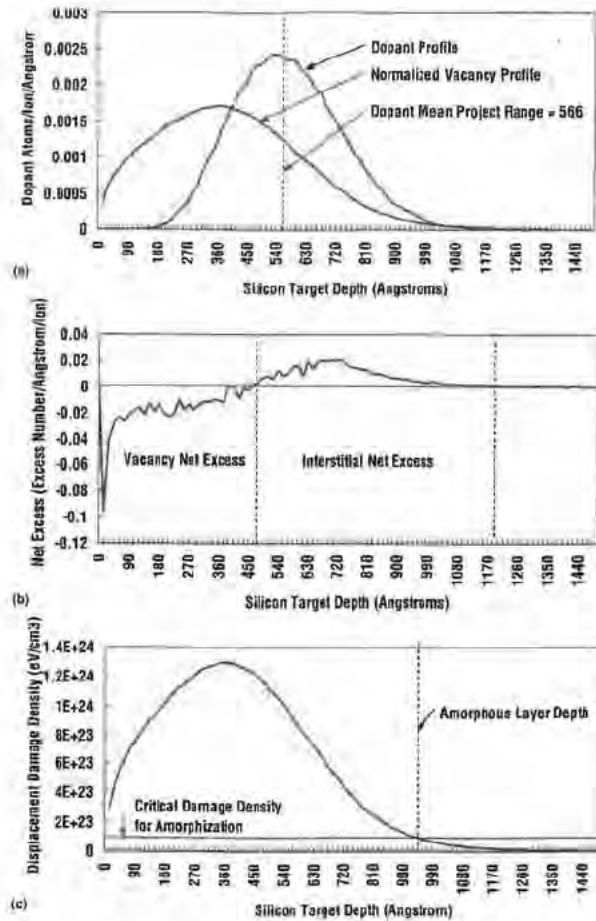


Figure 7 TRIM simulation results for 110 keV antimony ions implanted into silicon (99,999 ions counted). (a) Normalized vacancy profile and antimony dopant profile. (b) Net excess vacancy and interstitial profile. (c) Displacement damage profile for $1\text{E}15/\text{cm}^2$ antimony dose.

increased depth of back scattering prevents many ions from escaping the target surface.

Referring to the energy loss tabulations of Table 1 it is noticed that the percent electronic stopping experienced by the incident ion monotonically decreases from a high of 48.21% for 10 keV boron, to a low of 12.66% for antimony, whereas the energy dissipated via electronic stopping by the target atom recoils rises from a low of 22.27% for boron, to a high of 47.82% for antimony. Since electronic stopping is proportional to the square root of the velocity, this signifies that the average velocity of recoils is much higher with the large mass energetic ions.

Referring again to Tables 1 and 2 it is noted that for implants of comparable depth, the total energy dis-

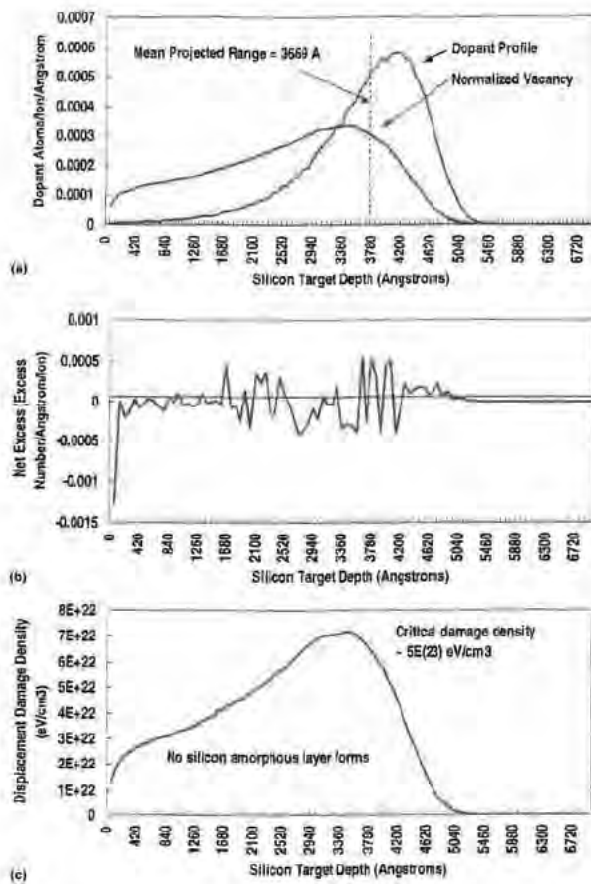


Figure 8 TRIM simulation results for 110 keV boron ions implanted into silicon (99,999 ions counted). (a) Normalized vacancy profile and boron dopant profile. (b) Net excess vacancy and interstitial profile. (c) Displacement damage profile for $1\text{E}15/\text{cm}^2$ boron dose.

sipated in nuclear stopping rises dramatically with atomic mass. A major contributor to this phenomenon is the larger nuclear stopping of the large mass ions, consequently requiring that dramatically higher ion energy be employed to achieve a comparable implant depth. As a result the nature of target crystal damage and amorphization is considerably different. Some insight into this phenomena may be gathered from studying, from the tables, the total nuclear stopping for both the primary ion and its recoils. According to the TRIM lexicon, nuclear stopping is comprised of energy loss allocated to "Target Vacancies" and "Phonon". "Target Vacancy" energy loss is the fraction of nuclear stopping which results in the generation of a Frenkel defect. It is the number of such defects produced multiplied by the binding energy of the Frenkel defect (taken to be 2 eV in the

simulation). The difference between the displacement energy (15 eV), and the binding energy, is dissipated as lattice vibration, i.e. "Phonon" energy loss. In addition, "Phonon" energy loss has further contributions which originate from collisions where the target is not displaced, but remains behind in an excited state. With these definitions in mind, Table 1 indicates that a 10 keV boron and its silicon recoil atoms dissipate a total of 2950 eV in nuclear stopping, of which 250 eV is the energy associated with the production of displacement events ("target vacancies"). The corresponding displacement event production energies for 28 keV phosphorus, 68 keV arsenic, and 110 keV antimony ions are respectively 920 eV, 2410 eV, and 3770 eV. Reference to normalized vacancy profiles of Figures 4(a), 5(a), 6(a) and 7(a), and the displacement damage density profiles of Figures 4(c), 5(c), 6(c), and 7(c) provide a measure of the path lengths over which this displacement energy is dissipated. From the figures these path lengths are ~ 545 Å, ~ 564 Å, ~ 715 Å, and ~ 735 Å for, respectively, boron, phosphorus, arsenic, and antimony.

From the above it may be concluded that light ions produce relatively low concentrations of damage as they come to rest in the target crystal, whereas heavy ions produce very high damage concentrations which are produced primarily by the energetic recoils. Gibbons [21] reviews the literature in this area, and concludes that heavy ions and their recoils induce sufficient displacement damage along the cascade track that a core of amorphized material is produced by each ion, whereas for light ions, amorphization is induced by the cumulative damage which results from the overlap of multiple damage tracks traversing a given region of the target crystal. The former has been termed heterogeneous damage nucleation, and the latter homogeneous. Heterogeneous damage results in the development of a continuous amorphous layer, when there is sufficient overlap of the individual amorphous cores along each damage track to produce the continuous amorphous layer. Homogeneous damage causes amorphization to nucleate when sufficient cumulative damage has occurred in a given crystal region. In both cases, the build up of the amorphous layer occurs in those regions of the target crystal where high levels of displacement damage occur. However, the mechanism for amorphous layer formation is fundamentally different in the heterogeneous versus the homogeneous case.

From the above it is also evident that many atoms in the region of the collision are in highly excited

vibration states, i.e. the target crystal is locally "heated". Although this heating rapidly dissipates ($\sim 10^{-11}$ seconds), opportunity exists for atom migration during this period, with the result that damage annealing can take place. In addition, the overall temperature of the target crystal may also allow for further damage annealing over the implant time period. The result is that the formation of amorphous layers, in addition to depending on ion dose, depends upon the target temperature during ion implantation, as well as dose rate. As a result the total dose required to achieve amorphization is dependent upon ion species, energy, dose rate, and target temperature. Morehead and Crowder [22] have modeled the dose and target temperature dependence for different ion species. The model is based upon the heterogeneous case, in which each ion trail is assumed to consist of an amorphous core, which is reduced in cross-section by diffusion induced damage annihilation. Morehead and Crowder made no attempt to model the dose rate dependence. The model results have been widely published [22,27], and show good agreement with heavy ion implantation results. Surprisingly, good agreement exists with light ion results, despite the fact that for light ions, homogeneous damage nucleation takes place [22]. According to the model results, there is a low temperature domain where the amorphization dose is target temperature independent. As target temperature is increased, a critical temperature is reached above which the dose required for amorphization rapidly rises. Below this critical temperature, the doses required for amorphization are, respectively, $\sim 8(E)^{1/3}$ ions/cm² for antimony, $\sim 2(E)^{1/4}$ ions/cm² for phosphorus, and $\sim 2(E)^{1/5}$ ions/cm² for boron. The critical temperatures above which amorphization is precluded are, respectively: 400°K for antimony, 250°K for phosphorus, and 225°K for boron. These results need to be taken into consideration when the damage profiles of Figures 4(a), 5(a), 6(a), and 7(a) are used to predict the onset of amorphous layer formation, and the depths at which such amorphous layers form.

Referring again to Figures 4 through 7, it is noted that when an amorphous layer forms, there is a region which lies deeper in the target crystal where significant damage exists, and wherein a significant concentration of dopant atoms resides. It also frequently corresponds to a region where a net excess of interstitial atoms resides. This region is known as the "end of range" damage region, and is of considerable interest in understanding transient enhanced diffusion, as well as the resulting electrical quality of the *p-n* junction

produced after thermal activation of the implanted ions. The placement of this damage region is also of great importance when iso-valent ions such as silicon, germanium, or tin are used to intentionally create amorphized regions in order to suppress channeling. It is also known that end of range damage cannot be completely annihilated within the thermal budget constraints of modern silicon manufacture. This becomes of concern when the remaining damage resides within the depletion region of the resulting *p-n* junction, where excessive electrical leakage may result. Fortunately, for most source-drain implants, this damage region is more shallow than the junction, leaving the damage in degeneratively doped silicon, and no junction leakage is observed. However, when using preamorphizing implants such as silicon, germanium or tin, this fortunate circumstance may not occur, making it important to understand the respective locations of depletion and residual damage regions.

III. CMOS APPLICATIONS OF ION IMPLANTATION

A. CMOS Structure

Figure 9 shows the doped regions of an advanced CMOS structure. Virtually all doping in modern CMOS devices is accomplished by ion implantation; no other technique offers comparable process control and repeatability for both the amount and position of the doping. MOSFET doping requirements span several orders of magnitude in both dose and energy for multiple species, as shown in Figure 10. Modern ion implantation equipment has been refined such that two to three carefully designed system architectures are capable of covering all of these applications.

B. Threshold Voltage Adjust Implants

The threshold voltage (V_T) at which the channel of the MOS transistor begins to conduct current is of fundamental importance. This voltage is directly proportional to the amount of charge carriers (i.e. doping) in the channel region. This implant allows the current/voltage characteristics for all transistors to be so similar that, even with other processing variations, a large area integrated circuit can operate on a single power supply voltage and have closely matched electrical behavior all across the chip. Dose uniformity across each wafer and dose repeatability, wafer-to-wafer and day-to-day, are absolutely essen-

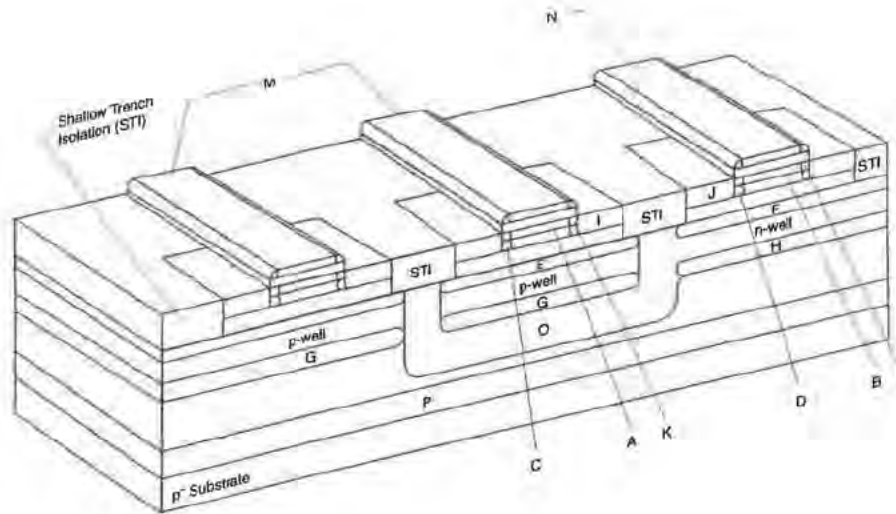


Figure 9 Cross section of a CMOS structure, indicating how virtually the entire subsurface structure is formed by ion implantation. These structures are found in all modern devices, with the exception of the triple well and the buried layer which are currently increasing in use. (A) NMOS threshold voltage adjust. (B) PMOS threshold voltage adjust. (C) NMOS punchthrough suppression. (D) PMOS punchthrough suppression. (E) NMOS channel stop. (F) PMOS channel stop. (G) Retrograde *p*-well (H) Retrograde *n*-well. (I) NMOS source/drain. (J) PMOS source/drain. (K) NMOS source/drain extension. (L) PMOS source/drain extension. (M) *n*⁺ polysilicon gate doping (NMOS). (N) *p*⁺ polysilicon gate doping (PMOS). (O) *n*-type triple well (P) *p*⁺ buried layer.

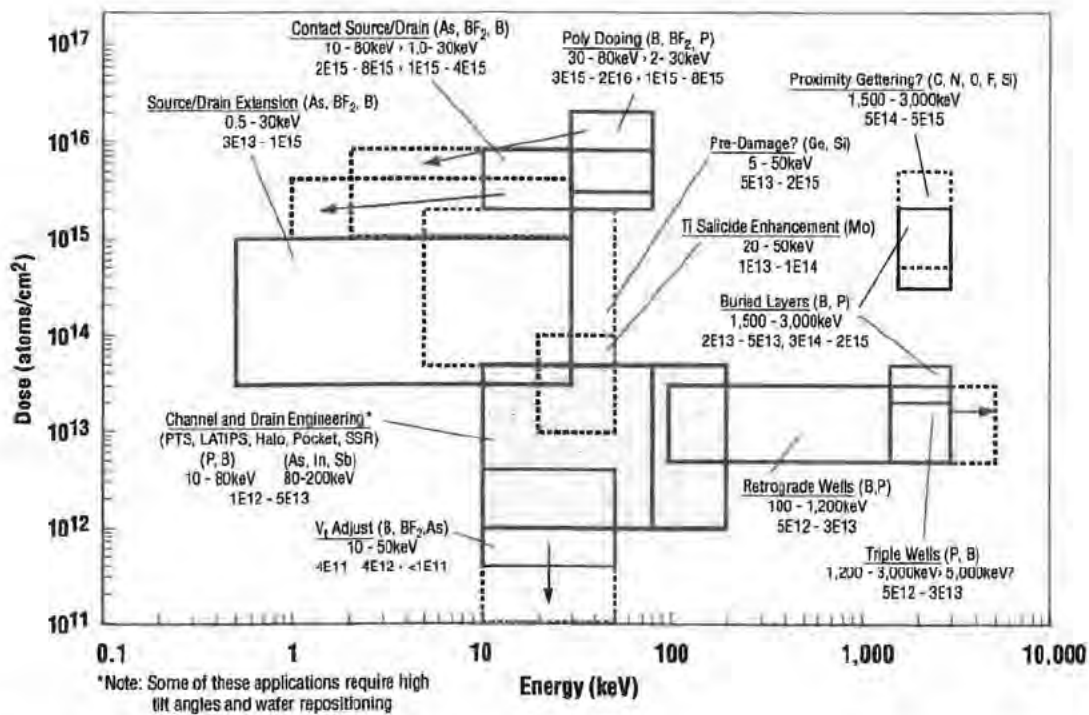


Figure 10 Typical dose and energy ranges for the doping applications in Figure 9. Within the energy range for each application, lower mass species are typical implanted at lower energies than heavier species. The dose of the application depends on device design requirements and is generally independent of species.

tial to achieving consistent, reproducible threshold voltages on all transistors in a modern IC. This application is more sensitive to doping variations than any other. Consistency in the doping profile is also extremely important, requiring reproducible beam energy and a lack of energy contamination (off-energy components) in the beam.

This implant places dopant just under the gate oxide in the device channel (Fig. 9). The energy varies depending on the thickness of the gate oxide present during implant. This implant application was the first widespread use of ion implantation in semiconductor production processes. It is one of the most widely used implantation steps in MOS production, and will remain so in the future.

C. Channel Engineering

1. Punchthrough Suppression

Punchthrough suppression implants (also known as HALO, SPI, TIPS, or "Pocket" implants) prevent expansion of the drain depletion region into the lightly doped transistor channel when the device is biased for operation. This expansion can increase subthreshold leakage currents or, if severe enough, short the channel (punchthrough). The implant is typically done after gate formation, ensuring that the dopant is self-aligned to the gate. The dopant is placed just below the active channel, adjacent to the source and drain (Fig. 9), and is of the same dopant type as the well. As with all implants in the channel region, precise control of the placement and dose of this implant within the transistor structure is required to achieve the intended enhancements.

High wafer tilt angles are commonly used for punchthrough suppression implants. Wafer tilt angle is an additional, controllable processing parameter that offers additional process freedom and flexibility for creating complex channel structures, without diffusion or additional masks. High tilt angles are crucial for achieving larger lateral penetration for the HALO implant than for the adjacent source/drain (S/D) implant without using thermal diffusion. Typical tilt angles are 20°–45° from the wafer normal. To maintain device symmetry with high tilt, the implants must be split into two segments, with the wafer rotated 180° in between. Since most circuits contain transistor gates placed 90° from each other, high tilt implants are typically done in four segments of equal dose ("quad" implants) with the wafer rotated 90° in between the segments.

High tilt punchthrough suppression implants significantly improve device performance. Junction capacitance can be reduced up to 65%; while the subthreshold cutoff of the device becomes more steep, suppressing short channel effects [28]. For similar drive currents, the body (backgate bias) effect is reduced up to 50%. The dramatic improvement in punchthrough resistance does not depend on extreme scaling of the S/D junction depth or *n*-well background doping. The reduced subthreshold slope and junction capacitance directly result from the carefully controlled doping underneath the channel at the gate edge and the near elimination of all other undesired doping that results from less controllable doping methods [29,30]. HALO implants are effective in devices with gate lengths ranging from 600 nm down to 50 nm [31–34], indicating that ion implantation will play a dominant role in CMOS transistor doping applications for the foreseeable future.

2. Retrograde Channel Doping

Surface channel devices with super-steep retrograde channels are formed by substituting a high mass dopant of the same conductivity type for the ordinary dopant in the surface region of the well (i.e. indium instead of boron and arsenic or antimony instead of phosphorus). The heavier ions have reduced diffusivity, allowing the fabrication of well profiles with reduced doping ($\sim 5 \times 10^{16} \text{ cm}^{-3}$) at the gate oxide interface, and a doping peak ($\sim 1 \times 10^{18} \text{ cm}^{-3}$) at $\sim 80 \text{ nm}$ below the gate oxide. This doping structure is excellent at reducing short channel effects and drain-induced barrier lowering without affecting drive current, but can increase body effects [33]. Retrograde channels will become increasingly important for smaller device generations. Because of its higher diffusivity and susceptibility to transient enhanced diffusion (TED) (see chapter on diffusion, [26,36]), boron may not be acceptable as a channel dopant for NMOS devices scaled down beyond 180 nm. Channel implants of indium [37] and arsenic [38] have been shown to reduce short channel effects, and slightly improve channel mobility for NMOS and PMOS devices, respectively.

3. Channel Stop

Regardless of whether a circuit uses field oxide (LOCOS) or shallow trench isolation (STI) for transistor isolation, it is necessary to prevent activation of the parasitic MOSFET that is unavoidably formed by active interconnect lines running over the



Figure 11 Doping profile of a modulated retrograde well structure, showing the device parameters affected by the doping level at each depth. Adapted from references [40,41].

thick oxide. A channel stop implant, also referred to as a "field isolation" or "guard ring", makes the parasitic transistor's V_T so large by sufficiently increasing the doping concentration at the well surface that it will not be reached in normal circuit operation. This implant places dopant just under the field oxide (Fig. 9). Channel stop implants (boron in the p -well and phosphorus in the n -well) are used for both intra-well (inter-device) and inter-well isolation as well as latch-up protection [39]. Proper field isolation is required to realize maximum packing density in CMOS circuits. In advanced processes, this isolation is achieved by implanting through the oxide (LOCOS or STI), as part of the implant chains that form the n -well and p -well structures. The implant energy depends on the thickness of oxide present.

D. Modulated/Retrograde n -Well and p -Well Implants

Ion implantation is essential for fabricating the twin tub (both p -well and n -well implants) CMOS process. The modulated well structure (Fig. 11) has replaced the older diffused well process, due to its higher processing flexibility and lower cost. Since the well forms the MOSFET's "back gate", the well doping will fundamentally affect the transistor's electrical performance. Engineering the well with multiple implants and minimal thermal diffusion allows independent control of dopant levels throughout the depth of the well, and thus independent optimization of

key MOSFET performance characteristics (Fig. 11). Device speed (carrier mobility, S/D capacitance), inter-device leakage currents, V_T control, punchthrough suppression, parasitic transistor effects, and soft error and latch-up resistance can be optimized almost independently by carefully positioned dopant peaks and valleys [41,42]. Low surface doping levels increase mobility and decrease capacitance. Heavier doping below the surface (retrograde doping) reduces minority carrier collection by reducing depletion widths, thus reducing soft errors and latch-up susceptibility [43–46]. This degree of design flexibility is not possible with diffused wells.

Advanced processes form modulated wells by "chaining" together multiple implants, eliminating the need for separate V_T adjust and channel engineering implants (except those using high wafer tilt for precision dopant placement). Long, high temperature well drive-ins are also eliminated, allowing the use of RTA. This reduces lateral dopant diffusion and permits higher circuit packing densities. Also reduced are silicon "wafer slip" and metallic contamination from furnace heating elements. Modulated well architectures reduce photomask count, process complexity, cycle time, and capital and production costs for both memory and logic devices [39,47].

Since the near surface implants of a modulated well dope the MOSFET channel, tight control of implant dose and energy is crucial. For the deeper implants, the doping asymmetry resulting from a 7° wafer tilt and high photoresist walls can significantly affect the resulting devices, despite the wider mask openings for well implants. The beam angle asymmetry will cause opposite corners of the photoresist to wear down and carbonize differently, eventually increasing the surface doping on the incoming side of the resist, degrading mobilities and junction capacitances. These problems can be minimized by reducing the tilt angle to the $2\text{--}4^\circ$ range, using 0° tilt, or wafer repositioning during high energy implants through photoresist.

E. Triple Wells

A triple well is a larger and deeper well of the opposite conductivity type as the substrate surrounding a well of the same conductivity type as the substrate (Fig. 9). Because the well that contains the active devices is isolated from the substrate by two p - n junctions in series with opposite orientations, it can be biased with any desired voltage with respect to the substrate without creating a forward biased junction. This gives additional flexibility to device designers to optimize

performance in specific applications [48]. Since the triple well is formed deep in the substrate, it is very important that the implanted beam be free of energy contamination, especially singly charged ions in a multiply-charged beam. Ions with insufficient energy will cause unwanted counterdoping of the encapsulated well.

Currently, triple wells are implemented mainly in DRAM and flash memory circuits. The independent well biasing possible in a DRAM triple well structure allows the simultaneous optimization of memory cell transistors for low leakage and peripheral transistors for speed [48]. In flash memory circuits, placing the NMOS row decoder circuitry inside a n -type triple well allows a negative bias to be generated on-chip for efficient erasing without unwanted source to substrate leakage. This gives additional flexibility in optimizing the channel design of the flash transistor. The independent biasing of wells actually allows the elimination of circuit components, simplifying the layout, improving reliability, and reducing chip area [42,49]. The additional isolation provided by the triple well effectively traps minority carriers, resulting in sharply reduced soft error rates [50] and substrate noise [48,51]. Triple well technology improves logic circuits by allowing back gate biasing that reduces junction capacitances and subthreshold slopes significantly [52].

F. Buried Layers

Buried layers are highly doped regions implanted 2–4 μm beneath the silicon surface, usually with no photomask present (Fig. 9). Buried layers can greatly enhance device performance on bulk substrates, and have the potential for large scale replacement of epi silicon substrates. The doping and end-of-range (EOR) damage in the buried layer region reduce the concentrations of metals and oxygen in the surface region in undenuded wafers down to those in denuded silicon, and almost down to the levels in epi layers. Additionally, the EOR damage getters defects induced by subsequent implants, reducing leakage currents [41,53–56]. Despite a much higher cost [39] epi substrates are not capable of damage gettering. An implanted buried layer is more effective than a highly doped epi substrate in suppressing latch-up [39], because it is located closer to the active devices. The position of a buried layer is set by the highly reproducible implant energy, and need not be set excessively deep to prevent well counterdoping by the epi substrate dopant. Buried layers can also be formed with

non-dopant species, providing gettering benefits but no latch-up suppression.

Buried layer implants have been put into production processes only recently. A successful buried layer process requires sufficient implant dose and proper thermal processing to engineer the buried layer damage into stable dislocation loops at EOR [41,54,57]. Improper or excessive annealing can result in leakage-inducing line dislocations propagating to the near surface regions or counterdoping of the well regions by the buried layer dopant. Compared to channel and well implants, buried layers are relatively insensitive to dose precision or shadowing effects. The high doses of buried layers require that the implanted beam be energy pure to prevent counter-doping of the wells.

G. Source/Drain Implants

These implants are used to form highly doped ($>10^{20} \text{ cm}^{-3}$) source and drain regions adjacent to the more lightly doped ($\sim 10^{18} \text{ cm}^{-3}$) active channel and well regions of the device (Fig. 9). The S/D regions are doped with the opposite conductivity type from the surrounding well to create diode isolation. Reverse-biasing of the drain junction is typical. S/D structures must be heavily doped to minimize MOSFET parasitic resistance and contact resistance to the silicide (see chapter on silicidation). To suppress punchthrough and the dependence of V_T on channel length (short channel effect), the S/D junction must be very shallow, and become even more shallow as gate widths decrease. Scaling considerations indicate that MOSFETs with dimensions $\leq 250 \text{ nm}$ will require S/D junction depths of $\leq 100 \text{ nm}$ [58,59].

Shallow S/D junctions for NMOSFETs can be formed easily by arsenic implantation, because of its high mass, and because the high dose used fully amorphizes the silicon, suppressing channeling effects. Shallow p -type junctions are very difficult to form due to the low mass and susceptibility to TED of boron, the only p -type dopant with solid solubility suitable for this application. This has driven boron implant energies to the ultra-low (0.5–10 keV) range, and forced the development of specialized ion implanters to do these implants economically. Channeling tails are relatively insignificant compared to TED effects below 5 keV, making optimization of the post-annealing very important. Instead of low energy boron, BF_2 can be implanted at higher energies. This can cause V_T shifts because the presence of fluorine

enhances diffusion of boron from the polysilicon gate into the channel.

S/D implants are usually done at 0° tilt or in a quad configuration to avoid device asymmetries. Beam energy purity is of paramount importance for S/D formation. Any high energy contaminants in the beam (e.g., neutrals arising from problems with deceleration mode) will result in deeper junctions and degraded devices. Low implant energies also preclude the use of screen oxides to capture sputtered-on metals, requiring minimal metallic contamination from the implanter. Because the S/D regions are degenerately doped, dose precision is far less of a concern than for channel implants. However, dose rate (beam current) reproducibility is important, since *p*-type S/D implants are usually close to the silicon amorphization threshold.

H. Source/Drain Extension Implants

The S/D extension is a highly doped ($\sim 10^{20} \text{ cm}^{-3}$) region under the sidewall spacer between the S/D regions and the channel (Fig. 9), where lightly doped drain (LDD) structures [28] used to be. The LDD structure forced a trade-off between hot carrier immunity and transistor drive current [60–62]. As power supply voltages were reduced from 5 V to as low as 1.0 V, the hot carrier problem became less severe, while the parasitic resistance contribution increased. To offset this, the doping has been increased from the $1\text{--}5 \times 10^{13} \text{ cm}^{-2}$ range to the $5\text{--}10 \times 10^{14} \text{ cm}^{-2}$ range, making this region a low resistivity extension of the S/D structure. Because it is directly adjacent to the channel, a low S/D extension junction depth is even more crucial for punchthrough resistance than is the S/D depth. Since there are no silicide contact issues in the extension region, the dose and energy of this implant are both lower than for the adjacent S/D implant. Implemented properly, an aggressively scaled extension junction can eliminate the need for a high tilt punchthrough stop implant, simplifying the process and the channel architecture. Phosphorus and arsenic are used for NMOS S/D extension implants, while boron is used for PMOS devices. Implanter requirements for extensions are similar to S/D structures; energy purity and low metallic contamination are required.

Control of the gate to extension overlap length to within $\sim 10 \text{ nm}$ is crucial for optimal device performance. Inadequate overlap degrades drive current and increases short channel effects, while extra

overlap increases parasitic capacitance [63]; device speed is limited in either case. Proper positioning of the extension is achieved by implanting at reproducible 3–7° tilt angles, usually combined with quad repositioning to ensure device symmetry. However, certain flash memory designs use an uncompensated 7° tilt for this implant; the resulting asymmetry improves programming and erasing efficiency [64].

I. Pre-Damage Implants

These implants are done prior to S/D or S/D extension doping implants to create damage in the wafer. Germanium or silicon ($2 \times 10^{14}\text{--}2 \times 10^{15} \text{ cm}^{-2}$) pre-amorphizes the silicon prior to depth-critical implants, preventing or suppressing channeling (depending on amorphous layer depth). Germanium is used more than silicon because its higher mass gives it a lower amorphization threshold dose, and because it retards the diffusion of boron during post-implant annealing [65]. Since it is easier to regrow an amorphous layer than to anneal a damaged crystal, pre-damage implants can result in higher final dopant activation and lower crystal defects [66]. The pre-damage implant energy must be selected so that EOR dislocation loops do not remain in the S/D depletion region where they would increase S/D junction leakage.

Indium and antimony are sometimes used to pre-amorphize and counterdope S/D junctions in NMOS and PMOS devices, respectively. The very high mass of these dopants facilitates amorphization, and the counterdoping helps to form an abrupt, shallow junction. The energy of this implant must be carefully controlled to achieve the proper counterdoping effect.

Nitrogen implants ($\sim 60 \text{ keV}$, $5 \times 10^{14}\text{--}2 \times 10^{15} \text{ cm}^{-2}$) performed prior to gate oxidation retard the oxidation rate, reduce the diffusivity of boron in the oxide, and improve the breakdown resistance of ultra-thin gate oxides [67,68]. Nitrogen is also effective at gettering metallic impurities [69].

J. Polysilicon Doping Implants

Polysilicon must be degenerately doped to be effective as a gate material. This doping is accomplished by ion implant, since thermal budget limitations have eliminated the past practice of chemical diffusion doping. High dose implants enable the “dual poly” process, where surface channel NMOSFETs and PMOSFETs have *n*-type and *p*-type polysilicon,

respectively. Dual poly is required for symmetrical threshold voltages at design rules below 250 nm, and it minimizes short channel effects [43,70,71]. Initially, the polysilicon was doped using the same implants used to form the S/D structures. At design rules below 250 nm, doping the *p*-type polysilicon requires implant doses and energies higher than *p*-type S/D junctions can tolerate and remain sufficiently shallow. A separate, masked, *p*-type polysilicon doping implant is required. A similar implant may also be eventually required for the *n*-type polysilicon. A beam free of energy contamination is required to prevent unwanted doping of the channel region during this implant. Implanting *p*-type polysilicon is easiest with low energy boron; this prevents the fluorine enhanced diffusion of boron through ultra-thin gate oxides that occurs with BF_2 implants [72]. The effect is suppressed somewhat by nitriding the gate oxide, either during oxidation or by co-implantation.

K. SOI Technologies

1. SIMOX

SIMOX (Separation by IMplanted OXygen) implants produce thin silicon films of high crystalline quality with an abrupt interface to a stoichiometric SiO_2 buried layer. Implant conditions for oxygen are 100–200 keV, 3×10^{17} – $2 \times 10^{18} \text{ cm}^{-2}$, with the wafer held at $\sim 600^\circ\text{C}$ during implantation. Very high temperature ($>1350^\circ\text{C}$) post-annealing is then required to form the SiO_2 layer and remove dislocations in the silicon [73]. Although the potential device and circuit benefits of silicon-on-insulator (SOI) are many, the extremely high doses required and the associated high costs have kept SIMOX a niche technology. Besides dose, energy, and implant temperature uniformity control, this process requires low metallic and particulate contamination in the implanter to achieve uniform, high quality layers of thin film silicon and buried oxide.

2. SmartCut

SmartCutTM is a technology for fabricating SOI structures based on both ion implantation and wafer bonding techniques [74,75]. Hydrogen and/or helium is implanted (~ 30 – 120 keV , 2×10^{16} – $2 \times 10^{17} \text{ cm}^{-2}$) beneath a thermal oxide on a wafer that is then bonded to a second wafer. When the bonded pair is annealed at 400 – 600°C , the voids formed by the implanted species cause the wafers to separate at the implant peak.

The resulting two pieces are an SOI wafer and a bulk silicon wafer, suitable for reuse. This process may significantly lower the cost of producing SOI, since the implant dose is an order of magnitude lower than for SIMOX, and the implant is done at room temperature in a standard high current implanter. Because of the high diffusivity of H and He in silicon, this process is insensitive to minor dose variations.

IV. COMMERCIAL ION IMPLANTATION EQUIPMENT

A. Introduction

The first commercial ion implanters were manufactured in 1973 [76]. The Accelerators 200 MP and Extrion 200–20 were both introduced at that time. Machines of the 1970s typically used cold cathode ion sources, which ultimately were able to produce ion currents of up to $200 \mu\text{A}$. In 1978, the first true high current ion implanter was introduced by Nova as the NV 10–80. This machine used a Freeman ion source and produced 10 mA of ion current at energies of up to 80 keV. These early ion implanters were quite complex in design and required considerable skill to set up and operate the equipment. Process capability was limited; for example, little was provided in the way of wafer cooling, particle control or charge control. Nevertheless, these machines greatly surpassed the capabilities of furnace diffusion and opened the way to present day ion implantation.

B. Implanter Architecture

Modern implanters, like their early counterparts differ considerably in their approach to beamline design. Ion implanters all include the same basic elements such as an ion source, extraction optics, analysis to separate out unwanted species, a scanning system to paint the beam uniformly across the wafer a dosimetry system, and a wafer handling system. However, the arrangement of these components to achieve the final beam on the wafer is often different. The simplest and most straightforward beamline provides only drift mode operation; that is, once the ions are extracted from the ion source, there is no further acceleration or deceleration of the ions (Fig. 12(A)). Currently, this type of operation is found only in implanters intended for high current, high dose operation. Analysis is provided by a magnet, which behaves as a mass

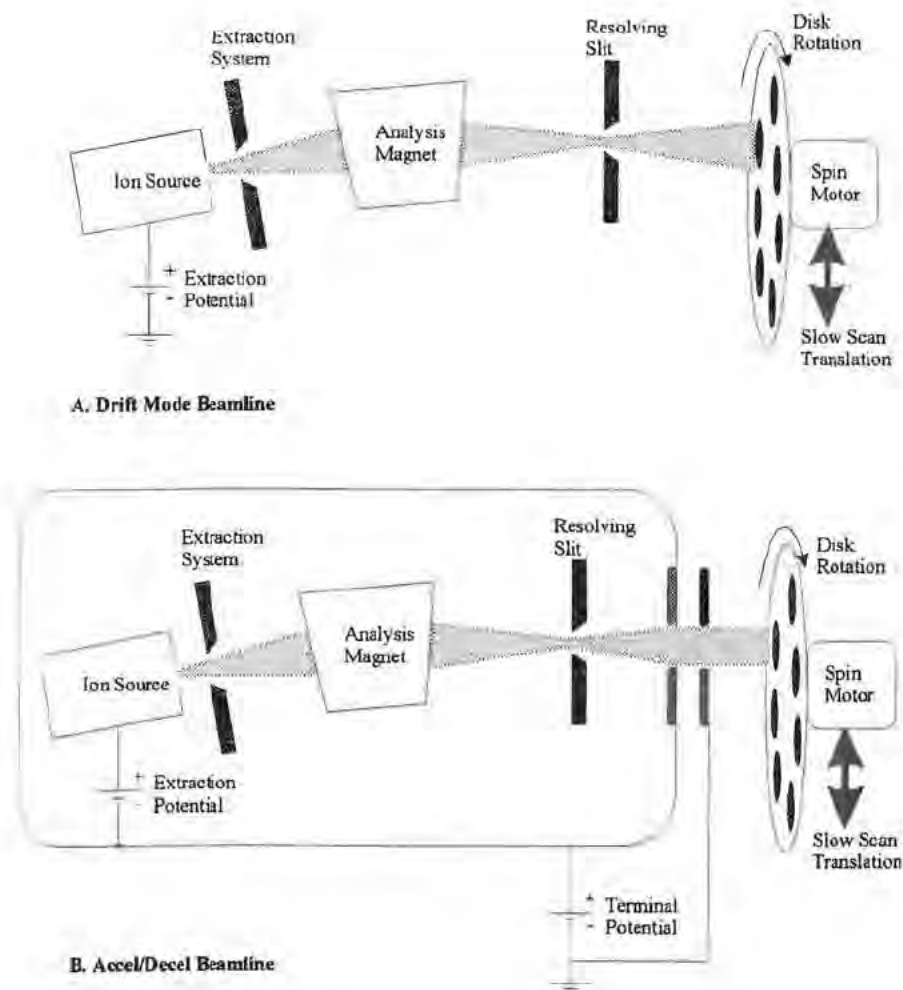


Figure 12 Illustration of high current "batch" implanter architectures.

spectrometer. In fact, magnetic mass analysis is universal in machines currently in production. Once the dopant species has been isolated in the ion beam, the beam must be painted uniformly across the wafer. In the high current implanters, which rely exclusively on drift mode operation, scanning is accomplished by a spinning disk which is translated through the beam (Fig. 12(A)).

Practical factors limit drift mode operation to ion energies below about 90 keV. At higher energies, arcing and glitching impact source extraction reliability and force a change in approach. At energies of 5 keV and below, depending on other details of the source and beamline design, it may prove difficult to obtain sufficient beam current to achieve the desired wafer

throughput. In either case the scheme shown in Figure 12(B) is normally used. Here the source, extraction and analysis systems are contained in a terminal, which is simply an enclosed metal shell held at a potential different from ground potential. If the terminal potential is above ground potential then the ion will be accelerated on leaving the terminal. This is usually termed post-(analysis) acceleration. If the terminal potential is below ground potential, the ion will be decelerated on leaving the terminal. This latter arrangement is useful for obtaining increased beam currents at low energy, particularly for boron. The total energy available from such a system for singly-charged species is just the sum of the extraction and post-accel potentials expressed as electron volts. Of course,

one way to extend the energy range of such a machine is to use ions with more than a single charge. Multiply-charged ions will increase the ion energy in proportion to their level of charge, but ion sources typically produce much less current in the multiply charged species than for singly charged. Note that while Figure 12(B) shows a single accel/decel gap, practical systems require two gaps to minimize x-ray production (see Section IV.B.1).

Acceleration and deceleration are not without problems. Deceleration typically causes a defocusing of the beam, which results in degraded transmission to the wafer. High electrical stress between the acceleration electrodes simplifies the optical design and improves beam focussing and transmission. However, the high electric fields may result in high particulate generation due to microdischarging [77]. A fundamental problem, which may occur in any acceleration or deceleration scheme, is that ions may undergo charge exchange by collision with residual gas in the beamline (e.g. $P^+ + N_2 \rightarrow P + N_2^+$). The original ion, now neutral, retains its kinetic energy and continues toward the wafer. However, if this occurs upstream of the acceleration or deceleration, because the dopant is neutral, it does not experience the electric field that is present and continues at its initial velocity. Thus, that portion of the ion current which has undergone charge exchange strikes the wafer at the wrong energy, and represents an energy contamination in the beam. Moreover, since the charge exchanged fraction is not sensed by the dose control system, which measures beam current, there will be a dose shift and possibly some dose non-uniformity. Modern machine design includes relatively large ion beams, in order to reduce space charge and improve low energy beam transmission. As a consequence, vacuum conductance down the beamline is high, so that when the ion beam impinges on photoresist wafers the resulting pressure burst can affect much of the beamline. This increases charge exchange by increasing the pressure-path length product the ion beam sees. Improving the vacuum in the beamline near the accelerating electrodes or adding a final analysis magnet is the key. Additional vacuum pumping in the implant chamber and a vacuum conductance restriction (as much as beam design will allow between the chamber and the remainder of the beamline), will help reduce the charge exchange contribution from photoresist outgassing.

Post-accel systems are widely used, not only for high current machines, but also for the lower dose machines usually termed medium current and high energy implanters. Other machine architectures are available

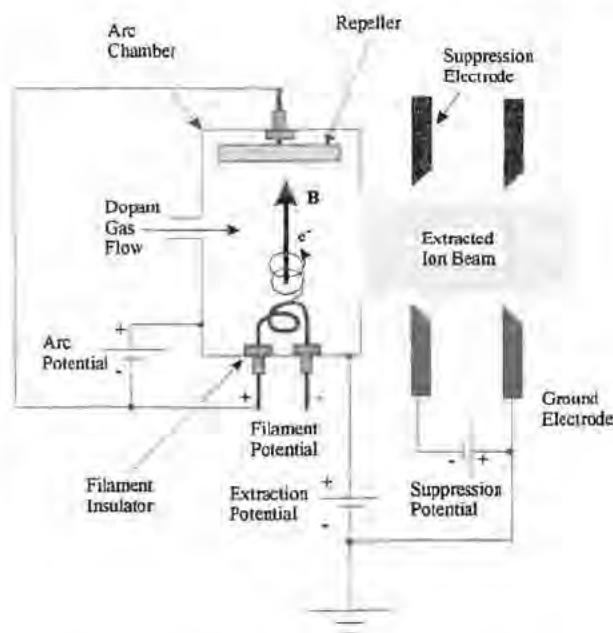


Figure 13 Illustration of enhanced Bernas ion source.

beyond those shown in Figure 12, but all are variants of the drift mode or post-accel machines shown. Several of these will be illustrated in discussions below.

1. Ion Sources and Beam Extraction

Early ion implanters used a variety of ion sources including the Freeman source, cold cathode sources, and PIG sources [78]. Recently, nearly all commercial equipment makers have adopted the Bernas source, developed by Rene Bernas in 1967. The basic configuration of the source is shown in Figure 13. Essentially the source is a small rectangular box with a gas feed tube. Typical feed gases are shown in Table 3. Gaseous source feed allows rapid changing of species for those cases where the user may want to change the implant species from batch to batch. However, some materials are not conveniently obtained as gases and for these materials a vaporizer may be used. Vaporizer feed materials are shown in Table 4. In any event the source material is introduced into the arc chamber as shown achieving a pressure in the millitorr region within the arc chamber. A thermionic filament (or cathode) isolated from the arc chamber is included to provide a source of primary electrons. These energetic primaries cause ionization of the dopant gas. As shown

Table 3 Source gases for different species

Implant species	Feed gas	Implant species	Feed gas
Arsenic	AsH ₃	Boron	BF ₃
Phosphorus	PH ₃	Silicon	SiF ₄
Germanium	GeF ₄	Argon	Ar

Table 4 Source material for vaporizer usage

Implant species	Feed material	Implant species	Feed material
Arsenic	As (metal)	Phosphorus	P (metal)
Antimony	Sb ₂ O ₃ or Sb (metal)	Indium	InCl ₃

in Figure 13 the primary electrons revolve around magnetic field lines toward the repeller. As the name suggests, the repeller is biased negatively with respect to the arc chamber, so electrons arriving in the vicinity of the repeller are turned around and spiral back toward the filament. The long electron path length gives efficient ionization of the dopant. In some Bernas source designs the repeller is not biased with a power supply but is electrically floating. In this case the repeller will charge up to the so-called floating potential, which is negative with respect to the plasma potential, and then will function in just the same way. Well-designed Bernas sources can achieve currents of 30 mA or more for arsenic and phosphorus, with filament lifetime of 100 h or more.

Figure 13 also shows the extraction geometry. The ion source is operated at a high potential relative to ground. Typically, the face of the source and the extraction electrodes contain a slit shaped opening to extract the ion beam. A simple grounded electrode could be placed opposite the ion source to provide an electric field for ion extraction. However, this would allow backstreaming electrons to pass through the extraction slit and strike the source, generating intense x-rays and adding to the extraction current. To avoid this problem the electrode facing the source is biased negatively with respect to ground. This repels backstreaming electrons, and prevents excessive x-ray production. As noted earlier, a similar suppression electrode is also required for the post-accel gap. Usually, the face of the source and the extraction slit are shaped to aid in focussing the beam. This shaping helps to ensure high transmission of the extracted beam down the full beamline.

Several variants of the simple Bernas ion source have been developed. A dual filament, dual repeller Bernas source is available from Varian [79]. The second filament improves boron fractionation and increases available multiply-charged currents. With recipes judiciously chosen to balance sputtering by phosphorus and arsenic against halogen cycling with boron trifluoride, lifetimes of several hundred hours can be achieved [80]. Still another variant on the Bernas source design is the Eaton Extended Life Source, which uses an indirectly heated cathode rather than a hot filament [81]. Removing the filament from the source arc volume much prolongs its life, since it is no longer in contact with the reactive gases and ion sputtering within the ion source. Consequently, source life is typically well in excess of 100 hours even without tailoring of recipe sequences.

2 Magnetic Analysis

Magnetic analysis is universal in all present commercial ion implanters, regardless of the architecture of their beamlines. The magnet mass spectrometer incorporated in the beamline usually includes an entrance slit, often the source slit or a part of the extraction system, and a mass resolving slit. When the charged particle enters the magnetic field the particle is bent into a circular orbit by the magnetic forces. The particle will travel in a trajectory where the centrifugal forces balance the magnetic forces or where

$$\frac{mv^2}{R} = q v B$$

where R is the radius of the trajectory, B the magnitude

of the magnetic field, m is the mass of the ion, q its charge and v its velocity. Here, since the velocity of the particle is orthogonal to the magnetic field, the usual cross product is replaced by the simple product of the magnitudes of the velocity and magnetic field. Expressing the velocity in terms of the kinetic energy, E , where

$$E = \frac{1}{2}mv^2, \text{ gives}$$

$$R B = \sqrt{\frac{2mE}{q^2}}$$

Only one radius will result in the transmission of current through the resolving slit, so the magnetic field must be adjusted to select out the desired species. The product, RB , is called the magnetic rigidity and the mass spectrometer actually selects out species according to this parameter. An important measure of the mass separation is the resolution defined as the center mass, M , for a particular peak divided by its full width at half maximum, ΔM . If two species have masses separated by a gap large compared to the lower mass divided by the resolution, then the masses will be completely separated and a high species purity can be expected. In commercial implantation equipment the mass resolution can vary from as low as 25 to as high as 100.

In most cases magnetic analysis gives very good species purity. However, there are well known cases of mass coincidences or near mass coincidences, which can be a problem. For example, when switching from boron to phosphorus, residual boron fluoride ($^{11}\text{B}^{19}\text{F}^+$) from the ion source will be present at mass 30, rather close to the mass for phosphorus (31). Allowing some time between the implants will resolve the problem as the BF^+ usually dissipates quickly. If the source contains graphite parts then $^{12}\text{C}^{19}\text{F}^+$, will also be produced, which is exactly coincident with phosphorus. In sources using molybdenum arc chambers, $^{98}\text{Mo}^{++}$ will be exactly coincident with $^{11}\text{B}^{19}\text{F}_2^+$ (mass 49), because the two have the same magnetic rigidity (the Mo^{++} will have twice the energy but twice the charge, so that it behaves as a particle of mass 49 rather than one of the mass 98). In this case a source with a tungsten arc chamber will eliminate the problem. Nitrogen often appears in the spectrum of the ion beams, due to air leaks in or near the ion source, or because the source has incorporated boron nitride as an internal insulator. Silicon implants (mass 28), often used for preamorphizing the wafer surface,

are then exactly coincident with the $^{14}\text{N}_2^+$. One solution in this case is to use $^{29}\text{Si}^+$, but because of the isotopic abundance, this entails a significant loss of beam current. In sources including graphite another difficult near coincidence occurs when these machines are tuned for $^{11}\text{B}^{19}\text{F}_2^+$ (mass 49) implants. A significant $^{12}\text{C}^{19}\text{F}_2^+$ (mass 50) current will also be found in the spectrum, and typically, commercial ion implanters do not have enough resolution to fully exclude the carbon from the resolved beam.

Other problems can occur with magnetic ion analysis, particularly when multiply-charged ion species are required. Useful currents of P^{++} and As^{++} can be extracted from Bernas type ion sources, and provide an easy way to double the energy of the implanted ion. However, phosphorus and arsenic produce dimers in the ion source, which likewise are ionized and accelerated (e.g. As_2^+). If these collide with residual gas, the dimer may decompose into two fragments with approximately equal energy. One of the fragments will be charged. This fragment will have exactly the same rigidity as the doubly-charged ion. Rather than a contaminant in the form of an undesired species, this gives a contaminant in the form of an undesired energy. The only solution in this case is to provide additional energy filtering, which usually takes the form of a decelerating einzel lens. If these issues are taken into account in setting up the equipment, then magnetic separation is very effective and serves the machine user well.

3. Beam Scanning and Dose Control

The use of a spinning disk for implantation has already been noted. The rotation of the disk provides one axis of scan, while the translation provides the other. Typically, disk rotation speeds are on the order of 1000 RPM and while the disk translates at speeds of the order of 10 cm/sec. By distributing the beam power over many wafers the wafer cooling requirements are eased and less effective, but more easily implemented cooling techniques may be used. All spinning disk implanters use elastomeric cooling, where thermal contact in the vacuum is achieved by using centrifugal force to press the wafer into a thin sheet of RTV bonded to the cooled disk pedestal. This technique allows implantation of photoresist-covered wafers at beam powers up to 5 KW, and gives ultimate wafer temperatures of below 100°C [82]. Since centrifugal clamping is utilized, most modern machines eliminate mechanical wafer clamping in

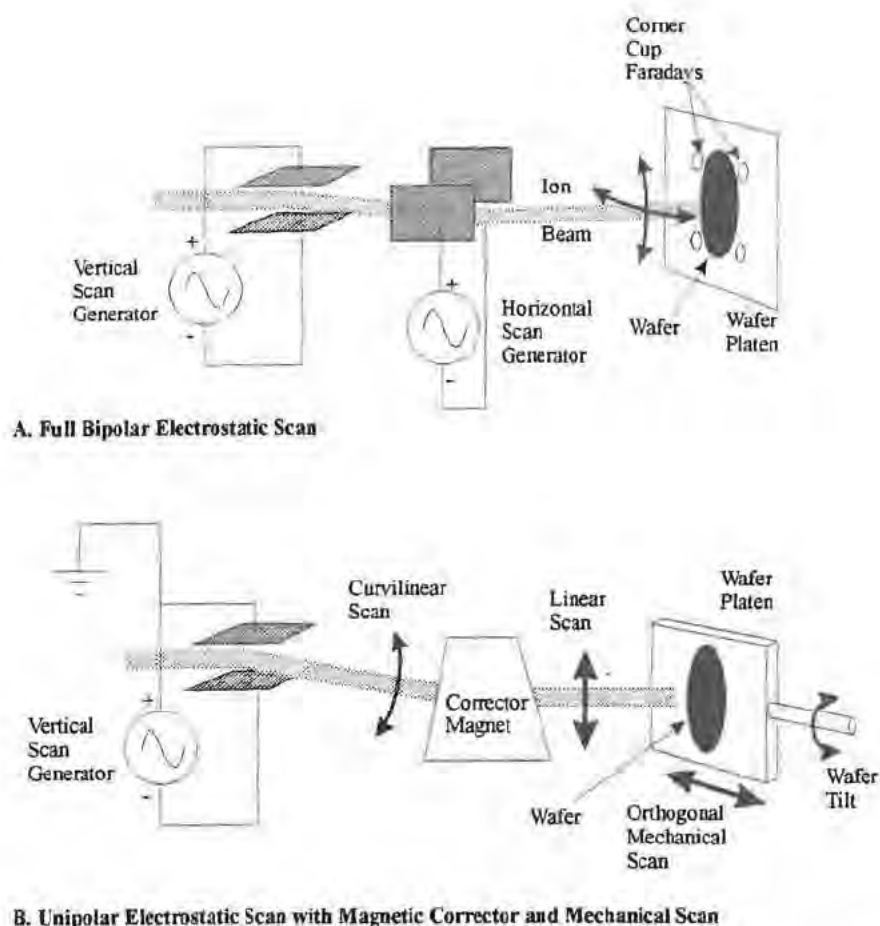


Figure 14 Illustration of beam scanning systems for single wafer implanters.

favor of simple retention systems, which hold the wafer in place when the disk stops spinning.

Alternative scanning systems are shown in Figure 14. These scanners are found primarily in medium current implanters, which typically are post accel machines, because of the need for higher energy. The scanning may be incorporated in the beamline either before the post-accel or after. If the scanner is incorporated before the post-accel gap, the post-accel electrodes must be wide enough to allow the full scanned beam to pass through. Figure 14(A) shows full electrostatic scanning. This system gives good uniformity and dose control, but has the disadvantage that the scanning is curvilinear, that is, the ion beam is deflected through an angle. As a consequence, the implant angle changes over the wafer. In many instances channeled implants are required, and for these implants it is essential that there be

no change in implant angle. Of course, in spinning disk scanning the beam is stationary and implant angle variations can be quite small depending on implanter design [83]. It is also possible to minimize angle variation in electrostatically scanned machines. This is shown in Figure 14(B), where electrostatic scanning is combined with a correcting dipole magnet [84]. Here the scanner is located at the focus of the corrector magnet resulting a linear and parallel scan. Scan correction also can be accomplished by using electrostatic elements, in which case the correction scheme can be incorporated into the post-accel electrode system [85]. In either case, the electrostatic scanning is usually combined with mechanical scanning as shown in Figure 14(B).

The scan systems in Figure 14(A) and 14(B) are usually encountered in medium current machines. These machines employ single wafer (serial) processing

rather than batch processing. Because of the lower beam powers, it is not necessary to distribute beam power over a number of wafers. Because the wafer platen is not rotating, it is possible to use a wafer clamp and use either elastomeric or gas cooling [82]. Mechanical clamping is often a source of particulates and in serial processing this is made possible by electrostatic clamping [86]. This can be combined with gas cooling in critical applications.

4. Dose Control

The scanning system and the dose control system are usually coupled together in a closed loop feedback scheme, to ensure consistent and uniform wafer dosing. Dose control, as mentioned earlier, involves the measurement of ion beam current and the exposure time for beam on the wafer. Current measurement requires the use of a Faraday and can suffer pitfalls [87], but these are usually well taken into account by the designers. Figure 15 shows the dose control arrangement for batch spinning disk machines. There are two philosophies involved in the current measurement, continuous measurement and sampled measurement. Sampled measurement is shown in Figure 15(A). Here the Faraday measures a pulse of current coming through a slot in the disk. Even at a fixed beam current the current pulse will vary as the disk scans across its range, because of the higher rotational velocity with increasing radius on the disk. However, the same effect occurs on the wafer and it is necessary to decrease the scan velocity as the beam moves out the disk. In other words, the slow scan speed must vary in inverse proportion to the radius of the disk. The sampling slot accomplishes this automatically. The current pulse in the Faraday is integrated and the scan speed is adjusted in proportion to the integrated charge measured. This also accounts automatically for any beam current drifts, or for momentary beam dropouts (glitching).

Continuous measurement (Fig. 15(B)) usually involves incorporating the wafer holder in the Faraday, which is often mechanically and electrically more complex. In this case, the reciprocal radius variation of the scan speed must be accomplished through software. While there are strong proponents for each type of system, both systems can work very well, and it is not uncommon for implanter manufacturers to have a high current machine using one approach and a medium current machine using the other. Both types of system control can achieve the 0.5%

uniformity and 0.5% dose repeatability that is required for semiconductor fabrication.

5. Other Process Issues

In the 1970s and early 1980s, machine development focused almost exclusively on beam current, energy and dose control. In recent years much of the attention of the machine designer has gone into the process issues. Implanter designers are now much more aware of the requirements of implanter users, and work much more closely with implanter users. Issues like wafer temperature, automation, wafer handling, throughput, safety, particulate and metal contamination, device charge control, implant angle control, beam current density, uptime, reliability and user cost of ownership (CoO) are integral to the design of modern implanters. Indeed, it is these issues which have shaped the evolution of implanters over the past decade, and these issues continue to drive this evolution.

C. Practical Implant Systems

1. Introduction

Due to space limitations it is not possible to do more than touch on a few examples of commercial ion implantation equipment. The examples chosen are for illustrative purposes only and, certainly, no effort has been made to sort out these machines in any other manner.

2. Varian E220 Medium Current Implanter

Figure 16 shows a beamline schematic for the Varian E220 medium current ion implanter. This implanter will produce up to over 2 mA of beam current for phosphorus at singly charge energies of up to 220 kV. The machine utilizes a Bernas ion source with up to a 70 kV extraction voltage. The beamline incorporates an energy filter to protect against dimer contamination in multiply-charged implants. Very simply, this is an electrode set that is biased at near the extraction voltage. Dimer breakup products do not have enough energy to pass through this retarding field, while the multiply-charged ions do. Since the beam path length is relatively long, a magnetic quadrupole is used to control spot size on the wafer. Scanning is accomplished by a unipolar electrostatic deflector. The straight plate is held at ground potential, while the curved plate is operated at a negative potential with a sawtooth waveform. The beam is recollimated by a lens magnet.

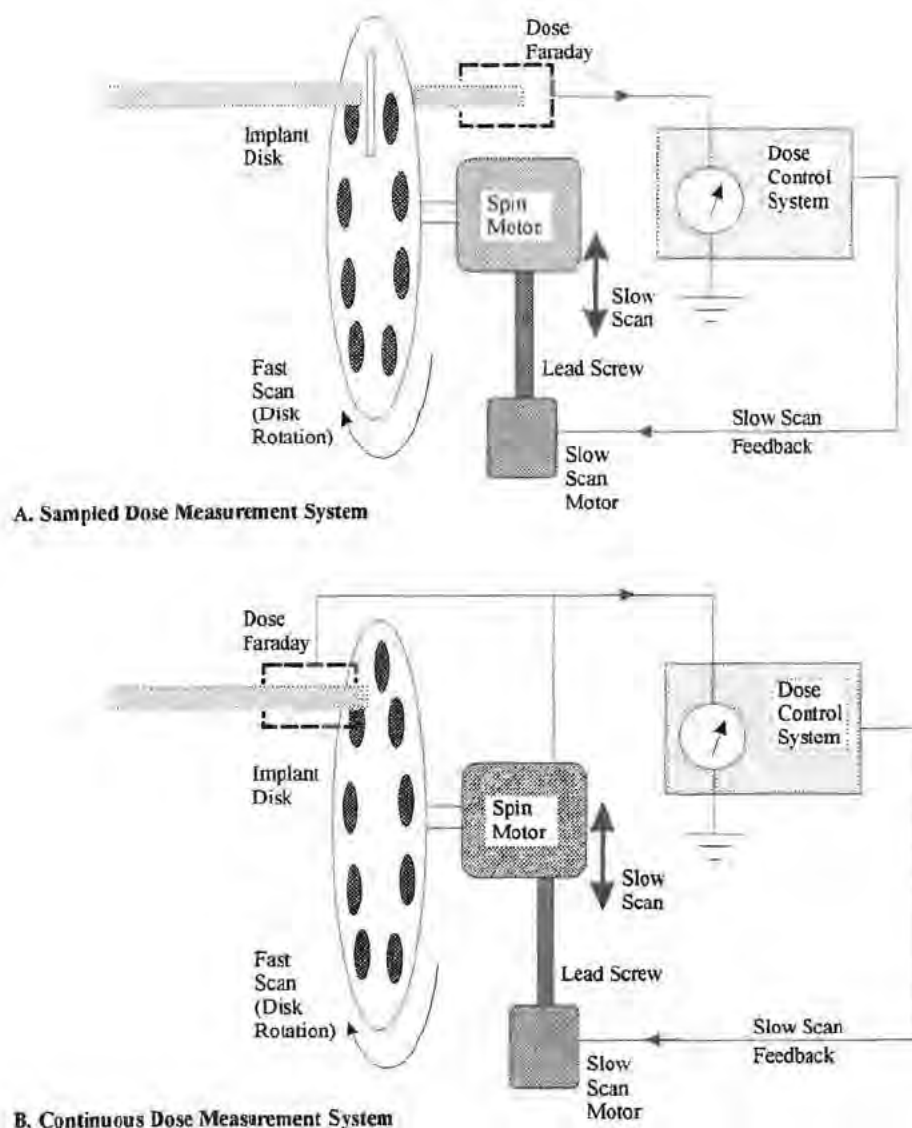


Figure 15 Illustration of dosimetry systems for batch implanters.

Since the beam is scanned before post acceleration, the post accel electrodes must be wide enough to accommodate the full scan beamwidth. This is quite wide indeed, given that the beam must be able to scan off of a 200 mm wafer in both directions by at least the beam radius. The slow scan is accomplished by moving the wafer stage mechanically in the plane perpendicular to the wafer. Note that a single wafer is implanted at one time. Throughput can be as high as 200 wafers per hour.

Dose control in this machine is quite sophisticated and illustrates some of the principles of modern

implanter operation. At the start of a batch of wafers, the traveling Faraday is moved across the scanned beam to determine the current profile. If the profile is not completely uniform, then a correction is developed for the scanning waveform to modify the scan. The process is iterated until the required degree of uniformity is reached. During implant the machine control computer keeps track of dose as a function of position on the wafer. In the last slow scan any glitching, which reduced the dose locally, or any current drifts are taken into account, to ensure a uniform and consistent implant.

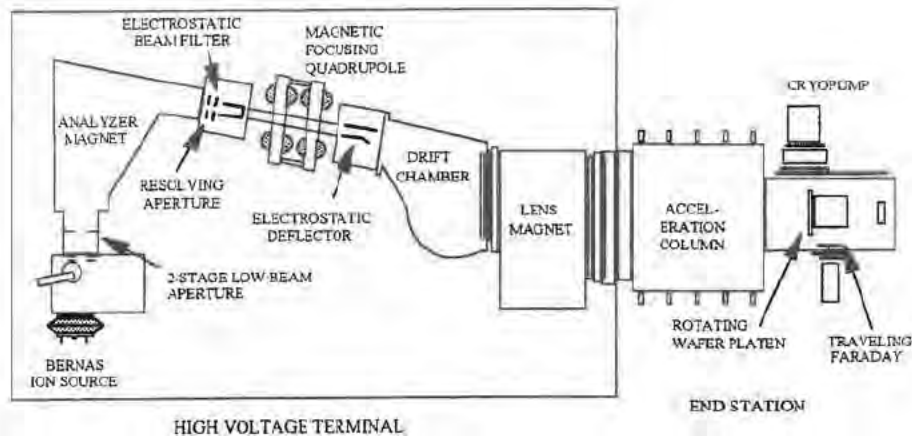


Figure 16 Schematic diagram of Varian EZZO medium current implanter.

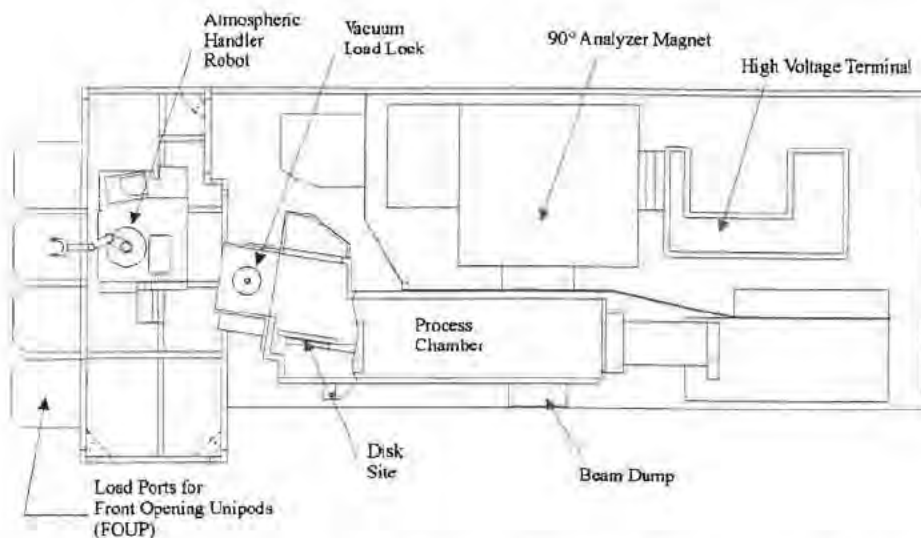


Figure 17 Schematic diagram of Applied Materials xR80 LEAP 300 high current batch implanter.

Not shown in Figure 16 is the wafer handling. The E220 incorporates vacuum load locks. The wafer cassette, which typically holds 25 wafers, is loaded placed in one of the load locks, a door is closed and the lock is evacuated. Wafers are then handled by a backside pick to orient the wafers and then place them on wafer platen. The wafer platen is rotated to a horizontal position during loading, and then moves up vertically for implant. The platen can achieve an implant tilt angle for $+60^\circ$ to -60° degrees. In addition, the azimuthal angle can be set or varied continuously during implant. Dose uniformity and

repeatability are within 0.5%, as is the case with most commercial equipment.

3. Applied Materials xR LEAP 300

Figure 17 shows a schematic for the xR LEAP 300. This machine has a very compact layout (2.2 meters wide) and will operate with wafers up to 300 mm in diameter. The endstation is interesting since it can utilize the front opening unipods (FOUP). The FOUP is a sealed mini-environment in which the wafer cassette is transported. This arrangement alleviates

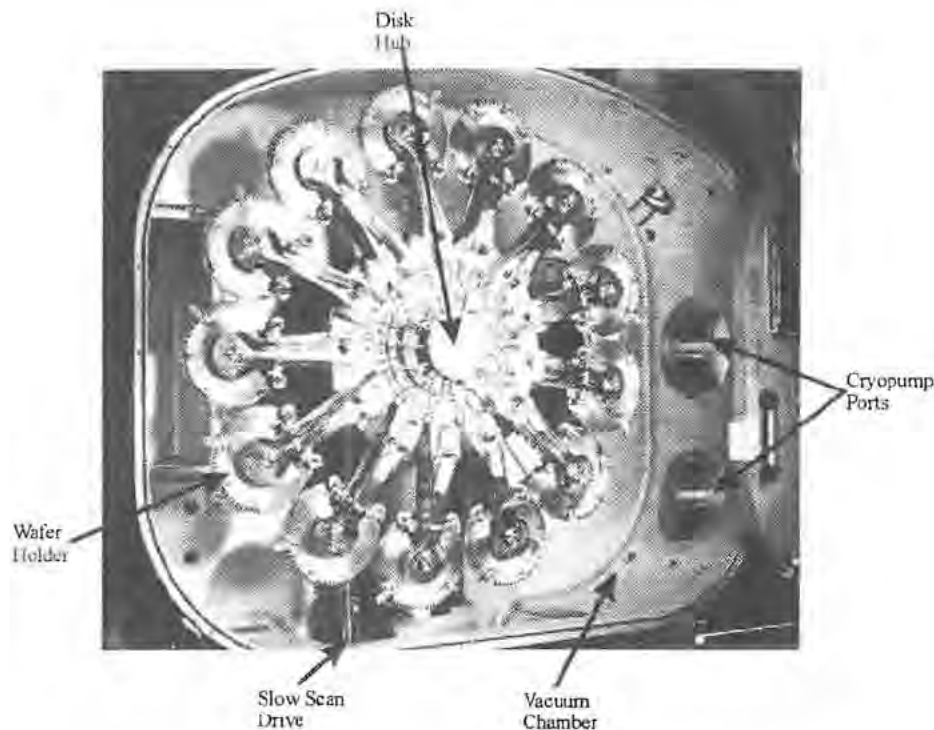


Figure 18 Process disk (wheel) in the Applied Materials xR80 LEAP (backside).

the requirements for extreme cleanliness in the environment in which the cassettes are moved. Inside the FOUPs the air must be extremely clean with very low particulate levels, and similarly inside the machine where wafers and cassettes are handled the air must be very clean. In any event, the wafers are transferred to a vacuum load lock for implantation by an internal robot in the machine.

The xR LEAP 300 is a batch machine and so utilizes a disk (wheel), shown in Figure 18. The entire disk rotates and is translated in vacuum to provide both axes of scan. In this machine, to minimize metallic contamination by ion beam sputtering, the disk is cut away leaving only the wafer holders and the support arms. Two cryopumps are employed on the vacuum chamber to minimize the pressure burst that occurs when the ion beam initially strikes photoresist covered wafers.

The xR LEAP 300 can use either the standard Bernas source or the recently developed UltraLife source, which is a Bernas source with an indirectly heated cathode (as described earlier). Two versions of the machine are available in the same package: a drift mode machine with 80 kV of extraction, and a post accel machine which provides an additional 40 keV of energy (120 keV total). The machine is auto-

matically tuned by the computer, and tracks wafers and recipes automatically. Wafer throughputs up to 235 wafers per hour can be achieved.

4. Eaton GSD HE High Energy Implanter

Figure 19 shows a beamline schematic of the Eaton GSD/HE machine. What distinguishes this machine is its unique beamline design. The post acceleration system is an rf linear accelerator operating at 13.56 MHz. Electrostatic quadrupoles are incorporated in the beamline, to maintain a tight beam throughout the beamline. Radiation (x-rays) are minimized by the fact that no gap has an excess of 80 kV, simplifying the shielding. This machine is available in two versions, the GSD/HE and GSD/VHE. The HE implanter can achieve useful beam current from 10 keV to 1 MeV. At 1 MeV, 1 mA of B+ can be obtained. Tuning is fully automated. The VHE implanter achieves still higher energy. The machine produces 1 mA B+ at 1.7 MeV, 300 μ A B++ at 3 MeV and 200 μ A P+++ at 5 MeV.

Like the Applied Materials implanter, this is a spinning disk machine. The 300 mm version of the machine includes FOUP capability, along with an

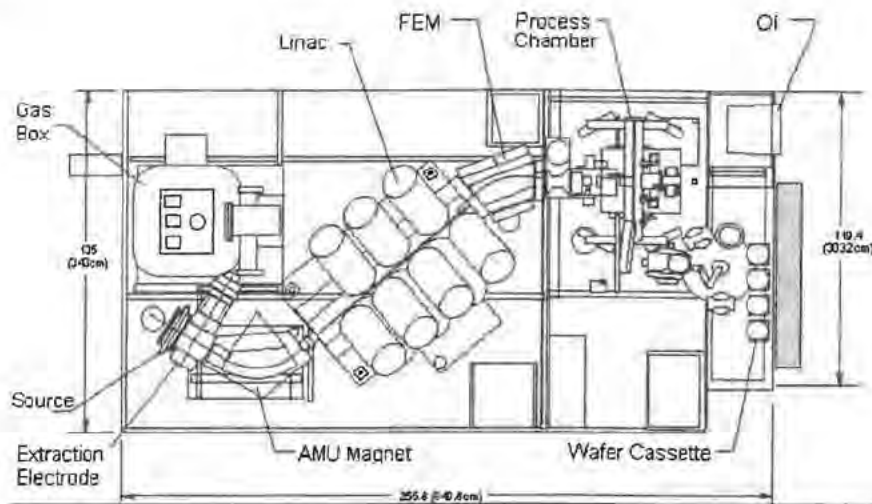


Figure 19 Schematic of Eaton GSD/HE high energy implanter.

internal stocker for storing work in process. The disk arrangement is unique in that it can be tilted by $\pm 10^\circ$ in two planes. This is very convenient for quad mode implants, that is, implants which must be performed at four different tilt angles. The reason for doing this is to avoid shadowing of the ion beam by the photoresist. In any event, such implants can be done without removing wafers from the disk, reducing particulates and improving throughput.

V. PROCESS CONTROL IN ION IMPLANTATION

A. Introduction

Ion implantation is a complex process. It involves the generation of intense beams of ionized doping species, their acceleration to a required potential, and delivery to target materials with widely different surface properties, such as crystal structure, resistivity, possible coverage with photoresist masks, etc. This complicated combination of numerous equipment and process related variables often yields implant process results that differ, sometimes dramatically, from originally targeted parameters. Thus, to achieve required process results, ensure repeatability of the implant process and, in certain cases, to avoid major implant errors, it is extremely important to understand the

key process variables for various types of implants, and to implement appropriate process control steps and procedures.

The list of the most important implant process parameters which must be monitored by the implant process engineer is quite long. It includes: implantation dose; depth distribution of the implanted species in a target material; uniformity of the above parameters across the wafer; nature and amount of contaminants introduced to the wafer during the implant process; occurrence of ion channeling in the crystalline implanted materials; severity and magnitude of charging stress imposed by the ion beam to the insulating structures on implanted wafers (such as gate oxides); and, finally, various manifestations of the effects of ion beam heating and beam interaction with photoresist masks. Many of these processes are interrelated. For example, channeling of implanted dopant ions in crystalline material, if allowed to occur, leads to changes in sheet resistivity of the implanted layer, which can easily be confused with dose error. Examples of similar interactions are numerous. Thus, the key factors in designing and sustaining robust implant processes are (1) understanding the physical mechanisms and materials properties responsible for specific phenomena; and (2) the implementation of process control procedures, involving various analytical techniques, which allow for root cause identification for observed process variation, and for the subsequent design of appropriate corrective actions.

B. Control of Implanted Dose

The most common cause of implant dose errors is the charge exchange between ions in the beam, and atoms and molecules of residual gas in the implanter beamline [92]. The physical mechanism of such charge exchange involves an electron exchange between the accelerated ionized species, and an atom (molecule) of residual gas in the ion path's vicinity. As a result of such a charge exchange, the momentum of accelerated dopant remains virtually unchanged. This means that if the charge exchange occurred in the section of beamline *after* the analyzing magnet, then affected dopant atoms will be implanted into the wafer, and will produce the same effects as ions which did *not* experience charge exchange. Since the implanted dose is determined through the integration of beam current as measured by the Faraday, any changes in the charge state of even a relatively small fraction of ions in the beam could lead to dose errors, unless properly compensated. In beam neutralization, when a fraction of ions in the beam captures electrons from residual gas atoms, an overdosing could occur if the implanter dosimetry system is not set to account for such interaction. Ion neutralization is dominant at low to medium ion energies. In high energy ranges, electron stripping becomes a dominant charge exchange reaction. In this case, the interaction of ionized species with residual gas results in the removal of an additional electron from the ion. This increases electrical beam current, as measured by the Faraday, without increasing the corresponding particle flux in the beam. As a result, underdosing is possible, unless the implanter dose control system compensates for electron stripping.

Dominant charge exchange reaction (neutralization versus stripping), which occurs when the beam interacts with residual gas, depends on ion species, its initial charge state and energy, and residual gas chemical composition. It was suggested that electron loss (stripping) is more probable when ion velocity exceeds orbital electron velocity [92]. Other theories predict slightly different cutoff energies for charge exchange interactions which result in electron stripping [93,94]. Ion neutralization can be described by the differential equation:

$$dn_i = -n_0 \sigma N dx \quad (8)$$

where n_0 is initial ion flux, σ is the cross section of charge exchange reaction, N is the volume concentration of residual gas atoms in the implanter beamline, and x is the length of the beam path after

the mass separation.

$$n_i = n_0 \exp(-\sigma N l) \quad (9)$$

Equation (9) represents the solution of Eq. (8). If particle flux were replaced with initial beam current and current as measured by Faraday, and concentration of residual gas atoms is converted into a pressure (P) in the implanter beamline, then (9) could be rewritten as

$$I_i = I_0 \exp(-\sigma N l) = I_0 \exp(-KP) \quad (10)$$

where

$$K = \sigma \frac{N}{P} l \quad (11)$$

Equation (10) is deployed in the dose control system of Eaton high current implanters to compensate for charge exchange effects between implanted ions, and residual gas. It is important to note that pressure in the implanter beam line is not constant. It varies from its baseline residual value, which is typically in the range of upper E-7 to low E-6 torr, when implantation is performed in wafers not covered with photoresist masks, but can easily be in the E-4 range during implantation into photoresist-covered wafers. When pressure in the beamline is low, then actual dopant flux in the beam is accurately represented by the current measured by Faraday, and little or almost no correction is required. It is when implantation is performed into a photoresist-covered wafer that the pressure-dependent dose correction is used.

In the case of high energy ion implantation, when electron stripping charge exchange reaction is the dominant process, beam current correction is described by Eq. (12) below

$$I_i = I_0 [1 + (\gamma - 1) (1 - \exp(-\sigma N l))] = I_0 [1 + (\gamma - 1) (1 - \exp(-KP))] \quad (12)$$

Derivation of this relation is more complex than for (10). It can be found in [95] and involves solving the system of two differential equations which describe both beam neutralization, and stripping. In Eq. (12) the factor γ is a final (asymptotically) ion charge state, as in an indefinitely long path length of residual gas. Its values are tabulated in the look-up table accessible by the computer controlling the dosimetry system, and are invisible to the user. It is important to note that in the case of beam neutralization, when the final charge state is zero ($\gamma=0$, e.g. all ions would

neutralize), (12) converges to (10). Dose correction based on (12) is employed in Eaton's GSD-HE family of high energy implanters. Simple empirical procedures for finding the coefficient K used in both (10) and (12) are described in [96]. Implanters from Applied Materials and Varian rely on different approaches for dealing with charge exchange reactions between the beam and residual gas. The 9x00 and XR-xx families of high current implanters from Applied Materials have an open loop dose control system. For this approach the beam current is measured each time during the slow scan of the process disk, when the beam is off the wafer, and when photoresist outgassing effects are minimal. During the fraction of wafer scanning cycle when the beam is on the wafer, and photoresist outgassing leads to pressure rise, the beam current readings from the Faraday are used only to monitor beam dropouts (glitching) and other critical errors. Otherwise, the beam current is assumed to be constant. In the VIISion family of high current ion implanters from Varian, the process disk and hardware for charge neutralization (plasma electron flood) are part of the implanter dosimetry system. Thus, charge exchange between the ions and residual gas which occurs in the area in front of the wafers has minimum impact on implanter dosimetry, since the total charge in the beam (ions plus ionized molecules of the residual gas) remains unchanged, and is registered by the implanter dosimetry system in its entirety. A dosimetry system utilizing the latter approach provides continuous beam monitoring, but it is more complex both mechanically and electrically (see Section IV in this chapter). An additional mechanism for dose errors and energy contamination exists during implantation of doubly-charged phosphorus and arsenic ions. In general, the problem can be encountered for any species which can form molecular dimers, e.g. P_2 and As_2 , as in the case of phosphorus and arsenic. Both species are generated by an ion source as ionized atoms (e.g. P^+ , P^{++} , As^+ , As^{++}) and as ionized dimers (P_2^+ and As_2^+).

As a result, whenever a beam of doubly-charged ions is tuned, beam contamination with singly-charged ions of the same species having one-fourth of the target energy can occur. This happens when a fraction of single charged dimers extracted from the source dissociates prior to being analyzed. Dissociation can occur due to dimer collisions with residual gas atoms. Dimer dissociation results in the formation of a neutral atom, and a singly-charged ion of the tuned species, each having an energy equal to one-half of the extraction potential, or one-fourth of the final energy

for the doubly-charged species. Since the magnetic rigidities of the singly-charged ions, having one-fourth of the target energy, and doubly-charged ions of the same species having a target energy are the same (see Section IV), then ions in both charged states will pass through the analyzed magnet. This will result in corruption of an as-implanted depth distribution, and in overdosing caused by a lower charge per ion for singly-charged ions as compared to doubly-charged ions. To avoid this problem, it is necessary to monitor the depth distribution of the implanted species during initial process setup, and subsequently check the relative intensity of dimer peak and the peaks of singly- and doubly-charged species in the mass scan.

C. Charging and Gate Oxide Integrity

The electrostatic potential of high intensity ion beams can easily reach tens and even hundreds of volts, unless compensated with electrons. Electrostatic beam potential in excess of ten volts, and even less for the most charge-sensitive structures, can induce current flow through the dielectric that causes either dielectric breakdown, or wearout. Dielectric wearout occurs due to the generation of latent defects in the SiO_2 structure. These defects, when their concentration is below critical value, result in the reduction of dielectric life expectancy during normal operating conditions of the final product. The high sensitivity of gate oxides to charging stress during ion implantation is due to the fact that their thickness is well below 100 Å, for most device generations currently in mass production, and continues to decrease with the introduction of every new device generation. The breakdown electric field for SiO_2 is about 12–13 MV/cm. It can be reached at beam potentials as low as 6 V for 50 Å thick gate oxides typical for 0.25 micron CMOS devices. This imposes stringent requirements for beam space charge neutralization with electrons, and dictates a reduction of electrostatic beam potential to several volts.

A number of factors, besides that of peak beam potential and oxide thickness, influence gate oxide sensitivity to charging in real life devices. Among them are I-V characteristics of beam plasma [96], and photoresist coverage of the area adjacent to the gate [97]. Also influencing device sensitivity are the structure of the charge-sensitive device, and, specifically, the type of Si doping (n or p -) under the gate oxide, the ratio of the gate charge collection area and of the gate itself, and gate geometry (exposed sidewalls or protected with wall spacer). In most cases it is

virtually impossible to predict accurately a correlation between device yield and beam characteristics, such as peak beam potential. For this reason, the most common approach to process control of charging effects is to set a limit on an easily measurable beam characteristic, when no device yield loss occurs. One of the most common monitored beam parameters is peak beam potential, as determined by in situ charging monitors. Modern high current implanters have charging sensors integrated into the process disk. Detailed descriptions of such a sensor and its operation can be found in [98]. Still, to determine the upper limits for positive and negative swings of beam potential that will ensure no yield loss in device manufacturing, it is necessary to establish an actual correlation between device yield and charge monitor response. Another important parameter to monitor is the residual pressure of gas (usually argon or xenon) bled to the process chamber. Even though the electrons required to compensate for positive beam space charge are supplied by either plasma electron flood or secondary electron flood, the gas supply which is required for operation of either type of hardware also plays an independent and essential role in space charge neutralization. This is accomplished through the generation of low energy electrons on a beam path. A charge exchange reaction responsible for this is:



where I^+ is an implanted ion, A is a residual gas atom or molecule and e^- is a free electron which results from ionization of residual gas. Electrons generated through ionization of residual gas are trapped by positive beam potential, while low energy, positively-charged atoms of residual gas are repelled from the beam. Detailed analysis of this process was presented by Holmes in [99]. Monitoring of the beam gas pressure and charge monitors response is a valuable process control tool, which can indicate deviation of the process from its baseline and be used to trigger further investigation. Still, actual information about the extent of gate oxide charging damage can be obtained only by either measuring the yield of actual devices, or by using charge-sensitive short loop structures. Due to cost and turnaround time considerations, monitoring charging damage using short loop test structures is the preferred and most commonly used approach.

Measurements of gate oxide (GO) charge-to-breakdown (Q_{BD}), voltage-to-breakdown (V_{BD}) and time-to-breakdown (T_{BD}) with MOS capacitors are the most widespread methods of evaluating charging

damage using short loop structures. These measurement techniques rely on the ability of high quality oxides to pass certain, typically around 10 C/cm^2 , electric charges prior to oxide breakdown. Any charging damage introduced to the gate oxide during implantation or plasma processing will result in a reduction of the charge which can be forced through the oxide during subsequent measurements. Thus, measuring a difference between Q_{BD} on the unimplanted and implanted structures, it is possible to evaluate charging damage introduced during ion implantation.

In the typical MOS structure used for Q_{bd} or similar measurements, a poly-Si antenna is attached to thin gate oxide. Large antennae increase the charge collection area of the test structure, and the sensitivity of the structure to the charging effects. Several other slightly different designs of test capacitors are also commonly used. They differ by having either perimeter-intensive or area-intensive antennae, that are protected or exposed to the beam edge of the gate stack. Usually, up to several hundred clusters of MOS capacitors with different ratios of gate-to-antenna areas are fabricated on a single wafer. This allows for the matching of the sensitivity of test structure array to induced charging stress, for a large variety of implantation conditions which may need to be evaluated. Thus, test wafers with a properly designed charge-sensitive structure can be used for evaluation of wafer charging for implants at beam currents, ion doses and energies. Requirement for having a large number of similar capacitors on single wafers is dictated by the statistical nature of the charging damage introduced to gate oxides. Typically, half of the test capacitors on a wafer are measured prior to and remaining after the implantation. In order to obtain accurate and consistent results, it is necessary to perform statistical analysis of collected data. The data collected from test structures are usually presented as a Weibull plot (Y-axis has an $\ln(-\ln(1-F))$ scale), (F is the cumulative failure rate), and X-axis is the parameter tracked (Q_{BD} , V_{BD} or T_{BD}). This format allows for fast comparison of charging damage for different conditions. A typical example of a Weibull plot for time-to-breakdown measurements is presented in Figure 20.

SPIDER and commercially available CHARM-2 structures (see Fig. 21) are two other types of test devices frequently used for evaluation of wafer charging. CHARM-2 structures are based on E^2 PROM devices with large charge collection antennae attached to the control gates [101]. This

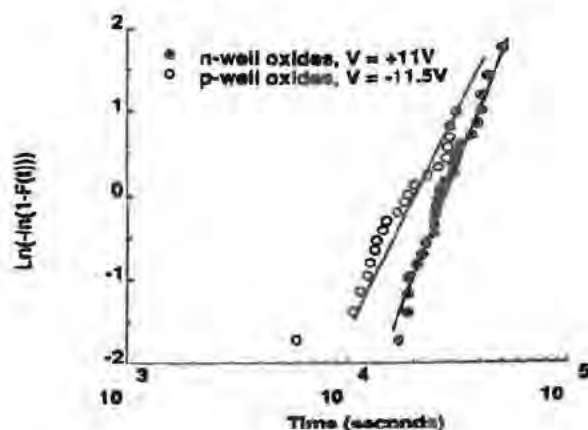


Figure 20 Typical T_{BD} Weibull plot of the cumulative failure rate of MOS capacitors stressed with positive and negative voltages.

structure allows the gauging of peak potentials induced by the ion beam. These potentials are determined through measurements of threshold voltage shift in devices after the implantation. CHARM-2 wafers contain clusters of charge-sensitive devices located on the wafers. Individual structures in each cluster have charge collection antennae connected to the substrate, with shunts having a different resistivity. This allows the determination not only of peak beam potentials, but also J-V characteristics of the beam plasma. This additional information is essential since electric current forced through gate oxides is the ultimate cause of charging damage. An analysis of peak voltages induced to the structures located in different areas on the wafers allows the mapping of beam-induced potential across the wafer.

SPIDER structures are transistor based charge-sensitive devices [102]. They consist of a full scale CMOS device fabricated up to a first level of metal, with large charge collection antennae connected to the gate stacks of each individual device to increase sensitivity to charging. Deviation of PMOS and NMOS device electrical characteristics is used to estimate charging damage during ion implantation. One of the advantages of using SPIDER structures is that charging damage is gauged through monitoring of the very same electrical characteristics, most commonly threshold voltage, which would deviate from targeted values in real devices when exposed to charging. Electrons tunneling through gate oxides under beam-induced charging stress generate oxide defects in the bulk of the oxide and at the Si/SiO₂

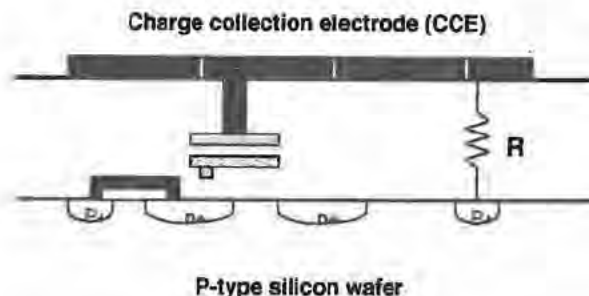
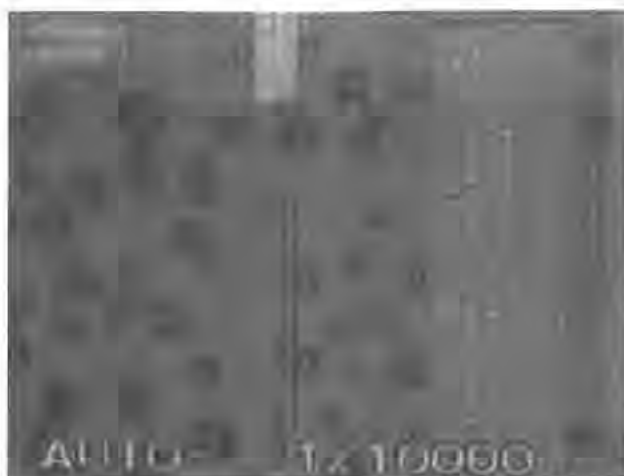


Figure 21 CHARM-2 charge flux sensor.

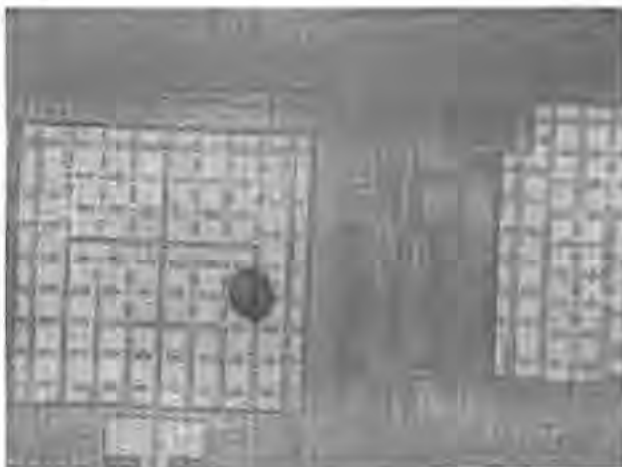
interface. A certain fraction of these defects can trap electrons and holes, resulting in threshold voltage shift. Thus, higher charging stress leads to an increased defect generation rate, and respectively to a greater voltage shift. Some oxide defects remain in an electrically neutral state and, therefore, do not contribute to V_t shift. Information about electrically inactive defects is important because they are likely to trap electric charge during device operation, or manifest themselves in reduced device life expectancy. The concentration of all oxide defects located within the Si/SiO₂ interface can be measured with a charge pumping technique [103–105] using SPIDER structures. Since measurements of device electrical characteristics are non-destructive, different types of techniques can be applied to the same test device for charging evaluation.

D. Wafer Cooling and Photoresist Mask Integrity

The high beam-power easily achievable in high current and high energy implanters can substantially increase the temperature of implanted wafers unless effective cooling is deployed. Increased wafer temperature during ion implantation can compromise process control in a number of ways. The first group of phenomena is due to a reduction in the rate of implantation-induced damage formation in implanted crystalline materials. This will result in increased dose requirements for amorphizing silicon [106], thus compromising the quality of amorphizing implants and causing a possibility of run-to-run deviation of implanted dopant distribution for high dose implants. Elevated temperature may also result in the formation of defect complexes with high thermal stability and, in extreme cases, even trigger radiation enhanced



(a)



(b)

Figure 22 Photoresist popping under excessive beam load (a); redeposited PR flake (b).

diffusion of the implanted dopant [107]. All of the above phenomena can affect both depth distribution and activation of implanted atoms, thus compromising implant process control. Still, the most common manifestations of excessive wafer temperature during ion implantation are related to properties of photoresist masking layers. Even a relatively moderate temperature rise due to beam heating will cause severe photoresist (PR) problems. PR temperatures in excess of 100°C may cause variation in critical dimensions of PR masking layers, and for severe heating conditions cause PR burning [108], blistering, flaking and popping [108,109], and generation of high particle

levels. Figures 22(a) and 22(b) show an example of photoresist popping (a) and redeposited PR flake (b) [109].

Maximum implanted wafer temperature rise depends on a variety of factors, including ion beam energy and current, dose of implanted ions and efficiency of wafer cooling in the implanter. For low dose implants the wafer temperature is limited by the heat mass of implanted wafer. Thus, for doses up to approximately 10^{14} cm^{-2} for the typical energy range for medium current applications, and up to 10^{13} cm^{-2} for most high energy applications, maximum wafer temperature rise will not exceed 30–50°C. This makes wafer cooling requirements not very stringent. For higher implant doses, wafer cooling must be deployed in order to prevent excessive temperature rise. Two methods are widely used for wafer cooling. Both of them rely on a conductive cooling to transfer heat from the wafer to the pad. In serial implanters, gas cooling [110] is widely used. Heat conductivity is substantially increased when gas is introduced between the backside of the implanted wafer and the wafer pad. The low efficiency of conductive cooling without the gas is due to a limited contact area between the backside of the wafer and the pad. This area is very small due to roughness of the wafer and pad contact surfaces. Thus, the gas between the wafer and the pad acts as a heat transfer media, providing a conductive path to the heat, from the wafer, to the cooled pad. Well-designed gas cooling systems can have a cooling coefficient of 15–30 $\text{mW/cm}^2\text{°C}$, depending on pressure and gas used. A detailed description of the gas cooling can be found in [110].

The most common technique for measuring wafer temperature during implantation is placing temperature sensitive stickers to the back or front side of the wafer. The stickers contain compounds with different pre-adjusted melting points. Once a melting temperature is reached, the color of the compound changes. Placing stickers on the backside of the wafer is preferred, since this protects the sticker from direct exposure to the ion beam. For this approach, in order to maintain measurement accuracy, it is important not to compromise thermal contact between the backside of the wafer and a wafer pad by the presence of a sticker. This is possible only when an adequate recessed area is present on a pad surface. Alternatively, the sticker is placed on a front side of the wafer. In this configuration the sticker must be shielded from direct exposure to the beam. Heat from the wafer will be transferred to the sticker laterally. This does not cause significant error in measurement of wafer temperature

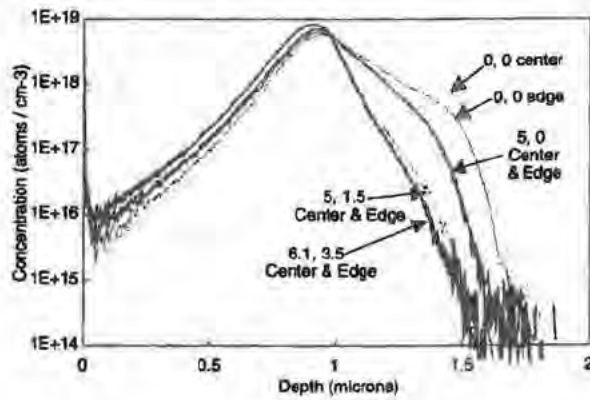


Figure 23 Variation of dopant depth distributions for different (α, β) wafer locations. 400 keV B^+ ions.

due to the very high heat conductivity of silicon. Should photoresist or other films with much lower heat conductivity be present on silicon, the temperature determined by the sticker can underestimate an actual wafer temperature.

E. Implant Angle Integrity

Control of the angle between the surface of implanted silicon wafer and direction of the ion beam is one of the key requirements for achieving a desired depth distribution of the implanted species that is uniform across the implanted wafer and repeatable from run to run. Variations of as-implanted depth distribution and uniformity deterioration occur whenever implanted ions channel along the rows and planes of crystalline silicon. It is not necessary for an ion beam to be perfectly aligned with the directions of major crystallographic axis or planes for ion channeling to occur. Forces of atomic interactions between implanted ions and atoms of the crystal lattice can steer ions into and guide within axial and planar channels in the crystal, even if initially ions were offset from the crystal by a small angle. This offset angle, when the probability of ion channeling starts to decrease rapidly, is referred to as the critical angle of channeling. This angle depends on the atomic numbers of the ion (Z_1) and atoms (Z_2) of the crystal, ion energy (E) and distance (d_{row}) between successive atoms along the channel wall [112]. For axial and planar channeling the critical angle is given by (14) and (15),

respectively.

$$\Theta_c = K \left[\frac{K_1 Z_2 e^2}{E d_{row}} \right]^{\frac{1}{2}} \quad (14)$$

$$\Theta_c = K \left[\frac{Z_1 Z_2 e^2 N d_p}{E} \right]^{\frac{1}{2}} \quad (15)$$

In (14) d_{row} is the distance between the adjacent atoms along the wall of the channel and in (15), N is the density of target atoms and d_p is distance between the atomic planes forming the channel walls. Expressions (14) and (15) do not take into account thermal vibrations of atoms in the lattice. Thus, experimentally found critical channeling angles can be smaller than predicted by (14) and (15).

The typical range of critical channeling angles for most implant recipes in CMOS technology is within 1° and 4° [113]. It became a common practice to tilt implanted wafers by 7° to produce ion distributions equivalent to implantation into non-crystalline material. In reality, optimum tilt and twist of implanted wafers varies, depending on the type of implanter scanning system, ion species and energy. Various considerations, dictated by process control and device architecture requirements, have to be taken into account to ensure desired process results. In general, implant conditions resulting in ion channeling are avoided. This is because ion channeling causes an increase, sometimes substantial, of the junction depth and modifies overall depth distribution of implanted specie. But, most importantly, channeling implants are very non-reproducible, since they depend on a combination of multiple factors other than ion dose and energy. Thickness of oxide film on the wafer surface, offset of wafer surface orientation with respect to major crystallographic axis, wafer temperature during implantation and, finally, non-reproducibility of beam direction in the beamline due to tuning variations impact ion channeling, strongly influencing the final characteristics of implanted layers. To achieve process reproducibility of channeled implants comparable to implants in a random direction, it is necessary to ensure the reproducibility of the angle between the beam and the wafer within one tenth of the critical channeling angle, e.g. 0.1 – 0.4° , depending on implant conditions. Despite the overall trend to avoid implantation under channeling conditions, some commercial processes utilizing channeling implants were developed. These processes rely on the ability of ion channeling to increase the range of dopant

penetration, and are used to form CMOS structures with relatively deep retrograde wells, using only a medium current implanter [114]. The availability of dedicated high energy implant tools in recent years eliminated channeling implants from virtually all new mainstream CMOS manufacturing processes.

For sub-10 keV boron recipes, which are typical for ultra-shallow junction formation in sub-0.25 μm nodes, channeling angle increases with reduction of ion energy and exceeds 10° for energies below 1 keV. Thus, for keV boron implants tilt angles in excess of 7° would have to be required to achieve even incomplete suppression of ion channeling. In reality, with few exceptions, large tilt angles are avoided because they cause mis-registration of dopant distribution in the areas close to mask edge features ("shadowing" effects). Asymmetry of two-dimensional lateral dopant profiles, and shadowing effects at the edges of illuminated and shadowed mask features become even more pronounced for high energy implants. This is due to the large thickness of photoresist masks necessary to block energetic ions. The extent of asymmetry is such that it was shown to degrade key device characteristics, such as intra-well isolation [115]. It is important to note that even relatively minor channeling for either frequently chained retrograde wells, or punchthrough stop implants, reduces near surface dopant concentration in the device channel region, and leads to a threshold voltage shift. Thus, many high energy implant processes require optimization of tilt and twist angles, in search for a compromise between preventing ion channeling, and minimizing asymmetry of lateral dopant distribution.

There are four major sources of angle variations that can occur in ion implantation. The first one is due to crystal cut errors during silicon wafer manufacturing. SEMI wafer spec dictates that the angle between the surface of silicon wafers and the direction of the Si major crystallographic axis must be no more than $\pm 1^\circ$. The second is due to tuning related differences of a beam trajectory in the implanter beamline. The third is due to beam direction change during electrostatic beam scanning, as deployed in old generation medium current tools; all of the latest tools have hardware for restoring beam direction after scanning. Finally, the configuration of batch endstations and the very beam scanning across the wafer in batch implanters causes variation of the tilt/twist angles across the wafer as it scans through the beam with rotation of the process disk (Fig. 23) [116–118].

Whenever non-uniformity on ThermoWave (TW) or four-point-probe wafer maps is observed, it is important to identify the correct cause of the problem, e.g. distinguish the impact of actual dose non-uniformity from effects related to differential channeling. If non-uniformity is caused by dosimetry errors, for example due to photoresist outgassing, then areas on a wafer map where a higher TW signal is observed should have reduced sheet resistance as well. In the case of non-uniformity caused by differential channeling, areas where channeling is more intensive will have a reduced TW signal, since formation of implantation defects decreases when ions travel along axial and planar channels. At the same time, the projected range of channeled ions increases, which leads to a reduction of peak dopant concentration in the implanted profile, increased carrier mobility after thermal anneal, and lower sheet resistance.

F. Wafer Contamination

Bombardment of solids with energetic ions causes surface sputtering, which is responsible for wafer elemental and particle contamination during ion implantation. Since a variety of materials used in implanters are exposed to ion beams, many different elemental contaminants can be introduced to implanted wafers in widely different quantities. These contaminants originate from sputtering implanter beamline components, areas of the process disk not covered with implanted wafers, materials on the surface of implanted wafers, and the surface of the Faraday. Most common, and usually found in greater quantities as compared to other elements are aluminium, carbon and species implanted on a tool prior to the investigated implant such as boron, phosphorus, and arsenic. Typical surface concentration of these contaminants in modern high current batch implanters ranges from less than a hundred to up to ten thousands of parts per million (ppm), which is equivalent to $\sim 10^{12}$ – 10^{14} cm^{-2} for a 10^{16} cm^{-2} implant dose. The lower range is typical for implanters with a silicon-coated process disk [120] and utilization of effective disk cleaning procedures to suppress cross-contamination. Transition metals comprise another group of contaminants. They are present as impurities in beam line materials and are found on the surface of implanted wafers in much lower quantities, typically $< 5 \text{ ppm}$. It is important to realize that the impact of various contaminants on device performance and process stability, strongly depends on the kind of con-

taminant and whether the contaminant is introduced at a wafer surface, or penetrates to the volume (in the case of energetic species) of the semiconductor [121]. Specifics of the process flow, intrinsic gettering structures, and type of device structures produced are other important parameters defining tolerable limits for each particular type of contamination.

Sputtered atoms have low energy and can typically be found on the surface of implanted wafers. Screen oxides grown on the wafer prior to ion implantation, and removed from the wafers prior to post implant anneal, allow the elimination of most contaminants from the wafer [122]. Energetic contamination usually occurs when the beam of the implanted dopant is contaminated with ions having magnetic rigidity close to that of the dopant ions. The most common manifestation of this effect is contamination of $^{49}\text{BF}_2^+$ beam with $^{98}\text{Mo}^{++}$ ions [123,124]. Arc chambers of implanter ion sources are commonly made of molybdenum. Thus, a certain amount of Mo^{++} ions (usually up to 10–20 ppm) is always present in the source plasma, due to sputtering of the arc chamber material and its subsequent ionization. To prevent contamination with Mo, more expensive tungsten arc chambers are used. Contamination of $^{31}\text{P}^+$ ion beam with $^{31}\text{BHF}^+$ ions is another example of possible energetic contamination [125]. Finally, energetic contamination with carbon oxygen, nitrogen and hydrogen can be observed during implantation into photoresist coated wafers in ion implanters with a post acceleration stage. This happens when gases released due to photoresist outgassing are not effectively pumped in the implanter beamline, and thus are allowed to expand into the post acceleration stage, become ionized there through interaction with the ion beam, and then accelerate up to a full post acceleration potential. The projected range of energetic contaminants is comparable to the projected range of dopant. Thus, screen oxides cannot effectively suppress energetic contaminants, and careful optimization of implant conditions, and subsequent process monitoring are required to minimize energetic contamination and keep it below the tolerable limit.

Contamination of P^+ ion beam with BHF^+ can be also considered as cross contamination, defined as the introduction to the wafer of dopant atoms other than the primary dopant. Still, the most significant contributor to cross-contamination is sputtering of the dopant atoms from the process disk, the surface of which is saturated with dopants other than the desired implant [126]. In most practical cases the effect of cross-contamination is limited to deviation of sheet

resistance in the implanted wafer from its target value. In situations when phosphorus is the cross-contaminant, in addition to the R_s shift, a significant increase of junction depths in silicon can occur [125]. This is due to higher phosphorus diffusivity, as compared to other common dopants.

Gold, iron, copper, nickel, chromium, and other transition metals are the least tolerable impurities in silicon processing technologies. All these elements introduce electron and hole traps located close to the middle of the silicon bandgap, thus acting as charge recombination centers. Several transition metals including gold, copper, and iron are highly diffusive in silicon. Thus, when introduced at a wafer surface but not removed with a screen oxide, they diffuse during subsequent thermal processing steps to a depth much greater than the dopant, and create charge traps (deep levels) in depletion regions of the p - n junctions. When present above critical concentration, deep traps significantly increase junction leakage currents. Tolerable levels of transition metal contamination depend on requirements associated with specific devices (CMOS logic, DRAM, BiCMOS, etc.), device generation, and manufacturing process flow [127]. Although under lab test conditions most devices do not demonstrate degradation of electrical characteristics if transition metals are in a 10^{11} – 10^{12} cm^{-2} range, 5 ppm is a currently accepted upper limit for these impurities in implanters. Upcoming device generations push this limit down even further, or will require more effective gettering methods.

G. Metrology

The large variety of parameters which characterize the implanted layers dictates a requirement for the utilization of multiple analytical techniques, to perform original setup and subsequent sustaining control of the implant process. Commonly used analytical techniques provide information on chemical, electrical and structural properties of the implanted layers. Some of these techniques, primarily ThermoWave (TW) and four-point probe (FPP) measurements, are fast and inexpensive to use, and have found wide use for routine monitoring of the implant process. In cases where deviations from the target values are observed, a comprehensive investigation of a particular implant is triggered. Depending on the nature of the problem, this investigation may involve more complex, time consuming, expensive and frequently destructive methods of chemical and structural analysis of the semiconductor.

TW [128,129] and FPP [130] are the most common techniques for implant monitoring. Both are fast, relatively inexpensive and enable wafer mapping. Thus, they are ideal tools for determining dose non-uniformity across the wafer. TW measures changes in light reflection from the wafer resulting from the implantation-induced crystal damage. TW is well suited for monitoring implants with doses starting from $\sim 10^{11} \text{ cm}^{-2}$ up to an amorphizing dose for any particular species. Since implant damage depends, in addition to the ion dose, on wafer temperature during implantation, ion beam current density and wafer orientation with respect to the beam (channeling effects), it is necessary to maintain run-to-run consistency of all implant parameters, in order to draw meaningful conclusions about the dose repeatability. FPP measurements require post-implant anneal in order to activate implanted dopant and to form a $p-n$ junction. Thus, overall error of FPP measurements comprise annealing variation (temperature, time, ambient, etc.).

Total X-Ray Fluorescence (TXRF) analysis [131] is a well established technique for measuring the composition and quantity of surface contaminants. In this technique, an x-ray beam impinges on a wafer surface at a grazing angle. Interference between the incident and reflected x-ray beams limits the excitation depth to several atomic layers. Thus, the high sensitivity of the TXRF technique is due to compression of the incoming x-ray beam within thin surface layer, and suppression of fluorescence from the background. TXRF technique is best suited for surface analysis of heavy contaminants. TXRF has a 10^{10} cm^{-2} or better detection limit for titanium and heavier elements. The detection limit for potassium and calcium is upward, to 10^{12} cm^{-2} and rapidly deteriorates further for lighter elements.

The Secondary Ion Mass Spectroscopy (SIMS) technique [132] is a destructive method of depth-dependent chemical analysis. It is time consuming, requires a skillful operator and is more expensive to use than TW and FPP techniques. On the other hand, the SIMS technique has low elemental detection limits (sub-ppm level or 10^{12} – 10^{16} cm^{-3}), a wide dynamic range of impurity concentration measurements (4–5 orders of magnitude), depth resolution as low as 2 nm and high lateral resolution (down to sub-1 micron). SIMS measurements allow the detection of virtually all elements of the periodic table. These advantages made the SIMS measurements an indispensable tool for initial setup of implant processes, and subsequent process troubleshooting when

deviations from target parameters are detected by TW, FPP or other monitoring techniques. The principle of SIMS operation is based on sputtering the solid surface with 1–20 keV primary beam (usually oxygen or cesium, sometimes argon, gallium). Sputtering results in ejection, from the sample surface, of neutral and ionized atoms which represent elements in the analyzed layer. Primary beam is scanned across a $0.5 \times 0.5 \text{ mm}^2$ area. Synchronously with this scan, ionized atoms from the target sputtered from the area close to the center of the sputter crater are mass-analyzed. Ion fluence for any particular mass plotted versus sputter time represents the depth distribution of the analyzed species in the sample. Several variations of the SIMS techniques have evolved to provide optimum performance for particular tasks. The majority of SIMS tools use either magnetic sector, quadrupole, or time-of-flight mass spectrometers. Tools with a magnetic sector have the highest mass resolution and provide excellent detection limits. Quadrupole mass spectrometers can rapidly switch from peak to peak, and therefore, are well suited for simultaneous acquisition of depth profiles of multiple elements. They also allow the achievement of improved depth resolution, when compared to SIMS tools with a magnetic sector. Requirements for accurate measurements of sub-50 nm depth profiles for ultra-shallow junctions, stimulated development of SIMS measurements performed with reduced energy of the primary beam, high incoming beam angle with respect to the surface, and stabilization of the sputtered surface with oxygen *in situ* leaked (O-leak) into the sputtered crater. O-leak [131] allows the reduction of the thickness of the sample depth mixed by the primary beam, stabilizes the sample surface during initial sputtering of the native oxide, and results in much improved accuracy and depth resolution of elemental SIMS analysis in the first tens of nanometers from the sample surface. O-leak SIMS measurements were demonstrated to provide superior performance for quantitative measurement of surface contamination introduced to the silicon during processing [133].

REFERENCES

1. J Gyulai, K Jones. Radiation Damage and Annealing in Silicon after Ion Implantation. In: JF Ziegler, ed. Ion Implantation Science and Technology. Yorktown, NY: Ion Implantation Technology Co., 1996, Chap. 4.
2. HA Bethe. Z Phys 76: 293, 1932.
3. F Bloch. Ann Phys 16: 287, 1933.

4. J Lindhard, A Winther, K Dan. *Vid Selks Nat, Fys Mat Fys Medd* 34(4) 1964.
5. PM Echenique, RM Nieminen, RH Ritchie, *Solid State Commun* 37: 779, 1981.
6. J Bausells. *J Appl Phys* 69: 155, 1991.
7. JF Ziegler, JP Biersack, U Littmark. The Stopping and Range of Ions in Solids. In: JF Ziegler, ed. *The Stopping and Ranges of Ions in Matter*. New York: Pergamon, 1985, Vol. 1.
8. PM Echenique, F Flores, RH Ritchie. *Solid State Phys* 43:229, 1998.
9. JF Ziegler. *Ion Implantation Physics*. In: JF Ziegler, ed. *Ion Implantation Science and Technology*. Yorktown, NY: Ion Implantation Technology Co., 1996, pp 175-238.
10. VE Golant, AP Zhilinsky, IE Sakharov. *Collisions in Plasmas*. In: *Fundamentals of Plasma Physics*. City: J. Wiley & Sons, 1980, Chap. 2, pp 16-76.
11. MT Robinson, IM Torrens. *Phys Review B* 9 5008, 1974.
12. KM Klein. In: *Monte Carlo Simulation of Boron Ion Implantation into Single Crystal Silicon*. PhD. Thesis, The University of Texas at Austin, Austin, TX, Dec, 1991.
13. J Linhard, M Scharff, H Schiott. *Range Concepts and Heavy Ion Ranges*. *Mat-Fys Med Dan Vid Selsk* 33(14): 1, 1963.
14. H Maes, W Vandervorst, R van Overstraten. *Impurity Profile of Implanted Ions in Silicon*. In: FY Wang, ed. *Impurity Doping Processes in Silicon*. Amsterdam: Ed North-Holland, 1981, Chap 1, pp 443-533.
15. C Park. *A Comprehensive and Computationally Efficient Modeling Approach for the Simulation of Ion Implantation for the ULSI Era*. Ph.D. Thesis, The University of Texas at Austin, Austin, TX, Dec 1991.
16. TRIM may be obtained from the IBM web site at <http://www.research.ibm.com/ionbeams/>
17. UT Marlowe may be obtained from Prof. AF Tasch, Department of Electrical and Computer Engineering, Microelectronics Research Center, University of Texas at Austin, Austin TX 78712.
18. S Tian. *Physical Basis of Monte Carlo Simulations of Ion Implantation Damage in Silicon*. Master's Thesis, The University of Texas at Austin, Austin, TX Nov 1994.
19. R Simonton, AF Tasch. *Channeling Effects in Ion Implantation into Silicon*. In: JF Ziegler, ed. *Ion Implantation Science and Technology*. Yorktown, NY: Ion Implantation Technology Co, 1996, pp 293-390.
20. NL Turner, et al. *Effects of Planar Channeling Using Modern Ion Implantation Equipment*, *Solid State Technol*, Feb 1985, pp 163.
21. JF Gibbons. *Ion Implantation in Semiconductors—Part II: Damage Production and Annealing*. *Proceedings of IEEE*, Sept 1972, pp 1062-1096.
22. FF Morehead, Jr BL Crowder. *A Model for the Formation of amorphous Si by Ion Bombardment*. *Proceedings of 1st International Conference On Ion Implantation*, L. Chadderton and F Eisen, Eds. New York: Gordon and Breach, 1971, pp 25-30.
23. PM Fahey, PB Griffin, JD Plummer. *Point Defects and Dopant Diffusion in Silicon*. *Rev Mod Phys* 61: 289-384, 1989.
24. JP Biersack. *From TRIM 97, PRAL determination of ranges and stopping powers*.
25. GH Kinchin, RS Pease. *The displacement of atoms in solids by radiation*. *Rep Prog Phys* 18: 2-50, 1955.
26. PA Stolk, HJ Gossman, DJ Eaglesham, DC Jacobson, CS Rafferty, GH Gilmer, M Jaraiz, JM Poate, HS Luftman, TE Haynes. *Physical Mechanisms of Transient Enhanced Diffusion in Ion Implanted Silicon*. *J Appl Phys* 81: 6031-6050, 1997.
27. S Wolf, RN Tauber. *Silicon Processing for the VLSI Era*. Vol 1, Sunset Beach, CA: Lattice Press, 1986, Chap 9.
28. S Wolf. *Silicon Processing for the VLSI Era*. Vol. 2. Sunset Beach, CA: Lattice Press, 1990, Chap 5.
29. T Hori, . *A New P-channel MOSFET with Large Angle Tilt Implanted Punchthrough Stopper (LATIPS)*. *IEEE Elec Dev Lett* 9: 641-643, 1988.
30. T Hori, . *A 0.1 μm CMOS Technology with Tilt Implanted Punchthrough Stopper (TIPS)*. 1994 IEDM Tech Digest pp 75-78.
31. A Hori, . *A 0.05 μm -CMOS with Ultra Shallow Source/Drain Junctions Fabricated by 5 keV Ion Implantation and Rapid Thermal Annealing*. 1994 IEDM Tech Digest, pp 485-488.
32. S Ogura, . *A Half-micron MOSFET using Double Implanted LDD*. 1982 Symp. VLSI Tech, Digest of Tech Papers, pp 42-43.
33. M Rodder, S Aur. IC Chen. *A Scaled 1.8 V, 0.18 μm Gate Length CMOS Technology: Device Design and Reliability Concerns*. 1995 IEDM Tech Digest, pp 415-418.
34. A Hori, A Hiroki, H Nakaoka, M Segawa, T Hori. *Quarter-Micrometer SPI (Self-aligned Pocket implantation) MOSFETs and Its Application for Low Supply Voltage Operation*. 1995 IEEE Trans Elec Dev, 42: 78-86.
35. PA Stolk, H-J Gossmann, DJ Eaglesham, DC Jacobson, CS Rafferty, GH Gilmer, M Jaraiz, JM Poate, HS Luftman, TE Haynes. *Physical mechanisms of transient enhanced diffusion in ion-implanted silicon*. *J Appl Phys* 81: 6031-6050, 1997.

36. A Agarwal, H-J Gossmann, DJ Eaglesham, L Pelaz, DC Jacobson, TE Haynes, Yu E Erokhin. Reduction of transient diffusion from 1–5 keV Si^+ ion implantation due to surface annihilation of interstitials. *Appl Phys Lett* 71: 3141–3143, 1997.
37. P Bouillon, F Benistant, T Skotnicki, G Guegan, D Roche, E Andre, D Mathiot, S Tedesco, F Martin, M Heitzmann, M Lerme, M Haond. Re-examination of Indium Implantation for a Low Power 0.1 μm Technology. 1995 IEDM Tech Digest, pp 897–900.
38. Y Taur, et al. High Performance 0.1 μm CMOS Devices with 1.5 V Power Supply IEDM Tech Digest, 1993, pp 127–130.
39. L Rubin, W Morris. High energy ion implanters and applications take off. *Semi International*, 20: 77–85, April 1997.
40. K Kanba, et al. A 7 Mask CMOS Technology Utilizing Liquid Phase Selective Oxide Deposition. IEDM Tech Digest, 1991, pp 637–640.
41. K Tsukamoto, et al. High Energy Ion Implantation for ULSI: Well Engineering and Gettering. *Solid State Tech* 35: 49, June 1992.
42. R Simonton, L Rubin, Yu Erokhin. Ion implantation applications in CMOS process technology. In: JF Ziegler, ed. *Ion Implantation Science and Technology*. Yorktown, NY: Ion Implantation Technology Co, 1996, Chap 1.
43. W-H Chang, et al. A High-Performance 0.25 μm CMOS Technology: I-Design and Characterization. *IEEE Trans Elec Dev* 39: 959–964, 1992.
44. A Stoltmeyer. A Twin-well CMOS Process Employing High Energy Ion Implantation. *IEEE Trans Elec Dev ED-33*: 450–455, 1986.
45. A Lewis, et al. Latch-up Performance of Retrograde and Conventional NWell CMOS Technologies. *IEEE Trans Elec Dev ED-34*: 2156–2162, 1987.
46. F Lai, et al. A Highly Latchup-immune/One Micron CMOS Technology Fabricated with 1 MeV Ion Implantation and Self-aligned TiSi_2 . *IEEE Trans Elec Dev ED-33*: 1308–1315, 1986.
47. Y Mochizuki. Special Report: High Energy Ion Implantation Technology. *Nikkei Microdevices*, Dec 1991, pp 92–96.
48. K Tsukamoto. Presented at the 10th International Conference on Ion Implantation Technology, Catania, Italy, June 13–17, 1994.
49. A Umezawa, et al. A 5-V-Only Operation 0.6 μm Flash EEPROM with Row Decoder Scheme in Triple-Well Structure. *IEEE J Sol State Circuits* 27:1540–1545, 1992.
50. T Yamashita, S Komori, K Horita, Y Kawasaki, Y Inoue, and T Nishimura. Highly reliable double well in thin- p^- on p^+ epitaxial wafer for logic embedded DRAM. IEDM Tech Digest, 1997, pp 673–676.
51. M Norishima, et al. High Performance 0.5 μm CMOS Technology for Logic LSIs with Embedded Large Capacity SRAMs. IEDM Tech Digest 1991, pp 489–492.
52. H Yoshimura, et al. New CMOS Shallow Junction Well FET Structure (CMOS-SJET) for Low Power Supply Voltage, IEDM Tech Digest, 1992, pp 909–912.
53. M Tamura, et al. MeV Energy B^+ , P^+ , and As^+ Ion Implantation into Si Nucl Instr Meth Phys Res B21: 438–441, 1987.
54. T Kuroi, et al. Self-Gettering and Proximity Gettering for Buried Layer Formation by MeV Ion Implantation. IEDM Tech Digest 1990, pp 261–264.
55. H Zappe, et al. Characteristics of CMOS Devices in High Energy Boron Implanted Substrates. *IEEE Trans Elec Dev* 35: 1029–1038, 1988.
56. Yu Erokhin, L Rubin, D Daniel, KH Lee, W Morris. Process trends for ultra-low energy and high energy ion implantation. *Future Fab International* 1:221–231, June/July 1997.
57. JY Cheng, DJ Eaglesham, DC Jacobson, PA Stolk, JL Benton, JM Poate. Formation of extended defects in silicon by high energy implantation of B and P. *J Appl Phys* 80: 2105–2112, 1996.
58. G Baccarani, et al. Generalized Scaling Theory and its Application to a 1/4 Micrometer MOSFET Design. *IEEE Trans Elec Dev* 31: 452–459, 1984.
59. C Osburn. Formation of Silicided, Ultra-Shallow Junctions Using Low Thermal Budget Processing. *J Elect Mat* 19: 67–76, 1990.
60. A Hamada, et al. N-Source/Drain Compensation Effects in Submicrometer LDD MOS Devices. *IEEE Elec Dev Lett EDL-8*: 398–400, 1987.
61. G Krieger, et al. Moderately Doped NMOS (M-LDD)—Hot Electron and Current Drive Optimization. *IEEE Trans Elec Dev* 38: 121–129, 1991.
62. A Yoshida, et al. Hot Carrier Induced Degradation Mode Depending on the LDD Structure in MOSFETs. IEDM Tech Digest, 1987, pp 42–45.
63. T Chan. Effects of the Gate-to-Drain/Source Overlap on MOSFET Characteristics, *IEEE Elec Dev Lett EDL-8*: 326–328, 1987.
64. P Capaletti, et al. Application of Advanced Ion Implantation Techniques to Flash Memories. *Nucl Instr Meth Phys Res B96*: 405–408, 1995.
65. J Pfister, et al. Improved CMOS Field Isolation using Germanium/Boron Implantation. *IEEE Elec Dev Lett* 9: 391–393, 1988.
66. M Ozturk, et al. Optimization of the Germanium Preamorphization Conditions for Shallow-junction Formation, *IEEE Trans Elec Dev* 35: 659–664, 1988.
67. YY Chen, IM Liu, M Gardner, J Fulford, DL Kwong. Performance and reliability assessment of dual-gate CMOS devices with gate oxide grown on nitrogen implanted Si substrates. IEDM Tech Digest, 1997, pp 639–642.

68. LK Han, S Crowder, M Hargrove, E Wu, SH Lo, F Gurain, E Crabbe, L Su. Electrical characteristics and reliability of sub-3 nm gate oxides grown on nitrogen implanted silicon substrates. IEDM Tech Digest 1997, pp 643-646.
69. S Shimizu, et al. Impact of Surface Proximity Gettering and Nitrided Oxide Side-Wall Spacer by Nitrogen Implantation on Sub-Quarter Micron CMOS LDD FETS. IEDM Tech Digest, 1995, pp 859-862.
70. K Lee, et al. Room Temperature 0.1 μm CMOS with 11.8 ps Gate Delay. IEDM Tech Digest, 1993, pp 131-134.
71. T Horiuchi, et al. A 7-Mask CMOS Process with Selective Oxide Deposition. IEEE Trans Elec Dev 40: 1455-1463, 1993.
72. T Aoyama, et al. Effect of Fluorine on Boron Diffusion in Thin Silicon Dioxides and Oxynitride. J Appl Phys 77: 417-424, 1995.
73. S Nakashima, et al. SIMOX Wafers with Low Dislocation Density Produced by a 100 mA High-current Oxygen Implanter. Nucl Instr Meth Phys Res B55: 847-850, 1991.
74. A Auberton-Herve, et al. SOI Materials for ULSI Applications. Semiconductor International, 18: 97-103, October 1995.
75. AJ Auberton-Herve. SOI: Materials to Systems. IEDM Tech Digest, 1996, pp 3-10.
76. Lienhard Wegmann. In: JF Ziegler, ed. Ion Implantation Science and Technology. Orlando, FL: Academic Press, 1984, pp 3.
77. ME Mack, GC Angel, ML Pascucci, D Prisby. In: Nucl Inst Meth B96:80, 1995.
78. K Stephens. Ion sources are reviewed by. In: JF Ziegler, ed. Ion Implantation Science and Technology. Yorktown, NY: Ion Implantation Technology Inc, 1996, pp 465.
79. A Renau, D Smatlak. In: E Ishida, S Banerjee, S Mehta, TC Smith, M Current, L Larson, A Tasch, eds. Ion Implantation Technology 96. Piscataway, NJ: IEEE, 1997, pp 279.
80. G Gammel, T Pennisi, D Smatlak, P Sullivan. In: E Ishida, S Banerjee, S Mehta, TC Smith, M Current, L Larson, A Tasch, eds. Ion Implantation Technology 96. Piscataway, NJ: IEEE, 1997, pp 404.
81. T Horsky, J Chen, H Rutishauser, F Sinclair, T McIntyre, W Reynolds, R Cloutier, F Tracira, W Loizides, W Bintz, J Neroda, J Grant, S Wilson. In: E Ishida, S Banerjee, S Mehta, TC Smith, M Current, L Larson, A Tasch, eds. Ion Implantation Technology 96. Piscataway, NJ: IEEE, 1997, pp 414.
82. ME Mack. In: JF Ziegler, ed. Handbook of Ion Implantation Technology. Amsterdam: North Holland 1992, pp 599.
83. MA Jones, F Sinclair. In: E Ishida, S Banerjee, S Mehta, TC Smith, M Current, L Larson, A Tasch, ed. Ion Implantation Technology 96. Piscataway, NJ: IEEE, 1997, pp 264.
84. DW Berrian, RE Kaim, JW Vanderpot, JFM Westendorp. Nucl Inst Meth B37: 500, 1989.
85. AM Ray, JP Dykstra, RB Simonton. In: DF Downey, M Farley, KS Jones, G Ryding, ed. Ion Implantation Technology-92 Amsterdam: Elsevier 1993, pp 401.
86. W Frutiger, R Eddy, DA Brown, ME Mack. In: E Ishida, S Banerjee, S Mehta, TC Smith, M Current, L Larson, A Tasch, ed. Ion Implantation Technology 96. Piscataway, NJ: IEEE, 1997, pp 346.
87. ME Mack, In: JF Ziegler, ed. Ion Implantation Science and Technology. NY: Academic Press, 1988, pp 313.
88. TC Smith. Particulate contamination is reviewed. In: JF Ziegler, ed. Handbook of Ion Implantation Technology. Amsterdam: North Holland, 1992, pp 555. More recent work can be found in ME Mack. In: E Ishida, S Banerjee, S Mehta, TC Smith, M Current, L Larson, A Tasch, ed. Ion Implantation Technology 96. Piscataway, NJ: IEEE, 1997, pp 166 and in Ref. [77] above.
89. ME Mack. Device charging is reviewed by. In: Ref [82] above. More recent work can be found in DL Smatlak, ME Mack, S Mehta. Nucl Inst Meth B96: 22, 1995.
90. H Ryssel, L. Frey. Metals contamination is reviewed. In: JF Ziegler, ed. Handbook of Ion Implantation Technology. Amsterdam: North Holland 1992, pp 675. More recent work can be found in DR Swenson, DF Downey, SR Walther, A Renau, G Gammel, ME Mack. In: E Ishida, S Banerjee, S Mehta, TC Smith, M Current, L Larson, A Tasch, ed. Ion Implantation Technology 96. Piscataway NJ: IEEE, 1997, pp 139, and in RD Rathmell, A Brune, DE Kamenitsa and D Seiler. Ion Implantation Technology-96, op cit, pp 143.
91. MI Current, L Larson, WA Keenan, CB Yarling. General process issues in ion implantation are discussed by. In: JF Ziegler, ed. Handbook of Ion Implantation Technology. Amsterdam: North Holland, 1992, pp 647.
92. N Bohr. Phys Rev 58: 654, 1940.
93. WE Lamb. Phys Rev 58: 696, 1940.
94. JF Ziegler, JP Biersack, U Littmark. The Stopping and Range of Ions in Solid, Vol. 1, JF Ziegler, ed., New York: Pergamon Press, 1985.
95. HG Chen, Y Erokhin, E McIntyre, F Sinclair, M Sugitani. Charge Exchange Effects in Production High Energy Ion Implanter Dosimetry Proc. of 11th International Conference on Ion Implantation Technology, 1996, p 104.
96. Wes Lukaszek, Understanding and Controlling Wafer Charging Damage, Solid State Technology, June 1998, p 101.

97. W Dixon, W Lukaszek, C Heden. Photoresist Enhanced Wafer Charging During High Current Ion Implantation, Proceedings of the 11th International Conference on Ion Implantation, E Ishida, ed. 1996, p 85.
98. ME Mack. Wafer Cooling and Wafer Charging in Ion Implantation, in Ion Implantation—Science and Technology, by JF Ziegler, ed. Ion Implantation Technology Co, 1996, p 538.
99. AFT Holmes. Phys Rev A19:389, 1979 and Radiat Eff 44: 47, 1979.
100. D Dumin, . High Field Related Thin Oxides Wearout and Breakdown, IEEE transactions on electron devices, 42, 1995, p 760.
101. M Current, W Lukaszek, M Vella, N Trispas. Surface Charge Control During High-Current Ion Implantation: Characterization with CHARM-2 sensors, Nucl Instr Meth Phys Res B96, 1995, pp 34–38.
102. YD Chan. Jpn J Appl Phys 33: 4458–4460, 1994.
103. H Groeseneken, N Maes, N Beltran, R De Keersmaecker. A reliable approach to charge-pumping measurements in MOS transistors, IEEE Trans Electron Dev ED-31 (1): 42–53, 1984.
104. P Heremans, J Witters, G Groeseneken, H Maes. Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation, IEEE Electron Dev 36(7): 1318–1335, 1989.
105. D Bauza, and Y Maneglia. In-depth exploration of Si-SiO₂ interface traps in MOS transistors using the charge pumping technique, IEEE Trans Electron Dev 44(12): 2262–2266, 1997.
106. FF Morehead, BL Crowder. A Model for the Formation of Amorphous Si by Ion Implantation, F Eisen and L Chadderton, eds. 1st International Conference on Ion Implantation, Thousand Oaks, New York: Gordon and Breach, 1971.
107. JC Tsai, JM Marabito, Surface Science, 44:247, 1974.
108. Romig, M Bishop, V Rio, Exploration and Prevention of Photoresist Burning in High Current Ion Implanters. Proceedings of the 11th International Conference on Ion Implantation Technology, Austin, Texas, 1996, p 190.
109. DA Flemming, M Desarno and R Mohondro, Manufacturing Improvements Realized through an Optimized pre-Implant UV/Bake Process, Future Fabs, 1(4), p 177.
110. M King, P Rose, Nucl Instr Meth 1989:169, 1981.
111. Benveniste, Ion Implantation Technology, MI Current, NW Chang, W Weisenberg, B Kerby, ed. Amsterdam: North Holland, 1992, p 336.
112. MW Thomson. In: DV Morgan, ed. Channeling, London: Wiley, 1973, p 1–33.
113. RB Simonton, AF Tasch, Channeling Effects in Ion Implantation into Silicon, Chapter 6. In: JF Ziegler, ed., Ion Implantation: Science and Technology, Ion Implantation Technology Co, 1996.
114. V Raineri, G Galvagno, E Rimini, A la Ferla, S Capizzi, A Carnelea, G Ferla. Nucl Instr Methods, B55:615, 1991.
115. R. C. Wijburg, et al. Strong Asymmetric Doping Profiles at Mask Edges in High Energy Implantation, IEEE Trans Elec Dev 37:79, 1990.
116. AM Ray, JP Dykstra, Beam Incidence Variations in Spinning Disk Ion Implanters, Nucl Instr Methods, B55:488, 1991.
117. M Jones and F Sinclair, Across-Wafer Channeling Variations in Batch Implanters: A Graphical Technique to Analyze Spinning Disk Systems, Proceedings of the 11th International Conference on Ion Implantation Technology, Austin, TX, p 264, 1996.
118. L Rubin, Differential Channeling Effects Arising from Wafer Angle Variations in Batch Ion Implanters, Technical note, Eaton Corporation, 1998.
119. JF Ziegler, RF Lever, Appl Phys Lett, 46:358, 1958.
120. Stone, R Becker, R Geraghty, D Stone, P Kopalidis and A Bratchun, Performance of New Silicon Coated Disk Material: Disk Manufacturing Control and Device 3 Production Experience, Proceedings of the 12th International Conference on Ion Implantation Technology, Kyoto, Japan, June 1998, in press.
121. K Graff, Metal Impurities in Silicon-Device Fabrication, In: H-J Queisser, ed., Springer Series in Materials Science, Vol. 24, Springer-Verlag (Berlin, New York, Heidelberg), 1995.
122. TC Smith, Photoresist and Particulate Problems, JF Ziegler, ed., Ion Implantation Technology Co, 1996, p 629.
123. MT Wauk, A Murrell, D Wagner, P Edwards, Mechanism of Elemental Contamination in Ion Implantation Equipment, Proceedings of the 11th International Conference on Ion Implantation Technology, Austin, TX, 1996, p 117.
124. MI Current, LA Larson, Ultra-Pure Processing: a Key Challenge for Ion Implantation Processing for Fabrication of ULSI Devices, Proceedings of the Spring MRS Meeting, San-Francisco, N Chang, A Marwick, J Roberto, eds., 14:365, April, 1989.
125. C Heden, K Ho, R Pong, W Weisenberger, ¹¹BFH Contamination of Phosphorus Ion Implants, J Electrochem Soc, 1995.
126. LA Larson, MI Current, C Heady, Enhanced Diffusion Effects and Dopant Cross-Contamination in Ion Implanted Surfaces, In: Semiconductor Silicon, Proceedings of Electrochemical Soc, 86-4, 1986, p 667.
127. N Natsuaki, T Kamata, K Kondo, Y Kureshi, ULSI-Process Demands of Contamination Control on Ion Implantation, Nucl Instr Meth, B96:62, 1995.
128. WL Smith, A Rosencwaig, DL Willenborg, Appl Phys Lett, 47:584, 1985.
129. R Martini, C Wichard, WL Smith, MW Taylor, Solid State Technology, May 1987.

130. WA Keenan, et al., Advances in Sheet Resistance Measurements for Ion Implant Monitoring, Solid State Technology, June 1985, p 155.
131. P Eichinger, Total Reflection X-Ray Fluorescence Analysis. In: CR Brundle, CA Evans, S Wilson, eds., Encyclopedia of Materials Characterization. Boston, London, Oxford, Singapore, Sydney, Toronto, Wellington: Butterworth-Heinemann, 1992, p 361.
132. S Smith, L Wang, J Ericson, V Chia, Materials Research Society Symposium Proc, Vol. 386, 1995.
133. S Biswas et al., Analytical Techniques for Measuring Contamination Introduced During Ion Implantation, Proceedings of the 11th International Conference on Ion Implantation Technology, Austin, TX, 1996, p 245.