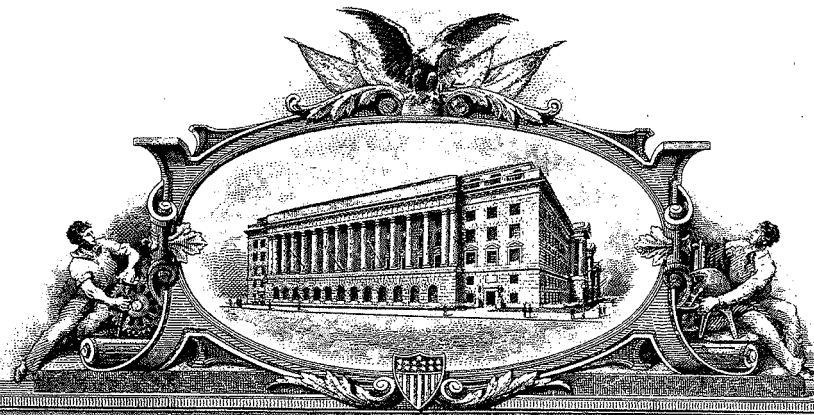


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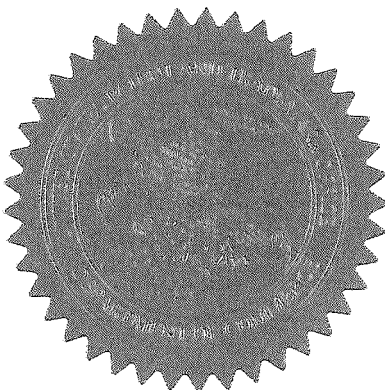
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Certifying Officer

Trudie Wallace
PART 2 OF 2 PARTS

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09/771391



Subclass	Class	ISSUE CLASSIFICATION

PATENT NUMBER

6701473



6701473

U.S. UTILITY Patent Application

<p>SCANNED <i>11/3</i> O.I.P.E. <i>A.A.</i></p>	<p>PATENT DATE MAR 02 2004</p>
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APPLICATION NO. 09/771391	CONT/PRIOR F	CLASS 324 <i>714</i>	SUBCLASS 724 <i>724</i>	ART UNIT 2858 <i>2133</i>	EXAMINER <i>DeLacy</i> <i>PAK Sline</i>
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APPLICANTS

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TITLE

Electrical circuit and method for testing a circuit component of the electrical circuit

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
<i>714</i>	<i>724</i>						
INTERNATIONAL CLASSIFICATION							
<i>G01R</i>	<i>31/3177</i>						
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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <i>2</i>	Figs. Drwg. <i>3</i>	Print Fig. <i>1</i>	Total Claims <i>38</i>	Print Claim for O.G. <i>1</i>
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
	<i>R. STEPHEN DILDINE</i> <i>PRIMARY EXAMINER</i> <i>A.U. 2133</i> <i>R. Stephen Dildine</i> <i>8/21/03</i> (Primary Examiner) (Date)			<i>1076103</i> ISSUE FEE <i>W</i> Amount Due <i>\$1330</i> Date Paid <i>1-9-04</i>	
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APPLICANTS Aaron Nygren, Munchen, GERMANY; Eckehard Plattner, Munchen, GERMANY; Andreas Tauber, Unterschleissheim, GERMANY;					
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Docket No.: GR 00 P 1142

Date: January 26, 2001

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : AARON NYGREN ET AL.

Title : ELECTRICAL CIRCUIT AND METHOD FOR TESTING A CIRCUIT
COMPONENT OF THE ELECTRICAL CIRCUIT

2 sheets of formal drawings in triplicate.
A check in the amount of \$ 1,034.00 covering the filing fee.

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(f). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

For Applicants

LAURENCE A. GREENBERG
REG. NO. 29,308

LAG:kc

ELECTRICAL CIRCUIT AND METHOD FOR TESTING A CIRCUIT COMPONENT
OF THE ELECTRICAL CIRCUIT

5

Background of the Invention:

Field of the Invention:

10 The present invention relates to an electrical circuit having
circuit components that are connected through a bus where at
least one of the circuit components can be tested
independently of the other circuit components. Additionally,
the present invention relates to a method for testing a
circuit component that is connected to other circuit
components through a bus, where the circuit component that is
15 to be tested, can be tested independently of the other circuit
components.

20 The circuit component that is to be tested is, by way of
example, a so-called macro of an integrated circuit. When
testing an integrated circuit, particular macros need or are
intended to be tested individually, i.e. independently of the
other circuit components of the integrated circuit.

25 Although only a relatively small part of the integrated
circuit is tested during such tests, such tests are frequently
relatively complex, particularly on account of the very high

currents that can flow through the integrated circuit during testing, and on account of the associated extreme evolution of heat. For the aforementioned reasons, unreliable test results are sometimes also obtained.

5

Summary of the Invention:

It is accordingly an object of the invention to provide an electrical circuit having circuit components that are connected through a bus and a method of testing at least one of the circuit components independently of the other circuit components which overcomes the above-mentioned disadvantageous of the prior art electrical circuits and methods of this general type, and in which the circuit components that are to be tested, can be reliably tested with a minimum amount of effort.

With the foregoing and other objects in view, there is provided, in accordance with the invention an electrical circuit that includes a bus; and a plurality of circuit components which are connected via the bus. At least one of the plurality of circuit components defines a circuit component to be tested and is configured to be tested independently from all others of the plurality of circuit components. The circuit component to be tested is configured to perform an operation, during the testing thereof, that is selected from the group consisting of outputting no data to

the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.

With the foregoing and other objects in view there is also
5 provided, in accordance with the invention, a method for testing a circuit component which is connected to other circuit components via a bus. The method includes a step of providing a plurality of circuit components that are connected to a bus. At least one of the plurality of circuit components
10 is configured such that it can be tested independently from all others of the plurality of circuit components, where the at least one of the plurality of circuit components defines a circuit component to be tested. While testing the circuit component to be tested, an operation is performed, with the
15 circuit component to be tested. The operation is selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.

20 Accordingly, the electrical circuit and the method are distinguished

- in that, during testing, the at least one circuit component which can be tested independently of the other circuit

25 components outputs no data to the bus and/or, instead of the data which would need to be output to the bus during normal

operation, outputs other data to the bus (characterizing part of patent claim 1), and

- in that steps are taken to ensure that, during testing, the circuit component which is to be tested outputs no data to the bus and/or, instead of the data which would need to be output to the bus during normal operation, outputs other data to the bus (characterizing part of patent claim 2).

By providing these features it is possible to ensure that the output drivers of the circuit component which is to be tested do not consume any power at all or only very little power. This is plausible for the case in which the circuit component which is to be tested outputs no data to the bus, but also applies to the case in which data are output to the bus. This is because the data which, if at all, are output to the bus by the circuit component which is tested, while it is being tested, are not the data which would be output to the bus by the tested circuit component during normal operation. The data can therefore be selected and output such that the power consumption of the output drivers is minimal.

The output drivers have a low power consumption when, amongst other things, the data which are to be output to the bus do not change or change only infrequently. The reason for this is that, in this case, the bus lines, which can have a

considerable capacity and which may require relatively high currents for reloading them, particularly at high clock frequencies, need not be reloaded or need be reloaded only infrequently. Reloading of the bus lines, which is necessary
5 infrequently or is not necessary at all, has the positive effect that the output drivers need never or need only infrequently deliver high currents. The effect achieved by this, in turn, is that, during testing, the relevant circuit component does not become nearly as hot as would be the case
10 without the inventive measures regarding the absence of output data or the limitation on the output data.

A low power consumption by the output drivers and the associated advantages can also be achieved by providing,
15 additionally or alternatively, for the data which need to be output to the bus to be able to be output so as to bypass the output drivers during testing. The output drivers can then be switched off or deactivated during testing.

20 The fact that, while it is being tested, the tested circuit component does not output data to the bus, and/or that it outputs data other than data which is output in the normal case, does not affect the test result. The circuit component which is to be tested is, of course, intended to be tested
25 independently of the other circuit components, which means that it is not necessary for data interchange between the

circuit components of the electrical circuit to take place via the bus.

The electrical circuit and the method therefore make it possible for circuit components, which are to be tested, to be reliably tested with a minimum amount of effort.

In accordance with an added feature of the invention, the circuit component to be tested includes output drivers for outputting data to the bus, the output drivers being deactivated during testing of the circuit component to be tested.

In accordance with an additional feature of the invention, the output drivers are deactivated by a test unit which is testing the circuit component to be tested.

In accordance with an another feature of the invention, a device is provided that is selected from the group consisting of a logic unit and a selection circuit. The device is for deactivating the output drivers. The device ensures: that during normal operation of the circuit component to be tested, the output drivers are controlled based upon an enable signal which is supplied to the circuit component to be tested by a bus control device which controls the bus, and that during testing of the circuit component to be tested, the output

XILINX EXHIBIT 1002

Page 11

drivers are controlled based upon a test control signal which the test unit supplies to the circuit component to be tested.

10 In accordance with a further feature of the invention, the
5 device is the logic unit, and the logic unit provides an
output signal resulting from a logical combination of the
enable signal and a test control signal.

10 In accordance with a further added feature of the invention,
the device is selected to be the selection circuit, the output
drivers include control connections, and the selection circuit
is formed by a multiplexer which selectively connects the
enable signal or the test control signal to the control
connections of the output driver.

15 In accordance with a further additional feature of the
invention, a bus control device is provided for controlling
the bus and for receiving a signal indicating testing of the
circuit component to be tested.

20

In accordance with yet an added feature of the invention,
during testing of the circuit component to be tested, the bus
control device ensures that the bus is terminated by a device
selected from the group consisting of the bus control device
25 and one of the others of the plurality of circuit components.

In accordance with yet an additional feature of the invention, the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during
5 normal operation, and the data outputted to the bus is data selected from the group consisting of infrequently changing data and non-changing data.

In accordance with yet another feature of the invention, a
10 device is provided that is selected from the group consisting of a logic unit and a selection circuit. The device ensures: that during normal operation of the circuit component to be tested, data that actually needs to be output to the bus are output to the bus, and that during testing of the circuit
15 component to be tested, the data outputted to the bus is from a test unit carrying out the testing of the circuit component to be tested.

In accordance with yet a further feature of the invention, the
20 device is selected to be the logic unit. The logic unit provides an output signal resulting from a logical combination of the data which would be output to the bus during normal operation and a test control signal. The test unit uses the test control signal to indicate that it is currently testing
25 the circuit component to be tested.

In accordance with yet a further added feature of the invention, the device is selected to be the selection circuit. The circuit component to be tested includes output drivers for outputting data to the bus, and the selection circuit is
5 formed by a multiplexer which selectively connects to the output drivers either the data which would be output to the bus during normal operation or the test control signal supplied by the test unit.

10 In accordance with yet a further additional feature of the invention, the circuit component to be tested includes output drivers for outputting data to the bus, and each one of the output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit.

15 In accordance with an added feature of the invention, each one of the output drivers receives an input signal that is an output signal of the respectively provided device.

20 In accordance with an additional feature of the invention, the circuit component to be tested includes output drivers with output connections; the operation performed by the circuit component to be tested, during testing thereof, is outputting data to the bus that is other than data which would be output
25 to the bus during normal operation; and the outputted data are

supplied to points situated between the output connections of the output drivers and the bus.

In accordance with another feature of the invention, a
5 switching device is provided for supplying the outputted data to the points situated between the output connections of the output drivers and the bus.

10 In accordance with a further feature of the invention, a logic unit is provided for controlling the switching device.

15 In accordance with yet a further feature of the invention, the logic unit provides an output signal resulting from a logical combination of an enable signal and a test control signal.

20 In accordance with a concomitant feature of the invention, the switching device, when turned on, connects the points situated between the output connections of the output drivers and the bus to at least one point which has a predetermined potential.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

25 Although the invention is illustrated and described herein as embodied in an electrical circuit and method for testing a circuit component of the electrical circuit, it is

nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

5

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 shows a first illustrative embodiment of the inventive electrical circuit;

Fig. 2 shows a second illustrative embodiment of the electrical circuit; and

Fig. 3 shows a third illustrative embodiment of the electrical circuit.

Description of the Preferred Embodiments:

The electrical circuit described below is an integrated circuit. However, before continuing, it should be pointed out that there is no restriction to this. The electrical circuit may also be any other electrical circuit.

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a first illustrative embodiment of an inventive electrical circuit.

5

The electrical circuit shown in figure 1 includes circuit components (macros) SK1, SK2, ... SKn, a bus "BUS" which connects the circuit components SK1, SK2, ... SKn, and a bus control device BUSCONTROL which handles the control (in particular the arbitration) of the bus "BUS".

The circuit components SK1, SK2, ... SKn include at least one circuit component which can be tested individually, i.e. independently of the other circuit components of the electrical circuit.

In the example under consideration, this circuit component is the circuit component denoted by the reference symbol SK1.

20 In the example under consideration, the circuit component SK1 is a memory module, more precisely a DRAM macro. However, before continuing, it should be pointed out that there is no restriction to this. The testable circuit component as described below may also be any other circuit component.

25

For testing the circuit component SK1, a test unit TE is provided. In the example under consideration, this test unit is a component part of the circuit component SK1 which is to be tested. However, there is no restriction to this either.

- 5 The test unit TE may also be provided outside the circuit component SK1 which is to be tested; in this context, it may be provided at random points within the electrical circuit, or else outside the electrical circuit.

10 The test unit TE

- inputs test data TESTIN into the circuit component SK1 which is to be tested,

15 - outputs test data TESTOUT from the circuit component SK1 which is to be tested,

- uses a test control signal TESTC to control the circuit component SK1 which is to be tested, and

20

- uses the test data TESTIN and TESTOUT to check whether the circuit component SK1 which is to be tested is operating correctly.

During normal operation of the circuit component SK1, that is to say when and so long as the circuit component SK1 is not being tested,

- 5 - data are supplied to the circuit component SK1 via the bus "BUS" and a data reception apparatus (not shown in figure 1), and

10 - the circuit component SK1 outputs data to the bus "BUS" via a multiplicity of output drivers, of which only a single output driver T is shown in figure 1.

15 In the example under consideration, the output drivers T are so-called tristate drivers and are activated and deactivated by the bus control device BUSCONTROL, more precisely by an enable signal EN output by the latter. When the output drivers T are activated, which may be the case when EN=1 in the example under consideration, they output the data supplied to them to the bus "BUS". When the output drivers T are

- 20 deactivated, which may be the case when EN=0 in the example under consideration, they cannot output any data to the bus "BUS"; they are then in a high-impedance state.

During testing of the circuit component SK1,

- the test data TESTIN from the test unit TE are used by the circuit component SK1 instead of the data supplied to it via the bus "BUS",

5 - the data normally output to the bus "BUS" are used as test data TESTOUT for the test unit TE, and

- instead of the data normally output to the bus "BUS", other data are output to the bus.

10 In the example under consideration, the data which are output to the bus "BUS" while the circuit component SK1 is being tested are generated independently of the data which actually need to be output to the bus; they have the special feature
15 that they do not change or change only very infrequently.

In the example under consideration, data which represent the level "0" are continuously output to the bus "BUS" while the circuit component SK1 is being tested.

20 In the example under consideration, when which data are output to the bus "BUS" is determined by a logic unit connected upstream of the output drivers T.

25 In the example under consideration, this logic unit includes an AND gate AND which receives as input signals the data DOUT

which need to be output to the bus "BUS" during normal operation of the circuit component SK1 and the test control signal TESTC, and whose output signal is supplied to the output driver T as input signal.

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During normal operation of the circuit component SK1, the test control signal TESTC has the value "1". The result of this is that the output signal from the AND gate is equivalent to the input signal DOUT of the AND gate. This means that, during normal operation of the circuit component SK1, the data DOUT which actually need to be output to the bus "BUS" are output to the bus.

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During testing of the circuit component SK1, the test control signal has the value "0". The result of this is that the output signal from the AND gate has the value "0", irrespective of the value of the other input signal of the AND gate. This means that the value "0" is continuously output to the bus while the circuit component SK1 is being tested.

20

The fact that, while it is being tested, the circuit component SK1 outputs data which never change or change only infrequently to the bus "BUS" has the positive effect that the bus lines need never be reloaded or need be reloaded only infrequently. This is advantageous because

25

- the output drivers T consequently consume only relatively little power, and

- the output drivers T and hence also the circuit component

5 SK1 do not heat up excessively.

The low power consumption of the electrical circuit during testing and the relatively low temperature of the electrical circuit during testing mean that the circuit component SK1
10 which is to be tested can be reliably tested with a minimum of effort. In particular, it means that

- the number and size of the elements (needles) used to supply the electrical circuit with power during testing can be kept
15 small, and

- it is a comparatively simple matter to carry out low-temperature tests.

20 The fact that the data DOUT which actually need to be output to the bus "BUS" are not output to the bus while the circuit component SK1 is being tested, but instead other data are output to the bus, has no negative effect on the test result. The circuit component SK1 which is to be tested is, of course,
25 intended to be tested independently of the other circuit components of the electrical circuit, so that it is

unimportant whether, and possibly which, data are output to the bus by the circuit component SK1.

5 The fact that the circuit component SK1 outputs data to the bus "BUS" is nevertheless found to be advantageous. If the circuit component SK1 were to automatically deactivate its output drivers (put them into the high-impedance state) during testing, this could lead to problems. In general, this is because the components connected to the bus "BUS" are not intended to (must not) ever, or possibly only to briefly, have all of the output drivers put into the high-impedance state at the same time. The bus "BUS" is intended to (must) be continually terminated by precisely one of the components which are connected to it.

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15 This problem does not arise in the present case, however. This means that the bus control device BUSCONTROL can continue to operate unchanged while the circuit component SK1 is being tested, and can retain exclusive control via the bus "BUS".

20 This in turn makes it possible for a plurality of circuit components of the electrical circuit to be tested at the same time.

25 It ought to be clear that it is not imperative for data continuously representing the level "0" to be output to the bus "BUS" while the circuit component SK1 is being tested.

5 Data continuously representing the level "1" can also be
output to the bus "BUS". Furthermore, provision may be made
for data which do not continuously have one predetermined
level, but instead change, to be output to the bus "BUS" while
the circuit component SK1 is being tested. In this case, the
important factor is that the data which are output to the bus
change only relatively infrequently, and thus it is
essentially possible to attain the same advantageous effects
as in the case when data which do not change are output to the
10 bus.

15 It should likewise be clear that the logic unit used to
generate the data which need to be output to the bus does not
necessarily have to be an AND gate AND of the design and
arrangement described. There are innumerable other options for
this: by way of example, a NAND gate may be used instead of
the AND gate AND. As another example, a multiplexer can be
used to selectively connect, to the output driver T, the data
DOUT which need to be output during normal operation or data
20 which need to be output during testing.

The electrical circuit can alternatively be designed such
that, while it is being tested, the circuit component which is
to be tested outputs no data to the bus.

An illustrative embodiment of such an electrical circuit is shown in figure 2 and is described below with reference thereto.

5 The electrical circuit shown in figure 2 is largely consistent with the electrical circuit shown in figure 1. Like the electrical circuit shown in figure 1, it (the electrical circuit shown in figure 2) includes circuit components (macros) SK1, SK2, ... SKn, a bus "BUS" which connects the circuit components SK1, SK2, ... SKn, and a bus control device
10 BUSCONTROL which handles the control (in particular the arbitration) of the bus "BUS". Of the circuit components present SK1, SK2, ... SKn, the intention is also again for the circuit component denoted by the reference symbol SK1 to be tested individually, i.e. independently of the other circuit
15 components of the electrical circuit. The circuit component which is to be tested is tested by a test unit TE which, like the test unit TE provided in the electrical circuit shown in figure 1, is contained in the circuit component which is to be tested, i.e. the circuit component SK1. To this extent, the
20 electrical circuit shown in figure 2 is equivalent to the electrical circuit shown in figure 1.

Unlike the circuit component SK1 shown in figure 1, however,
25 the circuit component SK2 shown in figure 2 outputs no data to the bus "BUS" while it is being tested.

In the example under consideration, this is achieved in that the (control) connections of the output drivers T (which are also present in the circuit component SK1 shown in figure 2), which connections can be used to activate and deactivate the output drivers, no longer have the enable signal EN which is output by the bus control device BUSCONTROL applied to them, but instead have the output signal from a logic unit connected upstream of the control connection applied to them.

In the example under consideration, this logic unit includes an AND gate AND which receives as input signals, the enable signal EN and the test control signal TESTC which is also provided in the electrical circuit shown in figure 2. The output signal of the AND gate AND is used to control the output drivers T.

During normal operation of the circuit component SK1, the test control signal TESTC has the value "1". The result of this is that, during normal operation of the circuit component SK1, the signal used to control the output drivers corresponds to the enable signal EN.

During testing of the circuit component SK1, the test control signal has the value "0". The result of this is that the signal used to control the output drivers T continuously has

the value "0" while the circuit component SK1 is being tested, as a result of which the output drivers T are deactivated and cannot output data to the bus "BUS".

- 5 Unlike in the electrical circuit shown in figure 1, in the electrical circuit shown in figure 2, the test control signal TESTC is not supplied only to the circuit component SK1 which is to be tested, but also to a bus termination logic unit BTL, which is a component part of the bus control device BUSCONTROL
- 10 in the example under consideration.

The bus termination logic unit BTL ensures that, during testing of the circuit component SK1 (when and so long as the test control signal TESTC is signaling that the circuit

15 component SK1 is currently being tested), the bus "BUS" is terminated by one of the other components connected to the bus "BUS". In the example under consideration, the bus termination logic unit BTL terminates the bus "BUS" itself if required.

- Alternatively, provision could be made for the bus termination
- 20 logic unit BTL to activate the output drivers of one of the other circuit components connected to the bus "BUS" while the circuit component SK1 is being tested, and for it then to have these circuit components terminate the bus.

- 25 It ought to be clear that the logic unit used to generate the control signal for controlling the output drivers T need not

necessarily be an AND gate AND of the design and arrangement described. There are innumerable other options for this: by way of example, a NAND gate may be used instead of the AND gate AND, or else a multiplexer which is used to selectively
5 connect the enable signal EN or the test control signal TESTC to the control connection of the output drivers T.

The fact that no data are output to the bus "BUS" while the circuit component SK1 is being tested has the positive effect
10 that the output drivers T have no or only a negligibly low power consumption and consequently do not heat up at all, or heat up only to a very small extent.

The low power consumption of the electrical circuit during
15 testing and the relatively low temperature of the electrical circuit during testing mean that the circuit component SK1 which is to be tested can be reliably tested with a minimum of effort. In particular, this means that

- 20 - the number and size of the elements (needles) used to supply the electrical circuit with power during testing can be kept small, and
- it is a comparatively simple matter to carry out low-
25 temperature tests.

These advantages are even more pronounced in the electrical circuit shown in figure 2 than is the case in the electrical circuit shown in figure 1.

5 The electrical circuit shown in figure 3 and described below with reference thereto permits the advantage of the electrical circuit shown in figure 1, namely that, during testing of the circuit component which is to be tested, the bus is terminated, as may be necessary, by the actual circuit component which is to be tested, to be combined with the advantage of the electrical circuit shown in figure 2, namely that the output drivers of the circuit component which is to be tested have no or only a negligibly low power consumption while the circuit component is being tested.

10 The electrical circuit shown in figure 3 is largely consistent with the electrical circuits shown in figures 1 and 2. Like the electrical circuits shown in figures 1 and 2, it (the electrical circuit shown in figure 3) includes circuit components (macros) SK1, SK2, ... SKn, a bus "BUS" which connects the circuit components SK1, SK2, ... SKn, and a bus control device BUSCONTROL which handles the control (in particular the arbitration) of the bus "BUS". Of the circuit components present SK1, SK2, ... SKn, the intention is also again for the circuit component denoted by the reference symbol SK1 to be tested individually, i.e. independently of

the other circuit components of the electrical circuit. The circuit component which is to be tested is tested by a test unit TE which, like the test unit TE provided in the electrical circuits shown in figures 1 and 2, is contained in the circuit component which is to be tested, i.e. the circuit component SK1. To this extent, the electrical circuit shown in figure 3 is equivalent to the electrical circuits shown in figures 1 and 2.

Like the circuit component SK1 shown in figure 1 and by contrast with the circuit component SK1 shown in figure 2, the circuit component SK1 shown in figure 3 outputs data to the bus "BUS" as required (particularly when the circuit component SK1 is determined by the bus control device BUSCONTROL as bus master) while the circuit component SK1 is being tested.

In the example under consideration, however, this is done not by means of the output drivers T, which are also present for the circuit component SK1 shown in figure 3, but rather by applying a predetermined potential or potential profile to points situated between the output connections of the output drivers T and the bus "BUS".

In the example under consideration, the predetermined potential is ground potential. It may also be any other

potential and also a potential which changes over time,
however.

In the example under consideration, a predetermined potential
5 or potential profile is applied to the points situated between
the output connections of the output drivers T and the bus
"BUS" by means of a switching device S, which in the present
case is formed by a transistor. In this context, it is
basically unimportant what type of transistor this is. Instead
10 of the transistor, any other switching device may also be
used, for example a so-called transmission gate.

The switching device S is controlled by a logic unit. In the
example under consideration, this logic unit includes a NOR
15 gate NOR and an inverter I, with the NOR gate NOR receiving a
test control signal TESTC and an enable signal EN inverted by
the inverter I as input signals, and the output signal from
the NOR gate NOR being used to control the switching device S.

20 The test control signal TESTC and the enable signal EN are
consistent with the signals of the same name in the electrical
circuits shown in figures 1 and 2.

The output drivers T of the circuit component SK1 which is to
25 be tested are deactivated while the circuit component is being
tested. In the example under consideration, this is achieved

in that the (control) connections of the output drivers T,
 which connections can be used to activate and deactivate the
 output drivers, have the output signal from a logic unit which
 is connected upstream of the control connection applied to
 5 them, as in the case of the electrical circuit shown in figure
 2.

10 In the example under consideration, as in the case of the
 electrical circuit shown in figure 2, this logic unit includes
 an AND gate AND which receives the test control signal TESTC
 and the enable signal EN as input signals, and whose output
 signal is used to control the output drivers T.

15 The switching device S, which controls the termination of the
 bus "BUS", and the output drivers T are controlled by the
 logic units AND and I/NOR such that the following conditions
 are established as a result:

TESTC	EN	Action
0	0	Test mode Output drivers deactivated Termination inactive
0	1	Test mode Output drivers deactivated Termination active

1	0	Normal operation Output drivers deactivated
1	1	Normal operation Output drivers activated

The electrical circuit shown in figure 3

- has the advantages, as compared with the electrical circuit
5 shown in figure 1,

- that the path via which the data DOUT are output during
normal operation contains no additional logic unit, which
means that data can be output more quickly, and

- that the output drivers are deactivated during testing of
the circuit component which is to be tested, which means that
they consume less power during testing and consequently also
heat up to a lesser extent, and

- has the advantage, as compared with the electrical circuit
shown in figure 2, that the circuit component which is to be
tested terminates the bus itself, which means that it is
possible to dispense with the bus termination logic unit BTL
20 or similar devices.

Furthermore, this is achieved without having to accept significant disadvantages as compared with the electrical circuits shown in figures 1 and 2.

5 It ought to be clear that the logic units used to generate the control signals for controlling the output drivers T and the switching device S need not necessarily be designed and arranged as described. There are innumerable other options for this.

10 The fact that the output drivers T are deactivated while the circuit component SK1 is being tested has the positive effect that they have no or only a negligibly low power consumption and consequently do not heat up at all or heat up only to a
15 very small extent.

20 The low power consumption of the electrical circuit during testing and the relatively low temperature of the electrical circuit during testing mean that the circuit component SK1 which is to be tested can be reliably tested with a minimum of effort. In particular, it means that

- the number and size of the elements (needles) used to supply the electrical circuit with power during testing can be kept
25 small, and

- it is a comparatively simple matter to carry out low-temperature tests.

The precautions taken for testing the circuit component which is to be tested do not in any way impair it during normal operation. In particular, there is no need for concern about any kind of effects on the operating speed and the other essential properties of the circuit component which is to be tested.

A common feature of the electrical circuits described, independently of the details of the practical implementation, is that they provide an amazingly simple way of reliably testing circuit components which are to be tested with a minimum of effort.

We claim:

1. An electrical circuit comprising:

a bus; and

a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components;

said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation.

2. The electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested.

3. The electrical circuit according to claim 2, wherein said output drivers are deactivated by a test unit which is testing said circuit component to be tested.

4. The electrical circuit according to claim 3, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring:

that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device which controls said bus, and

that during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested.

5. The electrical circuit according to claim 4, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the enable signal and a test control signal.

6. The electrical circuit according to claim 4, wherein said device is said selection circuit, said output drivers include control connections, and said selection circuit is formed by a multiplexer which selectively connects the enable signal or

the test control signal to said control connections of said output driver.

7. The electrical circuit according to claim 1, comprising a bus control device for controlling said bus and for receiving a signal indicating testing of said circuit component to be tested.

8. The electrical circuit according to claim 7, wherein, during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by a device selected from the group consisting of said bus control device and one of said others of said plurality of circuit components.

9. The electrical circuit according to claim 1, wherein the operation performed by said circuit component to be tested, during the testing thereof, is outputting data to said bus that is other than the data which would be output to said bus during normal operation, and the data outputted to said bus is data selected from the group consisting of infrequently changing data and non-changing data.

10. The electrical circuit according to claim 9, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device ensuring:

that during normal operation of said circuit component to be tested, data that actually needs to be output to said bus are output to said bus, and

that during testing of said circuit component to be tested, the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested.

11. The electrical circuit according to claim 10, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the data which would be output to said bus during normal operation and a test control signal, said test unit using said test control signal to indicate that it is currently testing said circuit component to be tested.

12. The electrical circuit according to claim 10, wherein said device is said selection circuit, said circuit component to be tested includes output drivers for outputting data to said bus, said selection circuit is formed by a multiplexer which selectively connects to said output drivers either the data which would be output to said bus during normal operation or said test control signal supplied by said test unit.

13. The electrical circuit according to claim 10, wherein said circuit component to be tested includes output drivers for outputting data to said bus, and each one of said output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit.

14. The electrical circuit according to claim 13, wherein each one of said output drivers receives an input signal that is an output signal of said respectively provided device.

15. The electrical circuit according to claim 1, wherein:

said circuit component to be tested includes output drivers with output connections;

the operation performed by said circuit component to be tested, during testing thereof, is outputting data to said bus that is other than data which would be output to said bus during normal operation; and

the outputted data are supplied to points situated between said output connections of said output drivers and said bus.

16. The electrical circuit according to claim 15, comprising a switching device for supplying the outputted data to said

points situated between said output connections of said output drivers and said bus.

17. The electrical circuit according to claim 16, comprising a logic unit for controlling said switching device.

18. The electrical circuit according to claim 17, wherein said logic unit provides an output signal resulting from a logical combination of an enable signal and a test control signal.

19. The electrical circuit according to claim 16, wherein said switching device, when turned on, connects said points situated between said output connections of said output drivers and said bus to at least one point which has a predetermined potential.

20. A method for testing a circuit component which is connected to other circuit components via a bus, the method which comprises:

providing a plurality of circuit components that are connected to a bus;

configuring at least one of the plurality of circuit components such that it can be tested independently from all others of said plurality of circuit components, the at least

one of the plurality of circuit components defining a circuit component to be tested; and

while testing the circuit component to be tested, performing an operation with the circuit component to be tested, the operation selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.

21. The method according to claim 20, which comprises:

providing the circuit component to be tested with output drivers for outputting data to the bus; and

deactivating the output drivers during testing of the circuit component to be tested.

22. The method according to claim 21, which comprises deactivating the output drivers by a test unit which is testing the circuit component to be tested.

23. The method according to claim 22, which comprises:

providing a device for deactivating the output drivers;

using the device to ensure:

that during normal operation of the circuit component to be tested, the output drivers are controlled based upon an enable signal which is supplied to the circuit component to be tested by a bus control device which controls the bus, and

that during testing of the circuit component to be tested, the output drivers are controlled based upon a test control signal which the test unit supplies to the circuit component to be tested.

24. The method according to claim 23, which comprises using the logic unit to provide an output signal resulting from a logical combination of the enable signal and a test control signal.

25. The method according to claim 23, which comprises providing the output drivers with control connections, and forming the selection circuit by a multiplexer which selectively connects the enable signal or the test control signal to the control connections of the output driver.

26. The method according to claim 20, which comprises signaling a bus control device which controls the bus that the circuit component to be tested is undergoing a test.

27. The method according to claim 26, which comprises using the bus control device to ensure that, during testing of the circuit component to be tested, the bus is terminated by a device selected from the group consisting of the bus control device and one of the others of the plurality of circuit components.

28. The method according to claim 20, wherein the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during normal operation, and selecting the data output to the bus from the group consisting of infrequently changing data and non-changing data.

29. The method according to claim 28, which comprises:

selecting a device from the group consisting of a logic unit and a selection circuit;

using the device to ensure:

that during normal operation of the circuit component to be tested, data that actually needs to be output to the bus are output to the bus, and

that during testing of the circuit component to be tested, the data outputted to the bus is from a test unit carrying out the testing of the circuit component to be tested.

30. The method according to claim 29, which comprises:

selecting the device to be the logic unit;

constructing the logic unit to provide an output signal resulting from a logical combination of the data which would be output to the bus during normal operation and a test control signal; and

using the test control signal, by the test unit, to indicate that the test unit is currently testing the circuit component to be tested.

31. The method according to claim 29, which comprises:

selecting the device to be the selection circuit;

providing the circuit component to be tested with output drivers for outputting data to the bus;

forming the selection circuit by a multiplexer which selectively connects to the output drivers either the data which would be output to the bus during normal operation or the test control signal supplied by the test unit.

32. The method according to claim 29, which comprises:

providing the circuit component to be tested with output drivers for outputting data to the bus; and

providing each one of the output drivers with a device that is selected from the group consisting of a logic unit and a selection circuit.

33. The method according to claim 32, wherein each one of the output drivers receives an input signal that is an output signal of the respectively provided device.

34. The method according to claim 20, wherein:

the circuit component to be tested is provided with output drivers having output connections;

the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during normal operation,; and

the outputted data are supplied to points situated between the output connections of the output drivers and the bus.

35. The method according to claim 34, which comprises providing a switching device for supplying the outputted data to the points situated between the output connections of the output drivers and the bus.

36. The method according to claim 35, which comprises controlling the switching device with a logic unit.

37. The method according to claim 36, wherein the logic unit provides an output signal resulting from a logical combination of an enable signal and a test control signal.

38. The method according to claim 36, wherein the switching device, when turned on, connects the points situated between the output connections of the output drivers and the bus to at least one point which has a predetermined potential.

Abstract of the Disclosure:

The electrical circuit includes a plurality of circuit components which are connected via a bus. At least one of the circuit components can be tested independently of the other circuit components. The circuit component which is to be tested and the method for testing the circuit component are distinguished in that steps are taken to ensure that, during testing, the circuit component which is tested, outputs no data to the bus, and/or instead of the data which would need to be output to the bus during normal operation, outputs other data to the bus.

MPW/kc

Docket No.: GR 00 P 1142

COMBINED DECLARATION AND POWER OF ATTORNEY
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ELECTRICAL CIRCUIT AND METHOD FOR TESTING A CIRCUIT COMPONENT
OF THE ELECTRICAL CIRCUIT

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 100 03 260.5 filed January 26, 2000 and German Application No. 100 16 127.8, filed March 31, 2000, the International Priority of which is claimed under 35 U.S.C. §119.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/771,391	01/26/2001	Aaron Nygren	GR 00 P 1142	6871

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EXAMINER

DILDINE JR, R STEPHEN

ART UNIT	PAPER NUMBER
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2133

6

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Notice of Allowability

Application No.

09/771,391

Examiner

R. Stephen Dildine

Applicant(s)

NYGREN ET AL

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

If claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

- ☐ This communication is responsive to ____.
- ☒ The allowed claim(s) is/are 1-38.
- ☒ The drawings filed on 26 February 2001 are accepted by the Examiner.
- ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: ____.
- ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- (a) ☐ The translation of the foreign language provisional application has been received.
- ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

- ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
- ☐ CORRECTED DRAWINGS must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No. ____.
- (b) ☐ including changes required by the proposed drawing correction filed ____, which has been approved by the Examiner.
- (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.

- ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statements (PTO-1449), Paper No. 5
- ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Interview Summary (PTO-413), Paper No. ____.
- ☐ Examiner's Amendment/Comment
- ☒ Examiner's Statement of Reasons for Allowance
- ☐ Other

R. Stephen Dildine
Primary Examiner
Art Unit: 2133

Allowable Subject Matter

Claims 1-38 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Portners et al. shows isolation of an analog circuit (macro) from a digital circuit in an IC being tested, but this reference doesn't show outputting either no data or data other than data which would be output to the bus during normal operation as claimed by applicant in claims 1 and 20. Jacobsen shows blocking test data from the output of a device under test, but this reference doesn't show outputting either no data or data other than data which would be output to the bus during normal operation as claimed by applicant in claims 1 and 20. Levy shows switchably coupling logic circuits to a bus during functionality testing of the logic circuits, but doesn't teach outputting either no data or data other than data which would be output to the bus during normal operation as claimed by applicant in claims 1 and 20. EPO patent application 0364925 shows forcing an input/output terminal to either 1 or 0 according to test mode signals, but this reference doesn't show plural circuits connected to a bus as claimed by applicant in claims 1 and 20, but instead is concerned with testing an isolated circuit 10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. Stephen Dildine whose telephone number is 703-305-5524. The examiner can normally be reached on M, Tu, Th, F 5:55 am to 4:25 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.


R. Stephen Dildine

R. Stephen Dildine
Primary Examiner
Art Unit 2133

Notice of References Cited

Application/Control No.

09/771,391

Applicant(s)/Patent Under
Reexamination
NYGREN ET AL.

Examiner

R. Stephen Dildine

Art Unit

2133

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2001/0049806	12-2001	PORTENERS et al.	714/724
	B	US-6,499,124	12-2002	Jacobson, Neil G.	714/727
	C	US-6,041,427	03-2000	Levy, Paul S.	714/724
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	EP 364925 A1	04-1990	European Patent	OHFUJI, KAZUYOSHI	G01R 31/318
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of Allowability	Application No.	Applicant(s)	
	09/771,391	NYGREN ET AL.	
	Examiner	Art Unit	
	R. Stephen Dildine	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
2. ☒ The allowed claim(s) is/are 1-38.
3. ☒ The drawings filed on 26 February 2001 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☐ CORRECTED DRAWINGS must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No. _____.
 - (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
 - (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1 <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 2 <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3 <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 4 <input type="checkbox"/> Interview Summary (PTO-413), Paper No. _____ |
| 5 <input checked="" type="checkbox"/> Information Disclosure Statements (PTO-1449), Paper No. <u>5</u> | 6 <input type="checkbox"/> Examiner's Amendment/Comment |
| 7 <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | 8 <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9 <input type="checkbox"/> Other |

R. Stephen Dildine
Primary Examiner
Art Unit: 2133

Allowable Subject Matter

Claims 1-38 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Portners et al. shows isolation of an analog circuit (macro) from a digital circuit in an IC being tested, but this reference doesn't show outputting either no data or data other than data which would be output to the bus during normal operation as claimed by applicant in claims 1 and 20. Jacobsen shows blocking test data from the output of a device under test, but this reference doesn't show outputting either no data or data other than data which would be output to the bus during normal operation as claimed by applicant in claims 1 and 20. Levy shows switchably coupling logic circuits to a bus during functionality testing of the logic circuits, but doesn't teach outputting either no data or data other than data which would be output to the bus during normal operation as claimed by applicant in claims 1 and 20. EPO patent application 0364925 shows forcing an input/output terminal to either 1 or 0 according to test mode signals, but this reference doesn't show plural circuits connected to a bus as claimed by applicant in claims 1 and 20, but instead is concerned with testing an isolated circuit 10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. Stephen Dildine whose telephone number is 703-305-5524. The examiner can normally be reached on M, Tu, Th, F 5:55 am to 4:25 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.


R. Stephen Dildine

R. Stephen Dildine
Primary Examiner
Art Unit 2133



UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 10/06/2003
LERNER AND GREENBERG, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER

DILDINE JR, R STEPHEN

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 10/06/2003

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/771,391	01/26/2001	Aaron Nygren	GR 00 P 1142	6871

TITLE OF INVENTION: ELECTRICAL CIRCUIT AND METHOD FOR TESTING A CIRCUIT COMPONENT OF THE ELECTRICAL CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	01/06/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.
- ☐ Applicant claims SMALL ENTITY status.
See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Page 1 of 4

PTOL-85 (Rev. 10/03) Approved for use through 04/30/2004.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail****Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

7590

10/06/2003

LERNER AND GREENBERG, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/771,391	01/26/2001	Aaron Nygren	GR 00 P 1142	6871

TITLE OF INVENTION: ELECTRICAL CIRCUIT AND METHOD FOR TESTING A CIRCUIT COMPONENT OF THE ELECTRICAL CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	01/06/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
DILDINE JR, R STEPHEN	2133	714-724000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1	_____
2	_____
3	_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☐ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
- ☐ Publication Fee
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

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This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

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TRANSMIT THIS FORM WITH FEE(S)

PTOL-85 (Rev. 10/03) Approved for use through 04/30/2004.

OMB 0651-0033

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