UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

DECLARATION OF STEPHEN W. MELVIN

Case No. IPR2023-00517

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

I. Introduction....1

II. Background and Qualifications....1

III. Documents and Materials Considered....3

IV. Relevant Legal Principles....4

V. Person of Ordinary Skill in the Art....11

VI. '473 Patent....12

VII. Technology Background....18

VIII. Claim Construction....24

IX. Summary of Opinions....24

X. Claims 1-5, 7, 9-10, 13-14, 20-24, 26, 28-29, 32-33 are Obvious over Slemmer....39

XI. Claims 1-5, 7-10, 13-14, 20-24, 26-29, 32-33 are Obvious over Slemmer and Gasbarro....114

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 6,701,473 (the "'473 Patent")
1002	Prosecution history of the '473 Patent
1004	Curriculum Vitae of Dr. Stephen Melvin
1005	U.S. Patent No. 5,072,138 to Slemmer ("Slemmer")
1006	U.S. Patent No. 6,308,232 to Gasbarro ("Gasbarro")
1007	Excerpts from the IEEE Standard Glossary of Computer Hardware Terminology, IEEE Standard 610.10-1994 (1995)
1008	Excerpts from National Semiconductor Scan Databook
1009	Excerpts from Bleeker et al., Boundary Scan Test: A Practical Approach
1010	Built-In Self-Test (BIST) Using Boundary Scan
1011	U.S. Patent No. 5,784,331 to Lysinger ("Lysinger")
1013	U.S. Patent No. 5,136,185 to Fleming ("Fleming")
1012	U.S. Patent No. 5,559,753 to Kocis ("Kocis")
1014	First Amended Complaint, Polaris Innovations Limited v. Xilinx, Inc., 1:22-cv-00174-RGA, Docket No. 14 (April 28, 2022)
1015	Excerpts from Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions v3.0, User Guide (UG586 Apr. 6, 2016)
1016	U.S. Patent No. 4,558,236 to Burrows ("Burrows")
1017	U.S. Patent No. 4,910,417 to Gamal ("Gamal")

I. Introduction

1. I have prepared this Declaration in connection with Xilinx, Inc.'s Petition for *Inter Partes* Review of U.S. Patent No. 6,701,473 (the "'473 Patent") (EX1001), which is to be filed concurrently with this Declaration.

2. In the course of preparing this Declaration, I reviewed the '473 Patent, its prosecution file history, as well as the other documents discussed in this Declaration.

3. I have been retained by Xilinx, Inc. ("Xilinx" or "Petitioner") as an expert in the fields of computer engineering, computer memory systems and related technologies. My employer is being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in Xilinx, the '4739 Patent or the owner of the '473 Patent.

II. Background and Qualifications

4. I received a Ph.D. in Computer Science from the University of California at Berkeley in 1991 and a B.S. in Electrical Engineering and Computer Science from the University of California at Berkeley in 1982. I have more than 40 years of experience in computer science and computer engineering. I am an inventor on over 45 patents, and I am a registered patent agent before the USPTO.

5. My Ph.D. research areas included high-performance computer architecture and microarchitecture and microcode-based system performance analysis tools. From September 2001 through April 2002, I was a Visiting Scholar at the University of Texas, Austin, where I directed graduate students in research in the area of high-performance computer architecture.

6. In May 2001, I co-founded and was the Chief Architect of Flowstorm, Inc., a start-up company based in Silicon Valley, where I defined and guided the overall chip architecture for a multithreaded packet processor. From March 2000 through May 2001, I worked as the Senior CPU Architect at Clearwater Networks, where I was involved in defining the architecture and microarchitecture of Clearwater's CNP810S multithreaded network processor. Both of those professional experiences required a deep understanding of memory devices and memory interfacing techniques, including DRAM devices conforming to JEDEC standards.

7. From 1983 to 2020, I was the President of Zytek Communications Corporation ("Zytek"). Zytek was an engineering, consulting, and small-scale manufacturing company that provided intellectual property consulting services as well as services related to the design, implementation, and testing of embedded systems. Zytek's general areas of activity included industrial control and measurement, Internet-related services, hard disk analysis and file recovery, and

computer engineering research services. Through my work at Zytek, I have designed numerous microprocessor-based embedded systems, including analog and digital circuit design, firmware development for embedded microcontrollers, and software development for host interfacing, product development, and debugging. My designs for embedded systems have all involved an understanding of memory devices and interfacing between microprocessors and memory devices.

8. I am currently employed as a Principal with Exponent, Inc., which is an international multidisciplinary engineering and scientific consulting firm.

9. I am a member of the Institute of Electrical and Electronics Engineers (IEEE) and the Association for Computing Machinery (ACM).

10. I served as General Chair of the 45th Annual International Symposium on Microarchitecture (Micro-45), held in Vancouver in December of 2012. I also served as co-chair of the 29th Annual International Symposium on Microarchitecture (Micro-29), held in Paris in December of 1996.

11. Additional details regarding my employment and academic history are included in my curriculum vitae (EX1004).

III. Documents and Materials Considered

12. In forming my opinions, in addition to my knowledge, education, training, and experience, I have considered the materials cited in this Declaration

and the documents and things that I have obtained, or that have been provided to me, as listed above in the Table of Exhibits.

13. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me. My consideration of materials in relation to this Declaration is ongoing and I will continue to review any new materials as it is provided. This Declaration represents only those opinions I have formed to date and I may supplement or amend this Declaration if additional facts or information that affects my opinions becomes available.

IV. Relevant Legal Principles

14. I am not an attorney. I offer no opinions on the law. But counsel has informed me of legal standards that apply to the issue of patent validity. I have applied these standards in arriving at my conclusions.

15. I understand that in an *inter partes* review the petitioner has the burden of proving a proposition of unpatentability by a preponderance of the evidence. I understand this standard is different from the standard that applies in a district court, where I understand a challenger bears the burden of proving invalidity by clear and convincing evidence.

16. I understand that a patent claim is invalid based on anticipation if a single prior art reference discloses all of the features of that claim, and does so in a way that enables one of ordinary skill in the art to make and use the invention. Each of the claim features may be expressly or inherently present in the prior art reference. I understand that if the prior art necessarily functions in accordance with, or includes a claim's feature, then that prior art inherently discloses that feature. I have relied on this understanding in expressing the opinions set forth below.

17. I understand that a prior art reference describes the claimed invention if it either expressly or inherently describes each and every feature set forth in the claim; *i.e.*, in determining whether a single item of prior art anticipates a patent claim, one should take into consideration not only what is expressly disclosed in that item, but also what is inherently present as a natural result of the practice of the system or method disclosed in that item.

18. I understand that to establish inherency, the evidence must make clear that the missing descriptive matter is necessarily present in the item of prior art and that it would be so recognized by persons of ordinary skill in the art. I also understand that prior art use of the claimed patented invention that was accidental, unrecognized, or unappreciated at the time of filing can still be an invalidating anticipation.

19. I understand that although multiple prior art references may not be combined to show anticipation, additional references may be used to interpret the allegedly anticipating reference and shed light on what it would have meant to those skilled in the art at the time of the invention. These additional references must make it clear that the missing descriptive matter in the patent claim is necessarily present in the allegedly anticipating reference, and that it would be so recognized by persons of ordinary skill in the art.

20. I understand that a patent may not be valid even though the invention is not identically disclosed or described in the prior art if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art in the relevant subject matter at the time the invention was made.

21. To determine if a claim is obvious, the following factors should be considered: (1) the level of ordinary skill in the art at the time the invention was made; (2) the scope and content of the prior art; (3) the differences between the claimed invention and the prior art; and (4) secondary considerations, including evidence of commercial success, long-felt but unsolved need, unsuccessful attempts by others, copying of the claimed invention, unexpected and superior results, acceptance and praise by others, independent invention by others, and the like.

22. For example, I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim because a court can take account of the inferences and/or creative steps that a person of ordinary skill in the art would employ.

23. I understand that the following rationales may be used to determine whether a piece of prior art can be combined with other prior art or with other information within the knowledge of one of ordinary skill in the art:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known techniques to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- "Obvious to try" - choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; or

- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

24. I understand that when a work is available in one field of endeavor, design incentives and/or other market forces, for example, can prompt variations of it, either in the same field or a different one. Moreover, if a person of ordinary skill can implement a predictable variation, I understand that that likely bars its patentability.

25. I understand that obviousness must be tested as of the time the invention was made. I understand that the test for obviousness is what the combined teachings of the prior art references would have suggested, disclosed, or taught to one of ordinary skill in the art. In particular, it is my understanding that a patent claim is invalid based upon obviousness if it does nothing more than combine familiar elements from one or more prior art references or products according to known methods to yield predictable results. For example, I understand that where a technique has been used to improve one device, and a person of ordinary skill in the art would have recognized that it would improve similar devices in the same way, using that technique is obvious. I understand that obviousness can be proved by showing that a combination of elements was obvious to try, *i.e.*: that it does no more than yield predictable results; implements a predictable variation; is no more than the predictable use of prior art elements

according to their established functions; or when there is design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions. I have been further informed that when a patent claim simply arranges old elements with each element performing the same function it had been known to perform and yields results no more than one would expect from such an arrangement, the combination is obvious.

26. I understand that another factor to be considered is common sense. For example, I understand that common sense teaches that familiar items may have obvious uses beyond their primary purposes, and, in many cases, a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.

27. I understand that the Supreme Court articulated additional guidance for obviousness in its *KSR* decision. My understanding is that the Supreme Court said that technical people of ordinary skill look for guidance in other solutions to problems of a similar nature, and that the obviousness inquiry must track reality, and not legal fictions. I have relied on these understandings in expressing the opinions set forth below.

28. I understand that a new use of an old product or material cannot be claimed as a new product; the apparatus or system itself is old and cannot be

patented. I further understand that, in general, merely discovering and claiming a new benefit to an old process cannot render the process newly patentable.

29. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their "ordinary and customary meaning." In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a person of ordinary skill in the art ("POSITA"). I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

30. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). I have been asked to use the priority date of January 26, 2000. However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere in the 1990s.

V. Person of Ordinary Skill in the Art

31. In order to determine the characteristics of a POSITA of the ’473 Patent, I have used January 26, 2000 as the relevant time frame. My understanding is that this is the priority date of the application that resulted in the ’473 Patent. For purposes of this Declaration, any reference to the priority date of the ’473 Patent is intended to refer to this January 26, 2000 date.

32. In determining the characteristics of a person of ordinary skill for the ’473 Patent, I have considered the state of the art of semiconductor memory devices at that time, the types of problems encountered with power-on and initialization of such devices, and the solutions that then existed. I have also considered the then-existing technology for semiconductor memory devices and computer memory systems, including the sophistication of the technology involved. I have also considered the education and experience of those working in the field at that time. I have also considered my personal knowledge and experience in the field at that time, including those I worked and interacted with regarding semiconductor memory devices and computer memory systems. I have also considered the knowledge, education, and experience of those in academia and industry at that time that were working, innovating, or performing research in the field of semiconductor memory devices and computer memory systems.

33. It is my opinion that a POSITA for the ’473 Patent at the time of this filing date would have had a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and two or three years of academic or industry experience in the use and testing of integrated circuits, or comparable experience. Additional work experience can substitute for educational or research experience, and vice versa.

34. Given this background, a POSITA would have been familiar with integrated circuit inputs/outputs (I/Os), including I/Os for memory devices and memory buses. In addition, a POSITA would have been familiar with common test principles and configuring driver outputs during testing and normal operation.

35. Based on my background and qualifications, I am currently and was as of the priority date of the ’473 Patent someone who had more than the level of experience of a POSITA in the subject matter of the ’473 Patent. When developing the opinions set forth in this declaration, I assumed the perspective of a POSITA.

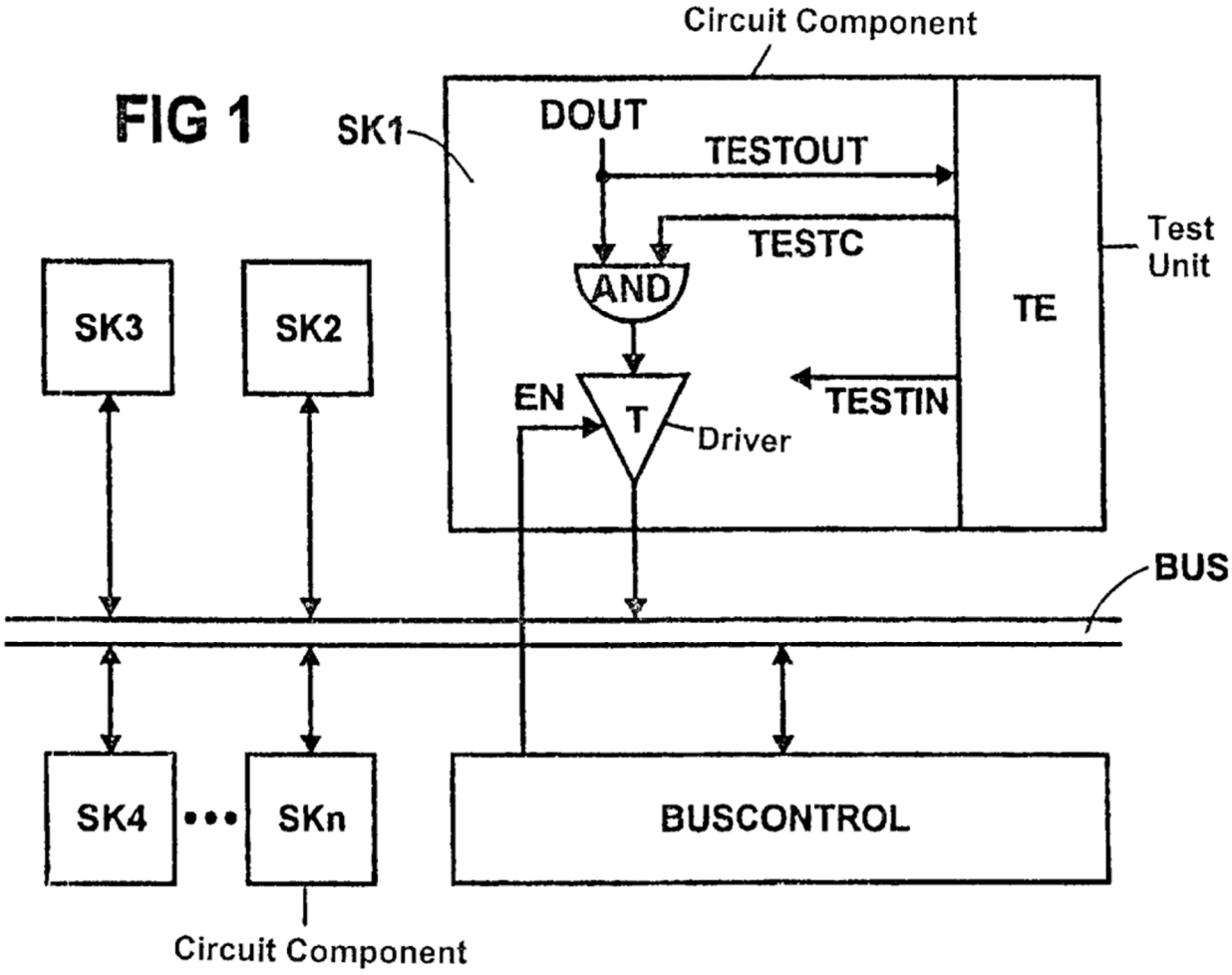
VI. ’473 Patent

A. Overview

36. The ’473 Patent is entitled “Electrical Circuit and Method for Testing a Circuit Component of the Electrical Circuit.” ’473 Patent (EX1001), at 1. The’473 Patent relates to testing a circuit component of an electrical circuit

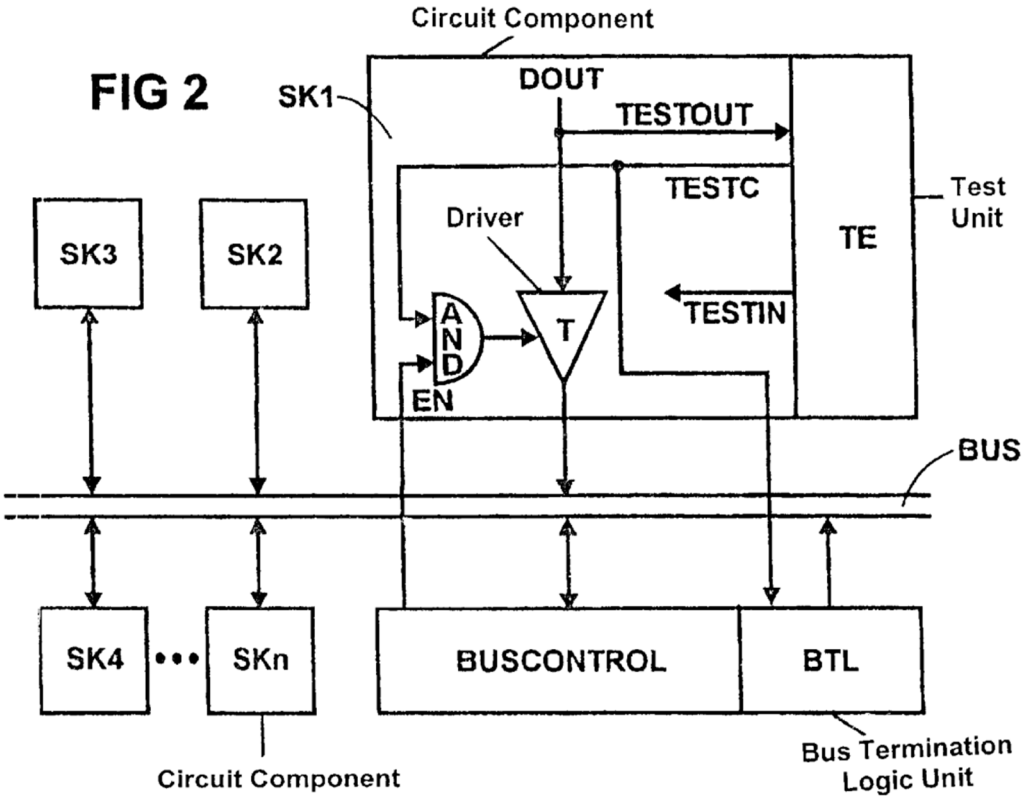
independently of other circuit components connected via a bus. *Id.* at Abstract, 1:8-16, 1:40-51. During testing, the circuit component outputs to the bus either no data or data other than that which would be output in normal operation. *Id.* The '473 Patent purports that this professed advancement ensures that the output drivers of the circuit component to be tested consume little power. *Id.*, 2:16-27.

37. As shown in Figure 1 of the '473 Patent below, circuit components (SK1 to SKn) are connected to a bus, as is a bus control device (BUSCONTROL).



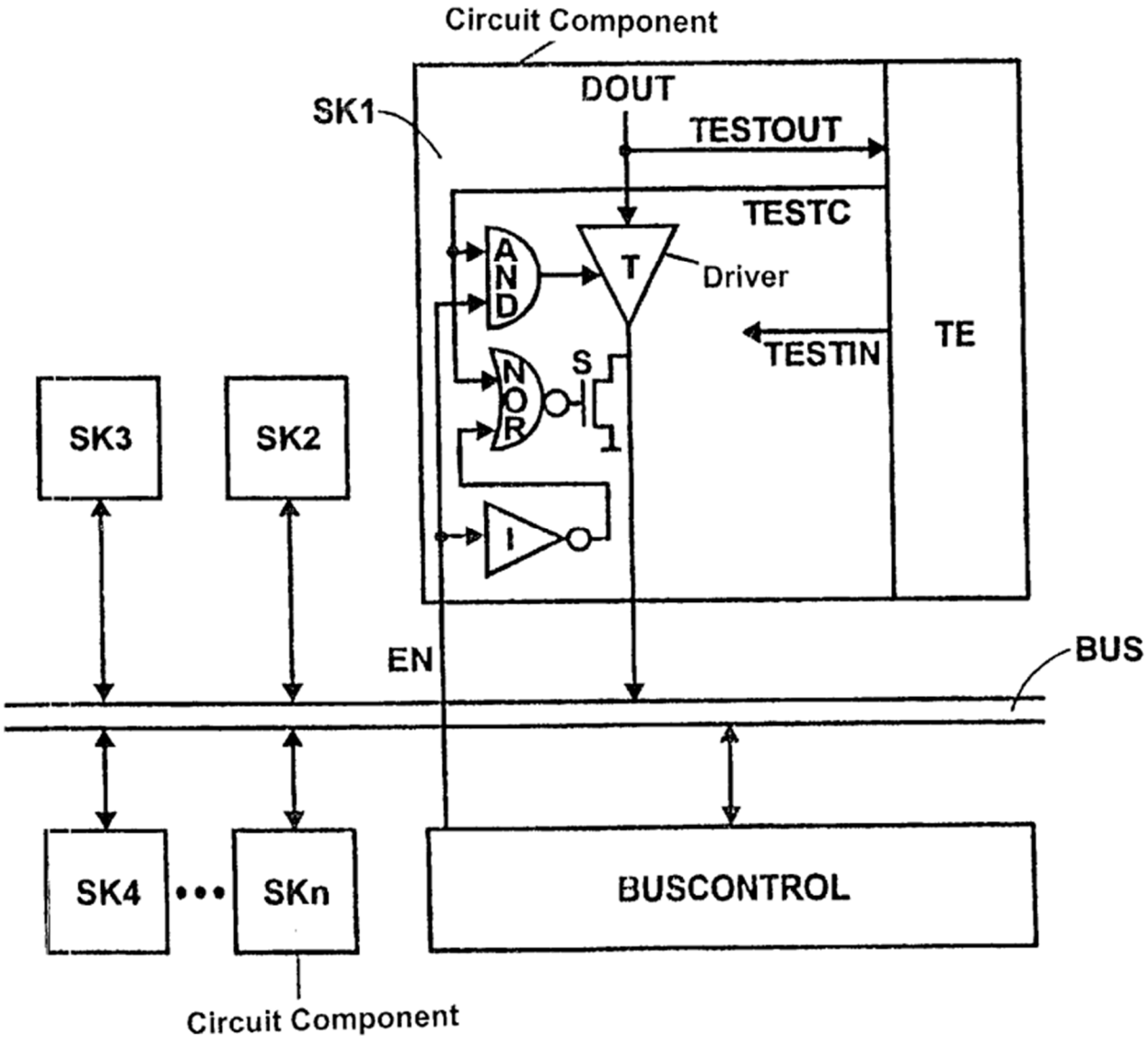
473 Patent (EX1001), FIG. 1, 4:61-5:2. As shown in the figure above, the circuit component SK1 includes a test unit (TE) to provide a test control signal (TESTC) and input test data (TESTIN) and to receive output test data (TESTOUT). *Id.* at 5:11-29. The circuit component SK1 also includes an AND-gate that receives the data to be output to the bus (DOUT) and the test control (TESTC) signal. *Id.*, 6:4-9. During normal operation of the circuit component SK1, test control signal (TESTC) has a value of "1," which causes a combined signal to be output from the AND gate that is equivalent to DOUT. *Id.*, 6:9-12. During testing of the circuit component, the test control signal (TESTC) has the value "0," which causes the combined signal output from the AND gate to be "0", irrespective of the value of DOUT. *Id.*, 6:16-20. Finally, the circuit component SK1 includes a tristate driver (T) to output the combined signal based on whether the driver is enabled via the EN signal. *Id.*, 5:39-49.

38. As shown below in Figure 2 of the '473 Patent, another embodiment of the '473 Patent adds a bus termination logic unit (BTL) to the bus control device (BUSCONTROL), as shown below.



Id. at FIG. 2, 8:10-28. The BTL receives a test control signal (TESTC) and ensures that, during testing of the circuit component, the bus is terminated by one of the other components connected to the bus. *Id.*, 8:16-21. Furthermore, the driver is enabled (or not) to send the value of DOUT on the bus based on the output of the AND-gate that combines the TESTC and EN signals. *Id.*, 7:60-65.

39. As shown below in Figure 3 of the ’473 Patent, yet another embodiment of the ’473 Patent modifies the circuit component relative to Figures 1 and 2 to implement additional circuitry to terminate the bus.



Id. at FIG. 3, 8:56-65, 9:24-47. As shown in Figure 3, the output of the driver is connected to a switch (S), which is connected by the TESTC and inverted EN signals. The switch, which controls the termination of the bus, and the output driver are controlled by the logic units AND, I (inverter), and NOR such that the following conditions are established as a result

TESTC	EN	Action
0	0	Test mode Output drivers deactivated Termination inactive
0	1	Test mode Output drivers deactivated Termination active
1	0	Normal operation Output drivers deactivated
1	1	Normal operation Output drivers activated

Id. at 9:66-10:15.

B. Prosecution History

40. On January 26, 2001, the ’473 Patent was filed as Application No. 09/771,391 (the “’391 Application”) entitled “Electrical Circuit and Method for Testing a Circuit Component of the Electrical Circuit.” I understand that the ’391 Application claims priority to two German patent applications and listed 38 claims. *See* File History of ’473 Patent (EX1002), at 3, 6, 36-47, 49. The first German patent application is German Patent Application 100 03 260, which was filed January 26, 2000, and the second German patent application is German Patent Application 100 16 127, which was filed March 31, 2000. *See id.* at 49.

41. Around October 6, 2003, a notice of allowance was issued and mailed in the ’391 Application without any rejections of the pending claims. *See id.* at 228-30, 290-92.

C. Priority Date

42. As discussed above, the ’391 Application claims priority to two German applications filed on January 26, 2000 and on March 31, 2000. ’473 Patent (EX1001) at 1. For the purposes of this Declaration, I have been asked to assume that the earliest priority date of the ’473 Patent is January 26, 2000.

D. Related Proceedings

43. I understand that Patent Owner, Polaris Innovations, Ltd. (“Patent Owner” or “Polaris”), filed a complaint on February 8, 2022 in the United States District Court for the District of Delaware (CA 1:22-CV-00174-RGA) against Petitioner, asserting four patents, including the ’473 Patent.

VII. Technology Background

44. The technology of the ’473 Patent generally relates to testing of circuit components, such as memory modules, including dynamic random access memory (“DRAM”) modules. As of the filing date of the ’473 Patent, there were multiple types of memory available. Such variants include Static RAM (“SRAM”), Synchronous Dynamic RAM (“SDRAM”), Erasable Programmable Read-Only Memory (“EPROM”), and embedded memories.

45. Memory chips or modules typically contain one or more memory arrays, which are rectangular grids of storage cells where each cell holds one bit of data.

46. SRAM is characterized as "static" because the values held in the memory array's storage cells are maintained as long as power is applied. The storage cells in a SRAM are implemented using storage elements such as flip-flops or registers.

47. DRAM is characterized as "dynamic" because the values held in the memory array's storage cells are represented by electric charges that slowly leak out of the circuit over time. In this sense, DRAM memory cells are similar to capacitors, in contrast to static memory cells, where the electric charge in a memory cell will be maintained indefinitely as long as power is applied. In order to maintain the data stored in dynamic memory cells, they must be periodically "refreshed" by reading the current value of a memory cell and restoring its charge.

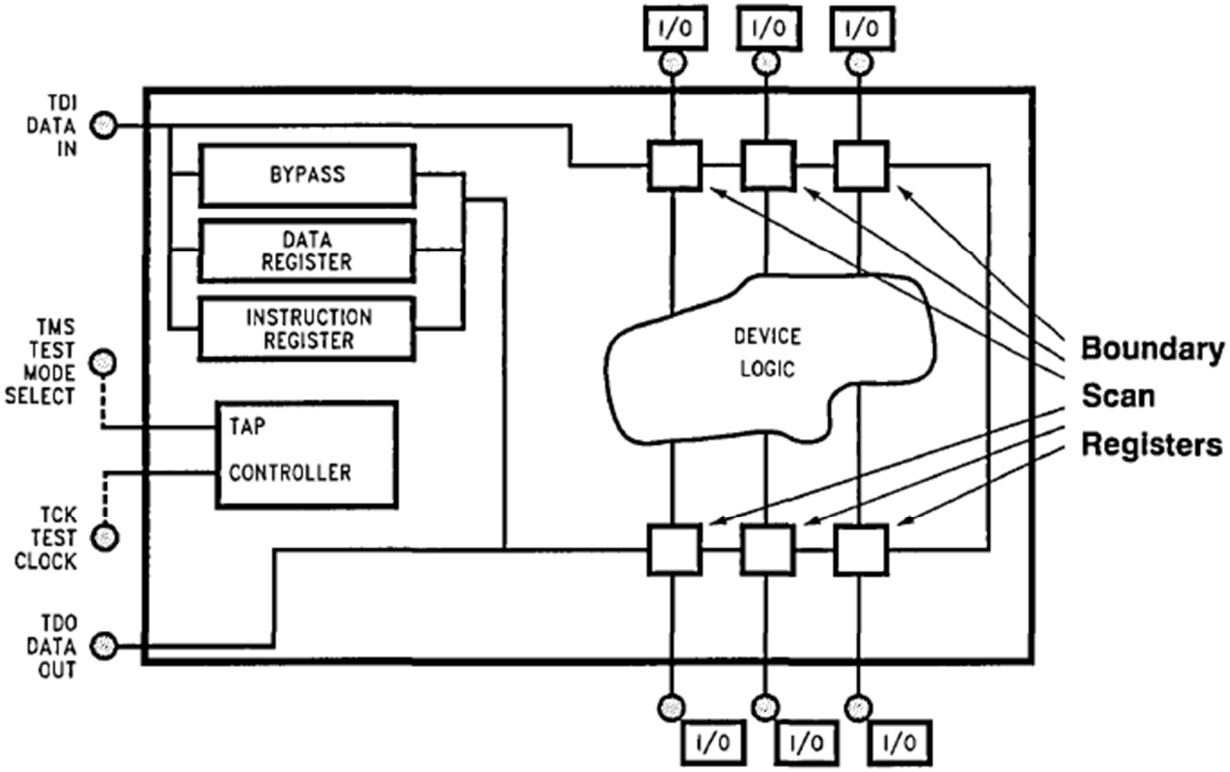
48. EPROM is characterized as "erasable programmable" because the values held in the memory array's storage cells are retained when the power supply to the EPROM is turned off. In this sense, EPROM memory cells are non-volatile because they retain data without a power supply.

49. Memory devices are typically equipped with address and data pins which connect the memory to address and data buses. A bus is typically a group of one or more wires that carry electrical signals between components. *See* EX1007, at 9 (defining "bus" as "[o]ne or more conductors that are used for the transmission of signals, data, or power."). Addresses buses convey address information to the

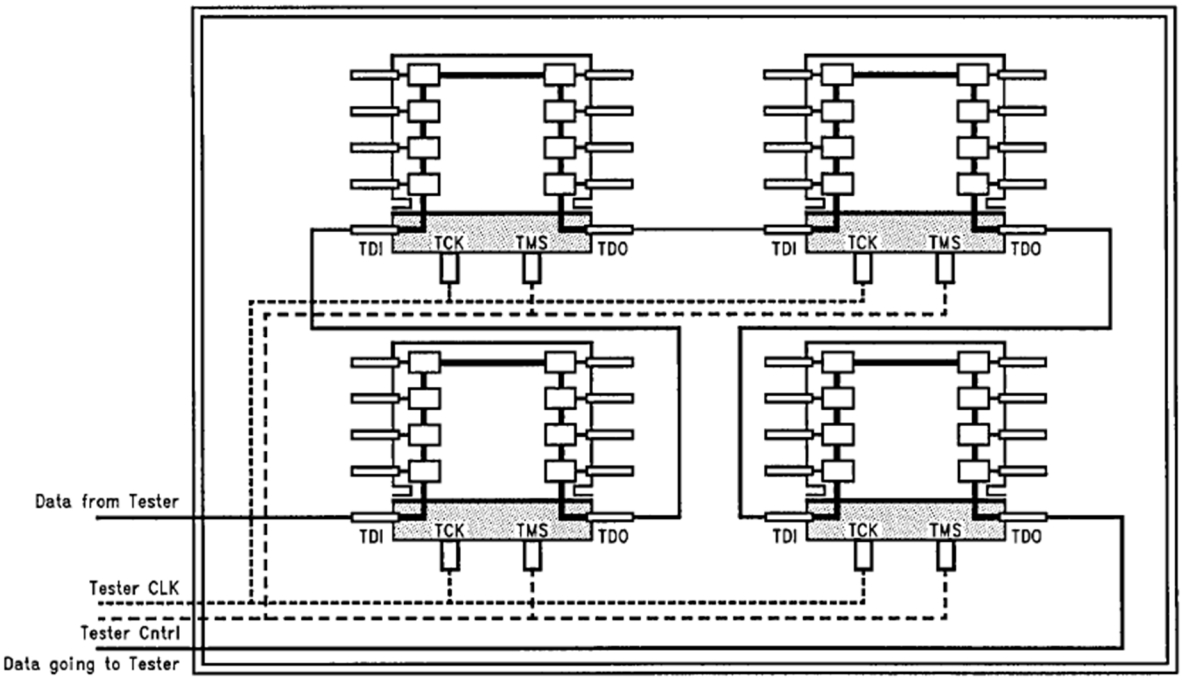
memory device and data buses communicate data for memory reads and writes. Memory devices also include control pins. Examples of control pins are write-enable and chip-select.

50. In typical systems involving memory devices, there is a dedicated address bus that carries address information to the memory, such as row and column addresses, and that has a width that grows with the physical storage on a memory device. There is also a dedicated data bus that communicates read and write data between the CPU and the DRAMs. Finally, the control signals comprise the output enables, chip enables and other related signals. These signals are typically controlled by a memory controller, that was either integrated with or separate from the CPU, and connect to every DRAM in the system.

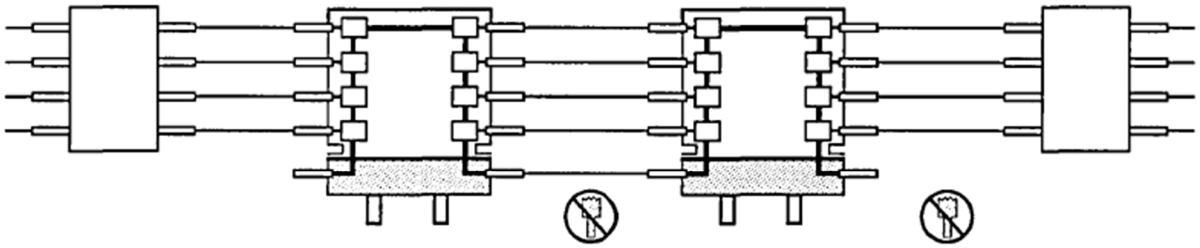
51. As of the filing date of the ’473 Patent, there were also several types of techniques for testing circuits. Since the 1990s, a testing technique called boundary scan has been used to test blocks within integrated circuit and signal lines on printed circuit boards (PCBs). In 1990, the Institute of Electrical and Electronics Engineers (IEEE) standardized a specification for boundary scan, called IEEE 1149.1, that was developed by the Joint Test Action Group (JTAG). IEEE 1149.1, also known as JTAG, is a 4-wire interface with Test Data In (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK) wires. *See* National Semiconductor Scan Databook (EX1008), at 18.



52. The JTAG interface connects to boundary scan registers that are to be placed at all I/O pins of device logic to form a serial chain of registers around the core functionality of the device logic between the TDI and TDO terminals. Additionally, the test interface for multiple circuit components can be connected together to form a larger serial chain. *See id.* at 19.



53. Although boundary scan was often used with dedicated test equipment to perform testing of circuit components and wires, it was also used with in-circuit testing (ICT) to test structural faults. *See id.* at 20.



Boundary scan works with an ICT to provide access to inaccessible nodes and/or to reduce ICT physical test points

54. In addition, boundary scan and hardware to use it could be embedded into a system without the use of external test equipment. System-level embedded test allows for off-the-shelf software tools to generate tests for various types of device logic. *See, e.g.*, *id.* at 20-21.

55. As discussed above boundary scan applied to the testing of individual circuit components, as well as wires between components. One type of test for testing the wires between component is known as EXTEST, which was implemented as a mandatory test instruction in IEEE 1149.1. EXTEST isolates the core logic of a circuit component from the input and output pins except for the test data flow. *See* Bleeker et al., Boundary Scan Test: A Practical Approach (EX1009), at 45-47. Because the output pins from one circuit component may be connected to those of another component, such as circuit components connected to a bus, only one component can drive its output at a time while the other connected components are kept in a high-impedance (HIGHZ) state. *Id.*

56. Boundary scan was also extended to support other types of tests such as built-in self-test (BIST) capability of a circuit component, which is a self-contained self-test of the circuit component. *See, e.g.*, Built-In Self-Test (BIST) Using Boundary Scan (EX1010), at 5. BIST often reduces the amount of time and energy required to perform testing. *See id.* at 10. For example, it does not require loading complex test data before running a test. *See* Bleeker et al., Boundary Scan Test: A Practical Approach (EX1009), at 48. Further, BIST can be used with other test techniques such as pseudo-random seed values to be input into a circuit component, data compression capabilities to generate signatures indicative of test

results, and parallel signature analysis (PSA). Built-In Self-Test (BIST) Using Boundary Scan (EX1010), at 10-11.

VIII. Claim Construction

57. I have interpreted the terms of the ’473 Patent according to their plain meaning. In interpreting the terms, I have carefully considered and applied the claim construction standard referred to in Section IV above.

IX. Summary of Opinions

58. In my opinion, U.S. Patent No. 5,072,138 to Slemmer entitled “Semiconductor Memory with Sequential Clocked Access Codes for Test Mode Entry” (“Slemmer”) renders obvious 1-5, 7, 9-10, 13-14, 20-24, 26, 28-29, 32-33 of the ’473 Patent (*see infra* at Section X).

59. In my opinion, Slemmer in combination with U.S. Patent No. 6,308,232 to Gasbarro entitled “Electronically Movable Terminator and Method for Using Same in a Memory System” (“Gasbarro”) renders obvious claims 1-5, 7-10, 13-14, 20-24, 26-29, 32-33 of the ’473 Patent (*see infra* at Section XI).

60. A table of the grounds is provided below for ease of reference:

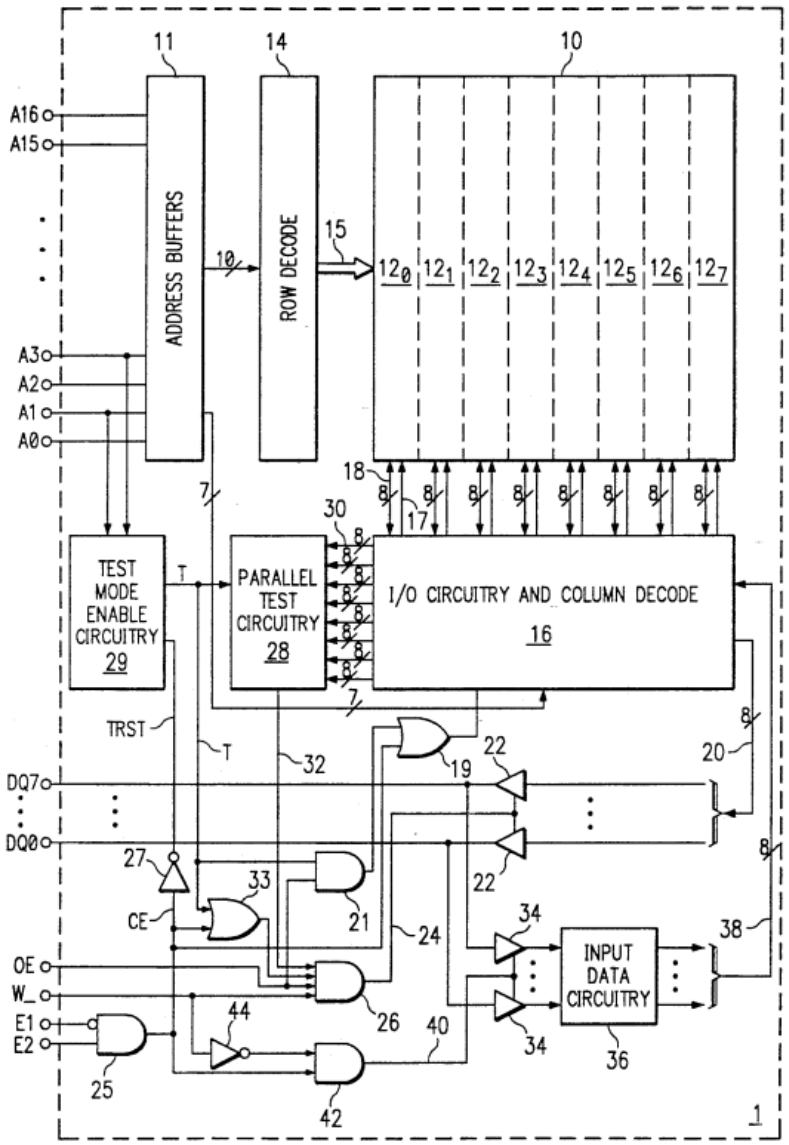
	Grounds	**Claims**
1	§103: Slemmer	1-5, 7, 9-10, 13-14, 20-24, 26, 28-29, 32-33
2	§103: Slemmer in combination with Gasbarro	1-5, 7-10, 13-14, 20-24, 26-29, 32-33

A. Overview of Slemmer (EX1005)

61. Slemmer was filed on August 17, 1990 and issued on December 10, 1991. Slemmer (EX1005), at 1. Slemmer discloses a system in which only one memory of many is tested at any one time. Slemmer (EX1005), at Abstract, 5:3-14, 37:11-24. Slemmer explains that the entry into the test mode is designed to avoid inadvertent entry by requiring a specific sequence of inputs, such as a sequence of codes. *See id.,* at 5:3-14, 10:35-47, Abstract. During testing, one or more output terminals in Slemmer (e.g., DQ0 to DQ7) may be placed in a high-impedance state or may be placed in a low-impedance state to acknowledge entry into the test mode. *See id.* at Abstract, 35:22-36:68, Fig. 9. Slemmer also discloses a solution for bus contention issues during testing in which the output enable (OE) terminal of the memory serves as a chip enable while the memory is in a test mode. *See, e.g.*, *id.* at 36:58-68, 37:11-26.

62. Figure 1 of Slemmer is an electrical diagram, in block form, of a memory device, according to a preferred embodiment. As shown below, the figure shows one of the memories 1 in the system with parallel address (e.g., A0 to A16), parallel data (e.g., DQ0 to DQ7), an output enable (OE), a write enable (W_), and chip enable (e.g., E1, E2) terminals.

FIG. 1



Slemmer (EX1005), at FIG. 1, 8:59-61, 37:11-24. The memory 1 includes test mode enable circuitry (TMEC) 29, which receives input signals via signal lines from address terminals A1 and A3, and an input signal TRST via a signal line coupled to the chip enable terminals E1 and E2 via AND-gate 25 and inverter 27. *Id.* at 9:19-30, 9:44-48, FIGS. 1-2b. Test mode enable circuitry (TMEC) 29

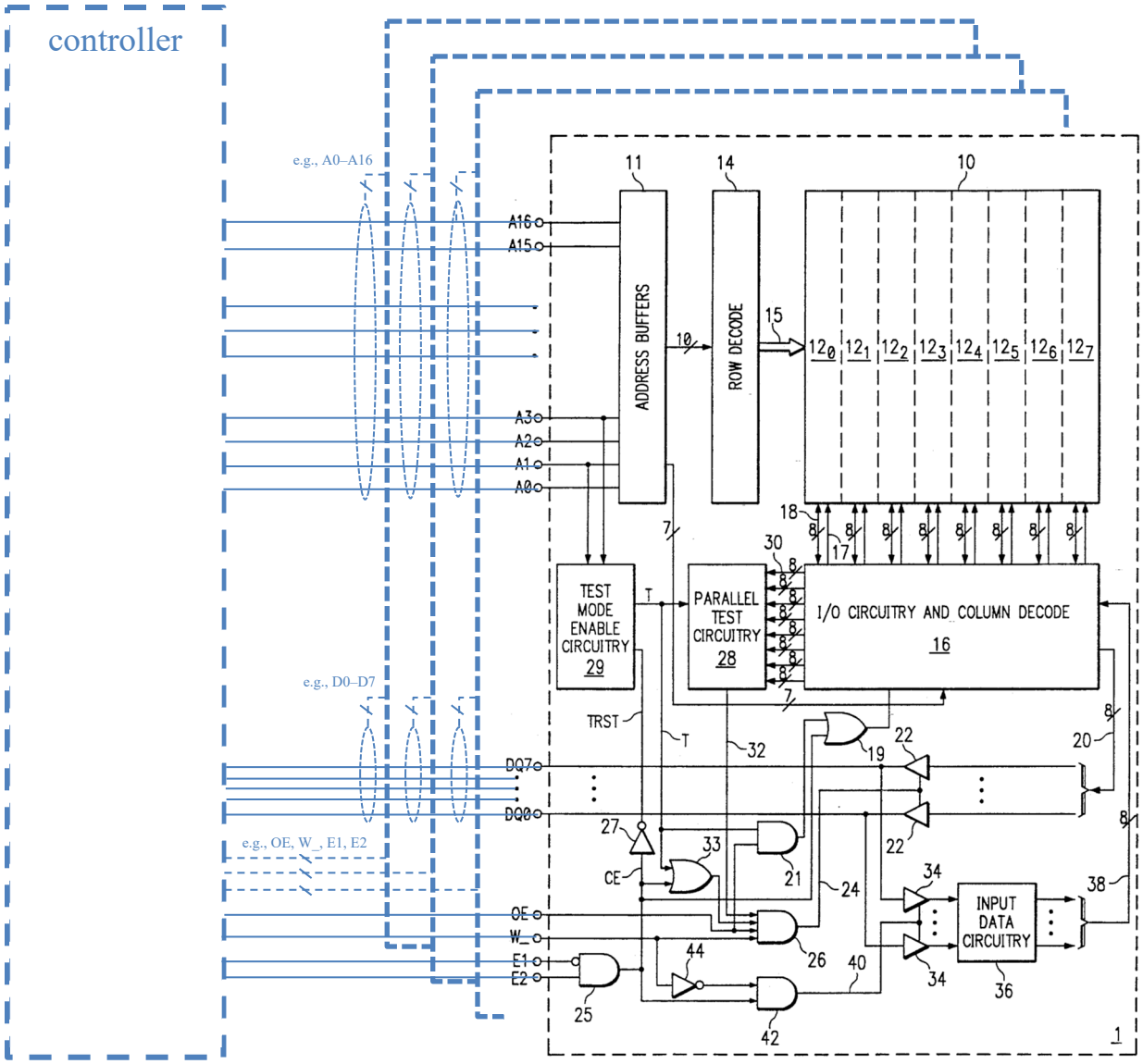
indicates to parallel test circuitry (PTC) 28 whether a test mode is enabled by generating a high logic level output signal on signal line T. *Id.*

63. As shown above in Figure 1 of Slemmer, parallel test circuitry (PTC) 28 receives the signal on signal line T from test mode enable circuitry (TMEC) 29, receives 8-bit data sets on lines 30 from input/output circuitry and column decoder 16, and generates a signal on signal line 32, which is input to AND-gate 26. *Id.*, FIGS. 1-2b, 7:35-8:58, 9:10-30. During normal operation, the signal on signal line 32 has a high logic level. *Id.* The signal also has a high logic level during testing when each of the data sets contains the same data, which indicates that there was no error and thus the test was successful. *Id.* However, when the data sets contain different data, the parallel test circuit (PTC) determines there was an error and thus the test was not successful and outputs a low logic level on signal line 32. Further, as shown above in Figure 1 of Slemmer, when signal line 32 is logic low, the output of AND-gate 26 is also logic low, which disables or deactivates the output buffers 22. *See id.* at FIG. 1. In my view, A POSITA would therefore have understood from Slemmer's disclosure that there is no output via output buffers 22 if an error occurs during testing and that there is an output via output buffers 22 if there is no error during testing and the test is a success. *See id.*

64. In addition to receiving an input from signal line 32, AND-gate 26 receives three other inputs and provides an output to control whether the output

buffers/drivers 22 drives data terminals (e.g., DQ0 to DQ7) to output the data from the internal output data bus 20, or whether the drivers 22 present a high-impedance state. Slemmer (EX1005), at 7:26-35. A POSITA would have recognized that the AND-gate 26 performs a logical AND function between the inputs such that a logic low on any input results in a logic low output from AND-gate 26. Further, the memory 1 in Slemmer provides an acknowledgement of entry into a test mode by presenting a low impedance state on one or more data terminals (e.g., DQ0), which are each driven by one of the drivers 22 that are controlled by AND-gate 26. EX1005, Abstract, 36:36-67.

65. Slemmer does not illustrate his system with memory 1. However, in my view, a POSITA would have understood that the conceptual figure below illustrates a system with multiple memory devices according to Slemmer's teachings:



Slemmer (EX1005), at FIG. 1 (annotated in view of Slemmer's teachings as I explain below). Consistent with the annotations, Slemmer discloses that multiple memories are connected together in parallel. Slemmer (EX1005), at 8:14-19, 36:60-64, 37:11-24, FIG. 1. As shown by the annotations in blue, Slemmer teaches to a POSITA that multiple memories 1 are connected via terminals to multiple signal lines, which are also connected to a controller, such as one in a system or

test equipment. The address terminals are connected to an address bus that is connected to the multiple memories 1 and the controller, and the data terminals are connected to a data bus that is connected to the multiple memories 1 and the controller. In addition, control terminals, such as output enable (OE), write enable (W_), and chip enable (E1, E2), are connected to control lines between the controller and the memory 1 so that the controller can control the memory 1. There are also control lines connected to the other memories 1.

66. In my view, a POSITA would have understood from Slemmer's disclosure that circuitry, commonly known as a memory controller, must be connected to the multiple memories to control and use them, such as by sending signals to and receiving signals from the memories. As I explained in the Technology Background in Section VII, the address, data, and control signals are typically controlled by a memory controller that is either integrated with or separate from the CPU that provides write data and receives and processes read data. *Supra* Section VII. Further, as I explain below, a memory controller is a well-known device for interfacing with memory.

67. For example, U.S. Patent No. 5,784,331 to Lysinger entitled "Multiple Access Memory Device" illustrates a system in which the CPU (PENTIUM) and a controller provide and receive signals from two memory devices.

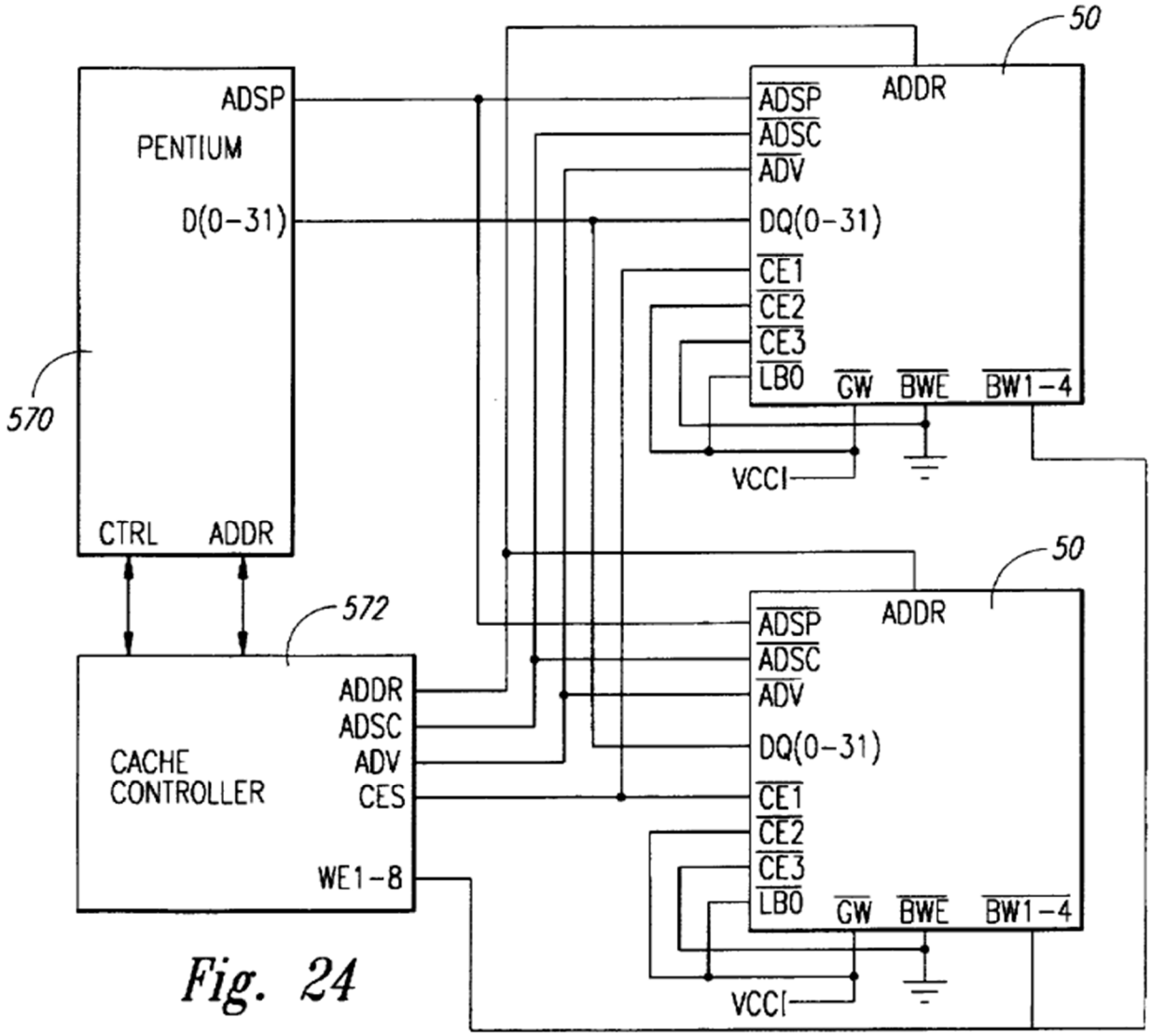


Fig. 24

Lysinger (EX1011), at FIG. 24. Lysinger explains that a memory controller may provide address and timing signals under instructions from a master microprocessor. *See id.* at 18:51-54 ("This is particularly advantageous in those situations where there is a memory controller which provides the address and timing sequence under the instructions of a master microprocessor."); *see also id.* at 8:9-13 ("A further advantage is that a memory controller or microprocessor has

a large time window in which to provide the new address data to the memory device 50 containing a burst counter 40 in accordance to the present invention."). As shown above in Figure 24 of Lysinger, the processor 570 works with the controller 572 to provide "full 32-bit read/write access from each of the memory devices 50." *Id.* at 26:8-12, FIG. 24.

68. Although Lysinger illustrates the processor connected to the data bus, it was also well-known that the controller is connected to the data bus. For example, U.S. Patent No. 5,559,753 to Kocis entitled "Apparatus and Method for Preventing Bus Contention During Power-Up in a Computer System With Two or More DRAM Banks" ("Kocis") illustrates a conventional computer system in its Figure 1:

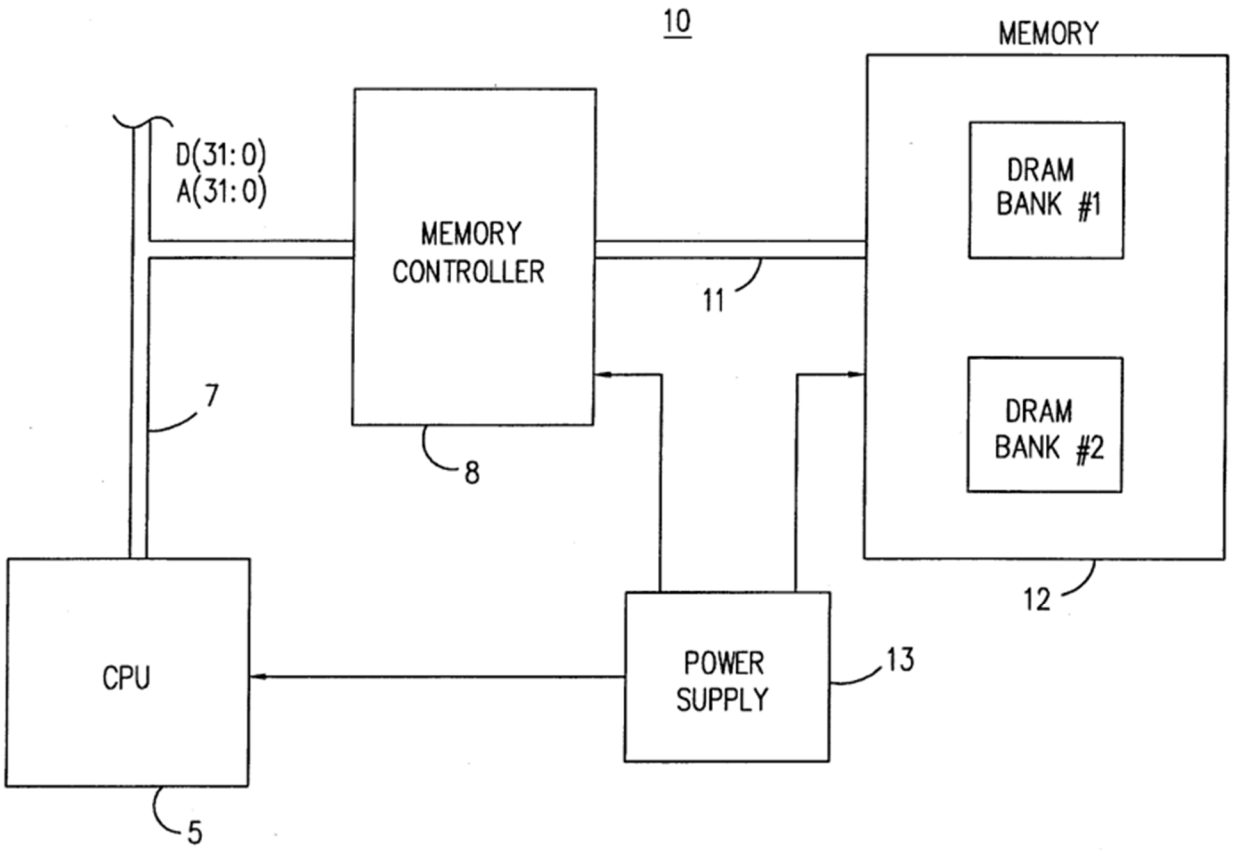


FIG. 1

Kocis (EX1012), at FIG. 1. As shown the local bus with address and data lines is coupled to the CPU 7 and a memory controller 8, which is coupled to memory 12 via a memory bus 11. *Id.* at FIG. 1, 1:16-21. Kocis explains that memory bus 11 comprises "memory address lines, memory data lines, and various control lines." *Id.* at 1:49-52.

69. Consistent with a memory controller being a well-known structure for interfacing with memory, Slemmer teaches how the memory interfaces with a memory controller, as I explain below. For example, Slemmer teaches that the memory 1 must receive address information at its address terminals. Slemmer

(EX1005), at 6:9-11 ("Memory 1 includes seventeen address terminals A0 through A16, for receiving the seventeen address bits required to specify a unique memory address."), FIG. 1; *see also* Slemmer (EX1005), at 6:18-23 ("Signals corresponding to the remaining seven address terminals (A0 through A6) are received by input/output circuitry and column decoder 16 to select one of sub-arrays 12 by way of control lines 17, and to select the desired columns therein according to the column address value.").

70. In addition, Slemmer teaches that data is both input to the memory 1 for write operations and output from the memory 1 for read operations or testing. *See id.* at 1:33-38 ("…the necessity of both writing data to and reading data from each of the bits in the memory"), 7:26-30 ("Each line of output data bus 20 is received by non-inverting output buffer 22, which drives the output terminal DQ with the correct data state, at levels and currents corresponding to the specifications of memory 1."), 8:59-67 ("It should be apparent from FIG. 1 that memory 1 is a common input/output memory, and as such terminals DQ both present output data and receive input data. Terminals DQ are thus connected to input buffers 34, which during write operations present the input data to input data control circuitry 36, which will communicate the input data, via input data bus 38, to the selected memory cells via input/output control circuitry and column decoder 16."), 35:22-42 ("…memory 1 can communicate its special test mode status,

providing the user (or the interrogating test equipment) acknowledgment that the device is in a special test mode…"), FIG. 1.

71. Further, Slemmer teaches that control terminals of memory 1 (e.g., OE, W_, E1, E2) are driven external to memory 1 or receive signals. Slemmer (EX1005), at 8:4-5 ("A second input received by AND gate 26 is the write enable signal received at terminal W_."), 37:27-29 ("…terminal OE is externally driven to a low logic level when memory 1 is in test mode…"), 37:33-37 ("…re-selection of memory 1 in test mode is accomplished by externally driving terminal OE…"), FIG. 1; *see also* Slemmer (EX1005), at 32:64-33:2 ("[T]he exit from special test mode is effected merely by the enabling of memory 1 by way of the chip enable function. Such enabling is of course available to the system user of memory 1, since enabling by chip enable is a necessary and specified function of this example of memory 1.").

72. Slemmer also teaches considerations for a system designer, such as the number of external terminals and support for inserting memory into a system already powered up. Slemmer (EX1005), at 3:1-16, 3:39-60, 35:52-64. Additionally, Slemmer teaches that a system or test equipment is required to test the memory by, for example, controlling when testing is enabled and receiving an acknowledgement of entry into a test mode. Slemmer (EX1005), at 1:21-22, 3:11-16, 32:64-33:2, 35:22-42, 35:47-51, 36:55-68.

73. In my view, a POSITA would have understood from Slemmer's disclosure, as discussed above, that the data and address terminals of the multiple memories are connected together and to the controller via signal lines, any combination of which is a bus. *See* Slemmer (EX1005), at FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:14-19, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 37:11-24, 37:27-29, 37:33-37. For example, in the annotated system of Slemmer in Paragraph 65 above, data lines D0 through D7 and address lines A0 through A16 are connected between the multiple memories 1. *Id.* at FIG. 1 (annotated above). Further, a POSITA would have understood from Slemmer's disclosure regarding the control or enable terminals, such as output enable (OE) and chip enable (E1, E2), that such terminals of multiple memories would not be connected together in Slemmer's system because the controller must be able to enable each of the memories independent of the other memories for testing. *See id.*, at 8:14-19, 36:60-64, 37:11-26, FIG. 1. Rather, the controller would provide unique enable or control signals for each of the multiple memories such as a unique output enable (OE) signal. *See id.* A POSITA would have understood from Slemmer's teaching that such functionality enables a memory being tested to avoid data contention problems on the bus that is also connected to the other memories. *See id.*; *see also* Bleeker et al., Boundary Scan Test: A Practical Approach (EX1009), at 45-47 (discussed above in Section VII).

B. Overview of Gasbarro (EX1006)

74. Gasbarro was filed on September 1, 1999. Gasbarro (EX1006), at p.1. Gasbarro discloses a system with a plurality of memory devices each with an electronically activated terminator and a method for detecting the last memory device arranged along a bus connecting a memory controller to the memory devices and activating the last device's active terminator. *Id.*, Abstract.

75. As shown below, Gasbarro discloses a conventional memory system that includes a memory controller (M) for writing data into and reading data from memory devices (D) via a bi-directional bus.

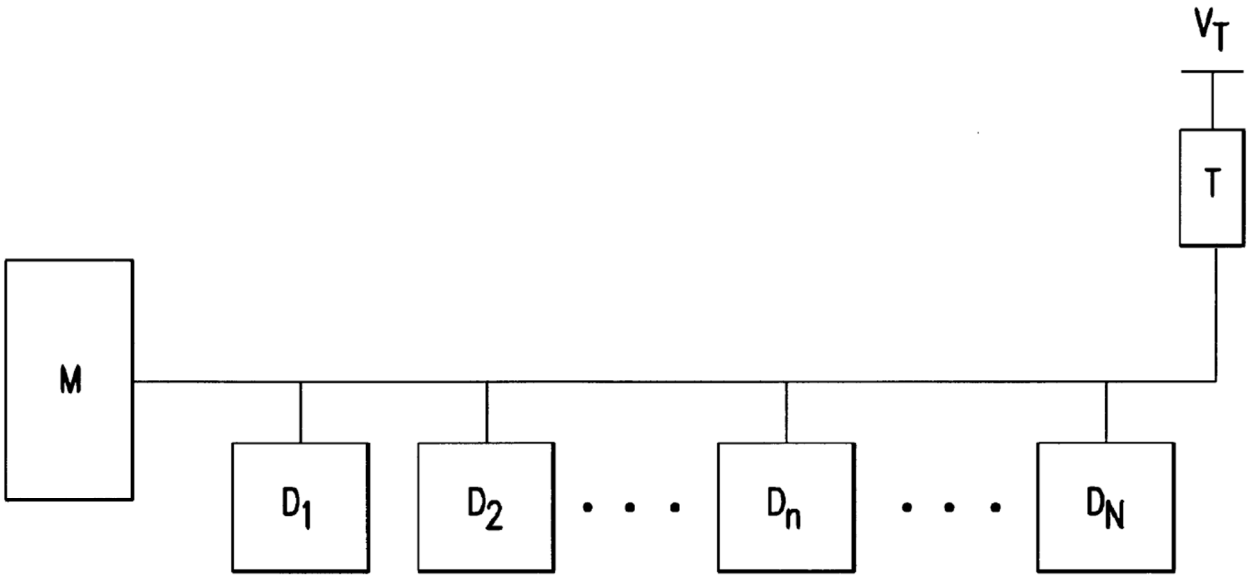


FIG. 1
PRIOR ART

Id., FIG. 1, 1:15-19; *see also id.*, FIG. 2. The devices (D) connected to the bus have a predetermined characteristic impedance and each signal line of the bus

terminates at an input/output pin of the controller (M) and a terminator (T). *Id.*, 1:19-27. Gasbarro explains that without "balance between the various memory system components . . . the signal line impedance will depart from its desired impedance," which "will result in unwanted signal reflections . . . and in increased signal line noise." *Id.*, 2:59-64.

76. To enable impedance balance in an expandable memory system, Gasbarro discloses that the controller may balance bus impedance by using an active terminator. *Id.*, 3:42-45. As shown in the figure below, the controller 70 uses a serial initialization line (SIL) 72 or channel 71 to communicate an active termination signal to any one of the devices (D).

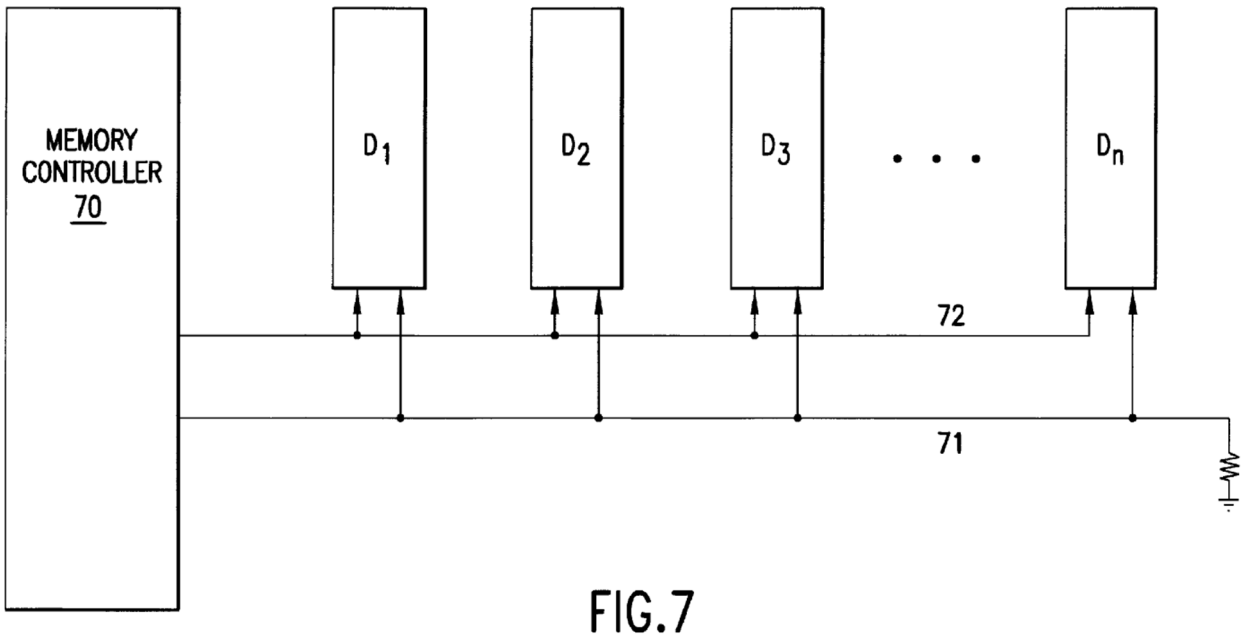


FIG.7

Id., FIG. 7, 6:49-54. The controller determines which device is the last on the data bus (D_n) during initialization and then enables the active terminator on that device.

Id., 6:55-7:5. By enabling the active terminator, the controller 70 balances impedances in the memory system to avoid signal reflections on the bus. *Id.*, 7:6-14.

X. Claims 1-5, 7, 9-10, 13-14, 20-24, 26, 28-29, 32-33 are Obvious over Slemmer

77. In my opinion, Slemmer renders obvious claims 1-5, 7, 9-10, 13-14, 20-24, 26, 28-29, 32-33 of the '589 Patent.

A. Claim 1

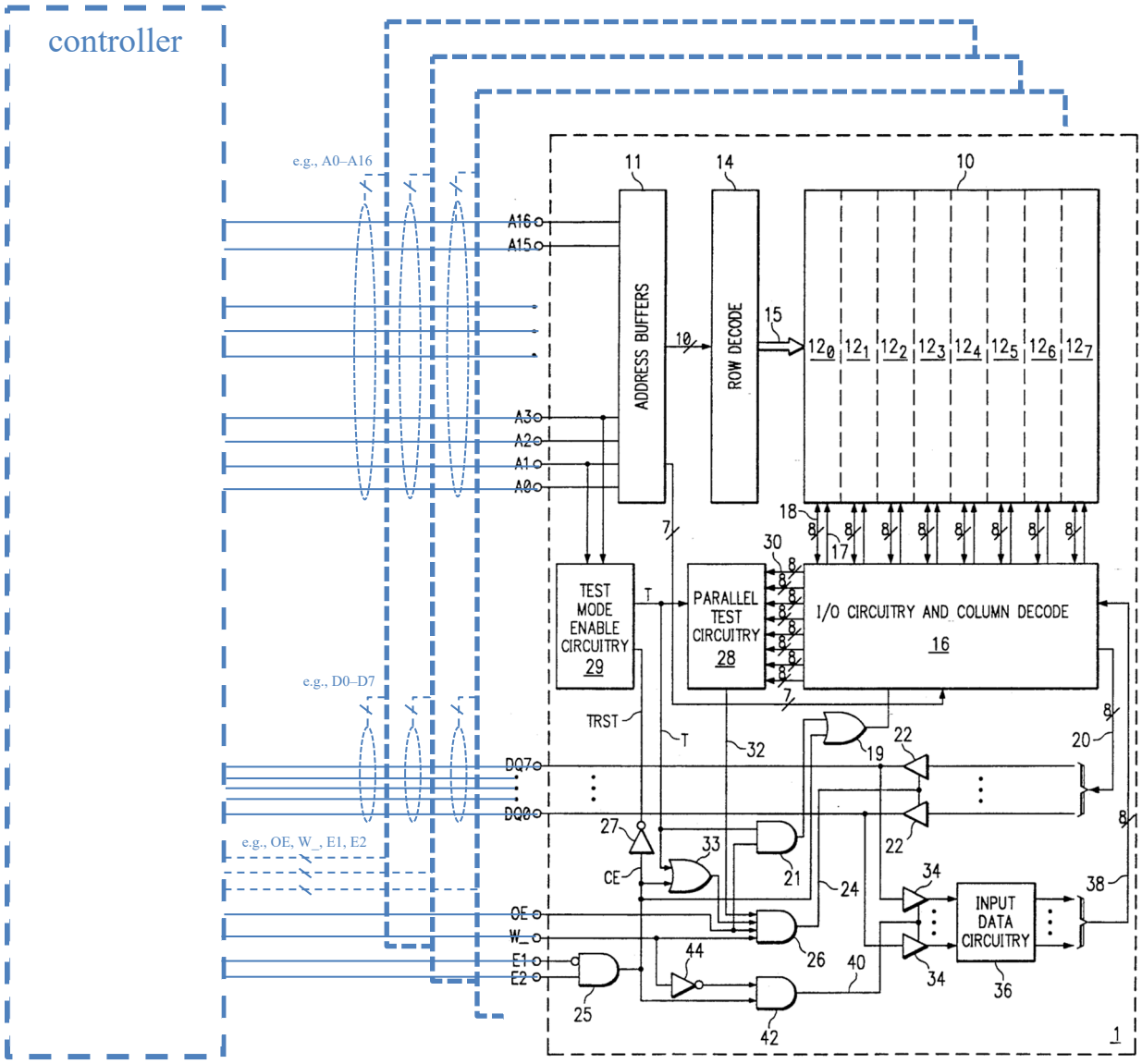
1. Claim Element [1.P]: "An electrical circuit comprising:"

78. I understand that the preamble of claim 1 is not limiting. Nevertheless, to the extent the preamble is found to be limiting, Slemmer teaches and discloses an electrical circuit that includes multiple integrated circuit memories that are connected via a bus. Slemmer (EX1005), 37:11-24, FIG. 1. Slemmer discloses that the electrical circuit is configured such that only one of the memories, such as memory 1 in Figure 1 of Slemmer, is to be tested at a time. *See id.* I discuss the functionality of Slemmer's system in more detail below, with respect to the claim elements of claim 1.

2. Claim Element [1.1]: "a bus; and"

79. As I explain below, Slemmer teaches data and/or address I/O connections that are connected to signal lines in which one or more signal lines is "*a bus*." Indeed, a "bus" was a widely known term of art that means "[o]ne or more

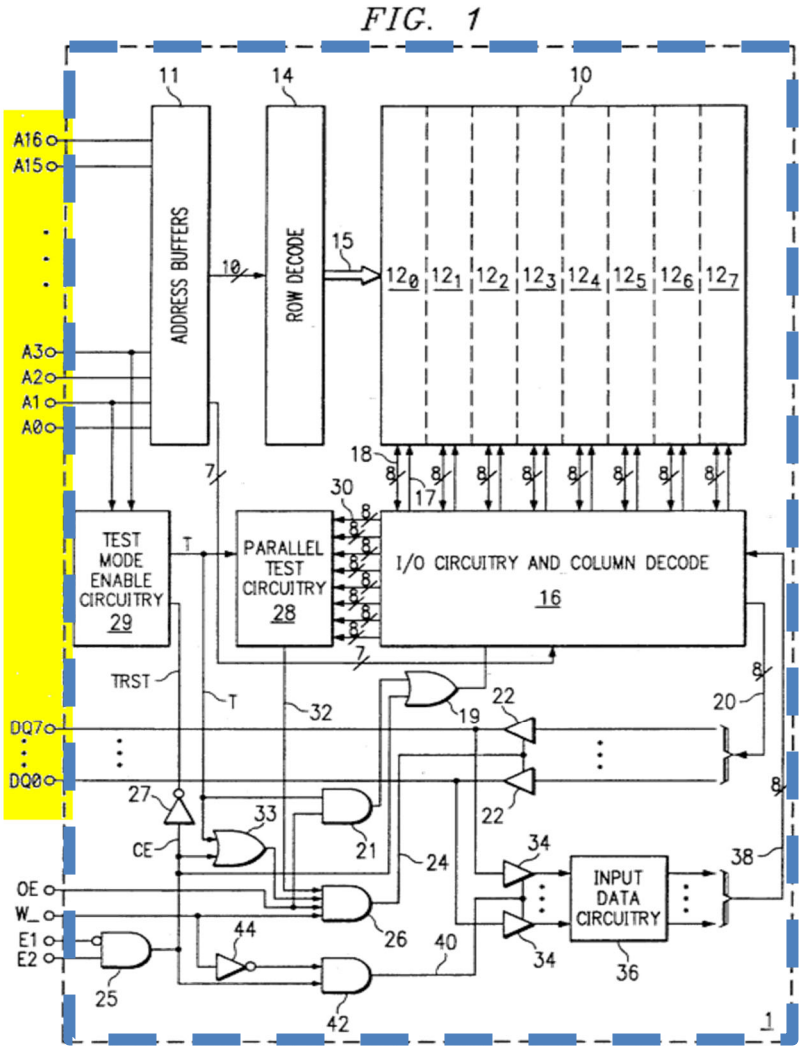
conductors that are used for the transmission of signals, data, or power." EX1007, at 9. As I explained in Section IX.A above, although Slemmer does not illustrate his system, the conceptual figure below illustrates Slemmer's system with multiple memory devices in accordance with Slemmer's teachings:



Slemmer (EX1005), at FIG. 1 (annotated in view of Slemmer's teachings as discussed in Section IX.A above). As shown in the annotated figure, Slemmer

teaches that multiple memories are connected together, via their terminals and signal lines, and to a controller, such as one in a system or test equipment. *See* Slemmer (EX1005), at FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:4-5, 8:14-19, 8:59-67, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 36:55-68, 37:11-24, 37:27-29, 37:33-37; *see e.g.*, EX1011, 18:9-13, 18:51-54, 26:8-12, FIG. 24; EX1012, FIG. 1, 1:16-21, 1:49-52.

80. As shown in Figure 1 of Slemmer below, Slemmer discloses that each memory 1 (annotated in blue in the figure below) has multiple terminals.



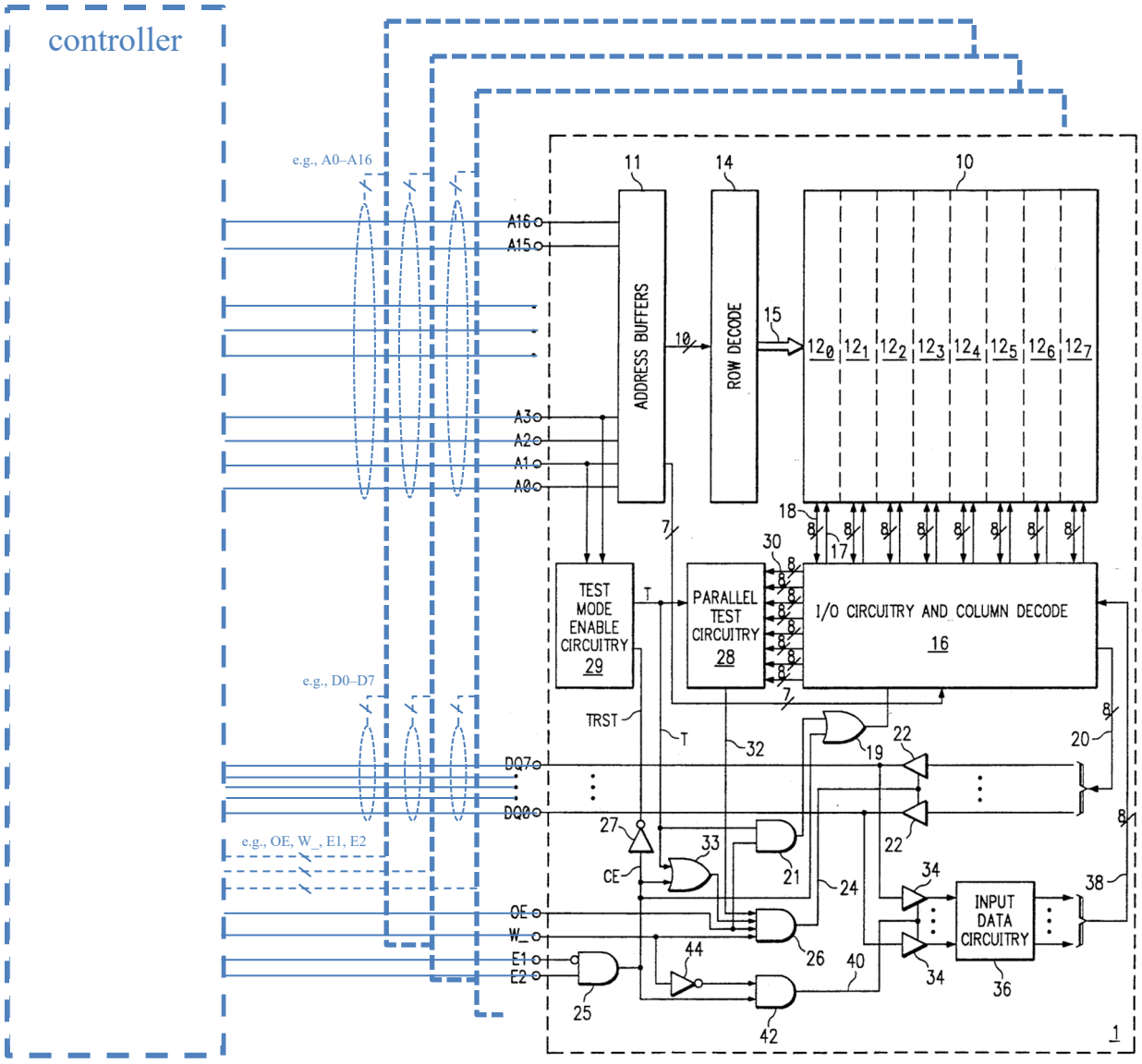
Slemmer (EX1005), at FIG. 1 (annotated above), 5:50-64, 6:9-29, 6:54-66. As shown, the memory 1 has multiple data input/output (I/O) terminals, such as DQ0 through DQ7 (annotated in yellow in the figure above), and multiple address terminals, such as A0 through A17 (annotated in yellow in the figure above). *See id.* Although Slemmer illustrates a static random access memory (SRAM) in Figure 1, Slemmer explains that his teachings benefits other memory types, such as dynamic random access memory (DRAM). *See id.*

81. Slemmer explains that the data I/O terminals receive input data, such as during write operations, and send output data, such as during read operations, and that. Slemmer (EX1005), at 7:15-34, 8:59-9:9, FIG. 1. Slemmer also explains that the address terminals receive a unique memory address and a test mode enable signal. *See id.* at 6:9-29, 9:19-30, FIG. 1. In addition, Slemmer discloses that multiple memories are connected in parallel. *See, e.g.*, *id.* at 37:17-18. Thus, in my opinion, it is obvious to a POSITA that Slemmer's data I/O connections and/or address connections are connected to signal lines and that one or more of those signal lines are "*a bus*."

3. Claim Element [1.2]: "a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components;"

82. As explained above in Section X.A.2 for claim element [1.1], Slemmer teaches that the data I/O connections and address connections are connected to signal lines and that one or more of the signal lines are "*a bus*." *See* Slemmer (EX1005), 35:22-42, 37:11-37.

83. Slemmer also teaches that multiple memories, each similar to memory 1, are connected in parallel via the bus.



Slemmer (EX1005), at FIG. 1 (annotated in view of Slemmer's teachings as discussed in Section IX.A above); *see also* EX1005, at 37:11-19. As shown in the figure, Slemmer's system illustrates multiple signal lines for the address information, such as the signal lines for A0 through A16, and multiple signal lines for the data information, such as the signal lines for D0 through D7. *See id.* Multiple signal lines that transfer data in parallel are commonly known to a POSITA as a

parallel bus. As shown in the figure above, Slemmer teaches that multiple signal lines are connected between multiple memories, which are connected to the multiple signal lines in parallel. *See id.* Accordingly, Slemmer teaches the multiple memories ("*a plurality of circuit components*") are connected together via one or more of the signal lines for the data I/O and/or address ("*which are connected via said bus*").

84. In addition, Slemmer teaches that only one of the multiple memories 1 is tested at a time:

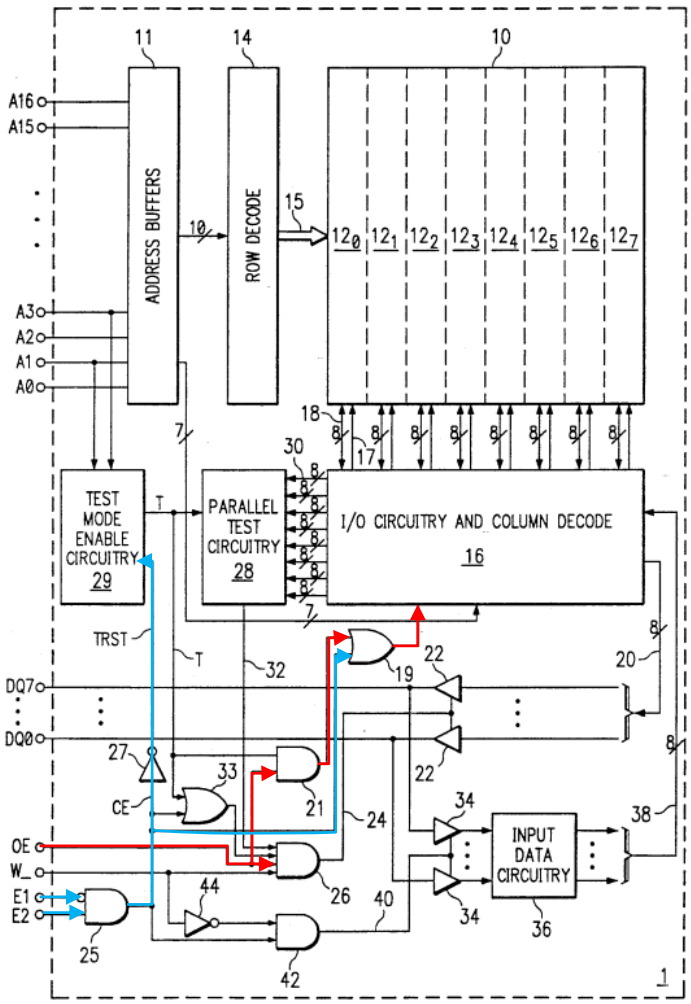
> "Accordingly, the output enable terminal OE serves not only to control the enabling and disabling of output buffers 22, but also serves as a chip enable terminal during a test mode. Such a function is especially useful if a special operating mode, such as a special test mode, is to be enabled when multiple memories 1 are connected in parallel and only one (or one bank) of memories 1 is to be tested. Since the chip enable terminals E1 and E2 in this embodiment provide exit from test mode, in this embodiment it is especially useful that the output enable terminal OE provide the chip enable control of memory 1. It is contemplated that other embodiments of the logic shown in FIG. 1 for accomplishing such control will now be apparent to those of ordinary skill in the art.
>
> In the example of FIG. 9, at time t_5 terminal OE is externally driven to a low logic level when memory 1 is in test mode (line T at a high logic level). Responsive to this signal, the output of AND gate 26 will go to a low logic level, disabling output buffers 22 and placing terminals DQ in a high impedance state, shown at time to. The re-selection of memory 1 in test mode is accomplished by externally driving terminal OE to a high logic level (shown at time t_7), responsive to which terminals DQ again become active and can present data thereat at time t_8. As described hereinabove, memory 1 may exit test mode by way of terminals E1 and E2 receiving the chip

enable code."

Slemmer (EX1005), at 37:11-37 (added emphasis).

85. As shown in the figure below, the chip enable signals (signals E1 and E2, and the resulting CE signal), annotated in blue, and the output enable signal (OE), annotated in red, control whether a particular memory is enabled for testing.

FIG. 1

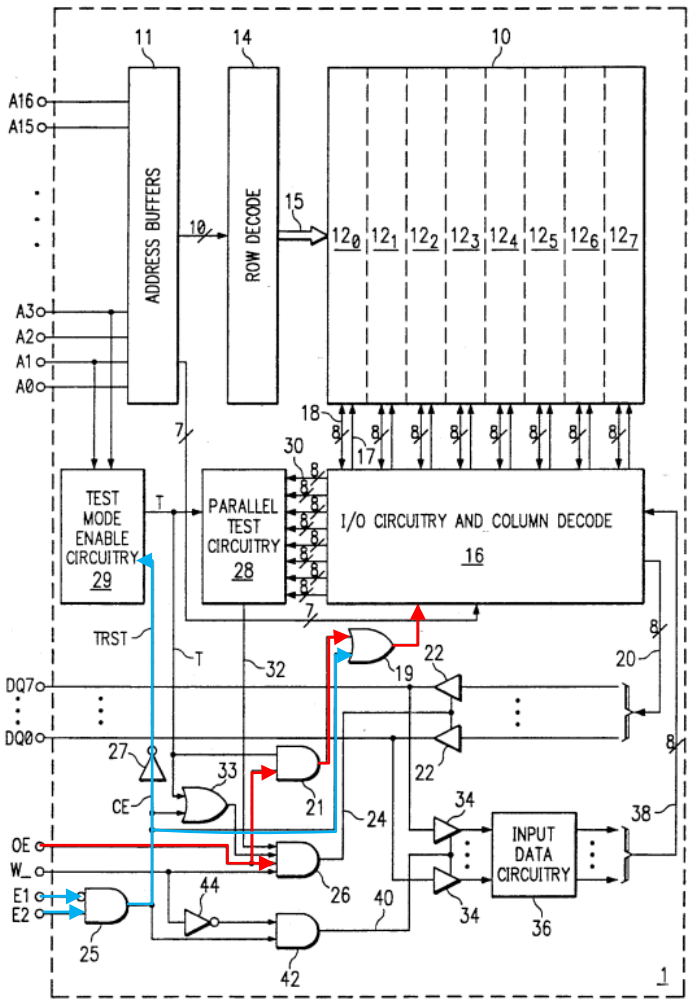


Slemmer (EX1005), at Abstract, 36:57-68, 37:1-20, FIG. 1 (annotated as I discuss below).

86. A POSITA would have understood from Slemmer's disclosure that the chip enable terminals (E1 and E2) are used to enable or disable normal operation for each of the memories. *See id.* at 36:2-25, 8:53-55, 37:19-23, 37:37-39, FIG. 9. Slemmer teaches that normal operation of a memory is disabled when E1 is logic high or E2 is logic low, because the CE signal output from AND-gate 25 would be logic low, which disables or deactivates the output drivers 22 (via OR-gate 33 and AND-gate 26) and disables the operation of I/O circuitry and column decode 16 (via AND-gate 21 and OR-gate 19). *See id.* at FIG. 1. However, when E1 is logic low and E2 is logic level high, the CE signal output from AND-gate 25 is logic high, which exits any testing and enables the operation of I/O circuitry and column decode 16 via AND-gate 21 and OR-gate 19. *See id.* at 7:37-51, 7:56-64; *see also id.* at 8:47-58. A POSITA also would have understood from Slemmer's disclosure that when one of the memories is enabled for testing, each of the other memories could receive signals on the chip enable terminals to disable normal operation or could alternatively receive signals on the chip enable terminals to allow normal operations. *See id.* at 36:2-25, 8:53-55, 37:15-25, 37:37-39, FIG. 9. In particular, a memory device that is enabled for normal operations will drive the TRST signal at a logic low level and prevent entry into a test mode. *See* EX1005, 18:46-53.

87. Additionally, a POSITA would have understood from Slemmer's disclosure that the output enable (OE) terminal is used to enable a particular memory during testing. *See* Slemmer (EX1005), at 37:15-19. Slemmer explains that the output enable (OE) signal serves as a chip enable during testing, which is useful for systems in which multiple memories are installed. *Id.*

FIG. 1



Slemmer (EX1005), at FIG. 1, Abstract, 36:57-68, 37:1-20. As shown by the annotations to the figure in red, the OE signal is input into both AND-gate 26 and

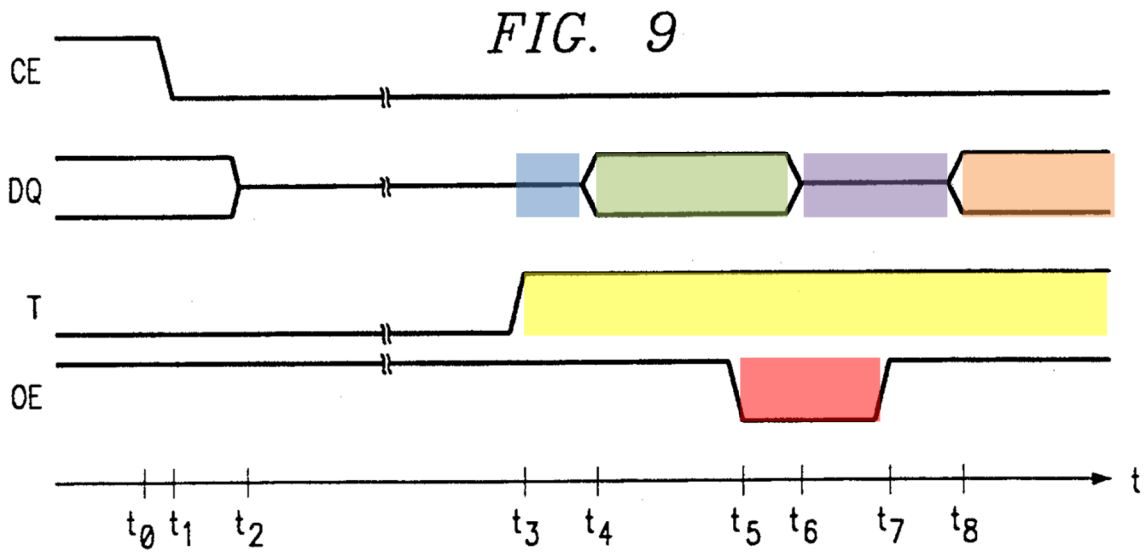
AND-gate 21. *Id.* The output of AND-gate 26 controls the output buffers 22 via line 24, and the output of AND-gate 21 is an input to OR-gate 19, which provides an enable signal for the I/O circuitry and column decode 16. *Id.* at FIG. 1, 37:1-15, 7:56-8:3. Based on Slemmer's teachings, a POSITA would have understood that the particular memory enabled for testing would receive an OE signal that is logic high, which can enable the output buffers 22 via AND-gate 26 and provide a chip enable to the I/O circuitry and column decode 16 via AND-gate 21 and OR-gate 19. *Id.* A POSITA would also have understood that the other memories disabled for testing would receive OE signals that are logic low, which disables the output buffers 22 via AND-gate 26 and can provide a chip disable to the I/O circuitry and column decode 16 via AND-gate 21 and OR-gate 19. *Id.*

88. Thus, a POSITA would have understood that one of the multiple memories 1 in Slemmer is enabled for testing while the other memories are disabled for testing, and thus the memory enabled for testing is to be tested independently from the other memories ("*one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components*").

4. Claim Element [1.3]: "said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus,

and outputting data to said bus that is other than data which would be output to said bus during normal operation."

89. Slemmer discloses a timing diagram in its Figure 9 to illustrate the operation of the test mode enable circuitry (TMEC) and memory, as illustrated in its Figure 1. *See* Slemmer (EX1005), at 5:44-46, FIGS. 1, 2, 9. As shown below, Figure 9 illustrates signals for CE, DQ, T, and OE.



Id. at FIG. 9 (annotated as I explain below). Although Figure 9 shows only one DQ terminal or signal, Slemmer teaches that one *or more* of the DQ terminals can be used by the memory during testing. *See id.* at 36:49-54 ("In addition, it should be noted that not all of the output buffers in a wide-word memory such as memory need be controlled in the manner described hereinabove, as the enabling of a special test mode can be adequately communicated by a selected one of terminals DQ presenting a low impedance state.").

90. As I explain below, Slemmer teaches that the memory 1 is configured to enter the special test mode during which one or more data I/O (DQ) terminals are initially in a high-impedance state, in which no data is output to the bus via the terminals and corresponding drivers ("*outputting no data to said bus*"). *See id.* FIG. 9, 36:10-25, 5:45-48. As shown by the annotation in yellow to Figure 9 above, Slemmer discloses that at time t_3 the test mode signal T goes to a high logic level. *See id.* 36:22-25 ("[U]pon the entry into a special test mode at time t_3 of FIG. 9, line T is driven by test mode enable circuitry 29 to a high logic level."). As shown by the annotation in blue, Slemmer discloses that the DQ terminal is initially in a high-impedance state:

> "The operation of memory 1 upon deselection from terminals E1 and E2 is indicated in FIG. 9, with line CE going to a low logic level at time t1, <u>followed by terminals DQ going to a high impedance state at time t2, as a result of the disabling of output buffers 22</u> by the operation of AND gate 25, OR gate 33, and AND gate 26. The disabling of output buffers 22, and the resultant high impedance state at terminals DQ, in response to deselection of memory 1 is conventional in memories and other integrated circuits having chip enable functions and terminals."

See id. at 36:10-21 (added emphasis). Slemmer also discloses, as shown in Figure 9 above, that at time t_5, the output enable (OE) terminal is externally driven from a high logic level to a low logic level (annotated in red above), which results in the DQ signal transitioning to a high-impedance state at time t_6 (annotated in purple above). *Id.* at 37:27-32, FIG. 9. The OE terminal then is driven back to a high logic

level at time t_7, which results in the DQ signal transitioning again to an active, low-impedance state at time t_8 (annotated in orange above). *Id.* at 37:33-37, FIG. 9.

91. A POSITA would have understood from Slemmer's disclosure that no data is output from the DQ terminals when they are in a high-impedance state because that state is the result of the output buffers 22 being disabled. Buffers or drivers such as those described by Slemmer were well known to be a tristate buffer or a tristate bus driver that outputs a logical high or low signal when enabled by a signal and provides an output that is equivalent to an open circuit when not enabled by the signal. *See, e.g.*, U.S. Patent No. 5,136,185 to Fleming (EX1013), at 1:11-16 ("A tristate bus driver (also called a tristate buffer), when enabled by an enable signal applied to its enable terminal, outputs a logical 1 or 0 signal in response a logical 1 or 0 signal applied to its input. When the tri state bus driver is not enabled by an enable signal, its output is an open circuit."). Thus, Slemmer teaches that during testing, such as between time t_6 and time t_8, that the memory to be tested is configured to output no data to the bus.

92. Further, as I explain below, Slemmer also teaches "*outputting data to said bus that is other than data which would be output to said bus during normal operation*."

93. As an initial matter, the '473 Patent does not explain to a POSITA how to distinguish "data which would be output to said bus during normal

operation" from "other" data output to the bus during testing. *See, e.g.*, '473 Patent, at 3:32-38, 5:58-6:49, 5:56-57, 5:59-67, 6:22-26. In the example provided by the '473 Patent, a value of '0' is output to the bus during testing, but there is no explanation why such a value, or series of values, cannot be output to the bus during normal operation. *See id.*

94. It is my understanding that Patent Owner has asserted that "outputting data through the DQ feedback line" for write leveling satisfies the claim element of "outputting data to the bus that is other than data which would be output to the bus during normal." *See* EX1014 at Paragraph 63. In support of its allegation, Patent Owner points to Figure 1-63 of the Xilinx Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solution v3.0 User Guide, which is reproduced below.

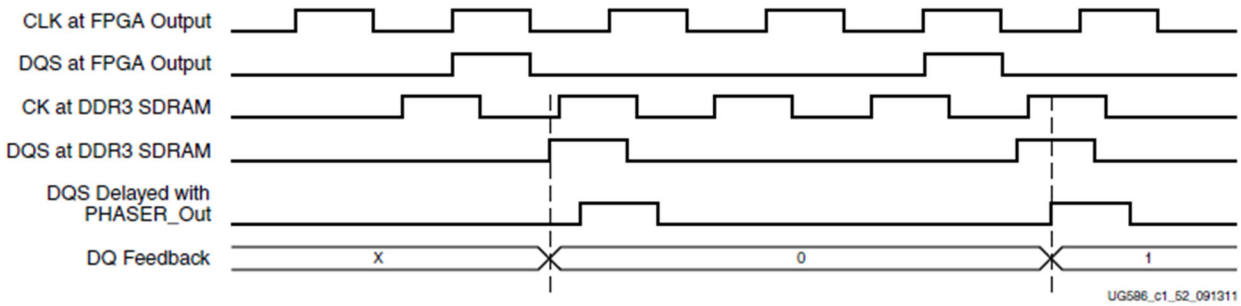
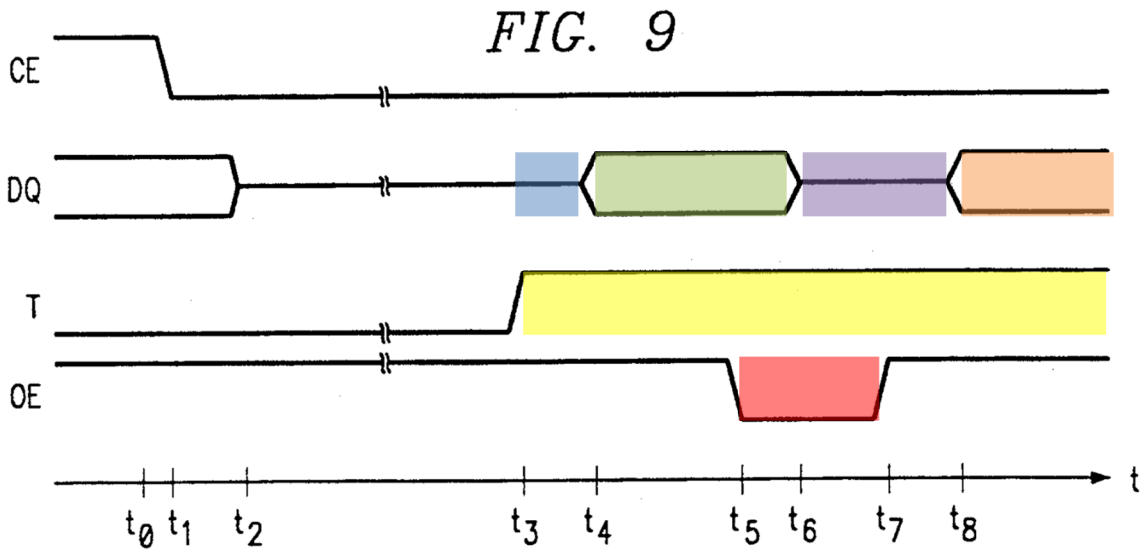


Figure 1-63: **Write Leveling Timing Diagram**

EX1015, at 23 (FIG. 1-63) (cited by EX1014, at 17). As shown in the figure, the "DQ Feedback" has a don't care value ('X'), transitions to a '0' value, and then transitions to '1' value. *Id.* As I explain below, Slemmer also discloses a similar

sequence of values on a DQ terminal between a high-impedance value and a low-impedance value.

95. Slemmer teaches that the memory 1 is configured to the special test mode during which one of more data I/O (DQ) terminals are initially in a low-impedance state, in which data is output to the bus via the terminals and corresponding drivers. *See id.* at 36:10-54, FIG. 9 (annotated below).



At time t_4, Slemmer discloses that the DQ terminal transitions to an active, low-impedance state, as shown by the annotation in green above, in which data is output to the bus. *Id.* at FIG. 9, 36:25-40 ("Responsive to line T at a high logic level, OR gate 33 will present a high logic level to AND gate 26. Since terminals OE and W_ are at high logic levels, and with line 32 from parallel test circuitry 28 remains high (i.e., the parallel test either passed, or has not taken place), terminals DQ go into an active state at time t_4. This condition, where terminals DQ present a

low impedance with chip enable terminals E1 and E2 not selecting memory 1, is unexpected in conventional memory operation, as terminals DQ are expected to remain in a high impedance state when the circuit is not enabled. Accordingly, the presentation of a low impedance state at terminals DQ when memory 1 is not enabled acknowledges entry into a special test mode, without requiring additional terminals for memory 1 for such communication.") (added emphasis). Slemmer explains that, "for purposes of communicating test mode entry, the data state presented at terminals DQ is unimportant," as a low-impedance state at the output is sufficient. *Id.*, 36:41-45. Slemmer also explains that, if desired, additional information is output at terminals DQ, such as an "identification of which test mode has been enabled." *Id.*, 36:45-49. Based on Slemmer's teachings, a POSITA would have understood that the active state of the one or more DQ terminals in Slemmer acknowledges test information, such as entry into a test mode and an identification of which test mode has been enabled.

96. Further, a POSITA would have understood that the data output to the bus during Slemmer's active state in testing is data that is different than the data which would be output during normal operation. Slemmer explains that normal operation is a different mode of operation than a test mode. *See, e.g.*, *id.* at 1:60-67 ("A solution which has been used in the past to reduce the time and equipment required for the testing of semiconductor memories such as RAMs is the use of

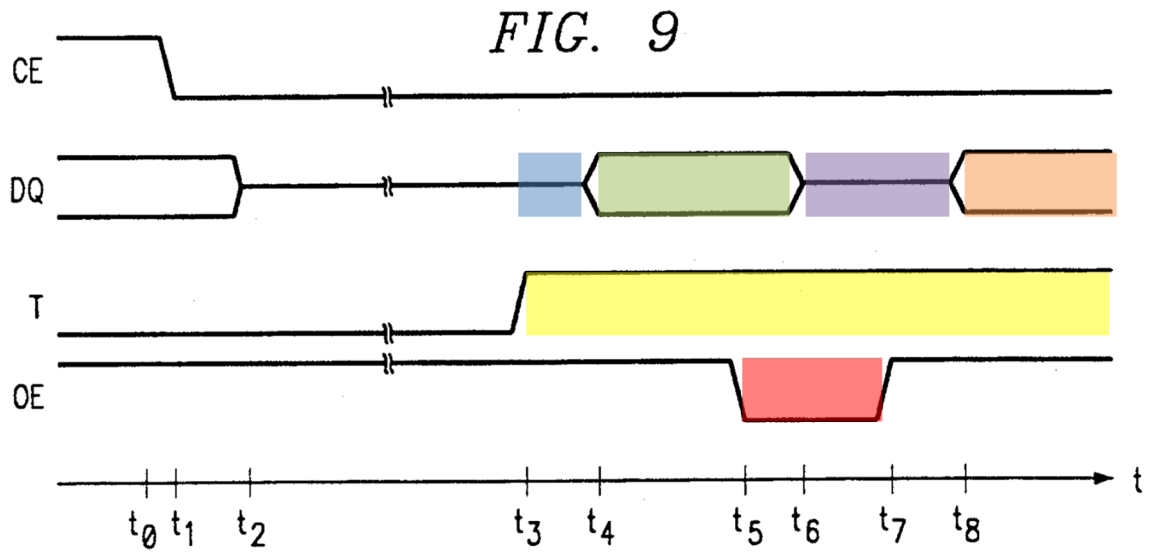
special ‘test’ modes, where the memory enters a special operation different from its normal operation. In such test modes, the operation of the memory can be quite different from that of normal operation, as the operation of internal testing can be done without being subject to the constraints of normal operation.”) (added emphasis). Slemmer also discloses that the DQ terminals have a different function in normal operation than during testing. As Slemmer explains:

> “Memory 1 according to this embodiment of the invention thus is capable of communicating its test mode status by using terminals, such as terminals DQ, which have a function in normal operation. In addition, memory 1 according to this embodiment provides a simple method of exiting a special test mode by use of chip enable, and also provides a chip enable function while in the special test mode by using yet another terminal which has a different function in normal operation. Accordingly, the need for additional terminals for the control and acknowledgment of a special test mode is avoided in memory 1 according to the invention.”

Id. at 37:40-51 (added emphasis); *see also id.* at 5:58-61 (“Accordingly, for example in a read operation, upon the access of one of the memory locations, eight data bits will appear at the eight input/output terminals DQ0 60 through DQ7.”), 8:59-61 (“It should be apparent from FIG. 1 that memory 1 is a common input/output memory, and as such terminals DQ both present output data and receive input data”).

97. Moreover, similar to Patent Owner’s allegations discussed above, Slemmer teaches that one or more DQ terminals transition between a high-

impedance and low-impedance state. Specifically, the DQ terminals transition back to a high-impedance state before transitioning again to an active, low-impedance state.



See Slemmer (EX1005), at FIG. 9. As shown in Figure 9, at time t_5, the output enable (OE) terminal is externally driven from a high logic level to a low logic level (annotated in red above), which results in the DQ signal transitioning back to a high-impedance state at time t_6 (annotated in purple above). *Id.* at 37:27-32, FIG. 9. The OE terminal then is driven back to a high logic level at time t_7, which results in the DQ signal transitioning again to an active, low-impedance state at time t_8 (annotated in orange above). *Id.* at 37:33-37, FIG. 9. Based on Slemmer's teachings, the memory to be tested is configured to perform several operations during testing, including an operation to output no data to the bus via the one or more DQ terminals, when the terminals are in a high-impedance state, and an

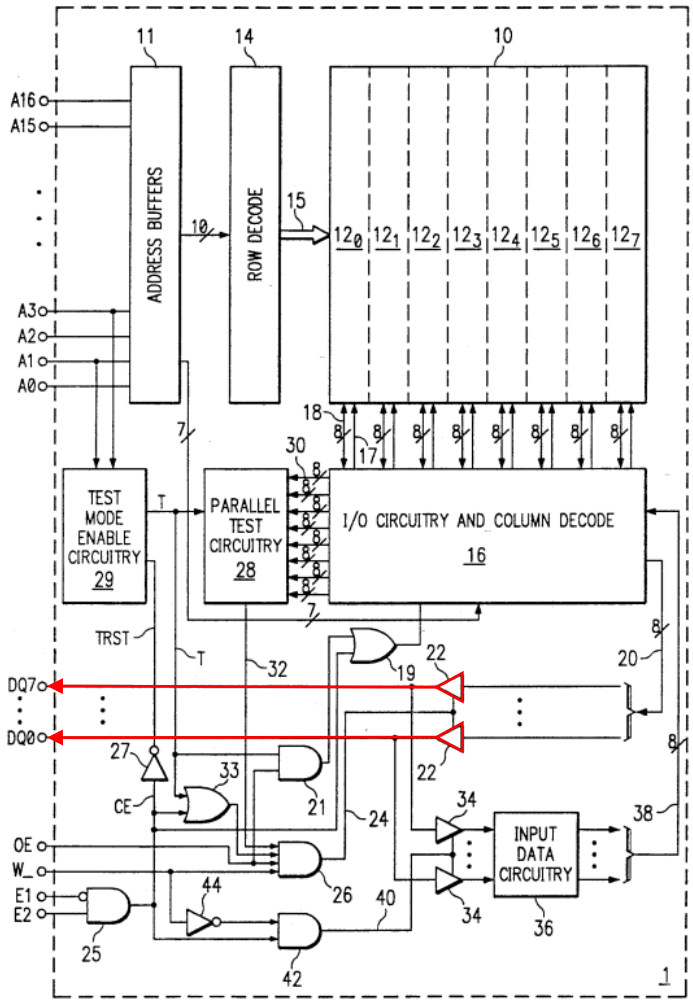
operation to output data to the bus via the DQ terminals, when the terminals are in a low-impedance state that conveys test information. Thus, Slemmer teaches claim element [1.3].

B. Claim 2: "The electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested."

98. As explained above in Section X.A.2 for claim element [1.1], Slemmer teaches that the data I/O connections and address connections are connected to signal lines and that one or more of the signal lines are "*a bus*." *See* Slemmer (EX1005), 35:22-42, 37:11-37.

99. Slemmer also teaches that the memory 1 includes output drivers that output data to the bus ("*circuit component to be tested includes output drivers for outputting data to said bus*"), as I explain below. Slemmer discloses that each line of an internal output data bus 20 of the memory is received by an output buffer 22 that drives a data output terminal (e.g., DQ0), as shown below.

FIG. 1

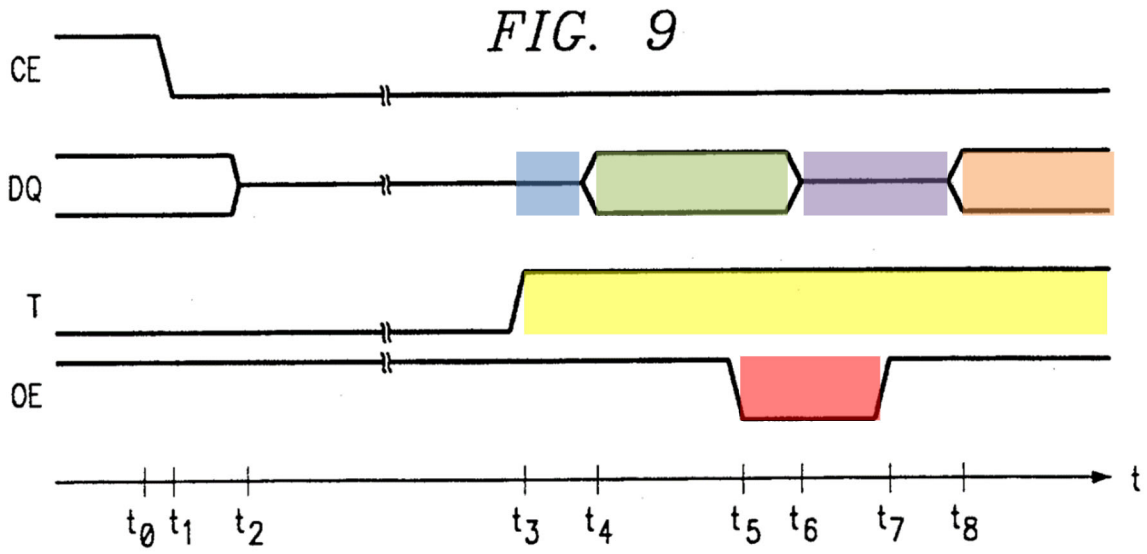


Slemmer (EX1005), at FIG. 1, 7:26-30 ("Each line of output data bus 20 is received by non-inverting output buffer 22, which drives the output terminal DQ with the correct data state, at levels and currents corresponding to the specifications of memory 1."). Based on Slemmer's disclosure, a POSITA would have understood that each data output terminal, such as DQ0, is connected to an external signal line that is connected between the multiple memories and the controller. *See supra* Section IX.A. A POSITA would also have understood that the external signal lines

enable the memory to send data, such as data read from the memory array 10 of the memory 1 via I/O circuitry and column decode 16, from the memory's data output terminals, such as DQ0 through DQ7. *See id.* Accordingly, a POSITA would have understood that the output buffers 22 in Slemmer are output drivers (of which any two or more are "*output drivers for outputting data to said bus*") because output buffers were also called output drivers (*see, e.g.* Fleming (EX1013), at 1:11-16), and because the output buffers in Slemmer are responsible for driving internal data (e.g., data from I/O circuitry and column decode 16) to an output (e.g., DQ0 and DQ1) to be provided external to the memory 1 (*see* Slemmer (EX1005), at FIG. 1 (above)).

100. Further, Slemmer teaches that the output buffers 22 are "*deactivated during testing of said circuit component to be tested*," as explained below. Slemmer explains "[e]ach of the output buffers 22 are enabled by a signal on line 24 from AND gate 26." Slemmer (EX1005), at 7:30-31. Specifically, the "signal on line 24 [] controls whether the logic level on output data bus 20 is presented at terminals DQ, or if output buffers 22 present a high-impedance state to terminals DQ." *Id.* at 7:31-34. Based on Slemmer's teachings, a POSITA would have understood that the output buffers 22 are not active, or are deactivated, when they present a high-impedance state at the terminals (*see, e.g.*, '473 Patent (EX1001), at 5:46-49, 6:52-53), because they do not output data to the terminal that is connected to the bus. *See id.*; Fleming (EX1013), at 1:11-16; *see also* Slemmer (EX1005), at

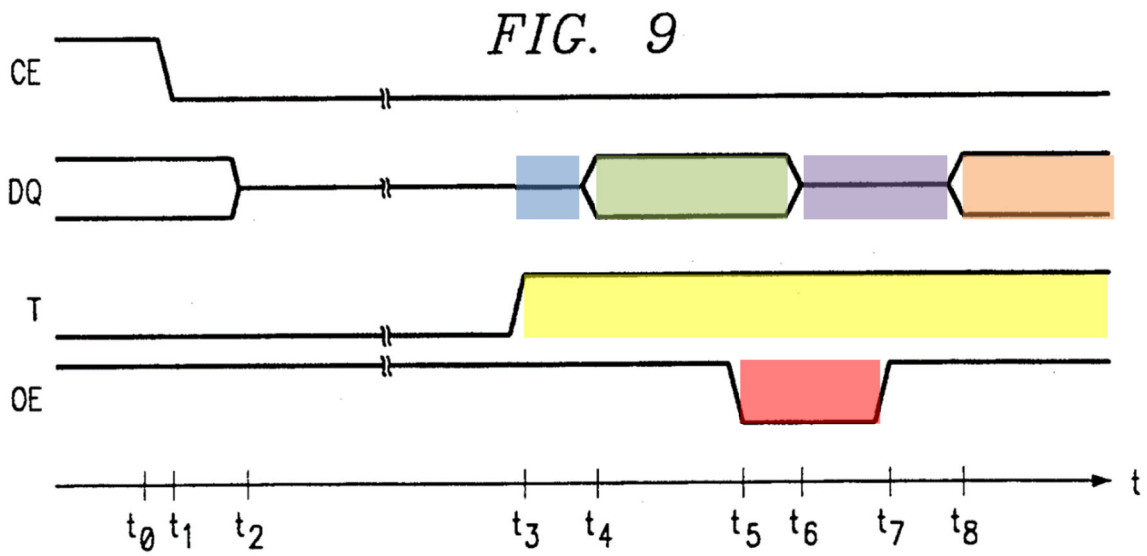
36:27-35, Fig. 9 (reproduced below with annotations as I discussed in Section X.A.4 for claim element [1.3]).



101. Although Figure 9 of Slemmer does not illustrate the chip enable (CE) or output enable (OE) logic for certain output buffers 22 that are not enabled during testing to provide the acknowledgement of test mode entry (*see* Slemmer (EX1005), at 36:49-54, 36:45-49), a POSITA would have understood that one or more output drivers in Slemmer would be activated, or enabled, to acknowledge the test mode entry (*see id.* at 36:49-54), while the remaining output drivers would remain deactivated, or not enabled, during testing. *See id.* at 36:22-54, FIG. 9. Slemmer explains that "not all of the output buffers . . . need be controlled" to acknowledge the test mode entry, as it "can be adequately communicated by a selected one of terminals DQ presenting a low impedance state." *Id.* at 36:49-54. Slemmer also explains that when memory 1 is selected for testing and not enabled

for normal operation, the "terminals DQ are expected to remain in a high impedance state." *Id.* at 36:31-36; *see also id.*, 36:10-21. Based on Slemmer's teachings, a POSITA would have understood that one of the terminals, such as DQ0 would be in a low-impedance state, with the corresponding output buffer 22 activated, to acknowledge the test mode entry, and that the remaining terminals, such as DQ1 to DQ7, would be in a high-impedance state, with the corresponding output buffers 22 deactivated. Thus, the remaining, deactivated output buffers in Slemmer teach the "*output drivers being deactivated during testing of said circuit component to be tested*."

102. Additionally and alternatively, a POSITA would have understood that, even for the output buffer(s) in Slemmer that are activated at certain times during testing to acknowledge the test mode, they are deactivated at other times during testing. As explained above for claim element [1.3], the buffer(s) 22 for the DQ terminal(s) that are in a low-impedance state, with the buffers 22 activated, at certain times during testing, are also in a high-impedance state, with the buffers 22 deactivated, at other times during testing. *See supra* Section X.A.4; *see* Slemmer (EX1005), at 36:10-54 (times t1 to t4), 37:27-39 (times t5 to t8), FIG. 9 (below).

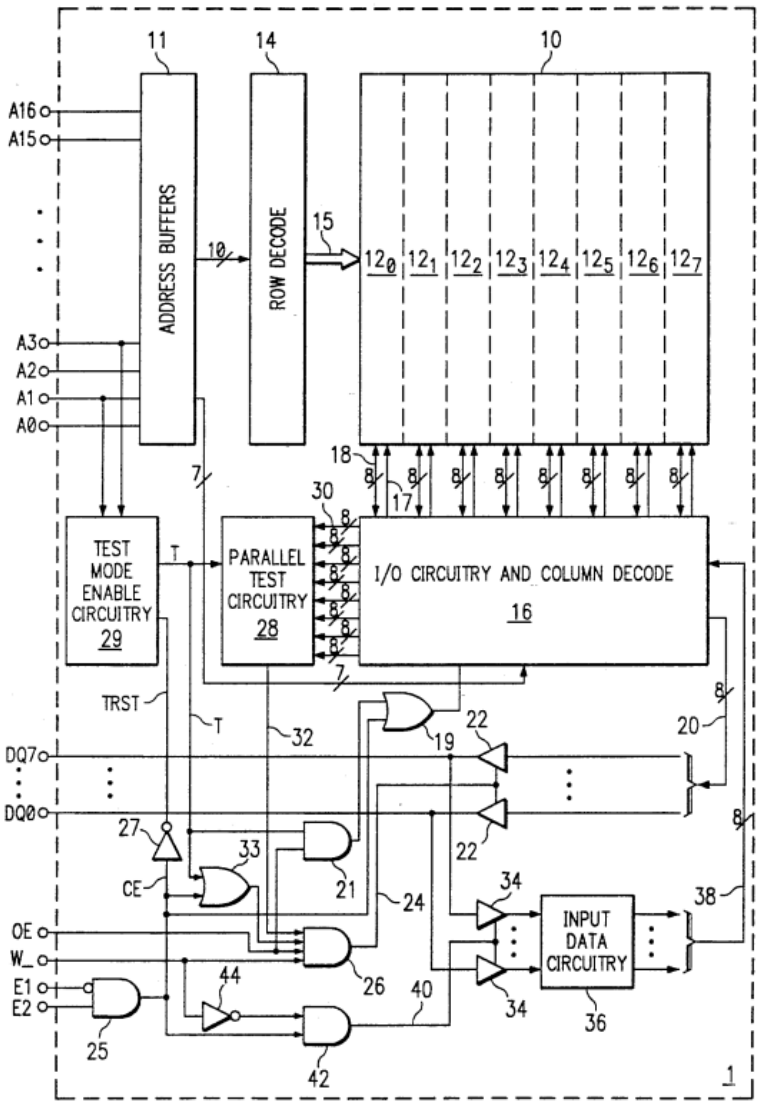


As shown by the yellow annotation to Figure 9, the test mode (T) is enabled at time t_3 and the DQ terminal, as shown in blue, is initially in a high-impedance state until time t_4. *See id.* at 36:10-54, FIG. 9. Between times t_4 and t_6, annotated in green, the DQ terminal is in a low-impedance state, which indicates that the output buffer is activated. *See id.* at 36:10-54, 37:27-39. However, at time t_5, the output enable (OE) terminal is externally driven low, annotated in red, which results in the DQ terminal transitioning back to a high-impedance state at time t_6, as annotated in purple above. *See id.* at 37:27-32, FIG. 9. At time t_7, the OE terminal is driven back to a high logical level, which results in the DQ terminal transitioning again to a low-impedance state at time t_8, as annotated in orange, which indicates that the output buffer is activated again. *See id.* at 37:33-37, FIG. 9. Thus, these one or more buffer(s) 22 in Slemmer that provide an acknowledgement of test information, such as entry into a test mode and an identification of which test mode

has been enabled, are deactivated at certain times during testing, such as between t_6 and t_8 in Figure 9 of Slemmer.

103. In addition to the deactivation of a buffer, which causes the DQ terminal to transition to a high-impedance state, when the OE terminal is low, Slemmer discloses that when there is an error during testing, such as "when the multiple data words compared do not present the same data," the parallel test circuitry 28 outputs a low logic level signal on signal line 32. *See id.* at 8:37-42. As shown in Figure 1 of Slemmer, signal line 32 is input to AND-gate 26, which outputs a signal on line 24 to enable (or activate) the output buffers 22 when the signal is logic high. *See id.* at FIG. 1, 7:26-24, 8:20-23; *see also id.* at 8:23-37.

FIG. 1



Thus, a POSITA would have understood that one or more buffers, such as those that are activated at certain times during test to acknowledge test mode entry or a successful test, are also deactivated (in a high-impedance state) at other times during testing. Thus, the one or more buffers deactivated at times during testing also teach the "*output drivers being deactivated during testing of said circuit component to be tested*."

C. Claim 3: "The electrical circuit according to claim 2, wherein said output drivers are deactivated by a test unit which is testing said circuit component to be tested."

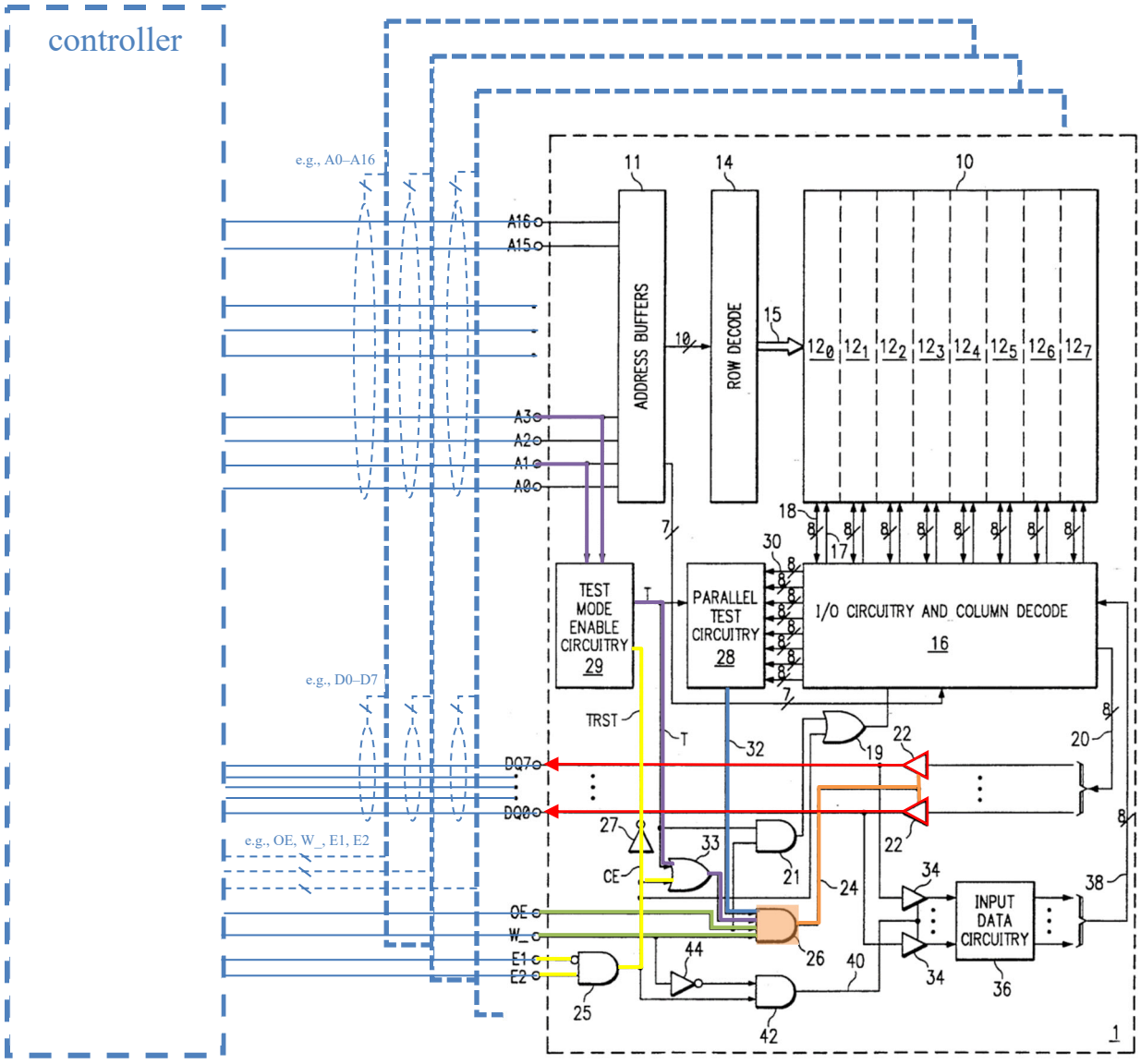
104. As explained above for claim 2, Slemmer teaches the memory 1 includes multiple output buffers 22 ("*output drivers*") that are deactivated during testing of the memory 1. *See supra* Section X.B; Slemmer (EX1005), at 36:22-54, FIGS. 1, 9.

105. As I explain below, Slemmer also teaches that the output drivers are deactivated by an external controller, test mode enable circuit (TMEC) 29, and/or parallel test circuitry (PTC) 28, any combination of which is "*a test unit*" that is testing the memory 1 ("*which is testing said circuit component to be tested*"). As an initial matter, the test unit disclosed in the '473 Patent can be part of the circuit component to be tested and the test unit (TE) is illustrated as part of the circuit component to be tested (SK1) in each of the figures. *See* '473 Patent (EX1001), at 5:11-18, FIGS. 1-3.

106. Slemmer teaches that the externally driven inputs from the controller to the memory 1 configure the memory for testing, which results in the deactivation of the output drivers. *See, e.g.*, *id.* at 9:19-30, FIG. 1. Slemmer also teaches that the inputs from the controller are provided to test mode enable circuit (TMEC) 29, which controls entry into and exit from testing. *See, e.g.*, *id.* at 8:32-

47, 9:19-30, 18:46-57, 36:10-16, 36:27-41. In addition, Slemmer teaches that the TMEC 29 uses PTC 28 to determine results during testing, such as whether or not there is an error, and to control the output of test information on one or more output driver(s), such as entry into a test mode and an identification of which test mode has been enabled. *See, e.g.*, *id.*

107. As shown in the annotated figure below for Slemmer's system, Slemmer discloses that the output of AND-gate 26 via signal line 24 (annotated in orange) controls whether the output buffers 22 (annotated in red) are activated to present output data with a low-impedance state (e.g., '0' or '1') or deactivated to present a high-impedance state at terminals DQ.



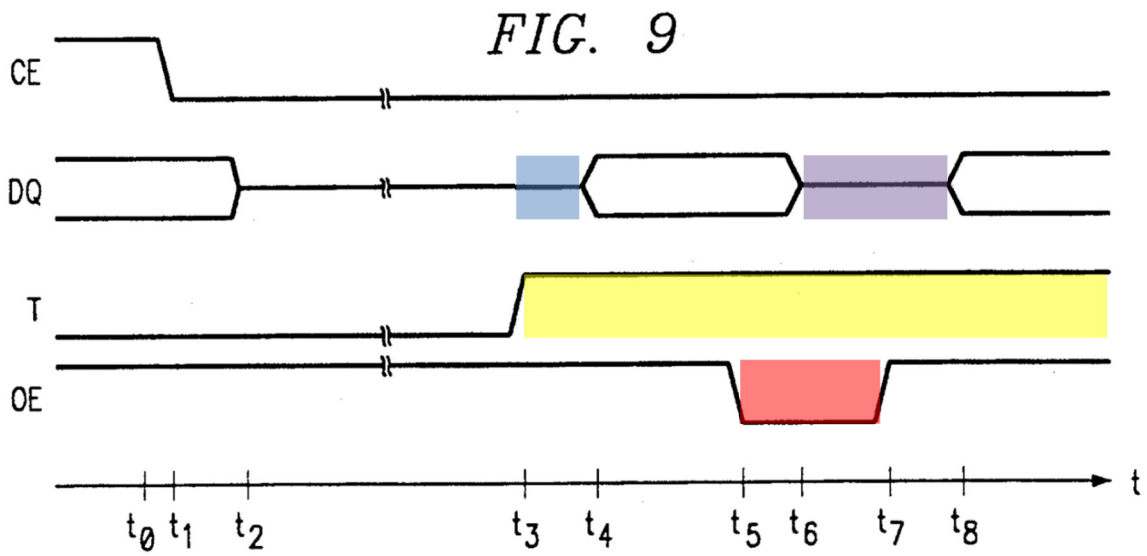
Id. at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above), 7:30-35, 34:54-57.

108. The output of AND-gate 26 is a function of its four inputs that are directly or indirectly provided by the controller, TMEC 29, or PTC 28. As shown by the annotations in green, the controller directly provides the write enable (W_) and output enable (OE) signals for two inputs to the AND-gate 26. *See id.* at FIG.

1, 8:4-14 (describing W_), 35:65-36:2 (same), 37:11-39 (describing OE). As shown by the annotations in yellow and purple, the controller indirectly provides a third input (in purple) to the AND-gate 26 by providing inputs at the chip enable terminals (E1 and E2) and inputs at the address terminals (such as A1 and A3), which are used to generate the test mode signal (T). *See id.* at FIG. 1, 9:19-30 (generating test (T) signal based on external inputs A1, A3, E1, E2), 18:46-57 (same), 36:10-16 (describing E1/E2). Specifically, the controller provides signals on the A1 and A3 terminals (annotated in purple in the figure above) to enable testing and on the E1 and E2 terminals (annotated in yellow) to disable normal operation of the memory device for testing. *See id.* at FIG. 1, 9:19-30, 18:46-57, 36:10-16.

109. The third input to the AND-gate (annotated in purple in the figure above) is also provided indirectly by TMEC 29, which generates a signal (T) when testing is enabled via the A1 and A3 terminals. *Id.* at FIG. 1, 9:19-30. Finally, the PTC 28 provides the fourth input (annotated in blue in the figure above) via signal line 32 to signal test information. *Id.* at FIG. 1, 8:32-47, 36:27-41. Accordingly, a POSITA would have understood that any one of or a combination of the controller, TMEC 29, and/or PTC 28 are "*a test unit which is testing said circuit component to be tested*."

110. As I explain below, a POSITA would also have understood that any one of or a combination of the controller, TMEC 29, and/or PTC 28 deactivate the output drivers during testing. As explained above for claim 2, a POSITA would have understood that one or more output drivers in Slemmer would be deactivated at certain times during testing to acknowledge the test mode, while the remaining output drivers would remain deactivated throughout testing. Slemmer (EX1005), at 36:10-54, FIG. 9; *see supra* Section X.B. A POSITA would also have understood that the controller deactivates the one or more output drivers when the write (W_) and/or output enable (OE) inputs are driven low. Slemmer (EX1005), at 8:4-14, 35:65-36:2, 37:11-39. For example, Slemmer teaches that the OE signal is used as a chip select during testing to activate or deactivate output driver(s) to provide test information, such as an acknowledgement of the test mode. *Id.* at 7:68-8:3, 8:14-19, 8:55-58, 36:55-68, 37:11-39. As shown in the figure below, the OE terminal is driven low at time t_5 (shown in red), which results in the output driver being deactivated at time t_6 with a high-impedance state at the DQ terminal (shown in purple).



Id. at FIG. 9 (annotated above), 36:10-54, 37:27-39. Based on Slemmer's teachings, a POSITA would have understood that the output driver(s) deactivated at certain times during testing are deactivated externally by the controller.

111. In addition, a POSITA would have understood that the output drivers that remain deactivated throughout testing are also deactivated by the controller. Specifically, the controller deactivates the output drivers when the chip enable (CE) signal is low by driving specific values on the E1 and E2 inputs during testing. *Id.* at 36:2-16, FIGS. 1, 9. As shown in Figure 9 above, the CE signal goes low at time t_1 and in response the output driver is deactivated at time t_2. As Slemmer explains, "[t]he disabling of output buffers 22, and the resultant high impedance state at terminals DQ, in response to deselection of memory 1 is conventional in memories and other integrated circuits having chip enable functions and terminals." *Id.* at 36:17-21; *see also id.* at 36:34-36 ("terminals DQ

are expected to remain in a high impedance state when the circuit is not enabled"), 36:10-17, 36:36-40.

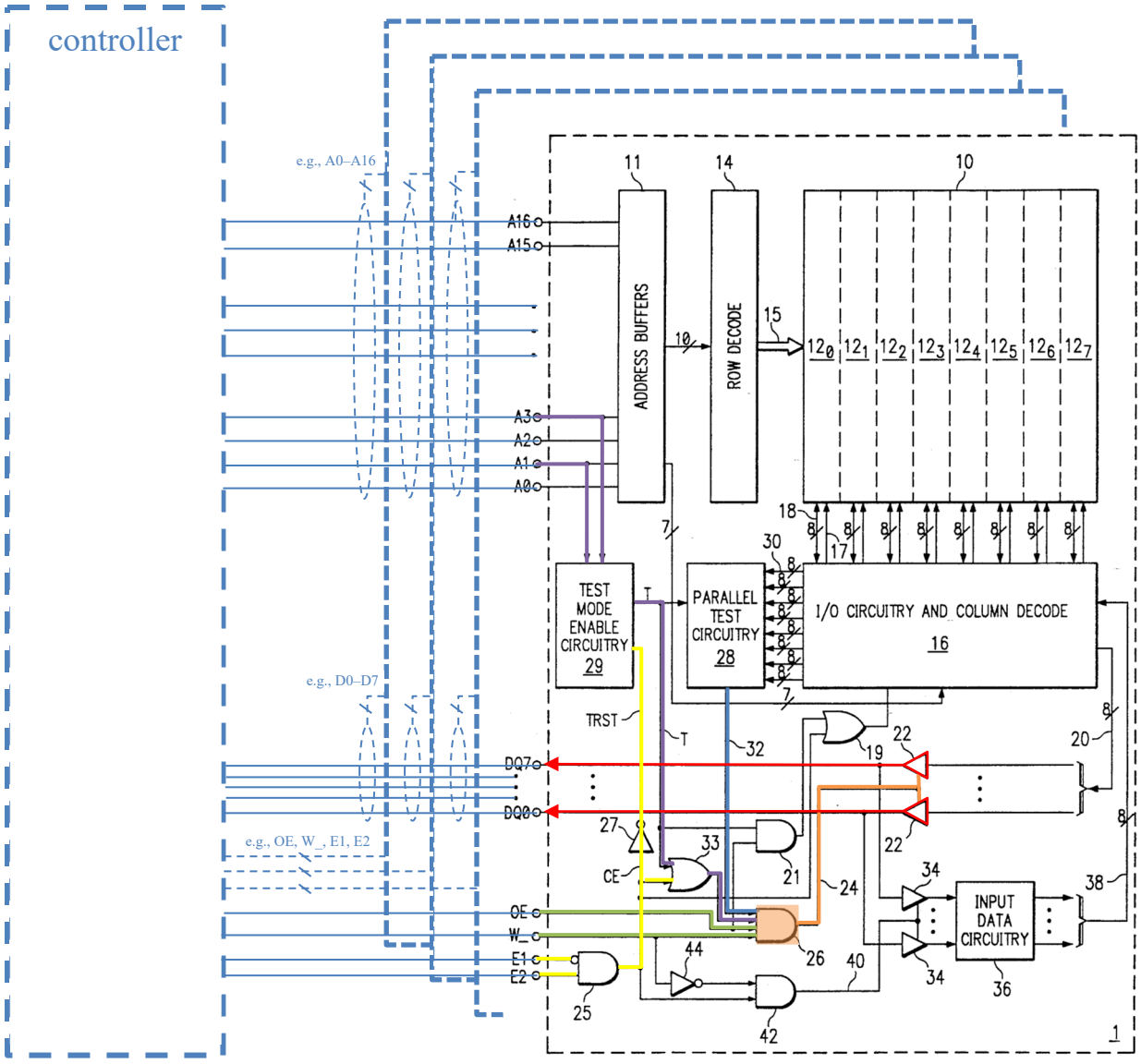
112. Further, Slemmer teaches that the PTC 28 deactivates the output drivers during testing when the test result indicates an error. *Id.* at 7:30-35, 8:20-42, FIG. 1. Slemmer discloses that signal line 32 from PTC 28 is driven to a "low logic level in test mode when there is an error." *Id.* at 8:37-42. A POSITA would have understood that a low logic level on signal line 32 would result in the deactivation of the output buffer(s) 22, because signal line 32 is one of the four inputs to AND-gate 26 and because AND-gate 26 provides a signal on line 24 to control the output buffer(s). *See id.* at FIG. 1, 7:30-35, 8:20-23.

113. Thus, the output drivers in Slemmer are "*deactivated by*" any one of or a combination of the controller, TMEC 28, and/or PTC 29 ("*a test unit*").

D. Claim 4

1. Claim Element [4.1]: "The electrical circuit according to claim 3, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring:"

114. As shown in the figure below, the electrical block diagram in Slemmer includes logic (annotated in orange below) that provides a signal on line 24 to activate or deactivate the output buffers 22.



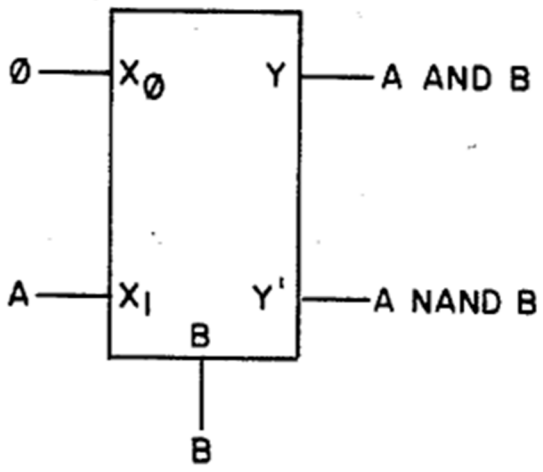
Slemmer (EX1005), at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above), 7:22-55, 8:47-55. The logic includes AND-gate 26, which receives four-inputs and provides an output on signal line 24. *Id.* Accordingly, a POSITA would have understood that this logic in Slemmer is "*a device selected from the group consisting of a logic unit and a selection circuit*" because it discloses an AND-gate 26 that is "*a logic unit*." A

POSITA would have recognized that an AND-gate performs a logical combination of the input signals into an output signal. More specifically, a POSITA would also have understood that the logic in Slemmer, including AND-gate 26, deactivates the output drivers because its output is provided as the control input to Slemmer's output buffers 22 that disables the buffers when the control input has a low logic level. *Id.* at FIG. 1, 7:26-34, 8:8-14. Slemmer's disclosure of an AND-gate whose output is used to deactivate the output buffers is a similar structure and function as disclosed in the '473 Patent, which discloses a logic unit that includes an AND gate whose output signal is supplied to the output driver. *See, e.g.*, '473 Patent (EX1001), at 6:4-9 ("In the example under consideration, this logic unit includes an AND gate AND which receives as input signals the data DOUT which need to be output to the bus "BUS" during normal operation of the circuit component SK1 and the test control signal TESTC, and whose output signal is supplied to the output driver T as input signal."), 7:60-65 ("In the example under consideration, this logic unit includes an AND gate AND which receives as input signals, the enable signal EN and the test control signal TESTC which is also provided in the electrical circuit shown in FIG. 2. The output signal of the AND gate AND is used to control the output drivers T."), FIGS 1-2.

115. Further, a POSITA would have recognized that the logic unit (e.g., AND gate) is a different structure than a multiplexer, according to the '473 Patent,

even though it was well-known in the art that multiplexers could be configured to perform logical combinations. For example, it was well-known to a POSITA that a multiplexer can be configured via its inputs to perform logical operations such as a logical OR and a logical AND. U.S. Patent No. 4,558,236 to Burrows discloses a universal logic circuit with a multiplexer configurable via its X0, X1, and B inputs to implement different logical functions, such as a logical OR and NOR function as shown in Figure 2A and a logical AND and NAND function as shown below in Figure 2B:

FIG. 2B



Burrows (EX1016), at Abstract, 2:7-18, 3:17-23, 3:24-4:38, FIGS, 1, 2A-2F.

116. Similarly, U.S. Patent No. 4,910,417 to Gamal discloses a programmable design in which a multiplexer, as shown in Figure 2B (reproduced below), is programmed using the A, B, and S inputs to implement different logical functions, such as a logical NAND and AND function and a logical NOR and OR function as shown in Figure 2C (also reproduced below).

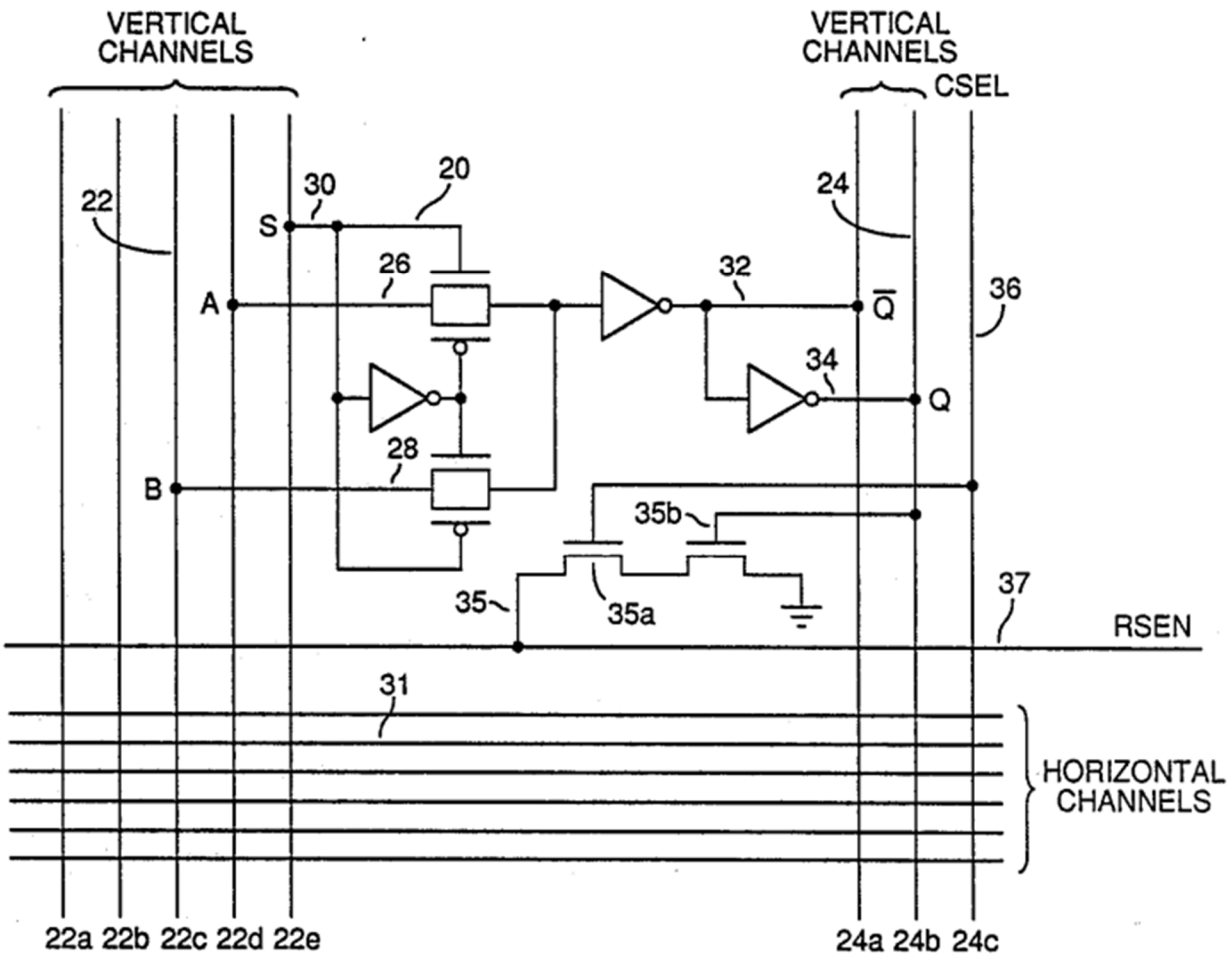

VERTICAL CHANNELS
VERTICAL CHANNELS
CSEL
22
30
20
24
S
26
32
36
A
Q
34
Q
28
B
35b
35
35a
37
RSEN
31
HORIZONTAL CHANNELS
22a 22b 22c 22d 22e
24a 24b 24c

FIGURE 2B

LOGIC FUNCTIONS TO BE REALIZED	UNIVERSAL MODULE				
	INPUT CONNECTIONS			OUTPUTS	
	S	A	B	$\overline{Q}$	Q
NAND / AND	X	Y	'0'	$\overline{X \cdot Y}$	$X \cdot Y$
NOR / OR	X	'1'	Y	$\overline{X+Y}$	$X+Y$
XNOR / XOR	X	$\overline{Y}$	Y	$X \cdot Y + \overline{X} \cdot \overline{Y}$	$X \cdot \overline{Y} + X \cdot \overline{Y}$
SR / LATCH	$\overline{Q}$	S	$\overline{R}$	$\overline{Q}$	Q
D / LATCH	L	D	Q	$\overline{Q}$	Q

FIGURE 2C

Gamal (EX1017), at Title, 6:64-7:17, FIGS. 2B-2C.

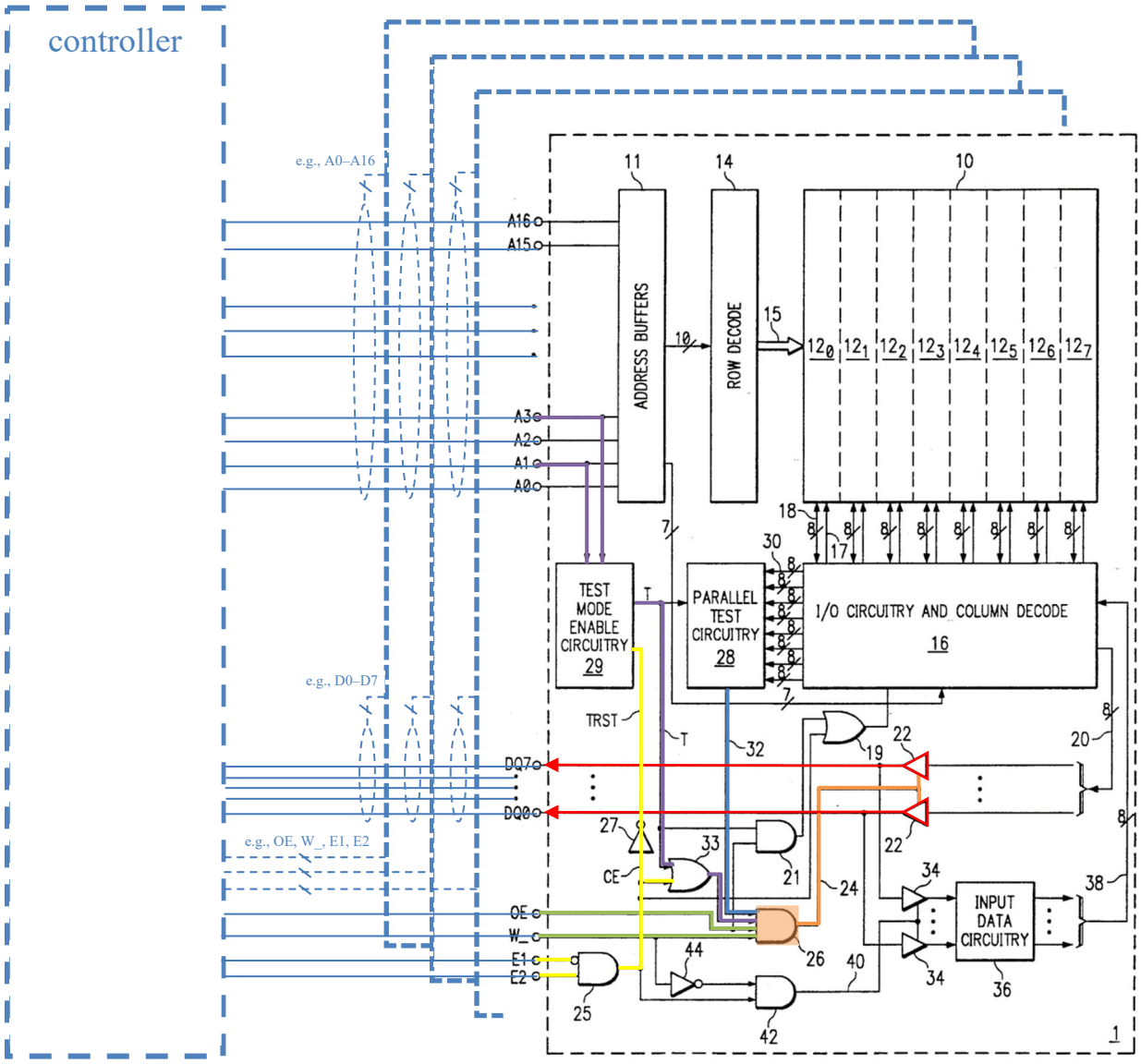
117. Thus, Slemmer also teaches a logic unit ("*said device*") for deactivating output buffers ("*for deactivating said output drivers*").

2. Claim Element [4.2]: "that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device which controls said bus, and"

118. As explained above for claim element [4.1], the output drivers (output buffers 22) are controlled by the output from AND-gate 26 on line 24. *See supra* Section X.D.1. As I discuss below, Slemmer also teaches claim element [4.2].

119. As shown in the figure below, Slemmer teaches an external controller ("*bus control device*") that drives an output enable (OE) signal ("*an enable*

signal") to the memory ("*circuit component to be tested*") to control the output drivers via AND-gate 26.



Slemmer (EX1005), at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above). As shown by the annotation in green, the OE signal provides an inputs to AND-gate 26, which is annotated in orange. *Id.* During normal operation, the output enable (OE) signal enables and

disables the output from the memory. *Id.* at 8:4-19. Thus, Slemmer teaches that during normal operation its output buffers are controlled based on the OE signal which is supplied to the memory to be tested by the memory controller ("*that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device*").

120. Additionally and alternatively, Slemmer teaches that the "*enable signal*" is any combination of the output enable (OE), chip enable (E1, E2), and/or write enable (W_). As shown in the figure above, the external controller ("*bus control device*") supplies the OE signal, the chip enable (E1/E2) signals, and a write enable (W_) signal to terminals of memory 1 to control the output buffers 22 via AND-gate 26. *Id.* at FIG. 1. As shown by the annotations in green to the figure above, the output enable (OE) and write enable (W_) signals provide two inputs to AND-gate 26, which is annotated in orange. *Id.* During normal operation, the write enable (W_) signal has a high logic level for read operations and a low logic level for write operations, and the output enable signal enables and disables the output from the memory. *Id.* at 8:4-19. Further, as shown by the annotations in yellow to the figure above, the chip enable signals (E1/E2) control a third input to AND-gate 26 via AND-gate 25 and OR-gate 33. *Id.* at FIG. 1. During normal operations, when terminal E1 is logic low and terminal E2 is logic high, the CE signal that is

output from AND-gate 25 is logic high. *Id.* at FIG. 1, 7:35-51, 8:49-55. The CE signal is input to OR-gate 33, which outputs a logic high signal when the CE signal is logic high, and the output of OR-gate 33 is input as a third input to AND-gate 26, as shown by the annotation in purple in the figure above. *Id.* Thus, Slemmer teaches that during normal operation its output buffers are controlled based on any combination of the output enable (OE), chip enable (E1/E2), and/or write enable (W_) signals which is supplied to the memory to be tested by the memory controller ("*that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device*").

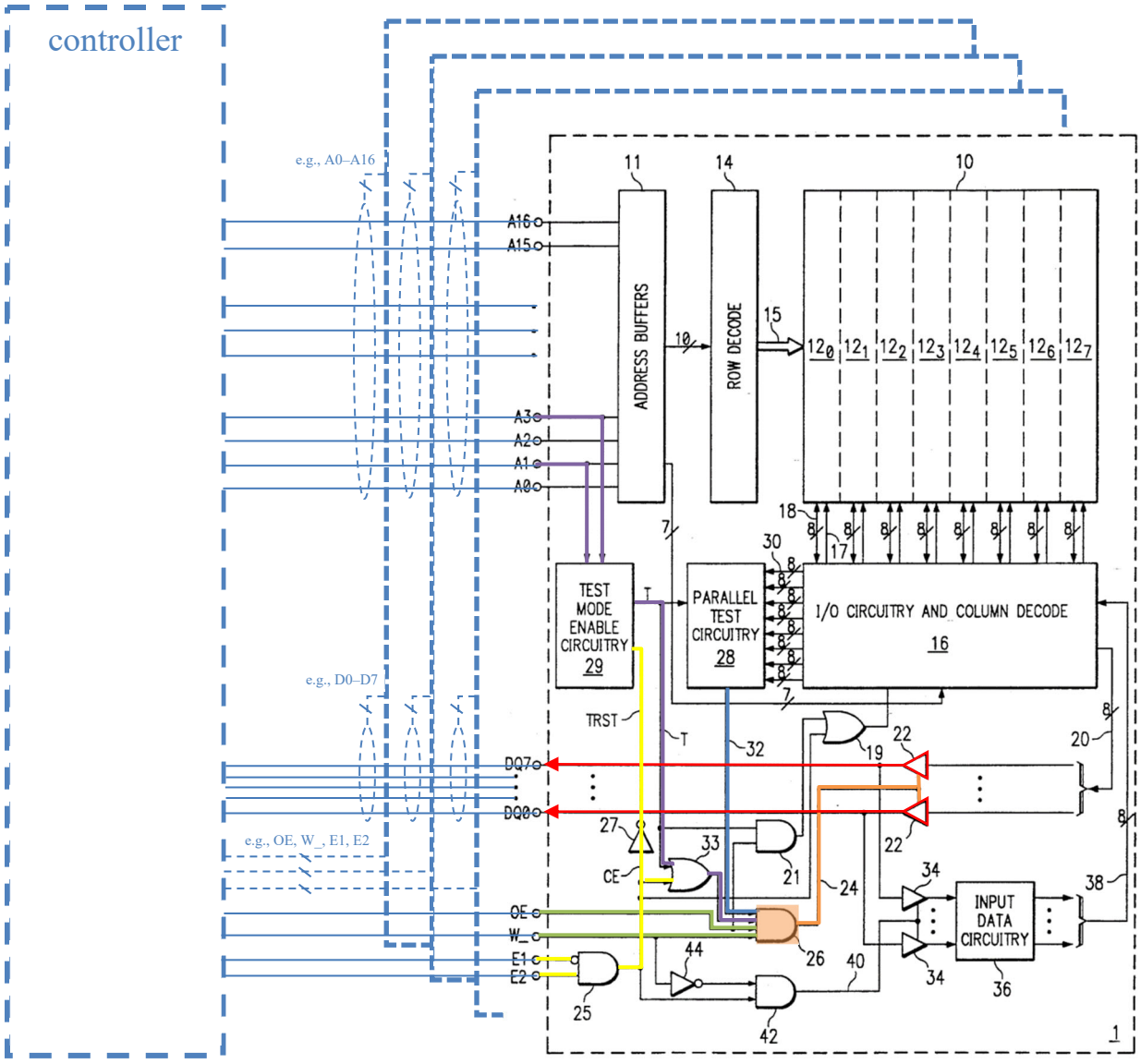
121. Further, a POSITA would have understood that Slemmer teaches a memory controller that is a bus control device "*which controls said bus*" because it outputs signals to control which memory device(s) connected to the bus are enabled or disabled for normal operation, which device(s) connected to the bus are configured for read or write operations, and which devices connected to the bus have their outputs enabled or disabled. *Id.* at FIG. 1, 7:35-51, 8:4-19, 8:49-55; *see also id.* at 36:55-64. For example, Slemmer teaches the chip enable signals, such as E1 and E2, control which memory devices connected to the bus are enabled or disabled for normal operation. *See id.* Slemmer also teaches that the write enable signals, such as W_, determines which memory devices connected to the bus are

configured for read or write operations. *See id.* And, Slemmer teaches that the output enable signals, such as OE, determines which memory devices connected to the bus have their outputs enabled or disabled. *See id.*

3. Claim Element [4.3]: "that during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested."

122. As I explained above for claim 3, Slemmer teaches that the output drivers are controlled, such as being deactivated or activated, by a test unit, which is any one of or a combination of an external controller, test mode enable circuitry (TMEC) 29, and/or parallel test circuitry (PTC) 28, via AND-gate 26. *See supra* Section X.C; Slemmer (EX1005), at 7:30-35, 7:68-8:47, 8:55-58, 9:19-30, 18:46-57, 35:65-36:58, 37:11-39, FIGS. 1, 9.

123. As shown in the figure below, the test mode enable circuitry (TMEC) 29 provides a test signal on line T, which is annotated in purple below, that is input to OR-gate 33, which provides its output, which is also annotated in purple below, as an input to AND-gate 26, which is annotated in orange.



Id. at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above). Slemmer explains that when testing is enabled TMEC 29 drives the test signal on line T to a high logic level. *Id.* at 8:47-49. The logic high test signal (T) causes the output of OR-gate 33 to go to high logic level, which is provided as an input to AND-gate 26. *See id.* at 8:49-55. Additionally, a logic high test signal (T) also causes parallel test circuitry (PTC) 28 to perform

operations and controls the enabling of input/output circuit and column decoder 16 via AND-gate 21 and OR-gate 19. *Id.* at 8:32-37, 7:56-68. Thus, Slemmer teaches that during testing of memory 1, the output buffers are controlled based upon a test signal on line T which the test mode enable circuitry (TMEC) 29 supplies to the memory ("*during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested*").

124. Additionally, as shown in the figure above, parallel test circuitry (PTC) 28 provides a signal on line 32, annotated in blue in the figure, that is directly input into AND-gate 26 to control whether the output buffers 22 are activated or deactivated. *See id.* at FIG. 1 (above). Slemmer explains that when there is an error during testing, PTC 28 drives line 32 to a logic low level, which would deactivate the output buffers. *See id.* at 8:38-42; *see also id.* at 8:32-37, 36:27-31, FIG. 9. Slemmer also explains that when there is no error during testing, PTC 28 drives line 32 to a logic high level, which enables the output buffers to be activated if the other inputs to AND-gate 26 are also logic high. *See id.* at 8:32-40. Thus, Slemmer teaches that during testing of memory 1, the output buffers are controlled based upon a signal on line 32 which the parallel test circuitry (PTC) 28 supplies to the memory ("*during testing of said circuit component to be tested, said*

output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested").

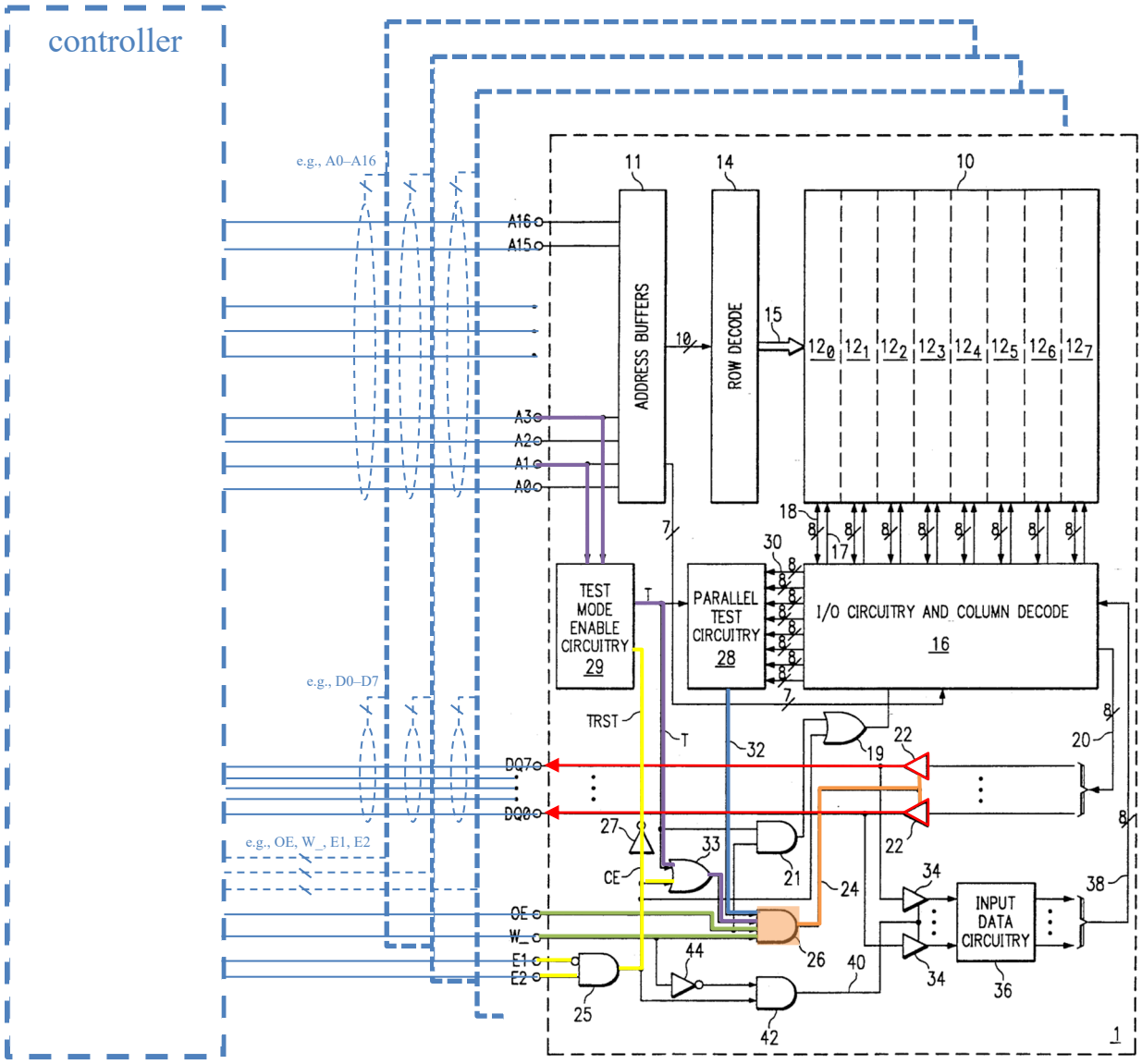
125. Thus, a POSITA would have understood the test signal on line T (output from TMEC 29) and the signal on line 32 (output from PTC 28) are individually and collectively a "*test control signal which the test unit supplies to said circuit component to be tested*."

E. Claim 5: "The electrical circuit according to claim 4, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the enable signal and a test control signal."

126. As an initial matter, claim 5 recites "a test control signal" but depends from claim 4, which also recites "a test control signal." *See* '473 Patent (EX1001), at 11:32-33 (claim 4), 11:38 (claim 5). It appears that claim 5 is referring to the "test control signal" introduced in claim 4.

127. As I explained above for claim element [4.1], the "*device*" in Slemmer is a "*logic unit*" that includes AND-gate 26. *See supra* Section X.D.1. And, as I explained above for claim elements [4.2] and [4.3], the "*enable signal*" in Slemmer is the output enable (OE) signal or alternatively any combination of the chip enable signals (E1/E2), write enable signal (W_), and OE signal, and the "*test control signal*" is individually and collectively the test mode signal on line T and the signal on line 32. *See supra* Sections X.D.2 and X.D.3. As I explain below, Slemmer also teaches claim 5.

128. As shown in the figure below, the AND-gate 26 (included in "*logic unit*") provides an output signal on line 24, which is annotated in orange, that results from a "*logical combination of the enable signal*" (E1/E2, W_, and/or OE) and "*a test control signal*" (signal on line T and/or signal on line 32).



Id. at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above), 7:22-55, 8:47-55. Slemmer explains that OR-

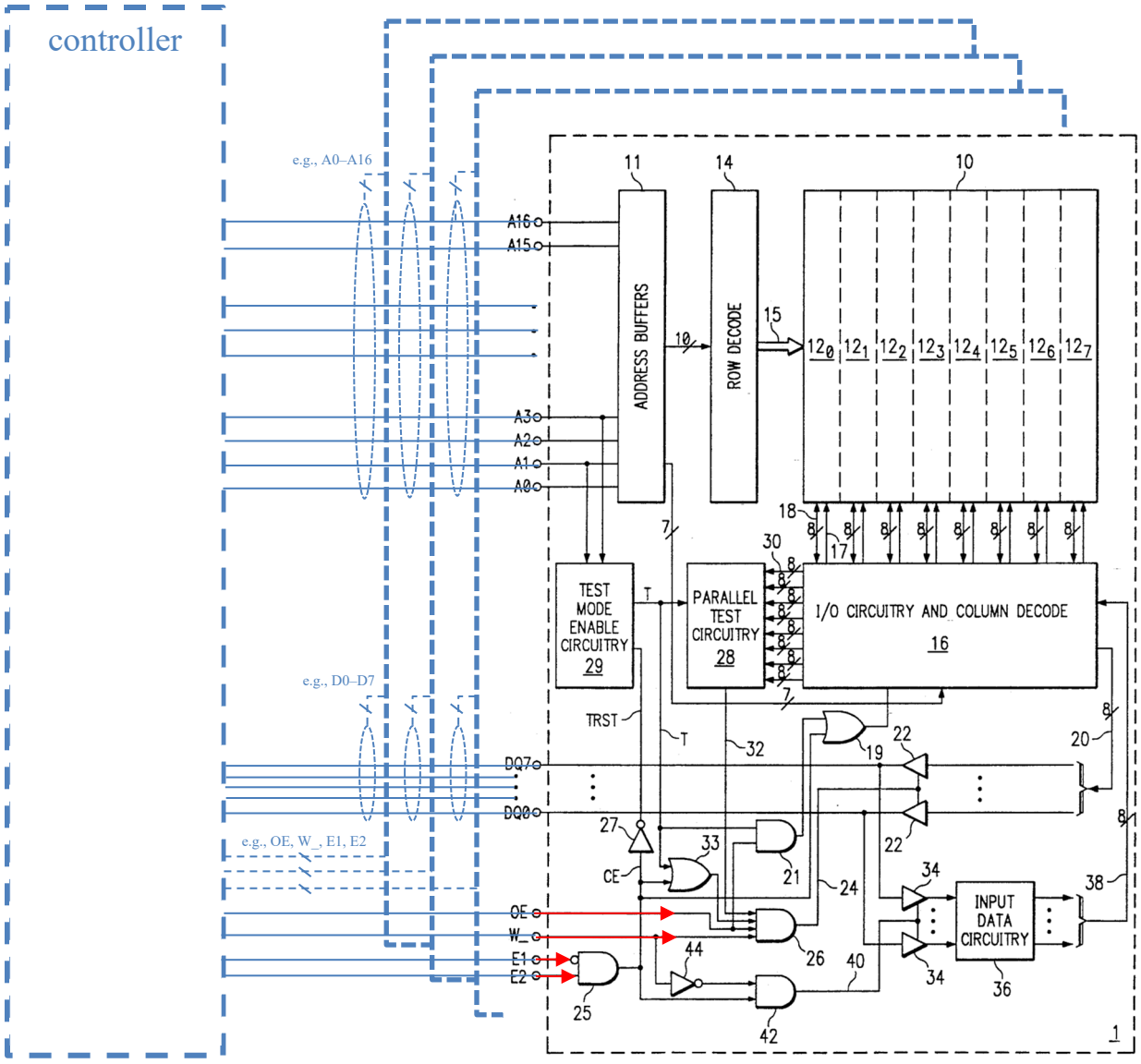
gate 33 receives one input, annotated in purple in the figure above, from the test mode signal on line T and another input, annotated in yellow in the figure above, from the chip enable (CE) signal, which is based on the chip enable inputs at the E1 and E2 terminals. *See id.* at FIG. 1, 36:10-16, 36:25-27. Slemmer also explains that the AND-gate 26 receives four inputs: the signal on line 32 (annotated in blue), the output from OR-gate 33, the signal from the OE input (in green), and the signal from the W_ input (also in green). *See id.* at FIG. 1, 7:35-8:46. Thus, Slemmer teaches that AND-gate 26 provides an output signal on line 24 resulting from a logical combination of the enable signal ((E1/E2, W_, and/or OE) and the test control signal (signal on line T and/or signal on line 32) ("*logic unit providing an output signal resulting from a logical combination of the enable signal and a test control signal*").

F. Claim 7: "The electrical circuit according to claim 1, comprising a bus control device for controlling said bus and for receiving a signal indicating testing of said circuit component to be tested."

129. As I explained above for claim element [1.1], Slemmer teaches that multiple memories are connected via their terminals to a controller, such as one in a system or test equipment. *See supra* Section X.A.2; *see, e.g.*, Slemmer (EX1005), at FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:4-5, 8:14-19, 8:59-67, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 36:55-68,

37:11-24, 37:27-29, 37:33-37; *see e.g.*, EX1011, 18:9-13, 18:51-54, 26:8-12, FIG. 24; EX1012, FIG. 1, 1:16-21, 1:49-52.

130. Slemmer also teaches that the controller externally drives input signals that are received at the terminals of a memory 1. *Id.* As shown in the figure below, several terminals of memory 1 in Slemmer receive external input signals, including signals at the output enable (OE) terminal, write enable (W_) terminal, and chip enable terminals (E1, E2).

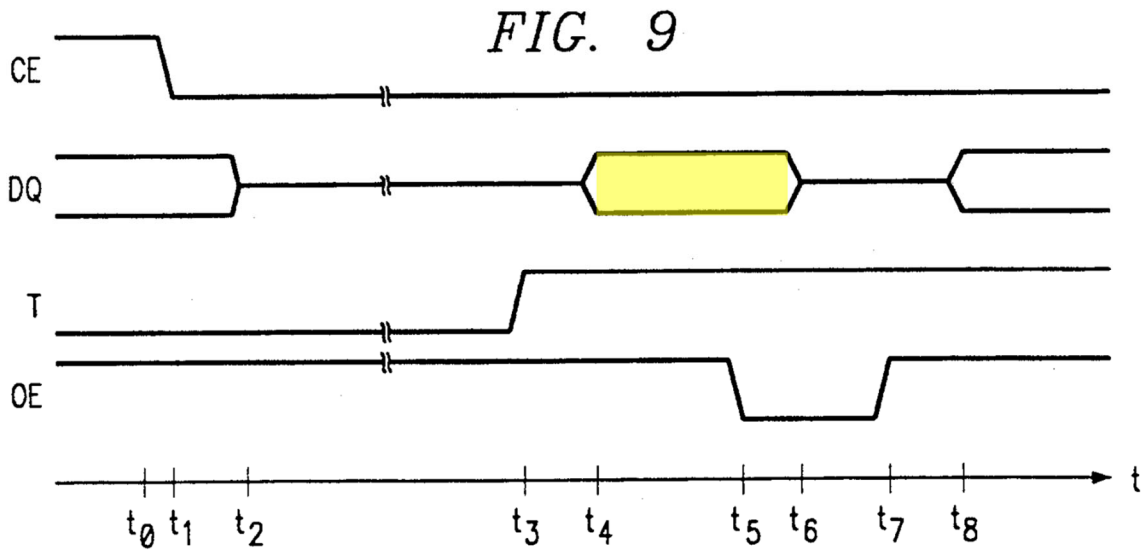


Id. at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above). Further, the address terminals, such as A0 through A16, and the data terminals, such as DQ0 through DQ7, of the multiple memories are connected together and to the controller. *Id.*

131. Based on Slemmer's teachings, a POSITA would have understood that the external signals input to memory 1, such as OE, W_, and/or E1/E2, that are

driven by the controller serve to control the bus between the memory devices ("*a bus control device for controlling said bus*"). Slemmer explains that the output enable (OE) terminal is "externally driv[en]" to "control the enabling and disabling of output buffers 22" and serve "as a chip enable terminal during a test mode." *Id.* at 37:11-15, 37:27-29. According to Slemmer, this function "is especially useful if a [test mode] is to be enabled when multiple memories 1 are connected in parallel and only one . . . of memories 1 is to be tested." *Id.*, 37:15-19. Slemmer also explains that a high logic level at the write enable (W_) terminal indicates a read operation and that a low logic level at the terminal indicates a write operation, which places "output buffers 22 in the high impedance state at their output." *Id.*, 8:4-14. Further, Slemmer explains that the "normal operating modes [are] entered, upon selection of memory 1 by the chip enable inputs E1 and E2" (*id.*, 10:10-12) and that the "test modes may be enabled only when memory 1 is not enabled from chip enable terminals E1 and E2, i.e., when line CE at the output of AND gate 25 is at a low logic level" (*id.*, 36:3-6). Accordingly, Slemmer teaches that the OE, W_, and/or E1/E2 terminals are externally driven by the controller to control the bus via, for example, enabling or disabling the memory and controlling whether the memory's output drivers are placed in a high-impedance state or output data ("*a bus control device for controlling said bus*").

132. As I explain below, Slemmer also teaches that the controller receives "*a signal indicating testing of said circuit component to be tested*." As I explained above for claim element [1.3], Slemmer teaches that the memory 1 communicates test information, such as an acknowledgement of entry into a test mode and identification of which test mode has been enabled, via one or more DQ terminals, which is highlighted in yellow in Figure 9 of Slemmer below. *See supra* Section X.A.4; EX1005 (Slemmer), at 36:10-54, FIG. 9 (below).



Slemmer explains that "not all of the output buffers . . . need be controlled" to acknowledge the test mode entry, as it "can be adequately communicated by a selected one of terminals DQ presenting a low impedance state." *Id.*, 36:49-54. Slemmer also explains that, if desired, additional information is output at terminals DQ, such as an "identification of which test mode has been enabled." *Id.*, 36:45-49. For example, Slemmer explains that the memory can support multiple testing

modes (*id.*, 9:55-64), which are selected by a sequence of selection codes, such as "01011" (*id.*, 27:6-15, 4:53-56, 5:3-14). Based on Slemmer's teachings, a POSITA would have understood that the controller would receive such test information, which indicates testing of the circuit component by, for example, acknowledging entry into a test mode or identifying which test mode has been enabled, on one or more DQ signal lines connected between the controller and the memory being tested ("*a bus control device … for receiving a signal indicating testing of said circuit component to be tested*"). *See, e.g.*, *id.*, 8:14-19, 35:22-30, 36:55-64.

G. Claim 9: "The electrical circuit according to claim 1, wherein the operation performed by said circuit component to be tested, during the testing thereof, is outputting data to said bus that is other than the data which would be output to said bus during normal operation, and the data outputted to said bus is data selected from the group consisting of infrequently changing data and non-changing data."

133. To the extent this claim has objective boundaries, it is taught by Slemmer, as I explain below. The '473 Patent does not expressly state what data would be output to the "bus that is other than the data which would be output … during normal operation" and what is "infrequently changing data." *See, e.g.*, EX1001, 3:32-38, 5:58-6:49; *see supra* Section X.A.4 (claim element [1.3]). Patent Owner has interpreted both claim elements as data on the "DQ Feedback" line, as shown below:

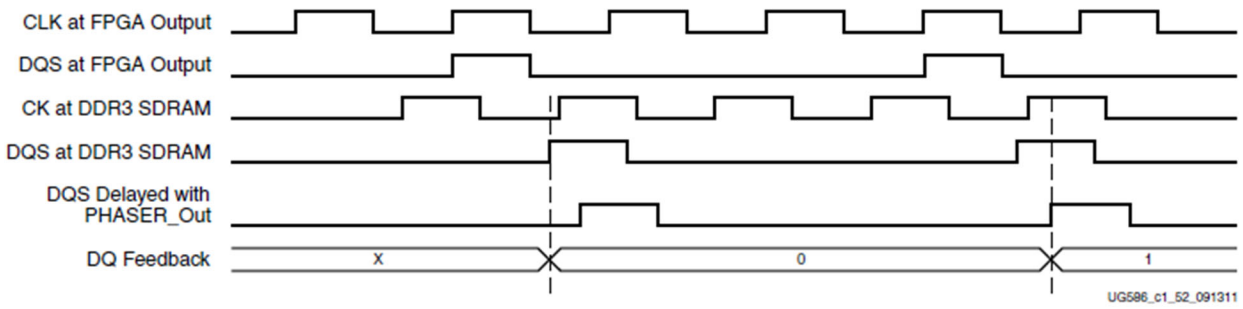
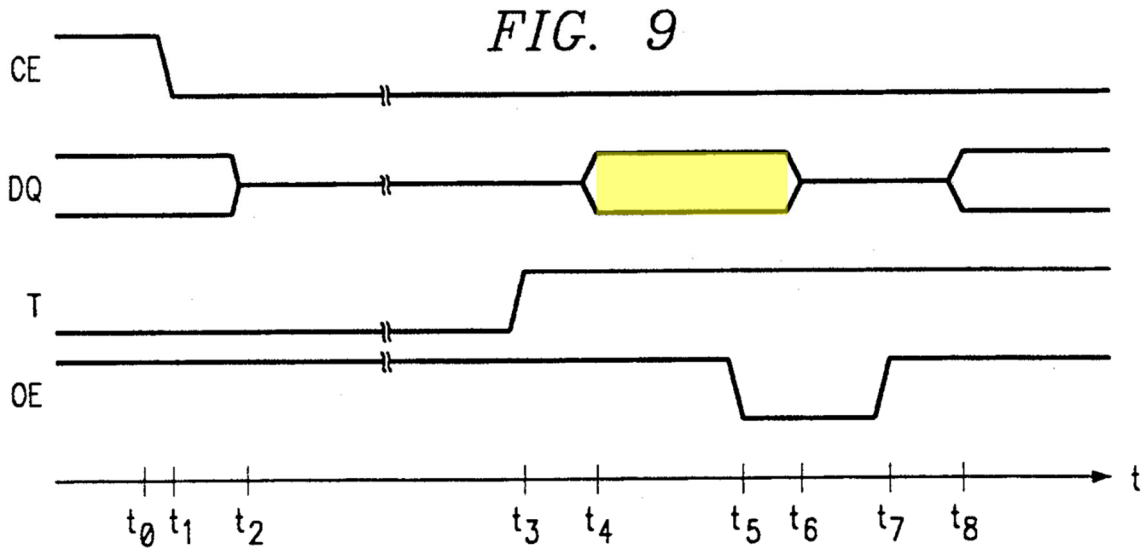


Figure 1-63: **Write Leveling Timing Diagram**

Xilinx Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solution v3.0 User Guide (EX1015), at 23 (FIG. 1-63) (cited by EX1014, at 17). Specifically, the "DQ Feedback" has a don't care value ('X'), transitions to a '0' value, and then transitions to a '1' value. *Id.*

134. Under Patent Owner's interpretation, Slemmer also teaches "*the operation performed by said circuit component to be tested, during the testing thereof, is outputting data to said bus that is other than the data which would be output to said bus during normal operation, and the data outputted to said bus is … infrequently changing data*." In particular, Slemmer teaches that one or more data terminals (DQ0-DQ7) outputs test information, such as an acknowledgement of the test mode entry, using an active state (in a low-impedance condition) (highlighted in yellow in the figure below) with either a '0' or '1' state. *See* Slemmer (EX1005), at FIG. 9, 35:65-67, 36:41-45, 36:45-54. As explained above for claim element [1.3], the test information provided during Slemmer's active state is different than the data which would be output during normal operation, because normal operation is a different operation mode and because the terminals

have a different function in normal operation than during testing. *See supra* Section X.A.4; *see also* Slemmer (EX1005), at 1:60-67, 37:40-51. As shown in the figure below, the DQ terminal transitions from an inactive state (high-impedance condition) to an active state (low-impedance condition) at time t_4 and back to an inactive state (high-impedance condition) at time t_6.



Slemmer (EX1005), at FIG. 9, 36:22-54. This behavior is similar to the "DQ Feedback" line, as accused by Patent Owner, that transitions from a don't care value to a '0' value and then from a '0' value to a '1' value. *See* Xilinx Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solution v3.0 User Guide (EX1015), at 23 (FIG. 1-63) (cited by EX1014, at 17). Accordingly, Slemmer teaches claim 9 under Patent Owner's claim interpretation.

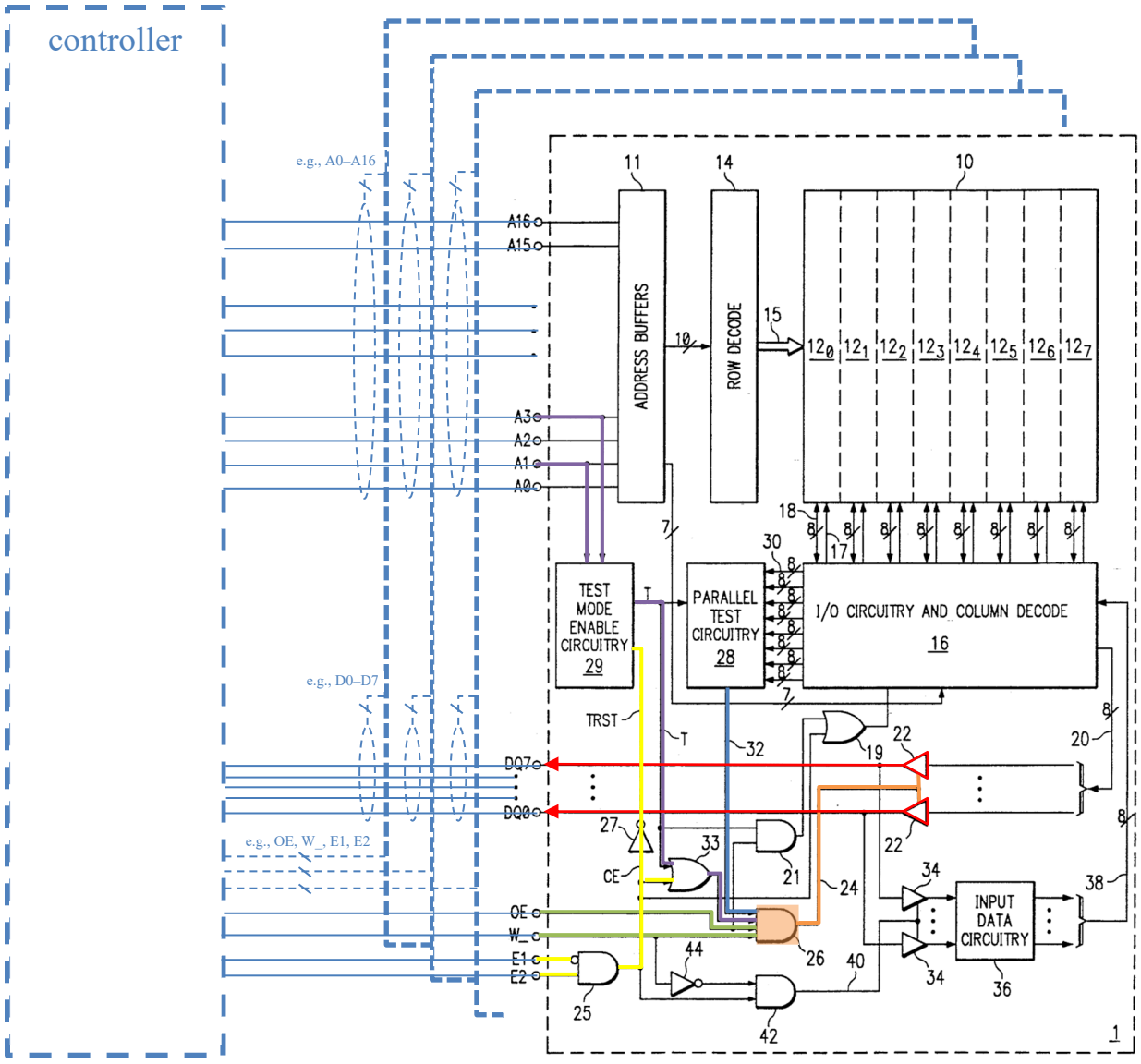
135. Alternatively, Slemmer teaches that the data output to the bus is "*non-changing data*." As shown in the figure above, the DQ terminal remains

active between time t_4 and time t_6. *Id.* at FIG. 9 (reproduced above). Slemmer teaches that the data state (e.g., '0' or '1') presented at terminal(s) DQ is unimportant because the entry into test mode is communicated by a low impedance condition on one of the terminals DQ. *Id.* at 36:41-45, 36:49-54. Accordingly, Slemmer teaches that the logic state of the data that represents entry into testing does not change during testing, such as between time t_4 and time t_6 in Figure 9 of Slemmer.

H. Claim 10

1. Claim Element [10.1]: "The electrical circuit according to claim 9, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device ensuring:"

136. As explained for claim element [4.1], Slemmer teaches that the electrical circuit includes logic, including AND-gate 26, which is "*a device*" that is "*a logic unit*."

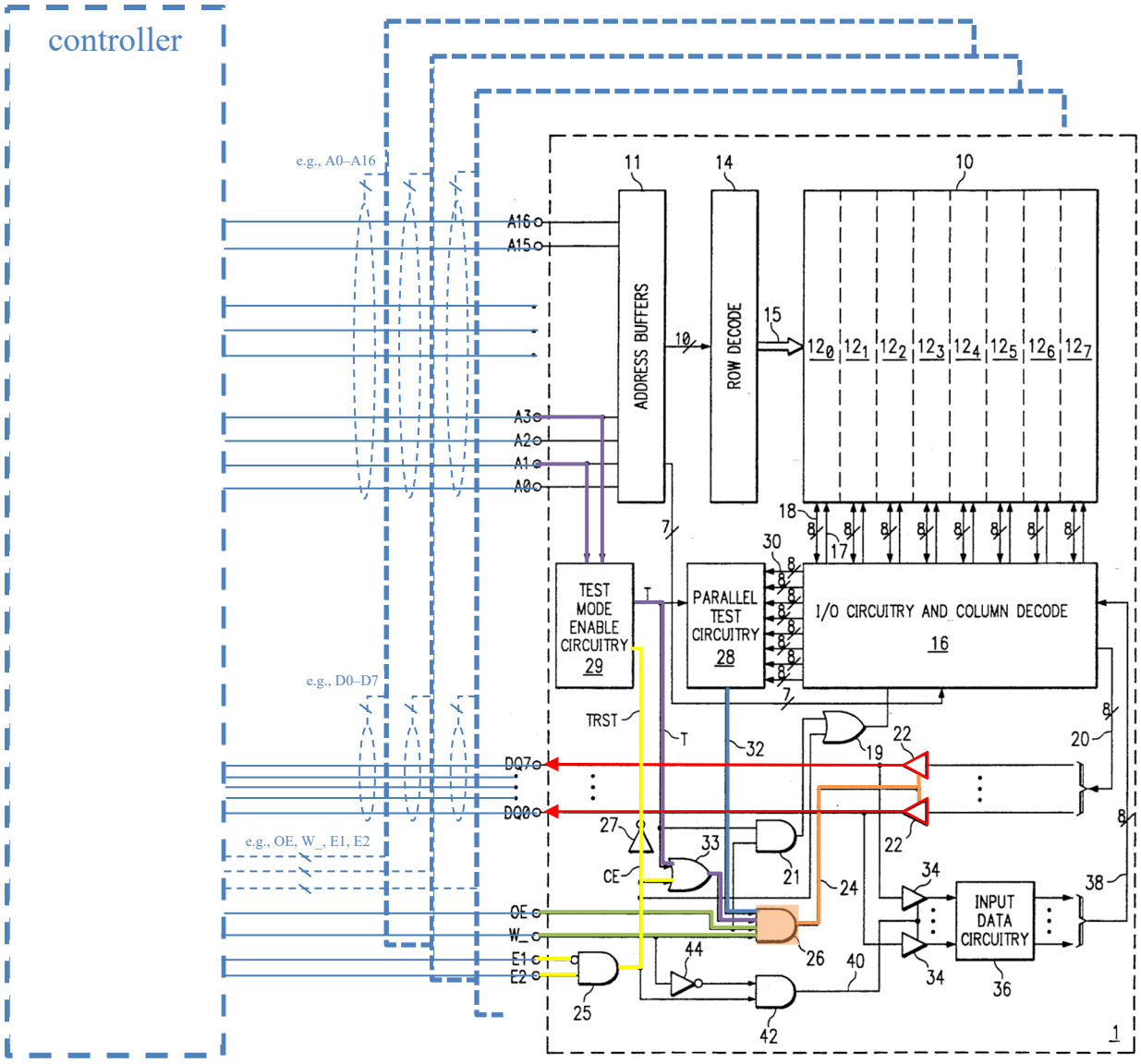


See supra Section X.D.1; Slemmer (EX1005), at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above), 7:22-55, 8:47-55. Accordingly, Slemmer teaches claim element [10.1] for the reasons provided above for claim element [4.1]. *Id.*

2. Claim Element [10.2]: "that during normal operation of said circuit component to be tested, data that actually needs to be output to said bus are output to said bus, and"

137. As I explained for claim element [4.2], the output drivers of the circuit component to be tested are controlled during normal operation based on an enable signal, which is an output enable (OE) signal or alternatively any combination of the OE signal, chip enable (E1/E2) signal, and/or write enable (W_) signal. *See supra* Section X.D.2; *See* Slemmer (EX1005), at FIG. 1.

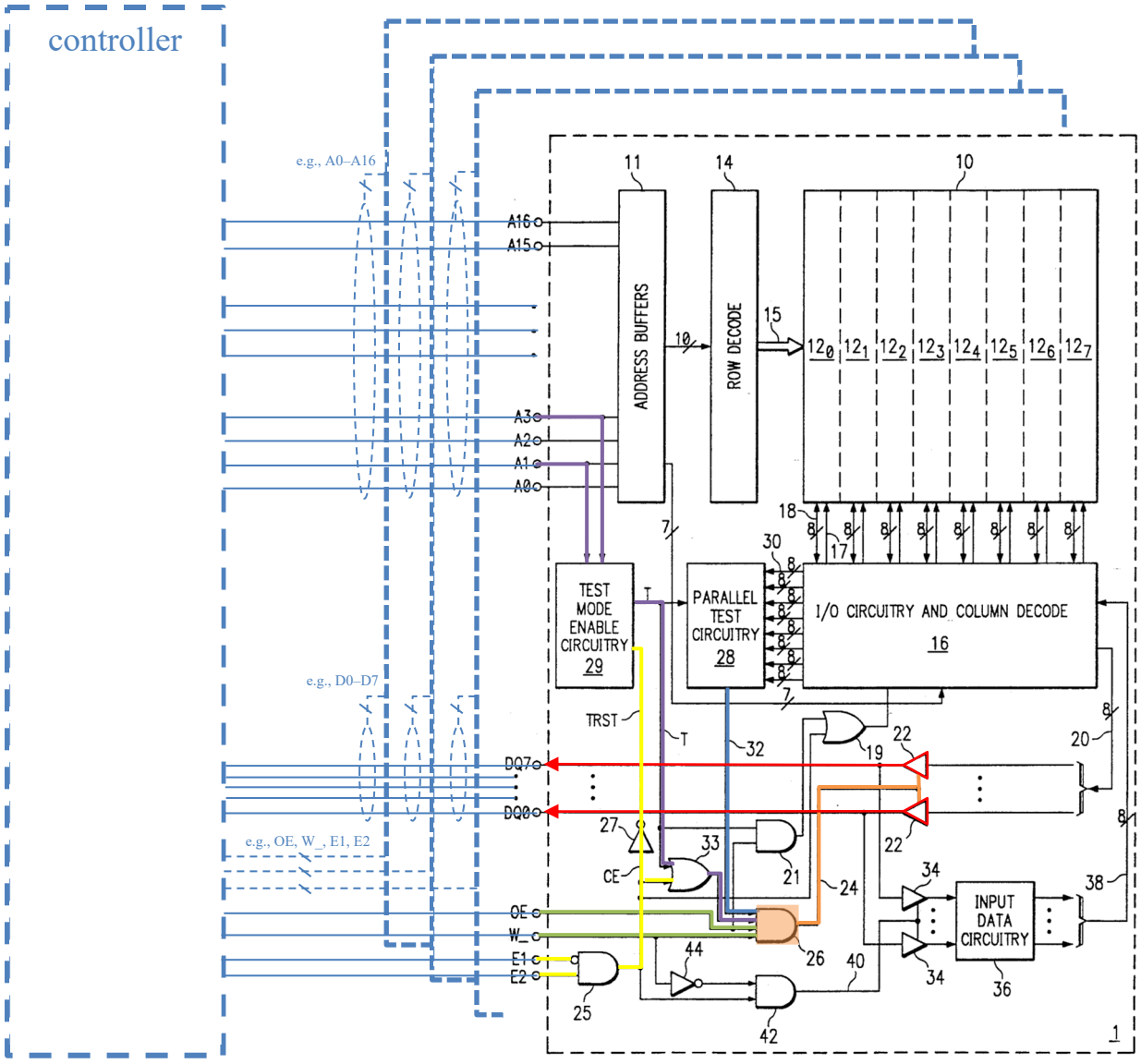
138. Slemmer teaches that the output drivers are enabled during normal operation when the write enable signal has a high logic level for read operations, the output enable signal has a high logic level, and the chip enable signals have logical levels to enable the memory device. *See* Slemmer (EX1005), at 8:4-19, :35-51, 8:49-55, FIG.; *see supra* Section X.D.2 (for claim element [4.2]). For a read operation, Slemmer teaches that the data to be output is read from the memory array and provided on internal output data bus 20 to the output buffers 22, which outputs the data because they are enabled by the enable signal.



Slemmer (EX1005), at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above), 7:22-34. Thus, Slemmer teaches that during normal operation of the memory, data for a read operation is output onto the bus ("*that during normal operation of said circuit component to be tested, data that actually needs to be output to said bus are output to said bus*").

3. Claim Element [10.3]: "that during testing of said circuit component to be tested, the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested."

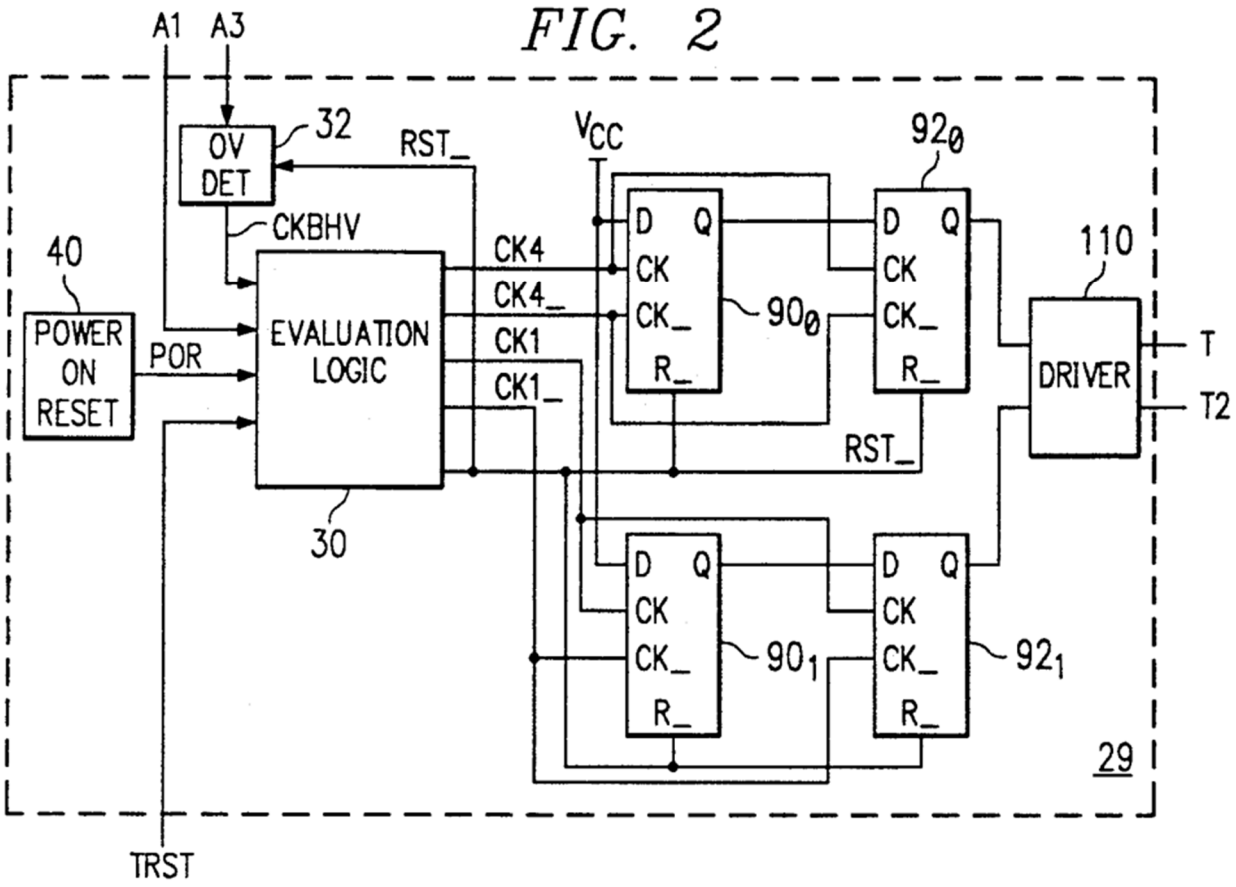
139. As I explained above for claim 7, Slemmer teaches that additional information is output at terminals DQ, such as an "identification of which test mode has been enabled" which is selected by a sequence of selection codes, such as "01011." *See supra* Section X.F; Slemmer (EX1005), at 36:45-49, 9:55-64, 27:6-15, 4:53-56, 5:3-14. Further, as I explained above for claim 3, Slemmer teaches "a test unit" that is any one of or a combination of an external controller, test mode enable circuitry (TMEC) 29, and/or parallel test circuitry (PTC) 28.



Slemmer (EX1005), at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above); *see supra* Section X.C. Accordingly, Slemmer teaches "a test unit" as recited in claim element [10.3] for at least the reasons provided above for claim 3. *Id*

140. Additionally, Slemmer teaches that the test mode is determined by the test unit because test mode enable circuitry (TMEC) 29 receives the test code and

determines which of the test modes is enabled. For example, Figure 2 of Slemmer teaches that a TMEC 29 determines which of two test modes (T and T2) are enabled:



Slemmer (EX1005), at FIG. 2. Slemmer also explains that many more test modes may be enabled by the logic of TMEC 29. *Id.* at 9:55-64. For example, Slemmer discloses that five address terminals may be used with the sequence "01011" to select a particular test mode. *See id.*, 27:6-15, FIGS. 2a, 5a-5b.

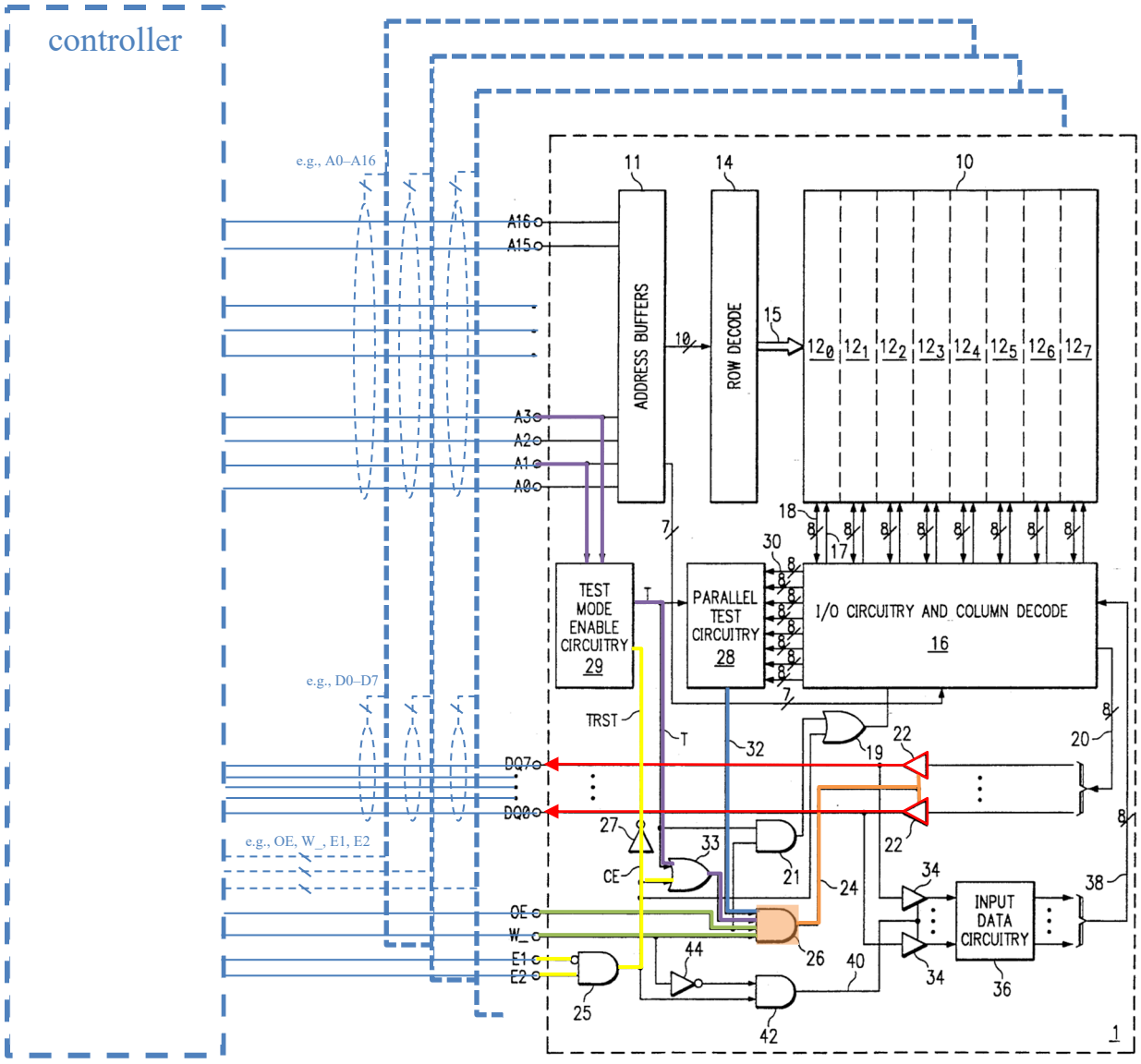
Further, a POSITA would have understood from Slemmer's teachings that the identification of which test mode is enabled that is output to the bus during

testing would be from the test unit ("*the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested*"). As I explained above, the TMEC 29 determines which test mode is enabled. A POSITA would have understood that the sequence of selection codes, such as "01011," would provide the necessary identification of the test mode to the external controller of the memory. *Id.*, at 27:6-15, 9:55-64, FIGS. 2, 2a, 5a-5b. A POSITA would also have understood that because the TMEC 29 determines the test mode based on the selection codes, the TMEC 29 ("*test unit*") also would provide the test mode information to be acknowledged by the memory to the external controller. *Id.* at 36:45-49, 9:55-64, 27:6-15, 4:53-56, 5:3-14, FIG. 1; *see supra* Section X.F for claim 7 and Section X.C for claim 3 (discussing Slemmer's "test unit"). For example, Slemmer discloses that TMEC 29 outputs the test mode information. Slemmer (EX1005), at 9:44-55, 7:35-45, 8:47-53, 34:58-35:6, FIGS. 1-2a. Thus, Slemmer teaches that during testing of the memory, an identification of which test mode is enabled is data output to the bus from TMEC 29 (part of the "test unit"), which carries out the testing of the memory by enabling the particular test mode upon determining a sequence of selection codes specific to the test mode ("*that during testing of said circuit component to be tested, the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested*").

I. Claim 13 ("The electrical circuit according to claim 10, wherein said circuit component to be tested includes output drivers for

outputting data to said bus, and each one of said output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit.") and Claim 14 ("The electrical circuit according to claim 13, wherein each one of said output drivers receives an input signal that is an output signal of said respectively provided device.")

141. As I explained above for claim 2, Slemmer teaches that the memory includes output buffers that drive output data to the bus ("*circuit component to be tested includes output drivers for outputting data to said bus*"). *See supra* Section X.B. Further, as I explained above for claim 4, Slemmer teaches that the electrical circuit includes logic, including AND-gate 26, which is "*a device*" that is "*a logic unit*."



Slemmer (EX1005), at FIG. 1 (annotated at system level in view of Slemmer's teachings as discussed in Section IX.A above), 7:22-55, 8:47-55; *see supra* Section X.D.1 for claim element [4.1]. As shown in the figure above, the output of AND-gate 26 is provided to the output buffers 22 ("*output drivers*"). *Id.* Based on Slemmer's teachings, a POSITA would have understood that each of the output buffers is controlled by the logic ("*provided with a device that is selected from the*

group consisting of a logic unit"). A POSITA would also have understood that the logic outputs an output signal, such as a signal on line 24, to be input to each of the output buffers ("*each one of said output drivers receives an input signal that is an output signal of said respectively provided device*").

142. Additionally, Slemmer teaches that the logic may be different between different ones of the output buffers. Slemmer discloses that the enabling of testing "can be adequately communicated by a selected one of terminals DQ presenting a low impedance state." *Id.*, 36:41-54. Slemmer also discloses that "additional information could be presented" at terminals DQ such as an "identification of which test mode has been enabled." *Id.*, 36:45-49. Slemmer also teaches that the terminals DQ are normally deactivated (in a high impedance state) when the chip is not enabled. *Id.*, 36:31-40. Accordingly, a POSITA would have understood that other terminals DQ, that are not selected to communicate the enabling of testing, would be deactivated. To activate some drivers of some DQ terminals while deactivating other drivers of other DQ terminals, a POSITA would have understood that each of the drivers and DQ terminals would be controlled by different logic that outputs a different signal for its corresponding driver to implement its corresponding functionality during testing, such as activating or deactivating the driver of the DQ terminal ("*each one of said output drivers is*

provided with a device that is . . . a logic unit"). *See, e.g.*, *id.*, 36:45-54.

Accordingly, Slemmer teaches claims 13 and 14.

J. Claim 20

1. Claim Element [20.P]: "A method for testing a circuit component which is connected to other circuit components via a bus, the method which comprises:"

143. I understand that the preamble of claim 1 is not limiting. Nevertheless, to the extent the preamble is found to be limiting, Slemmer teaches this claim element for the reasons I provided above for claim elements [1.P], [1.1] ("a bus"), and 1.2] ("a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components"). *See supra* Sections X.A.1-X.A.3.

2. Claim Element [20.1]: "providing a plurality of circuit components that are connected to a bus;"

144. Slemmer teaches this claim element for the reasons provided above for claim element [1.2], which recites "a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components." *See supra* Section X.A.3. As I explained, Slemmer teaches multiple memories connected to a bus. *Id.*; *see also* Slemmer (EX1005), at 35:22-42, 37:11-37.

3. Claim Element [20.2]: "configuring at least one of the plurality of circuit components such that it can be tested independently from all others of said plurality of circuit components, the at least one of the plurality of circuit components defining a circuit component to be tested; and"

145. Slemmer teaches this claim element for the reasons provided above for claim element [1.2], which recites "a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components." *See supra* Section X.A.3. As I explained, Slemmer teaches that one of the multiple memories is configured to be tested, and defines a circuit component to be tested, independent from the other memories by providing input signals to the terminals of the memory. *Id.*; *see also* Slemmer (EX1005), at 36:2-25, 37:1-37, FIGS. 1, 9.

4. Claim Element [20.3]: "while testing the circuit component to be tested, performing an operation with the circuit component to be tested, the operation selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation."

146. Slemmer teaches this claim element for the reasons provided above for claim element [1.3], which recites "said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus

that is other than data which would be output to said bus during normal operation." *See supra* Section X.A.4.

K. Claim 21

1. Claim Element [21.1]: "The method according to claim 20, which comprises: providing the circuit component to be tested with output drivers for outputting data to the bus; and"

147. Slemmer teaches this claim element for the reasons provided above for claim 2, which recites the "electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested." *See supra* Section X.B.

2. Claim Element [21.2]: "deactivating the output drivers during testing of the circuit component to be tested."

148. Slemmer teaches this claim element for the reasons provided above for claim 2, which recites the "electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested." *See supra* Section X.B.

L. Claim 22: "The method according to claim 21, which comprises deactivating the output drivers by a test unit which is testing the circuit component to be tested."

149. Slemmer teaches this claim for the reasons provided above for claim 3, which recites the "electrical circuit according to claim 2, wherein said output

drivers are deactivated by a test unit which is testing said circuit component to be tested." *See supra* Section X.C.

M. Claim 23

1. Claim Element [23.1]: "The method according to claim 22, which comprises: providing a device for deactivating the output drivers;"

150. Slemmer teaches this claim element for the reasons provided above for claim element [4.1], which recites the "electrical circuit according to claim 3, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring." *See supra* Section X.D.1.

2. Claim Element [23.2]: "selecting the device from the group consisting of a logic unit and a selection circuit;"

151. Slemmer teaches this claim element for the reasons provided above for claim element [4.1], which recites the "electrical circuit according to claim 3, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring." *See supra* Section X.D.1.

3. Claim Element [23.3]: "using the device to ensure: that during normal operation of the circuit component to be tested, the output drivers are controlled based upon an enable signal which is

supplied to the circuit component to be tested by a bus control device which controls the bus, and"

152. Slemmer teaches this claim element for the reasons provided above for claim element [4.2], which recites "that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device which controls said bus." *See supra* Section X.D.2.

4. Claim Element [23.4]: "that during testing of the circuit component to be tested, the output drivers are controlled based upon a test control signal which the test unit supplies to the circuit component to be tested."

153. Slemmer teaches this claim element for the reasons provided above for claim element [4.3], which recites "that during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested." *See supra* Section X.D.3.

N. Claim 24: "The method according to claim 23, which comprises using the logic unit to provide an output signal resulting from a logical combination of the enable signal and a test control signal."

154. Slemmer teaches this claim for the reasons provided above for claim 5, which recites the "electrical circuit according to claim 4, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the enable signal and a test control signal." *See supra* Section X.E.

O. Claim 26: "The method according to claim 20, which comprises signaling a bus control device which controls the bus that the circuit component to be tested is undergoing a test."

155. Slemmer teaches this claim for the reasons provided above for claim 7, which recites the "electrical circuit according to claim 1, comprising a bus control device for controlling said bus and for receiving a signal indicating testing of said circuit component to be tested." *See supra* Section X.F.

P. Claim 28: "The method according to claim 20, wherein the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during normal operation, and selecting the data output to the bus from the group consisting of infrequently changing data and non-changing data."

156. Slemmer teaches this claim for the reasons provided above for claim 9, which recites the "electrical circuit according to claim 1, wherein the operation performed by said circuit component to be tested, during the testing thereof, is outputting data to said bus that is other than the data which would be output to said bus during normal operation, and the data outputted to said bus is data selected from the group consisting of infrequently changing data and non-changing data." *See supra* Section X.G.

Q. Claim 29

1. Claim Element [29.1]: "The method according to claim 28, which comprises: selecting a device from the group consisting of a logic unit and a selection circuit;"

157. Slemmer teaches this claim element for the reasons provided above for claim element [4.1], which recites "electrical circuit according to claim 3, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring," and claim element [10.1], which recites "electrical circuit according to claim 9, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device ensuring." *See supra* Sections X.D.1, X.H.1.

2. Claim Elements [29.2]: "using the device to ensure: that during normal operation of the circuit component to be tested, data that actually needs to be output to the bus are output to the bus, and"

158. Slemmer teaches this claim element for the reasons provided above for claim element [4.2], which recites "that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device which controls said bus," and claim element [10.2], which recites "that during normal operation of said circuit component to be tested, data that actually needs to be output to said bus are output to said bus." *See supra* Sections X.D.2, X.H.2.

3. Claim Element [29.3]: "that during testing of the circuit component to be tested, the data outputted to the bus is from a test unit carrying out the testing of the circuit component to be tested."

159. Slemmer teaches this claim element for the reasons provided above for claim element [4.3], which recites "that during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested," and claim element [10.3], which recites "that during testing of said circuit component to be tested, the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested." *See supra* Sections X.D.3, X.H.3.

R. Claim 32

1. Claim Element [32.1]: "The method according to claim 29, which comprises: providing the circuit component to be tested with output drivers for outputting data to the bus; and"

160. Slemmer teaches this claim element for the reasons provided above for claim 2, which recites the "electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested." *See supra* Section X.B.

2. Claim Element [32.2]: "providing each one of the output drivers with a device that is selected from the group consisting of a logic unit and a selection circuit."

161. Slemmer teaches this claim element for the reasons provided above for claim element [4.1] ("electrical circuit according to claim 3, comprising a

device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring"), claim 13 ("The electrical circuit according to claim 10, wherein said circuit component to be tested includes output drivers for outputting data to said bus, and each one of said output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit") and claim 14 ("The electrical circuit according to claim 13, wherein each one of said output drivers receives an input signal that is an output signal of said respectively provided device"). *See supra* Section X.D.1, X.I.

S. Claim 33: "The method according to claim 32, wherein each one of the output drivers receives an input signal that is an output signal of the respectively provided device."

162. Slemmer teaches this claim element for the reasons provided above for claim element [4.1] ("electrical circuit according to claim 3, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring"), claim 13 ("The electrical circuit according to claim 10, wherein said circuit component to be tested includes output drivers for outputting data to said bus, and each one of said output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit") and claim 14 ("The electrical circuit according to claim 13, wherein each one of said output drivers receives an input

signal that is an output signal of said respectively provided device"). *See supra* Section X.D.1, X.I.

XI. Claims 1-5, 7-10, 13-14, 20-24, 26-29, 32-33 are Obvious over Slemmer and Gasbarro

A. Combination of Slemmer and Gasbarro

163. The teachings of Slemmer and Gasbarro can and would have been combined to arrive at the claimed electrical circuits and methods of the '473 Patent. As I explain in more detail below, Gasbarro teaches how to implement a memory system that balances impedances to support expandable memory while avoiding signal reflections and increased line noise and a POSITA would have been motivated to combine Slemmer with Gasbarro, and had a reasonable expectation of success in doing so.

164. Both Slemmer and Gasbarro relate to the field of memories and their systems. *See* Slemmer (EX1005), at 1:6-8, 3:7-16, 36:64-68; Gasbarro (EX1006), at 1:6-9, FIG. 1. Slemmer discloses a bus with bi-directional lines for data transfer to and from the memory. Slemmer (EX1005), at 8:59-61, FIG. 1. Slemmer also teaches that multiple memories are connected via their terminals to a bus that connects them to a controller, such as a controller used in an end-user system for reads from and writes to the memories and for testing of the memories. Slemmer (EX1005), at FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:4-5, 8:14-19, 8:59-67, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 36:55-

68, 37:11-24, 37:27-29, 37:33-37; *see e.g.*, EX1011, 18:9-13, 18:51-54, 26:8-12, FIG. 24; EX1012, FIG. 1, 1:16-21, 1:49-52. Similarly, Gasbarro discloses that a conventional memory system includes a memory controller for writing data into and reading data from the memory devices via a bi-directional bus. Gasbarro (EX1006), at 1:15-19, 4:45-48.

165. Slemmer also teaches that his invention benefits many types of memories, including static random access memory (SRAM) and dynamic RAM (DRAM). Slemmer (EX1005), at 6:54-66, 2:60-66, 5:50-55 (examples of SRAM), 2:9-21, 3:16-28 (examples of DRAM). Similarly, Gasbarro teaches that his invention benefits many configurations of memory systems, including those that include multiple memory devices, modules, or slots along a bus. Gasbarro (EX1006), at 3:39-42, 5:18-21. Further, Gasbarro teaches that his invention benefits "standard" memory devices that incorporate an active terminator. *See* Gasbarro (EX1006), at 5:1-8. Accordingly, a POSITA would have been motivated to support such standard memory devices and their active terminators.

166. Although Slemmer teaches a controller to a POSITA and discloses multiple memories connected together, it does not expressly disclose certain details about a memory system that connects to the multiple memories. *See* Slemmer (EX1005), at 8:14-19, 37:15-19. For example, Slemmer does not expressly illustrate the connection between the multiple memories, disclose a controller

connected to the memories to provide external inputs and receive acknowledgements of testing, or discuss termination of the connections of the memory. However, Gasbarro does disclose these technical aspects. Gasbarro discloses an expandable memory system, such as one with customizable memory system capacity, that includes a memory controller connected to multiple memories via a bus, and that uses an active terminator for each of the memory devices, such that they balance the impedance on the bus. *See* Gasbarro (EX1006), at 3:28-45.

167. As shown in the figure below, Gasbarro discloses a memory system in which the memory controller 70, that is connected to the memory devices via a channel 71 that includes a bus, uses a serial initialization line (SIL) 71 or the channel 72 to communicate an active termination signal to any one of the devices.

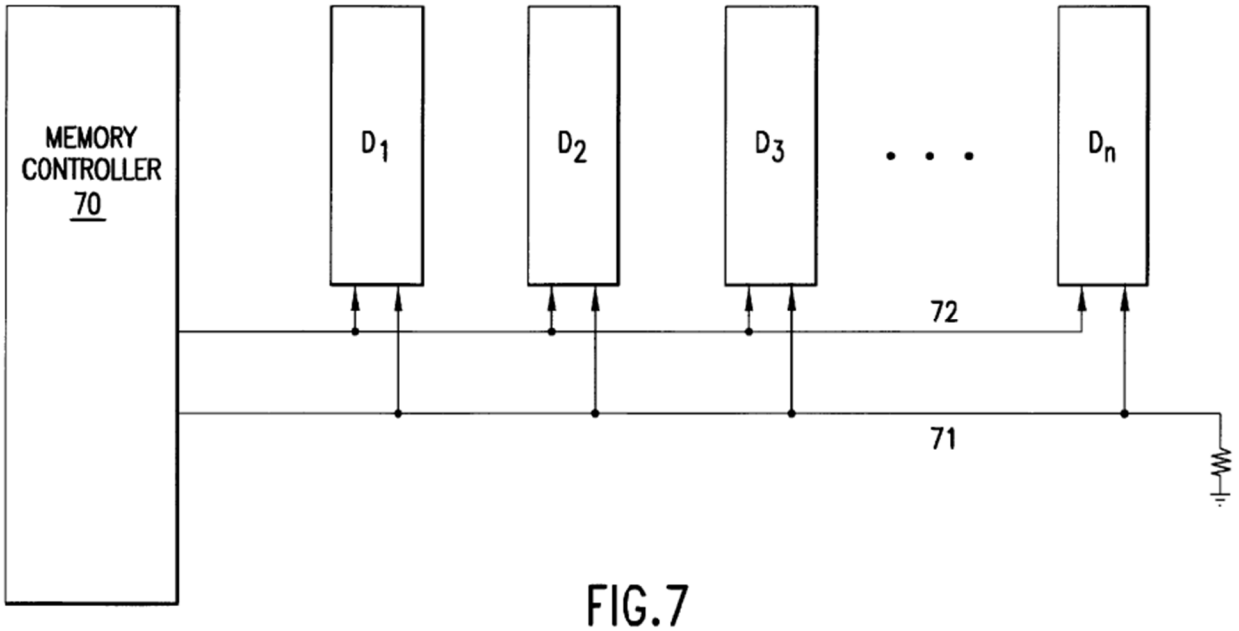


FIG.7

Gasbarro (EX1006), at FIG. 7, 6:49-54. Gasbarro explains that each of the memory devices is assigned and identified by a device identification (ID), such as via SIL 71, and that the memory controller recognizes the last device on the bus (D_n in the figure above) and turns on its corresponding active terminator. Gasbarro (EX1006), at 2:46-56, 5:63-66, 6:55-7:5. By switching on the active terminator in the last memory device, Gasbarro discloses that the memory devices on the bus benefit from balanced impedances to avoid undesired signal reflections and noise. Gasbarro (EX1006), at 7:6-14.

168. A POSITA looking to implement Slemmer's memory devices and testing architecture would have been motivated to look to a reference like Gasbarro, which discloses, as I explained above, a system with a memory controller for sending signals to and receiving signals from the memory devices and a termination architecture for sending and receiving those signals. In the combination, Slemmer's memory devices and testing architecture would be implemented using Gasbarro's teachings about a memory system, including Gasbarro's teachings that the memory devices are connected via a bus to a memory controller for read, write, and control operations and for active termination of the bus. Gasbarro (EX1006), at 1:16-19, 4:36-48, 6:8-12, FIG. 7. In the combination, the memory system would be implemented with a memory controller to send and receive signals to Slemmer's multiple memories via a bus. *See id.*; *see also*

Slemmer (EX1005), at FIG. 1, 8:14-19, 36:60-64, 37:11-26. Further, the memories, such as memory 1, disclosed by Slemmer would be implemented with active termination that is externally controlled, such as via SIL 71, and the controller would be implemented to recognize the last memory device on the bus and turn on its corresponding active terminator, such as via SIL 71. *Id.*; *see also* Slemmer (EX1005), at FIG. 1; Gasbarro (EX1006), at FIG. 7. A POSITA would have understood that this implementation of Slemmer in view of Gasbarro simply uses a known technique (e.g., active termination for expandable memory) to improve a similar device (e.g., Slemmer's memory devices with testing functionality) in the same way (e.g., by implementing a memory system with a bus connecting a controller to the memory devices, supporting active termination in the memory devices, supporting recognition of the last memory device in the controller, as well as the ability to turn on the corresponding active terminator for bus termination). Additionally, a POSITA would have understood that this implementation of Slemmer in view of Gasbarro simply uses prior art elements (e.g., Slemmer's memory devices with testing functionality and Gasbarro's memory controller connected to those memory devices with active termination for the bus) according to known methods (e.g., using a conventional memory system controller and connection to the terminals of the memories and using active terminators for expandable memory support) to yield predictable results (e.g., a memory system

with support for expandable memory that balances impedances to avoid signal reflections and noise).

169. Further, a POSITA would have been motivated to implement Slemmer in accordance with Gasbarro's teachings to ensure interoperability and proper operation with standard memory devices that already incorporate active termination, as taught by Gasbarro. *See* Gasbarro (EX1006), at 5:1-8. Accordingly, a POSITA implementing Slemmer with such standard memory devices would have looked to Gasbarro's teachings of how to use the active terminator so that it supports an expandable memory system.

B. Claim 1

170. As explained above for Ground 1, Slemmer teaches claim limitations [1.P], [1.1], [1.2], and [1.3]. *See supra* Sections X.A.1-X.A.4; *see, e.g.*, Slemmer (EX1005), at FIGS. 1, 9. For at least reasons provided for Ground 1, Slemmer also teaches these claim limitations in combination with Gasbarro.

171. Further, in the combination, Slemmer and Gasbarro teach the limitations of claim 1. For claim limitation [1.1], Gasbarro discloses that between multiple memory devices and a memory controller is a channel (71) that includes a data bus, which is similar to Slemmer's teaching of a memory with multiple terminals connected to signal lines (e.g., one or more of those signal lines are "a bus") to send and/or receive data and Slemmer's teachings of multiple memories

connected in parallel in a system. Gasbarro (EX1006), at FIG. 7, Abstract, 4:36-44, 6:65-7:1; Slemmer (EX1005), at FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:14-19, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 37:11-24, 37:27-29, 37:33-37. Accordingly, a POSITA would have understood that in the combination, the multiple data terminals (e.g., DQ0 through DQ7) and multiple address terminals (e.g., A0 through A17) in Slemmer's memories would be connected to signal lines and that one or more signal lines are "*a bus*" that connects the memory devices to a memory controller. *See supra* Section X.A.2; Gasbarro (EX1006), at 1:16-19, 4:36-48, 6:8-12, FIG. 7. A POSITA would also have understood that the bus is part of a channel connecting the memory devices together, such as one disclosed by Gasbarro that includes signal lines for control information. *Id.* Further, a POSITA would have understood that the memory controller provides external inputs to the memory devices including control for active termination, such as via SIL 71 or channel 72 as disclosed by Gasbarro. Gasbarro (EX1006), at 2:46-56, 5:63-66, 6:55-7:5, FIG. 7.

C. Claim 2: "The electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested."

172. Claim 2 depends from claim 1, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claim 2. *See supra* Section X.B.

D. Claim 3: "The electrical circuit according to claim 2, wherein said output drivers are deactivated by a test unit which is testing said circuit component to be tested."

173. As I explained above for Ground 1, Slemmer teaches claim 3. *See supra* Section X.C; *see, e.g.*, Slemmer (EX1005), at FIGS. 1, 9.

174. Additionally, a POSITA would have understood that the memory controller in the combination of Slemmer and Gasbarro is the external controller that externally drives inputs to configure the memory for testing, which results in the deactivation of the output drivers. Slemmer (EX1005), at 9:19-30, FIG. 1; *see supra* Sections X.D.2 (for claim element [4.2]), XI.A (combination of Slemmer and Gasbarro), XI.B (for claim 1) (each discussing memory controller in combination).

175. Accordingly, the output drivers are "*deactivated by*" any one of or a combination of the memory controller, TMEC 28, and/or PTC 29 ("*a test uni*t").

E. Claim 4

176. As I explained above for Ground 1, Slemmer teaches claim 4. *See supra* Section X.D; *see, e.g.*, Slemmer (EX1005), at FIGS. 1, 9.

177. Additionally, a POSITA would have understood that in the combination of Slemmer and Gasbarro, the memory controller is a "bus control device" (as recited in claim element [4.2]) that provides control information, including the chip enable (E1/E2) signals, a write enable (W_) signal, and an

output enable (OE) signal to the memory (any one of or a combination of which is "*an enable signal*"), to control the output drivers of memory 1 in Slemmer via AND-gate 26. Slemmer (EX1005), at FIG. 1; *see supra* Sections X.D.2 (for claim element [4.2]), XI.A (combination of Slemmer and Gasbarro), XI.B (for claim 1) (each discussing memory controller in combination). Further, as I discussed above, the memory controller in the combination of Slemmer and Gasbarro is the external controller discussed in Ground 1. *See supra* Section XI.D.

F. Claim 5: "The electrical circuit according to claim 4, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the enable signal and a test control signal."

178. Claim 5 depends from claim 4, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claim 5. *See supra* Section X.E.

G. Claim 7: "The electrical circuit according to claim 1, comprising a bus control device for controlling said bus and for receiving a signal indicating testing of said circuit component to be tested."

179. Claim 7 depends from claim 1, whose limitations are above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claim 7. *See supra* Section X.F.

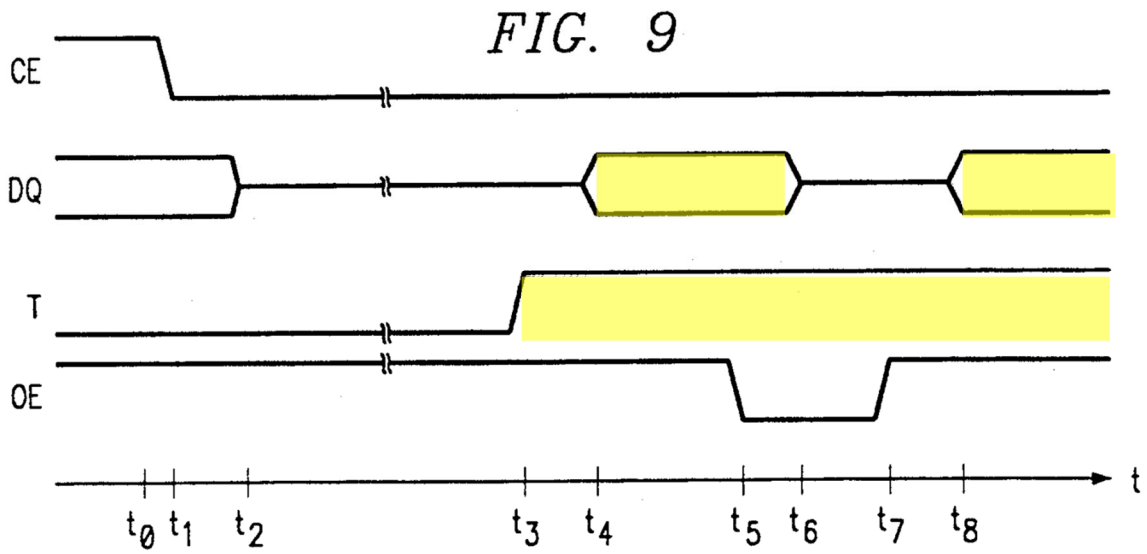
180. Additionally, as I discussed above, the memory controller in the combination is the "*bus control device*." *See supra* Section XI.E. A POSITA would

have understood that the memory controller receives a signal indicating testing of the memory to be tested. *See supra* Sections XI.E-XI.F.

H. Claim 8: "The electrical circuit according to claim 7, wherein, during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by a device selected from the group consisting of said bus control device and one of said others of said plurality of circuit components."

181. As explained for Ground 1, Slemmer teaches claim 7, including teaching that a controller ("*bus control device*") receives test information on one or more DQ terminals/lines from the memory 1 during tested. *See supra* Section X.F; *see also supra* Section X.D.2 (discussing Slemmer's "bus control device" for claim element [4.2]). Additionally, as explained for Ground 2, Slemmer and Gasbarro teaches claim 7, including teaching a memory controller ("*bus control device*"). *See supra* Section XI.G.

182. Further, as I explain below, Slemmer in view of Gasbarro also teaches that in order for the controller to receive the test information successfully from the memory 1 during testing, it must ensure that the DQ terminals/lines ("*bus*") are terminated by the last memory device on the bus, as explained in more detail below. As shown in the figure below, the memory 1 of Slemmer drives the DQ terminal during testing between times t_4 and t_6 and after time t_8 (highlighted in yellow).



Slemmer (EX1005), at FIG. 9. Slemmer explains that at time t_4, "[r]esponsive to line T at a high logic level, OR gate 33 will present a high logic level to AND gate 26." *Id.*, 36:25-27. In addition, the "terminals OE and W_ are at high logic levels" and "line 32 from parallel test circuitry 28 remains high." *Id.*, 36:27-30. Accordingly, the terminal(s) DQ "go into an active state" (in a low-impedance) to communicate test information, such as whether a particular "test either passed, or has not taken place" during testing. *Id.*, 36:29-31, 36:32-40, 36:41-54. Similarly, at time t_8, responsive to "externally driving terminal OE to a high logic level," the terminal(s) DQ again become active and present data. *Id.*, 37:33-37.

183. Further, Slemmer teaches that the controller, such as one in a system or test equipment, must receive the test information from the DQ terminal(s). *See* Slemmer (EX1005), at FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:4-5, 8:14-19, 8:59-67, 32:64-33:2, 35:22-42, 35:47-51, 35:52-

64, 36:55-68, 37:11-24, 37:27-29, 37:33-37; *see e.g.*, EX1011, 18:9-13, 18:51-54, 26:8-12, FIG. 24; EX1012, FIG. 1, 1:16-21, 1:49-52. For example, communication of the test information "allows detection of [an] inadvertent entry into [a test] mode, so that the user may perform the necessary cycles to return to the normal operating mode of the device." Slemmer (EX1005), at 35:47-51. The information also allows "the test equipment and personnel" of a system to distinguish between "whether the memory actually failed the test or if it merely failed to enter the test mode." *Id.*, 35:36-42; *see also id.*, 35:25-30 ("A first function of such construction is that memory 1 can communicate its special test mode status, providing the user (or the interrogating test equipment) acknowledgment that the device is in a special test mode, prior to such time as special test operations are performed."). Similarly, Gasbarro teaches a memory controller for receiving data from a memory device. Gasbarro (EX1006), at 1:16-19, 4:45-48, 6:8-12, FIG. 7.

184. A POSITA would have understood that in order for the controller to receive the test information from the DQ terminal(s), the controller must ensure that the bus is properly terminated. As I explained above, in the combination, the memories disclosed by Slemmer would be modified to be implemented with active termination that is externally controlled, and the controller, as taught by Slemmer and disclosed by Gasbarro, would be modified to recognize the last memory device on the bus and turn on its corresponding active terminator. *See supra* Section XI.A.

Accordingly, a POSITA would have understood that when testing a memory that is not the last memory device on the bus, the memory controller ("*bus control device*") would enable the active terminator of another memory device that is the last device on the bus ("*one of said others of said plurality of circuit components*"). Because termination is needed for the bus, a POSITA would have recognized that Gasbarro teaches using active termination for all operations, including normal operation and testing. More specifically, termination is needed any time commands or data is to be transmitted over the bus, such as being sent from the controller to the memory. For example, during normal operation, read operations would require bus termination for the memory to send read data and write operations would require bus termination for the controller to send write data. Similarly, for testing, sending test data from the memory would require bus termination for the controller to receive that data successfully. Indeed, Gasbarro teaches that imbalance between memory components will result in unwanted signal reflections and increased signal line noise. Gasbarro (EX1006), at 2:59-64. To enable balance of impedances in an expandable memory system, the controller in the combination ("*bus control device*") controls active terminators in each of the memory devices, such as via serial initialization line (SIL) 72 or channel 71, as shown below:

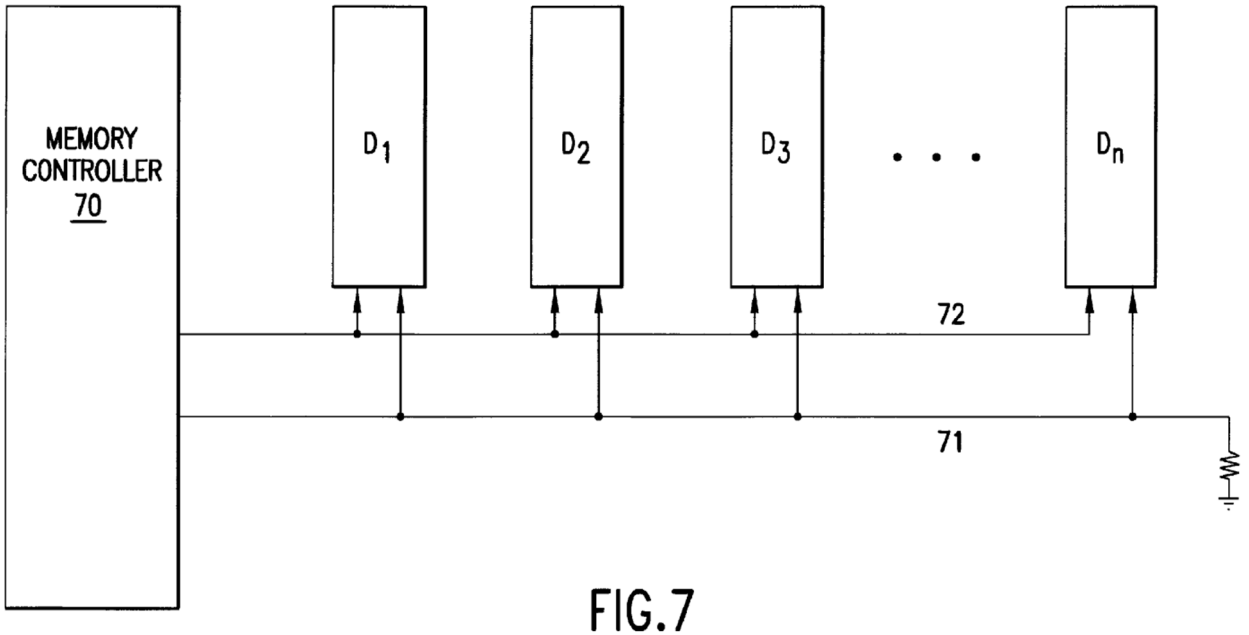


FIG.7

Id. at FIG. 7, 3:42-45, 6:49-54. Specifically, the controller determines which device is the last on the bus (D_n in the figure above) during initialization and then enables the active terminator on only that device to balance impedances. *Id.* at 6:55-7:5; *see also id.* at 6:49-54, 7:6-14. Accordingly, Slemmer in view of Gasbarro teaches "*during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by . . . one of said others of said plurality of circuit components*."

I. Claims 9-10 and 13-14

185. Claims 9-10 and 13-14 depend from claim 1, whose limitations I discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claims 9-10 and 13-14. *See supra* Sections X.G, X.H, X.I. Moreover, as I addressed in Ground 1, claim 10

contains claim elements similar to claim elements in claims 3, 4, and 7, and claims 13 and 14 contain claim elements similar to claim elements in claims 2 and 4. *Id.* I also discussed claims 2-4 and 7 and their claim elements above in this ground. *See supra* Sections XI.C-XI.E, XI.G. As I explained for claim 4, for example, the memory controller in the combination of Slemmer and Gasbarro provides control information, such as an enable signal to control the output drivers to output data during normal operation. *See supra* Section XI.E; Slemmer (Slemmer (EX1005), at FIG. 1.

J. Claim 20

186. As explained above for Ground 1, Slemmer teaches claim limitations [20.P], [20.1], [20.2], and [20.3]. *See supra* Section X.J; *see, e.g.*, Slemmer (EX1005), at FIGS. 1, 9.

187. Further, in the combination, Slemmer as modified by Gasbarro's teachings of a memory controller and memory with support for expandable memory teach the limitations of claim 20. For the reasons explained above for claim 1, a POSITA would have understood that in the combination, a channel with a bus would have been implemented to connect a controller of the memory to multiple memory devices to support expandable memory, such as by providing external inputs to the memory devices including control for active termination, such as via SIL 71 or channel 72 as disclosed by Gasbarro, as well as to support

normal operation and test modes, as disclosed in Slemmer. *See supra* Section XI.B; Gasbarro (EX1006), at 2:46-56, 5:63-66, 6:55-7:5, FIG. 7; *see, e.g.*, Slemmer (EX1005), at FIGS. 1, 9.

K. Claims 21-24 and 26

188. Claims 21-24 and 26 depend from claim 20, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claims 21-24 and 26. *See supra* Sections X.K- X.O. Further, the limitations of claims 21-24 and 26 are similar the limitations of claims 2-5 and 7, respectively. *Id.* Slemmer and Gasbarro teach claims 21-24 and 26 for the additional reasons provided above for this ground. *See supra* Sections XI.C-XI.G.

L. Claim 27: "The method according to claim 26, which comprises using the bus control device to ensure that, during testing of the circuit component to be tested, the bus is terminated by a device selected from the group consisting of the bus control device and one of the others of the plurality of circuit components."

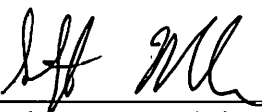
189. As explained for claim 8 above, Slemmer and Gasbarro teach "during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by . . . one of said others of said plurality of circuit components," and thus also teach claim 27. *See supra* Section XI.H; Gasbarro (EX1006), at 6:49-7:14, FIG. 7.

M. Claims 28-29 and 32-33

190. Claims 28-29 and 32-33 depend from claim 20, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claims 28-29 and 32-33. *See supra* Sections X.P-X.Q, X.R-X.S. Moreover, as I addressed in Ground 1, claim 29 contains claim elements similar to claim elements in claims 4 and 10, and claims 32 and 33 contain claim elements similar to those in claims 2, 4, and 13-14. *Id.* Claims 2, 4, 10, and 13-14, and their claim elements, are also discussed above in this ground. *See supra* Sections XI.C, XI.E, XI.I.

I, Stephen W. Melvin, Ph.D., declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Dated: January 30, 2023



Stephen W. Melvin, Ph.D.