

## EDUCATION

**Ph.D., Computer Science**, University of California, Berkeley, May 1991.

Research Areas: High-performance computer architecture and microarchitecture (exploiting fine-grained parallelism in general purpose programs through a combination of hardware and software techniques); Microcode-based system performance analysis tools.

Minor Areas: Statistics, Computer Theory

**B.S. (with high honors), Electrical Engineering and Computer Science**, University of California, Berkeley, May 1982.

## GENERAL WORK EXPERIENCE

April 2020 – Present, **Principal, Exponent, Inc.**

Advising industrial and legal clients on issues relating to intellectual property, including patent, copyright and trade secret litigation.

August 1983 – March 2020, **President, Zytek Communications Corporation**

Founded Zytek as an engineering, consulting and small-scale manufacturing company. Zytek provided consulting services related to intellectual property litigation and licensing, patent prosecution as well as services related to the design, implementation and testing of embedded systems. General areas of activity have also included source code analysis and comparison, forensic hard disk analysis and file recovery, industrial control and measurement, Internet related services and computer engineering research services.

January 2014 - December 2015, **President, Stage Innovations, Inc.**

Formed Stage Innovations to hold and develop patents in the area of Internet based voice messaging and fax and email notification. Prosecuted multiple patent applications to issuance and successfully negotiated a sale of the entire portfolio.

August 2002 – October 2005, **Patent Agent and Technical Advisor, O'Melveny & Myers LLP**

Assistance with a broad range of intellectual property cases, including patent, copyright and trade secret litigation, patent licensing and due diligence. Prior art research, patent validity and infringement analysis, source code comparison, forensic hard disk analysis. Preparation and prosecution of patents in different areas of technology.

May 2001 – August 2002, **Founder and Chief Architect, FlowStorm, Inc. (later ConSentry Networks)**

Defined and guided the overall chip architecture for a new packet processor. Managed a group of RTL designers to develop working RTL code for the processing core, packet management and interconnect blocks. Developed verification strategy and worked with performance analysis and software groups.

March 2000 - May 2001, **Senior Architect, Clearwater Networks (formerly XStream Logic, Inc.)**

Helped define the architecture and microarchitecture of the XStream network processor. Worked with a team of design engineers to evaluate tradeoffs in microarchitecture, directed design choices to balance tradeoffs in performance and cost. Documented the architecture and worked with software engineers to analyze performance and develop software.

July 1999 – July 2002, **Consulting Engineer, Adroit Engineering, Inc.**

Development of hardware and firmware for optical headlight alignment system for Ford Motor Company. Analog and digital circuit design, firmware engineering, calibration and testing.

September 1998 - December 1998, 1991-1995 **Consulting Engineer, HaL Computer Systems, Inc.**

Analysis and testing of cycle by cycle simulator of new SPARC based microprocessor. Validation of results and comparison with microarchitecture definition. Assisted in advanced microarchitecture research on a new implementation of the SPARC architecture, including performance modeling and simulation. Maintenance and enhancement of microarchitecture level and architecture level simulation tools.

June 1986 - December 1987, **Consulting Engineer, Digital Equipment Corporation**

Consulting for the High-Performance Advanced Development Group in Marlboro on VAX 8600 microcode and the application of out-of-order execution concepts to the VAX architecture. Development of special purpose VAX 8600 microcode and porting and improvement of an HPS/VAX microarchitectural simulator.

June 1984 - September 1984, **Engineer, Denelcor Corporation**

Investigation of the design of architecture to follow the HEP-1 and HEP-2 under the supervision of Dr. Burton Smith. Development of a new architecture, Vulture, allowing higher function unit utilization and incorporating a new method of scheduling register reads and writes in a multiprogrammed pipelined system.

**INTELLECTUAL PROPERTY CONSULTING EXPERIENCE**

September 2018 – September 2019, **Testifying Expert, F. Tabaian and A. Ashrafzadeh v. Intel Corp. (OR)**

Analysis of patents, analysis of source code related to voltage regulation technology.

August 2017 – October 2017, **Testifying Expert, Tripwire, Inc. v. UpGuard, Inc. (OR)**

Analysis of patents, analysis of source code related to security software.

December 2017 – January 2018, **Testifying Expert, NFL Enterprises LLC v. OpenTV, Inc. (USPTO)**

Analysis of patents and prior art related to media streaming and content distribution, declaration for IPR.

November 2015 – May 2016, **Testifying Expert, OpenTV, Inc., NagraVision SA and Nagra France S.A.S. v. Apple, Inc. (NDCAL, USPTO)**

Analysis of patents and prior art related to media streaming and content distribution, declaration for IPR.

December 2014 – January 2015, **Testifying Expert, Amazon, Inc. v. c4cast.com, Inc. (USPTO)**

Analysis of patents and prior art related to content distribution, declaration for IPR.

February 2012 – December 2017, **Testifying Expert / Consulting Expert, Mentor Graphics Corporation v. EVE-USA, Inc., Emulation and Verification Engineering, S.A., Synopsys, Inc. (OR, CAND, Japan)**

Analysis of patents, prior art and software and firmware technology related to electronic design automation. Declarations for Japan litigation.

August 2010 – March 2014, **Testifying Expert, The Quantum World Corporation v. Dell Inc. et al. (TXWD)**

Analysis of patents and prior art relating to true random number generators. Statistical analysis of random data sets.

February 2011 – April 2012, **Testifying Expert, Pact XP Technologies, AG v. Xilinx, Inc. (TXED)**

Analysis of patents, prior art and technology related to programmable logic devices.

April 2011 – May 2011, **Testifying Expert, Microsoft Corporation v. Phoenix Solutions, Inc. (CACD)**

Analysis of technology related to speech processing and voice recognition.

January 2010 – June 2010, **Testifying Expert, Optimum Processing Solutions, v. AMD et al. (GAND)**

Analysis of patent relating to optically interconnected processing elements. Testimony regarding claim construction.

May 2009 – October 2009, **Testifying Expert, Saxon Innovations v. Samsung Electronics (ITC)**

Analysis of patents and prior art relating to interprocessor communication and interrupt masking. Review of source code for cellphones. Testimony at ITC hearing.

January 2008 – March 2009, **Testifying Expert, Quantum World Corporation v. Atmel Corp., et al. (TXED)**

Analysis of patents and prior art relating to true random number generators. Statistical analysis of random data sets.

March 2007 – August 2008, **Testifying Expert, Silicon Image Inc. v. Analogix Semiconductor, Inc. (CAND)**

Analysis of data sheets, product specifications and firmware related to HDMI digital television interface and devices for receiving and processing digital video data.

July 2001 – October 2001, **Testifying Expert, Intel v. Via Technologies**

Analysis of patents, AGP specifications, and other documents related to CPU/memory systems and architectures.

October 1999 - May 2000, **Testifying Expert, Accton v. Micro Linear Corporation**

July 1999 - September 1999, **Testifying Expert, Allied Telesyn v. Micro Linear Corporation**

Analysis of on-chip circuitry, testing procedures and data sheets for Ethernet controller ICs. Analysis of the application of Ethernet controller ICs in hubs and switches, design and testing. Compliance with data sheet and other published specifications.

August 1998 - December 1998, **Court Appointed Expert, Cadence v. Avant!**

Assisting Northern California Federal District Court Judge Ronald Whyte in understanding issues and technology relating to CAD design software and its alleged copyright infringement and trade secret misappropriation; source code analysis and comparison.

June 1998 - December 1998, **Testifying Expert, Canter, et. al. v. West Publishing**

Analysis of source code, proposals, internal documentation and other materials relating to natural language processing of database queries in connection with patent and trade secret misappropriation case.

June 1998 – December 1998, **Testifying Expert, Xircom v. General Patent**

Analysis of patents and other references relating to modem and packaging technology.

May 1998 – August 1999, **Testifying Expert, Hilgraeve v. Symantec**

December 1997 - February 1998, **Consulting Expert, Trend v. Symantec**

Analysis of source code, patents and other references relating to virus checking software. Analysis and operation of virus checking software and development operational tests.

May 1995 - May 1997, **Testifying Expert, DSC v. DGI**

Analysis and comparison of firm ware for a microprocessor-based telecommunications board relating to copyright issues. Testimony regarding source code analysis and concepts and practices in reverse engineering.

March 1996 - November 1996, **Testifying Expert, AMD v. Hyundai**

Analysis of flash EEPROM integrated circuits including analysis of internal circuitry, analysis of product development data and comparison of testing procedures in a trade secret case.

October 1996 - November 1996, **Testifying Expert, Texas Instruments v. Samsung**

Analysis of firm ware (ladder logic) for programmable controllers used in assembly lines in a patent infringement case.

December 1992 - July 1993, **Testifying Expert, Conner v. Western Digital**

August 1994 to December 1995, **Testifying Expert, IBM v. Conner**

Analysis of the architecture of hard disk drives, including microcontroller firm ware analysis, digital and analog circuit analysis, and dynamic testing. Analysis of patents and other references.

## TEACHING AND ACADEMIC EXPERIENCE

December 2011 - December 2012, **General Chair, 45th Annual Symposium in Microarchitecture (MICRO-45)**

Set up and managed academic conference held in Vancouver, British Columbia in December 2012.

September 2001 – April 2002, **Visiting Scholar, University of Texas, Austin**

Monthly visit to lead discussions and direct graduate students in research into high performance computer architecture.

December 1995 - December 1996, **Co-Chair, 29th Annual Symposium in Microarchitecture (MICRO-29)**

Set up and managed academic conference held in Paris, France in December 1996.

## PUBLICATIONS

Patt, Y., Hwu, W., Melvin, S., and Shebanow, M., "HPS Papers: A Retrospective," IEEE Micro July/August 2016, vol. 36, no. 4, pp. 76-79.

Melvin, S., "Endpoint Identification Using System Logs", Workshop on the Analysis of System Logs (WASL) 2009, held in conjunction with the 22nd ACM Symposium on Operating System Principles (SOSP), Big Sky, Montana, October 2009.

Melvin, S., Nemirovsky, M., Musoll, E., Huynh, J., Milito, R., Urdaneta, H., and Saraf, K., "A Massively Multithreaded Packet Processor," *NP2: Workshop on Network Processors, held in conjunction with The 9th International Symposium on High-Performance Computer Architecture (HPCA-9)*, Anaheim, California, February 8-9, 2003.

Melvin, S. and Patt, Y., "Handling of Packet Dependencies: A Critical Issue for Highly Parallel Network Processors," *Proceedings, International Conference on Compilers, Architectures, and Synthesis for Embedded Systems*, October 8 – 11, 2002.

Melvin, S., and Patt, Y., "Enhancing Instruction Scheduling with a Block-Structured ISA," *International Journal of Parallel Processing*, 23(3):221-243, 1995.

Melvin, S., and Patt, Y., "Exploiting Fine-grained Parallelism Through a Combination of Hardware and Software Techniques," *Proceedings, 18th International Symposium on Computer Architecture*, Toronto, Canada, May 1991.

Melvin, S., and Patt, Y., "Performance Benefits of Large Execution Atomic Units in Dynamically Scheduled Machines," *Proceedings, 1989 Supercomputer Conference*, Crete, Greece, June 1989.

Melvin, S., Shebanow, M., and Patt, Y., "Hardware Support for Large Atomic Units in Dynamically Scheduled Machines," *Proceedings, 21st Annual Workshop on Microprogramming and Microarchitecture*, San Diego, California, November 1988.

Melvin, S., and Patt, Y., "The Use of Microcode Instrumentation for Development, Debugging and Tuning of Operating System Kernels," *Proceedings, 1988 ACM SIGMETRICS*, Santa Fe, New Mexico, May 1988.

Melvin, S., and Patt, Y., "A Clarification of the Dynamic/Static Interface," *Proceedings, 20th Hawaii International Conference on System Sciences*, Kailua-Kona, Hawaii, January 1987.

Gee, J., Melvin, S., and Patt, Y., "Advantages of Implementing Prolog by Microprogramming a General Purpose Host Computer," *Proceedings, Fourth International Conference on Logic Programming*, Melbourne, Australia, May 1987.

Melvin, S., and Patt, Y., "SPAM: A Microcode Based Tool for Tracing Operating System Events," *Proceedings, 20th Annual Workshop on Microprogramming*, Colorado Springs, Colorado, December 1987.

Melvin, S., Wilson, J., Shebanow, M., Hwu, W. and Patt, Y., "On Tuning the Microarchitecture of an HPS Implementation of the VAX," *Proceedings, 20th Annual Workshop on Microprogramming*, Colorado Springs, Colorado, December 1987.

Melvin, S., and Patt, Y., "A Microcode-Based Environment for Non-invasive Performance Analysis," *Proceedings, 19th Annual International Workshop on Microprogramming*, New York, October 1986.

Gee, J., Melvin, S., and Patt, Y., "The Implementation of Prolog via VAX 8600 Microcode," *Proceedings, 19th Annual Workshop on Microprogramming*, New York, October 1986.

Patt, Y., Melvin, S., Hwu, W., Shebanow, M., Chien, C., and Wei, J., "Run-Time Generation of HPS Microinstructions from a VAX Instruction Stream," *Proceedings, 19th Annual Workshop on Microprogramming*, New York, October 1986.

Patt, Y., Hwu, W., Melvin, S., Shebanow, M., Chien, C., and Wei, J., "An HPS Implementation of VAX: Initial Design and Analysis," *Proceedings, 19th Hawaii International Conference on System Sciences*, Honolulu, Hawaii, January 1986.

Patt, Y., Shebanow, M., Hwu, W., and Melvin, S., "A C Compiler for HPS I, A Highly Parallel Execution Engine," *Proceedings, 19th Hawaii International Conference on System Sciences*, Honolulu, Hawaii, January 1986.

Patt, Y., Melvin, S., Hwu, W., and Shebanow, M., "Critical Issues Regarding HPS, A High Performance Microarchitecture," *Proceedings, 18th Annual Workshop on Microprogramming*, Asilomar, California, December 1985.

## **OTHER**

USPTO Registered Patent Agent

Named Inventor on 49 U.S. Patents

Professional Association Memberships:

The Institute of Electrical and Electronics Engineers (IEEE)

The Association for Computing Machinery (ACM)