



National Semiconductor

400103

National SCAN Databook

*IEEE 1149.1 Products
Design For Test With Boundary Scan*



SCAN

DATABOOK

1996 Edition

**Design for Test Solutions with
Boundary Scan**

Description of Boundary Scan

**Device Description and Characteristics
Loading Specifications, Waveforms,
Quality and Reliability**

Characterization Data

Boundary Scan Design Support

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National Semiconductor's SCAN Data Book offers Design for Test Solutions to improve R&D development cycle time, reduce test development and manufacturing cost and improve a customer's end system uptime. Designers, test engineers and engineering management using concurrent engineering practices will see life-cycle cost of ownership go down for systems designed with boundary scan.

The SCAN Family of IEEE 1149.1 (JTAG) compliant devices simplify integration of design and test.

SCAN Data Book

Product Index and Selection Guide

The Product Index is a numerical list of all device types contained in this book. The Selection Guide groups the products by function and by family.

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The Embedded Boundary Scan Controller, SCANPSC100F, allows creation of an on-board embedded test environment. It provides the interface from a target system's microprocessor and memory to the IEEE 1149.1 Test Access Port. The Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F Bridge, provides access to multiple boards within a system for simultaneous testing of like boards as well as system partitioning to better isolate test faults. SCAN EASE is a suite of software tools that enables test vectors to be embedded within an 1149.1 system; compiles and compresses vectors; controls and applies tests; reports failures; and includes a graphical user interface.

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Functional description of the ordering codes, package outlines, θ_{JA} information and Dry Pack handling procedures.

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

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SCAN Products Selection Guide

Function	Device	Bit-Width	Features
TRANSCEIVERS			
Non-Inverting	SCAN18245T	18-bit	• Dual Output Enable Control Signals • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP and HIGHZ Instructions • 9-Bit Data Busses for Parity Applications • TRI-STATE® Outputs for Bus-Oriented Applications • Reduced-Swing Outputs source 32 mA/sink 64 mA (Comm), and source 24 mA/sink 48 mA (Military) • Guaranteed to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V • TTL Compatible Inputs • 25 mil Pitch SSOP (Shrink Small Outline Package)
Non-Inverting	SCAN182245A	18-bit	• High performance BiCMOS technology ($t_{PD} < 4$ ns, typ) • 25Ω series resistors in outputs eliminate the need for external terminating resistors • Dual output enable control signals • TRI-STATE outputs for bus-oriented applications • 25 mil pitch SSOP (Shrink Small Outline Package) • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP, IDCODE and HIGHZ instructions
FLIP-FLOPS			
D	SCAN18374T	18-bit	• Buffered Positive Edge-Triggered Clock • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP and HIGHZ Instructions • 9-Bit Data Busses for Parity Applications • TRI-STATE Outputs for Bus-Oriented Applications • Reduced-Swing Outputs source 32 mA/sink 64 mA (Comm), and source 24 mA/sink 48 mA (Military) • Guaranteed to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V • TTL Compatible Inputs • 25 mil Pitch SSOP (Shrink Small Outline Package)
D	SCAN182374A	18-bit	• High performance BiCMOS technology ($T_{PD} < 4$ ns, typical) • 25Ω series resistor outputs eliminate need for external terminating resistors • Buffered positive edge-triggered clock • TRI-STATE outputs for bus-oriented applications • 25 mil pitch SSOP (Shrink Small Outline Package) • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP, IDCODE and HIGHZ instructions

Function	Device	Bit-Width	Features
LATCHES			
Transparent	SCAN18373T	18-bit	• Buffered Active-Low Latch Enable • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP and HIGHZ Instructions • 9-Bit Data Busses for Parity Applications • TRI-STATE Outputs for Bus-Oriented Applications • Reduced-Swing Outputs source 32 mA/sink 64 mA (Comm), and source 24 mA/sink 48 mA (Military) • Guaranteed to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V • TTL Compatible Inputs • 25 mil Pitch SSOP (Shrink Small Outline Package)
Transparent	SCAN182373A	18-bit	• High performance BiCMOS technology ($T_{PD} < 4$ ns, typical) • 25Ω series resistor outputs eliminate need for external terminating resistors • Buffered active-low latch enable • TRI-STATE outputs for bus-oriented applications • 25 mil pitch SSOP (Shrink Small Outline Package) • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP, IDCODE and HIGHZ instructions
LINE DRIVERS			
Inverting	SCAN18540T	18-bit	(Same Features of the SCAN18541T)
Non-Inverting	SCAN18541T	18-bit	• Dual output enable signals per byte • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP and HIGHZ Instructions • 9-Bit Data Busses for Parity Applications • TRI-STATE Outputs for Bus-Oriented Applications • Reduced-Swing Outputs source 32 mA/sink 64 mA (Comm), and source 24 mA/sink 48 mA (Military) • Guaranteed to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V • TTL Compatible Inputs • 25 mil Pitch SSOP (Shrink Small Outline Package)
Non-Inverting	SCAN182541A	18-bit	• High performance BiCMOS technology ($T_{PD} < 4$ ns, typical) • 25Ω series resistor outputs eliminate need for external terminating resistors • Dual output enable signals per byte • TRI-STATE outputs for bus-oriented applications • 25 mil pitch SSOP (Shrink Small Outline Package) • IEEE 1149.1 (JTAG) Compliant • Includes CLAMP, IDCODE and HIGHZ instructions

Function	Device	Features
SYSTEM SUPPORT		
Embedded Boundary Scan Controller	SCANPSC100F	• Compatible with the IEEE Std. 1149.1 (JTAG) Test Access Port and Boundary Scan Architecture • Interfaces up to Two 1149.1 Scan Rings • Fabricated in FACT™ 1.5μ CMOS Process • Generic Parallel Interface Synchronizes Processor Signals with the SCANPSC100F Operation Clock, SCK • 16-Bit Serial Signature Compaction (SSC) at the Test Data in (TDI) Port • Automatically produces Pseudo-Random Patterns at the Test Data Out (TDO) Port • 25 MHz Operation • TTL Compatible Inputs, Outputs are Full-Swing CMOS with 24 mA Source/Sink Capability
Hierarchical and Multidrop Addressable JTAG Port	SCANPSC110F	• True IEEE1149.1 Hierarchical and Multidrop Addressable Capability • The 6 Slot Inputs Support Up to 59 Unique Addresses, a Broadcast Address, and 4 Multi-cast Group Addresses • 3 IEEE 1149.1-Compatible Configurable Local Scan Ports • Mode Register Allows Local TAPs to be Bypassed, Selected for Insertion into the Scan Chain Individually, or Serially in Groups of Two or Three • 32-bit TCK Counter • 16-bit LFSR Signature Compactor • Local TAPs Can Be TRI-STATE Via the $\overline{OE}$ Input to Allow an Alternate Test Master to Take Control of the Local TAPs
SCAN Embedded Application Software Enabler	SCAN EASE	• Processor independent—runs on big/little endian and memory- and I/O-mapped architectures • Compatible with Teradyne VICTORY™ ATPG and JTAG Technology BTPG™ tools (others supported upon request) • Provides automated translation, application and evaluation of ATPG-generated tests in an embedded system environment • Includes a Scan Function Library and National's Embedded Boundary Scan Controller SCANPSC100F device driver to support custom or non-ATPG generated vector applications • Supports embedded test data log for diagnostic processing • Includes Microsoft Windows GUI and serial communication tool for system administration and remote testing • Supports SCANPSC110F Hierarchical and Multidrop JTAG Addressable Port architecture



Section 1
**Design for Test Solutions
with Boundary Scan**

1



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Design for Test Solutions with Boundary Scan

What is DFT?

Design for Test, or DFT, is being used by many companies to lower the overall cost of development, manufacturing, test and field service. Some companies call it "Concurrent Engineering" and it replaces the "Over-the-wall" method of product development. In each stage of the product life-cycle, a consideration for testing is made in the earliest stages of design.

National employs boundary scan technology to enable not just chip testing, but also board testing, system testing, and in-field service testing.

What is the standard? For most purposes the following terms are used interchangeably:

- IEEE 1149.1
- 1149.1
- JTAG
- Dot 1
- Boundary Scan
- SCAN

IEEE 1149.1 is a set of standards for *board* test protocol. Newer standards are being developed by different IEEE working groups for *system* test and *analog* test protocol. IEEE 1149.1 is a 4-wire standard which allows compliant silicon to perform interconnect testing. It supports BIST (Built In Self-Test), and provides an alternative or supplement to Bed of Nails testing and functional testing.

Adding boundary scan to a board does add cost and time to the design cycle due to the increased cost of boundary scan compliant components and initial time investment required to understand the boundary scan architecture and tools. However, these costs are easily justified when viewing the benefits and cost savings boundary scan provides at every stage of a product's life cycle. What was originally developed as a manufacturing test tool offers benefits before, during and after manufacturing.

Board Development

A designer uses boundary scan to save time during the prototyping and design debug stage. With boundary scan, non design-related, structural faults can be detected and then eliminated at both the board level and component level. This allows designers to effectively locate and resolve design related problems. Additionally, designers use boundary scan to partition a board, load seed values for devices (e.g. internal scan, LSSD, etc.) to isolate logic errors. With boundary scan, many of the vectors developed and used during the design phase can be passed on to manufacturing to provide an additional cost and time savings.

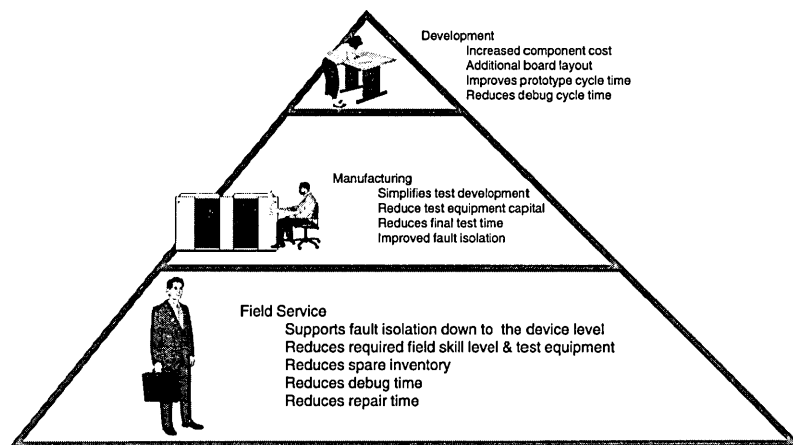


FIGURE 1. Boundary Scan Benefits Entire Product Life Cycle

TL/F/11587-5

Board Manufacturing

The key benefits at the manufacturing phase are test development time savings; improved fault coverage and diagnosis; and improved test throughput through reduced test times. As with the design phase, boundary scan provides the additional advantage of applying many of the vectors used for manufacturing to be later applied during field debug and diagnosis.

Field Service

Field failures are often due to structural failures which surface due to the stress—temperature, humidity, vibration—that the boards are exposed to in the field environment. Using boundary scan, field technicians have the ability to quickly test for structural faults down to the component level without the burden of probing or returning the board to the factory. Eliminating these tasks allows for more efficient diagnosis and repair which reduces cost and system downtime.

The advantage of boundary scan become even more apparent when boundary scan is extended from the board level to the system level test.

Often, the objection to the use of boundary scan include:

1. Performance (speed) decreases due to the extra delay added by the boundary scan multiplexer in the data path.
2. Cost increases due to additional silicon and TAP pins on the device package—as well as design time.
3. Delay to market due to additional circuit design time.

However, the manufacturing benefits as well as product development cycle time improvements easily outweigh the initial added efforts.

Using boundary scan on their 80486 design, Intel realized two orders of magnitude improvement in time to develop circuit test-patterns with significant cost reduction, too. See *Figure 2*.

Boundary scan provides cost savings over the life cycle of a system in the testing of boards, systems, and in field maintenance.

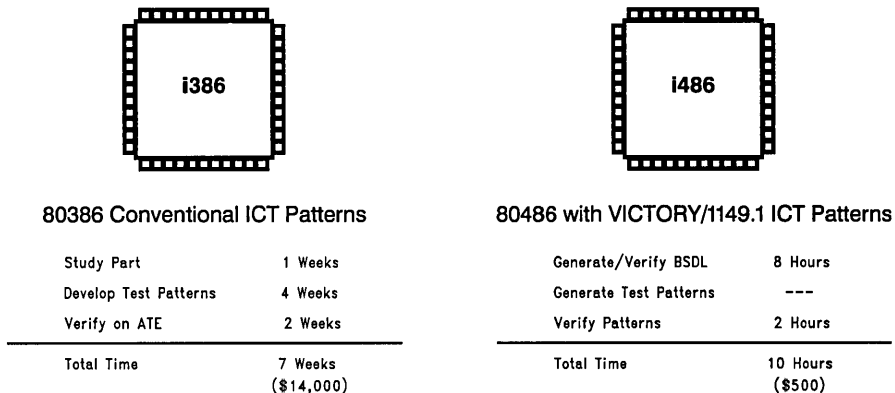


FIGURE 2. Intel Reduced Test Development Time and Test Cycle Time

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The Economics of Design for Test

Many of the perceived costs of a DFT strategy fall upon the design organization, while many of the benefits reward the manufacturing and test organizations. This adversarial position can be eliminated by meeting the needs of all organizations involved in DFT.

EFFECT OF DFT BY DEPARTMENT

Design	Die Area	Increased Cost
	Design Cycle Time	Lowered Cost
	Performance Impact	Increased Cost
	EDA Tools	Increased Cost
Test	Fault Simulation	Lowered Cost
	Simplified Debug & Diagnostics	Lowered Cost
	Fewer Design Changes	Lowered Cost
	Lower ATE Cost	Lowered Cost

IMPACT OF DFT VARIABLES BY DEPARTMENT

Profit Factor	Department	Impact
Units Sold	Design	New product feature, faster design cycle time
	Marketing	Lower selling price through cost reduction
	Sales	Lower selling price
Selling Price	Design	New product features
	Marketing	of higher quality
	Sales	
Variable Cost	Marketing	Higher cost of silicon,
	Sales	lower overall
	Manufacturing	manufacturing costs
Fixed Cost	Design	
	Manufacturing	Lower cost ATE, more productive ATE (higher throughput), improved fault coverage
	Field Service	Less field spare inventory, faster debug and diagnosis
Total Profit	Management	Overall investment strategy, capital utilization, ROA, cost calculation methods

Boundary scan also provides cost savings which can be measured directly in production and can reduce the time to market. This method fits within a concurrent engineering environment in various ways:

- Reduces test time and costs
- Reduces test preparation time and costs
- Increases the time available for test programs for production
- Allows simpler, less costly testers
- Shortens diagnostic times
- Provides a commonality of tester interface
- Allows the continued test of high density/poor-access boards

Where the Failures Are

PCB test failures can result from either structural faults (opens, stuck-at's, bridging, missing/wrong components, etc.), analog failures (faulty or incorrect passive components) or performance faults (timing problems or board/component design errors). However, structural faults account for the overwhelming majority of board failures during manufacturing test. In fact, data from Teradyne, a leader in the test industry, suggests that greater than 80% of the board level test manufacturing failures are structural in nature. See *Figure 3*.

Where the Failures Are (Continued)

A number of methods have been implemented to provide a means of detecting structural failures. These methods range from use of functional board testers (FBT) to in-circuit testers (ICT) and combinational (ICT and FBT) testers. Boundary scan was created to provide an improved technique for screening structural faults through reduced test programming time and improved fault coverage.

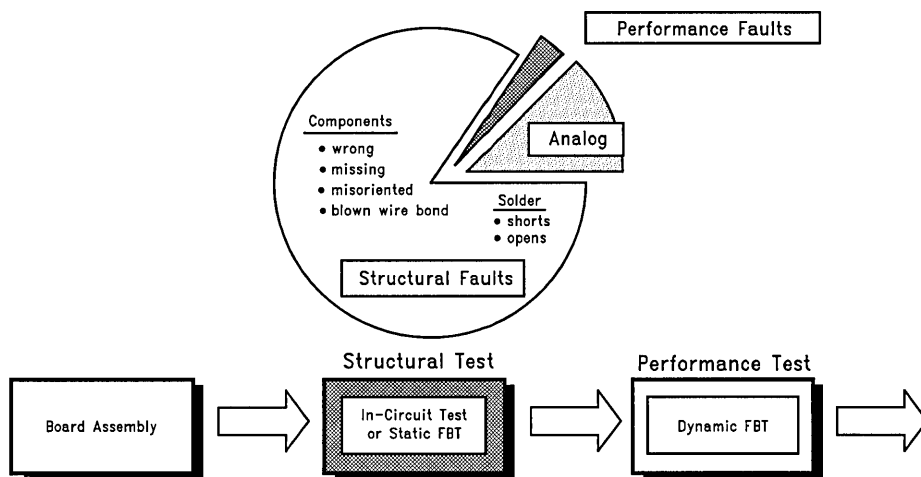
It should be noted that boundary scan is not a technique for detecting at-speed, dynamic performance faults. Performance fault testing requires the use of an at-speed functional board tester. With very thorough debug and simulation during board development and pre-assembly test of board components, the need for performance fault testing during manufacturing is up to the discretion of the board manufacturer and its customers. Even if at-speed functional testing is required, the use of structural testing prior to functional testing will help eliminate manufacturing defects and ease the diagnosis of performance or functional failures.

For the cases where access is possible, the access occurs at a price. Even if it is possible to add test pads, pads consume board area—contrary to the goal of saving board

area—and can present performance degradation. Additionally, the cost increases substantially for test point fixtures, the fine tip probes or clam shell probes for double sided boards. See *Figure 4*.

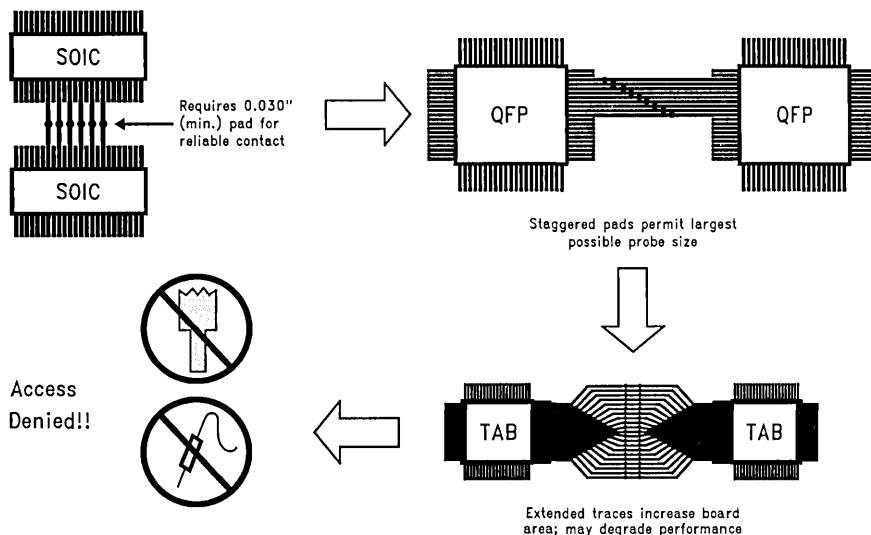
For the case of MCMs (multi-chip modules) and inaccessible board nodes (nodes under a mezzanine card, blocked by a component or other hardware, etc.), access is not possible and the only option other than boundary scan is cluster testing: using bed of nails to apply stimulus on MCM or board cluster inputs and measure values at outputs of the MCM or board cluster. This creates the same burdens as when using a FBT, where creating test vectors requires knowledge of the entire MCM or board cluster functionality which increases test development, diagnostics and test time.

The existence of inaccessible nodes in manufacturing are passed on to the field service engineer attempting to use manual probing as a vital step in debugging a board failure. This leads to increased field service time and costs and, longer system down time for your customer.



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FIGURE 3. The Majority of Printed Circuit Board (PCB) Manufacturing Failures Are a Result of Structural Faults



TL/F/11587-8

FIGURE 4. Device Packaging Density Makes Physical Access Expensive, Unreliable, or Impossible

Boundary Scan Fundamentals

The IEEE 1149.1 standard defines a 4 pin TAP (Test Access Port) which allows electrical access around the "boundary" of compliant devices. The TAP pins are:

TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
TCK	Test Clock

It also defines a 16 state TAP Controller and several registers used to control the test data.

Boundary scan registers are placed at all I/O pins, and they are interconnected to form a serial chain around the core functionality of the device.

With the addition of the boundary scan registers at the I/O of a component, interconnect testing with boundary scan devices can be performed with no dependence on device functionality. IEEE 1149.1 compliant automatic test program generation (ATPG) tools are available from a number of vendors to automatically generate interconnect tests using a board netlist and BSDL files for each 1149.1 compliant device on the board as inputs. BSDL files provide a description of the specific implementation of boundary scan features within each compliant component.

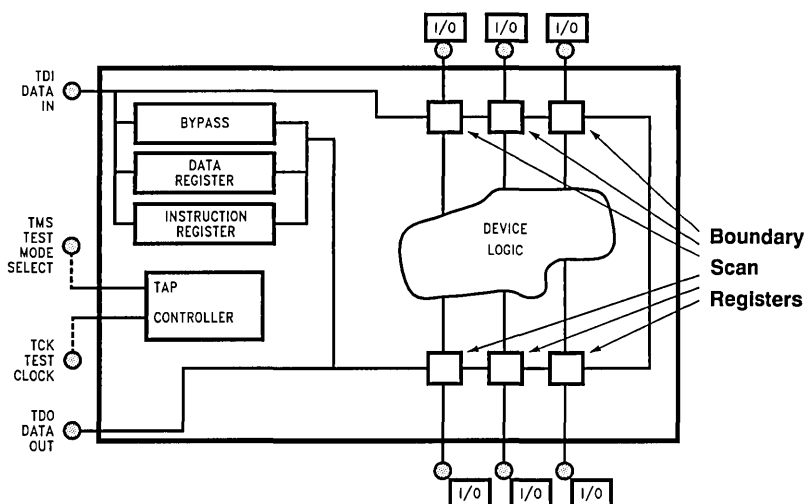


FIGURE 5. 1149.1 Device Hardware

TL/F/11587-9

In like fashion as the chip, the boundary scan chain is extended to the board in a serial scan chain. Boards in systems can also be linked in a scan chain.

When placed on a printed circuit board, each 1149.1 component is connected together to form a chain of boundary scan devices. In *Figure 6*, note the scan chain connections:

TDI/TDO: The tester's serial test data out pin is connected to the first device's TDI. The test data is passed from the first device to the second device via the TDO pin which connects to the second device's TDI pin. This chain formation continues until the last device's TDO pin is connected back to the tester. Therefore, shifting data into a device's instruction or data registers requires that the data passes through every JTAG device which is connected ahead of the device in the scan chain. Additionally, as the data is shifted into the device, the data previously stored in the selected instruction or data register is shifted out of the chain. The tester software either reads and evaluates the returning data or masks it out. The Bypass register is included to shorten the chain when shifting data through devices which are not participating in a given scan operation.

TCK/TMS: All devices in the chain are connected in parallel to the TCK and TMS signals. This means that all the devices' TAP controllers are in the exact same state and transition simultaneously. The instruction register allows each device to include different data registers in the scan chain and perform different scan operations.

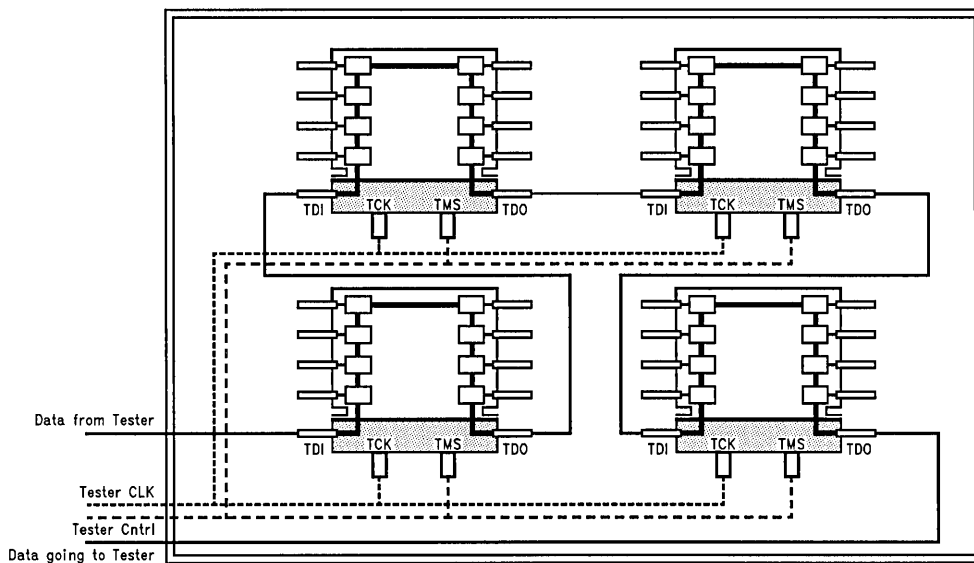


FIGURE 6. 1149.1 Boundary Scan Chain

TL/F/11587-10

Implementing boundary scan on every component on the board provides the maximum benefit in terms of reduced tester cost, test development times and concurrent engineering. However, boundary scan can also complement an ICT in testing structural faults. See *Figure 7*. This was fully recognized by ICT tester companies when they developed their ICT systems and most ICT's now have a connector dedicated for boundary scan testing. Additionally, these tester companies included the option of mixing boundary scan and ICT in their ATPG tools by using ICT component libraries for non-scan products and BSDL for scan products. For example, vectors can be automatically generated to drive signals with boundary scan and compare results using physical test probes. Many companies have already invested millions of dollars in ICTs and may want to use boundary scan only where required for inaccessible nodes, non-library parts, etc. or as a means of cutting ICT fixture costs.

For smaller companies or companies in the process of purchasing new ICT equipment, implementing boundary scan may provide a way to reduce the required ICT features like number of channels providing a tremendous reduction in the tester cost where cost ranges from \$200K up to \$1M.

Figure 7 shows two examples of ICT and boundary scan working together. The lower of the two graphics shows cluster testing. Cluster testing is the testing of a group of devices by applying data to the inputs of the group or cluster and evaluating the results on the output of the group or cluster. Cluster testing can vary from testing the interconnects between the components in the cluster to testing the internal nodes of each component within the cluster.

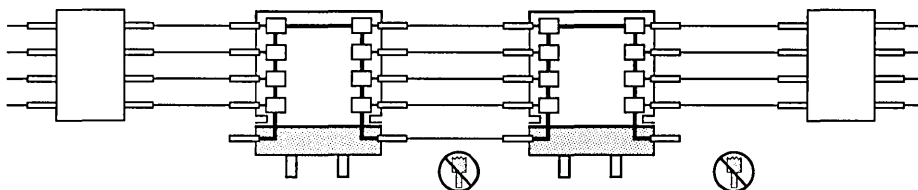
System Test

National supports the needs of the system design architect by:

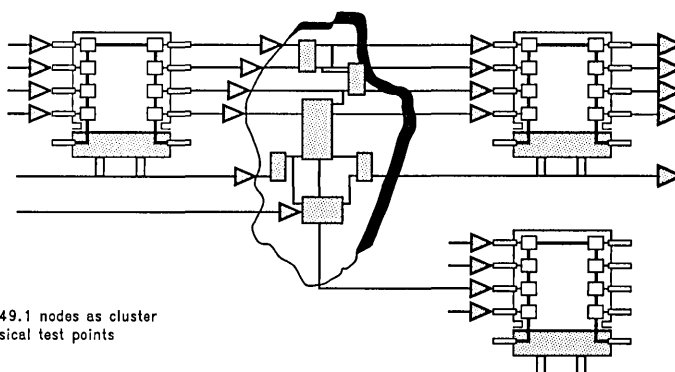
- Acknowledging the need for live insertion on the backplane
- Fully complying to IEEE 1149.1 (board test)
- Addressing the 1149.5 standard (system test)

While boundary scan diagnostics are particularly useful for telecommunications and workstations, their benefits also extend to board manufacturers that want to reduce the time-to-market of their products.

For small companies, we provide the option to expensive \$1 million test equipment. With help from our software and hardware partners (such as Corelis and JTAG Technologies), National can support total system test solutions with PC-based boundary scan devices, software, and hardware solutions.



Boundary scan works with an ICT to provide access to inaccessible nodes and/or to reduce ICT physical test points



Treating non-IEEE 1149.1 nodes as cluster can eliminate ICT physical test points

FIGURE 7. Boundary Scan and ICT Can Work Together

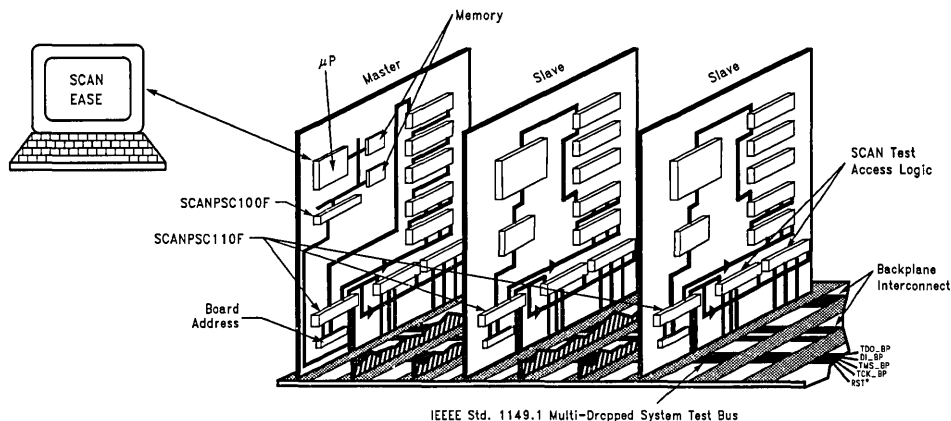
TL/F/11587-11

HOW IT WORKS

For system test and diagnostics, start with the Embedded Boundary Scan Controller, SCANPSC100F and your choice of microprocessor and memory to create an embedded test master, freeing up external test equipment.

Add the Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F Bridge to each board in the multidrop or hierarchical backplane to address any number of boards, selectively or in groups, for board test as well as backplane interconnect failures. If a board is off-line or removed, the scan chains remain unbroken.

But what if a board is removed while powered up? Then add SCAN ABT Test Access Logic along the back-plane card edge to provide fault-tolerant power-up and power-down live insertion. Now backplane interconnect checks can be performed and boards inserted/removed through controlled power-up/power-down sequences. The 25 Ω series resistors on SCAN ABT outputs also eliminates the need for an external damping resistor.



- SCAN EASE Compatible with 1149.1 hardware and existing test board vectors
- SCANPSC100F creates embedded test master
- SCANPSC110F enables individual board addressing, multiple and hierarchical boards for testing "like" boards simultaneously
- SCAN ABT live insertion

TL/F11587-16

FIGURE 8. Creating Embedded System Test

System-Level Embedded Test

Developing hardware and software to implement embedded test capability can be significant in terms of both time and expense. To reduce our customers' in-house software development efforts, National offers SCAN EASE to apply, control, and evaluate tests within an IEEE 1149.1-compliant embedded system. For more examples refer to AN-1022, Boundary-Scan, An Enabling Technology for System Level Embedded Test.

SCAN EASE TOOLS

SCAN EASE (Embedded Applications Software Enabler) is a suite of software tools that enables ATPG (Automatic Test Program Generation) or custom-generated test vectors to be embedded within an IEEE 1149.1 compatible system. See Figure 9. SCAN EASE includes three groups of tools:

- EmbedPrep
- EmbedTest
- EmbedComm

TEST DEVELOPMENT PROCESS

The test development process for embedded system test begins with generating tests using an off-the-shelf ATPG tool. See Figure 10. Separate tests are created for each board type in the system during manufacturing test development. These tests can be re-used for embedded test. National's SCAN EASE includes tools to compile test vectors

stored in Serial Vector Format (SVF) or Pattern Format (PAT) into Embedded Vector Format (EVF) for use with EmbedTest. EVF is a compact binary vector format suitable for embedded applications. Several of the board-level EVF files can be concatenated to create a system-level test. Partitioning tests enables EmbedTest to isolate and report pass/fail information to the partition level (board, module, etc.) without running diagnostic software. EVF test files can be located in ROM for power-up self test or down loaded to RAM.

EmbedTest provides a set of functions that enable communication between the embedded system and a serial interface to a system administrator or remote computer. EmbedTest commands—such as configuration, reporting test results, downloading new tests, and uploading data logs—are performed over this interface.

Note that SCAN EASE is also included in our SCAN Developer/Demo Kit. This kit demonstrates system board check, interconnect testing, and backplane testing (see Figure 8). Included are:

- Embedded Boundary Scan Controller—SCANPSC100F works with customer's choice of microprocessor
- Multidrop and Hierarchical Addressable JTAG Port SCANPSC100F SCAN Bridge for system test—addresses any number of boards in the backplane
- SCAN ABT Test Access Logic—provides live insertion capability for boards along the backplane

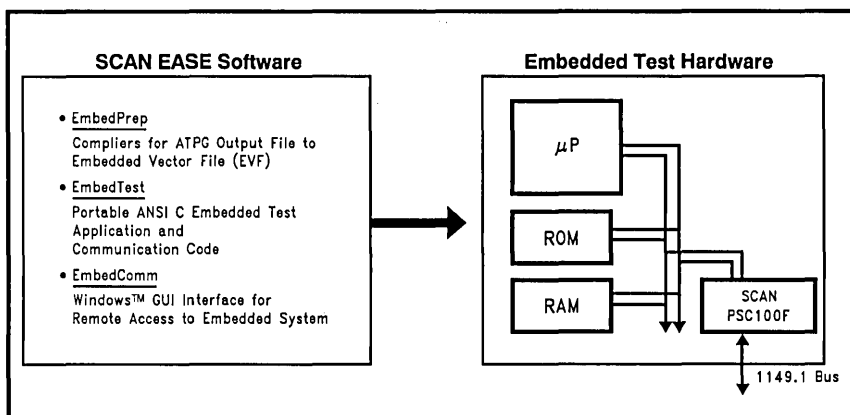


FIGURE 9. SCAN EASE Enables ATPG Test Vectors to be Embedded

TL/F/11587-14

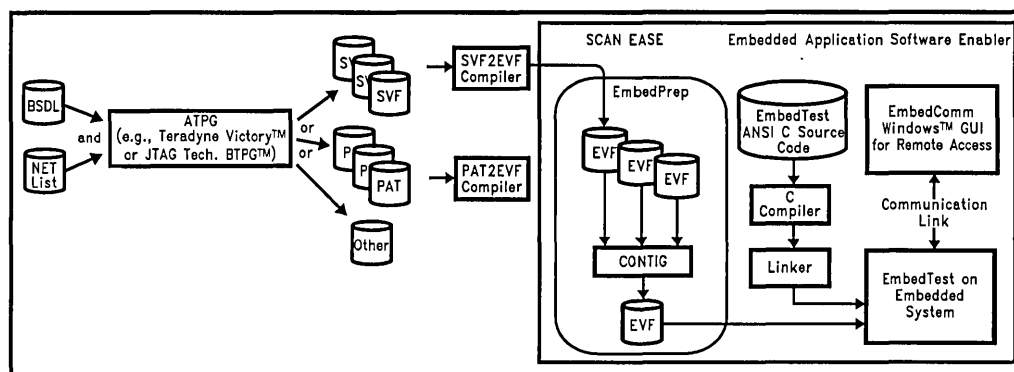


FIGURE 10. SCAN EASE Reuses Existing Test Vectors, Compiles them for your Target Microprocessors and Compresses them for Storage in Memory

TL/F/11587-15

The Impact of PC and Communications Technology

The market is ripe for the valuable services provided by PC-based and in-system testing. Having a system perform its own self-test upon power-up frees up design engineers to add more features to an end system, as opposed to spending money on testing a system. With advances in PCs, the capability of remote testing now exists. It is possible to dial up a modem service, connect to a remote system in the field and perform maintenance, improving the end-system uptime. Once the target site is on-line, the system performs self-testing and reports back failures.

There are many factors associated with improving end-system uptime including systems that require high reliability, systems that perform services for large groups of people or customers that need to stay on-line all the time. Initially SCAN EASE will diagnose the problem for the purpose of repair. Since vectors are stored in ROM, it will be easy to download system upgrades and new system configurations in the near future.

Recent applications have arisen to extend the use of IEEE 1149.1 boundary scan all the way to system integration and field service. This new arena boasts additional leverage for the re-use of test vectors, improved time to break-even for products and increased value to end-users.

What products will result from this technology? A tester on a chip will go into simple machines that give people trouble like printers, copiers, facsimile machines, and give them the intelligence to do power-on self-test, diagnosis and repair. The machine will be able to call the home office through advanced communications capabilities, communicate with the home office, literally saying, "This is what is wrong with me." Remote verification of the diagnosis as well as repair can then take place.

On an even wider scale, telecommunications equipment buried in remote locations will be accessible. Board will be tested, brought off-line, and others brought on-line to replace them—electronically and remotely.



Section 2

Description of Boundary Scan



Section 2 Contents

Boundary-Scan Circuitry	2-3
Boundary-Scan Registers	2-4
Boundary Scan Overview	2-5

Description of Boundary-Scan

Boundary-Scan Circuitry

The scan cells used in the Boundary-Scan register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10-11* for a further description of scan cell TYPE1 and *Figure 10-12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals see *Figure 1*. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

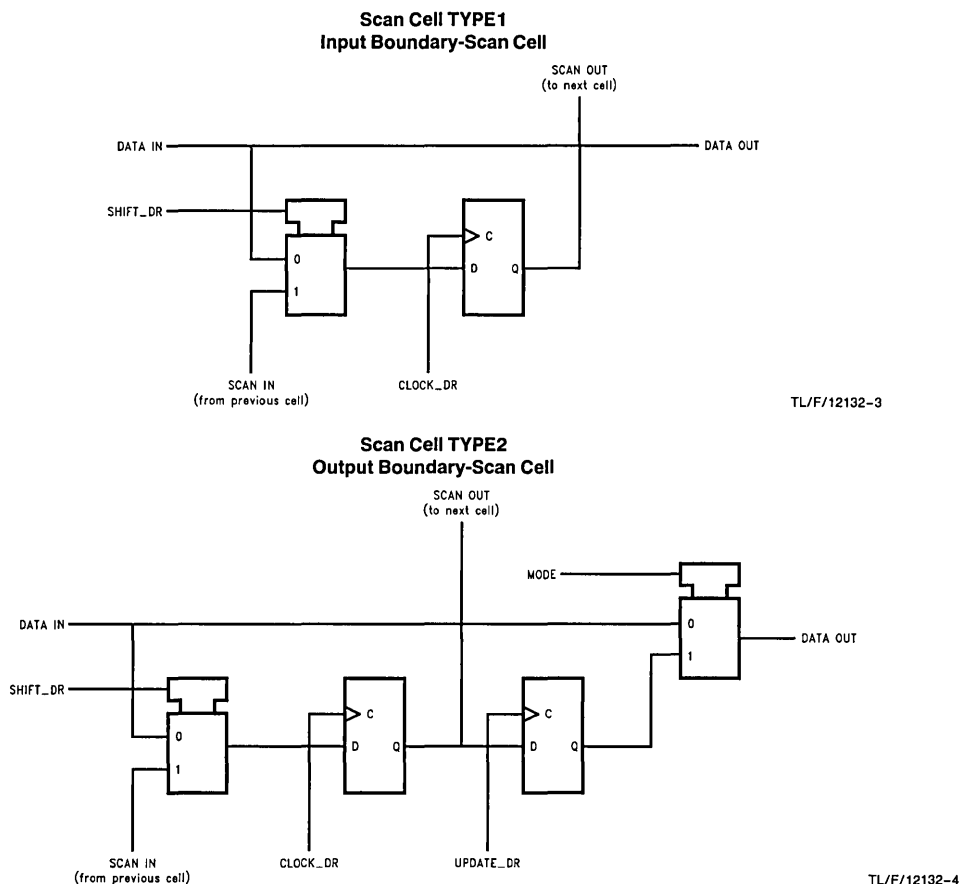
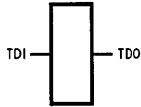


FIGURE 1. Type 1 and Type 2 Scan Cells are Located at Input and Output Pin, Respectively

Boundary-Scan Registers

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Logic 0



TL/F/12132-1

FIGURE 2. Bypass Register Scan Chain Definition

TABLE Ia. Scan ABT Product IDCODE
(32-Bit Code per IEEE 1149.1)

Device	Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
SCAN182245A	0000	111111	0000000000	00000001111	1
SCAN182373A	0000	111111	0000001000	00000001111	1
SCAN182374A	0000	111111	0000000111	00000001111	1
SCAN182541A	0000	111111	0000001001	00000001111	1

MSB

LSB

TABLE Ib. SCAN CMOS Device Identification
(8-Bit Code Described in Device BSDI)

Device	8-Bit Code
SCAN18245T	00111101
SCAN18373T	00101101
SCAN18374T	00011101
SCAN18540T	01001101
SCAN18541T	10111101

Scan ABT devices include the 32-bit 1149.1-compliant IDCODE as shown in Table Ia. Scan CMOS devices do not include the IDCODE, however they do have an 8-bit device identification code which is described in its device BSDI model and shown in Table Ib.

Tables IIa, IIb and IV show which instructions are included for SCAN ABT and SCAN CMOS.

The INSTRUCTION register *Figure 3* is an 8-bit register which, for SCAN ABT, captures the default value of 10000001 (SAMPLE/PRELOAD, Table IIa) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is not required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction.

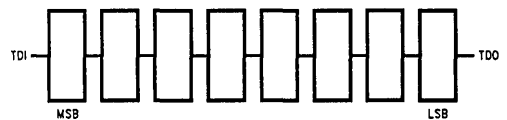
In the case of SCAN CMOS, the 8-bit INSTRUCTION register captures the device's 8-bit identification code in Table Ib. For more information refer to the section on instruction definitions.

TABLE IIa. SCAN ABT Instruction Registers

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

TABLE IIb. SCAN CMOS Instruction Register

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All Others	BYPASS



TL/F/12132-2

FIGURE 3. Instruction Register Scan Chain Definition

Boundary Scan Overview

This document is a supplement to the National Semiconductor SCAN Test Access Logic products datasheets. It provides an overview of the IEEE 1149.1 (boundary scan) circuit features included on the National's SCAN devices. The IEEE 1149.1 Std. document should be consulted for more detailed information about the IEEE 1149.1 standard requirements.

The IEEE 1149.1 boundary scan standard circuitry is comprised of 3 functional blocks—a test access port (TAP), a TAP controller and a set of registers.

I. TEST ACCESS PORT (TAP)

The Test Access Port (TAP) consists of four pins dedicated solely to the operation of the test logic. The four pins include TMS (Test Mode Select), TDI (Test Data In), TDO (Test Data Out), and TCK (Test Clock). These products contain a power-up reset function in lieu of adding the TRST pin. The motivation of this option is to save package size and hence customer board space, thus making the decision to implement 1149.1 less costly to the system designer.

TCK: This input provides the test clock for the test logic defined by the IEEE 1149.1 Standard. In accordance with the standard requirements, all test logic will retain its state indefinitely upon stopping TCK at a logic low, or 0. Additionally, the same retention may occur upon stopping TCK at a logic high, or 1, which is a permission granted by the standard. The motivation for TCK to be a dedicated test input is 1) to insure that it can be used independently of system clocks running at different frequencies, 2) that it permits shifting of test data without altering any system logic state when undertaking on-line system monitoring tasks, and 3) that it can be used to test all board interconnect even when that interconnect transfers clock signals from one device to another.

TMS: This input is the command signal to control system operation modes. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. The requirement that an unforced TMS input produce a logic high is to ensure that the normal operation of the design can continue without interference from the test logic by guaranteeing that an undriven TMS input can put the TAP Controller into the Test Logic Reset state.

TDI: This signal provides the serial data input of test instructions and data to the test logic. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. Test data will arrive at TDO without inversion after the appropriate number of clock cycles as determined by the length of the register currently connected between TDI and TDO. The requirement that an unforced TDI input produce a logic high is to assist in the determination of manufacturing defects in the test scan chain interconnect. A consistent field of 1's in shifting out the data registers can indicate where a break in the scan chain interconnect occurred.

TDO: This signal provides the serial data output of test instructions and data from the test logic. Changes in the logic state and drive activity for this output occur upon the falling edge of TCK. This is to avoid a race condition when TDO is connected to TDI of the next chip in the scan chain which is sampled on the rising edge. This output shall remain inactive except when the scanning of data is in progress. This is to permit the ability to multiplex scan chains on the board without causing signal contention between multiple TDO outputs connected together to form parallel scan chains.

II. TAP CONTROLLER

The TAP controller is a 16 state finite state machine which controls the insertion of the data and instruction registers (described later in this document) between TDI and TDO pins, and controls the flow of data through these registers.

Changes in the state of the TAP Controller (see *Figure 4*) are solely a response to the value of TMS upon the rising edge of TCK, or upon power-up (or the application of a logic low to the optional TRST input which is not included in the products referring to this document). In any given state actions of the test logic taken in that state occur on the falling or rising edge of TCK following the rising edge of TCK which caused the TAP Controller to enter the state initially.

Note: It may happen that actions to occur in one state happen on the same rising edge of TCK that cause the TAP Controller to enter the next state.

Test Logic Reset: In this state, the boundary scan test logic is disabled to allow the device to function normally. All boundary scan registers are reset to their default states. This state is entered by at most, five TCK cycles while holding TMS high or asynchronously by pulling TRST low (if TRST pin is included). The IEEE 1149.1 standard requires that an internal pull-up be included on the TMS pin to assure the TAP will return and remain in test logic reset if TMS is floating.

Run Test/Idle: This state provides a dual purpose depending on the active instruction. It is included to allow for optional or user defined tests, including BIST, to be performed. For the required IEEE 1149.1 instructions, all test data registers retain their current state (i.e., remain idle).

SELECT-DR Scan: This is a temporary state in which all test data registers retain their previous values.

Capture-DR: In this controller state data may be parallel loaded into the data register selected by the current instruction; otherwise, it retains its previous values.

SHIFT-DR: In this state the test data register selected between TDI and TDO by the current instruction will shift one stage at each rising edge of TCK. TDO is active during this state. Test data registers not selected by the current instruction maintain their previous values.

Exit1-DR: This is a temporary state in which all test data registers retain their previous values.

PAUSE-DR: This is a temporary state in which all data registers retain their previous values. This state is intended to temporarily halt the shifting of test data into the data register selected while retaining the ability to keep TCK running; TCK may be a free-running clock. This state is often used to load additional test vectors from external memory.

Exit2-DR: This is a temporary state in which all test data registers retain their previous values.

UPDATE-DR: The parallel output register of the selected test data register may be updated on the falling edge of TCK in this state, provided the test data register has such a parallel output register. The intent of the parallel output register is to provide the ability to apply the contents of the test data registers to the test logic simultaneously rather than applying it as it is being shifted in. All test data registers not selected by the current instruction retain their previous values.

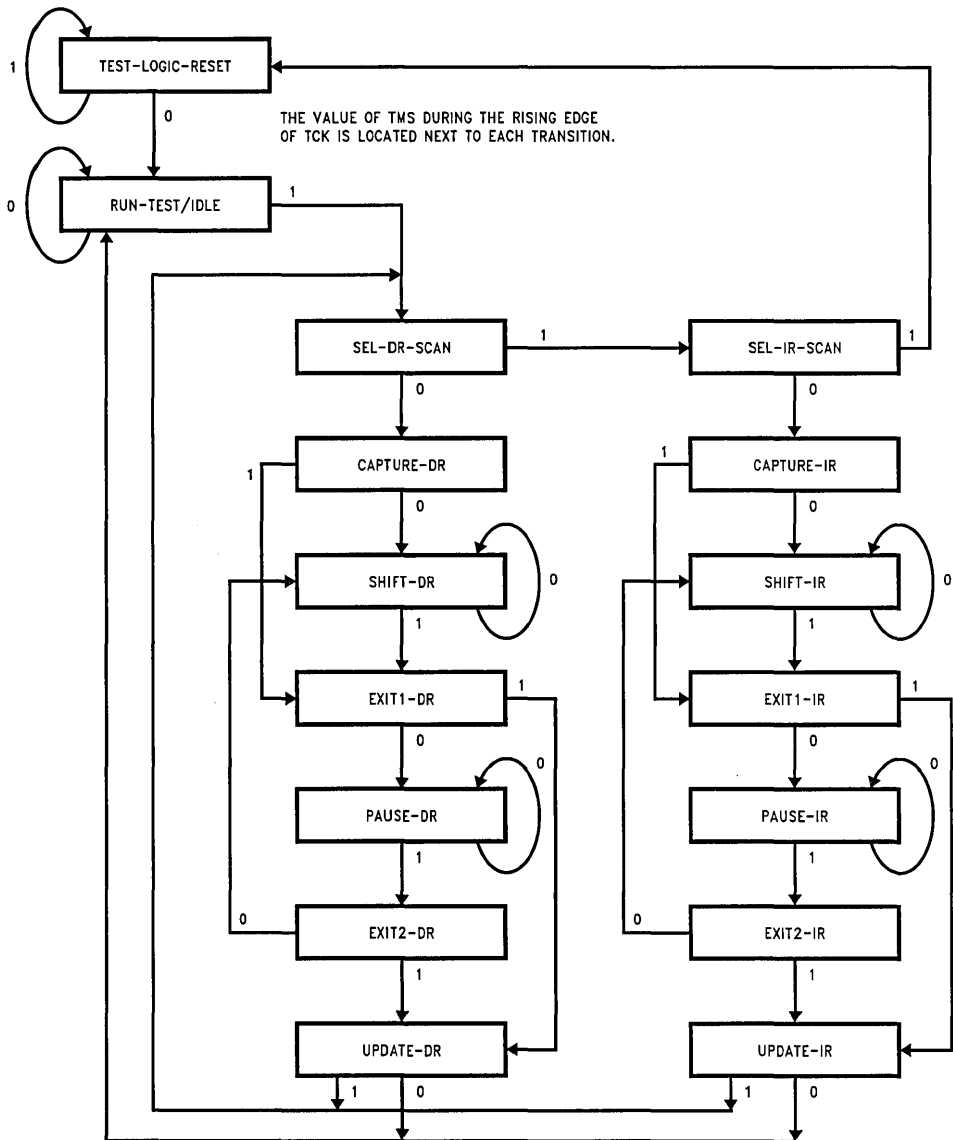


FIGURE 4. TAP Controller State Diagram

TL/F/12132-18

SELECT-IR Scan: This is a temporary state in which the INSTRUCTION register retains its previous value.

Capture-IR: In this controller state, a fixed value must be parallel loaded into the INSTRUCTION register. The only restriction on what that data may be is that its least significant bit must be a logic high, or 1, and its second least significant bit must be a logic low, or 0. These opposite state bits can be used to check the correct operation of the scan chain on the board by forcing a bit toggle when the instructions are shifted.

SHIFT-IR: In this state the INSTRUCTION register selected between TDI and TDO will shift one stage at each rising edge of TCK. TDO is active during this state.

Exit1-IR: This is a temporary state in which the INSTRUCTION register retains its previous value.

PAUSE-IR: This is a temporary state in which the INSTRUCTION register retains its previous value. This state is intended to temporarily halt the shifting of test data into the INSTRUCTION register while retaining the ability to keep TCK running. This state is often used to load additional test vectors from external memory.

Exit2-IR: This is a temporary state in which the INSTRUCTION register retains its previous value.

UPDATE-IR: The parallel output register of the INSTRUCTION register will be updated on the falling edge of TCK in this state. The intent of the parallel output register is to provide the ability to apply the contents of the INSTRUCTION register to the test logic simultaneously rather than applying it as it is being shifted in.

TDO OUTPUT ACTIVITY

Control of the TDO output buffer follows Table III.

TABLE III. TDO Output Buffer Control

Controller State	Register Selected between TDI and TDO	TDO Driver
Test Logic Reset	BYPASS	Inactive
Run Test/Idle	BYPASS	Inactive
SELECT-DR Scan	**	Inactive
SELECT-IR Scan	INSTRUCTION	Inactive
Capture-IR	INSTRUCTION	Inactive
SHIFT-IR	INSTRUCTION	ACTIVE
Exit1-IR	INSTRUCTION	Inactive
PAUSE-IR	INSTRUCTION	Inactive
Exit2-IR	INSTRUCTION	Inactive
UPDATE-IR	INSTRUCTION	Inactive
Capture-DR	**	Inactive
SHIFT-DR	TEST DATA	ACTIVE
Exit1-DR	**	Inactive
PAUSE-DR	**	Inactive
Exit2-DR	**	Inactive
UPDATE-DR	**	Inactive

Note: ** = Data register selected depends on currently active instruction.

FEATURES OF THE TAP CONTROLLER

The TAP Controller will not be initialized by the operation of any system pin such as a system reset. The TAP Controller will be initialized into the Test Logic Reset state upon power-up. This requirement is intended to avoid bus signal contention upon system power-up by disabling the test logic

which allows the system logic to operate normally and hence be controlled to avoid any contention. (The TAP Controller will return to the Test Logic Reset state after, at most, five clock cycles of TCK with TMS high; but the time required to enact that operation may not be sufficient to avoid contention.)

Note that the TAP Controller has been defined such that six of the sixteen states have the ability to maintain their state provided that TMS remains at the same value it had when entering the state. Those states include Test Logic Reset to hold off the test logic during normal system operation, Run Test/Idle to undertake multi-cycle self tests, SHIFT-DR and SHIFT-IR to maintain the data shifting process for an extended period, and PAUSE-DR and PAUSE-IR to halt the shifting process while some other activity is performed such as retrieving test data from additional memory. This feature is available in any/all states where multiple clock cycles may be required to achieve the desired outcome or where activity is to be halted but still provide the ability to make TCK a free-running clock.

III. BOUNDARY SCAN REGISTERS

INSTRUCTION REGISTER

The INSTRUCTION register permits specific commands to be shifted into the design to select a particular test data register and/or a specific test function. Additionally, the capture sequence of the INSTRUCTION register permits design specific data to be examined.

The INSTRUCTION register must be at least two bits long, the specific INSTRUCTION register included into the devices which reference this document is eight bits long, and the two least significant bits must capture the value "01". The significance of the two bit minimum length is two fold. First it permits the ability to supply unique codes for at least each of the three mandatory instructions required by the standard. Secondly, the bit value "01" in the least significant locations can be used to check the connectivity of the scan chain by forcing a bit toggle at each instruction during a scan of the INSTRUCTION registers. This technique not only assists in determining the correct connectivity of the scan chain about the board, but also assists in pin-pointing the location of any break in the scan chain.

All of National's SCAN Test Access Logic devices utilize an 8-bit instruction register. For the SCAN CMOS Test Access Logic devices, the 6 most significant bits which are loaded into the instruction register during the CAPTURE-IR state are used to provide a "pseudo ID code". The different codes captured into the INSTRUCTION register is a means of distinguishing the products in order to supply a method of evaluating the correct board placement of the products when an interrogation is performed through the scan chain only.

The captured "pseudo ID code" value is provided in each of the SCAN CMOS Test Access logic datasheets.

The SCAN ABT Test Access Logic devices include the IEEE 1149.1 optional ID CODE register and each device captures the same fixed value. This fixed value is the opcode for the SAMPLE/PRELOAD instruction, 1000001.

The order of scan through the INSTRUCTION register must be least-to-most; that is, the least significant bit is closest to TDO for a loaded instruction. During the SHIFT-IR state the instruction shifts one bit between TDI and TDO upon each rising edge of TCK and appears without inversion at TDO following the appropriate number of TCK cycles depending

on the fixed length of the INSTRUCTION register. A latched parallel output register accompanies each bit of the INSTRUCTION register such that the instruction can be updated or applied to the test logic simultaneously, rather than during the shift sequence. This latched parallel output changes upon the falling edge of TCK in the Update-IR state as well as upon the falling edge of TCK during the Test Logic Reset state. (It changes asynchronously upon the low assertion of the TRST input or upon power-up.)

Each instruction will identify a particular test data register to be connected between TDI and TDO when in the Shift-DR state along with defining any particular test actions to occur to that test data register and/or any others.

INSTRUCTION DEFINITIONS

The required instructions (see Table IV) include the BYPASS, EXTEST, and SAMPLE/PRELOAD instructions with optional instructions of HIGH-Z and CLAMP; and, for SCAN ABT only, the IDCODE. The additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT have also been incorporated into the SCAN ABT devices. The optional INTEST instruction was not incorporated because it adds a delay penalty to the system logic from gating that logic in order to provide controllability as well as observability. In the following descriptions each instruction will identify the test data register to be connected between TDI and TDO during the SHIFT-DR state, any restrictions on the binary codes used to implement the instruction, and what test data registers are used in undertaking the actions of the instruction.

1. **EXTEST.** This instruction allows circuitry external to the component package, typically the board interconnect, to be tested. Boundary-Scan register cells at the output pins are used to apply test stimuli, while those at the input pins capture test results. When this instruction is selected, the states of all signals on the system input pins will be loaded into the Boundary-Scan register upon the rising edge of TCK in the Capture-DR state and the contents of the Boundary-Scan register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-DR state. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 000...0 instruction binary code must invoke the EXTEST instruction. During this instruction the Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state. Additional binary codes for this instruction are permitted.

2. **SAMPLE/PRELOAD.** This instruction allows a "snapshot" of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan SHIFT register prior to selection of another Boundary-Scan test instruction. During this instruction the Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state. When this instruction is selected, the states of all signals on the system pins will be loaded into the Boundary-Scan register upon the rising edge of TCK in the CAPTURE-DR state and the contents of the Boundary-Scan register will be loaded into the parallel output register included with the Boundary-Scan register bits upon the falling edge of TCK in the UPDATE-DR state.

Note that by interfacing these two actions through the Exit1-DR state, the current state of the system pins can be captured into the Boundary-Scan register and stored into its parallel output registers for later application back onto those same pins. When the SAMPLE/PRELOAD instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. This instruction is mandatory under the guidelines of IEEE Standard 1149.1, but the binary code may be device specific.

3. **BYPASS.** This instruction allows rapid movement of test data to and from other components on a board that are required to perform test operations by selecting the BYPASS register, a single-bit shift-register stage, between TDI and TDO in the SHIFT-DR state to provide a minimum-length serial scan path. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 111...1 instruction binary code must invoke the BYPASS instruction. This specific opcode, along with the requirement that an undriven TDI input produce a logic high value, is intended to load the BYPASS instruction during an instruction-scan cycle if the scan chain is broken. In such a case all instructions following the break in the scan chain will be loaded with the BYPASS instruction and hence have no impact upon the system's normal functional operation. Additional binary codes for this instruction are permitted. When the BYPASS instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. When the optional IDCODE register is not included, this instruction is loaded into the INSTRUCTION register in the Test Logic Reset state.

TABLE IV. Required and Optional Instructions Included

IEEE 1149.1	SCAN ABT	SCAN CMOS
Required	BYPASS	BYPASS
Required	EXTEST	EXTEST
Required	SAMPLE/PRELOAD	SAMPLE/PRELOAD
Optional	HIGH-Z	HIGH-Z
Optional	CLAMP	CLAMP
Optional	IDCODE	
Optional	SAMPLE-IN	
Optional	SAMPLE-OUT	
Optional	EXTEST-OUT	

4. **CLAMP.** This instruction allows fixed guarding values to be placed on signals that control the operation of logic not involved in the test, but does not require that the Boundary-Scan register be part of the serial scan path as in the EXTEST instruction. The contents of the Boundary-Scan register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-IR state for this instruction. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.
5. **HIGH-Z.** This instruction allows all of a components system outputs to be placed in an inactive drive state to permit its outputs to be safely backdriven during testing of other integrated circuits on the printed circuit board. All outputs of the device will become inactive even if during their normal system function they are two-state outputs. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.
6. **IDCODE.** (SCAN ABT and PSC110F only.) This instruction allows a blind interrogation of an identification code that is unique to this device type. During this instruction the IDCODE Register is connected between TDI and TDO in the SHIFT-DR state.
7. **SAMPLE-IN.** (SCAN ABT only.) This instruction is analogous to SAMPLE/PRELOAD but shortens the SCAN chain to include only the input and control pin cells (see Input Boundary-Scan register definition diagram in each datasheet). During this instruction only the Input Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.
8. **SAMPLE-OUT.** (SCAN ABT only.) This instruction is analogous to SAMPLE/PRELOAD but shortens the SCAN chain to include only the output and internal TRI-STATE control cells (see Output Boundary-Scan register definition diagram in each datasheet). During this instruction only the Output Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.
9. **EXTEST-OUT.** (SCAN ABT only.) This instruction is analogous to EXTEST but shortens the SCAN chain to include only the output and internal TRI-STATE control cells (see Output Boundary-Scan register definition diagram in each datasheet). During this instruction only the Output Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.

Each of the previously defined instructions fully indicates which data registers may operate or interact with the system logic while the instruction is current. Test data registers that are not selected by the current instruction must be controlled such that they do not interfere with the system logic or the operation of the test data registers currently selected. While a given instruction may lead to operation of more than one test data register, only one test data register may be connected between TDI and TDO during the SHIFT-DR state for the given instruction.

BOUNDARY-SCAN REGISTER

The Boundary-Scan register permits testing of printed circuit board interconnects such as opens and shorts while also providing access to the components inputs and outputs when testing or monitoring its system logic. This register, as with all test data registers included in a 1149.1-compliant device, must be of fixed length. Data applied at the TDI input must appear without inversion at TDO during the SHIFT-DR state following the appropriate number of TCK cycles determined by the specific fixed length. This test data register will shift one stage toward TDO at each rising edge of TCK in the SHIFT-DR state when selected by the current instruction. Data will be parallel loaded into the Boundary-Scan register upon a rising edge of TCK in the Capture-DR state and the parallel register stages of the Boundary-Scan register will be latched upon the falling edge of TCK in the UPDATE-DR state provided that it is selected by the current instruction; otherwise, no change to its contents shall occur.

The shift register stages used in the make-up of the Boundary-Scan register may or may not be required to incorporate a parallel output register as well as its shift register stage. This requirement depends on the function of the system logic pin with which it is associated as well as the operational requirements of that pin during certain instructions defined for the device. The Input and Output Boundary-Scan cells demonstrate the parallel register stage, or lack thereof. The first cell can be used on system input pins where only observability of its logic state is necessary while the second scan cell can be used at system outputs where observability and controllability are required. Note that in the input scan cell there is no multiplexer directly in the data path while one does exist in the output scan cell. It is the logic gating of the data path that results in the performance penalty of the data path when controlling test logic is added. It is for this reason that the optional INTEST instruction was not included as one of the available features on the products which specifically reference this document. It was deemed unnecessary to pay the performance cost in exchange for the limited functional extension of controlling inputs as well.

If INTEST capability is desired, the system logic of the products referencing this document can be considered an extension of the EXTEST capability. All 1149.1-compliant devices require that the input and output data path scan cells be placed at logically equivalent locations to the system pin. As a result of that action the input/output buffers and voltage level translators are already tested as an extension of interconnect tests. If these interconnect tests are combined with the triggering of a 374 flip-flop clock input, as an example, the internal logic of the device can be evaluated as an extension of the EXTEST capability. Because the National SCAN products currently offered have easily manipulated

system logic, the 1149.1 user can logically extend the internal system logic to the EXTEST function. This feature is available during the EXTEST instructions for these products because the state of the outputs is captured along with the state of the inputs during the rising edge of TCK in the CAPTURE-DR state. Note that this is contrary to a recommendation of capturing fixed values on the outputs during EXTEST, but it provides for a feature that would otherwise not exist.

While these cells are sufficient to observe the logic state of the signal in which they are placed, they have a limitation in observing the activity of such a signal as in the specific case of a three-stated output. To determine the activity as well as the logic state of such an output, two such scan cells are required. One in the data signal path and another in the output enable signal path. By observing at both locations the drive activity and/or logic value can be inferred. In the case of a single output enable signal controlling more than one output data path, the output enable signal may be observable and controllable at a single location rather than at each specific output without loss of functional intent provided that the specific location retain control over all the data outputs in unison. This provision is included to reduce the hardware overhead as in the case of a device where such output enable signals are organized byte-wide.

The order of the required scan cells in the Boundary-Scan register is undefined by the 1149.1 Standard and hence can be device specific even if the system function of that device be identical to another 1149.1-compliant device. In other words, even if two identical system function devices are 1149.1-compliant there is no guarantee that such devices will be identical in the structure of the Boundary-Scan register.

A description of the Boundary Scan Register for each device is included in its datasheet.

Input Boundary-Scan Register (SCAN ABT only)

The Input Boundary-Scan register operates in a manner analogous to the full length Boundary-Scan register.

Output Boundary-Scan register (SCAN ABT only)

The Output Boundary-Scan register operates in a manner analogous to the full length Boundary-Scan register.

Please refer to the device datasheet for a description of its input and output Boundary-Scan Registers.

BYPASS REGISTER

The BYPASS register is also a test data register and therefore must comply with the definitions surrounding test data register operation; but its advantage is in its size, not neces-

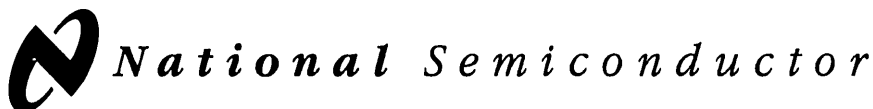
sarily in its function. The BYPASS register consists of a single shift register stage in order to shorten the board-level serial scan chain by bypassing some devices while accessing others. This feature is intended to reduce the software overhead in applying and retrieving serial test data by permitting a shortcut between TDI and TDO of any given integrated circuit in order to expedite access to others.

The BYPASS register must capture a logic low value upon the rising edge of TCK in the SHIFT-DR state provided that it is selected by the current instruction. This feature is designed to accompany those devices which incorporate the 32-bit device identification register. (The BYPASS register is a test data register whose least significant bit is a fixed logic high.) Upon an initial scan of the data registers connected across the board, all devices will either connect the BYPASS register or the optional device IDENTIFICATION register in its test data register scan path between TDI and TDO while in the SHIFT-DR state. (This condition is a result of power-up or a logic low assertion to TRST to initialize each 1149.1 device on board.) By shifting the data registers the retrieval of each logic zero indicates a BYPASS register connection until the first logic high is read. The logic high will be the framing bit of a device IDENTIFICATION register which would then indicate that the following thirty-one bits are identifiers to the specific device at that location of the scan chain. The requirement that the BYPASS register capture a logic low value is intended to form the background for the device IDENTIFICATION register framing bit. Additionally, the logic low value is opposite the value to be produced in the case of an undriven TDI input pin.

Device Identification Register

The device identification register is a 32-bit, read only register compliant with IEEE Std. 1149.1. When the IDCODE instruction is active, the identification register is loaded with a fixed, unique value upon leaving the Capture-DR state. The ID code register contains information pertaining to the device manufacturer, part number and revision. It is used to ensure the correct device is properly placed in the correct location within a boundary scan chain.

An identification (ID) register is included within the National SCAN ABT Test Access Logic devices. The specific ID register value is provided in the associated device datasheets.



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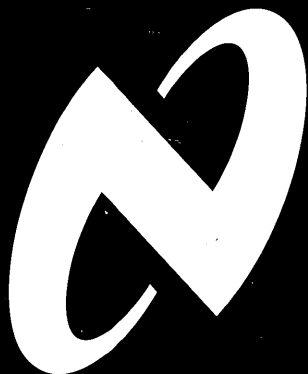
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