

Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions v3.0

User Guide

UG586 April 6, 2016



Date	Version	Revision
04/06/2016	3.0	- Updated to core version 3.0. - Updated Termination for all sections. - Updated 1.0 μF capacitor in General Memory Routing Guideline chapter. DDR3 and DDR2 - Added note in FPGA Options section. - Added note in Interfacing to the Core section. - Updated sys_rst descriptions in DDR3 and DD2 Configuration sections. - Added note in Debug Signals section. - Updated reset description in General Checks section.
11/18/2015	2.4	- Added asynchronous to sys_rst in all sections. - Added note to RELAXED mode in DDR3/DDR2 and LDDR2 sections. - Updated code in all Configuration sections - Added Important jitter note in Pinout Requirements in all sections. DDR3 and DDR2 - Added Synplify Pro Black Box Testing section. QDR II+ - Updated DEBUG_PORT Signal Descriptions, Write Init Debug Signal Map, and Read Stage 1 Debug Signal Map tables. - Updated Calibration of Read Clock and Data description. - Updated Write Calibration description. RLDRAM II/ RLDRAM 3 - Updated Read Stage 1 Debug Signal Map table. - Updated Calibration of Read Clock and Data description.
09/30/2015	2.4	- Added CLOCK_DEDICATED_ROUTE Constraints in all sections. DDR3 and DDR2 - Updated Trace Lengths section. QDR II+ - Added Termination section. RLDRAM II/ RLDRAM 3 - Added Termination section. - Updated Margin Check section. - Updated Automatic Margin Check section. - Updated Table 3-33: Debug Port Signals. LPDDR2 - Updated Trace Lengths section. Appendix - Added General Memory Routing Guidelines.

Date	Version	Revision
06/24/2015	2.3	- Added Simulation Flow Using VCS and IES to all sections. - Added Clocking sections to QDR II+, RLD RAM II/RLDRAM 3, and LPDDR2 chapters. RLDRAM II/ RLD RAM 3 - Added address/control signal and SSI descriptions in Pinout Requirements section. - Updated Input Clock Guidelines section.
04/01/2015	2.3	- Updated description in all Configuration sections. - Updated SIM_BYPASS_INIT_CAL. Chapter 1 - Added description in Setting DDR3 Memory Parameter Option section. - Added Note to Answer Record: 54025 in Controller Options section. - Added description to app_rd_data_end in Table 1-17: User Interface. - Updated Table 1-19: AXI4 Slave Interface Parameters. - Updated description in AXI4 Slave Interface Signals section. - Updated Time Division Multiplexing (TDM), Round-Robin, and Read Priority (RD_PRI_REG) sections. - Updated GES description in Calibration Times section. - Updated Fig. 1-50: Clocking Architecture. - Updated Table 1-87: Memory Controller to Calibration Logic Interface Signals. - Updated AXI Addressing section. - Updated Write Path section. - Updated Fig. 1-84: Command Processing. - Updated Physical Layer Interface (Non-Memory Controller Design) section. - Updated CK signal description in Trace Length section. - Updated Fig. 1-93: Calibration Stages. - Updated description in Determine the Failing Calibration Stage section. - Updated Table 1-100: DDR2/DDR3 Debug Signals. - Updated Table 1-102: Debug Signals of Interest for Write Leveling Calibration. - Updated Table 1-103: Debug Signals of Interest for MPR Read Leveling Calibration. - Updated calibration overview in Debugging OCLKDELAYED Calibration Failures section. - Updated Debug bullets in Debugging OCLKDELAYED Calibration Failures section. - Updated Table 1-104: Debug Signals of Interest for OCLKDELAYED Calibration to Table 1-106: Debug Signals of Interest for Read Leveling Stage 1 Calibration. - Updated Table 1-108: Calibration Time in Hardware. - Updated Checking and Varying Read Timing to Manual Window Check sections. - Updated Calibration Times section. Chapter 2 - Updated Fig. 2-43: High-Level PHY Block Diagram for a 36-Bit QDR II+ Interface. - Updated Margin Check and Automated Margin Check sections.

Date	Version	Revision
Continued		Chapter 3 - Updated description in Interfacing with the Core through the Client Interface section. Chapter 4 - Corrected app_wdf_data[APP_DATA_WIDTH – 1:0] and app_wdf_mask[APP_MASK_WIDTH – 1:0] sections. - Updated Fig. 4-43: Clocking Architecture. - Updated Read Path section.
11/19/2014	2.3	Chapter 1 - Updated description in Round-Robin section. - Updated RTT_WR in Table 1-92: 7 Series FPGA Memory Solution Configuration Parameters. - Updated description in Debugging OCLKDELAYED Calibration Failures section. - Updated Table 1-106: Debug Signals of Interest for OCLKDELAYED Calibration. - Updated GES time in Calibration Times section. - Updated bits in left_loss_pb and right_gain_pb in Table 1-109: Debug Signals of Interest for PRBS Read Leveling Calibration.
10/01/2014	2.2	- Global update to example design link in Files in example_design/sim Directory tables, updated links in Simulation Flow Using IES and VCS Script Files section, updated Simulation Flow Using Vivado Simulator section, and updated Simulation Flow Using QuestaSim section. Chapter 1 - Updated Reference Clock description in FPGA Option section. - Updated C_S_AXI_DATA_WIDTH description in Table 1-19: AXI4 Slave Interface Parameters. - Updated Fig. 1-50: Clocking Architecture. - Updated OCLKDELAYED Calibration section. - Updated Write Path section. - Added REF_CLK_MMCM_IODELAY_CTRL in Table 1-92: 7 Series FPGA Memory Solution Configuration Parameters. - Added note for nBANK_MACHS in Table 1-93: Embedded 7 Series FPGAs Memory Solution Configuration Parameters. - Added row and updated Table 1-94: DDR2/DDR3 SDRAM Memory Interface Solution Pinout Parameters - Updated CK/CK# bullet in Trace Length section. - Updated Table 1-102: DDR2/DDR3 Debug Signals. - Updated debug signals in Table 1-112: Debug Signals Used for Checking and Varying Read/Write Timing.

Date	Version	Revision
Continued		Chapter 2 - Added Bank Sharing Among Controllers section in Design Guideline section. Chapter 3 - Added Bank Sharing Among Controllers section in Design Guideline section. Chapter 4 - Updated Figs. 4-57 to 4-59 and Figs. 4-62 to 4-63. - Updated 2:1 description in Write Path section. - Updated rules in Termination section.
06/04/2014	2.1	Chapter 1 - Added reference to data sheet in Features section. - Added Important note about Data Mask in Controller Options section. - Added note in Precharge Policy section. - Added PRBS_SADDR_MASK)POS to Table 1-11: Traffic Generator Parameters Set in the example_top Module. - Updated IDELAYCTRL frequency in IDELAYCTRL section. - Updated IDELAY Reference Clock section. - Updated PRBS Read Leveling section. - Updated CL description for DDR3 in Table 1-93: Embedded 7 Series FPGAs Memory Solution Configuration Parameters. - Updated package length descriptions in Trace Length section. - Added simulation description in Note in Debugging DDR3/DDR2 Designs. - Updated description in Debugging PRBS Read Leveling Failures section. - Updated Table 109: Debug Signals of Interest for PRBS Read Leveling Calibration. Chapter 2 - Added reference to data sheet in Introduction section. - Updated package length descriptions in Trace Length Requirements section. - Added CPT_CLK_SEL_* row in Table 2-11: QDR II+ SRAM Memory Interface Solution Pinout Parameters. - Added simulation description in Note in Debugging QDR II+ Designs. Chapter 3 - Added reference to data sheet in Features section. - Added note in Memory Controller section. - Added PRBS_SADDR_MASK)POS to Table 3-8: Traffic Generator Parameters Set in the example_top Module. - Updated rules and package length descriptions in Trace Length Requirements section. - Added simulation description in Note in Debugging RLDRAM II and 3 Designs.

Date	Version	Revision
Continued		Chapter 4 - Added note in Precharge Policy section. - Added PRBS_SADDR_MASK)POS to Table 4-11: Traffic Generator Parameters Set in the example_top Module. - Updated package length descriptions in Trace Length Requirements section. - Added simulation description in Note in Read Path section.
04/02/2014	2.0	Chapter 1 - Updated book to DQS. - Updated Table 1-4: Files in example_design/sim Directory. - Updated file description in Simulation Flow Using IES and VCS Script Files section. - Added No Buffer description in the System Clock bullet in FPGA Options section. - Updated mc_data_offset description in Memory Controller to Calibration Logic Interface Signals table. - Added MPR read leveling process in Multi-Purpose Register Read Leveling section. - Updated Temperature Monitor section. - Added tempmon information in Physical Layer Interface (Non-Memory Controller Design) section. - Added description in address and control signals in Termination section for DDR3. - Added description in address and control signals and updated CKE signal bullet in Termination section for DDR2. - Added CK description in Trace Lengths section. - Added new code constraints for DDR3/DDR2 Configuration sections. - Added Clocking section. - Updated ocal signals in Table 1-102: DDR2/DDR3 Debug Signals. Chapter 2 - Added new code constraints in Configuration section. - Updated Table 2-3: Files in example_design/sim Directory. - Updated file description in Simulation Flow Using IES and VCS Script Files section. Chapter 3 - Added new code constraints in Configuration section. - Updated Table 3-3: Files in example_design/sim Directory. - Added important note on write and read commands in Interfacing with the Core through the Client Interface section. - Updated option for MRS_RD_LATENCY in RLDRAM II Memory Interface Solution Configurable Parameters table. - Updated file description in Simulation Flow Using IES and VCS Script Files section. Chapter 4 - Added new code constraints in Configuration section. - Updated Table 4-4: Files in example_design/sim Directory. - Updated file description in Simulation Flow Using IES and VCS Script Files section.

Date	Version	Revision
12/18/2013	2.0	• Vivado Design Suite release only for MIG v2.0. Chapter 1 • Added Out of Context content. • Updated Table 1-4: Modules in example_design/sim Directory. • Updated <component name>/user_design section. • Updated Fig. 1-39: Synthesizable Example Design Block Diagram. • Added simulator flows. • Added Bits[39:32] to Table 1-15: Debug Status for the Write Transaction. • Added Bits[39:32] to Table 1-16: Debug Status for the Read Transaction. • Added OOC description in Customizing the Core section. • Added ILA trigger settings in Vivado Lab Tools section. • Added note on read latency in Debug section. • Updated Chipscope triggers to R in Debug section. Chapter 2 • Added Out of Context content. • Updated Table 2-3: Modules in example_design/sim Directory. • Updated <component name>/user_design section. • Added OOC description in Customizing the Core section. • Added simulator flows. • Added ILA trigger settings in Vivado Lab Tools section. Chapter 3 • Added Out of Context content. • Updated Table 3-3: Modules in example_design/sim Directory. • Updated <component name>/user_design section. • Updated Fig. 3-35: Synthesizable Example Design Block Diagram. • Added OOC description in Customizing the Core section. • Added simulator flows. • Added ILA trigger settings in Vivado Lab Tools section. • Updated Fig. 3-48 Write Path Block Diagram of the RLDRAM II Interface Solution. • Added note on read latency in Debug section. Chapter 4 • Added Out of Context content. • Updated Table 4-4: Modules in example_design/sim Directory. • Updated <component name>/user_design section. • Updated Fig. 4-37: Synthesizable Example Design Block Diagram. • Added OOC description in Customizing the Core section. • Added simulator flows. • Added note on read latency in Debug section. Chapter 5 • Added Out of Context content.

Date	Version	Revision
10/02/2013	2.0	• Vivado Design Suite release only for MIG v2.0. • Removed ISE content throughout book and updated screenshots to v2.0. Chapter 1 • Updated Memory Part bullet description. • Updated Table 1-4 sim.do description and simulation directory. • Updated Fig. 1-44 7 Series FPGAs MIS. • Added aresetn in Table 1-20 AXI4 Slave Interface Signals. • Added Caution note in Single Error and Double Error Reporting section. • Updated Table 1-77 Memory Interface Commands. • Updated and added stage 3 tap in OCLKDELAYED Calibration section. • Added #4 table note to Table 1-91 7 Series FPGA Memory Solution Configuration Parameters. • Updated description in app_wdf_mask[APP_MASK_WIDTH - 1:0] section. • Added Memory Address Mapping description in User Interface section. • Updated Table 1-106 Debug Signals of Interest for OCLKDELAYED Calibration Chapter 2 • Updated Table 2-3 sim.do description and simulation directory. • Updated DIFF_HSTL_I in I/O Standards table. • Updated reference clock descriptions in Clocking Architecture section. • Added #1 table note to Table 2-11 7 Series FPGAs QDR II+ SRAM Memory Interface Solution Configurable Parameters. And updated SIM_BYPASS_INIT_CAL. Chapter 3 • Updated Table 3-3 sim.do description and simulation directory. • Updated reference clock descriptions in Clocking Architecture section. • Added #1 table note to Table 3-13 RLDRAM II Memory Interface Solution Configurable Parameters. And updated SIM_BYPASS_INIT_CAL. Chapter 4 • Updated Table 4-4 sim.do description and simulation directory. • Updated Fig. 4-37 7 Series FPGAs MIS. • Updated Table 4-14 User Interface. • Added #4 note to Table 4-25 7 Series FPGA Memory Solution Configuration Parameters. • Updated description in app_wdf_mask[APP_MASK_WIDTH - 1:0] section. • Added Memory Address Mapping description in User Interface section.

Date	Version	Revision
06/19/2013	2.0	• Vivado Design Suite release only for MIG v2.0. Revision number advanced to 2.0 to align with core version number. Chapter 1 • Updated ChipScope to Vivado logic analyzer, VIO, and ILA. • Updated ui_clk and ui_clk_sync_rst descriptions in Table 1-17 User Interface. • Updated ui_clk and ui_clk_sync_rst descriptions. • Added Ordering Modes in Reordering section and added modes in Table 1-91. • Updated ECC enable in AXI4 Slave Interface Block section. • Updated Read Priority (RD_PRI) section. • Updated Table 1-19 AXI4 Slave Interface Parameters, C_S_AXI_ADDR_WIDTH value and descriptions. • Added Write Priority description. • Updated PHASER_IN DQSFOUND Calibration section. • Removed Downsizing Option. • Added DM in DQ descriptions. • Added Dynamic Calibration and Periodic Read Behavior section. • Added Vivado Lab Tools section. • Added AR 54025 for Vivado. • Updated Debugging PHASER_IN DQSFOUND Calibration Failures (dbg_pi_dqsfound_err = 1) section. Chapter 2 • Updated ChipScope to Vivado logic analyzer, VIO, and ILA. • Added Fixed Latency Mode description in Controller Options section. • Removed qdr_qvld in Table 2-12 Physical Interface Signals. • Updated Figure 2-26 Four-Word Burst Length Memory Device Protocol. • Updated Output Architecture section in Write Path. • Added Write Calibration section. • Removed QVLD. • Updated Table 2-20 Write Init Debug Signal Map. • Updated Tables 2-21 and 2-22 Read Stage 1 and Stage 2 Debug Signal Map tables. Chapter 3 • Updated ChipScope to Vivado logic analyzer, VIO, and ILA. • Removed rld_qvld in Table 3-13 Physical Interface Signals. • Removed QVLD and QVLD_MAP in Table 3-16 RLDRAM II Memory Interface Solution Pinout Parameters. • Removed QVLD. • Updated descriptions in Manual Pinout Changes section. • Added new calibration description in Calibration section. • Updated Table 3-26 Physical Layer Simple Status Bus Description Defined in the rld_phy_top Module.

Date	Version	Revision
Continued		- Updated Table 3-27 DEBUG_PORT Signal with dbg_rd_stage1_rtr_error[N_DATA_LANES - 1:0] and dbg_rd_stage1_error[N_DATA_LANES - 1:0]. - Updated Tables 3-31 and 3-32 Read Stage 1 and Stage 2 Debug Signal Map tables. - Added Fig. 3-36 Calibration Flow Diagram and Fig. 3-37 Read Level Stage 1. - Added description to Data Alignment and Valid Generation section. - Updated description and added Figs. 3-38 to 3-43 in Write Calibration section. - Added Write Calibration Debug Map section. Chapter 4 - Updated ChipScope to Vivado logic analyzer, VIO, and ILA. - Updated ui_clk and ui_clk_sync_rst descriptions in Table 4-14 User Interface. - Updated ui_clk and ui_clk_sync_rst descriptions. - Added Ordering Modes in Reordering section and added modes in Table 4-25. - Added DM in DQ descriptions. - Added Termination description in LPDDR2 Pinout Examples section. Chapter 6 - Added Upgrading the ISE/CORE Generator MIG Core in Vivado section.
03/20/2013	1.9	- ISE 14.5 and Vivado Design Suite 2013.1 releases for MIG v1.9 and v1.9a. Chapter 1 - Added Memory Part frequency in Controller Options section. - Added No Buffer option description in FPGA Options section. - Added pinout description in Verify Pin Changes and Update Design section. - Updated Fig. 1-15 Setting Memory Mode Options. - Updated Fig. 1-16 FPGA Options. - Updated Fig. 1-30 7 Series FPGAs Memory Interface Solution to User's FPGA Logic - Added ECC description in AXI4 Slave Interface Block section. - Updated Table 1-91 7 Series FPGA Memory Solution Configuration Parameters. - Updated Table 1-92 Embedded 7 Series FPGAs Memory Solution Configuration Parameters. - Updated Table 1-93 DDR2/DDR3 SDRAM Memory Interface Solution Pinout Parameters. - Added description in Verifying the Simulation Using the Example Design section. - Reworked Design Guidelines DDR3 SDRAM section. - Added new debug section.

Date	Version	Revision
Continued		Chapter 2 - Added No Buffer option description in FPGA Options section. - Added pinout description in Verify Pin Changes and Update Design section. - Updated Fig. 2-15 FPGA Options. - Updated REFCLK_FREQ and RST_ACT_LOW in Table 2-13 7 Series FPGAs QDR II+ SRAM Memory Interface Solution Configurable Parameters - Updated Table 2-14 QDR II+ SRAM Memory Interface Solution Pinout Parameters. - Added description in Verifying the Simulation Using the Example Design section.
		Chapter 3 - Added No Buffer option description in FPGA Options section. - Updated Fig. 3-14 FPGA Options. - Added Verify Pin Changes and Update Design section. - Updated nCK_PER_CLK in Table 3-10 Traffic Generator Parameters Set in the example_top Module - Updated Table 3-15 RLDRAM II Memory Interface Solution Configurable Parameters. - Updated Table 3-16 RLDRAM II Memory Interface Solution Pinout Parameters. - Added description in Verifying the Simulation Using the Example Design section.
		Chapter 4 Added new LPDDR2 SDRAM section.
		Chapter 6 Updated to new GUIs.

Date	Version	Revision
12/18/2012	1.8	• ISE 14.4 and Vivado 2012.4 Design Suite releases for MIG v1.8. Chapter 1 • Updated Table 1-2 to 1-9 with new table note and.v name. • Updated Fig. 1-16 FPGA Options GUI. • Added XADC Instantiation bullet. • Added description to sim.do in Table 1-4. • Updated Table 1-11 DATA_PATTERN to 0xA. • Updated Table 1-13 vio_data_mode_value[3:0] to 0xA. • Updated description in Setting Up for Simulation. • Added description to EDK Clocking. • Updated ui_clk and ui_clk_sync_rst in Table 1-17. • Added description in Internal (FPGA) Logic Clock. • Added TEMP_MON_CONTROL to Table 1-91. • Added DATA_IO_IDLE_PWRDWN and CA_MIRROR to Table 1-92. • Added HP bank description in Bank and Pin Selection Guides for DDR3 Designs. • Added DDR3 SDRAM interface description to Configuration. • Added HP bank description in Bank and Pin Selection Guides for DDR2 Designs. • Added DDR2 SDRAM interface description to Configuration. Chapter 2 • Updated Table 2-2 and 2-7 to 2-8 with new table note and.v name. • Added description to sim.do in Table 2-3. • Updated descriptions and added Fig 2-26 to Clocking Architecture. • Updated description in Write Path Output Architecture. • Updated descriptions in Trace Length Requirements. • Added QDRII description in Configuration. • Added description to Verifying the Simulation Using the Example Design. • Added Margin Check and Automated Margin Check sections. Chapter 3 • Updated Table 3-2 and 3-6 to 3-8 with new table note and.v name. • Added description to sim.do in Table 3-3. • Updated Table 3-10 DATA_PATTERN to 0xA. • Updated descriptions and added Fig 3-30 to Clocking Architecture. • Updated descriptions in Trace Length Requirements. • Added descriptions in RLDRAM II. • Added RLDRAM II description in Configuration. • Added description to Verifying the Simulation Using the Example Design. • Added Debug section.

Date	Version	Revision
10/16/2012	1.7	• MIG 1.7 release. Updated ISE Design Suite version to 14.3. • Chapter 1: Added AXI4-Lite Slave Control/Status Register Interface Block section. Updated figures (1-32 and 1-37) and added PRBS and Temperature Monitor sections. Added CLKIN_PERIOD to USE_DM_PORT parameters in Table 1-37. Updated Table 1-38 PHY0_BITLANES description. • Chapter 2: Added CLKIN_PERIOD to DIVCLK_DIVIDE parameters in Table 2-13. • Chapter 3: Added RLDRAM 3 content throughout. Updated/added figures (3-10, 3-13, 3-23 to 3-32, 3-36 to 3-37, 3-40 to 3-41, 3-45 to 3-47, and 3-50). Added mem_ck_lock_complete parameter in Table 3-11. Added CLKOUT0_PHASE parameter in Table 3-15. Updated descriptions in Table 3-16 and added Table 3-28. Updated Table 3-29 user_cmd signal. Updated Table 3-31 and 3-34 descriptions. Added Debugging Write Calibration section. • Chapter 4: Added System Clock Sharing section • Chapter 5: Updated figures (5-15, 5-17 to 5-20), updated steps in Getting Started with Vivado – MIG IP Generation
07/25/2012	1.6	• MIG 1.6 release. Updated ISE Design Suite version to 14.2. Updated GUI screen captures throughout document. • Chapter 1: Added No Buffer, Use System Clock, and Sample Data Depth in FPGA Options, page 36. Changed the parameters nCK_PER_CLK, tZQI, SYSCLK_TYPE, REFCLK_TYPE, and APP_DATA_WIDTH. Added bulleted item about multiple CK outputs to Bank and Pin Selection Guides for DDR3 Designs, page 186. Updated Trace Lengths, page 191 and Termination, page 200. • Chapter 2: Added No Buffer, Use System Clock, and Sample Data Depth in FPGA Options, page 282. Changed the parameters SYSCLK_TYPE and REFCLK_TYPE. • Chapter 3: Added No Buffer, Use System Clock, and Sample Data Depth in FPGA Options, page 282. Changed the parameters SYSCLK_TYPE and REFCLK_TYPE. • Chapter 6: Added new chapter on migrating to Vivado Design Suite.
06/13/2012	1.5	Revised the recommended total electrical delay on CK/CK# relative to DQS/DQS# on page 191.

Date	Version	Revision
04/24/2012	1.4	• MIG 1.5 release. Updated ISE Design Suite version to 14.1. Updated GUI screen captures throughout document. Replaced IODELAYCTRL with IDELAYCTRL throughout. • Chapter 1: Added I/O Power Reduction option to FPGA Options. Revised I/O standards for sys_rst option in Bank Selection. Added Creating ISE Project Navigator Flow for MIG Example Design, Power-Saving Features, Multi-Purpose Register Read Leveling, OCLKDELAYED Calibration, Upsizing, and External Vref sections. Changed bits [16:15] to from Rank Count to Reserved in the PHY Control word. Revised maximum setting of NUM_DQ_PINS in Table 1-11. Revised Figure 1-55 flowchart. Removed RankSel[1:0] from Figure 1-56 and Figure 1-58. Added mc_odt and mc_cke to Table 1-87. Replaced AXI Addressing. Updated REFCLK_FREQ, RANK_WIDTH, and WRLVL in Table 1-92. Added DATA_IO_PRIM_TYPE to Table 1-93. Added bullet about DQS pins to Bank and Pin Selection Guides for DDR3 Designs. Changed DIFF_SSTL_15 to DIFF_SSTL18_II and SSTL15 to SSTL18_II. • Chapter 2: Changed DIFF_SSTL_15 to DIFF_HSTL_I and SSTL15 to HSTL_I. Revised I/O standards for sys_rst option in System Pins Selection. Revised the PHY_BITLANE parameters in Table 2-11. Added System Clock, PLL Location, and Constraints and Configuration sections. • Chapter 3: Changed DIFF_SSTL_15 to DIFF_HSTL_I and SSTL15 to HSTL_I. to Revised I/O standards for sys_rst option in System Pins Selection. Added the Write Calibration, System Clock, PLL Location, and Constraints, and Configuration sections. Revised the PHY_BITLANE parameters in Table 3-15. In Table 3-28, added dbg_wrcal_sel_stg[1:0], dbg_wrcal[63:0], dbg_wrcal_done[2:0], dbg_wrcal_po_first_edge[5:0], dbg_wrcal_po_second_edge[5:0], and dbg_wrcal_po_final[5:0].
01/18/2012	1.3	• MIG 1.4 release. Updated ISE Design Suite version to 13.4. Updated GUI screen captures throughout document. • Chapter 1: Added support for DDR2 SDRAM. Added option 3 to MIG Output Options. Added EDK Clocking. Added Replaced Figure 1-41 and Figure 1-69. • Chapter 2: Removed Input Clock Period option from Controller Options. Added Memory Options. Added Reference Clock option to FPGA Options. Updated Debug Signals. • Chapter 3: Removed Input Clock Period option from Controller Options. Added Input Clock Period option to Memory Options. Added Reference Clock option to FPGA Options. Added Debugging RLD RAM II and RLD RAM 3 Designs.

Date	Version	Revision
10/19/2011	1.2	• MIG 1.3 release. Updated ISE Design Suite version to 13.3. • Chapter 1: Added step 2 to MIG Output Options, page 26. Added note about optional use of the memory controller to Controller Options, page 30. Added arbitration scheme to AXI Parameter Options, page 33. Added description of DCI Cascade under Figure 1-23. Updated text about devices with SSI technology and SLRs on page 41 and page 187. Changed error to tg_compare_error on page 42. Replaced Table 1-8. Added qdr_wr_cmd_o, vio_fixed_instr_value, vio_fixed_bl_value, vio_pause_traffic, and vio_data_mask_gen signals to Table 1-13. Added signals to the User Interface in Figure 1-49 and Figure 1-51. Added app_sr_req, app_sr_active, app_ref_req, app_ref_ack, app_zq_req, and app_zq_ack signals to Table 1-17. Added app_wdf_rdy, app_ref_req, app_ref_ack, app_zq_req, app_zq_ack, Read Priority with Starve Limit (RD_PRI_REG_STARVE_LIMIT), Native Interface Maintenance Command Signals, User Refresh, and User ZQ sections. Added C_RD_WR_ARB_ALGORITHM to Table 1-19. Updated fields in Table 1-84, changed Hi Index (Rank) to Rank Count, and added CAS slot field. Updated AXI Addressing and Physical Layer Interface (Non-Memory Controller Design). Added Figure 1-75 through Figure 1-77 in Write Path. In Table 1-92, removed DISABLED option from RTT_NOM for DDR3_SDRAM, changed RTT_NOM to RTT_WR in RTT_WR, updated SIM_BYPASS_INIT_CAL, and updated table note 2. In Table 1-93, updated tZQI and added USER_REFRESH. Added Table 1-94. In Configuration, updated constraints example and removed paragraph about SCL and SDA. • Chapter 2: Added step 2 to MIG Output Options, page 275. Added Input Clock Period description in Controller Options, page 279. Added Debug Signals Control and Internal Vref Selection options to FPGA Options, page 282. Added I/O Planning Options, page 285. In System Pins Selection, page 288, changed cal_done signal to init_calib_complete and error signal to tg_compare_error. Replaced Table 2-2. Changed file names in Table 2-5. Updated signal names in Figure 2-38, Figure 2-39, and Figure 2-40. Updated signal names in Table 2-7. Added CPT_CLK_CQ_ONLY and updated value for SIM_BYPASS_INIT_CAL in Table 2-10. Added Table 2-11. Updated pinout rules in Pinout Requirements, page 337. Added paragraph about DCI and IN_TERM after Table 2-12. Added Debugging QDR II+ SRAM Designs, page 340. • Chapter 3: Added step 2 to MIG Output Options, page 375. Added Input Clock Period description in Controller Options. Added Debug Signals Control and Internal Vref Selection options to FPGA Options, page 382. In System Pins Selection, changed cal_done signal to init_calib_complete and error signal to tg_compare_error. Changed file names in Table 3-6. Removed Table 3-12, which contained Reserved signals not used. Added rst_phaser_ref to Table 3-11. Removed PHY-Only Interface section. In Table 3-14, added RLD_ADDR_WIDTH, MEM_TYPE, CLKIN_PERIOD, and SIMULATION, and renamed CLKFBOUT_MULT, CLKOUT0_DIVIDE, CLKOUT1_DIVIDE, CLKOUT2_DIVIDE, and CLKOUT3_DIVIDE. Updated Table 3-15. Added paragraph about DCI and IN_TERM after Table 3-24. • Added Chapter 5, Multicontroller Design.

Date	Version	Revision
06/22/2011	1.1	• MIG 1.2 release. Updated ISE Design Suite version to 13.2. Updated GUI screen captures throughout document. • Chapter 1: Added Verify Pin Changes and Update Design, Simulating the Example Design (for Designs with the AXI4 Interface), Error Correcting Code, and DDR3 Pinout Examples sections. Added paragraph about SLRs to Pin Compatible FPGAs, page 27. Added Input Clock Period and PHY to Controller bullets in Controller Options, page 30. To Setting DDR3 Memory Parameter Option, page 35, indicated that DDR3 SDRAM supports burst lengths of 8. Added Internal Termination for High Range Banks option under Figure 1-23. Added bulleted item about Pin/Bank selection mode on page 39. Added notes about chip select and data mask options on page 74. Added app_correct_en_i to Table 1-17. Added three command types to Command Path, page 134. Added phy_mc_ctl_full, phy_mc_cmd_full, and phy_mc_data_full signals to Table 1-87. Added paragraph about FIFOs at the end of Physical Layer Interface (Non-Memory Controller Design), page 168. Updated the description and options for DATA_BUF_ADDR_WIDTH in Table 1-93. Added bullet about SLRs to Bank and Pin Selection Guides for DDR3 Designs, page 186. Added LVCMOS15 and DIFF_SSTL15 I/O standards to Configuration, page 194. Changed resistor values in Figure 1-88, Figure 1-89, and Figure 1-90. Changed resistor values in FPGA DCI or IN_TERM column in Table 1-95. • Chapter 2: Added the Verify Pin Changes and Update Design and Output Path sections. Revised latency mode description on page 280. Added bulleted item about Pin/Bank selection mode on page 285. Added Internal Termination for High Range Banks option under Figure 2-22. Updated Implementation Details, page 324. • Chapter 3: Added new chapter on RLDRAM II.
03/01/2011	1.0	Initial Xilinx release.

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DDR3 and DDR2 SDRAM Memory Interface Solution

Introduction

The Xilinx® 7 series FPGAs Memory Interface Solutions (MIS) core is a combined pre-engineered controller and physical layer (PHY) for interfacing 7 series FPGA user designs and AMBA® Advanced eXtensible Interface (AXI4) slave interfaces to DDR3 and DDR2 SDRAM devices. This user guide provides information about using, customizing, and simulating a LogiCORE™ IP DDR3 or DDR2 SDRAM interface core for 7 series FPGAs. The user guide describes the core architecture and provides details on customizing and interfacing to the core.



IMPORTANT: *Memory Interface Solutions v3.0 only supports the Vivado® Design Suite. The ISE® Design Suite is not supported in this version.*

Features

Enhancements to the Xilinx 7 series FPGA memory interface solutions from earlier memory interface solution device families include:

- Higher performance.
- New hardware blocks used in the physical layer: PHASER_IN and PHASER_OUT, PHY control block, and I/O FIFOs (see [Core Architecture, page 89](#)).
- Pinout rules changed due to the hardware blocks (see [Design Guidelines, page 190](#)).
- Controller and user interface operate at 1/4th the memory clock frequency.

For a full list of supported features, see the *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions Data Sheet (DS176)* [[Ref 1](#)].

The OUT_FIFO serializes from eight bits to four bits and outputs the 4-bit data to the OSERDES in the OCLKDIV domain that is half the frequency of the DDR2 or DDR3 SDRAM clock. The OSERDES further serializes the 4-bit data to a serial DDR data stream in the OCLK domain. The PHASER_OUT clock output OCLK is used to clock DQ bits whereas the OCLK_DELAYED output is used to clock DQS to achieve the 90° phase offset between DQS and its associated DQ bits during writes. During write leveling, both OCLK and OCLK_DELAYED are shifted together to align DQS with CK at each DDR2 or DDR3 component.

The IN_FIFO shown in [Figure 1-59](#) receives 4-bit data from each DQ bit ISERDES in a given byte group and writes them into the storage array. The IN_FIFO is used to further deserialize the data by writing two of the 4-bit datagrams into each 8-bit memory element. This 8-bit parallel data is output in the PHY_Clk clock domain which is 1/4 the frequency of the DDR2 or DDR3 SDRAM clock. Each read cycle from the IN_FIFO contains all the byte data read during a burst length 8 memory read transaction. The data bus width input to the dedicated PHY is 8x that of the DDR2 or DDR3 SDRAM when running the FPGA logic at 1/4 the frequency of the DDR2 or DDR3 SDRAM clock.

Power-Saving Features

Designs generated by the MIG tool use the SSTL T_DCI standards, which save power by turning off the DCI when the FPGA output driver is active. Also, by using the IOBUF_DCIN (High Performance banks) and IOBUF_INTERMDISABLE (High Range banks) primitives, designs automatically disable the IBUF when the output is active. The controller uses these primitives to disable both DCI/IN_TERM and the IBUF when the controller is idle.

For more information on the IOBUF_DCIN and IOBUF_INTERMDISABLE primitives, see *7 Series FPGAs SelectIO™ Resources User Guide* (UG471) [\[Ref 2\]](#).

Calibration and Initialization Stages

Memory Initialization

The PHY executes a JEDEC®-compliant DDR2 or DDR3 initialization sequence for memory following deassertion of system reset. Each DDR2 or DDR3 SDRAM has a series of mode registers, accessed through mode register set (MRS) commands. These mode registers determine various SDRAM behaviors, such as burst length, read and write CAS latency, and additive latency. The particular bit values programmed into these registers are configurable in the PHY and determined by the values of top-level HDL parameters like BURST_MODE (BL), BURST_TYPE, CAS latency (CL), CAS write latency (CWL), write recovery for auto precharge (tWR), on-die termination resistor values (RTT_NOM and RTT_WR), and output driver strength (OUTPUT_DRV).

PHASER_IN Phase Lock

PHASER_IN is placed in the read calibration mode to phase align its free-running frequency reference clock to the associated read DQS. The calibration logic issues back-to-back read commands to provide the PHASER_IN block with a continuous stream of DQS pulses for it to achieve lock. A continuous stream of DQS pulses is required for the PHASER_IN block to phase align the free-running frequency reference clock to the associated read DQS. Each DQS has a PHASER_IN block associated with it. When the PHASER_IN lock signal (`pi_phase_locked`) of all the DQS PHASER_INs are asserted, the calibration logic deasserts the read calibration signal to put the PHASER_INs in normal operation mode.

PHASER_IN DQSFOUND Calibration

This calibration stage is required to align the different DQS groups to the same PHY_Clk clock edge in an I/O bank. Different DQS groups have different skews with respect to each other because of the clock (CK) fly-by routing differences to each DDR2 or DDR3 component and delay differences in each component. This calibration stage is required to determine the optimal position of read `data_offset` with respect to the read command per I/O bank.

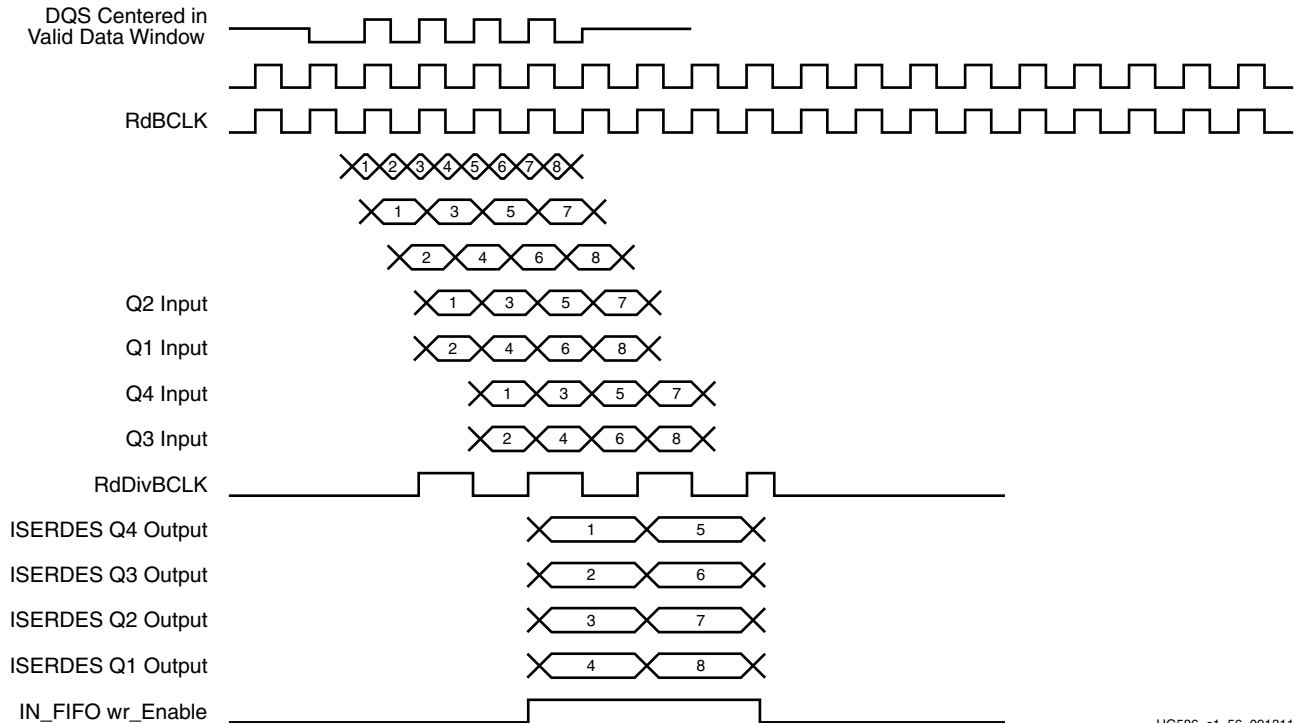
In this stage of calibration, the PHASER_IN block is in normal operation mode and the calibration logic issues a set of four back-to-back read commands with gaps in between. The `data_offset` associated with the first read command is not accurate because the round-trip delays are unknown.

For interfaces using HP I/O banks, the `data_offset` for the first set of read commands is set to CL + 13. The `data_offset` value for the subsequent set of reads is decreased one memory clock cycle at a time until the DQSFOUND output from the PHASER_IN block is asserted. When the DQSFOUND signal is asserted for all of the bytes, the CK delay stage begins.

For interfaces using HR I/O banks, the `data_offset` for the first set of read commands is set to CL – 2. The `data_offset` value for the subsequent set of reads is increased one memory clock cycle at a time until the DQSFOUND output from the PHASER_IN block is asserted. When the DQSFOUND signal is asserted for all of the bytes, the CK delay stage begins.

In the CK delay stage, the PHASER_OUT stage 2 delay tap is increased one at a time starting from 0 to 63 for CK/Address/Command/Control byte lanes. This effectively moves where the read DQS preamble begins and causes the DQSFOUND to fail. Any one DQSFOUND failure of the entire interface is considered a failure. A passing window is determined by recording the taps where the DQSFOUND failures occur. The final tap value for CK/Address/Command/Control byte lanes is set to the center of the passing window. If no failing edges are found the final tap is set to 32.

Each byte group can be read out of the IN_FIFO on different PHY_Clk cycles due to fly-by routing and delay differences within each group. Therefore, the IN_FIFO Not Empty flags for all the byte groups are ANDed together and used as the read enable for all data IN_FIFOs. Figure 1-61 shows the read data capture timing diagram.



UG586_c1_56_091311

Figure 1-61: Read Data Capture Timing Diagram

Write Leveling

Write leveling, which is a feature available in DDR3 SDRAM, is performed in this stage of calibration. DDR3 SDRAM modules have adopted fly-by topology on clocks, address, commands, and control signals to improve signal integrity. Specifically, the clocks, address, and control signals are all routed in a daisy-chained fashion, and termination is located at the end of each trace. However, this causes a skew between the strobe (DQS) and the clock (CK) at each memory device on the module. Write leveling, a new feature in DDR3 SDRAMs, allows the controller to adjust each write DQS phase independently with respect to the CK forwarded to the DDR3 SDRAM device. This compensates for the skew between DQS and CK and meets the τ_{DQSS} specification.

During write leveling, DQS is driven by the FPGA memory interface and DQ is driven by the DDR3 SDRAM device to provide feedback. The FPGA memory interface has the capability to delay DQS until a 0-to-1 transition is detected on DQ . Write leveling is performed once after power-up. The calibration logic ORs the DQ bits in a byte to determine the transition because different memory vendors use different bits in a byte as feedback. The DQS delay can be achieved with the PHASER_OUT fine and coarse delay adjustment in the 7 series FPGAs. Figure 1-62 shows the write leveling block diagram.

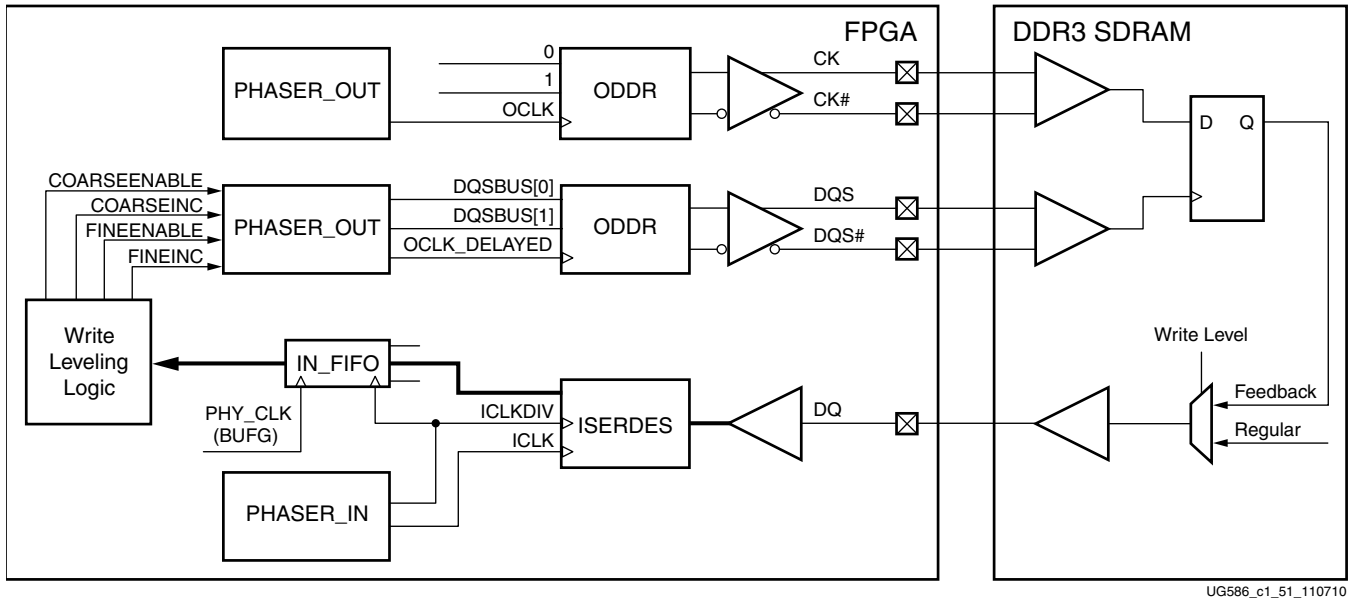


Figure 1-62: Write Leveling Block Diagram

The timing diagram for write leveling is shown in Figure 1-63. Periodic DQS pulses are output by the FPGA memory interface to detect the level of the CK clock at the DDR3 SDRAM device. The interval between DQS pulses is specified as a minimum of 16 clock cycles. DQS is delayed using the PHASER_OUT fine and coarse delay in unit tap increments until a 0 to 1 transition is detected on the feedback DQ input. The DQS delay established by write leveling ensures the t_{DQSS} specification.

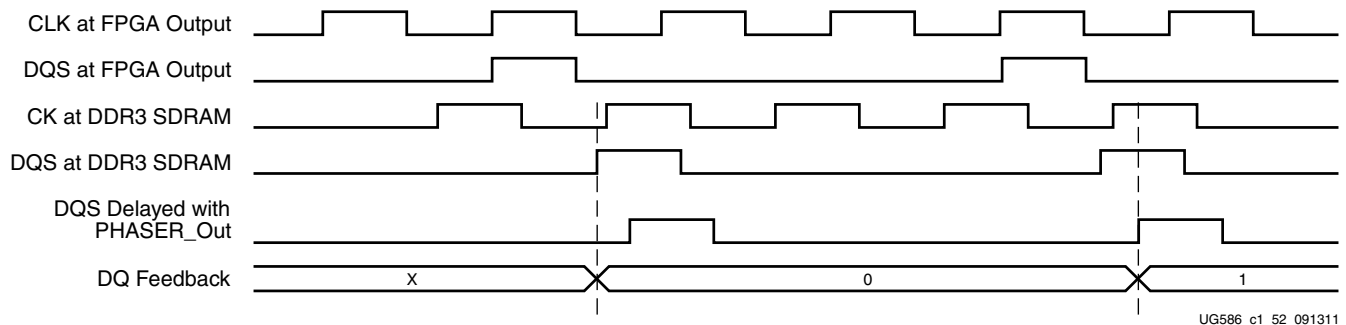


Figure 1-63: Write Leveling Timing Diagram

Figure 1-64 shows that the worst-case delay required during write leveling can be one tCK (DDR3 SDRAM clock period).

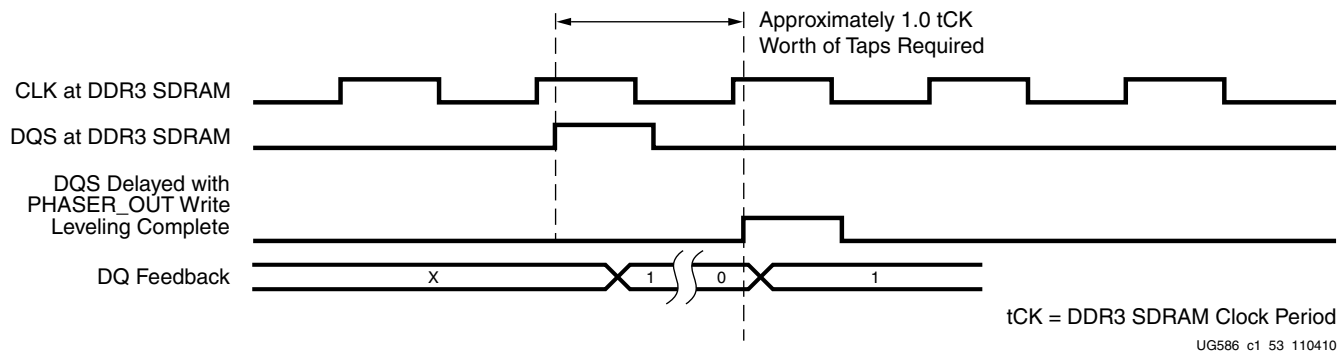


Figure 1-64: Write Leveling Taps Requirement

Implementation Details

The `write_calib_n` signal indicating the start of write leveling mode is input to the PHY control block after `tWLDQSEN` to ensure that `DQS` is driven Low after `ODT` is asserted. In this mode, periodic write requests must be issued to the PHY control block to generate periodic `DQS` pulses for write leveling. During write leveling, `PHASER_IN` outputs a free-running clock used to capture the `DQ` feedback to the `DQ IN_FIFOs`. During write leveling, the data byte group `IN_FIFOs` is in flow-through mode.

Figure 1-65 shows the flow diagram of the sequence of commands during write leveling. The `PHASER_OUT` fine phase shift taps are increased one tap at a time to observe a 0-to-1 transition on the feedback `DQ`. A stable counter is implemented in the write leveling logic to mitigate the risk of finding a false edge in the jitter region. A counter value of three means that the sampled data value was constant for three consecutive tap increments and `DQS` is considered to be in a stable region with respect to `CK`. The counter value is reset to 0 whenever a value different from the previous value is detected. Edge detection is inhibited when the stable counter value is less than 3. The `write_calib_n` signal is deasserted when write leveling is performed on all `DQSs` in all ranks.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

References

Unless otherwise noted, IP references are for the product documentation page. These references provide supplemental information useful for this document:

1. *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions Data Sheet* ([DS176](#))
2. *7 Series FPGAs SelectIO™ Resources User Guide* ([UG471](#))
3. *7 Series FPGAs Packaging and Pinout Specification* ([UG475](#))
4. [ARM® AMBA® Specifications](#)
5. *Vivado® Design Suite User Guide: Hierarchical Design* ([UG905](#))
6. *Vivado Design Suite Tutorial: Hierarchical Design* ([UG946](#))
7. *Vivado Design Suite User Guide: Designing with IP* ([UG896](#))
8. *Vivado Design Suite User Guide: Logic Simulation* ([UG900](#))
9. *Embedded System Tools Reference Manual* ([UG111](#))
10. *7 Series FPGAs Clocking Resources User Guide* ([UG472](#))
11. *XADC Wizard v2.4 LogiCORE IP Product Guide* ([PG091](#))
12. *7 Series FPGAs PCB Design and Pin Planning Guide* ([UG483](#))
13. [7 Series FPGAs Data Sheets](#)
14. *DDR2-533 Memory Design Guide For Two-DIMM Unbuffered Systems*. Micron Technology, Inc., ([TN-47-01](#))
15. *Xilinx Timing Constraints User Guide* ([UG612](#))

16. *Vivado Design Suite User Guide: Programming and Debugging* ([UG908](#))
 17. *Command Line Tools User Guide, COMPLIB* ([UG628](#))
 18. *Synthesis and Simulation Design Guide* ([UG626](#))
 19. [PlanAhead™ Design Analysis tool](#)
 20. *Virtex®-5 FPGA ML561 Memory Interfaces Development Board User Guide* ([UG199](#))
 21. JESD79-3E, *DDR3 SDRAM Standard*, JEDEC® Solid State Technology Association
 22. "Improving DDR SDRAM Efficiency with a Reordering Controller", XCELL Journal Issue 69
 23. *AXI Multi-Ported Memory Controller* ([XAPP739](#))
 24. *ISE® to Vivado Design Suite Migration Guide* ([UG911](#))
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