

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LIMITED,
Patent Owner.

IPR2023-00517
Patent 6,701,473 B2

Before JEAN R. HOMERE, BARBARA A. PARVIS, and MINN CHUNG,
Administrative Patent Judges.

CHUNG, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Xilinx, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–5, 7–10, 13, 14, 20–24, 26–29, 32, and 33 (the “challenged claims”) of U.S. Patent No. 6,701,473 B2 (Ex. 1001, “the ’473 patent”). Polaris Innovations Limited (“Patent Owner”) timely filed a Preliminary Response. Paper 11 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), institution of an *inter partes* review may not be authorized unless “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Upon consideration of the Petition and the Preliminary Response, we conclude that the information presented does not show there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of any challenged claim of the ’473 patent. Accordingly, we do not institute an *inter partes* review.

II. BACKGROUND

A. Related Matters

According to the parties, the ’473 patent is the subject of the following district court litigation: *Polaris Innovations Ltd. v. Xilinx, Inc.*, No. 1:22-cv-00174-RGA (D. Del.). Pet. 1; Paper 3, 2.

B. Real Party-in-Interest

Petitioner identifies itself, Advanced Micro Devices, Inc., and ATI Technologies ULC as the real parties-in-interest. Pet. 1. Patent Owner

identifies itself, Wi-LAN Inc., Owlpoint IP Opportunities JVF LP, and Quarterhill Inc. as the real parties-in-interest. Paper 10, 2.

C. The '473 Patent

The '473 patent issued March 2, 2004 from U.S. Patent Application No. 09/771,391, filed January 26, 2001. Ex. 1001, codes (21), (22), (45).

The '473 patent describes electrical circuits where circuit components can be tested independently of the other circuit components. Ex. 1001, Abstract. In addition, the '473 patent purports to disclose circuits that consume little or no power during testing of the circuit components. *Id.* at 2:16–18.

Figure 1 of the '473 patent is reproduced below.

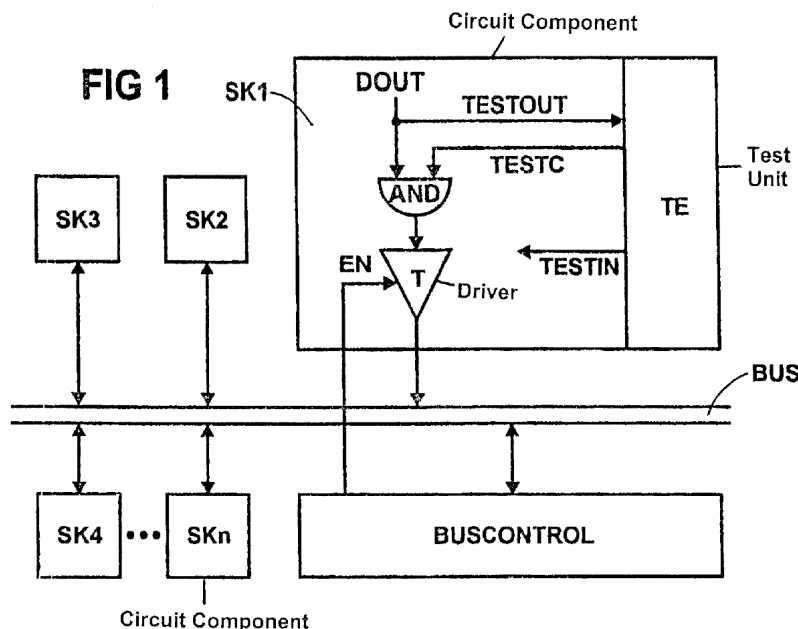


Figure 1 illustrates a first embodiment of the electrical circuit of the '473 patent. *Id.* at 4:43–44.

As shown above, the electrical circuit of Figure 1 includes circuit components SK1, SK2, . . . , SKn and a bus which connects the circuit

components. *Id.* at 4:60–62. The circuit components SK1, SK2, . . . , SKn include at least one circuit component which can be tested individually, i.e., independently of the other circuit components of the electrical circuit. *Id.* at 4:65–5:2.

In the example described in Figure 1, circuit component SK1 is a memory module. *Id.* at 5:6–7. In this example, as shown in Figure 1, circuit component SK1 includes Test Unit TE for testing the circuit component. *Id.* at 5:11–14, Fig. 1. The '473 patent describes that during testing of the circuit component SK1, the Test Unit TE inputs test data TESTIN and outputs test data TESTOUT to test whether the circuit component SK1 is operating correctly. *Id.* at 5:19–28.

The '473 patent further describes that during normal operation of the circuit component SK1, signal DOUT is output to the bus, whereas during testing, the value “0” is continuously output to the bus. *Id.* at 6:10–22. According to the '473 patent, “[t]his is advantageous because the output drivers T consequently consume only relatively little power” during testing. *Id.* at 6:26–28.

In an alternative embodiment depicted in Figure 2 (not reproduced herein), no data is output to the bus during testing. *Id.* at 7:24–8:9.

According to the '473 patent,

[t]he fact that no data are output to the bus . . . while the circuit component SK1 is being tested has the positive effect that the output drivers T have no or only a negligibly low power consumption and consequently do not heat up at all, or heat up only to a very small extent.

Id. at 8:38–42.

D. Illustrative Claim

Of the challenged claims, claims 1 and 20 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below with bracketing used by Petitioner (Pet. v, 18–25).

1. An electrical circuit comprising:

[1.1] a bus; and

[1.2] a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components;

[1.3] said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation.

Ex. 1001, 11:2–14.

E. Prior Art and Declaration Evidence

Petitioner cites the following references in its challenge to patentability:

U.S. Patent No. 5,072,138, issued Dec. 10, 1991 (Ex. 1005, “Slemmer”); and

U.S. Patent No. 6,308,232 B1, issued Oct. 23, 2001 (Ex. 1006, “Gasbarro”).

Petitioner supports its challenge with a declaration from Stephen W. Melvin (Ex. 1003, “Melvin Declaration”). Patent Owner’s Preliminary Response does not rely on the testimony of any declarant.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 2–3).

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–5, 7, 9, 10, 13, 14, 20–24, 26, 28, 29, 32, 33	103(a) ¹	Slemmer
1–5, 7–10, 13, 14, 20–24, 26–29, 32, 33	103(a)	Slemmer, Gasbarro

III. ANALYSIS

A. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the relevant time is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To assess the level of ordinary skill, we construct a hypothetical “person of ordinary skill in the art,” from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct “presumes that all prior art references in the field of the invention are available to this hypothetical

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the ’473 patent has a filing date prior to the effective date of the applicable AIA amendment, we refer to the pre-AIA version of § 103.

skilled artisan.” *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Citing testimony from Dr. Melvin, Petitioner asserts a person of ordinary skill in the art (“POSITA”) at the relevant time would have had “a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and two or three years of academic or industry experience in the use and testing of integrated circuits, or comparable experience.” Pet. 8 (citing Ex. 1003 ¶ 33). According to Dr. Melvin, “[a]dditional work experience can substitute for educational or research experience, and vice versa.” Ex. 1003 ¶ 33.

Patent Owner states that “[f]or the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner’s definition of a person of ordinary skill in the art, but it reserves the right to do so if trial is instituted.” Prelim. Resp. 11.

For purposes of this Decision, based on our review of the ’473 patent, the types of problems and solutions described in the ’473 patent, and cited prior art, we adopt and apply Petitioner’s unopposed definition of a person of ordinary skill in the art.

B. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2022). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the effective filing date of the patent application and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13.

“In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner asserts that “[c]onstruction of any terms is unnecessary because it is not dispositive—the art teaches the claims under any construction.” Pet. 9. Patent Owner addresses constructions for two claim terms recited in claims 1 and 20—“outputting data to said bus that is other than data which would be output to said bus during normal operation” and “outputting no data to the bus.” Prelim. Resp. 11–16. Patent Owner asserts that the term “outputting data to said bus that is other than data which would be output to said bus during normal operation” should be construed to mean “instead of the data which would be output to the bus by the circuit component during normal operation, outputting data to the bus that is other than the data which would be output to the bus during normal operation.” *Id.* at 11–12. As for the claim term “outputting no data to the bus,” Patent Owner argues that the term should be interpreted to mean “outputting no data to the bus when and so long as the circuit component is being tested.” *Id.* at 12–16.

Based on the record presented, we do not discern a need to construe explicitly any claim terms because doing so would not change the outcome of the analysis below. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the

controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Asserted Obviousness over Slemmer

Petitioner asserts that claims 1–5, 7, 9, 10, 13, 14, 20–24, 26, 28, 29, 32, and 33 are unpatentable under § 103(a) over Slemmer. Pet. 18–68. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 21–36. Based on the record presented and for the reasons discussed below, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that the subject matter of claims 1–5, 7, 9, 10, 13, 14, 20–24, 26, 28, 29, 32, and 33 would have been obvious to a person having ordinary skill in the art over Slemmer.

1. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.² *Graham*, 383 U.S. at 17–18.

² The parties do not present arguments or evidence related to such secondary considerations. Therefore, secondary considerations do not constitute part of our analysis in this Decision.

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)); see *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366–67 (Fed. Cir. 2012) (holding that “some kind of motivation must be shown from some source, so that the [trier of fact] can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented [invention]”).

Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

We analyze the asserted grounds based on obviousness with the principles identified above in mind.

2. Overview of *Slemmer* (Ex. 1005)

Slemmer describes an integrated circuit having a normal operating mode and a special test mode. Ex. 1005, Abstract. As background, *Slemmer* describes various problems in the conventional testing approaches that may cause accidental or inadvertent entry into the test mode or testing operations due to noise, power-up, etc. *Id.* at 2:53–4:42.

Against this backdrop, *Slemmer* purports to disclose an improved circuit and method for enabling a special mode in an integrated circuit device to avoid accidental or inadvertent entry into the test mode by providing increased security against inadvertent entry into the special test mode. *Id.* at 4:43–51, 5:3–14, Abstract.

Figure 1 of Slemmer is reproduced below.

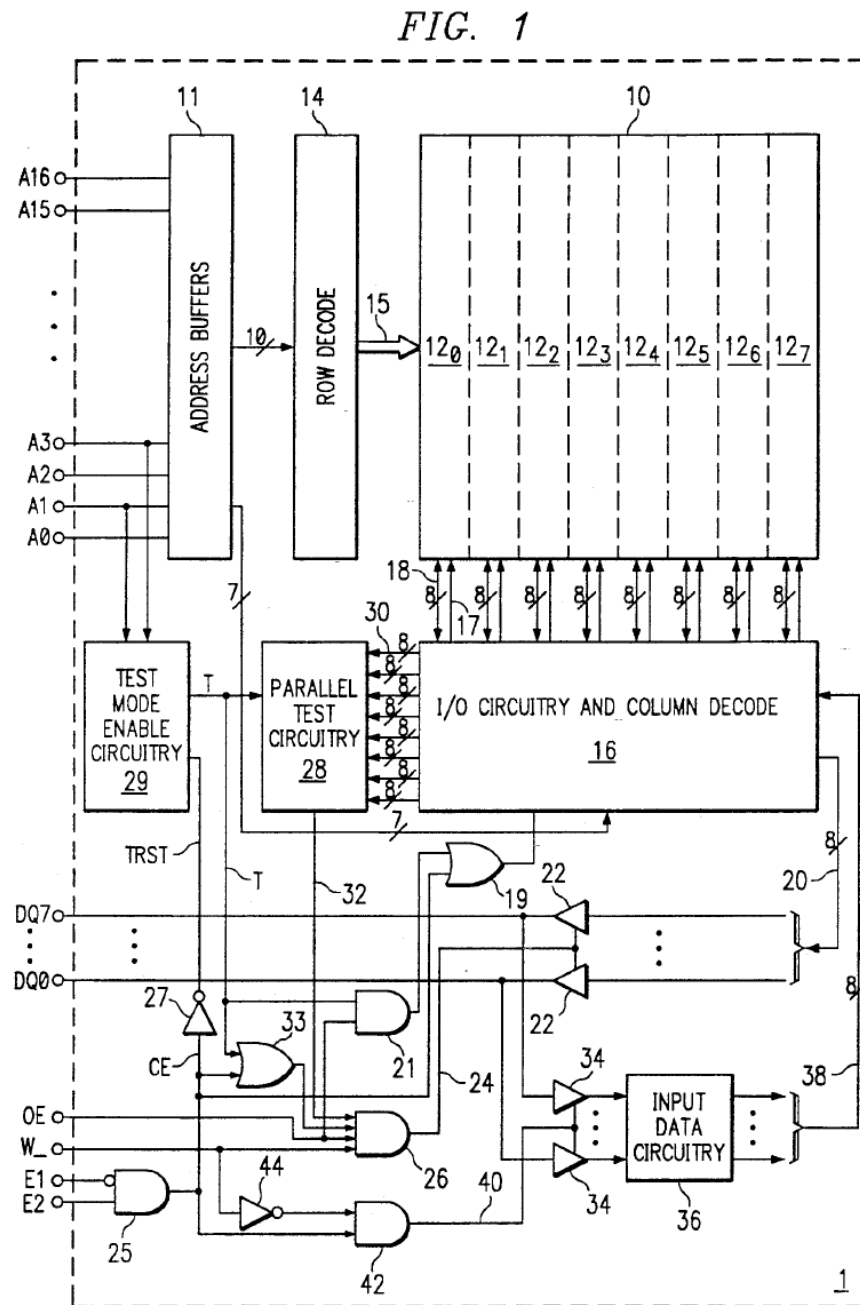


Figure 1 is an electrical block diagram of an exemplary memory device of Slemmer. *Id.* at 5:17–19.

As shown above, memory 1 of Figure 1 includes memory array 10, address terminals A0 through A16, for receiving the address data to specify

a unique memory address, and input/output terminals DQ0 through DQ7, for writing and reading data to and from the memory array. *Id.* at 5:50–6:11.

Memory 1 also includes test mode enable circuit 29 and parallel test circuitry 28. *Id.* at 8:20–23, 9:10–11, Fig. 1.

Slemmer describes that during normal memory operation, such as a read, the memory data will be accessed from one of subarrays 12 of memory array 10 and that upon the access of the memory location, eight data bits will appear at the eight input/output terminals DQ0 through DQ7. *Id.* at 5:58–61, 6:5–8. Slemmer further describes that when memory 1 is placed into a special test mode, parallel test circuitry 28 performs a comparison of multiple data words accessed from memory 10 and “generates a signal on line 32 corresponding to whether or not the comparison was successful.” *Id.* at 8:20–31. Slemmer describes that

[i]n this embodiment, line 32 is driven to a high logic level by parallel test circuitry 28 in test mode when the multiple data words all present the same data, and to a low logic level in test mode when there is an error, i.e., when the multiple data words compared do not present the same data.

Id. at 8:37–42.

As described in Slemmer, test mode enable circuit 29 enables parallel test circuitry 28 by using a test mode enable signal on line T that connects the test mode enable circuit 29 to the parallel test circuitry 28. *Id.* at 8:32–33, 9:45–48 (“Test mode enable circuitry 29 presents signals on line T to parallel test circuitry 28 . . . to indicate whether or not the parallel test mode is enabled.”), 23:55–57, 34:58–60, Fig. 1. Slemmer describes that line T is used to enable the special test mode “*prior to* such time as special test operations are performed.” *Id.* at 35:22–30 (emphasis added). According to

Slemmer, using test mode enable circuit 29 and line T to enable the special test mode before subsequent special test operations are performed “allows detection of an inadvertent entry” into the test mode (due to noise, etc.) so that the memory device may be returned to the normal operating mode without performing inadvertent test operations. *Id.* at 35:47–51.

Figure 9 of Slemmer is reproduced below.

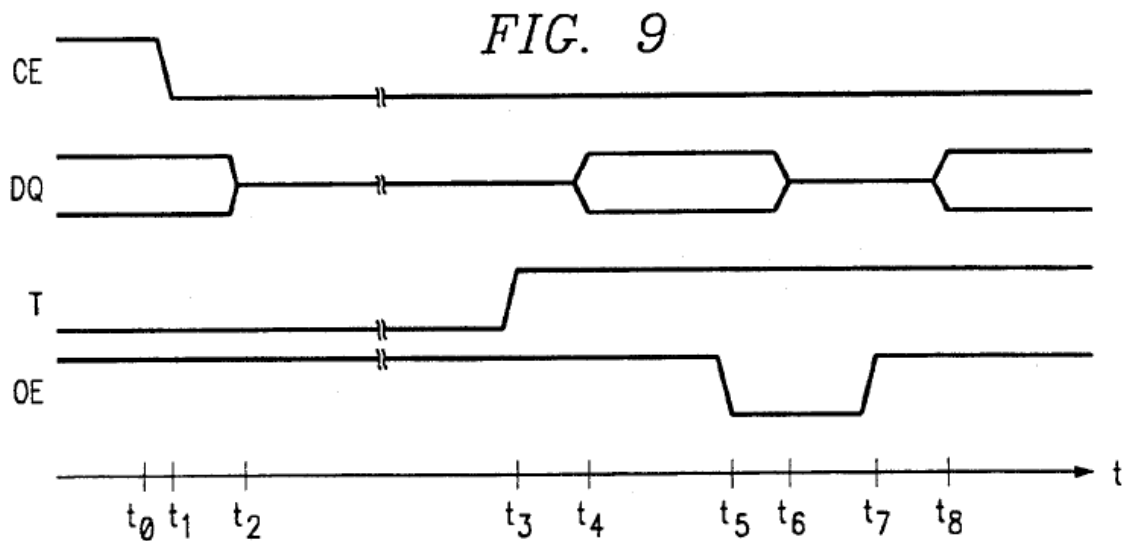


Figure 9 is a timing diagram illustrating the operation of the test mode enable circuitry depicted in Figure 1. *Id.* at 5:44–46.

Referencing Figure 9, Slemmer describes that enabling of the special test mode is indicated by employing lines T, CE, OE, and DQ. *Id.* at 36:1–2. Slemmer further describes that upon the entry into the special test mode at time t₃ of Figure 9, line T is driven by test mode enable circuitry 29 to a high logic level. *Id.* at 36:22–24. As shown in Figure 9, at time t₃ the line CE is at a low logic level and the line OE is at a high logic level. *Id.* at 36:2–6, 36:26–27.

According to Slemmer, “with line 32 from parallel test circuitry 28 remains high (i.e., the parallel test either passed, or has not taken place),”

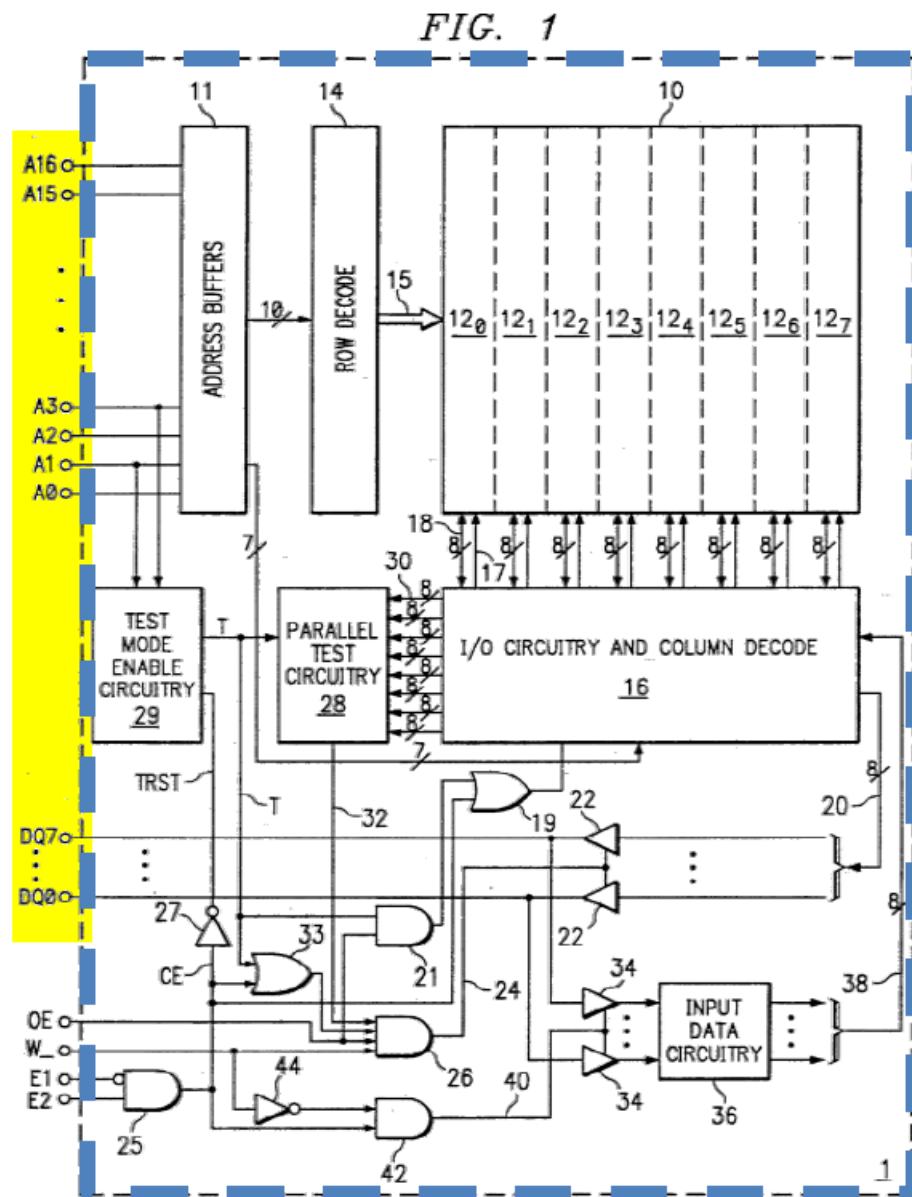
terminals DQ go into an active state at time t_4 to present a low impedance state. *Id.* at 36:26–32. This presentation of a low impedance condition at terminals DQ indicates the entry into the test mode. *Id.* at 36:40–44.

3. Independent Claims 1 and 20

Petitioner presents essentially the same analysis regarding independent claims 1 and 20, asserting that the independent claims recite similar limitations. *See* Pet. 18–29, 64–65. Patent Owner contests Petitioner’s showing, addressing claims 1 and 20 together. Prelim. Resp. 21–36. Because the parties do not dispute, and we agree, that claims 1 and 20 recite substantially similar limitations, our discussion below focuses on claim 1. Unless otherwise noted, our analysis below applies equally to both independent claims 1 and 20.

Petitioner contends that Slemmer teaches the preamble and all limitations of claim 1. Pet. 18–29. In particular, Petitioner relies on Slemmer’s embodiment depicted in Figures 1 and 9 as teaching all limitations of claim 1.

Figure 1 of Slemmer as annotated by Petitioner is reproduced below.



Pet. 20. Annotated Figure 1 of Slemmer reproduced above illustrates Petitioner's alleged identification in Slemmer of certain limitations recited in claim 1. *Id.* at 18–22.

Petitioner contends that multiple data input/output (I/O) terminals (e.g., DQ0–DQ7) and multiple address terminals (e.g., A0–A17) (annotated

in yellow in Petitioner-annotated Figure 1 of Slemmer reproduced above) teaches limitation [1.1], which is “a bus.” Pet. 18–21 (citing Ex. 1003 ¶¶ 79–81).

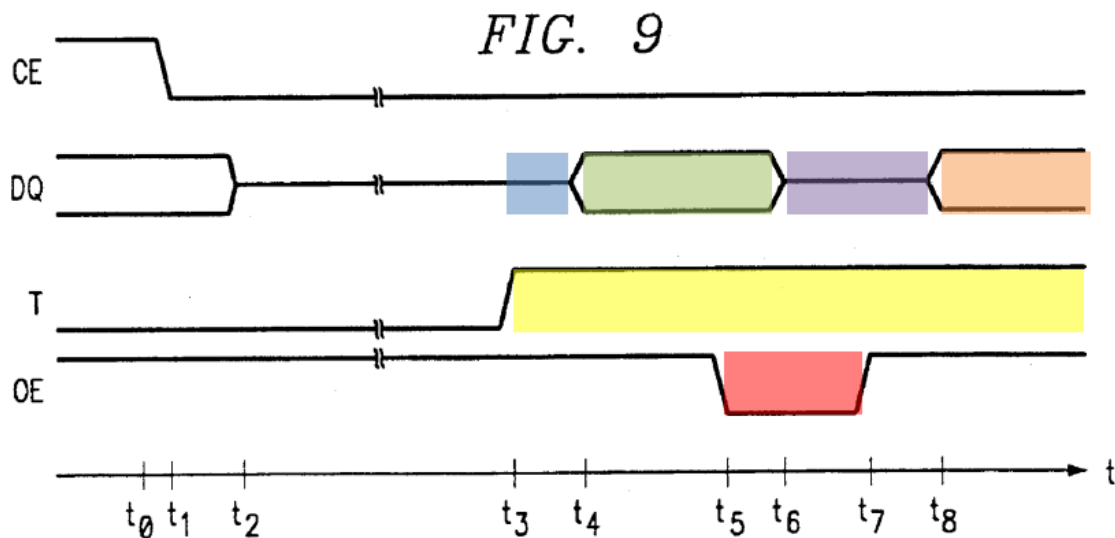
Addressing limitation [1.2], which is “a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components,” Petitioner asserts that Slemmer teaches that its multiple memories (“a plurality of circuit components”), each similar to memory 1 (annotated in blue above), are connected together via one or more signal lines for data I/O and/or address (“which are connected via said bus”). Pet. 21–22 (citing Ex. 1005, 35:22–42, 37:11–37, Fig. 1; Ex. 1003 ¶¶ 82, 83). Petitioner further argues that

a POSITA would have understood that one of the multiple memories 1 in Slemmer is enabled for testing whereas the remaining memories are disabled, and thus, the enabled memory is to be tested independent from the other memories (“*one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components*”).

Id. at 25 (citing Ex. 1005, 37:1–37, Fig. 1; Ex. 1003 ¶¶ 82–88).

Turning to limitation [1.3], which is “said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation,” Petitioner contends that Slemmer’s operations to enter the special test mode, as depicted in Figure 9 of Slemmer, teaches limitation [1.3]. Pet. 25–29.

Figure 9 of Slemmer as annotated by Petitioner is reproduced below.



Pet. 26. Annotated Figure 9 of Slemmer reproduced above illustrates Petitioner’s alleged identification in Slemmer the operations recited in limitation [1.3]. *Id.* at 25–29.

Referencing Petitioner-annotated Figure 9 of Slemmer reproduced above, Petitioner asserts that in Slemmer “testing is enabled at **time t₃** by the assertion of the ‘T’ signal to a high logic level (annotated in yellow) and the DQ terminal is initially in a high-impedance state (in blue)” in which no data is output to the bus. Pet. 25–26 (emphasis added) (citing Ex. 1005, 36:10–25; Ex. 1003 ¶¶ 90–91). Petitioner also contends that “[t]he DQ terminal is also in the high-impedance state between times t₆ and t₈ (in purple).” *Id.* at 26 (citing Ex. 1005, 37:27–32). In the cited paragraph of his Declaration, Dr. Melvin opines that “[a] POSITA would have understood from Slemmer’s disclosure that no data is output from the DQ terminals when they are in a high-impedance state.” Ex. 1003 ¶ 91 (citing Ex. 1013, 1:11–

16). Thus, Petitioner argues that Slemmer teaches “outputting no data to said bus,” as recited in limitation [1.3]. Pet. 25–26.

Petitioner further asserts that Slemmer teaches “outputting data to said bus that is other than data which would be output to said bus during normal operation,” as alternatively recited in limitation [1.3], because “after testing is enabled (annotated in yellow), the DQ terminal transitions at *time t₄* to an active, low-impedance state (in green), in which data is output to the bus.” Pet. 27–28 (emphasis added) (citing Ex. 1005, 36:10–54, Fig. 9; Ex. 1003 ¶ 95).

In the Preliminary Response, Patent Owner asserts that Slemmer does not teach “outputting no data to said bus” “during testing” as recited in claim 1 (limitation [1.3]) or “while testing” as recited in claim 20 (limitation [20.3]). Prelim. Resp. 29–34. We agree with Patent Owner that none of the operations in Figure 9 of Slemmer cited by Petitioner describe any operation performed “during testing” or “while testing,” as recited in limitation [1.3] or limitation [20.3].

As discussed above in Section III.C.2, Slemmer describes that line T is used to enable the special test mode “*prior to* such time as special test operations are performed.” Ex. 1005, 35:22–30 (emphasis added). Slemmer also describes that “upon the entry into a special test mode at *time t₃* of FIG. 9, line T is driven by test mode enable circuitry 29 to a high logic level.” *Id.* at 36:22–24 (emphasis added). Slemmer further describes that “with line 32 from parallel test circuitry 28 remains high (i.e., the parallel test either passed, or *has not taken place*),” terminals DQ “go into an active state at *time t₄*” to present a low impedance state. *Id.* at 36:26–32 (emphasis added). Thus, Slemmer discloses that the enabling of the special test mode

at time t_3 or time t_4 described in Figure 9—which Petitioner relies on as teaching “outputting no data to said bus” (at time t_3) and “outputting data to said bus that is other than data which would be output to said bus during normal operation” (at time t_4)—takes place *before* the test operations are performed.

Petitioner acknowledges that Figure 9 of Slemmer describes transactions to enter or enable the special test mode. *See* Pet. 25–27. Petitioner, however, does not address Slemmer’s disclosures that such transactions or operations take place *before* test operations are performed, which directly contradict Petitioner’s assertion that the operations described in Figure 9 of Slemmer are performed “during testing” as required by claim 1. *See id.* at 29.

Although Petitioner asserts that “Slemmer discloses that the terminals DQ have a different function in normal operation than during testing,” Petitioner does not explain adequately how Figure 9 describes operations performed “during testing” as required by claim 1 or “while testing” as required by claim 20. *See* Pet. 28 (citing Ex. 1005, 37:40–51, 5:58–61, 8:59–61; Ex. 1003 ¶¶ 96–97). Dr. Melvin similarly does not explain adequately why the operations described in Figure 9 of Slemmer are performed “during testing,” despite Slemmer’s express disclosures to the contrary. *See* Ex. 1003 ¶¶ 96–97.

As discussed above in Section III.C.2, Slemmer describes that using test mode enable circuit 29 and line T to enable the special test mode *before* subsequent special test operations are performed “allows detection of an inadvertent entry” into the test mode (due to noise, etc.) so that the memory device may be returned to the normal operating mode without performing

inadvertent test operations. Ex. 1005, 35:47–51. Thus, enabling the test mode prior to performing test operations avoids accidental or inadvertent entry into the test mode, which is one of the stated goals of Slemmer. *Id.* at 4:43–51, 5:3–14 (Summary of the Invention), Abstract.

In view of these disclosures in Slemmer, we find that Petitioner’s contentions directly contradict key disclosures in Slemmer. Based on the record presented, Petitioner does not show sufficiently that Slemmer teaches “outputting no data to said bus” or “outputting data to said bus that is other than data which would be output to said bus during normal operation” “during testing” as required by claim 1 (limitation [1.3]) or “while testing” as required by claim 20 (limitation [20.3]).³ Thus, Petitioner does not demonstrate sufficiently that Slemmer teaches or suggests all elements of claims 1 and 20.

Based on the record before us, Petitioner has not set forth sufficient argument and supporting evidence to demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claims 1 and 20 would have been obvious over Slemmer.

³ Although claims 1 and 20 recite the alternative operations in a Markush group form such that any plurality of the recited alternatives found in the prior art meets the Markush group element, *see In re Gosteli*, 872 F.2d 1008, 1010 (Fed. Cir. 1989), we find that neither “outputting no data to said bus” nor “outputting data to said bus that is other than data which would be output to said bus during normal operation” has been sufficiently shown to be performed in Slemmer “during testing” or “while testing” because no operations described in Figure 9 of Slemmer are performed during the testing mode or testing operation.

4. Dependent Claims 2–5, 7, 9, 10, 13, 14, 21–24, 26, 28, 29, 32, and 33

Claims 2–5, 7, 9, 10, 13, and 14 depend from claim 1 and claims 21–24, 26, 28, 29, 32, and 33 depend from claim 20.

Petitioner’s arguments and evidence presented with respect to these dependent claims only address the additionally recited limitations of claims 2–5, 7, 9, 10, 13, 14, 21–24, 26, 28, 29, 32, and 33, and, therefore, do not remedy the deficiencies in Petitioner’s analysis of claims 1 and 20 discussed above. *See* Pet. 29–68. Accordingly, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claims 2–5, 7, 9, 10, 13, 14, 21–24, 26, 28, 29, 32, and 33 are unpatentable under § 103(a) over Slemmer.

D. Asserted Obviousness over Slemmer and Gasbarro

Petitioner contends that claims 1–5, 7–10, 13, 14, 20–24, 26–29, 32, and 33 are unpatentable under § 103(a) over the combination of Slemmer and Gasbarro.

In this asserted ground of obviousness over the combination of Slemmer and Gasbarro, Petitioner relies on Slemmer only as teaching limitation [1.3] of claim 1 and limitation [20.3] of claim 20, citing Petitioner’s analysis of Slemmer as applied to limitation [1.3] and limitation [20.3] discussed above. Pet. 73, 81. Thus, for the same reasons discussed above in Section III.C.3, Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claims 1 and 20 would have been obvious over Slemmer and Gasbarro.

Claims 2–5, 7–10, 13, and 14 depend from claim 1 and claims 21–24, 26–29, 32, and 33 depend from claim 20. Petitioner’s arguments and evidence presented with respect to these dependent claims only address the

additionally recited limitations of claims 2–5, 7–10, 13, 14, 21–24, 26–29, 32, and 33, and, therefore, do not remedy the deficiencies in Petitioner’s analysis of claims 1 and 20 discussed above. *See* Pet. 75–83. Accordingly, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claims 2–5, 7–10, 13, 14, 21–24, 26–29, 32, and 33 are unpatentable under § 103(a) over the combination of Slemmer and Gasbarro.

IV. CONCLUSION

For the foregoing reasons, based on the arguments and evidence presented in the Petition, we conclude that Petitioner has not demonstrated a reasonable likelihood that Petitioner would prevail in showing at least one of the challenged claims of the ’473 patent is unpatentable based on any asserted ground of unpatentability. Therefore, we do not institute an *inter partes* review with respect to any of the challenged claims of the ’473 patent.

V. ORDER

In consideration of the foregoing, it is
ORDERED that Petitioner’s request for an *inter partes* review is *denied* as to all challenged claims of the ’473 patent, and no trial is instituted.

IPR2023-00517
Patent 6,701,473 B2

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