

U.S. Patent No. 8,775,833 (“the ’833 Patent”) Claim Mapping Table

1[Pre] A processor comprising:		13[Pre] A system comprising:
1[A] a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency;	8[A] determining, in a power controller of a multi-domain processor, a power budget for the multi-domain processor, the multi-domain processor including at least a first domain and a second domain;	13[A.i] a multicore processor having a first domain including a plurality of cores, a second domain including a graphics engine, and
		13[A.ii(1)] a third domain including system agent circuitry,
		13[A.ii(2)] the third domain to operate at a fixed power budget and
1[B] a memory controller coupled to the first and second domains;		
1[C] at least one interface; and		
1[D.i]: first logic to dynamically allocate a power budget for the processor between the first and second domains at run time	8[B.i] determining, in the power controller, a portion of the power budget to be allocated to the first and second domains,	13[A.ii(3)] including a power sharing logic to dynamically allocate a variable power budget between the first and second domains
1[D.ii] according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.	[8B.ii] including allocating a minimum reservation value to the first domain and a minimum reservation value to the second domain, and sharing a remaining portion of the power budget according to a first sharing policy value for the first domain and a second sharing policy value for the second domain; and	13[A.ii(4)] based at least in part on a first power sharing value for the first domain stored in a first storage and a second power sharing value for the second domain stored in a second storage; and
		13[B] a dynamic random access memory (DRAM) coupled to the multicore processor.
	8[Pre] A non-transitory machine-readable medium having stored thereon instructions, which if performed by a	

	machine cause the machine to perform a method comprising:	
	[8C] controlling a frequency of the first domain and a frequency of the second domain based on the allocated portions.	
2. The processor of claim 1, wherein the first logic is to determine a portion of the power budget to allocate to the first domain based on the first sharing policy value.		
		14. The system of claim 13, wherein the power sharing logic to determine the variable power budget for a current time interval and to allocate a first portion of the variable power budget to the first domain according to the first power sharing value, and to allocate a second portion of the variable power budget to the second domain according to the second power sharing value.
3. The processor of claim 1, wherein the first logic is to dynamically allocate the power budget further according to a first minimum reservation value for the first domain and a second minimum reservation value for the second domain, the first and second minimum reservation values controllable by the user-level software.	10. The non-transitory machine-readable medium of claim 9, wherein the method further comprises obtaining the minimum reservation value for the second domain from a configuration register written by user-level software.	17. The system of claim 14, wherein the power sharing logic is to further allocate the first portion of the variable power budget according to a first minimum reservation value for the first domain and allocate the second portion of the variable power budget according to a second minimum reservation value for the second domain.
4. The processor of claim 3, wherein the first logic is to provide at least a first portion of the power budget to the first		

domain, the first portion corresponding to the first minimum reservation value.		
5. The processor of claim 1, wherein the first logic is to determine the power budget for a current time interval based at least in part on a power budget carried forward from a previous time interval, a power consumed in the previous time interval, and a power budget decay value.		
6. The processor of claim 5, wherein the first logic is to determine the power budget according to $E_n = E_{n-1} * \alpha + (1 - \alpha) * (\text{Power\_Limit} * \text{deltaT} - \text{Energy})$ , where: $E_n$ is the power budget for the current time interval; $E_{n-1}$ is the power budget carried forward from the previous time interval; Power_limit is a threshold power level; deltaT is a length of the time interval; Energy is the power consumed during the previous time interval; and alpha is the power budget decay value.		
7. The processor of claim 1, wherein the first logic is to dynamically allocate substantially all of the power budget to the first domain for a first workload, and to dynamically allocate substantially all of the power budget to the second domain for a second workload executed after the first workload.		15. The system of claim 14, wherein the power sharing logic is to dynamically allocate substantially all of the variable power budget to the first domain for a first workload, and to dynamically allocate substantially all of the variable power budget to the second domain for a second workload executed after the first workload.

	9. The non-transitory machine-readable medium of claim 8, wherein determining the portion of the power budget to be allocated to the first and second domains includes allocating the power budget to the second domain and not to the first domain if the power budget is less than the minimum reservation value for the second domain.	
	11. The non-transitory machine-readable medium of claim 9, wherein the method further comprises allocating the minimum reservation value for the second domain to the second domain, and allocating a remaining portion of the power budget to the first domain when the power budget is greater than the minimum reservation value for the second domain but less than a sum of the minimum reservation value for the second domain and a minimum reservation value for the first domain.	
	12. The non-transitory machine-readable medium claim 8, wherein the first sharing policy value is controllable by software executing on the first domain, the first sharing policy value to be incremented when a request for a higher frequency for the first domain is not granted, and the second sharing policy value is controllable by software executing on the second domain, the second sharing policy value to be incremented when a request for a	16. The system of claim 14, wherein the power sharing logic is to increment the first power sharing value when a request for a higher frequency for the first domain is not granted, and to increment the second power sharing value when a request for a higher frequency for the second domain is not granted.

	higher frequency for the second domain is not granted.	
		18. The system of claim 14, wherein the power sharing logic is to further allocate the variable power budget according to a preference value, the preference value to favor the second domain over the first domain.