

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

Case IPR2023-00550
Patent 8,775,833 B2

Before WILLIAM V. SAINDON, ARTHUR M. PESLAK, and
KRISTIL R. SAWERT, *Administrative Patent Judges*.

SAWERT, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Qualcomm Incorporated (“Petitioner”) filed a petition to institute *inter partes* review of claims 1–5, 7, and 13–18 of U.S. Patent No. 8,775,833 B2 (Ex. 1001, “the ’833 patent”). Paper 1 (“Pet.”). Daedalus Prime LLC (“Patent Owner”) filed a Preliminary Response. Paper 12 (“Prelim. Resp.”).

We have authority under 35 U.S.C. § 314 to determine whether to institute an *inter partes* review. The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” If the Board institutes trial, it “will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” 37 C.F.R. § 42.108(a); see also *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute to require “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

Applying those standards, and upon considering the Petition, the Preliminary Response, and the evidence of record, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of the challenged claims of the ’833 patent. Accordingly, we institute an *inter partes* review of claims 1–5, 7, and 13–18 of the ’833 patent on the grounds asserted in the Petition.

The following preliminary findings of fact and conclusions of law are made solely for determining whether to institute review. Any final decision will be based on the full trial record.

II. BACKGROUND

A. *Related Matters*

Petitioner identifies the following non-PTAB proceedings as related matters involving the '833 patent:

- (1) *Daedalus Prime LLC v. Arrow Electronics, Inc. et al.*, 1:22-cv-01107 (D. Del.);
- (2) *Daedalus Prime LLC v. Mazda Motor Corporation et al.*, 1:22-cv-01109 (D. Del.);
- (3) *Daedalus Prime LLC v. Mazda Motor Corporation et al.*, 1:22-cv-01108 (D. Del.);
- (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352 (E.D. Tex.);
- (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, U.S. International Trade Commission (“ITC”) Inv. No. 337-TA-1335 (Violation); and
- (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, ITC Inv. No. 337-TA-1332 (Violation).

Pet. 2–3. Patent Owner identifies above proceedings (4) and (5). Paper 6 (Mandatory Notices) 1.

We note the following Board proceedings involve the same parties and related patents: IPR2023-00547 (Patent 10,705,588 B2); IPR2023-00567 (Patent 10,049,080 B2); and IPR2023-00617 (Patent 8,898,494 B2).

B. *Real Parties in Interest*

Petitioner identifies Qualcomm Incorporated and Qualcomm Technologies, Inc. as its real parties in interest. Pet. 2. Petitioner also identifies Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc., Mercedes-Benz Group AG, Mercedes-Benz

AG, Mercedes-Benz USA, LLC, and Visteon Corporation “as parties that Patent Owner has accused of infringing the ’833 Patent based on incorporation of Qualcomm products.” *Id.* Petitioner does not concede, however, that these parties are real parties in interest. *Id.*

Patent Owner identifies Daedalus Prime LLC as its real party in interest. Paper 6, 1.

C. Overview of the ’833 patent

The ’833 patent, titled “Dynamically Allocating a Power Budget Over Multiple Domains of a Processor,” relates to “a power balancing mechanism that can be implemented between the different domains of a multicore processor.” Ex. 1001, code [54], 2:14–17. As background, the ’833 patent states that “[o]ne issue that arises” with multicore processors “is that the different circuitry can consume differing amounts of power based on their workloads,” but that “suitable mechanisms to ensure that these different units have sufficient power do not presently exist.” *Id.* at 1:22–26.

The ’833 patent purports to solve this problem by providing a power budget management (“PBM”) algorithm that dynamically apportions power among multiple domains at run time. *Id.* at 1:56–58; *see also id.* at 2:14–17 (“Thus embodiments provide a power balancing mechanism that can be implemented between the different domains of a multicore processor.”). According to the ’833 patent, the PBM algorithm “may be executed by logic such as logic of a power control unit (PCU) of a processor to control the power of an entire processor or an individual domain to a configured power limit.” *Id.* at 2:32–36. The algorithm is based, in part, on “various processor parameters.” *Id.* at 2:36–37. These parameters include guaranteed frequency (P1), “which is a frequency that a domain is guaranteed to operate

at and not exceed power or thermal specifications of the product,” and maximum turbo frequency (P0), “which is a highest frequency at which a domain can operate.” *Id.* at 2:37–40, 3:1–3.

Figure 7, reproduced below, is a block diagram of one embodiment of a multicore processor according to the ’833 patent. *Id.* at 1:48–50.

400

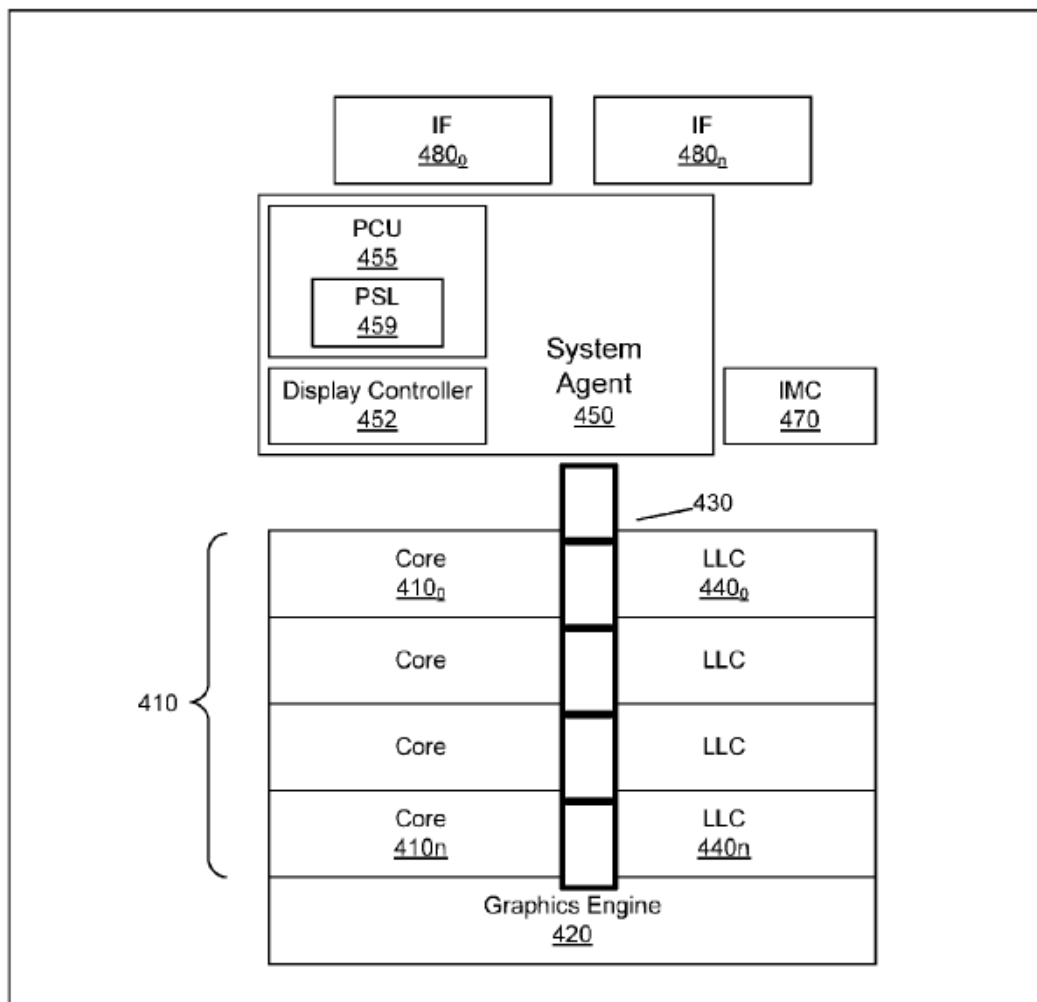


FIG. 7 is a block diagram of a processor according to the ’833 patent.

As shown, processor 400 includes: (1) a core domain 410 having a plurality of cores 410 a –410 n ; (2) last level caches (LLC) 440 o –440 n ; (3) a graphics domain 420 having one or more graphics engines; and (4) a system agent domain 450. *Id.* at 9:10–15, 9:33–35. A ring interconnect 430 couples the cores, and further interconnects the cores, graphics domain 420, and system agent domain 450. *Id.* at 9:40–44.

The system agent domain 450 includes a display controller 452 that provides a user interface, and a power control unit 455 having power sharing logic 459 to “execute algorithms . . . to thus dynamically share an available package power budget between the core domain and the graphics domain.” *Id.* at 9:50–54. The ’833 patent states that system agent domain 450 “may execute at a fixed frequency and may remain powered on at all times to handle power control events and power management such that domains 410 and 420 can be controlled to dynamically enter into and exit low power states.” *Id.* at 9:16–21.

D. The Challenged Claims

Petitioner challenges claims 1–5, 7, and 13–18 of the ’833 patent. Pet. 5–6. Of the challenged claims, claims 1 and 13 are independent. Claims 1 and 13 are illustrative of the claimed subject matter and reproduced below with Petitioner’s added identifiers bolded and in brackets.

1. **[pre]** A processor comprising:

[A] a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency;

[B] a memory controller coupled to the first and second domains;

[C] at least one interface; and

[D.i] first logic to dynamically allocate a power budget for the processor between the first and second domains at run time **[D.ii]** according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.

Ex. 1001, 11:26–38; Pet. 16–26 (identifiers).

13. **[pre]** A system comprising:

[A.i] a multicore processor having a first domain including a plurality of cores, a second domain including a graphics engine, and **[A.ii(1)]** a third domain including system agent circuitry, **[A.ii(2)]** the third domain to operate at a fixed power budget and **[A.ii(3)]** including a power sharing logic to dynamically allocate a variable power budget between the first and second domains **[A.ii(4)]** based at least in part on a first power sharing value for the first domain stored in a first storage and a second power sharing value for the second domain stored in a second storage; and

[B] a dynamic random access memory (DRAM) coupled to the multicore processor.

Ex. 1001, 12:52–64; Pet. 35–45 (identifiers).

E. Evidence

Petitioner submits the following evidence:

| Evidence | Exhibit No. |
|---|--------------------|
| Declaration of Dr. Trevor Mudge | 1002 |
| U.S. Published Patent Appl. No. 2010/0115304 A1 (“Finkelstein”) | 1005 |
| U.S. Published Patent Appl. No. 2007/0049133 A1 (“Conroy”) | 1006 |
| U.S. Published Patent Appl. No. 2011/0022356 A1 (“Nussbaum”) | 1007 |
| U.S. Published Patent Appl. No. 2009/0089602 A1 (“Bose”) | 1008 |

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

| Claims Challenged | 35 U.S.C. § | Reference |
|-----------------------|---------------------|---------------------|
| 1–5, 7 | 103(a) ¹ | Finkelstein |
| 7 | 103(a) | Finkelstein, Conroy |
| 13–15, 17, 18 | 103(a) | Nussbaum |
| 16 | 103(a) | Nussbaum, Bose |
| 13–15, 17, 18 | 103(a) | Conroy |
| 16 | 103(a) | Conroy, Bose |
| 1–5, 7, 13–15, 17, 18 | 103(a) | Conroy, Finkelstein |

Pet. 5–6. Patent Owner disputes Petitioner’s asserted grounds of unpatentability. *See generally* Prelim. Resp.

G. Overview of the Asserted Prior Art

We now provide brief summaries of the asserted references.

1. Finkelstein (Ex. 1005)

Finkelstein “relates to power management for multiple processor cores.” Ex. 1005 ¶ 1. According to Finkelstein, the power management system improves over the prior art by utilizing local throttling techniques on a per core basis in response to detection of excessive temperature at one or more of the cores. *Id.* ¶ 9.

¹ Congress amended §§ 102 and 103, among other sections, when it passed the Leahy-Smith America Invents Act (“AIA”). Pub. L. No. 112–29, § 3(c), 125 Stat. 284, 287 (2011). Petitioner does not identify whether the challenges are based on pre-AIA or post-AIA §§ 102 and 103. Because Petitioner asserts the “earliest possible priority for the ’833 Patent is September 6, 2011” (Pet. 8) and the AIA’s changes to §§ 102 and 103 impact only applications filed on or after March 16, 2013, we herein denote (for purposes of institution) Petitioner’s challenges as being based on pre-AIA statutes.

Figure 1, reproduced below, is a block diagram illustrating one embodiment of Finkelstein's power management system. *Id.* ¶ 5.

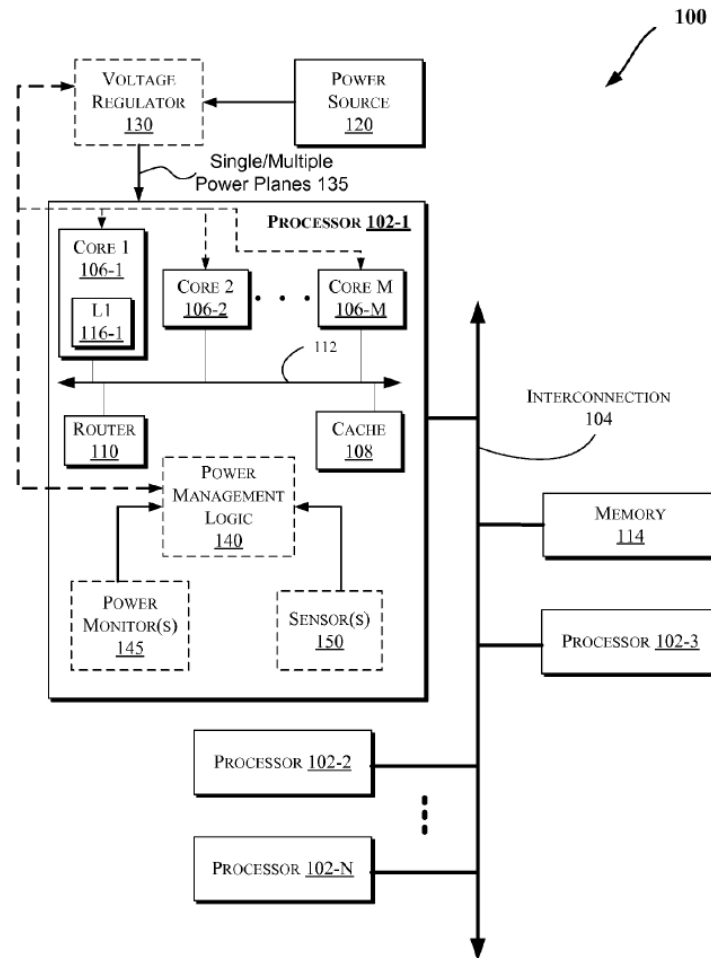


FIG. 1 is a block diagram of a power management system according to Finkelstein.

As shown, computing system 100 includes: (1) power source 120; (2) voltage regulator (“VR”) 130; (3) one or more processors 102-1 to 102-N (called “processor 102” or “processors 102”); (4) memory 114; and (5) bus 104 interconnecting processors 102 and memory 114. *Id.* ¶¶ 10, 13–14. Processor 102, in turn, includes: (1) one or more processor cores 106–1 to 106-M (called “core 106” or “cores 106”); (2) cache 108; (3) router 110, and (4) bus 112 connecting the cores 106, cache 108, and router 110. *Id.*

¶ 11. Processor 102 also includes power management logic 140 that controls power supply to the cores 106. *Id.* ¶ 16.

According to Finkelstein, power management logic 140 receives status information from sensors 150 monitoring the cores and interconnections for variations in, *e.g.*, temperature, operating frequency, operating voltage, power consumption, and inter-core communication activity. *Id.* The logic 140 causes the VR 130, power source 120, and/or individual components (*e.g.*, cores 106) to modify their operations, such as operating frequency and power consumption. *Id.*

2. *Conroy (Ex. 1006)*

Conroy relates to “methods and apparatuses to dynamically redistribute power in a system that includes a plurality of subsystems.” Ex. 1006, code (57). In one embodiment, Conroy’s system identifies a “load profile” and redistributes power between subsystems “while tracking the load profile.” *Id.* Conroy states that, if “a workload of one subsystem is substantially higher than the workload of another subsystem”—*i.e.*, an “asymmetric load profile”—then “the power of the system may be shifted toward the subsystem having a higher workload.” *Id.* ¶ 6. But, “[i]f the workloads of each of the subsystems are about the same”—*i.e.*, a “balanced load profile”—then “the power of the system may be distributed substantially evenly among the subsystems.” *Id.*

Conroy states that the load profile is identified based on a “utilization factor” for each of the subsystems. *Id.* The utilization factor may be determined in various ways, including by measuring the “actual power used by each of the subsystems” and by calculating “as a ratio of the actual power used by the subsystem to the power allocated to the subsystem.” *Id.* Conroy

then utilizes a “power weighting arrangement”—such as a power distribution table—to determine how to reallocate power to the subsystems.
Id.

3. *Nussbaum (Ex. 1007)*

Nussbaum “relates to power allocation in computer systems and more particularly to allocating power to improve performance.” Ex. 1007 ¶ 2. Nussbaum states that known “approaches for homogenously increasing power to all cores or to one or more cores based on performance states of the cores, allow for power to be reallocated from idle computational units, . . . but treat all active units homogeneously when dithering frequency or boosting steady state frequency.” *Id.* ¶ 19. Nussbaum states that a better approach is to “[s]electively distribut[e] power among the active cores or other computational units based on frequency sensitivity.” *Id.* But this approach, Nussbaum states, “requires an effective approach to identify workload sensitivity to changes in core frequency.” *Id.* Nussbaum provides systems and methods for “analysis of workload executed on computational units to help identify those computational units that are more performance sensitive to a change in performance capability caused by, e.g., a frequency change.” *Id.* ¶ 5.

Figure 1, reproduced below, is a block diagram illustrating one embodiment of Nussbaum’s power management system. *Id.* ¶ 10.

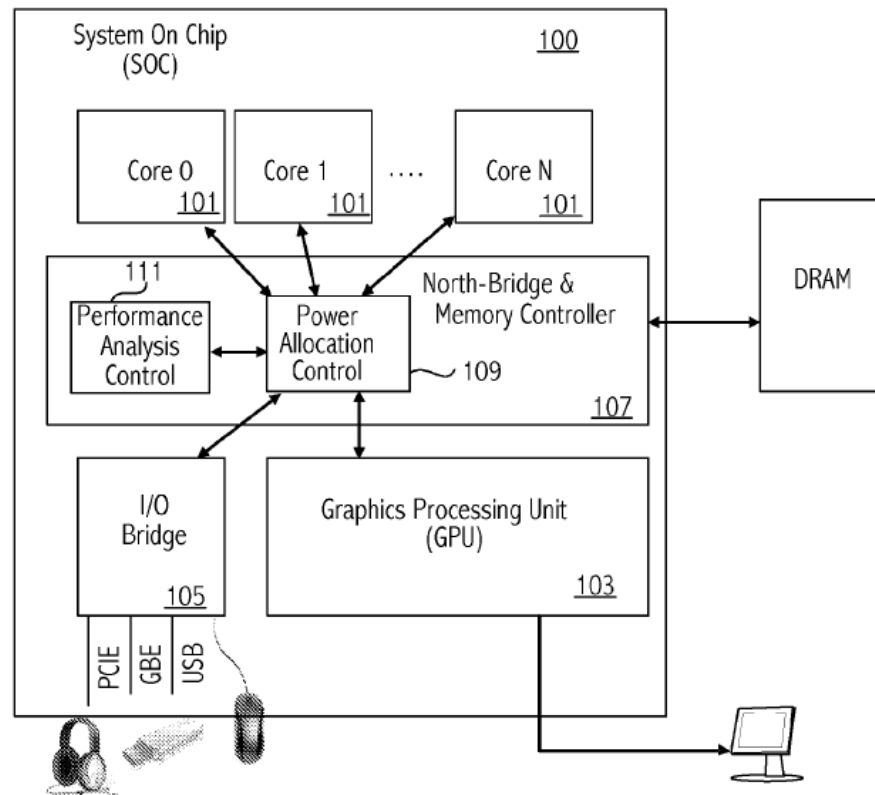


FIG. 1 is a block diagram of a power management system according to Nussbaum.

As shown, System on a Chip (SOC) 100 includes multiple CPU processing cores 101, a GPU (Graphics Processing Unit) 103, an I/O Bridge 105 (called “South-Bridge” in some embodiments) and a North-Bridge 107. *Id.* ¶ 20. Nussbaum states that North-Bridge 107 “may be combined with the Memory Controller in some embodiments.” *Id.* SOC 100 also includes a power allocation control 109, which Nussbaum describes as a “functional element.” *Id.* The performance analysis control 111 is logic that “analyzes performance sensitivity of the cores and other computational units.” *Id.*

In one embodiment, Nussbaum discloses the “reallocation of the power from idle or less active components to the busy components by having more power allocated to the busy ones.” *Id.* ¶ 23. Nussbaum states

that “one way to determine how to allocate power between” two cores (i.e., Core 0 and Core 1), “is to know which of the two cores, if any, can better exploit an increase in performance capability provided, e.g., by an increase in frequency.” *Id.* ¶ 25. Nussbaum describes the process of evaluating the “performance sensitivity of each computational unit to frequency change, and/or other change in performance capability” as determining “boost sensitivity” and states that it is “stored on a computational unit basis.” *Id.*

4. *Bose (Ex. 1008)*

Bose relates to the “power management of a system of connected components . . . wherein each component is assigned a power budget as determined by a number of allocated tokens in the token allocation map.” Ex. 1008, code (57). In Bose’s system, each token “connotes a pre-specified quantum of power, and as such, the total number of tokens owned by a component determines its own power limit.” *Id.* ¶ 68.

In one embodiment involving “multi-core chips or multiprocessor systems,” Bose utilizes a centralized bus “that has embedded space for token storage and specialized interfaces to support a token exchange protocol among the managed components of the system.” *Id.* ¶ 68. The bus “is also equipped with arbitration logic and protocol to determine the order in which multiple, simultaneous requests for token read/write operations are to be serviced.” *Id.* Bose states that “[e]ach managed component, in response to its own operating conditions (as evidenced by its utilization markers) can either attempt to donate one or more token(s) to the embedded token storage space within the centralized bus 905, or to read (receive) one or more token(s) from the bus 905.” *Id.*

Figure 13, reproduced below, provides a flowchart “illustrating a method of token-based control and management of peak power that presupposes a bus-based token exchange system used in the context of multi-core chips or multiprocessor systems.” *Id.* ¶ 30.

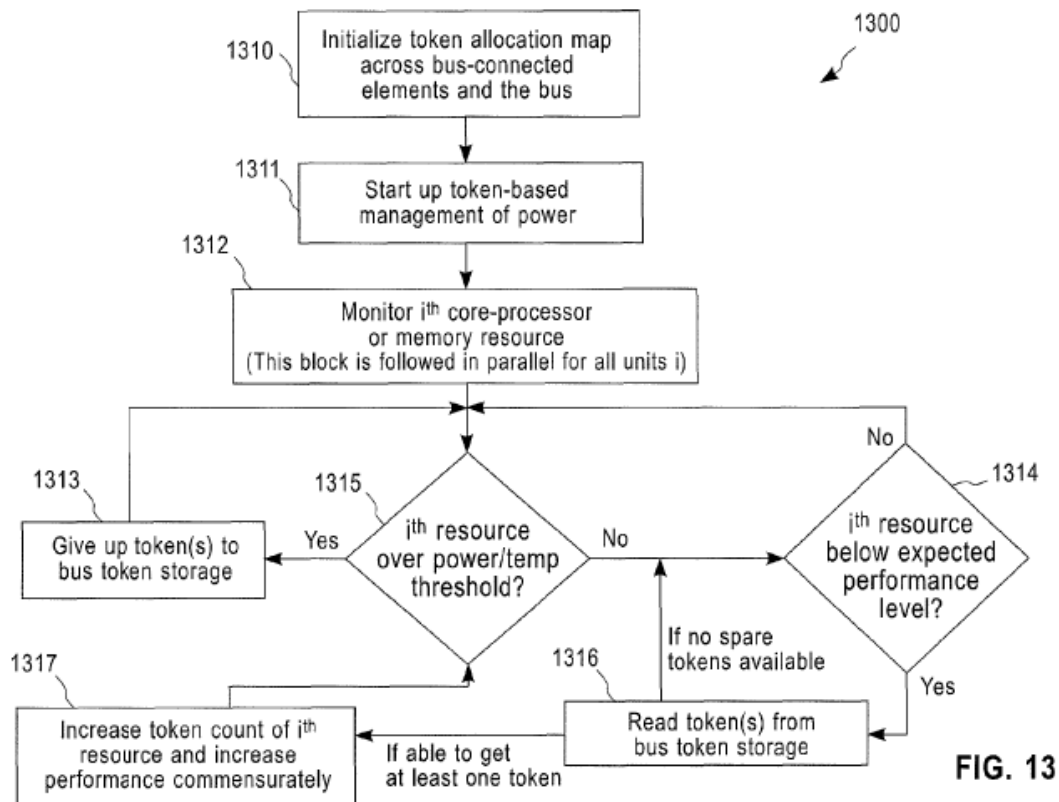


FIG. 13 is a flowchart of a token-based power management system according to Bose.

Bose states that, in block 1310, the initial token allocation map is set and applied across the managed units and the centralized bus, which has token storage space. *Id.* ¶ 85. The token managed system is started up in block 1311, and “each of the bus-connected resources is monitored for power and performance level in block 1312.” *Id.* Bose states that, when “a monitored unit is assessed to be above a predefined power or temperature threshold” in block 1315, the unit “is forced to give up one or more tokens to

the centralized bus token storage in block 1313.” *Id.* ¶ 86. But, when a monitored unit is “assessed to be below a predefined minimum performance,” then “block 1316 is used to try and read additional tokens from the centralized bus token storage.” *Id.* These extra tokens “are used to boost up performance in the targeted unit in block 1317 (e.g., by increasing its voltage and frequency, if allowed by the system architecture) and then block 1315 is again entered to check if the resource is within the power and temperature limits.” *Id.*

III. DISCUSSION

Petitioner contends that claims 1–5, 7, and 13–18 of the ’833 patent are unpatentable under 35 U.S.C. § 103 as obvious over various combinations of prior-art references Finkelstein, Conroy, Nussbaum, and Bose. A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103(a) (2006); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any objective indicia of nonobviousness.² *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness determination requires finding a reason to combine accompanied by a reasonable expectation of achieving what is

² At this time, Patent Owner does not assert objective indicia supporting nonobviousness of the challenged claims. *See generally* Prelim. Resp.

claimed in the challenged patent. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016). “[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *KSR*, 550 U.S. at 419–20.

In an *inter partes* review, “the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). Petitioner ultimately bears the burden of persuasion to prove unpatentability of each challenged claim by a preponderance of the evidence. 35 U.S.C. § 316(e). This burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). The Board may authorize an *inter partes* review if we determine that the information presented in the Petition and Patent Owner’s Preliminary Response shows that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the claims challenged in the petition. 35 U.S.C. § 314(a).

We organize our discussion into three sections. First, we address the level of ordinary skill in the art. Second, we address claim construction. And third, taking account of the information presented, we consider whether the Petition satisfies the threshold requirement for instituting an *inter partes* review under 35 U.S.C. § 314(a).

A. Level of Ordinary Skill in the Art

We consider the asserted grounds of unpatentability in view of the understanding of a person of ordinary skill in the art. In assessing the level of ordinary skill in the art, various factors may be considered, including (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983). Not all of these factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, “[t]hese factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art.” *Daiichi Sankyo Co. Ltd, Inc. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

Relying on the declaration testimony of Dr. Mudge, Petitioner contends that an ordinarily skilled artisan for the ’833 patent:

would have had a bachelor’s degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.

Pet. 8 (citing Ex. 1002 ¶¶ 25, 37–43). Patent Owner does not appear to address the level of ordinary skill in the art. *See generally* Prelim. Resp.

Based on the record presented, including our review of the ’833 patent and cited prior art, we agree with Petitioner’s proposed definition. Thus, we apply Petitioner’s definition for this decision. *See, e.g.*, Ex. 1001, 1:9–26

(describing in the “Background” section of the ’833 patent various conventional methods of computation and their alleged deficiencies).

B. Claim Construction

Next, we turn to claim construction. In interpreting the claims of the ’833 patent, we “us[e] the same claim construction standard that would be used to construe the claim[s] in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). The claim construction standard includes construing claims in accordance with the ordinary and customary meaning of such claims as would have been understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (*en banc*).

Petitioner states that it “does not believe that any term requires explicit construction.” Pet. 9 (citing Ex. 1002 ¶ 62). Patent Owner also does not present claim constructions nor assert whether any term requires express construction. *See generally* Prelim. Resp.

Having considered the record, we conclude that no terms require express interpretation at this time. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). Any final written decision entered in this case may include a final claim construction based on the full trial record that differs from any discussion of claim scope provided in our analysis below.

C. Asserted Grounds of Unpatentability

We now consider whether the Petition satisfies the threshold requirement for instituting an *inter partes* review under 35 U.S.C. § 314(a) by addressing each of Petitioner’s asserted grounds of unpatentability, below.

1. Alleged Obviousness of Claims 1–5 and 7 over Finkelstein

Petitioner contends that claims 1–5 and 7 of the ’833 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Finkelstein. Pet. 16–33. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 21–30. Having considered the arguments and evidence before us, we find that the record establishes a reasonable likelihood that Petitioner would prevail on this asserted ground of unpatentability. Nevertheless, we recognize that the issues in dispute are highly fact-intensive and implicate genuine issues of fact more appropriately resolved on a fully developed record.

a) Currently undisputed limitations I[pre], I[B], and I[C]

Taking claim 1 as illustrative, Petitioner provides a limitation-by-limitation analysis alleging that Finkelstein teaches or suggests each and every limitation of the claim and therefore renders claim 1 unpatentable for obviousness. Pet. 16–33. We have reviewed Petitioner’s contentions and supporting evidence regarding the currently undisputed limitations of claim 1, and are satisfied that the record establishes sufficiently for institution that Finkelstein teaches or suggests these limitations.

Specifically, as to the preamble³ (i.e., “[a] processor comprising”), Petitioner has shown sufficiently on this record and for institution that Finkelstein’s processor 102-1 satisfies the “processor” recited in the preamble. *See* Pet. 16–17 (citing Ex. 1005, Fig. 1; Ex. 1002 ¶¶ 64–66). As to limitation 1[B], (i.e., “a memory controller coupled to the first and second domains”), Petitioner has shown sufficient on this record that Finkelstein’s memory controller or hub satisfies this claim limitation. *See id.* at 19–21 (citing Ex. 1005 ¶¶ 11, 13, 49, Fig. 1; Ex. 1002 ¶¶ 72–75). And, as to limitation 1[C] (i.e., “at least one interface”), Petitioner has shown sufficiently on this record and for institution that Finkelstein’s disclosure of “buses or interconnections (such as a bus or interconnection 112)” satisfies this claim limitation. *See id.* at 21–22 (citing Ex. 1005 ¶¶ 11–13, 47, 48, Fig. 1; Ex. 1002 ¶¶ 76–78).

b) Limitation 1[A]

We now turn to the disputed limitations. Limitation 1[A] recites “a first domain and a second domain, each of the first and second domains to operate at an independent voltage and frequency.” Ex. 1001, 11:27–29. Petitioner contends that Finkelstein’s “multiple power planes 135” satisfies this limitation. Pet. 17–19 (citing Ex. 1005 ¶¶ 14, 16, 24, 27, 31, 32, 39, Fig. 1). Specifically, Petitioner contends that Finkelstein’s multiple power planes (each including a set of processor cores) correlates to the claimed “first domain” and “second domain,” and that each power plane operates at

³ Neither party takes a position on whether the preambles to the claims are limiting. At this stage of the proceeding, we accept Petitioner’s showing that the preambles are taught by the prior art, without deciding whether the preambles are limiting.

an independent voltage and frequency. *Id.* Petitioner contends that, because Finkelstein teaches that its power management logic can “throttle or modify an operational characteristic of *one* or more of the cores 106 (such as an operating voltage and/or an operating frequency of *a processor core* 106),” an ordinarily skilled artisan would have been motivated to operate the cores (and thus the claimed “domains”) at independent voltages and frequencies. *Id.* at 18–19 (quoting Ex. 1005 ¶ 24).

In response, Patent Owner argues that Petitioner fails to demonstrate that Finkelstein’s power planes operate at an independent voltage and frequency. Prelim. Resp. 21–22. Patent Owner argues that “merely operating at *different* voltages or frequencies does not demonstrate that voltages or frequencies operate *independently* as claimed.” *Id.*

We have considered the parties’ respective arguments and evidence, and determine, on this record and for institution, that Petitioner has met the reasonable likelihood standard for moving forward with trial. Finkelstein discloses that its power management logic 140 can “throttle or modify” operating voltage and/or operating frequency “of *a processor core* 106.” Ex. 1005 ¶ 24 (emphasis added). This disclosure appears to support Petitioner’s contention that the domains can operate at an independent voltage and frequency as claimed.

But even if Patent Owner’s characterization of Finkelstein is correct, the dispute between the parties appears to become one of claim construction, and neither party has set forth a construction for limitation 1[A] at this stage of the proceeding. It is not clear to us, at least on this record, that the claim language “to operate at an independent voltage and frequency” requires that

the voltages and frequencies be *set* independently of the first voltage, as Patent Owner appears to argue.

For these reasons, we determine that Petitioner, on this record and for institution, has shown sufficiently that Finkelstein’s power planes satisfy limitation 1[A]. The parties are encouraged to further develop the record on claim construction if necessary.

c) Limitation 1[D.i]

Limitation 1[D.i] recites “first logic to dynamically allocate a power budget for the processor between the first and second domains at run time.” Ex. 1001, 11:33–35. For this limitation, Petitioner relies on Finkelstein’s disclosure of the “processors having multiple power planes” that, because they “shar[e] the same power source 120,” also “share a common package power/energy budget.” Pet. 22–23 (citing Ex. 1005 ¶ 26). Petitioner contends that an ordinarily skilled artisan “would have recognized that Finkelstein teaches allocating a power budget between the first and second domains ‘at run time,’” because Finkelstein teaches that “unused processor core power” can be used for “more Graphics Effect(s) (GFX) performance in a GFX intensive workload.” *Id.* (citing Ex. 1005 ¶ 26; Ex. 1002 ¶ 80). Petitioner correlates the “unused processor core power” as that from the claimed first domain, and the GFX performance to “a core in the second domain.” *Id.*

In response, Patent Owner argues that Petitioner fails to show that the alleged domains in Finkelstein “share a power budget” and that Finkelstein’s graphics circuit satisfies the claimed “second domain.” Prelim. Resp. 22–24. Although we have considered Patent Owner’s argument, we determine that Petitioner has met the reasonable likelihood standard for moving

forward with trial. Finkelstein discloses that processors having multiple power planes may share “the same power source 120” and, correspondingly, “a common package power/energy budget.” Ex. 1005 ¶ 26. We credit Dr. Mudge’s currently unrebutted testimony—on this record and for institution—that graphics effects are “being performed by a core in the second domain (e.g., Core 2)” as claimed. Ex. 1002 ¶ 80.

d) Limitation 1[D.ii]

Turning to the final disputed limitation of claim 1, limitation 1[D.ii] recites “according to a first sharing policy value for the first domain and a second sharing policy value for the second domain, the first and second sharing policy values controllable by user-level software.” Ex. 1001, 11:35–38. For this limitation, Petitioner relies on two “approaches” in Finkelstein that Petitioner contends “dynamically allocate a power budget according to a first sharing policy value for the first domain and a second sharing policy value for the second domain.” See Pet. 24–26 (describing the “first approach” as involving a set of energy sharing policy values for each plane “i” and the “second approach” involving a set of sharing policy values based on Thermal Design Power (TDP) power limit).

We discuss the “first approach” as an example. In this approach, Petitioner relies on Finkelstein’s equation:

$$E^{k,i} = W_{ki} E^k$$

Id. at 24–25. Petitioner contends that E^k represents the “unused budget” for a “particular power plane,” and that “vectors W_{ki} ”—which Petitioner correlates to the claimed first and second sharing policy values—are “used to determine $E^{k,i}$, which represents the portion of the power budget plane ‘i’

may obtain.” *Id.* at 24 (citing Ex. 1005 ¶ 34). Petitioner also contends that W_{k1} and W_{k2} (i.e., the policy sharing values for the first domain and second domain, respectively), “are controllable by user-level software,” such as via a graphical interface. *Id.* at 25 (citing Ex. 1005 ¶¶ 34–35; Ex. 1002 ¶ 84).

In response, Patent Owner argues that “Petitioner’s ‘First Approach’ does not identify a ‘power budget’ allocated according to the first and second sharing policy values as claimed.” Prelim. Resp. 25. Patent Owner appears to argue that the “unused” power budget is not, in fact, a “power budget” because it is a variable that “is a function of $[W_{ki}]$ vectors.” *Id.* at 24. Patent Owner argues that the variable merely illustrates that the power plane does not utilize all the power budgeted to it, and does not show that that unused power budget can be allocated to a different domain. *Id.* at 24–25.

Again, although we have considered Patent Owner’s arguments, we determine that Petitioner has met the reasonable likelihood standard for moving forward with trial. In this regard, we determine that Petitioner—on this record and for institution—sufficiently shows that Finkelstein teaches a power management approach where unused power from one power plane may be distributed to another power plane based on sharing policy values represented by W_{ki} . Indeed, Finkelstein teaches that, for “different power planes,” “user (or application defined) preferences that describe how budget E^k is distributed among power planes . . . may be provided as input in the form of vectors W_k .” Ex. 1005 ¶ 34. And Finkelstein teaches that, when power allocated to a particular power plane “is high enough to provide maximal turbo,” “the ‘unused’ budget for this power plane . . . may be distributed among the rest of the power planes proportionally to their

weights” (i.e., W_{ki}). *Id.* at 35. Thus, Finkelstein’s disclosure—at least on this record—supports Petitioner’s contentions that the “power budget” is the unused power from one power plane that is available for distribution to the remaining power planes based on their weighted sharing policy values W_{ki} .

Patent Owner makes similar arguments that there is no “power budget” under Petitioner’s second approach. Prelim. Resp. 25–26. For similar reasons, however, and based on the current record, we determine that Petitioner’s second approach is also sufficient for meeting the reasonable likelihood standard for moving forward with trial.

e) Claims 2–5 and 7

We have reviewed Petitioner’s contentions that Finkelstein teaches or suggests the limitations recited in claims 2–5 and 7. Pet. 26–33. Patent Owner’s arguments about these claims generally are rooted in its arguments as to claim 1 (i.e., that Finkelstein fails to teach or suggest allocation of power budget among domains based on policy values). *See generally* Prelim. Resp. 26–30. On this record and for institution, we determine that Petitioner has shown sufficiently that Finkelstein teaches or suggests the limitations of these claims.

f) Summary

Accordingly, for the reasons set forth above and based on the totality of the evidence currently in the record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claims 1–5 and 7 of the ’833 patent as unpatentable for obviousness over Finkelstein.

2. *Alleged Obviousness of Claim 7 over Finkelstein and Conroy*

Petitioner contends that claim 7 of the '833 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over Finkelstein and Conroy. Pet. 33–34. Claim 7 depends from claim 1 and states that the claimed logic “dynamically allocate[s] substantially all of the power budget to the first domain for a first workload,” and then to “the second domain for a second workload.” Ex. 1001, 12:1–6. Petitioner contends that the combination of Finkelstein and Conroy teaches or suggests claim 7, and that an ordinarily skilled artisan would have had a reason to combine the references with a reasonable expectation of success. Pet. 33–34 (citing Ex. 1002 ¶¶ 106–111; Ex. 1005 ¶ 26; Ex. 1006, code [54], ¶¶ 6, 196).

Because we determined above that Petitioner demonstrated a reasonable likelihood of prevailing in its challenge to at least one claim of the '833 patent, we institute *inter partes* review on all claims and grounds, including this claim (i.e., claim 7) and this ground. See 37 C.F.R. § 42.108(a) (“When instituting . . . review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”). In this section, therefore, we will focus on Patent Owner’s arguments.

Patent Owner argues that Petitioner has failed to provide an adequate rationale for combining Finkelstein with Conroy. Prelim. Resp. 30–34. For example, Patent Owner argues that Petitioner’s rationale for the combination is based on hindsight and is inconsistent with Petitioner’s contention that the subject matter of claim 7 would have been obvious based on Finkelstein alone. *Id.* As to the latter, Patent Owner argues that Petitioner’s allegations

“that Finkelstein already discloses the additional limitations of claim 7 itself, . . . goes against any alleged motivation to combine it with Conroy.” *Id.* at 34.

As an initial matter, we do not view Petitioner’s contention that claim 7 would have been obvious over Finkelstein as necessarily contradictory to its contention that claim 7 also would have been obvious over Finkelstein and Conroy. We are unaware of any case holding that, when a first reference suggests certain subject matter, a second reference cannot be combined with the first reference as further support for the obviousness of that subject matter.

In any event, we understand Petitioner’s argument as to claim 7 to be that an ordinarily skilled artisan would have understood that Finkelstein’s power management system would dynamically allocate “substantially all” of its power budget to the first domain and thereafter to a second domain given Finkelstein’s disclosure that—in some scenarios involving multiple power planes sharing a single power budget—“a single power plane may obtain the entire budget.” Pet. 32 (quoting Ex. 1005 ¶ 34; citing *id.* ¶¶ 26, 28). We further understand Petitioner’s argument as to the combination of Finkelstein and Conroy to be that Conroy expressly states that “higher power draw is allocated to and allowed for the subsystem having a higher workload.” *Id.* at 33–34 (quoting Ex. 1006 ¶ 6). In our view, that Conroy arguably goes further in explaining that more power is allocated to a domain having a higher workload does not necessarily negate Petitioner’s argument that an ordinarily skilled artisan would have already understood that principle from Finkelstein. Patent Owner does not, on this record, adequately explain why Petitioner’s contentions are not supported by the references.

For these reasons, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claim 7 of the '833 patent as unpatentable for obviousness over Finkelstein and Conroy.

3. *Alleged Obviousness of Claims 13–15, 17, and 18 over Nussbaum*

Petitioner contends that claims 13–15, 17, and 18 of the '833 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Nussbaum. Pet. 35–50. Patent Owner disputes Petitioner's contentions. Prelim. Resp. 34–40. Having considered the arguments and evidence before us, we find that the record establishes a reasonable likelihood that Petitioner would prevail on this asserted ground of unpatentability. Nevertheless, we recognize that the issues in dispute are highly fact-intensive and implicate genuine issues of fact more appropriately resolved on a fully developed record.

a) *Currently undisputed claim limitations*

Taking independent claim 13 as illustrative, Petitioner provides a limitation-by-limitation analysis alleging that Nussbaum teaches or suggests each and every limitation of the claim and therefore renders claim 13 unpatentable for obviousness. Pet. 16–33. At this stage of the proceeding, Patent Owner disputes Petitioner's contentions as to limitations 13[A.1] and 13[A.ii(4)]. Prelim. Resp. 34–37.

We have reviewed Petitioner's contentions and supporting evidence regarding the currently undisputed limitations of claim 13, and are satisfied that the record establishes sufficiently for institution that Nussbaum teaches or suggests these limitations. Thus, we agree with and adopt Petitioner's detailed mapping of: the preamble, *see* Pet. 35 (citing Ex. 1007 ¶¶ 10, 31, 43, Fig. 1; Ex. 1002 ¶¶ 112–114); limitation 13[A.ii(1)], *see id.* at 38–40

(citing Ex. 1007 ¶¶ 20–24, 39, Fig. 1, Tables 1 & 2; Ex. 1002 ¶¶ 121–125); limitation 13[A.ii(2)], *see id.* at 40–41 (citing Ex. 1007 ¶¶ 20–24, 39, Fig. 1, Tables 1 & 2; Ex. 1002 ¶¶ 126–129); limitation 13[A.ii(3)], *see id.* at 41–42 (citing Ex. 1007 ¶¶ 19–25, 36, 39, Fig. 1; Ex. 1002 ¶¶ 130–133); and limitation 13[B], *see id.* at 44–45 (citing Ex. 1007 ¶ 43, Fig. 1; Ex. 1002 ¶¶ 138–140).

b) Limitation 13[A.i]

We now turn to the disputed limitations. Limitation 13[A.i] recites “a multicore processor having a first domain including a plurality of cores” and “a second domain including a graphics engine.” Ex. 1001, 12:52–55. For this limitation, Petitioner relies on an annotated version of Nussbaum’s Figure 1, which we reproduce below:

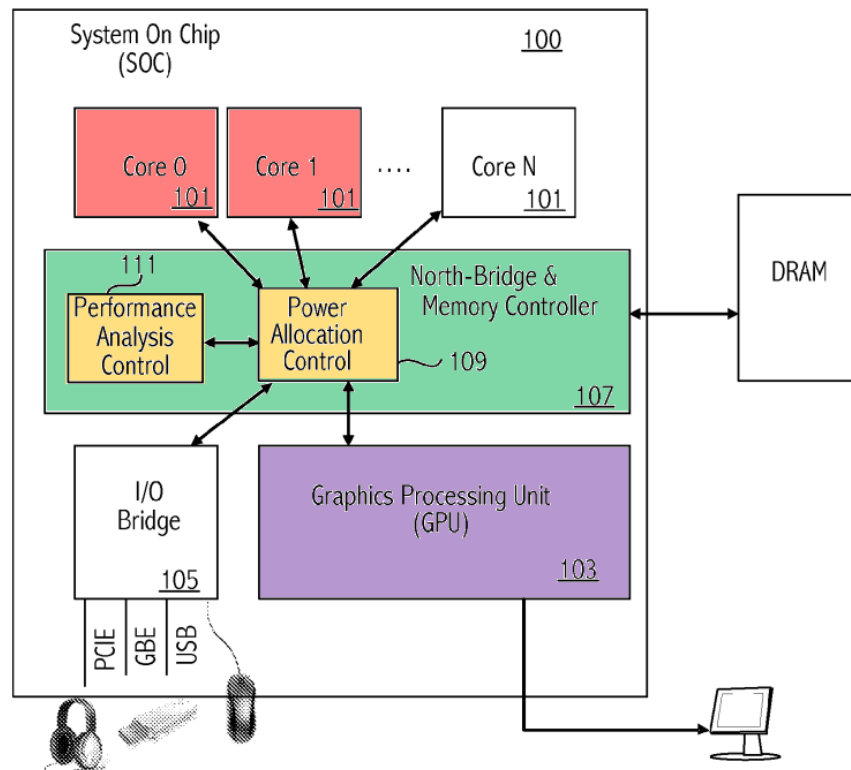


FIG. 1

Pet. 36. Figure 1 depicts Nussbaum's System On Chip (SOC) 100. In its annotated version of Figure 1, Petitioner highlights Core 0 and Core 1 in red and the Graphics Processing Unit (GPU) in purple. *Id.* at 36–37. Petitioner contends that Core 0 and Core 1 represent “a plurality of cores” in a first domain, while the GPU represents “a second domain including a graphics engine.” *Id.* As to the cores, Petitioner contends that an ordinarily skilled artisan would recognize that the cores are in the same power domain (i.e., “first domain”), because Nussbaum teaches that the plurality of cores “are equally boosted to a higher F, V to fill new power headroom” and Tables 1 and 2 of Nussbaum show Core 0 and Core 1 having the same allocated power. *Id.* (citing Ex. 1007 ¶¶ 21–24, Tables 1–2; Ex. 1002 ¶ 118).

In response, Patent Owner argues that Petitioner fails to demonstrate that Nussbaum's plurality of cores are included in a “first domain.” Prelim. Resp. 34–36. Patent Owner argues that “merely having multiple cores does not render them a ‘first domain.’” *Id.* at 34.

We have considered the parties' respective arguments and evidence, and determine, on this record and for institution, that Petitioner has met the reasonable likelihood standard for moving forward with trial. As Petitioner points out, the '833 patent states that “[a]s used herein the term ‘domain’ is used to mean a collection of hardware and/or logic that operates at the same voltage and frequency point.” Ex. 1001, 1:58–60; *see also* Pet. 36.

Nussbaum's cores appear to meet this definition, given that Tables 1 and 2 show Core 0 and Core 1 allocated the same power—i.e., 8 watts in Table 1 and 16.75 watts in Table 2. Ex. 1007 ¶¶ 21–24, Tables 1 & 2. We further accept for institution Dr. Mudge's currently un rebutted testimony that an

ordinarily skilled artisan “would have understood this to mean that Core 0 and Core 1 are operating in the same power domain.” Ex. 1002 ¶ 118.

c) Limitation 13[A.ii(4)]

Limitation 13[A.ii(4)] recites that the claimed system’s power sharing logic dynamically allocates power budget between the first and second domains “based at least in part on a first power sharing value for the first domain stored in a first storage and a second power sharing value for the second domain stored in a second storage.” Ex. 1001, 12:57–62. Petitioner maps Nussbaum’s “boost sensitivities” for computational units to the first and second power sharing values. Pet. 43–44 (citing Ex. 1007 ¶¶ 19–25). Petitioner contends that Nussbaum’s boost sensitivity “indicates a ‘performance sensitivity of each computational unit to frequency change, and/or other change in performance capability.’” *Id.* at 43 (citing Ex. 1007 ¶¶ 19–25). Patent Owner, in response, argues that “Nussbaum’s cores do not share a boost sensitivity,” and, accordingly, Nussbaum does not satisfy the claim language of “a first power sharing value for the first domain.” Prelim. Resp. 36 (citing Ex. 1007 ¶ 25).

We have considered Patent Owner’s argument, but determine, on this record and for institution, that Petitioner has met the reasonable likelihood standard for moving forward with trial. Patent Owner’s argument relies on its position that Nussbaum fails to teach or suggest a first domain including a plurality of cores, which we do not find persuasive for the reasons explained above. Thus, while we agree with Patent Owner on this record that *each computational unit* in Nussbaum appears to have its own boost sensitivity, we accept for institution Petitioner’s contention that each computational unit

of Nussbaum may include a plurality of cores for the reasons explained above. *See supra* § III.3.b.

d) Claims 14, 15, 17, and 18

We have reviewed Petitioner’s contentions that Nussbaum teaches or suggests the limitations recited in claims 14, 15, 17, and 18. Pet. 45–50. Patent Owner’s arguments about these claims generally are rooted in its arguments as to claim 13 (i.e., that Nussbaum fails to teach or suggest multiple cores in the same domain). *See generally* Prelim. Resp. 37–40. On this record and for institution, we determine that Petitioner has shown sufficiently that Nussbaum teaches or suggests the limitations of these claims.

e) Summary

Accordingly, for the reasons set forth above and based on the totality of the evidence currently in the record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claims 13–15, 17, and 18 of the ’833 patent as unpatentable for obviousness over Nussbaum.

4. Alleged Obviousness of Claim 16 over Nussbaum and Bose

Petitioner contends that claim 16 of the ’833 patent is unpatentable under 35 U.S.C. § 103(a) as obvious over Nussbaum and Bose. Pet. 50–53. Claim 16 depends indirectly from independent claim 13 and recites that the power sharing logic “increment[s] the first power sharing value when a request for a higher frequency for the first domain is not granted, and . . . increment[s] the second power sharing value when a request for a higher frequency for the second domain is not granted.” Ex. 1001, 13:11–16.

Petitioner contends that the combination of Nussbaum and Bose teaches or suggests claim 16, and that an ordinarily skilled artisan would have had a reason to combine the references with a reasonable expectation of success. Pet. 50–53 (citing Ex. 1002 ¶¶ 155–159; Ex. 1007 ¶¶ 7, 27, 30, 32; Ex. 1008, code [57], ¶¶ 38, 39, 68, 86, Fig. 13). Again, in light of 35 U.S.C. § 314(a), we institute *inter partes* review of claim 16 on this ground of unpatentability, and therefore will focus on Patent Owner’s arguments below.

Patent Owner argues that Petitioner has failed to provide an adequate rationale for combining Nussbaum and Bose. Prelim. Resp. 40–42. For example, Patent Owner argues that Petitioner’s rationale for the combination is based on hindsight, and that, “Nussbaum’s ‘boost sensitivities’ are incompatible with Bose’s tokenizing power allocation because the sensitivities are calculated (not expected to be whole numbers), and therefore not capable of being assigned a whole number of tokens.” *Id.* at 41 (citing Ex. 1008 ¶ 68). Although we have considered Patent Owner’s argument, we determine that Petitioner has met the reasonable likelihood standard for moving forward with trial. In this regard, Patent Owner’s argument appears to require the bodily incorporation of Bose’s tokens into Nussbaum, which is not required for obviousness. *See, e.g., Facebook, Inc. v. Windy City Innovations, LLC*, 973 F.3d 1321, 1343 (Fed. Cir. 2020) (“[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference”).

Patent Owner also argues that neither Nussbaum nor Bose teach or suggest “increment[ing] the first power sharing value” as claimed. Prelim.

Resp. 42. Bose, Patent Owner argues, “explicitly describes the opposite” because, in Bose’s system, “when a request for a higher token count is not granted, the component must ‘wait,’ and cannot increase its token count.” *Id.* at 42–43. We find that Patent Owner’s argument has merit.

Nussbaum expressly contemplates reevaluating (and changing) the boost sensitivity based on changes in the current processor context and/or expiration of a timer. *See* Ex. 1007 ¶ 30 (stating that, in some implementations, “both a timer and context switch, whichever occurs first, are used to initiate the boost sensitivity reevaluation”). Nussbaum, however, does not appear to expressly contemplate what happens when “a request for a higher frequency . . . is not granted” because Nussbaum appears to assume sufficient power for each component.

We understand Petitioner’s argument to be that an ordinarily skilled artisan would have found it obvious to increment a particular component’s share of a power budget after denial of a power request based on Bose. Pet. 52–53. But Bose’s Figure 13 appears to show only that, when a request for additional tokens is denied, then that component’s “ith resource” is reevaluated for below-expected performance level. Ex. 1008 ¶ 86, Fig. 13. Put differently, although Bose appears to expressly contemplate what happens when “a request for a higher frequency . . . is not granted,” Bose does not appear to teach or suggest that the power sharing value for the underperforming component is necessarily incremented after that denial. *See* Pet. 52 (contending that “Bose explains that if no additional tokens can be allocated to the particular resource at the moment (i.e., a request for a higher frequency is not granted), that particular resource can wait for its token count to be increased in the next iteration of the process.”). During

trial, the parties should address how Bose’s process utilizes “incrementing” in the manner claim 16 requires.

5. *Alleged Obviousness of Claims 13–15, 17, and 18 over Conroy*

Petitioner contends that claims 13–15, 17, and 18 the ’833 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Conroy. Pet. 54–66. Again, in light of 35 U.S.C. § 314(a), we institute *inter partes* review of claims 13–15, 17, and 18 on this ground of unpatentability. Patent Owner’s arguments about this particular ground of unpatentability appear to be substantially similar to those presented with respect to the above grounds, and are not persuasive on this record for the reasons discussed above. *See* Prelim. Resp. 43–46. Given the fact-intensive nature of the parties’ dispute, we will evaluate this ground on the record that is developed during trial.

6. *Alleged Obviousness of Claim 16 over Conroy and Bose*

Petitioner contends that claim 16 of the ’833 patent is unpatentable under 35 U.S.C. § 103(a) as obvious Bose. Pet. 66–68. Again, in light of 35 U.S.C. § 314(a), we institute *inter partes* review of claim 16 on this ground of unpatentability. Patent Owner’s arguments about this particular ground of unpatentability appear to be substantially similar to those presented with respect to the above grounds, and are not persuasive on this record for the reasons discussed above. *See* Prelim. Resp. 46–48. Given the fact-intensive nature of the parties’ dispute, we will evaluate this ground on the record that is developed during trial.

7. *Alleged Obviousness of Claims 1–5, 7, 13–15, 17, and 18 over Conroy and Finkelstein*

Petitioner contends that claims 1–5, 7, 13–15, 17, and 18 of the ’833 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Conroy

and Finkelstein. Pet. 68–83. Again, in light of 35 U.S.C. § 314(a), we institute *inter partes* review of claims 1–5, 7, 13–15, 17, and 18 on this ground of unpatentability. Patent Owner’s arguments about this particular ground of unpatentability appear to be substantially similar to those presented with respect to the above grounds, and are not persuasive on this record for the reasons discussed above. *See* Prelim. Resp. 48–56. Given the fact-intensive nature of the parties’ dispute, we will evaluate this ground on the record that is developed during trial.

IV. CONCLUSION

After considering the arguments presented in the parties’ papers and the evidence of record, we determine that Petitioner has demonstrated at least a reasonable likelihood of success in proving that at least one claim of the ’833 patent is unpatentable. Thus, we institute an *inter partes* review of all challenged claims on all grounds set forth in the Petition. Our determinations at this stage of the proceeding are based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which we have instituted an *inter partes* review. *See TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner’s burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving invalidity by a preponderance of the evidence at trial”). We will base any final decision on the full record developed during trial.

V. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1–5, 7, and 13–18 of the ’833 patent on the unpatentability grounds asserted in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision.

IPR2023-00550
Patent 8,775,833 B2

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