



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/655,438	06/04/2019	10312335	200371.00125	5778

24998 7590 05/15/2019
Blank Rome LLP
1825 Eye Street, NW
Washington, DC 20006-5403

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Jianjun Cao, Torrance, CA;
Efficient Power Conversion Corporation, El Segundo, CA;
Alexander Lidow, Santa Monica, CA;
Alana Nakata, Redondo Beach, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)

PART B-FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By fax, send to: (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24998
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
15/655,438	07/20/2017	Jianjun Cao	200371.00125	5778

TITLE OF INVENTION: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500.00			\$500.00	05/13/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
J. C. Niesz	2822	

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Blank Rome LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE or COUNTRY)

Efficient Power Conversion Corporation

El Segundo, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees Submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment (Please first reapply any previously paid fee shown above):

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 23-2185

5. Change of Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27.
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid Certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

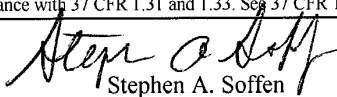
NOTE: If the application was previously under micro entity status, checking this box will be taken as a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken as a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature

Typed or printed name


Stephen A. Soffen

Date April 19, 2019

Registration No. 31,063

PTOL-85 Part B (08-18) Approved for use through 01/31/2020

OMB 0651-0033

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

200371.00125/119163813v.1

Electronic Patent Application Fee Transmittal				
Application Number:		15655438		
Filing Date:		20-Jul-2017		
Title of Invention:		GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS		
First Named Inventor/Applicant Name:		Jianjun Cao		
Filer:		Stephen A. Soffen/Cheryl de Lopez		
Attorney Docket Number:		200371.00125		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	500	500

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				500

Electronic Acknowledgement Receipt	
EFS ID:	35774311
Application Number:	15655438
International Application Number:	
Confirmation Number:	5778
Title of Invention:	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl de Lopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	200371.00125
Receipt Date:	19-APR-2019
Filing Date:	20-JUL-2017
Time Stamp:	10:25:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 500
RAM confirmation Number	041919INTEFSW10260400
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	issuefee125.pdf	83577	no	1
			29c46ce591d6013d9602c2616c9637e42aa8d94f		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30438	no	2
			d66fdda9f635fff87a690a4700cddb05efacd9a0		
Warnings:					
Information:					
Total Files Size (in bytes):			114015		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

24998 7590 02/12/2019
Blank Rome LLP
1825 Eye Street, NW
Washington, DC 20006-5403

EXAMINER

NIESZ, JAMIE C

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 02/12/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/655,438	07/20/2017	Jianjun Cao	E0101.0032-A	5778

TITLE OF INVENTION: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0.00	\$0.00	\$500	05/13/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

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24998 7590 02/12/2019
Blank Rome LLP
1825 Eye Street, NW
Washington, DC 20006-5403

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(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/655,438	07/20/2017	Jianjun Cao	E0101.0032-A	5778

TITLE OF INVENTION: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0.00	\$0.00	\$500	05/13/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
NIESZ, JAMIE C	2822	257-194000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/655,438	07/20/2017	Jianjun Cao	E0101.0032-A	5778
24998	7590	02/12/2019	EXAMINER	
Blank Rome LLP 1825 Eye Street, NW Washington, DC 20006-5403			NIESZ, JAMIE C	
			ART UNIT	PAPER NUMBER
			2822	
DATE MAILED: 02/12/2019				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/655,438	Applicant(s) Cao et al.	
	Examiner JAMIE C NIESZ	Art Unit 2822	AIA Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed October 31, 2018.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1,5-8 and 10-11. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	5. <input type="checkbox"/> Examiner's Amendment/Comment
2. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.	6. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance
3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. <input type="checkbox"/> Other _____.
4. <input type="checkbox"/> Interview Summary (PTO-413), Paper No./Mail Date. _____.	

/JAMIE C NIESZ/ Primary Examiner, Art Unit 2822	
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DETAILED ACTION

1. This office action is in response to the amendment filed October 31, 2018.

Notice of Pre-AIA or AIA Status

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Objections

3. The objection to claim 1 has been obviated by amendment and is therefore withdrawn.

Allowable Subject Matter

4. Claims 1, 5-8, 10 and 11 are allowed.
5. The following is an examiner's statement of reasons for allowance:
6. Regarding claim 1, the prior art of record fails to disclose "the p-type gate material having side surfaces extending horizontally towards the source contact and the drain contact, respectively, and contacting the barrier layer" and "wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact" in combination with the rest of the limitations in the claim. These limitations, in the device as claimed in claim 1, are neither anticipated nor made obvious by the prior art of record, in the Examiner's opinion.
7. Claims 5-7 depend from claim 1 and are therefore also found allowable.

8. Regarding claim 8, the prior art of record fails to disclose wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and the drain contact, respectively; and (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer” in combination with the rest of the limitations in the claim. These limitations, in the device as claimed in claim 8, are neither anticipated nor made obvious by the prior art of record, in the Examiner’s opinion.

9. Claims 10 and 11 depend from claim 8 and are therefore also found allowable.

10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMIE C NIESZ whose telephone number is (303)297-4333. The examiner can normally be reached on M-F 9 a.m. - 5 p.m.

12. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMIE C NIESZ/
Primary Examiner, Art Unit 2822

<i>Notice of References Cited</i>	Application/Control No. 15/655,438		Applicant(s)/Patent Under Reexamination Cao et al.	
	Examiner JAMIE C NIESZ		Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20060273347-A1	12-2006	Hikita; Masahiro	H01L29/66462	257/192
*	B	US-20060157735-A1	07-2006	Kanamura; Masahito	H01L29/42316	257/194
*	C	US-20090072272-A1	03-2009	Suh; Chang Soo	H01L29/1066	257/194
*	D	US-20100258843-A1	10-2010	Lidow; Alexander	H01L29/1066	257/192
*	E	US-20040119110-A1	06-2004	Park, Sung-Chul	H01L21/28273	257/315
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS


*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)

Notice of References Cited

Part of Paper No. 20190115a

<i>Search Notes</i> 	Application/Control No. 15/655,438	Applicant(s)/Patent Under Reexamination Cao et al.
	Examiner JAMIE C NIESZ	Art Unit 2822

CPC - Searched*		
Symbol	Date	Examiner
H01L29/42316 or H01L21/283	July 24, 2018	JCN
H01L29/42316 or H01L21/283	01/15/2019	JCN

CPC Combination Sets - Searched*		
Symbol	Date	Examiner


US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Reviewed Search History for Parent Application 14/447,069	July 24, 2018	JCN
Text Search EAST (see search history)	July 24, 2018	JCN
Updated Text Search EAST (see search history)	01/15/2019	JCN

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	Interference Search EAST (see search history)	July 24, 2018	JCN
	Updated Interference Search EAST (see search history)	01/15/2019	JCN

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Issue Classification 	Application/Control No. 15/655,438	Applicant(s)/Patent Under Reexamination Cao et al.
	Examiner JAMIE C NIESZ	Art Unit 2822


CPC						
Symbol					Type	Version
H01L	/	29	/	42316	F	2013-01-01
H01L	/	21	/	283	I	2013-01-01
H01L	/	29	/	66462	I	2013-01-01
H01L	/	29	/	7786	I	2013-01-01
H01L	/	29	/	1066	I	2013-01-01
H01L	/	29	/	2003	I	2013-01-01
H01L	/	21	/	28587	I	2013-01-01
H01L	/	29	/	205	I	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/				

NONE (Assistant Examiner)		Total Claims Allowed: 7	
/JAMIE C NIESZ/ Primary Examiner, Art Unit 2822 (Primary Examiner)		15 January 2019 (Date)	O.G. Print Claim(s) 1
			O.G. Print Figure 5

U.S. Patent and Trademark Office

Part of Paper No.: 20190115a

Issue Classification 	Application/Control No. 15/655,438	Applicant(s)/Patent Under Reexamination Cao et al.
	Examiner JAMIE C NIESZ	Art Unit 2822

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L		29	423

NON-CLAIMED			


US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	7	
/JAMIE C NIESZ/ Primary Examiner, Art Unit 2822	15 January 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

U.S. Patent and Trademark Office

Part of Paper No.: 20190115a

Issue Classification 	Application/Control No. 15/655,438	Applicant(s)/Patent Under Reexamination Cao et al.
	Examiner JAMIE C NIESZ	Art Unit 2822

<input checked="" type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47
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CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	6	10												
	2	7	11												
	3														
	4														
2	5														
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4	7														
5	8														
	9														

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 7	
/JAMIE C NIESZ/ Primary Examiner, Art Unit 2822 (Primary Examiner) _____ (Date) 15 January 2019		O.G. Print Claim(s) 1	O.G. Print Figure 5

U.S. Patent and Trademark Office

Part of Paper No.: 20190115a

Bibliographic Data

Application No: 15/655,438

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/JAMIE C NIESZ/

Examiner's Signature

Initials

Title:

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT
MODE GaN TRANSISTORS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
07/20/2017	257	2822	
RULE			

APPLICANTS

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Alana Nakata Redondo Beach, CA, UNITED STATES

CONTINUING DATA

This application is a DIV of 14447069 07/30/2014 PAT 9748347

14447069 has PRO of 61860976 08/01/2013

14447069 is a CIP of 13838792 03/15/2013 PAT 8890168

13838792 is a DIV of 12756960 04/08/2010 PAT 8404508

12756960 has PRO of 61167777 04/08/2009

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

07/27/2017

** SMALL ENTITY **

STATE OR COUNTRY

UNITED STATES

ADDRESS

FILING FEE RECEIVED

\$730

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	"14447069"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/11 12:23
S2	5	("20090004872" "20100258843" "20130168743" "6730552" "7939880").PN.	US-PGPUB; USPAT	ADJ	ON	2015/12/11 12:35
S3	18	(GaN) and enhancement and (isotropically with gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:57
S4	264	(photoresist or resist) same (isotropically with gate with etch\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S5	111	(photoresist or resist) same (isotropically with gate with etch\$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S6	5935	(H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S7	3	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S9	4	"14447069"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:29
S10	4	"13838792"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:30
S11	111	(photoresist or resist) same (isotropically with gate with etch\$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:15
S12	1	tw "201314898"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:16
S13	2	(cao or lidow or nakata).in. and ((photoresist or resist) same (isotropically with gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:19
S14	4	"20130075788"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	ADJ	ON	2017/01/27 13:50

			DERWENT			
S15	3	"20060273347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 13:58
S16	162	20070254418 20060192218 6833161 6537838 6001716 20080116492 5474946 7470941	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:00
S17	43	(20070254418 20060192218 6833161 6537838 6001716 20080116492 5474946 7470941) and (sheppard or kyono or wang or stockman or liao or wu or ajit or micovic).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:01
S18	1096	(gate with ledge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:03
S19	54	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:03
S20	8	"6730552"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:18
S21	4	jp "2011142182"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:22
S22	11	cn "101022128"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:26
S23	26	"7576373"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:26
S24	6	jp "2008159681"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:28
S25	5	jp "2008091392"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:30
S26	8	"20080079023"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:33
S27	105	(gate with ledge) and barrier	US-PGPUB; USPAT; USOCR;	ADJ	ON	2017/01/27 16:01

			FPRS; EPO; JPO; DERWENT			
S28	181	(gate with ledge).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:15
S29	7	(gate with ledge).ab. and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:17
S30	3913	gate and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:19
S31	2637	barrier and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:19
S32	1068	barrier and 2DEG and (etch\$4 with gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:19
S33	1032	2DEG and (pattern\$4 with gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 11:40
S34	479	2DEG and (pattern\$4 with gate with (resist or mask or photoresist or photo-resist))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 11:40
S35	22	"11856687"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:05
S36	6	2DEG and (cap near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:06
S37	13	2DEG and (p-type gate material)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:09
S38	4	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:24
S39	888	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:24
S42	108	"5985687"	US-PGPUB; USPAT; USOCR;	ADJ	ON	2017/01/31: 09:10

			EPO; JPO; DERWENT			
S43	2	us-5985687-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:10
S44	2	us-20080006845-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:11
S45	2	us-20080296618-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:11
S46	2	us-20060273347-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:18
S47	2	us-6537838-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:18
S48	2	us-6235547-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:19
S49	2	us-4987462-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:19
S50	7	"12756960"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 09:16
S51	5	"14447069"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 09:29
S52	5	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:28
S53	55	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:33
S54	111	(photoresist or resist) same (isotropically with gate with etch\$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:38
S55	220	2DEG and (p-type near2 gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:38
S57	1	"15655438"	US-PGPUB; USPAT; USOCR; FPRS;	ADJ	ON	2018/07/23 11:06

			EPO; JPO; DERWENT; IBM TDB			
S58	9	("20040119110" "20060157735" "20060273347" "20090004872" "20090072272" "20100258843" "20130168743" "6730552" "7939880").PN.	US-PGPUB; USPAT	ADJ	ON	2018/07/23 11:07
S59	1018	((H01L29/42316 or H01L21/283).cpc.) and ((gate with (sidewall or side-wall)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2018/07/23 11:57
S60	121	HFET and ((side-wall or sidewall) with (slant\$4 or taper\$4 or slop\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2018/07/23 11:59
S61	60	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/07/24 12:47
S62	4	hfet and (cap near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/07/24 12:48
S63	210	hfet and (gate near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/07/24 12:48
S65	9	"9748347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/01/15 11:34
S66	822	(H01L29/42316 or H01L21/283).cpc. and ((photoresist or resist) same (gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2019/01/15 12:43
S67	4	hfet and (cap near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/01/15 12:50
S68	61	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2019/01/15 12:51

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	0	(GaN and gate metal and Photoresist and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2015/12/14 12:01
S40	11	(GaN and barrier and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2017/01/30 12:21
S41	3	(GaN and barrier and ledges and photoresist).clm.	US-PGPUB; USPAT	ADJ	ON	2017/01/30 12:23
S56	4	(GaN and barrier and ledges and photoresist).clm.	US-PGPUB; USPAT	ADJ	ON	2017/03/20 10:42
S64	14	(GaN and barrier and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2018/07/24 14:10
S69	14	(GaN and barrier and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2019/01/15 12:54

1/ 15/ 2019 12:54:25 PM

C:\Users\jniesz1\Documents\EAST\Workspaces\15655438.wsp

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 15/655,438		Filing Date 07/20/2017		<input type="checkbox"/> To be Mailed		
ENTITY: <input type="checkbox"/> LARGE <input checked="" type="checkbox"/> SMALL <input type="checkbox"/> MICRO										
APPLICATION AS FILED – PART I										
		(Column 1)		(Column 2)						
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)		
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A				
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A				
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =				
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL				
APPLICATION AS AMENDED – PART II										
		(Column 1)		(Column 2)		(Column 3)				
AMENDMENT	10/31/2018		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		* 7		Minus	** 20	= 0	X \$50 =	0	
	Independent (37 CFR 1.16(h))		* 2		Minus	***3	= 0	X \$230 =	0	
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))									
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
	TOTAL ADD'L FEE								0	
		(Column 1)		(Column 2)		(Column 3)				
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		*		Minus	**	=	X \$ =		
	Independent (37 CFR 1.16(h))		*		Minus	***	=	X \$ =		
	<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))									
	<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
	TOTAL ADD'L FEE									
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

LIE
ANGELA s. WHITE

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Docket No.: E0101.0053-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 15/655,438

Confirmation No.: 5778

Filed: July 20, 2017

Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR
ENHANCEMENT MODE GAN
TRANSISTORS

Examiner: J. C. Niesz

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated August 2, 2018, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Amendments to the Specification are set forth on page 4 of this paper.

Remarks/Arguments begin on page 5 of this paper.

200371.00125/110988761v.1

Electronic Acknowledgement Receipt	
EFS ID:	34170340
Application Number:	15655438
International Application Number:	
Confirmation Number:	5778
Title of Invention:	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl de Lopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032-A
Receipt Date:	31-OCT-2018
Filing Date:	20-JUL-2017
Time Stamp:	11:50:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		amendp053a.pdf	154743	yes	5
			8a1583b70fda8a1380071b523fb7e59509af6211		

Multipart Description/PDF files in .zip description			
Document Description		Start	End
Applicant Arguments/Remarks Made in an Amendment		5	5
Specification		4	4
Claims		2	3
Amendment/Req. Reconsideration-After Non-Final Reject		1	1

Warnings:

Information:

Total Files Size (in bytes):	154743
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Claims 1, 5-8 and 10-11 are pending in the present application.

The specification has been amended to correct errors in paragraphs [0027] and [0030].
No new matter has been added.

Claim 1, line 10, has been amended to correct “the pair of horizontal edges” to “the pair of horizontal **ledges**,” to address the objection raised by the Examiner.

Claim 1 has also been amended to incorporate the allowable subject matter of claim 4 (and intervening claims 2-3), and claim 8 has been amended to incorporate the allowable subject matter of claim 9. Claims 2-4 and 9 have been canceled. Accordingly, the rejection of claims 1-3, 5-8, 10 and 11 under 35 U.S.C. 102(a)(1) as being anticipated by Hikita et al. (US 2006/0273347) is rendered moot, and should be withdrawn.

A prompt passage to issuance is earnestly solicited.

Dated: October 31, 2018

Respectfully submitted,

By: 

Stephen A. Soffen

Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

AMENDMENTS TO THE SPECIFICATION

Please amend paragraphs [0027] and [0030] of the specification as follows:

[0027] Figs. 6A-6C illustrate a manufacturing process for fabricating a gate with self-aligned ledges in accordance with an exemplary embodiment of the present invention. As shown in Fig. 6A, the base structure of the device is first formed with a base layer 601 of gallium nitride (GaN), a barrier layer 602 of aluminum gallium nitride (AlGaN) formed on the GaN layer 601, and a layer of p-type gate material 603 formed on the barrier layer ~~[[502]]~~ 602, over which the gate metal 604 is deposited.

[0030] Figs. 7A-7B illustrate, respectively, a transmission electron microscopy (“TEM”) image of a cross-sectional view of a conventional transistor gate and ~~an x-ray~~ of a cross-sectional view of a gate with a self-aligned ledge according to the exemplary embodiment disclosed herein. Fig. 8 illustrates a graph comparing the gate leakage current of the present invention (shown in Fig. 7B) with the gate leakage current of a conventional transistor (shown in Fig. 7A). As can be clearly seen in Fig. 8, the gate with self-aligned ledges has significantly lower gate leakage current than conventional gates without ledges when the transistor device is in the ON state.

AMENDMENTS TO THE CLAIMS

1. (Currently amended) An enhancement-mode GaN transistor, comprising:
- a GaN layer;
 - a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
 - a source contact and a drain contact formed on the barrier layer;
 - a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
 - a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,
- wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

Claims 2-4. (Canceled)

5. (Original) The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.
6. (Original) The enhancement-mode GaN transistor according to claim 1, wherein the barrier layer comprises aluminum gallium nitride (AlGa_N).
7. (Original) The enhancement-mode GaN transistor according to claim 1, wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width.

8. (Currently amended) An enhancement-mode GaN transistor, comprising:
 - a GaN layer;
 - a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
 - a source contact and a drain contact disposed on the barrier layer;
 - a p-type gate material formed above the barrier layer and between the source and drain contacts;
 - and a gate metal disposed on the p-type gate material,
 - wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.
9. (Canceled)
10. (Original) The enhancement-mode GaN transistor according to claim 8, wherein the barrier layer comprises aluminum gallium nitride (AlGa_N).
11. (Original) The enhancement-mode GaN transistor according to claim 8, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/655,438	07/20/2017	Jianjun Cao	E0101.0032-A	5778
24998	7590	08/02/2018	EXAMINER	
Blank Rome LLP 1825 EYE STREET NW Washington, DC 20006-5403			NIESZ, JAMIE C	
			ART UNIT	PAPER NUMBER
			2822	
			NOTIFICATION DATE	DELIVERY MODE
			08/02/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WashingtonDocketing@blankrome.com

Office Action Summary	Application No. 15/655,438	Applicant(s) CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 July 2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-11 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-3,5-8,10 and 11 is/are rejected.
- 8) ☒ Claim(s) 4 and 9 is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 7/20/2017 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 3) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) | Paper No(s)/Mail Date. ____. |
| Paper No(s)/Mail Date ____. | 4) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

1. This office action is in response to the application filed July 20, 2017.
2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Objections

3. Claim 1 is objected to because of the following informalities:
4. Claim 1 recites "the pair of horizontal edges" in the tenth line of the claim. This limitation, however, lacks antecedent basis and will instead be interpreted as "the pair of horizontal **ledges**." Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

6. **Claims 1-3, 5-8, 10 and 11** are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Hikita et al. (US 2006/0273347).
7. Regarding claim 1, Hikita discloses an enhancement-mode GaN transistor (Fig. 1), comprising:

a GaN layer (103; ¶ [0033]);

a barrier layer (104) disposed on the GaN layer (103) with a 2DEG region formed at an interface between the GaN layer (103) and the barrier layer (104; ¶ [0038]);

a p-type gate material (105/106) formed above the barrier layer (104), the p-type gate material (105/106) having side surfaces (sidewalls) extending towards the barrier layer (104); and

a gate metal (111) disposed on the p-type gate material (105/106), the gate metal (111) having sidewalls extending towards the p-type gate material (105/106),

wherein the p-type gate material (105/106) comprises a pair of horizontal ledges (top corners) that extend past the respective sidewalls of the gate metal (111), the pair of horizontal ledges (top corners) having substantially equal widths from the sidewalls of the gate metal (111) to the side surfaces (sidewalls) of the p-type gate material (105/106), respectively.

8. Regarding claim 2, Hikita further discloses a source contact (109) and a drain contact (110) disposed on the barrier layer (104).

9. Regarding claim 3, Hikita discloses wherein the pair of horizontal ledges (top corners) of the p-type gate material (105/106) extend toward the source contact (109) and the drain contact (110), respectively.

10. Regarding claim 5, Hikita discloses wherein the pair of horizontal ledges (top corners) of the p-type gate material (105/106) are self-aligned (i.e., ledges are symmetrical).

11. Regarding claim 6, Hikita discloses wherein the barrier layer (104) comprises aluminum gallium nitride (AlGa_N) (¶ [0033]).

12. Regarding claim 7, Hikita discloses wherein the p-type gate material (105/106) has a first width between the side surfaces (sidewalls) of the p-type gate material (105/106) and the gate metal (111) has a second width between sidewalls of the gate metal (111), the second width being less than the first width (see Fig. 1).

13. Regarding claim 8, Hikita discloses an enhancement-mode GaN transistor (Fig. 1), comprising:

a GaN layer (103; ¶ [0033]);

a barrier layer (104) disposed on the GaN layer (103) with a 2DEG region formed at an interface between the GaN layer (103) and the barrier layer (104; ¶ [0038]);

a source contact (109) and a drain contact (110) disposed on the barrier layer (104);

a p-type gate material (105/106) formed above the barrier layer (104) and between the source and drain contacts (109 and 110);

and a gate metal (111) disposed on the p-type gate material (105/106),

wherein the p-type gate material (105/106) comprises a pair of self-aligned (i.e., symmetrical) horizontal ledges (top corners) that extend past sidewalls of the gate metal (111) toward the source contact (109) and the drain contact (110), respectively.

14. Regarding claim 10, Hikita discloses wherein the barrier layer (104) comprises aluminum gallium nitride (AlGaN) ($\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$).

15. Regarding claim 11, Hikita discloses wherein the pair of self-aligned ledges (top corners of 105/106) are symmetric with respect to the gate metal (111).

Allowable Subject Matter

16. **Claims 4 and 9** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. Claim 4 recites “wherein the side surfaces of the p-type gate material extend horizontally towards the source contact and the drain contact, respectively, and contact the barrier layer” and claim 9 recites “wherein the p-type gate material further comprises side surfaces extending horizontally towards the source contact and the drain contact, respectively, and contacting the barrier layer.” These limitations, in combination with the rest of the limitations in the parent claims, respectively, are neither anticipated nor made obvious by the prior art of record, in the Examiner’s opinion.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMIE C. NIESZ whose telephone number is (303)297-4333. The examiner can normally be reached on Monday through Friday 10-6 EST.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMIE C NIESZ/
Primary Examiner
Art Unit 2822

Notice of References Cited	Application/Control No. 15/655,438	Applicant(s)/Patent Under Reexamination CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2006/0273347 A1	12-2006	Hikita; Masahiro	H01L29/66462	257/192
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Bibliographic Data

Application No: 15/655,438

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/JAMIE C NIESZ/

Examiner's Signature

Initials

Title:

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT
MODE GaN TRANSISTORS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
07/20/2017	257	2822	E0101.0032-A
RULE			

APPLICANTS

Efficient Power Conversion Corporation, El Segundo, CA, UNITED STATES

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Alexander Lidow Santa Monica, CA, UNITED STATES

Alana Nakata Redondo Beach, CA, UNITED STATES

CONTINUING DATA

This application is a DIV of 14447069 07/30/2014 PAT 9748347

14447069 has PRO of 61860976 08/01/2013

14447069 is a CIP of 13838792 03/15/2013 PAT 8890168

13838792 is a DIV of 12756960 04/08/2010 PAT 8404508

12756960 has PRO of 61167777 04/08/2009

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

07/27/2017

** SMALL ENTITY **

STATE OR COUNTRY

UNITED STATES

ADDRESS

Blank Rome LLP


1825 EYE STREET NW

Washington, DC 20006-5403

UNITED STATES

FILING FEE RECEIVED

\$730

Search Notes 	Application/Control No. 15655438	Applicant(s)/Patent Under Reexamination CAO ET AL.
	Examiner JAMIE C NIESZ	Art Unit 2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/42316 or H01L21/283	July 24, 2018	JCN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner


US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed Search History for Parent Application 14/447,069	July 24, 2018	JCN
Text Search EAST (see search history)	July 24, 2018	JCN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Interference Search EAST (see search history)	July 24, 2018	JCN

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<p align="center"><i>Index of Claims</i></p> 	Application/Control No. 15655438	Applicant(s)/Patent Under Reexamination CAO ET AL.
	Examiner JAMIE C NIESZ	Art Unit 2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47										
CLAIM		DATE								
Final	Original	07/24/2018								
	1	✓								
	2	✓								
	3	✓								
	4	O								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	O								
	10	✓								
	11	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	"14447069"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/11 12:23
S2	5	("20090004872" "20100258843" "20130168743" "6730552" "7939880").PN.	US-PGPUB; USPAT	ADJ	ON	2015/12/11 12:35
S3	18	(GaN) and enhancement and (isotropically with gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:57
S4	264	(photoresist or resist) same (isotropically with gate with etch\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S5	111	(photoresist or resist) same (isotropically with gate with etch\$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S6	5935	(H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S7	3	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S9	4	"14447069"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:29
S10	4	"13838792"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:30
S11	111	(photoresist or resist) same (isotropically with gate with etch\$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:15
S12	1	tw "201314898"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:16
S13	2	(cao or lidow or nakata).in. and ((photoresist or resist) same (isotropically with gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:19
S14	4	"20130075788"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	ADJ	ON	2017/01/27 13:50

			DERWENT			
S15	3	"20060273347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 13:58
S16	162	20070254418 20060192218 6833161 6537838 6001716 20080116492 5474946 7470941	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:00
S17	43	(20070254418 20060192218 6833161 6537838 6001716 20080116492 5474946 7470941) and (sheppard or kyono or wang or stockman or liao or wu or ajit or micovic).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:01
S18	1096	(gate with ledge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:03
S19	54	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:03
S20	8	"6730552"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:18
S21	4	jp "2011142182"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:22
S22	11	cn "101022128"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:26
S23	26	"7576373"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:26
S24	6	jp "2008159681"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:28
S25	5	jp "2008091392"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:30
S26	8	"20080079023"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:33
S27	105	(gate with ledge) and barrier	US-PGPUB; USPAT; USOCR;	ADJ	ON	2017/01/27 16:01

			FPRS; EPO; JPO; DERWENT			
S28	181	(gate with ledge).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:15
S29	7	(gate with ledge).ab. and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:17
S30	3913	gate and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:19
S31	2637	barrier and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:19
S32	1068	barrier and 2DEG and (etch\$4 with gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 09:19
S33	1032	2DEG and (pattern\$4 with gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 11:40
S34	479	2DEG and (pattern\$4 with gate with (resist or mask or photoresist or photo-resist))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 11:40
S35	22	"11856687"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:05
S36	6	2DEG and (cap near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:06
S37	13	2DEG and (p-type gate material)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:09
S38	4	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:24
S39	888	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/30: 12:24
S42	108	"5985687"	US-PGPUB; USPAT; USOCR;	ADJ	ON	2017/01/31: 09:10

			EPO; JPO; DERWENT			
S43	2	us-5985687-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:10
S44	2	us-20080006845-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:11
S45	2	us-20080296618-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:11
S46	2	us-20060273347-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:18
S47	2	us-6537838-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:18
S48	2	us-6235547-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:19
S49	2	us-4987462-\$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:19
S50	7	"12756960"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 09:16
S51	5	"14447069"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 09:29
S52	5	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:28
S53	55	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:33
S54	111	(photoresist or resist) same (isotropically with gate with etch\$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:38
S55	220	2DEG and (p-type near2 gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:38
S57	1	"15655438"	US-PGPUB; USPAT; USOCR; FPRS;	ADJ	ON	2018/07/23 11:06

			EPO; JPO; DERWENT; IBM, TDB			
S58	9	("20040119110" "20060157735" "20060273347" "20090004872" "20090072272" "20100258843" "20130168743" "6730552" "7939880").PN.	US-PGPUB; USPAT	ADJ	ON	2018/07/23 11:07
S59	1018	((H01L29/42316 or H01L21/283).cpc.) and ((gate with (sidewall or side-wall)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2018/07/23 11:57
S60	121	HFET and ((side-wall or sidewall) with (slant\$4 or taper\$4 or slop\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2018/07/23 11:59
S61	60	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/07/24 12:47
S62	4	hfet and (cap near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/07/24 12:48
S63	210	hfet and (gate near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2018/07/24 12:48

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	0	(GaN and gate metal and Photoresist and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2015/12/14 12:01
S40	11	(GaN and barrier and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2017/01/30 12:21
S41	3	(GaN and barrier and ledges and photoresist).clm.	US-PGPUB; USPAT	ADJ	ON	2017/01/30 12:23
S56	4	(GaN and barrier and ledges and photoresist).clm.	US-PGPUB; USPAT	ADJ	ON	2017/03/20 10:42
S64	14	(GaN and barrier and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2018/07/24 14:10

7/24/2018 2:11:11 PM

C:\Users\jniesz1\Documents\EAST\Workspaces\15655738.wsp

Used in Lieu of PTO/SB/08A/B
(Based on PTO 10-07 version)

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Jianjun Cao
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	E0101.0032-A

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
**	AA	2010/0258843 A1	10-2010	Lidow et al.	
**	AB	6,730,552	05-2004	Abadeer et al.	
**	AC	20130168743	07-2013	Dove	
**	AD	7,939,880	05-2011	Kang et al.	
**	AE	2009/0004872 A1	01-2009	Okamoto	
**	AF	2006/0273347 A1	12-2006	Hikita	
**	AG	2006/0157735 A1	07-2006	Kanamura	
**	AH	2009/0072272 A1	03-2009	Suh	
**	AI	2010/0258843 A1	10-2010	Lidow	
**	AJ	2004/0119110 A1	06-2004	Park	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
**	BA	JP-2011-142182 A	07-2011			✓
**	BB	TW 201232779	08-2012			
**	BC	TW 201314898	04-2013			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. ** CITE NO.: Those document(s) which are marked with an double asterisk (**) next to the Cite No. are not supplied because they were previously cited by or submitted to the Office in a prior application relied upon in this application for an earlier filing date under 35 U.S.C. 120. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

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¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	/JAMIE C NIESZ/	Date Considered	07/24/2018
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200371.00053/105864833

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.C.N/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/655,438	07/20/2017	Jianjun Cao	E0101.0032-A

CONFIRMATION NO. 5778

24998
Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

PUBLICATION NOTICE



OC000000095207045

Title:GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

Publication No.US-2017-0317179-A1

Publication Date:11/02/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

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Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
15/655,438	07/20/2017	2811	730	E0101.0032-A	11	2

CONFIRMATION NO. 5778

FILING RECEIPT



000000093072822

24998
Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

Date Mailed: 07/28/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jianjun Cao, Torrance, CA;
Alexander Lidow, Santa Monica, CA;
Alana Nakata, Redondo Beach, CA;

Applicant(s)

Efficient Power Conversion Corporation, El Segundo, CA;

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Priority data as claimed by applicant

This application is a DIV of 14/447,069 07/30/2014
which is a CIP of 13/838,792 03/15/2013 PAT 8890168
which is a DIV of 12/756,960 04/08/2010 PAT 8404508
which claims benefit of 61/167,777 04/08/2009
and said 14/447,069 07/30/2014
claims benefit of 61/860,976 08/01/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 07/27/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/655,438**

Projected Publication Date: 11/02/2017

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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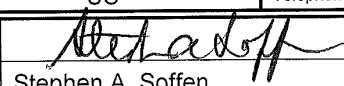
PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 15/655,438	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(j))	11	minus 20 = *	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
				TOTAL		TOTAL	
* If the difference in column 1 is less than zero, enter "0" in column 2.				730			
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		OTHER THAN SMALL ENTITY
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	RATE(\$)
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	ADDITIONAL FEE(\$)
	Application Size Fee (37 CFR 1.16(s))					OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR	
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		OTHER THAN SMALL ENTITY
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	RATE(\$)
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	ADDITIONAL FEE(\$)
	Application Size Fee (37 CFR 1.16(s))					OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR	
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							

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UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>		Attorney Docket No. E0101.0032-A	
		First Named Inventor Jianjun Cao	
		Title GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS	
		Express Mail Label No. _____	

APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
1. <input type="checkbox"/> Fee Transmittal Form <small>(PTO/SB/17 or equivalent)</small> 2. <input checked="" type="checkbox"/> Applicant asserts small entity status. <small>See 37 CFR 1.27</small> 3. <input type="checkbox"/> Applicant certifies micro entity status. See 37 CFR 1.29. <small>Applicant must attach form PTO/SB/15A or B or equivalent.</small> 4. <input checked="" type="checkbox"/> Specification [Total Pages <u>13</u>] <small>Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement)</small> 5. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets <u>6</u>] 6. <input checked="" type="checkbox"/> Inventor's Oath or Declaration [Total Pages <u>3</u>] <small>(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))</small> a. <input type="checkbox"/> Newly executed (original or copy) b. <input checked="" type="checkbox"/> A copy from a prior application (37 CFR 1.63(d)) 7. <input checked="" type="checkbox"/> Application Data Sheet * See note below. <small>See 37 CFR 1.76 (PTO/AIA/14 or equivalent)</small> 8. CD-ROM or CD-R <small>in duplicate, large table, or Computer Program (Appendix)</small> <input type="checkbox"/> Landscape Table on CD 9. Nucleotide and/or Amino Acid Sequence Submission <small>(if applicable, items a. - c. are required)</small> a. <input type="checkbox"/> Computer Readable Form (CRF) b. <input type="checkbox"/> Specification Sequence Listing on: i. <input type="checkbox"/> CD-ROM or CD-R (2 copies); or ii. <input type="checkbox"/> Paper c. <input type="checkbox"/> Statements verifying identity of above copies	ACCOMPANYING APPLICATION PAPERS 10. <input type="checkbox"/> Assignment Papers <small>(cover sheet & document(s))</small> <div style="border: 1px solid black; padding: 5px; margin-top: 5px;"> Name of Assignee </div> 11. <input type="checkbox"/> 37 CFR 3.73(c) Statement <small>(when there is an assignee)</small> <input checked="" type="checkbox"/> Power of Attorney 12. <input type="checkbox"/> English Translation Document (if applicable) 13. <input checked="" type="checkbox"/> Information Disclosure Statement <small>(PTO/SB/08 or PTO-1449)</small> <input type="checkbox"/> Copies of citations attached 14. <input type="checkbox"/> Preliminary Amendment 15. <input type="checkbox"/> Return Receipt Postcard <small>(MPEP § 503) (Should be specifically itemized)</small> 16. <input type="checkbox"/> Certified Copy of Priority Document(s) <small>(if foreign priority is claimed)</small> 17. <input type="checkbox"/> Nonpublication Request <small>Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.</small> 18. <input type="checkbox"/> Other: <div style="border: 1px solid black; height: 40px; width: 100%; margin-top: 5px;"></div>

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
 (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS					
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200371.00053/105864733

Application Data Sheet

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Application Information

Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R?::	None
Sequence submission?::	None
Computer Readable Form (CRF)?::	No

Title:: GATE WITH SELF-ALIGNED LEDGE
FOR ENHANCEMENT MODE GaN
TRANSISTORS

Attorney Docket Number:: E0101.0032-A

Request for Early Publication?: No

Request for Non-Publication?: No

Total Drawing Sheets:: 6

Small Entity?: Yes

Petition included?: No

Portions or all of the application associated with this No

Application Data Sheet may fall under a Secrecy

Order pursuant to 37 CFR 5.2::

Representative Information

Representative Customer Number:: 24998

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application	Divisional of	14/447,069	07/30/14
14/447,069	Continuation-in-part of	13/838,792 (now U.S. Patent No. 8,890,168)	03/15/2013
13/838,792	Division of	12/756,960 (now U.S. Patent No. 8,404,508)	04/08/2010
12/756,960	An application claiming the benefit under 35 USC 119(e)	61/167,777	04/08/2009
14/447,069	An application claiming the benefit under 35 USC 119(e)	61/860,976	08/01/2013

Applicant Information

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Applicant Type:: Assignee

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State or Province of mailing address:: CA

Country of mailing address:: US

Postal or Zip Code of mailing address:: 90245

Authorization or Opt-Out of Authorization to Permit Access

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

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The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

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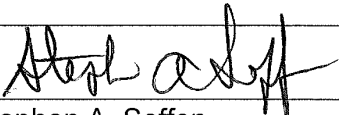
NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, all joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of all joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature		Date (YYYY-MM-DD)	2017-07-20
Name	Stephen A. Soffen	Registration Number	31,063

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
NON-PROVISIONAL APPLICATION FOR U.S. LETTERS PATENT

**GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN
TRANSISTORS**

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200371.00053/105864542

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. Patent Application No. 14/447,069, filed July 30, 2014, which is a continuation-in-part of U.S. Patent Application No. 13/838,792, filed March 15, 2013, now U.S. Patent No. 8,890,168, which is a divisional of U.S. Patent Application No. 12/756,960, filed April 8, 2010, now U.S. Patent No. 8,404,508, which claims the benefit of U.S. Provisional Application No. 61/167,777, filed April 8, 2009. Application No. 14/447,069 also claims the benefit of U.S. Provisional Application No. 61/860,976, filed on August 1, 2013. The entire disclosures are hereby incorporated by reference in their entireties.

BACKGROUND OF THE INVENTION

1. Field of the Invention:

[0002] The present invention relates generally to transistors and, more particularly, to an enhancement mode GaN transistor with reduced gate leakage current between the gate and the 2DEG region.

2. Description of the Related Art:

[0003] GaN semiconductor devices are increasingly desirable because of their ability to switch at high frequency, to carry large current, and to support high voltages. Development of these devices

has generally been aimed at high power/high frequency applications. Devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFET), high electron mobility transistors (HEMT), or modulation doped field effect transistors (MODFET). These types of devices can typically withstand high voltages, e.g., 30V-to-2000 Volts, while operating at high frequencies, e.g., 100 kHz-100 GHz.

[0004] A GaN HEMT device includes a nitride semiconductor with at least two nitride layers. Different materials formed on the semiconductor or on a buffer layer cause the layers to have different band gaps. The different material in the adjacent nitride layers also causes polarization, which contributes to a conductive two dimensional electron gas (2DEG) region near the junction of the two layers, specifically in the layer with the narrower band gap.

[0005] The nitride layers that cause polarization typically include a barrier layer of AlGaN adjacent to a layer of GaN to include the 2DEG, which allows charge to flow through the device. This barrier layer may be doped or undoped. Because the 2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices. If the 2DEG region is depleted (*i.e.*, removed) below the gate at zero applied gate bias, the device can be an enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide and because they are easier to control with simple, low cost drive circuits. An enhancement mode device requires a positive bias applied at the gate in order to conduct current.

[0006] Fig. 1 illustrates a conventional schematic enhancement-mode GaN transistor. As shown, a p-type material 101 is used as the gate 103. At 0V bias, the p-type material 101 depletes the 2DEG 102 under the gate 103, and the device is in an OFF state. The transistor is turned ON by applying a positive voltage to the gate 103. Fig. 2 illustrates a schematic diagram of two gate leakage current paths 201, 202 of a conventional enhancement-mode GaN transistor. The first gate leakage current path 201 flows along the sidewall of the p-type gate material 101 and the second gate leakage current path 202 flows through the bulk of the p-type gate material 101.

[0007] Figs. 3A and 3B illustrate schematic diagrams of two test structures 300A, 300B designed to determine the types of structures for an enhancement-mode GaN transistor that may result in lower gate leakage current. In particular, the transistor structure 300A illustrated in Fig. 3A is designed with a larger gate surface area and fewer gate edges when compared to the transistor structure 300B illustrated in Fig. 3B. In this example, the transistor structure 300A has a gate surface area of $140,000 \mu\text{m}^2$ and $2,500 \mu\text{m}$ edges, while the transistor structure 300B has a gate surface area of $84,000 \mu\text{m}^2$ and $247,000 \mu\text{m}$ edges.

[0008] Fig. 4 illustrates a graphical comparison of the gate leakage currents of the transistor structures 300A and 300B illustrated in Fig. 3A and 3B, respectively. As shown, structure 300B has a higher gate leakage current than structure 300A, suggesting that the gate leakage current is predominately along the gate edge, *i.e.*, path 201 illustrated in Fig. 2.

[0009] Accordingly, it is an object of the present invention is to provide an enhancement-mode GaN transistor with reduced gate leakage current between the gate 103 and the 2DEG 102.

SUMMARY OF THE INVENTION

[0010] An enhancement-mode GaN transistor and method for manufacturing the same is disclosed herein with the enhancement-mode GaN transistor having reduced gate leakage current between a gate contact and a 2DEG region and a method for manufacturing the same. The enhancement-mode GaN transistor including a GaN layer, a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer, and source contact and drain contacts disposed on the barrier layer. The GaN transistor further includes a p-type gate material formed above the barrier layer and between the source and drain contacts and a gate metal disposed on the p-type gate material, with wherein the p-type gate material including comprises a pair of self-aligned ledges that extend toward the source contact and drain contact, respectively.

[0011] A method for manufacturing the enhancement-mode GaN transistor disclosed herein includes the steps of forming a GaN layer; forming a barrier layer on the GaN layer; depositing a p-type gate material on the barrier layer; depositing a gate metal on the p-type gate material; forming a photoresist over the gate metal; etching the gate metal and the p-type gate material; and isotropically etching the gate metal to form pair of ledges on the p-type gate material below the gate metal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The features, objects, and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

[0013] Fig. 1 illustrates a schematic of a conventional enhancement-mode GaN transistor.

[0014] Fig. 2 illustrates a schematic diagram of two gate leakage current paths of a conventional enhancement-mode GaN transistor.

[0015] Fig. 3A illustrates a schematic diagram of test structure of an enhancement-mode GaN transistor.

[0016] Fig. 3B illustrates a schematic diagram of test structure of another enhancement-mode GaN transistor.

[0017] Fig. 4 illustrate a graphical comparison of the gate leakage currents of structures shown in Figs. 3A and 3B.

[0018] Fig. 5 illustrates a schematic diagram of a transistor device according to an exemplary embodiment of the present invention.

[0019] Figs. 6A-6C illustrates a fabrication process to manufacture a gate of a transistor device with self-aligned ledges according to an exemplary embodiment.

[0020] Fig. 7A illustrates a cross-sectional image of a conventional gate structure without a ledge.

[0021] Fig. 7B illustrates a cross-sectional image of a gate structure with a self-aligned ledge according to an exemplary embodiment.

[0022] Fig. 8 illustrates a graphical comparison of gate leakage current of the gate structures illustrated in Figs. 7A and 7B.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0023] In the following detailed description, reference is made to certain embodiments. These embodiments are described with sufficient detail to enable those skilled in the art to practice them. It is to be understood that other embodiments may be employed and that various structural, logical, and electrical changes may be made. The combinations of features disclosed in the following detailed description may not be necessary to practice the teachings in the broadest sense, and are instead taught merely to describe particularly representative examples of the present teachings.

[0024] Fig. 5 illustrates a schematic diagram of a transistor device according to an exemplary embodiment of the present invention. As shown, the transistor includes a source metal 510 (i.e., source contact) and a drain metal 512 (i.e., drain contact) with a gate contact disposed between the source and drain metals. In particular, a GaN base layer 501 is provided with a barrier layer 502 formed over the GaN base layer 501 and a two dimensional electron gas (2DEG) region formed at the interface between the GaN base layer and the barrier layer 502. In the exemplary embodiment, the barrier layer 502 is formed from aluminum gallium nitride (AlGaIn).

[0025] As further shown, the gate contact includes a p-type gate material 503 formed on the barrier layer 502 and includes ledges 506 that are created by a self-aligned process at the top corners of the p-type gate material 503 as will be discussed in detail below. A gate metal 504 is disposed over the p-type gate material 503. As shown, the gate metal 504 has a smaller width (i.e., the width

between sidewalls of the gate metal 504) than the width of the p-type gate material 503 (i.e., the width between side surfaces of the p-type gate material 503), effectively forming the pair of horizontal ledges 506 on each side of the gate metal 504. The pair of ledges 506 that extend past sidewalls of the gate metal 504 have equal or substantially equal widths, *i.e.*, the respective ledges are symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material, which is due to the self-aligned manufacturing process.

[0026] The primary benefits of using a self-aligned manufacturing process is to: (1) enable the creation of a p-type gate with a minimum critical dimension (“CD”), (2) lower processing cost because a second mask is not required, and (3) create ledges 506 that are symmetric to the gate metal 504 disposed on the p-type gate material. As indicated by the arrows (denoted by reference numbers 505) shown on ledges 506 and the side surfaces of the p-type gate material 503, when a positive voltage V_g is applied to the gate metal 504, the gate current path 505 first travels horizontally along the upper edge of the p-type gate material 503 and, once it reaches the ledges 506, the current path 505 follows the diagonal path along the edge of the p-type gate material 503. This structure results in reduced gate leakage current as discussed below with respect to Fig. 8.

[0027] Figs. 6A-6C illustrate a manufacturing process for fabricating a gate with self-aligned ledges in accordance with an exemplary embodiment of the present invention. As shown in Fig. 6A, the base structure of the device is first formed with a base layer 601 of gallium nitride (GaN), a barrier layer 602 of aluminum gallium nitride (AlGaN) formed on the GaN layer 601, and a layer of

p-type gate material 603 formed on the barrier layer 502, over which the gate metal 604 is deposited.

[0028] Next, as shown in Fig. 6B, a photoresist 605 is deposited and the gate metal 604 is then etched. The p-type gate material 603 is also etched in a manner that results in the gate structure depicted in Fig. 6B. As shown in Fig. 6C, the gate metal 604 is then etched isotropically, which results in the gate metal have a width less than the planar upper surface of the p-type gate material 603. This second etching step results in the formation of the ledges 506 of the p-type gate material 603.

[0029] Finally, the manufacturing process includes a step of removing the photoresist 605, which is not shown, and results in the gate with self-aligned ledge shown in Fig. 5. It should also be appreciated that contact metals for the drain and source contacts can be separately deposited using conventional fabrication techniques, but their formation will not be described herein so as to not unnecessarily obscure the aspects of the invention.

[0030] Figs. 7A-7B illustrate a transmission electron microscopy ("TEM") image of a cross-sectional view of a conventional transistor gate and an x-ray of a cross-sectional view of a gate with a self-aligned ledge according to the exemplary embodiment disclosed herein. Fig. 8 illustrates a graph comparing the gate leakage current of the present invention (shown in Fig. 7B) with the gate leakage current of a conventional transistor (shown in Fig. 7A). As can be clearly seen in Fig. 8, the gate with self-aligned ledges has significantly lower gate leakage current than conventional gates without ledges when the transistor device is in the ON state.

[0031] Finally, it is noted that the self-aligned process illustrated in Figs. 6A-6C is vastly superior to forming gate ledges using separate masks. In the process of using separate masks, a photoresist mask is applied to the unetched structure after the p-type gate material is deposited on the barrier layer of the device. In this instance, the first mask is used to pattern and etch the gate metal to a minimum CD. A second mask is then used to pattern and etch the p-type material with a wider CD than the gate metal. One significant disadvantage of this two mask process is the possibility of misalignment between the gate metal and the p-type gate material.

[0032] The above description and drawings are only to be considered illustrative of specific embodiments, which achieve the features and advantages described herein. Modifications and substitutions to specific process conditions can be made. Accordingly, the embodiments of the invention are not considered as being limited by the foregoing description and drawings.

CLAIMS

What is claimed:

1. An enhancement-mode GaN transistor, comprising:
 - a GaN layer;
 - a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
 - a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending towards the barrier layer; and
 - a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal, the pair of horizontal edges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.
2. The enhancement-mode GaN transistor according to claim 1, further comprising a source contact and a drain contact disposed on the barrier layer.
3. The enhancement-mode GaN transistor according to claim 2, wherein the pair of horizontal ledges of the p-type gate material extend toward the source contact and drain contact, respectively.

4. The enhancement-mode GaN transistor according to claim 3, wherein the side surfaces of the p-type gate material extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.
5. The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.
6. The enhancement-mode GaN transistor according to claim 1, wherein the barrier layer comprises aluminum gallium nitride (AlGa_N).
7. The enhancement-mode GaN transistor according to claim 1, wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width.
8. An enhancement-mode GaN transistor, comprising:
 - a GaN layer;
 - a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
 - a source contact and a drain contact disposed on the barrier layer;
 - a p-type gate material formed above the barrier layer and between the source and drain contacts;
 - and a gate metal disposed on the p-type gate material,

wherein the p-type gate material comprises a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively.

9. The enhancement-mode GaN transistor according to claim 8, wherein the p-type gate material further comprises side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer.

10. The enhancement-mode GaN transistor according to claim 8, wherein the barrier layer comprises aluminum gallium nitride (AlGaIn).

11. The enhancement-mode GaN transistor according to claim 8, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

ABSTRACT

An enhancement-mode GaN transistor with reduced gate leakage current between a gate contact and a 2DEG region and a method for manufacturing the same. The enhancement-mode GaN transistor including a GaN layer, a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer, and source contact and drain contacts disposed on the barrier layer. The GaN transistor further includes a p-type gate material formed above the barrier layer and between the source and drain contacts and a gate metal disposed on the p-type gate material, with wherein the p-type gate material including comprises a pair of self-aligned ledges that extend toward the source contact and drain contact, respectively.

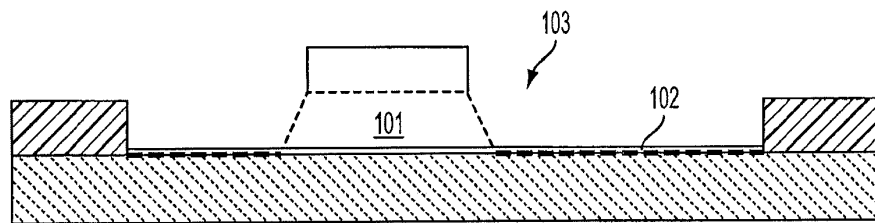


FIG. 1
PRIOR ART

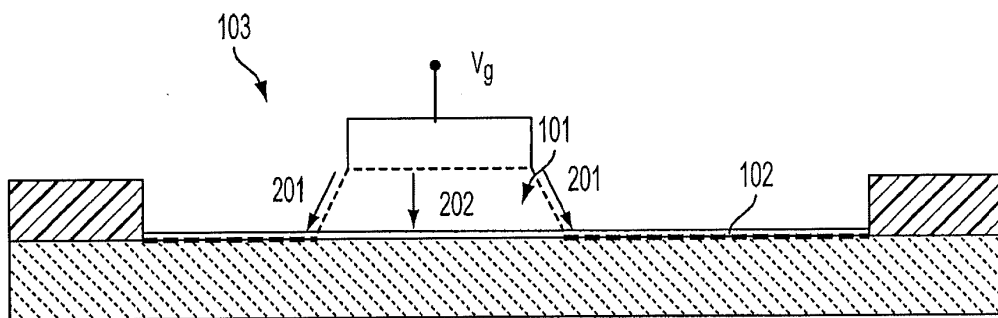


FIG. 2
PRIOR ART

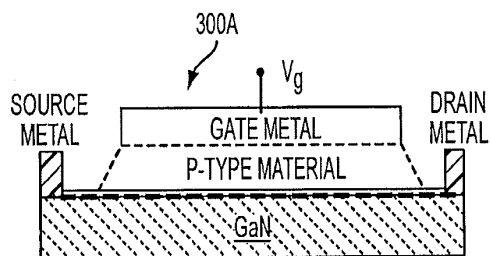


FIG. 3A
PRIOR ART

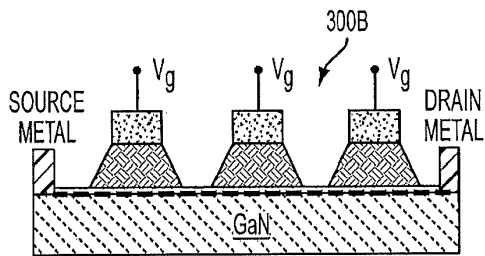


FIG. 3B
PRIOR ART

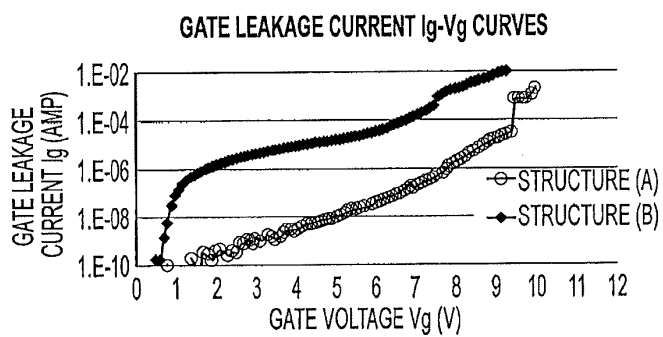


FIG. 4
PRIOR ART

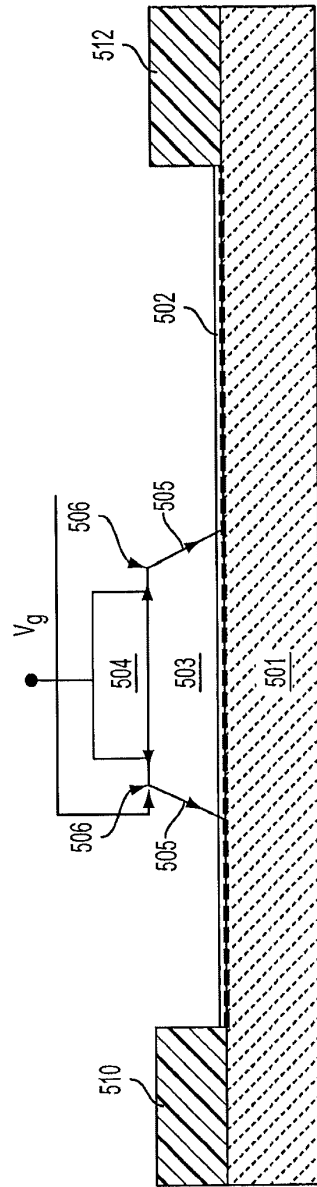


FIG. 5

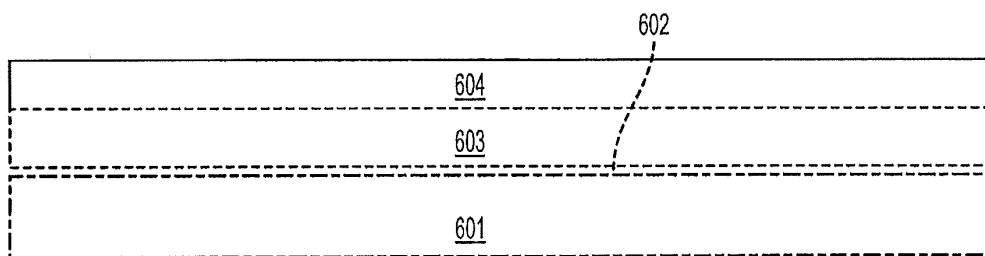


FIG. 6A

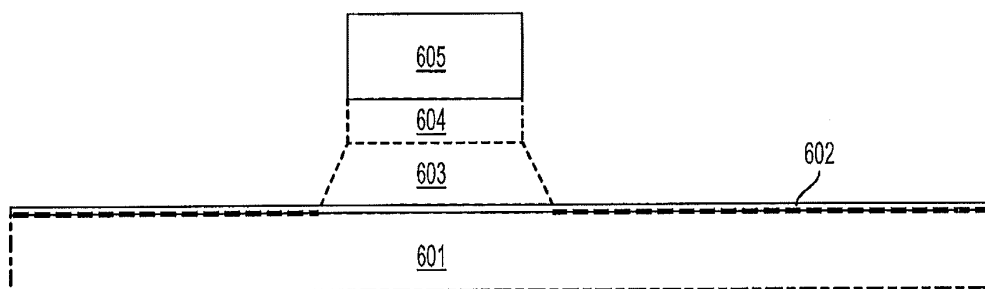


FIG. 6B

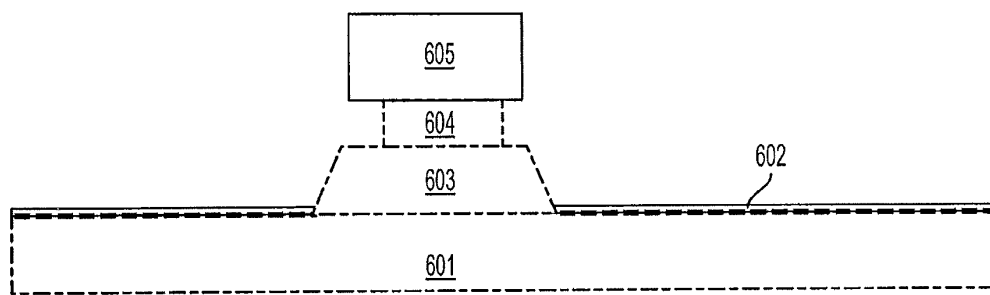


FIG. 6C

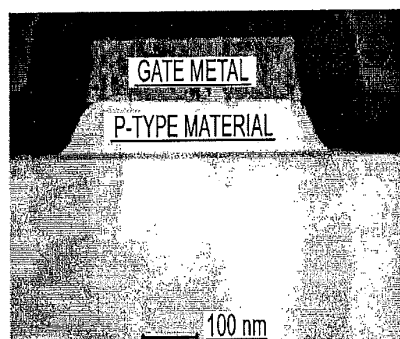


FIG. 7A
PRIOR ART

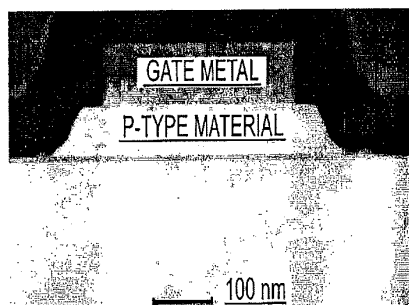


FIG. 7B

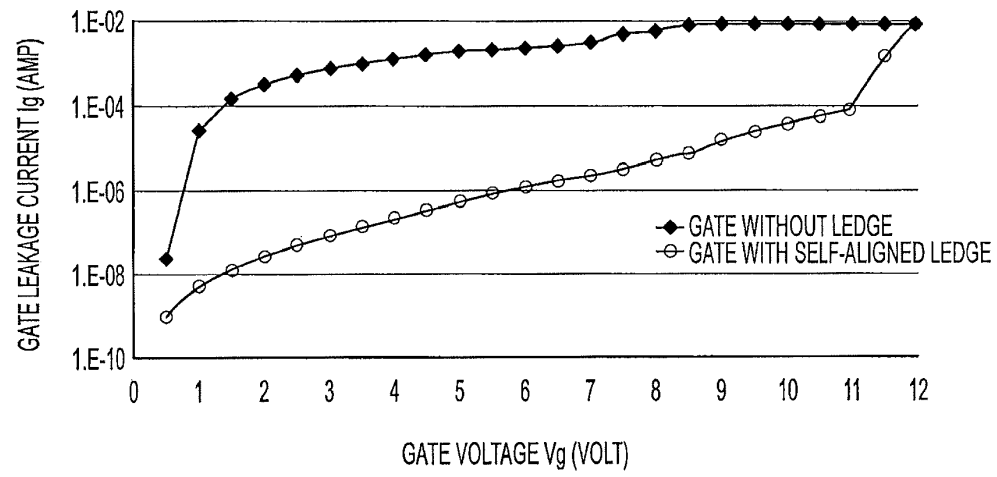


FIG. 8

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)**Title of
Invention**

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

As the below named inventor, I hereby declare that:

This declaration ☒ The attached application, or
is directed to:☐ United States application or PCT international application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: _____ Jianjun Cao _____

Date (Optional): _____

Signature:  _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of
Invention

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

As the below named inventor, I hereby declare that:

This declaration ☒ The attached application, or
is directed to:

☐ United States application or PCT International application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

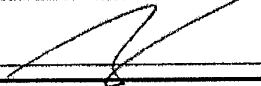
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LEGAL NAME OF INVENTOR

Inventor: Alexander Lidow

Date (Optional): _____

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

**Title of
Invention**

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

As the below named inventor, I hereby declare that:

This declaration ☒ The attached application, or
is directed to:

☐ United States application or PCT international application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Alana Nakata

Date (Optional): July 25, 2014

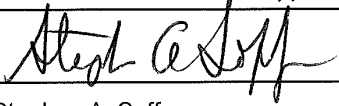
Signature: Alana Nakata

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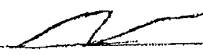
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NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	Not Yet Assigned		
Filing Date	Concurrently Herewith		
First Named Inventor	Jianjun Cao		
Title	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS		
Art Unit	N/A		
Examiner Name	Not Yet Assigned		
Attorney Docket Number	E0101.0032-A		
SIGNATURE of Applicant or Patent Practitioner			
Signature		Date	July 20, 2017
Name	Stephen A. Soffen	Telephone	(202) 420-4879
Registration Number	31,063		
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.			
<input type="checkbox"/> *Total of <u>1</u> forms are submitted.			

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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<input type="checkbox"/>	Practitioner(s) named below (If more than ten patent practitioners are to be named, then a customer number must be used):		
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The practitioners appointed in this form are authorized to act on behalf of the assignee and/or applicant to transact all business in the United States Patent and Trademark Office.			
SIGNATURE of Assignee and/or Applicant			
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee and/or applicant			
Signature			Date October 5, 2015
Name	Alexander Lidow		Telephone
Title and Company	President/CEO		

DSMDB-3268583 v1

Docket No.: E0101.0032-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: Not Yet Assigned

Confirmation No.: N/A

Filed: Concurrently Herewith

Art Unit: N/A

For: GATE WITH SELF-ALIGNED LEDGE FOR
ENHANCEMENT MODE GAN
TRANSISTORS

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, the attention of the United States Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of the above-identified application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

Copies of the references on the PTO/SB/08 are not provided.

In accordance with 37 C.F.R. § 1.98(d)(1) and as noted by a double-asterisk next to the Cite No. on the attached PTO/SB/08, the following references are not supplied because they were previously cited by or submitted to the Office in prior application number 14/447,069 filed

200371.00053/105864821

Application No.: Not Yet Assigned

Docket No.: E0101.0032-A


July 30, 2014 and relied on in the above-identified application for an earlier effective filing date under 35 U.S.C. § 120.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made. In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in this Information Disclosure Statement is, or is considered to be, material to the patentability as defined in 37 C.F.R. § 1.56(b).

It is submitted that the Information Disclosure Statement is in compliance with 37 C.F.R. § 1.98, and the Examiner is respectfully requested to consider the listed references.

Dated: July 20, 2017

Respectfully submitted,

By 
Stephen A. Soffen

Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Jianjun Cao
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	E0101.0032-A

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
**	AA	2010/0258843 A1	10-2010	Lidow et al.	
**	AB	6,730,552	05-2004	Abadeer et al.	
**	AC	20130168743	07-2013	Dove	
**	AD	7,939,880	05-2011	Kang et al.	
**	AE	2009/0004872 A1	01-2009	Okamoto	
**	AF	2006/0273347 A1	12-2006	Hikita	
**	AG	2006/0157735 A1	07-2006	Kanamura	
**	AH	2009/0072272 A1	03-2009	Suh	
**	AI	2010/0258843 A1	10-2010	Lidow	
**	AJ	2004/0119110 A1	06-2004	Park	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
**	BA	JP-2011-142182 A	07-2011			✓
**	BB	TW 201232779	08-2012			
**	BC	TW 201314898	04-2013			

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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

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¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	Date Considered
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200371.00053/105864833

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS		
First Named Inventor/Applicant Name:		Jianjun Cao		
Filer:		Stephen A. Soffen/Cheryl de Lopez		
Attorney Docket Number:		E0101.0032-A		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	70	70
UTILITY SEARCH FEE	2111	1	300	300
UTILITY EXAMINATION FEE	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				730

Electronic Acknowledgement Receipt	
EFS ID:	29846259
Application Number:	15655438
International Application Number:	
Confirmation Number:	5778
Title of Invention:	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl de Lopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032-A
Receipt Date:	20-JUL-2017
Filing Date:	
Time Stamp:	16:43:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$730
RAM confirmation Number	072117INTEFSW16434600
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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		applicationp032a.pdf	2567877	yes	35
			9621173886df51814d037049169400566679556		
	Multipart Description/PDF files in .zip description				
	Document Description		Start		End
	Transmittal of New Application		1		1
	Application Data Sheet		2		7
	Specification		8		17
	Claims		18		20
	Abstract		21		21
	Drawings-only black and white line drawings		22		27
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	Transmittal Letter		33		34
	Information Disclosure Statement (IDS) Form (SB08)		35		35
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	34912	no	2
			2174b49c618c729b9147a29bc6fd1fadbb669b25		
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.