

Enhancement mode AlGaIn/GaN HFET with selectively grown *pn* junction gate

X. Hu, G. Simin, J. Yang, M. Asif Khan, R. Gaska and M.S. Shur

A report is presented into the fabrication and characterisation of an enhancement mode AlGaIn/GaN heterojunction field-effect transistor (HFET) with selectively grown *pn* junction gate. At zero gate bias the device channel is depleted due to the high built-in potential of the gate-channel junction. The selective area growth approach enables both depletion and enhancement mode HFETs to be fabricated on the same wafer thus opening up the possibility of designing high speed, low consumption GaN-based logic integrated circuits.

Since the first demonstration of a depletion mode AlGaIn/GaN high electron mobility transistor (HEMT) [1], there has been rapid progress towards the realisation of high power microwave devices [2, 3]. However to date few reports have been made of AlGaIn/GaN based enhancement mode transistors. Khan *et al.* reported such a device using AlGaIn/GaN heterojunctions where a Schottky barrier gate was used [4]. For high temperature digital IC applications it is ideal to fabricate both enhancement and depletion mode (AlGaIn/GaN) devices in selective areas on the same wafer. In this Letter we describe a novel approach to realising an enhancement mode AlGaIn/GaN heterostructure field effect transistor (HFET) with a selective area grown *pn* junction gate. The *p*-GaN layers for the gate were grown in selective areas defined by openings in an SiO₂ mask. Our novel approach therefore opens up the possibility of monolithically integrating AlGaIn/GaN based normally-on and normally-off logic devices on a single wafer.

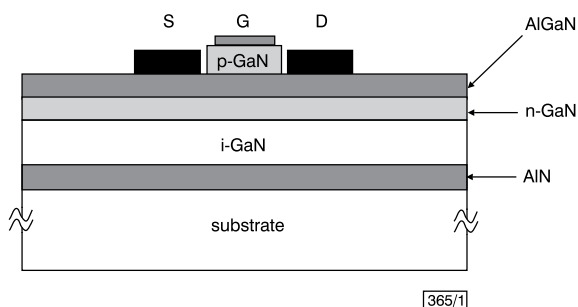


Fig. 1 Schematic diagram of structure of *pn* junction regrown gate HFET

The epilayer structure for our devices is schematically shown in Fig. 1. It was deposited over a basal plane sapphire substrate using low pressure metal organic chemical vapour deposition (MOCVD) epitaxy. The 300 Å AlN buffer layer of our structure was deposited at 400°C and 76 torr. All the other layers were deposited at 1000°C and 76 torr. The Al_{0.2}Ga_{0.8}N barrier layer was 300 Å thick and was silicon-doped to N barrier layer was 300 Å thick and was silicon-doped to $n = 3 \times 10^{18} \text{ cm}^{-3}$. All layers of the structure were grown with a low-level flux of trimethyl-indium (TMI). This incorporates trace amount of In in all the layers and helps with the layer and interface smoothness. For the structure, the room temperature sheet carrier density and mobility were measured to be $n_s = 8 \times 10^{12} \text{ cm}^{-2}$ and $\mu = 1000 \text{ cm}^2/\text{V.s}$.

Mg-doped 1000 Å thick *p*-GaN ($p = 10^{17} \text{ cm}^{-3}$) was then selectively grown using $10 \mu\text{m} \times 150 \mu\text{m}$ openings in a 1000 Å thick SiO₂ masking layer. The SiO₂ mask layer was deposited using a plasma enhanced chemical vapour deposition (PECVD) system. Transistors were then fabricated with Ti/Al/Ti/Au (100 Å/200 Å/100 Å/500 Å) source-drain contacts. The contacts were then RTA annealed at 850°C for 1 min in a nitrogen ambient. Ni/Au contacts were then deposited over the selective area grown *p*-GaN regions. These were annealed at 450°C in oxygen ambient. Our transistor structure thus had a gate length of 10 μm and a gate width of 150 μm. The source drain opening was 10 μm. Note that this geometry was selected only for a proof of principle. For higher performance devices much shorter gate lengths and source drain distances will be required.

In Fig. 2a we include the source drain current-voltage characteristics. As seen at zero gate bias the device does not conduct because the channel is depleted due to the high built-in voltage of the *pn* junction gate. With positive gate voltage the device reaches a saturation current of

40 mA/mm at +4 V gate bias. Fig. 2b shows the external transconductance g_m as a function of gate bias measured at 25 V drain to source voltage. The peak g_m value of 10 mS/mm is reached at +3 V gate bias. These I_{ds} and g_m values are limited by the low channel conductance from the very large gate and channel length (10 μm). Assuming an inverse linear dependence of both saturation current and transconductance on the gate length, we estimate these values to be 400 mA/mm and 150 mS/mm, respectively, for a 1 μm-gate device. These estimated values of I_{ds} and g_m are quite close to those typically reported for depletion mode devices.

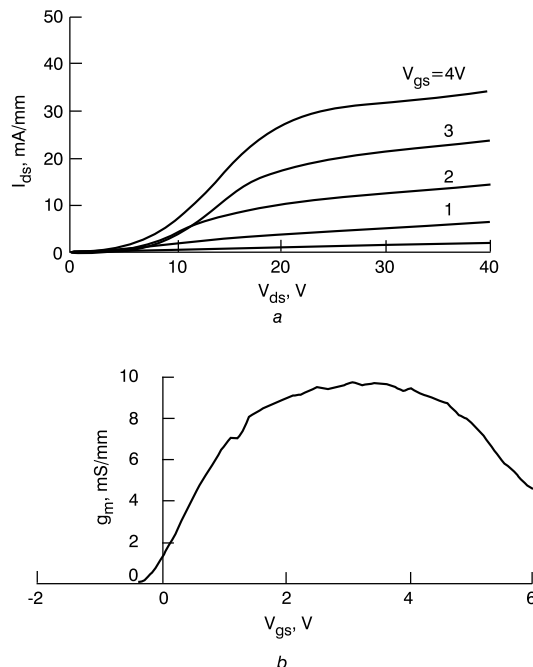


Fig. 2 Current-voltage characteristics of enhancement mode *pn* junction gate HFET

a Channel current dependence on drain to source voltage
b Transconductance dependence on gate bias

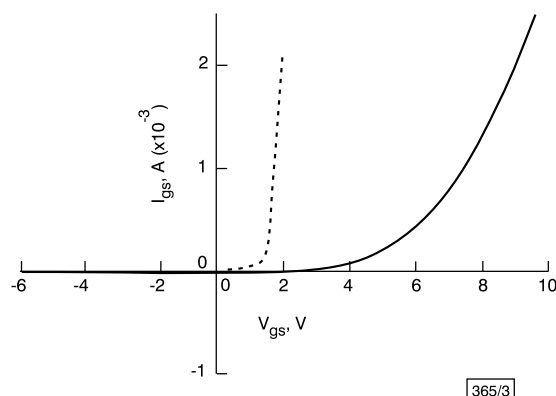


Fig. 3 Current voltage characteristics of *pn* junction and Schottky gate devices

— *pn* junction device
--- Schottky gate device

The maximum current for heterostructure field-effect transistors depends on the maximum charge induced in the device channel. This charge increases with the increase in positive gate bias (for an *n*-channel device). Thus the maximum saturation current is limited by the gate leakage at positive bias. For our enhancement mode transistor with a *pn* junction gate, the range of positive gate bias which maintains a low gate leakage current is significantly larger than that for a regular Schottky-gate device. This is illustrated by Fig. 3 showing gate channel I-V curves for a *pn* junction gate enhancement mode HFET and a regular Schottky gate HFET on the same wafer. As seen, for a *pn* junction gate device the maximum operating gate voltage can be as high as 3 V as compared to ~1 V maximum operating voltage for a Schottky gate

HFET. This proves that in principle, *pn* junction gate enhancement mode HFETs can provide much higher induced channel charge, and hence, saturation current and transconductance as compared to a Schottky gate depletion mode HFET.

Our estimates of the threshold voltage as a function of the distance between the channel and the gate showed that the effective channel-to-gate separation is close to the thickness of the AlGa_N layer. This means that the *p*-type AlGa_N layer operates as a *p*-type gate. As a result, the threshold voltage is shifted by ~2.5V towards positive values (i.e. by the difference between the Ga_N energy gap and the Schottky barrier height).

In Fig. 3 it can be seen that the differential resistance of the *pn* junction gate is ~1k Ω . This resistance is largely due to the relatively low doping level in regrown *p*-material as well as to the low hole mobility in *p*-Ga_N. The *pn* junction gate capacitance was measured to be < 1pF. Using these values of gate series resistance and capacitance, we estimate the characteristic time constant RC of our enhancement mode HFET to be < 1ns. By making use of a higher doping level in the *p*-Ga_N gate material and with shorter gate length this time constant can be considerably decreased to achieve switching rates in the gigabit per second range.

In conclusion we have fabricated a new enhancement mode Ga_N/AlGa_N HEMT with a selective area deposited *pn* junction gate. We have also established the feasibility of our approach to produce enhancement and depletion mode Ga_N/AlGa_N HEMTs on the same wafer. This is an important step towards the goal of realising monolithically integrated logic circuits based on AlGa_N/Ga_N heterojunctions.

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