Case No: IPR2023-01382
Patent No. 9,748,347

Case No: IPR2023-01384
Patent No. 10,312,335

Petitioner's Demonstrative Exhibits

Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc.
v. Efficient Power Conversion Corporation

January 7, 2024

INNOSCIENCE EXHIBIT 1033
INNOSCIENCE v. EPC
IPR2023-01384

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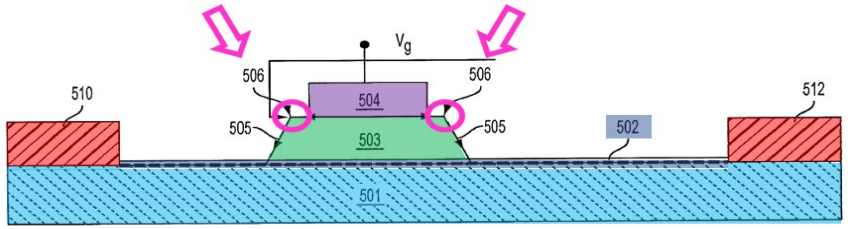
Overview of the ’347 and ’335 Patents and the Admitted Prior Art

The ’347 and ’335 patents

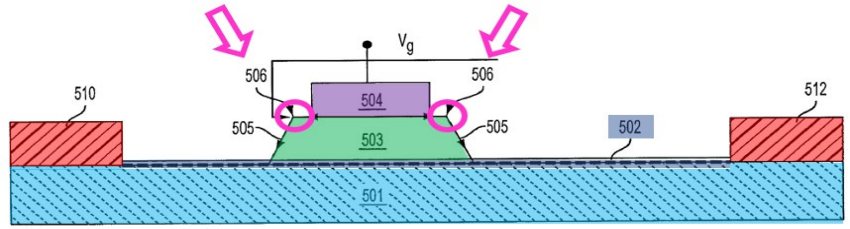
’347 patent claim 1: Method



[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a **GaN layer**;
[1b] forming a **barrier layer** on the **GaN layer**;
[1c] depositing **source** and a **drain contacts** on the **barrier layer**;
[1d] depositing a **p-type gate material** on the **barrier layer**;
[1e] depositing a **gate metal** on the **p-type gate material**;
[1f] forming a photoresist over the **gate metal**;
[1g] etching the **gate metal** and the **p-type gate material**,
[1h] wherein the step of etching the **p-type gate material** comprises forming side surface of **the p-type gate material** that extend horizontally towards the **source** and **drain contacts**, respectively, and contact the **barrier layer**; and
[1i] etching the gate metal to form a pair of **ledges** on the **p-type gate material** below the gate metal..

’335 patent claim 1: Device



[1p] An enhancement-mode GaN transistor, comprising:

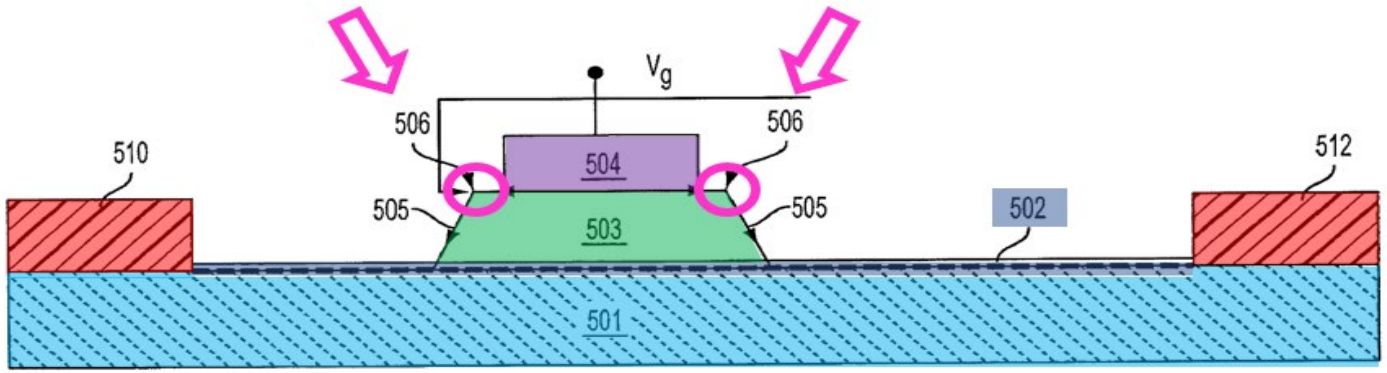
[1a] a **GaN layer**;
[1b] a **barrier layer** disposed on the **GaN layer** with a 2DEG region formed at an interface between the **GaN layer** and the **barrier layer**;
[1c] a **source contact** and a **drain contact** formed on the barrier layer;
[1d] a **p-type gate material** formed above the **barrier layer**, the **p-type gate material having side surfaces extending horizontally** towards the **source contact and drain contact**, respectively, and contacting the **barrier layer**; and
[1e] a **gate metal** disposed on the **p-type gate material**, the **gate metal** having sidewalls extending towards the **p-type gate material**,
[1f] wherein the **p-type gate material** comprises a pair of **horizontal ledges** that extend past the respective sidewalls of the **gate metal** and toward the **source contact and the drain contact**, respectively, the pair of **horizontal ledges** having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the **p-type gate material**, respectively.

’347 patent claim 1; ’335 patent, claim 1

Admitted Prior Art Has All But Self-Aligned Ledges

Innoscience

Alleged Invention



A pair of self-aligned ledges on p-type gate material is the *only* claimed feature of that is not admitted prior art

Admitted Prior Art: ’335 and ’347 Patent

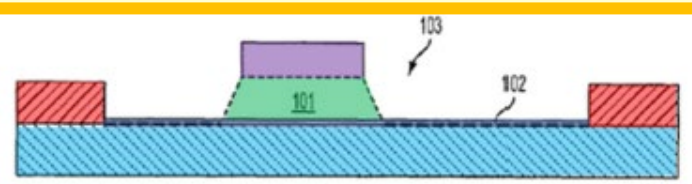


FIG. 1
PRIOR ART

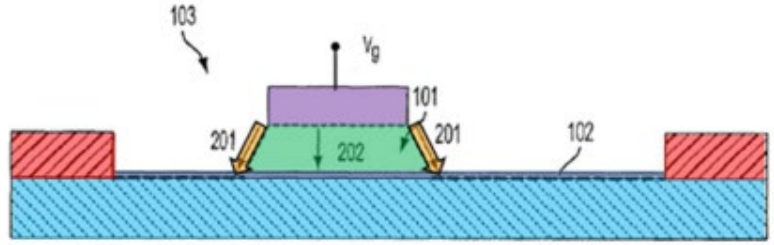


FIG. 2
PRIOR ART

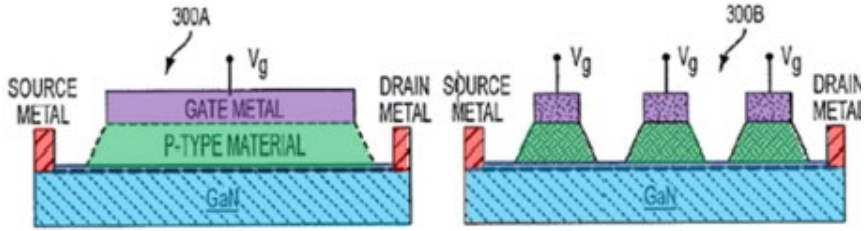


FIG. 3A
PRIOR ART

FIG. 3B
PRIOR ART

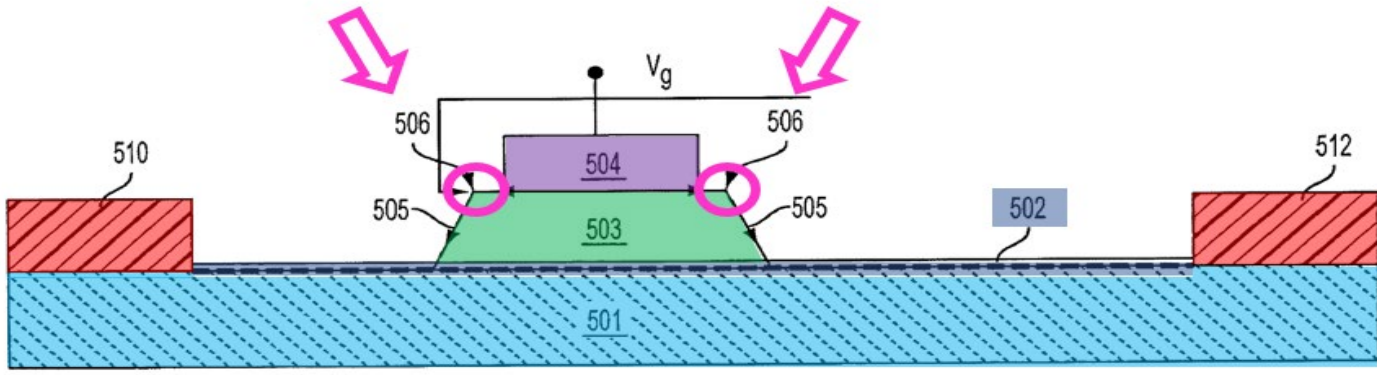
Ex. 1001, Figs. 1-2, 3A-3B.

’335 Paper No. 1 (’335 Pet.”), 8-10; ’347 Paper No. 1 (“’347 Pet.”), 8-10.

Admitted Prior Art Has All But Self-Aligned Ledges

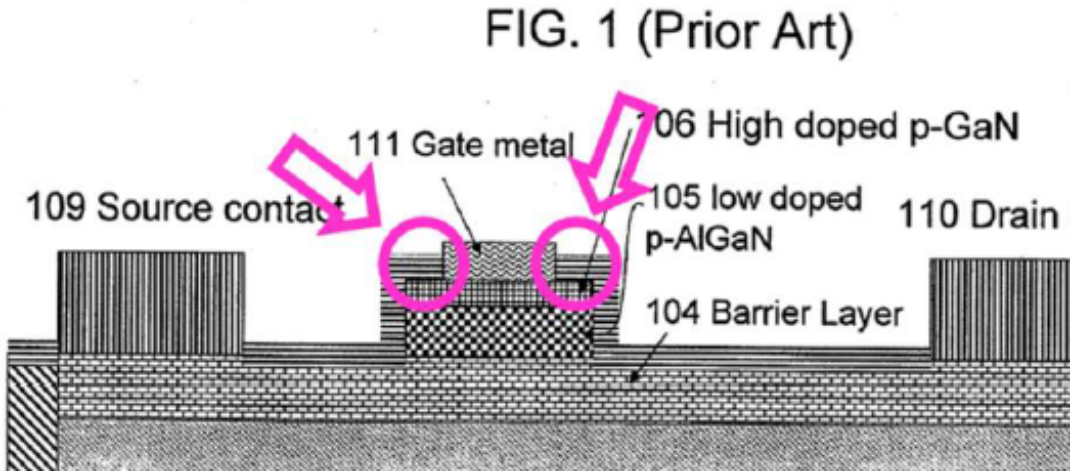
Innoscience

Alleged Invention



A pair of self-aligned ledges on p-type gate material is the *only* claimed feature of that is not admitted prior art

Admitted Prior Art: ’335 and ’347 Patent



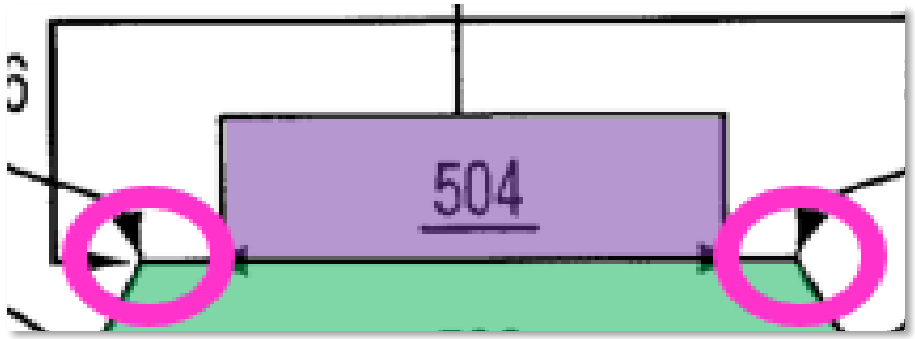
Priority Application Lidow (Ex. 1011) shows prior art ledges of equal width but does not describe that they are self-aligned

’335 Pet., 8-13; ’347 Pet., 8-12; Ex. 1011 (Lidow), [0006], Fig. 1.

Admitted Prior Art Has All But Self-Aligned Ledges

Innoscience

Alleged Invention

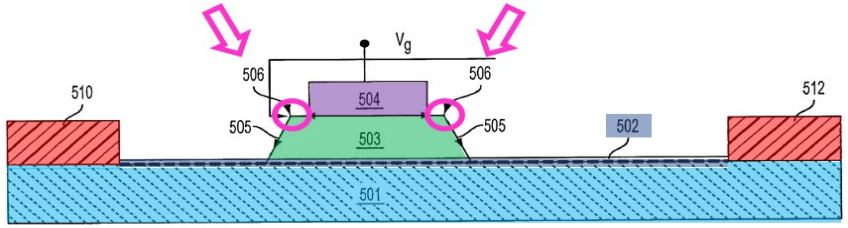


A pair of self-aligned ledges on p-type gate material is the *only* claimed feature of that is not admitted prior art

’335 Pet., 8-13; ’347 Pet., 8-12.

Admitted Prior Art Has All But Self-Aligned Ledges

’347 patent: Claims 1 and 3



Admitted Prior art

Admitted

Admitted

Admitted

Admitted

Admitted

Admitted

Admitted Prior art

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a **GaN layer**;

[1b] forming a **barrier layer** on the **GaN layer**;

[1c] depositing **source** and a **drain contacts** on the **barrier layer**;

[1d] depositing a **p-type gate material** on the **barrier layer**;

[1e] depositing a **gate metal** on the **p-type gate material**;

[1f] forming a photoresist over the **gate metal**;

[1g] etching the **gate metal** and the **p-type gate material**,

[1h] wherein the step of etching the **p-type gate material** comprises forming side surface of **the p-type gate material** that extend horizontally towards the **source** and **drain contacts**, respectively, and contact the **barrier layer**; and

Admitted Prior Art

[1i] etching the gate metal to form a pair of **ledges** on the **p-type gate material** below the gate metal.

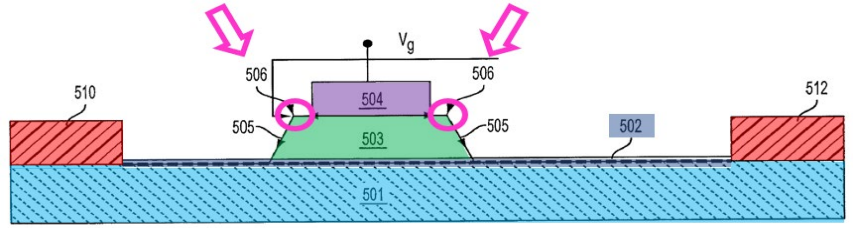
Not Admitted

[3] The method according to claim 1, wherein the pair of **ledges** of the **p-type gate material** are **self-aligned**.

’347 Pet., 8-12.

Admitted Prior Art Has All But Self-Aligned Ledges

’335 patent: Claims 1 and 2



Admitted Prior art

Admitted Prior art

Admitted Prior art

Admitted Prior art

Admitted Prior art

Admitted Prior art

Not Admitted

[1p] An **enhancement-mode** GaN transistor, comprising:

[1a] a GaN layer;

[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[1c] a source contact and a drain contact formed on the barrier layer;

[1d] a p-type gate material formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the source contact and drain contact, respectively, and contacting the barrier layer; and

[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

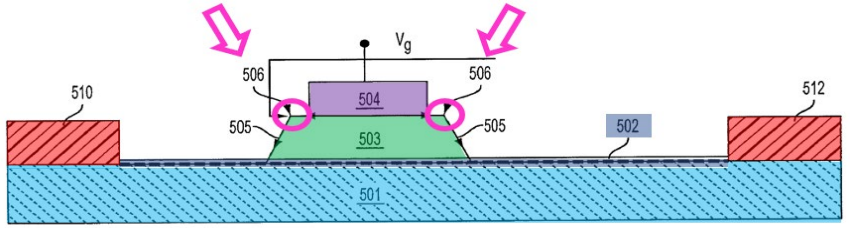
[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of **horizontal ledges** having **substantially equal widths** from the sidewalls of the gate metal to the side surfaces of the **p-type gate material**, respectively.

[2] The enhancement mode transistor according to claim 1, wherein the pair of **ledges** of the **p-type gate material** are **self-aligned**.

’335 Pet., 8-13.

Admitted Prior Art Has All But Self-Aligned Ledges

’335 patent: Claim 5



Admitted

Admitted

Admitted Prior art

[5p] An **enhancement-mode** GaN transistor, comprising:

[5a] a **GaN layer**;

[5b] a **barrier layer** disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

Admitted Prior art

[5c] a **source contact** and a **drain contact** formed on the barrier layer;

Admitted Prior art

[5d] a **p-type gate material** formed above the barrier layer and between the source and drain contacts,

Admitted

[5e] **a gate metal** disposed on **the p-type gate material**,

Not Admitted

[5f] wherein the p-type gate material comprises: (i) a pair of **self-aligned ledges** that extend past sidewalls of the **gate metal** towards the **source contact** and **drain contact**, respectively; and

Admitted Prior art

[5g] (ii) **side surfaces that extend horizontally** towards the source contact and drain contact, respectively, and contact the **barrier layer.**

’335 Pet., 8-13.

’347 Patent: Undisputed Statement of Facts under 37 C.F.R. § 42.22(c)

Innoscience

Before April 8, 2009, the following were known:

- ✓ [1.a] Forming a GaN layer;
- ✓ [1.b] Forming a barrier layer on the GaN layer;
- ✓ [1.c] Depositing source and drain contacts on the barrier layer;
- ✓ [1.d] Depositing a p-type gate material on the barrier layer;
- ✓ [1.e] Depositing a gate metal on the p-type gate material;
- ✓ [1.f] Forming a photoresist over the gate metal;
- ✓ [1.g] Etching the gate metal, and;
- ✓ [1.h] Etching the p-type gate material to form side surfaces that slope towards the source and drain contacts;
- ✓ [2.a] 1.a-1.g (agove)
- ✓ [2.b] etching the p-type gate material; and
- ✓ [2.c] including a pair of ledges on the p-type gate material below the gate metal;
- ✓ [3] self-aligned gate structures

Patent Owner Did Not Dispute These Facts

- All facts thus admitted. ’347 Reply, 2; *AVX Corp. v. Presidio Components, Inc.*, IPR2018-00292, Paper No. 16 at 9 (P.T.A.B. May 15, 2019).
- Patent Owner sidestepped the merits by asking the Board to “ignore[]” the statement because it did not cite the record. ’347 POR, 10.
  - A Statement “preferably” cites the record, but the law does not require citations. 37 C.F.R. § 42.22(c).
  - The Petition repeatedly showed the patent admitted these facts. ’347 Pet., 8-11, 18; ’347 Shealy, [044]-[046].

’347 Pet., 18; Paper No. 17 (’347 POR) 10; Paper No. 19 (’347 Reply), 2-3; Paper No. 21 (’347 Sur-Reply), ’347 Exhibit 1003 (“’347 Shealy”), [044]-[046].

’335 Patent: Undisputed Statement of Facts under 37 C.F.R. § 42.22(c)

Innoscience

Before April 8, 2009, the following were known:

- ✓ [1.a] A **GaN** layer;
- ✓ [1.b] An **AlGaN barrier layer** disposed on the **GaN layer**;
- ✓ [1.c] **Source and drain electrodes** disposed on the **AlGaN barrier layer**;
- ✓ [1.d] A gate structure disposed on the **barrier layer** between **source and drain electrodes**;
- ✓ [1.e] A gate structure with a **p-type GaN layer with sloped sidewalls that extend horizontally** towards **the source and drain electrodes**;
- ✓ [1.f] A gate structure with an overlying **gate metal**;
- ✓ [2] Self-aligned gate structures.

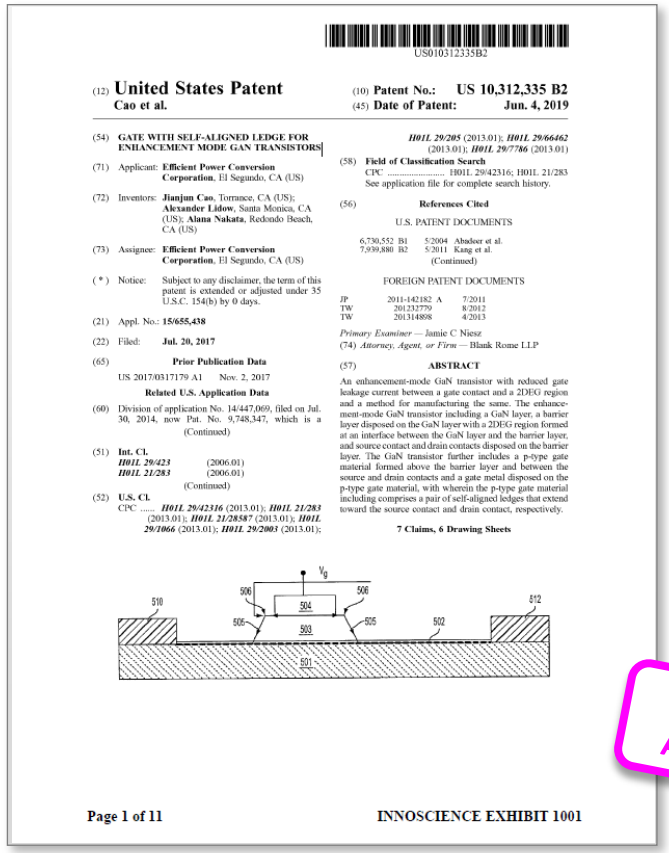
Patent Owner Did Not Dispute These Facts

- All facts thus admitted. ’335 Reply, 2; *AVX Corp. v. Presidio Components, Inc.*, IPR2018-00292, Paper No. 16 at 9 (P.T.A.B. May 15, 2019).
- Patent Owner sidestepped the merits by asking the Board to “ignore[]” the statement because it did not cite the record. ’335 POR, 8.
  - A Statement “preferably” cites the record, but the law does not require citations. 37 C.F.R. § 42.22(c).
  - The Petition repeatedly showed the patent admitted these facts. ’335 Pet., 8-9, 17-18; ’335 Shealy [044]-[046].

’335 Pet., 1-2, 8-9, 17-18; Paper No. 17 (’335 POR) 8; Paper No. 19 (’335 Reply), 2; Paper No. 21 (’335 Sur-Reply), 3-4; ; ’335 Exhibit 1003 (“’335 Shealy”), [044]-[046].

The ’335 patent has just one alleged new feature

A pair of self-aligned ledges on p-type gate material is the *only* feature of the claimed enhancement mode GaN transistor that is not admitted prior art



US010312335B2

(12) **United States Patent**
Cao et al.

(10) **Patent No.: US 10,312,335 B2**
(45) **Date of Patent: Jun. 4, 2019**

(54) **GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GAN TRANSISTORS**

(71) Applicant: **Efficient Power Conversion Corporation**, El Segundo, CA (US)

(72) Inventors: **Jianjun Cao**, Torrance, CA (US); **Alexander Lidow**, Santa Monica, CA (US); **Alana Nakata**, Redondo Beach, CA (US)

(73) Assignee: **Efficient Power Conversion Corporation**, El Segundo, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/655,438**

(22) Filed: **Jul. 20, 2017**

(65) **Prior Publication Data**

US 2017/0317179 A1 Nov. 2, 2017

Related U.S. Application Data

(60) Division of application No. 14/447,069, filed on Jul. 30, 2014, now Pat. No. 9,748,347, which is a (Continued)

(51) **Int. Cl.**
H01L 29/423 (2006.01)
H01L 21/283 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/42316*** (2013.01); ***H01L 21/283*** (2013.01); ***H01L 21/28587*** (2013.01); ***H01L 29/1066*** (2013.01); ***H01L 29/2003*** (2013.01); ***H01L 29/205*** (2013.01); ***H01L 29/66462*** (2013.01); ***H01L 29/7786*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/42316; H01L 21/283
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,730,552 B1 5/2004 Abadeer et al.
7,939,880 B2 5/2011 Kang et al.
(Continued)

FOREIGN PATENT DOCUMENTS

JP 2011-142182 A 7/2011
TW 201232779 8/2012
TW 201314898 4/2013

Primary Examiner — Jamie C Niesz
(74) *Attorney, Agent, or Firm* — Blank Rome LLP

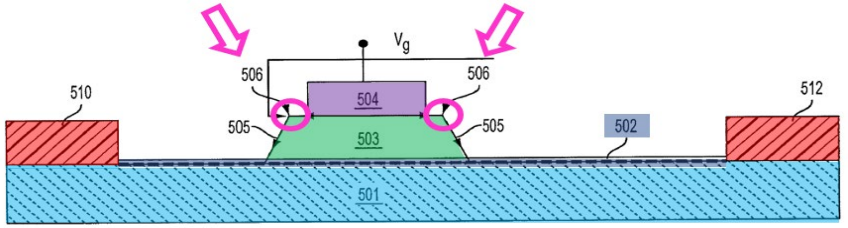
(57) **ABSTRACT**

An enhancement-mode GaN transistor with reduced gate leakage current between a gate contact and a 2DEG region and a method for manufacturing the same. The enhancement-mode GaN transistor including a GaN layer, a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer, and source contact and drain contacts disposed on the barrier layer. The GaN transistor further includes a p-type gate material formed above the barrier layer and between the source and drain contacts and a gate metal disposed on the p-type gate material, with wherein the p-type gate material including comprises a pair of self-aligned ledges that extend toward the source contact and drain contact, respectively.

7 Claims, 6 Drawing Sheets

Page 1 of 11 INNOSCIENCE EXHIBIT 1001

Not Admitted



[1p] An **enhancement-mode** GaN transistor, comprising:

[1a] a GaN layer;

[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[1c] a source contact and a drain contact formed on the barrier layer;

[1d] a p-type gate material formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the source contact and drain contact, respectively, and contacting the barrier layer; and

[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

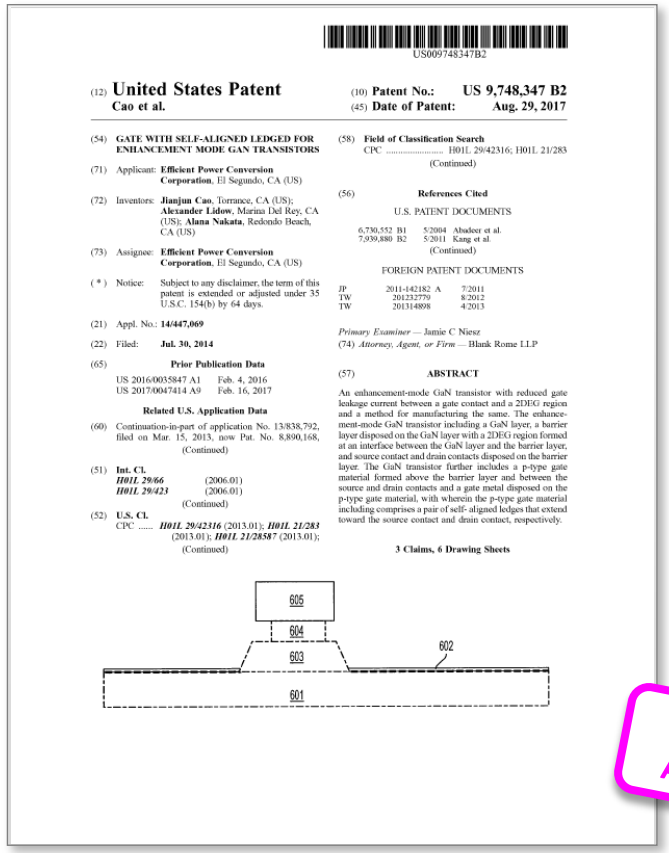
[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of **horizontal ledges** having **substantially equal widths** from the sidewalls of the gate metal to the side surfaces of the **p-type gate material**, respectively.

[2] The enhancement mode transistor according to claim 1, wherein the pair of **ledges** of the **p-type gate material** are **self-aligned**.

’335 Patent, Cover; ’335 Pet., 1-2, 8-13.

The ’347 patent has just one alleged new feature

Forming a pair of self-aligned ledges on p-type gate material is the *only* feature of the claimed method that is not admitted prior art



US009748347B2

(12) **United States Patent**
Cao et al.

(10) **Patent No.: US 9,748,347 B2**
(45) **Date of Patent: Aug. 29, 2017**

(54) **GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GAN TRANSISTORS**

(71) Applicant: **Efficient Power Conversion Corporation**, El Segundo, CA (US)

(72) Inventors: **Jianjun Cao**, Torrance, CA (US); **Alexander Lidow**, Marina Del Rey, CA (US); **Alana Nakata**, Redondo Beach, CA (US)

(73) Assignee: **Efficient Power Conversion Corporation**, El Segundo, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 64 days.

(21) Appl. No.: **14/447,069**

(22) Filed: **Jul. 30, 2014**

(65) **Prior Publication Data**

US 2016/0035847 A1 Feb. 4, 2016
US 2017/0047414 A9 Feb. 16, 2017

Related U.S. Application Data

(60) Continuation-in-part of application No. 13/838,792, filed on Mar. 15, 2013, now Pat. No. 8,890,168, (Continued)

(51) **Int. Cl.**
H01L 29/66 (2006.01)
H01L 29/423 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/42316*** (2013.01); ***H01L 21/283*** (2013.01); ***H01L 21/28587*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 29/42316; H01L 21/283
(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,730,552 B1 5/2004 Abadeer et al.
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(Continued)

FOREIGN PATENT DOCUMENTS

JP 2011-142182 A 7/2011
TW 201232779 8/2012
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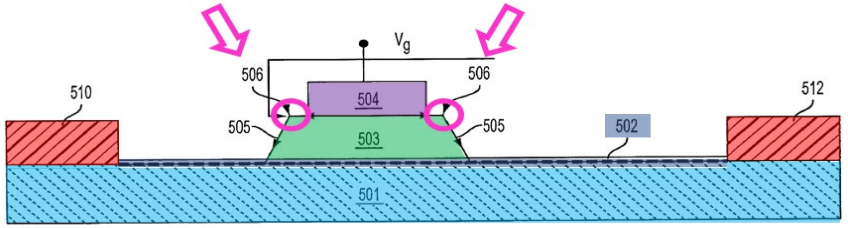
Primary Examiner — Jamie C Niesz
(74) *Attorney, Agent, or Firm* — Blank Rome LLP

(57) **ABSTRACT**

An enhancement-mode GaN transistor with reduced gate leakage current between a gate contact and a 2DEG region and a method for manufacturing the same. The enhancement-mode GaN transistor including a GaN layer, a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer, and source contact and drain contacts disposed on the barrier layer. The GaN transistor further includes a p-type gate material formed above the barrier layer and between the source and drain contacts and a gate metal disposed on the p-type gate material, with wherein the p-type gate material including comprises a pair of self- aligned ledges that extend toward the source contact and drain contact, respectively.

3 Claims, 6 Drawing Sheets

Not Admitted



[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

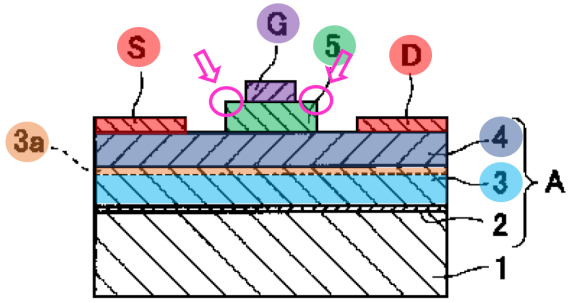
[1a] forming a **GaN layer**;
[1b] forming a **barrier layer** on the **GaN layer**;
[1c] depositing **source** and a **drain contacts** on the **barrier layer**;
[1d] depositing a **p-type gate material** on the **barrier layer**;
[1e] depositing a **gate metal** on the **p-type gate material**;
[1f] forming a photoresist over the **gate metal**;
[1g] etching the **gate metal** and the **p-type gate material**,
[1h] wherein the step of etching the **p-type gate material** comprises forming side surface of **the p-type gate material** that extend horizontally towards the **source** and **drain contacts**, respectively, and contact the **barrier layer**; and
[1i] etching the gate metal to form a pair of **ledges** on the **p-type gate material** below the gate metal.

[3] The method according to claim 1, wherein the pair of **ledges** of the **p-type gate material** are **self-aligned**.

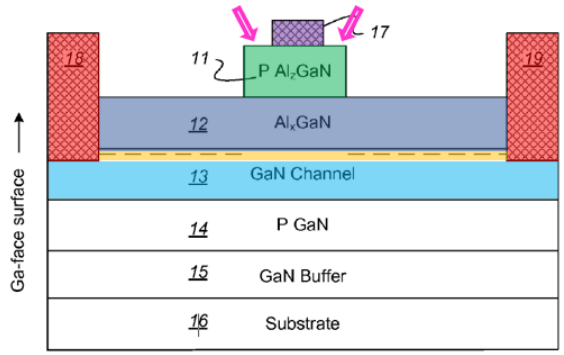
EX. 1001, Cover; ’347 Pet., 1-2.

The alleged new feature was well known

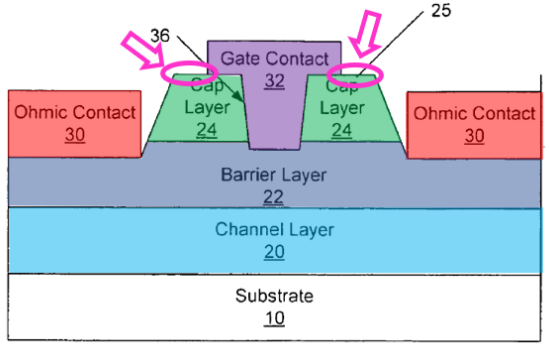
Horizontal ledges on p-type gate material were well known as of April 8, 2009



Ex. 1005 (*Yoshida*) (1999)



Ex. 1017 (*Suh*) (2009).



Ex. 1007 (*Saxler*) (2006)

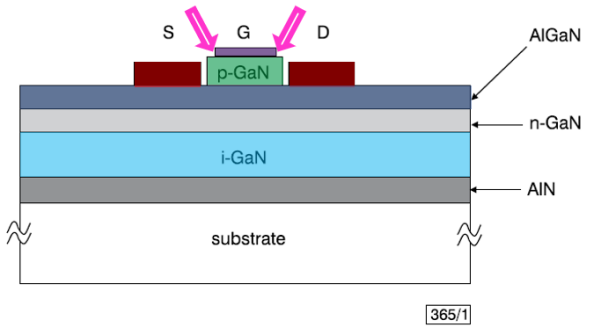


Fig. 1 *Schematic diagram of structure of pn junction regrown gate HFET*

Ex. 1018 (*Hu*) (2000)

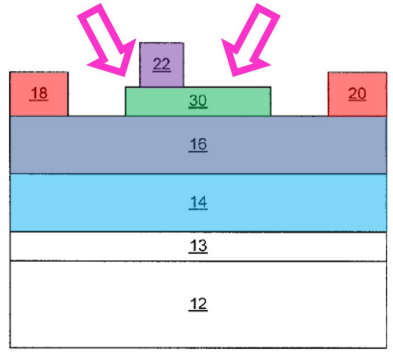


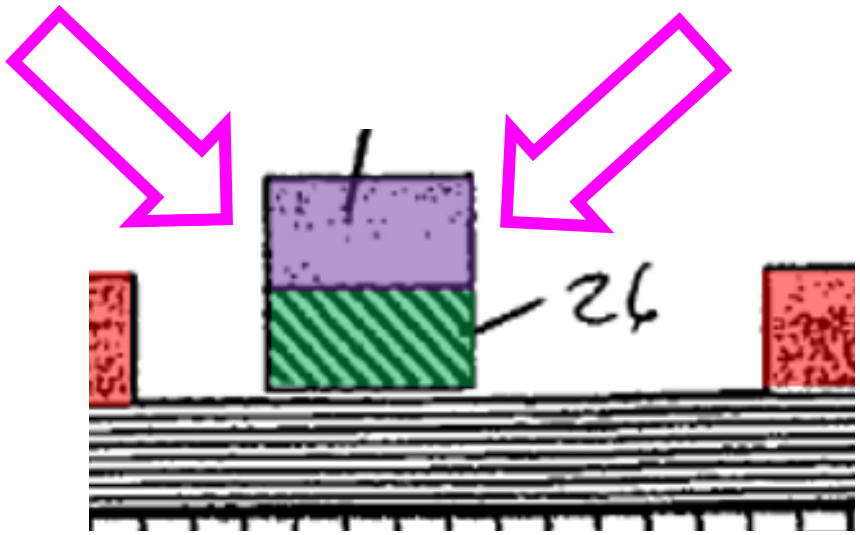
Figure 5B

Ex. 1015 (*Smith*) (2002).

'335 Pet., 3-8; '347 Pet., 2-10.

The alleged new feature was well known

Self-Aligned gate structures using a single mask were well known as of April 8, 2009



Beach, Fig. 1.

FIG. 4A

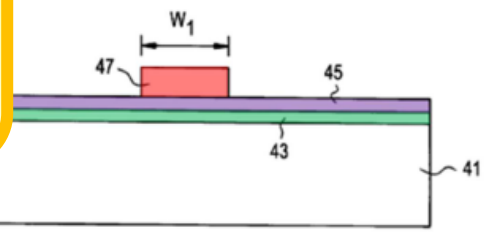


FIG. 4B

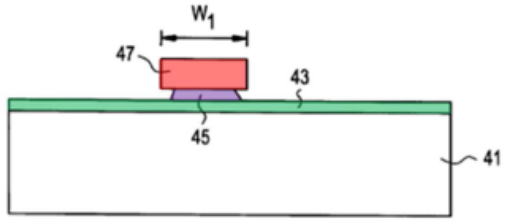
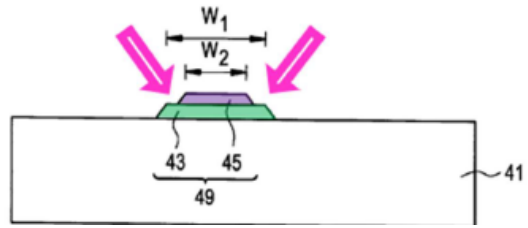


FIG. 4C



Ahn, Figs. 4A-4C.

The self-aligned approach uses a single mask

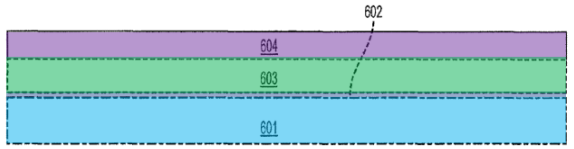


FIG. 6A

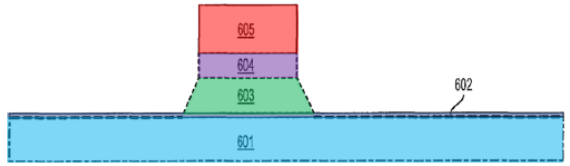


FIG. 6B

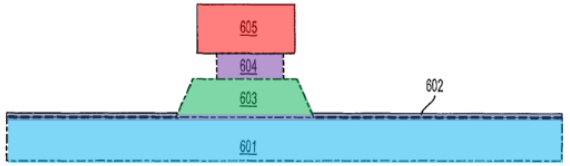


FIG. 6C

'335 and '347 Patents, Figs. 6A-6C

'335 Pet., 6-7, 11-12, 57-58, 60-63; '347 Pet., 6-7, 11-12, 26-35, 60-62;
Beach, [0040], [0045], [0054], Fig. 1; *Smith*, [0041]-[0044] Fig. 5B; *Ahn*, 4:52-49, 5:55-62, 6:27-37, 7:15-46, Figs. 4A-4C; '347 Shealy, [094].

Claim Construction

Claim Construction Overview

Two Terms Construed in the Petitions

1) ’335 and ’347 Patents: “side surfaces” limitations

’335 Patent claims 1 and 5: “side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer”

’347 Patent claim 1: “forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer”

2) ’335 Patent: “self-aligned” limitations

’335 Patent, claims 2 and 5: “self-aligned” ledges

1. No construction is needed to resolve the dispute--any horizontal extension satisfies the limitation

2. The prior art need not teach “self-aligned” because it is a product-by process limitation.

’335 Pet., 18-24; ’347 Pet., 19-23.

’335/’347: Any horizontal extension of “side surfaces”

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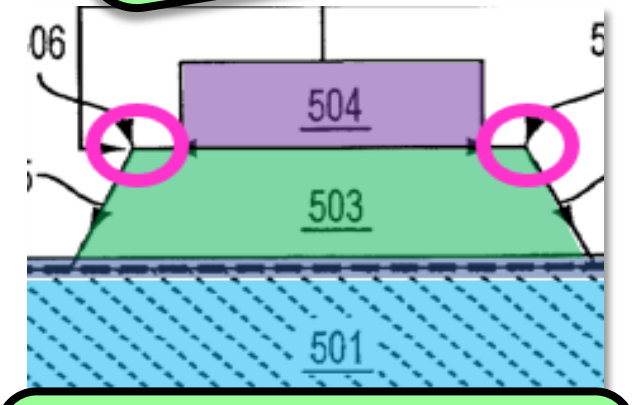
’335 Patent claims 1 and 5: “side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer”

’347 Patent claim 1: “forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer”

Petitioners’ Proposed Construction	Patent Owner’s ITC Construction	Patent Owner’s IPR Construction
“side surfaces of the p-type gate material such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces that contact the barrier layer”	“p-type gate material having side surfaces extending horizontally such that the bottom of the material is wider than the top of the material”	No construction needed

Board’s Construction at Institution
No construction needed

Under Board’s construction, any horizontal extension satisfies the claim



No need to resolve dispute further for purposes of validity. Petitioner adopts Board’s construction for this proceeding

’335 Pet., 18-23; Paper No. 7 (’335 POPR), 6-10; Paper No. 11 (’335 ID), 11-16.
’347 Pet., 19-23; Paper No. 7 (’347 POPR), 6-9; Paper No. 11 (’347 ID), 11-15.

’335/’347: Any horizontal extension of “side surfaces”

’335 Patent claims 1 and 5: “side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer”

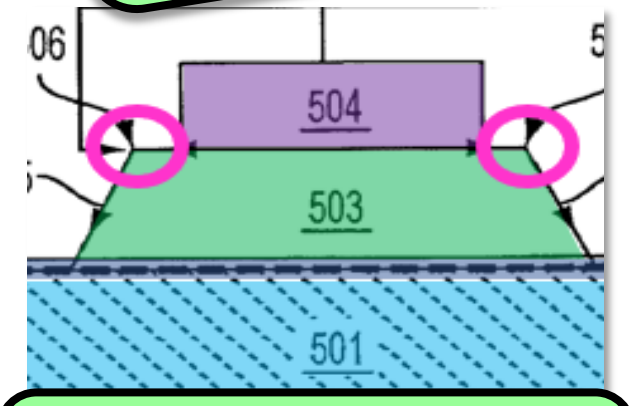
’347 Patent claim 1: “forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer”

“[B]ecause no express construction is needed for our decision, we do not construe them. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).’”

PNC Bank, N.A. v. United Servs. Auto. Ass’n, No. IPR2021-01073, Paper 72, 13 (P.T.A.B. Jan. 19, 2023).

Board’s Construction at Institution
No construction needed

Under Board’s construction, any horizontal extension satisfies the claim



No need to resolve dispute further for purposes of validity. Petitioner adopts Board’s construction for this proceeding

’335 Pet., 18-23; Paper No. 7 (’335 POPR), 6-10; Paper No. 11 (’335 ID), 11-16.
’347 Pet., 19-22; Paper No. 7 (’347 POPR), 6-9; Paper No. 11 (’347 ID), 11-15.

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1. No construction is needed to resolve the dispute—any horizontal extension satisfies the limitation

’335 Pet., 19-23; ’347 Pet., 19-22.

’335 Patent: “Self-Aligned” Lends No Patentable Weight

Innoscience

’335 Patent claims 2 and 5: “self-aligned” ledges

Petitioners’ Proposed Construction	Patent Owner’s IPR Construction
Product-by-process	Not product-by-process

Board’s Construction at Institution
Invite the parties to brief this issue, raising questions on Patent Owner’s Analysis

“Self-aligned” describes how the ledges are made, not what they are: no patentable weight

~~***[2] The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.***~~

[5f] wherein the p-type gate material comprises: (i) a pair of ~~***self-aligned***~~ ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively

’335 Pet., 23-24; ’335 Reply, 19-21.

’335 Patent: “Self-Aligned” Lends No Patentable Weight

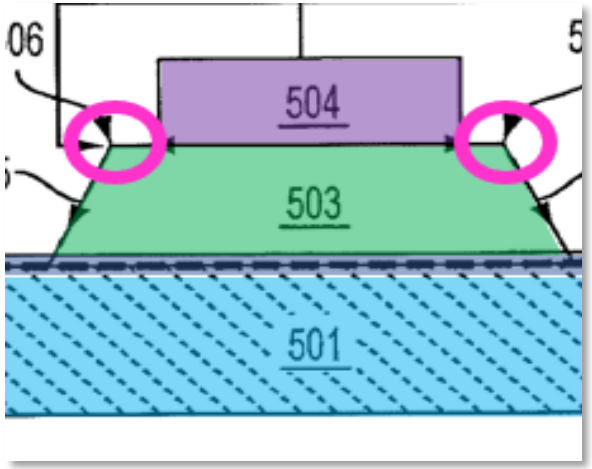
Innoscience

’335 Patent claims 2 and 5: “self-aligned” ledges

Petitioners’ Proposed Construction	Patent Owner’s IPR Construction
Product-by-process	Not product-by-process

Board’s Construction at Institution
Invite the parties to brief this issue, raising questions on Patent Owner’s Analysis

The Board noted “at least one other method can produce transistors with the same structure features” as a “self-aligned” approach and “the language in the Specification addresses making an old product using a new, more advantageous process.” ’335 ID, 18-19.



Patentability of the claimed transistor does not depend on *how* it is made. The patent says the claimed structure can be made by other processes.

’335 Pet., 23-24; ’335 ID, 16-20 ’335 Reply, 19-21

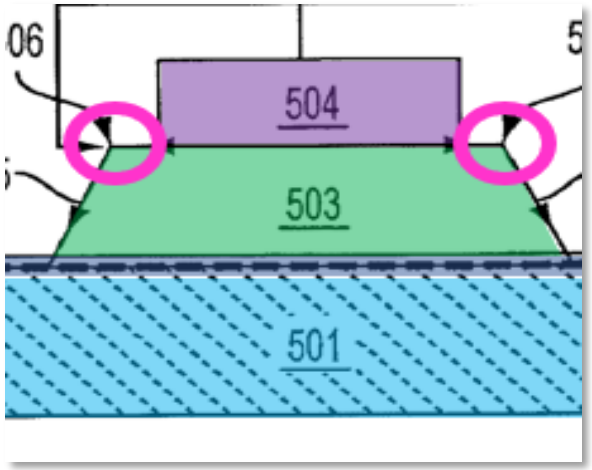
’335 Patent: “Self-Aligned” Lends No Patentable Weight

Innoscience

’335 Patent claims 2 and 5: “self-aligned” ledges

Petitioners’ Proposed Construction	Patent Owner’s IPR Construction
Product-by-process	Not product-by-process

Board’s Construction at Institution
Invite the parties to brief this issue, raising questions on Patent Owner’s Analysis



***In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985)**

> “The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.”

***Kamstrup A/S v. Axioma Metering UAB*, 43 F.4th 1374, 1381-83 (Fed. Cir. 2022)**

> Finding “cast in one piece” in claim to flow meter a product-by-process element that gives no patentable weight);

***United Therapeutics Corp. v. Liquidia Techs., Inc.*, 74 F.4th 1360, 1373 (Fed. Cir. 2023)**

> “As these claims are product claims, they are anticipated by a disclosure of the same product irrespective of the processes by which they are made.”).

Patentability of the claimed transistor does not depend on *how* it is made. The patent says the claimed structure can be made by other processes.

’335 Pet., 23-24; ’335 ID, 16-20; ’335 Reply, 19-21; ’335 Sur-Reply, 9.

’335 Patent: “Self-Aligned” Lends No Patentable Weight

’335 Patent claims 2 and 5: “self-aligned” ledges

It is undisputed that “self-aligned” refers to *how* the ledges are made

Patent Owner incorrectly alleges “self-aligned” connotes specific structure: a “minimum CD” (critical dimension) gate width and “substantially equal” ledges

But the patent provides different ways to make these features

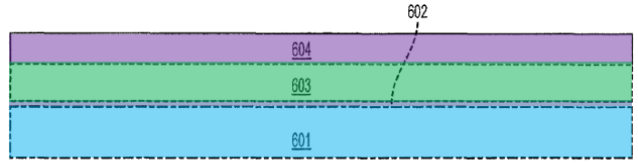


FIG. 6A

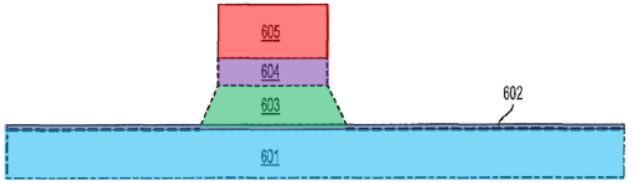


FIG. 6B

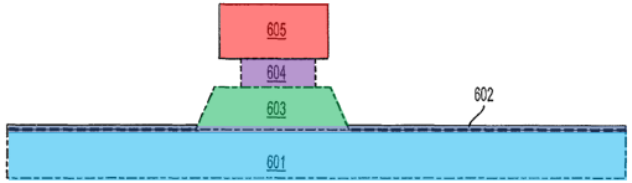


FIG. 6C

Patent Owner Incorrectly Argues That the Resulting Structure is Specific

’335 Pet., 23-24; ’335 POPR, 10-14; ’335 ID, 16-20; ’335 POR, 38-44; ’335 Reply, 19-21; ’335 Sur-Reply, 9.

’335 Patent: “Self-Aligned” Lends No Patentable Weight

Innoscience

’335 Patent claims 2 and 5: “self-aligned” ledges

The patent provides different ways to make “symmetric” ledges

- **Claim Differentiation: Claim 1 recites “substantially equal” ledges while claim 2 requires “self-aligned” ledges.**
- **Specification: The two-mask process may result in the *possibility* of misalignment, acknowledging that it may also result in alignment. ’335 patent, 4:52-63.**

The patent provides different ways to make reach “minimum CD”

- **Specification: The two-mask process “etch[es] the gate metal to a minimum CD”. ’335 patent, 4:57-58.**

The Reply is consistent with the Institution Decision

Patent Owner’s contrary expert testimony should be given no weight. ’335 Reply, 20-21 (citing Ex. 2005 ¶¶48-52; *Genuine Enabling Tech. LLC v. Nintendo Co., Ltd.*, 29 F.4th 1365, 1373 (Fed. Cir. 2022); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005)).

’335 Pet., 23-24; ’335 ID, 16-20; ’335 Reply, 19-21.

’335 Patent: “Self-Aligned” Lends No Patentable Weight

’335 Patent claims 2 and 5: “self-aligned” ledges

Prior art references Beach and Shenoy are only relied on for “self-aligned” ledges (Grounds 3, 6). If the Board agrees “self-aligned” is a product-by-process term, the claims are invalid over Saxler, Yoshida, and their combinations (Grounds 1-2, 4-5).

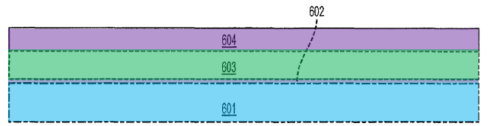


FIG. 6A

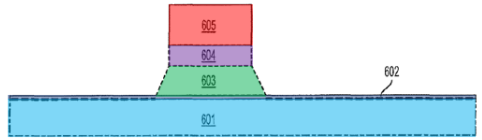


FIG. 6B

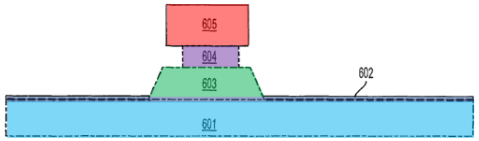
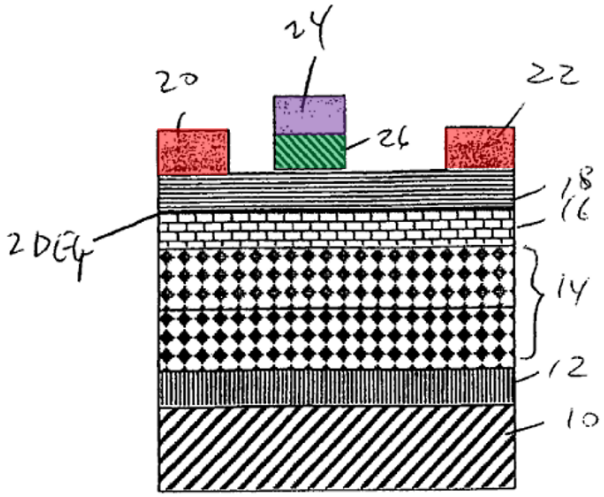


FIG. 6C



Beach, Fig. 1.

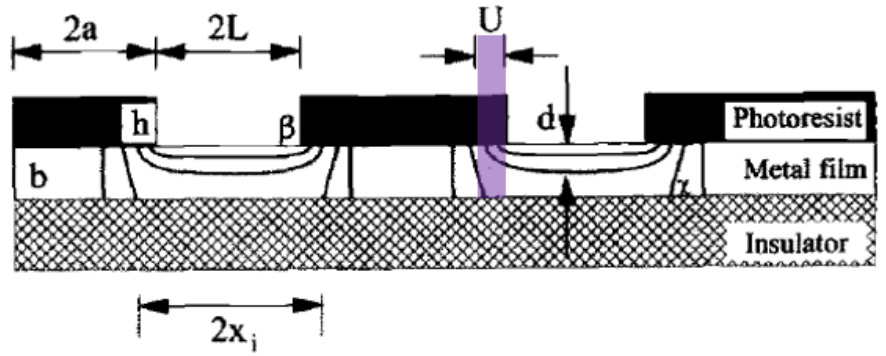


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

Shenoy, Fig. 1.

’335 Pet., 57-67, 88-97.

Claim Construction Overview

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’335 Patent, claims 2 and 5: “self-aligned” ledges

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2. The prior art need not teach “self-aligned” because it is a product-by process limitation.

’335 Pet., 18-24; ’347 Pet., 19-22.

’335 Patent Invalidity Grounds

’335 Patent Invalidity Grounds

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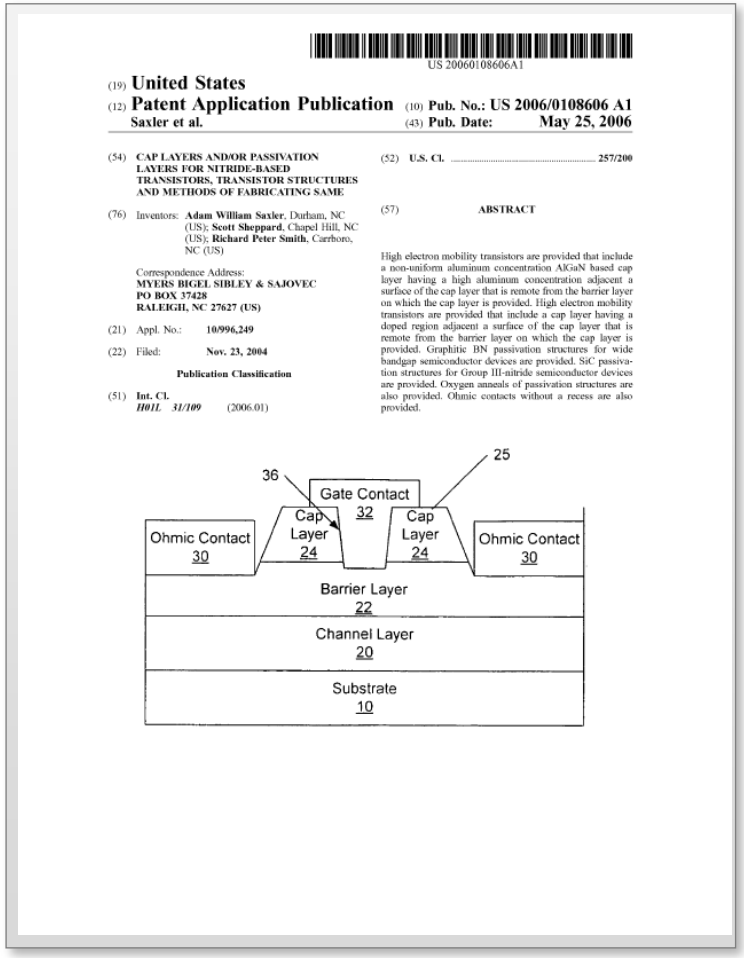
Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	**Saxler** in view of the knowledge of a POSITA
2	1-7	§ 103	**Saxler** in view of Yoshida
3	2, 5-7	§ 103	**Saxler** in view of Yoshida, Beach, and Shenoy
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA
5	1-7	§ 103	**Yoshida** in view of Saxler
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy

’335 Pet. at 29.

Saxler Renders the Claims of the ’335 Patent Obvious



US 20060108606A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0108606 A1**

Saxler et al. (43) **Pub. Date: May 25, 2006**

(54) **CAP LAYERS AND/OR PASSIVATION LAYERS FOR NITRIDE-BASED TRANSISTORS, TRANSISTOR STRUCTURES AND METHODS OF FABRICATING SAME**

(76) Inventors: **Adam William Saxler**, Durham, NC (US); **Scott Sheppard**, Chapel Hill, NC (US); **Richard Peter Smith**, Carrboro, NC (US)

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RALEIGH, NC 27627 (US)

(21) Appl. No.: **10/996,249**

(22) Filed: **Nov. 23, 2004**

Publication Classification

(51) **Int. Cl.**
H01L 31/109 (2006.01)

(52) **U.S. Cl.** **257/200**

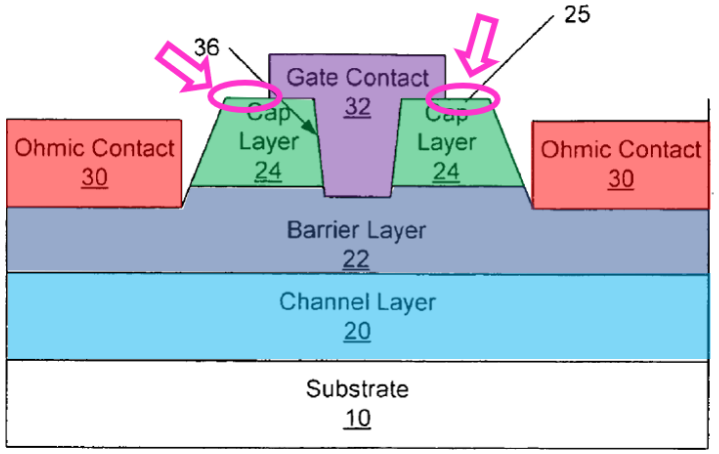
(57) **ABSTRACT**

High electron mobility transistors are provided that include a non-uniform aluminum concentration AlGaN based cap layer having a high aluminum concentration adjacent a surface of the cap layer that is remote from the barrier layer on which the cap layer is provided. High electron mobility transistors are provided that include a cap layer having a doped region adjacent a surface of the cap layer that is remote from the barrier layer on which the cap layer is provided. Graphitic BN passivation structures for wide bandgap semiconductor devices are provided. SiC passivation structures for Group III-nitride semiconductor devices are provided. Oxygen anneals of passivation structures are also provided. Ohmic contacts without a recess are also provided.

Ex. 1007 at Cover

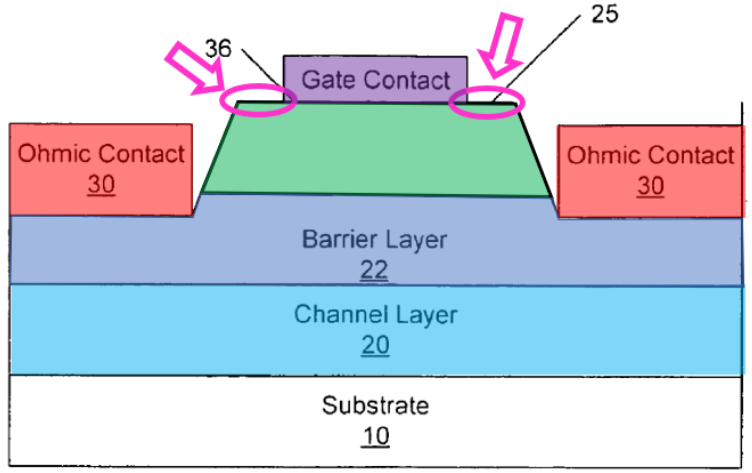
35 U.S.C. §102(b) Prior Art (published May 25, 2006)

Saxler depicts a depletion mode device with a recessed gate



Saxler, Fig. 1A.

A POSITA would have removed Saxler’s recess based on Saxler’s express teachings to do so and to achieve an enhancement mode device



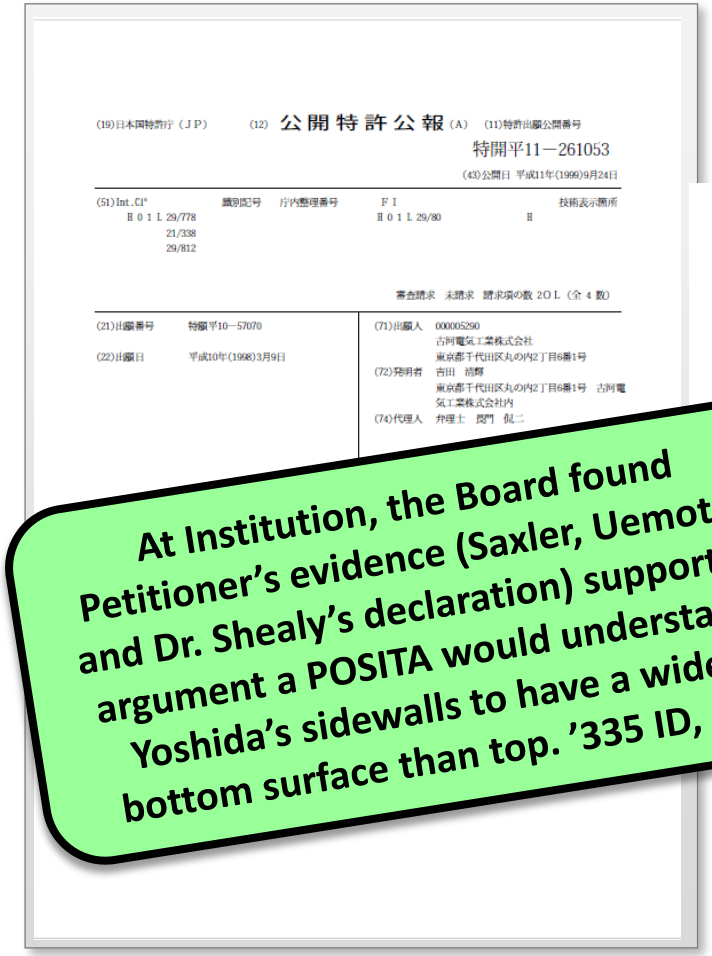
Saxler, Fig. 1A (modified).

If the Board agrees on claim construction, to find all claims invalid over Saxler (Ground 1) or Saxler-Yoshida (Ground 2), the Board need only:

- ✓ Agree modified Fig. 1A would have been obvious and is in enhancement mode
- ✓ Agree *Saxler’s* drawings can be relied on to disclose “substantially equal” ledges (no factual dispute, only a legal dispute that drawings can disclose this limitation)

’335 Pet. at Cover, 16, 25-26, 35-36.

Yoshida Renders the Claims of the ’335 Patent Obvious



(19)日本国特許庁（JP）　(12) 公開特許公報（A）　(11)特許出願公開番号

特開平11－261053

(43)公開日 平成11年(1999)9月24日

(51)Int.Cl.⁶　識別記号　庁内整理番号　F I　技術表示箇所

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21/338
29/812

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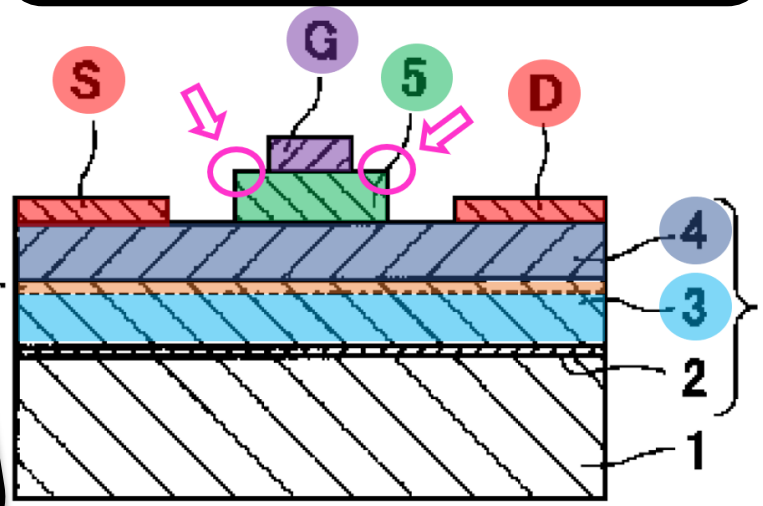
Ex. 1005 at Cover

35 U.S.C. §102(b) Prior Art (published Sept. 24, 1999)

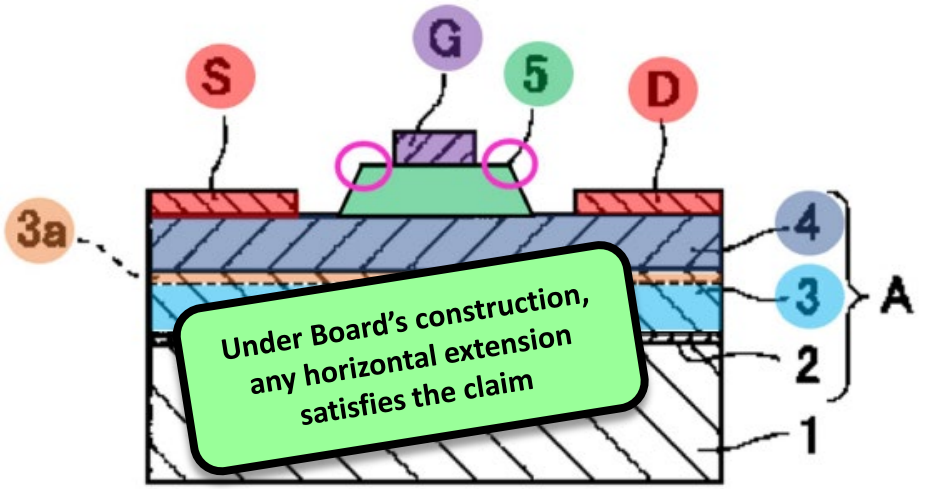
At Institution, the Board found Petitioner’s evidence (Saxler, Uemoto, and Dr. Shealy’s declaration) supported argument a POSITA would understand Yoshida’s sidewalls to have a wider bottom surface than top. ’335 ID, 51.

Yoshida depicts an enhancement mode device with every feature but the horizontally extended sidewalls



Yoshida, Fig. 1.

A POSITA would have found horizontally extended sidewalls obvious over Yoshida because perfectly vertical sidewalls were rare in practice when making real devices



Yoshida, Fig. 1 (modified).

If the Board agrees on claim construction, to find all claims invalid over Yoshida (Ground 4), the Board need only:

- ✓ Agree horizontally extended sidewalls were obvious because perfectly vertical sidewalls were rare in practice when making real devices
- ✓ Agree *Yoshida’s* drawings can be relied on to disclose “substantially equal” ledges (no factual dispute, only a legal dispute that drawings can disclose this limitation)

’335 Pet. at 16, 27, 67-68.

’335 Patent: Just Four Claim Features Disputed

Patent Owner only disputes the combinations of prior art shows *four* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1d], [5g] the **p-type gate material having side surfaces extending horizontally** (Yoshida alone)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivations to combine (grounds 2-3, 4-5)

At the Board found Petitioners’ evidence that p-type doping would provide an enhancement-mode transistor persuasive. The Board further noted that the cap layer *does not* extend from source to drain as Patent Owner alleged to argue the device non-operational. ’335 ID, 31.

At Institution, the Board found Petitioner’s evidence (Saxler, Uemoto, and Dr. Shealy’s declaration) supported argument a POSITA would understand Yoshida’s sidewalls to have a wider bottom surface than top. ’335 ID, 51.

At Institution, the Board reasoned “‘substantially’ is a common approximation or term of degree in patent claims,” which Patent Owner did not dispute, so *Hockerson* does not apply, and drawings can disclose this limitation. ’335 ID, 38-39.

The Board noted “at least one other method can produce transistors with the same structure features” as a “self-aligned” approach and “the language in the Specification addresses making an old product using a new, more advantageous process.” ’335 ID, 18-19.

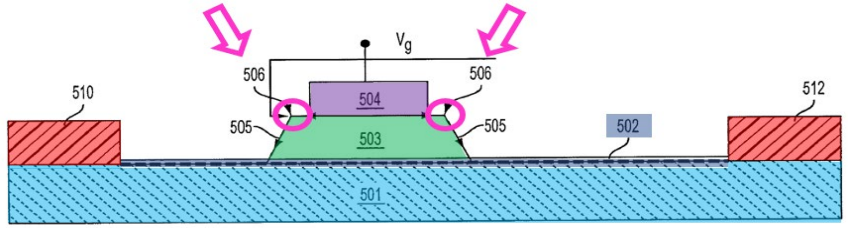
See generally ’335 POR

’335 Patent: Just Four Claim Features Disputed

Patent Owner only disputes the combinations of prior art shows *four* features of the ’335 patent claims 1-4

Disputed limitations:

- ✓ [1p] **enhancement mode** (Saxler grounds)
- ✓ [1d] the **p-type gate material having side surfaces extending horizontally** (Yoshida alone)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2] **self aligned ledges** (all grounds)



[1p] An **enhancement-mode** GaN transistor, comprising:

[1a] a GaN layer;

[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[1c] a source contact and a drain contact formed on the barrier layer;

[1d] a p-type gate material formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the source contact and drain contact, respectively, and contacting the barrier layer; and

[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of **horizontal ledges** having **substantially equal widths** from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

[2] The enhancement-mode GaN transistor according to claim1, wherein the pair **of horizontal ledges** of the **p-type gate material** are **self aligned.**

Disputed

Disputed

Disputed

Disputed

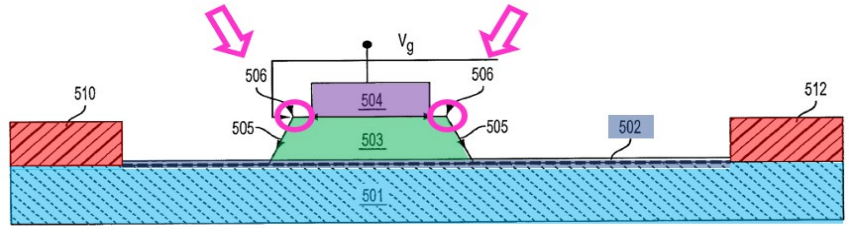
See generally ’335 POR.

’335 Patent: Just Four Claim Features Disputed

Patent Owner only disputes the combinations of prior art shows *three* features for claims 5-7

Disputed limitations:

- ✓ [5p] **enhancement mode** (Saxler grounds)
- ✓ [5g] the **p-type gate material** having side surfaces **extending horizontally** (Yoshida alone)
- ✓ [5f] **self aligned ledges** (all grounds)



[5p] An **enhancement-mode** GaN transistor, comprising:

[5a] a **GaN layer**;

[5b] a **barrier layer** disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[5c] a **source contact** and a **drain contact** formed on the barrier layer;

[5d] a **p-type gate material** formed above the barrier layer and between the source and drain contacts,

[5e] **a gate metal** disposed on **the p-type gate material**,

[5f] wherein the p-type gate material comprises: (i) a pair of **self-aligned ledges** that extend past sidewalls of the **gate metal** towards the **source contact** and **drain contact**, respectively; and **[5g]** (ii) **side surfaces that extend horizontally** towards the source contact and drain contact, respectively, and contact the **barrier layer.**

Disputed

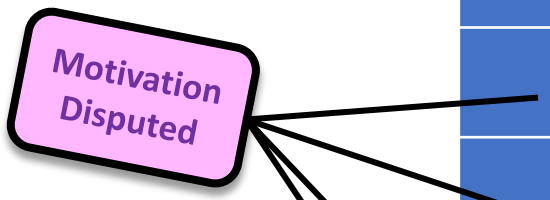
Disputed

Disputed

See generally ’335 POR

’335 Patent: Just Four Claim Features Disputed

Patent Owner disputes the motivations to combine for grounds 2, 3, 5, and 6



Ground	Challenged Claims	Ground
1	1-7	**Saxler** in view of the knowledge of a POSITA
2	1-7	**Saxler** in view of Yoshida
3	2, 5-7	**Saxler** in view of Yoshida, Beach, and Shenoy
4	1-7	**Yoshida** in view of the knowledge of a POSITA
5	1-7	**Yoshida** in view of Saxler
6	2, 5-7	**Yoshida** in view of Saxler, Beach, and Shenoy

See generally ’335 POR

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience

Saxler Grounds

Yoshida Grounds

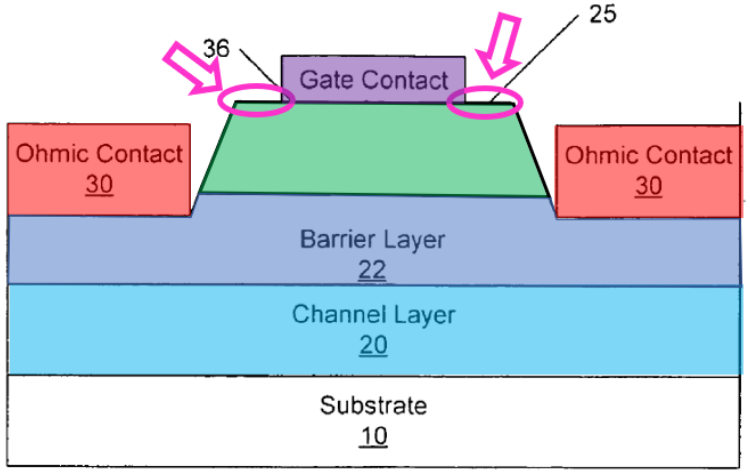
Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	**Saxler** in view of the knowledge of a POSITA
2	1-7	§ 103	**Saxler** in view of Yoshida
3	2, 5-7	§ 103	**Saxler** in view of Yoshida, Beach, and Shenoy
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA
5	1-7	§ 103	**Yoshida** in view of Saxler
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy

If the Board agrees on claim construction, to find all claims invalid over Saxler (Ground 1) or Saxler-Yoshida (Ground 2), the Board need only:

- ✓ Agree modified Fig. 1A would have been obvious and is in enhancement mode
- ✓ Agree *Saxler’s* drawings can be relied on to disclose “substantially equal” ledges (no factual dispute, only a legal dispute that drawings can disclose this limitation)

’335 Pet. at 16, 24-56.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

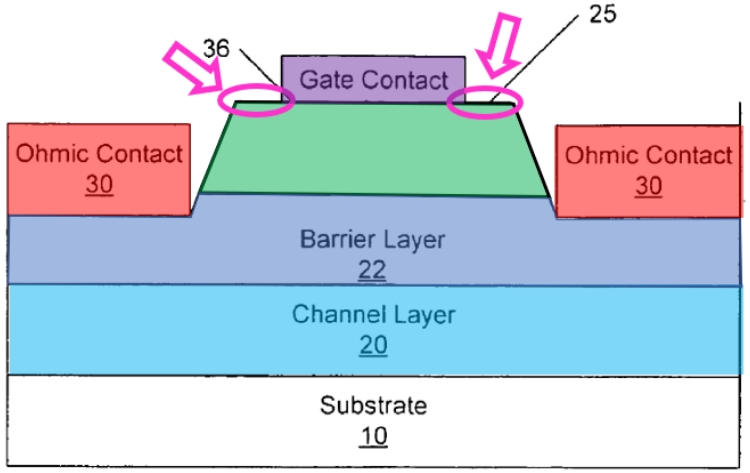


Saxler, Fig. 1A (modified).

’335 Pet. at 24-51

Saxler	Limitation
✓	**[1p]** An **enhancement-mode** GaN transistor, comprising:
✓	**[1a]** a **GaN layer**;
✓	**[1b]** a **barrier layer** disposed on the GaN layer with **a 2DEG region formed at an interface between the GaN layer and the barrier layer**;
✓	**[1c]** a **source contact** and a **drain contact** formed on the barrier layer;
✓	**[1d]** a **p-type gate material** formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the **source contact and drain contact**, respectively, and contacting the **barrier layer**; and
✓	**[1e]** a **gate metal** disposed on the **p-type gate material**, the **gate metal** having sidewalls extending towards the **p-type gate material**,
✓	**[1f]** wherein the **p-type gate material** comprises a pair of **horizontal ledges** that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of **horizontal ledges** having **substantially equal widths** from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.
No patentable weight	**[2]** The enhancement-mode GaN transistor according to claim 1, wherein the pair of **horizontal ledges** of the **p-type gate material** are **self-aligned**.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p]** An **enhancement-mode** GaN transistor, comprising:
✓	**[1a]** a **GaN layer**;
✓	**[1b]** a **barrier layer** disposed on the GaN layer with **a 2DEG region formed at an interface between the GaN layer and the barrier layer**;
✓	**[1c]** a **source contact** and a **drain contact** formed on the barrier layer;
✓	**[1d]** a **p-type gate material** formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the **source contact and drain contact**, respectively, and contacting the **barrier layer**; and
✓	**[1e]** a **gate metal** disposed on the **p-type gate material**, the **gate metal** having sidewalls extending towards the **p-type gate material**,
✓	**[1f]** wherein the **p-type gate material** comprises a pair of **horizontal ledges** that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of **horizontal ledges** having **substantially equal widths** from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.
No patentable weight	**[2]** The enhancement-mode GaN transistor according to claim 1, wherein the pair of **horizontal ledges** of the **p-type gate material** **are** **self-aligned**.

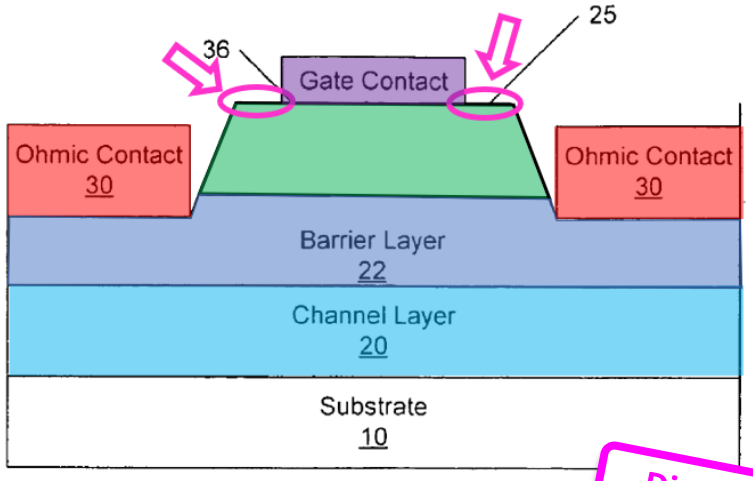
Disputed

Disputed

Disputed

’335 Pet. at 24-51; ’335 POR, 16-47.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[5p]** An **enhancement-mode** GaN transistor, comprising:
✓	**[5a]** a **GaN layer**;
✓	**[5b]** a **barrier layer** disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
✓	**[5c]** a **source contact** and a **drain contact** formed on the barrier layer;
✓	**[5d]** a **p-type gate material** formed above the barrier layer and between the source and drain contacts,
✓	**[5e]** **a gate metal** disposed on **the p-type gate material**,
✓	**[5f]** wherein the **p-type gate material** comprises: (i) a pair of **self-aligned ledges** that extend past sidewalls of the **gate metal** towards the **source contact** and **drain contact**, respectively; and
✓	**[5g]** (ii) **side surfaces that extend horizontally** towards the **source contact** and **drain contact**, respectively, and contact the **barrier layer.**

Disputed

Disputed

’335 Pet. at 24-51; ’335 POR, 16-47.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Patent Owner only disputes the Saxler combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivation to modify Saxler

See generally ’335 POR

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Patent Owner only disputes the Saxler combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

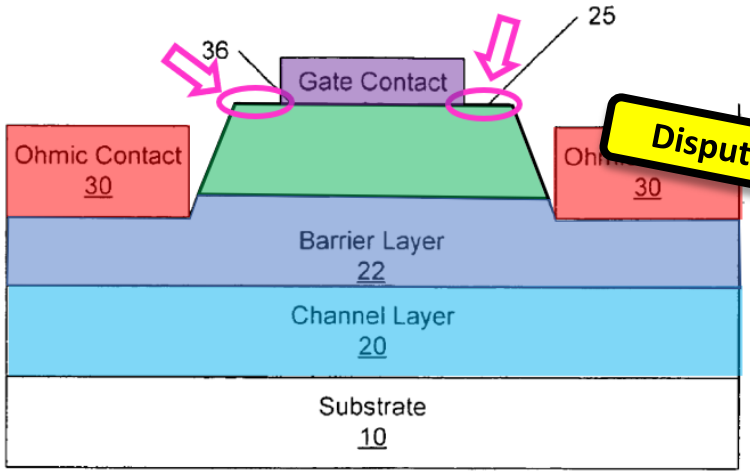
- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivation to modify Saxler

✓ Saxler’s modified Fig. 1A is in enhancement mode.

✓ A POSITA would have modified Fig. 1A based on Saxler’s teachings and for the benefits of enhancement mode.

See generally ’335 POR

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

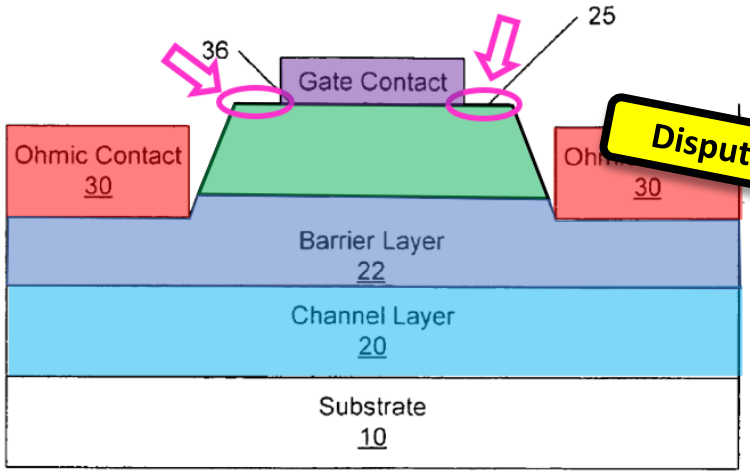
- ✓ Modified Fig. 1A would have been obvious and is in enhancement mode

The Petition shows:

1. The gate recess of Saxler’s Fig. 1A is optional
2. A POSITA would have removed Fig. 1A’s recess to achieve the benefits of enhancement mode

’335 Pet., 25-26, 35-36; ’335 Reply, 2-11.; ’335 Shealy, [090]-[091], [108]-[109], [122]; Ex. 2004, 31:1-20, 37:7-21.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

1. **The gate recess of Saxler’s Fig. 1A is optional**

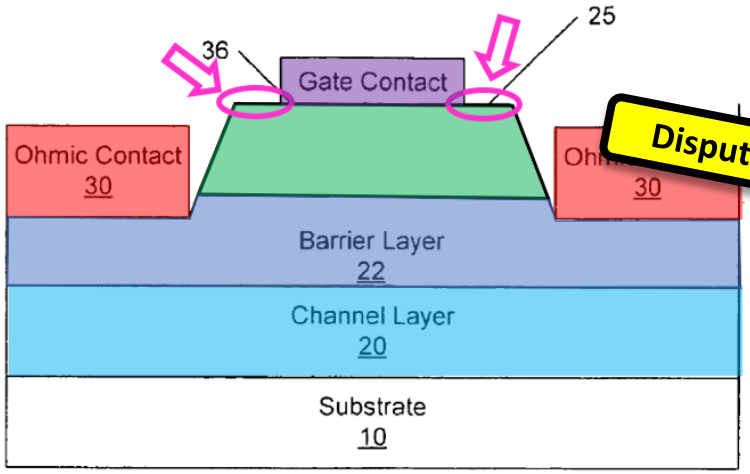
Saxler at [0052] unambiguously states the recess is optional in every figure (may or may not include)

[0052] Exemplary devices according to some embodiments of the present invention are schematically illustrated in **FIGS. 1A through 6**. Thus, while embodiments of the present invention are described herein with reference to a recessed gate structure or a non-recessed gate structure, other embodiments of the present invention may include or not include a gate recess. Accordingly, embodiments of the present invention should not be construed as limited to the particular exemplary embodiments described herein but may include any suitable structure having a cap layer and/or passivation layer as described herein.

B.F. Goodrich Co. v. Aircraft Braking Sys. Corp., 72 F.3d 1577, 1583 (Fed. Cir. 1998) (upholding single-reference obviousness for explicit suggestion to modify); *Boston Sci. Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009).

’335 Pet., 24-26, 31, 35-36, 40-41; ’335 Reply, 2-11.; ’335 Shealy, [090]-[091], [108]-[109], [122]; Ex. 2004, 31:1-20, 37:7-21.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

2. A POSITA would have removed Fig. 1A’s recess to achieve the benefits of enhancement mode

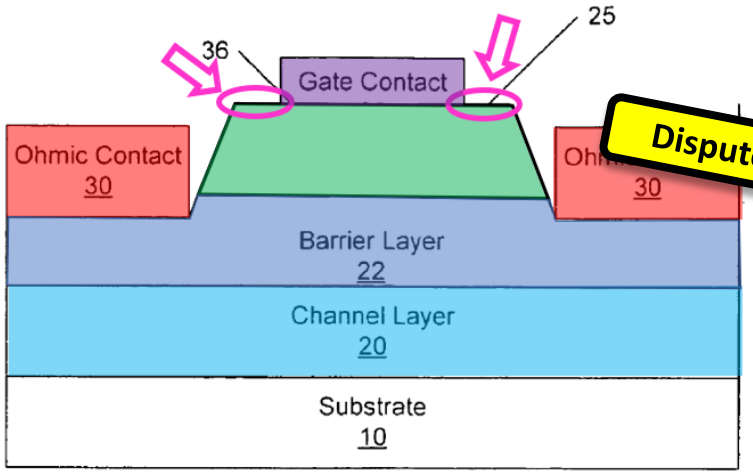
Further, with the recess, *Saxler*’s device is not enhancement mode (always off), and a POSITA would have been motivated to remove the recess to create an enhancement mode device and realize the benefits of a normally off device, which renders it suitable for high power applications. *Suh*, 1.

’335 Shealy, [103]

Petitioner’s expert Dr. Shealy confirms: Saxler’s device is enhancement mode when doped p-type without the recess

’335 Pet., 25-26, 35-36; ’335 Reply, 2-11.; ’335 Shealy, [090]-[091], [103], [108]-[109], [122]; Ex. 2004, 31:1-20, 37:7-21.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Patent Owner’s Four Arguments Fail (1A-1D)

Fig. 1A and Fig. 1B are not mutually exclusive embodiments as Patent Owner alleges.

1A
Patent Owner wrongly contends Saxler discloses distinct embodiments, one with a gate recess (Fig. 1A) and one without (Fig. 1B). POR, 16-22; Ex. 20065 [81]-[112].

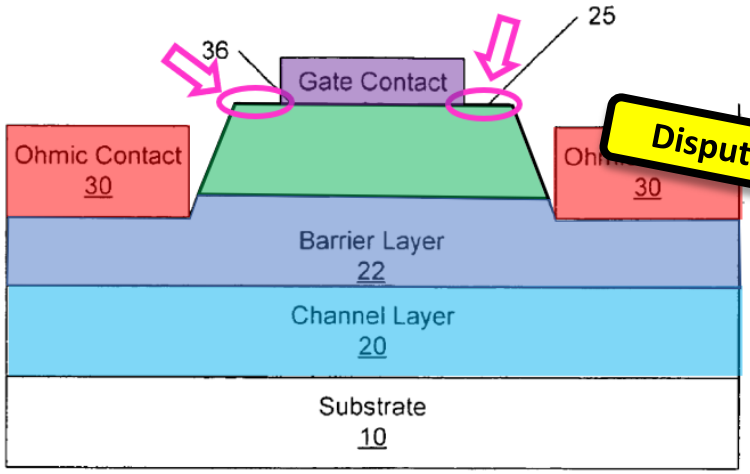
1B
Patent Owner incorrectly asserts Dr. Shealy engages in hindsight. POR, 21.

1C
Dr. Schubert employs a legally inaccurate, rigid understanding of obviousness (Ex. 2005, [102]) and incorrectly argues Saxler at [0052] does not mean what it says because it was “written by a patent attorney” (Ex. 2005, [101]).

1D
Patent Owner incorrectly alleges the Reply’s obviousness position on Saxler’s non-recessed embodiment contradicts the Petition. ’335 Sur-Reply, 9-11

’335 POR, 16-22; Reply, 2-11.; ’335 Shealy, [090]-[091], [103], [108]-[109], [122]; Ex. 2004, 31:1-20, 37:7-21; ’335 Sur-Reply, 9-11.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

The gate recess of Saxler’s Fig. 1A is optional

1A
Patent Owner wrongly contends Saxler discloses distinct embodiments, one with a gate recess (Fig. 1A) and one without (Fig. 1B). POR, 16-22; Ex. 20065 [81]-[112].

Saxler at [0052] unambiguously states the recess is optional in every figure

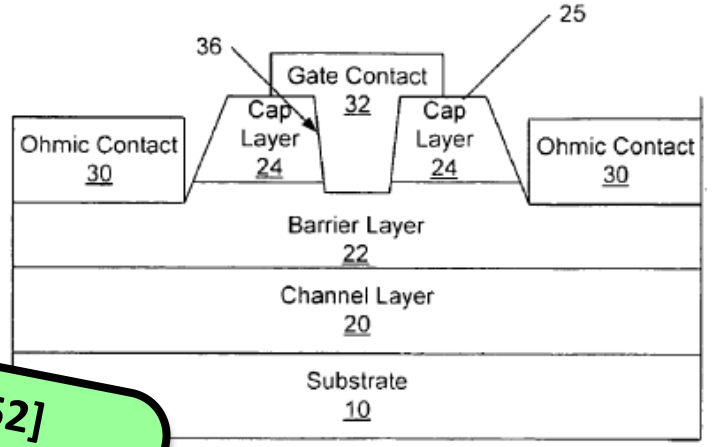


Figure 1A

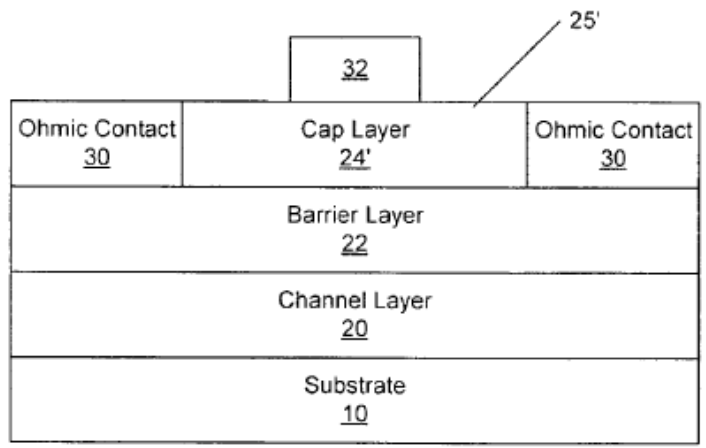
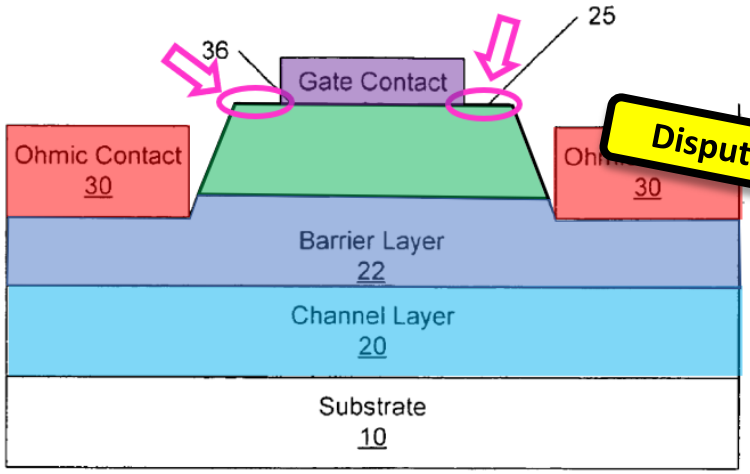


Figure 1B

’335 POR, 18-20; ’335 Reply, 3-4.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

1A
Patent Owner wrongly contends Saxler discloses distinct embodiments, one with a gate recess (Fig. 1A) and one without (Fig. 1B). POR, 16-22; Ex. 20065 [81]-[112].

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

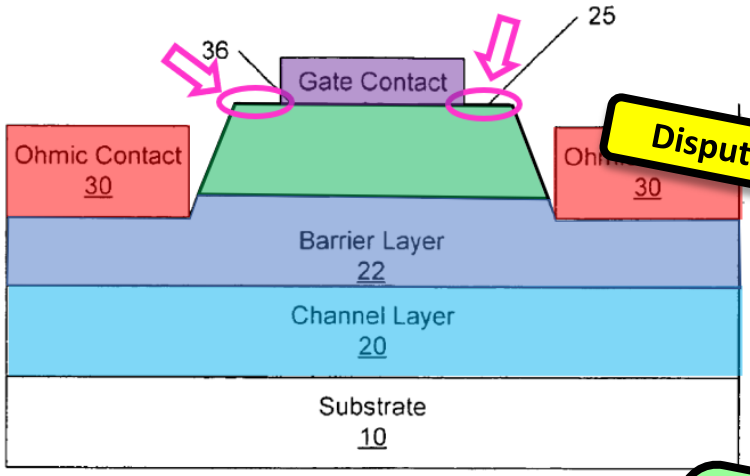
Disputed

The gate recess of Saxler’s Fig. 1A is optional

Patent Owner alleges *differences* between Fig. 1A and 1B	But Saxler discloses *similarities*
☒ Cap layer thickness	✓ The quoted range overlap (5-20 Å).
☒ Thickness of doped region.	✓ The quoted range overlaps (20-50 Å)
☒ Dopant concentration.	✓ Patent Owner cites example ***n-type*** dopant ranges. *Saxler*, [0012]. But ***p-type*** is used in enhancement mode. ***P-type*** ranges are the same for recessed and non-recessed. *Saxler*, [0013], [0071].
☒ Thickness of increased Al concentration	✓ The quoted range overlaps (30-100 Å)

’335 POR, 18-20; ’335 Reply, 3-4.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

The gate recess of Saxler’s Fig. 1A is optional

Dr. Shealy’s Testimony Was Not Hindsight

24	A. As I said before, I think you could take
25	all the embodiments and bring in which ones you
1	want, depending on what you're trying to accomplish.

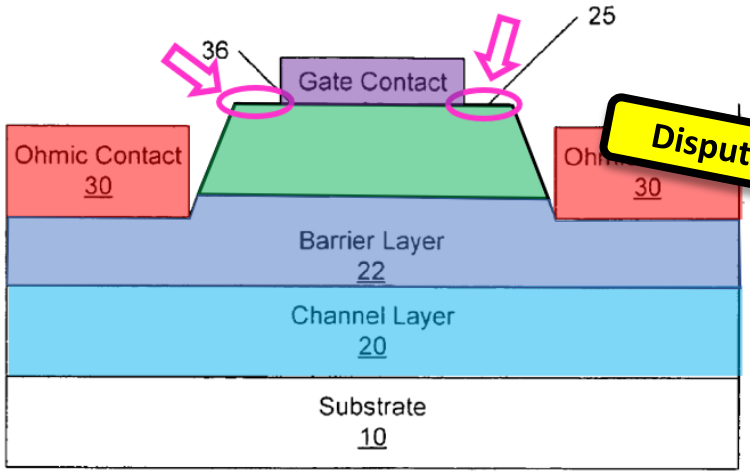
Shealy Transcript, Ex. 2004, 41:24-42:1.

1B
Patent Owner incorrectly asserts Dr. Shealy engages in hindsight. POR, 21.

- **First, *Saxler*** tells a POSITA to remove Figure 1A’s recess. Saxler, [0052]. *B.F. Goodrich Co. v. Aircraft Braking Sys. Corp.*, 72 F.3d 1577, 1583 (Fed. Cir. 1998) (upholding single-reference obviousness for explicit suggestion to modify).
- **Second, *“take all the embodiments”:*** prior art must be considered for “everything it teaches.” *EXP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985)
- **Third, *“depending on what you’re trying to accomplish”***: POSITA may modify with reason to do so. *KSR Int’l v. Teleflex, Inc.*, 550 U.S. 398, 401-402 (2007). A POSITA would have removed *Saxler*’s recess to obtain benefits of enhancement mode. **These benefits are not disputed.**

’335 POR, 21; ’335 Reply, 4-5; Ex. 2004, 41:24-42:1.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

The gate recess of Saxler’s Fig. 1A is optional

1C
Dr. Schubert employs a legally inaccurate, rigid understanding of obviousness (Ex. 2005, [102]) and incorrectly argues Saxler at [0052] does not mean what it says because it was “written by a patent attorney” (Ex. 2005, [101]).

KSR Rejected Dr. Schubert’s Rigid Understanding of Obviousness as Limited to “What is Actually Disclosed”

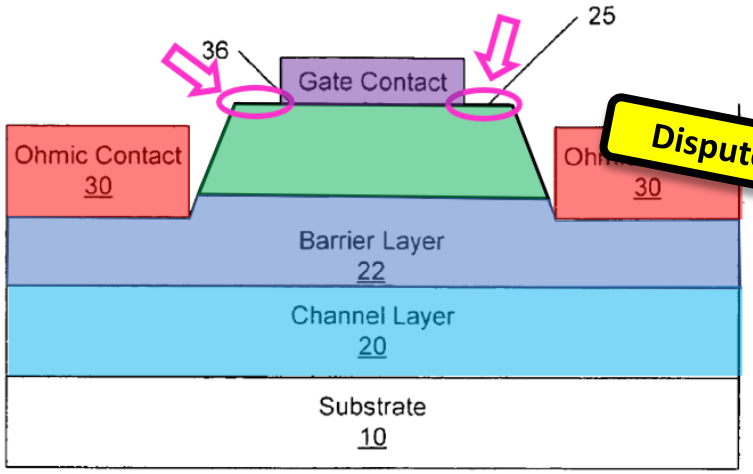
Although ¶[0052] of Saxler says “embodiments of the present invention should not be construed as limited to the particular exemplary embodiments,” it is only reasonable to consider that the disclosure of Saxler must be “limited” to what is actually disclosed. Importantly, ¶[0052] of Saxler does not mention anything about **combining** features of the recessed and the non-recessed embodiments as

Ex. 2005, [102]

KSR, 550 U.S. at 418 (obviousness accounts for “inferences and creative steps”), 422 (A POSITA “is also a person of ordinary creativity, not an automaton.”).

’335 POR, 17-18; ’335 Reply, 5-6; Ex. 2005, 102.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

The gate recess of Saxler’s Fig. 1A is optional

Dr. Schubert Cannot Ignore Saxler [0052] –
Saxler did “actually disclose[]” the non-recessed Fig. 1A

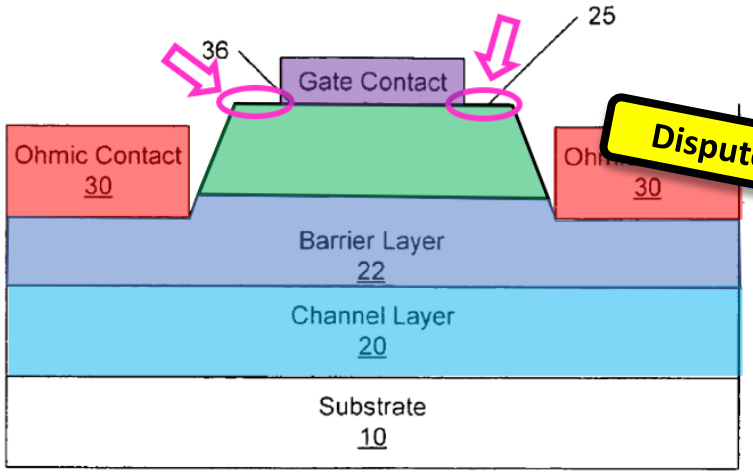
101. ¶52 of Saxler is nothing more than a “catch-all” paragraph written by a patent attorney, commonly used in many patent applications, from my understanding. ¶52 of Saxler does not provide support to POSA to modify (“mix and match”) the transistors of Saxler to produce the particular structure as claimed. **Ex. 2005, [101]**

[0052] Exemplary devices according to some embodiments of the present invention are schematically illustrated in **FIGS. 1A through 6**. Thus, while embodiments of the present invention are described herein with reference to a recessed gate structure or a non-recessed gate structure, other embodiments of the present invention may include or not include a gate recess. Accordingly, embodiments of the present invention should not be construed as limited to the particular exemplary embodiments described herein but may include any suitable structure having a cap layer and/or passivation layer as described herein.

1C
Dr. Schubert employs a legally inaccurate, rigid understanding of obviousness (Ex. 2005, [102]) **and incorrectly argues Saxler at [0052] does not mean what it says because it was “written by a patent attorney” (Ex. 2005, [101]).**

’335 POR, 17-18; ’335 Reply, 5-6; Ex. 2005, 102.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

The gate recess of Saxler’s Fig. 1A is optional

The Petition Reasoned Saxler’s Non-Recessed Embodiments Are At Least Obvious Just Like the Reply

1D
Patent Owner incorrectly alleges the Reply’s position on Saxler’s non-recessed embodiment was obvious contradicts the Petition. ’335 Sur-Reply, 9-11

Saxler discloses “*a* p-type gate material … having side surfaces” as recited in claim 1. Although it depicts its gate recess may separate its cap layer into two portions in some embodiments, the recess in *Saxler*’s cap layer 24 need not be present and need not extend through the cap layer 24 and into the barrier layer. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; Shealy, [122]. *Saxler* thus discloses or at least renders obvious a single p-type gate material having two side surfaces that extend horizontally towards the source and drain. Shealy, [123].

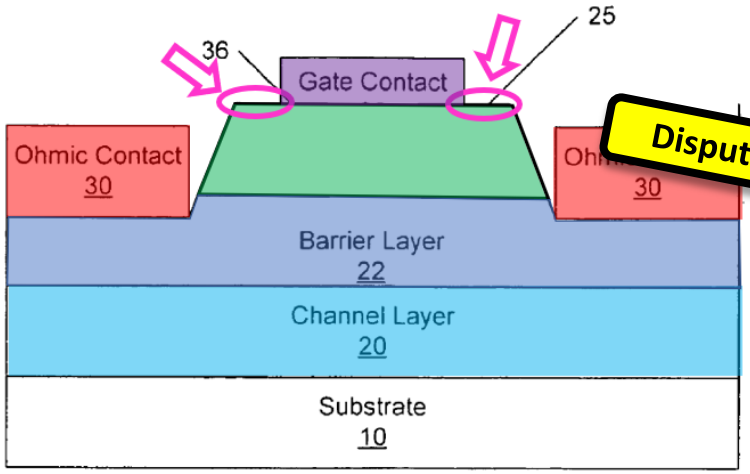
The petition states Saxler “discloses or at least renders obvious” modified Figure 1A. ” ’335 Pet., 40-41.

However, *Saxler* repeatedly discloses that its gate recess is optional. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88. While its figures do not explicitly depict a ***stacked*** gate structure having a gate contact and cap layer isolated from the source and drain contacts and without a gate recess, this disclosure would at a minimum render the claimed structure obvious. Shealy, [101]. To the extent Patent Owner disagrees with *Saxler*’s

The petition states Saxler’s disclosure of a non-recessed embodiment “render[s] the claimed structure obvious.” ’335 Pet., 31.

’335 Pet., 31, 40-41.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

The gate recess of Saxler’s Fig. 1A is optional

The Petition Reasoned a POSITA Would Have Been Motivated to Remove Saxler’s Recess to Achieve the Benefits of Enhancement Mode Just Like the Reply

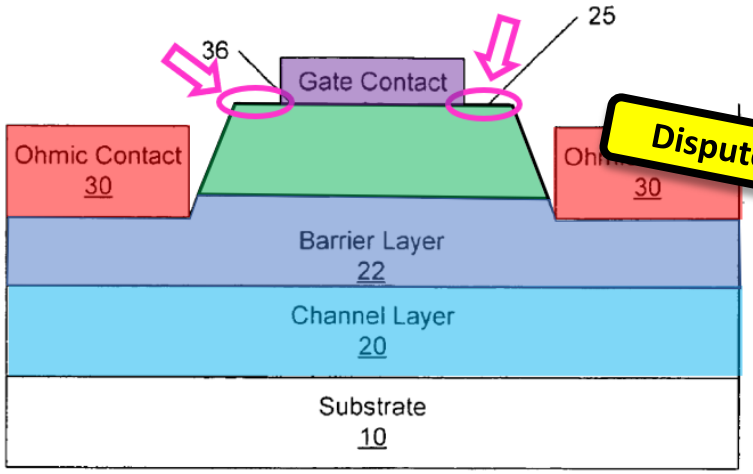
> A POSITA would have further been motivated to remove the gate recess to turn *Saxler*’s device into an enhancement mode device, thus realizing the benefits of reduced power consumption and suitability for high power applications. *Suh*, 1; Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [103].
>
> **’335 Pet., 33**

The known benefits of enhancement mode are not disputed.

1D
Patent Owner incorrectly alleges the Reply’s position on Saxler’s non-recessed embodiment was obvious contradicts the Petition. ’335 Sur-Reply, 9-11

’335 Pet., 33

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Patent Owner’s Four Arguments Fail (1A-1D)

Fig. 1A and Fig. 1B are not mutually exclusive embodiments as Patent Owner alleges.

All of Patent Owner’s Arguments Fail

1A
Patent Owner wrongly contends Saxler discloses distinct embodiments, one with a gate recess (Fig. 1A) and one without (Fig. 1B). POR, 16-22; Ex. 20065 [81]-[112]

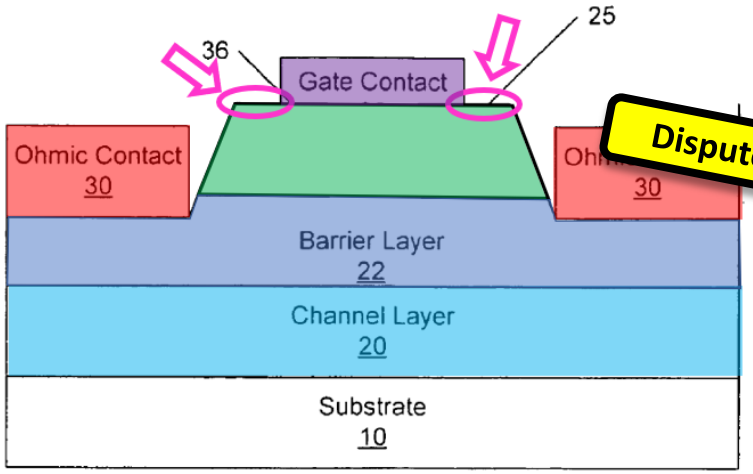
1B
Patent Owner incorrectly asserts Dr. Shealy engages in hindsight. POR, 21.

Dr. Schubert employs a legally inaccurate, rigid understanding of obviousness (Ex. 2005, [102]) and incorrectly argues Saxler at [0052] does not mean what it says because it was “written by a patent attorney” (Ex. 2005, [101]).

1D
Patent Owner incorrectly alleges the Reply’s obviousness position on Saxler’s non-recessed embodiment contradicts the Petition. ’335 Sur-Reply, 9-11

’335 Pet., 25-26, 35-36; ’335 Reply, 2-11.; ’335 Shealy, [090]-[091], [103] [108]-[109], [122]; Ex. 2004, 31:1-20, 37:7-21.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Patent Owner’s Arguments That Saxler is Not in Enhancement Mode Fail (2A-2C)

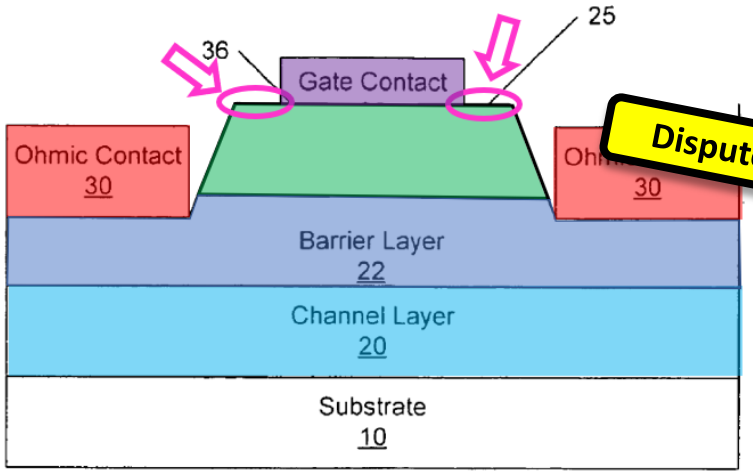
2A
The POR incorrectly contends modified Figure 1A would be inoperable in enhancement mode because its cap layer purportedly extends from source to drain

2B
The POR wrongly argues modified Figure 1A would be inoperable in enhancement mode because “access regions” remain depleted “even for positive gate voltage.”

2C
Patent Owner misreads Saxler to argue its p-type dopants function as “deep level dopants” and thus do not “act as acceptors.”

’335 POR, 24-25; ’335 Reply, 11.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

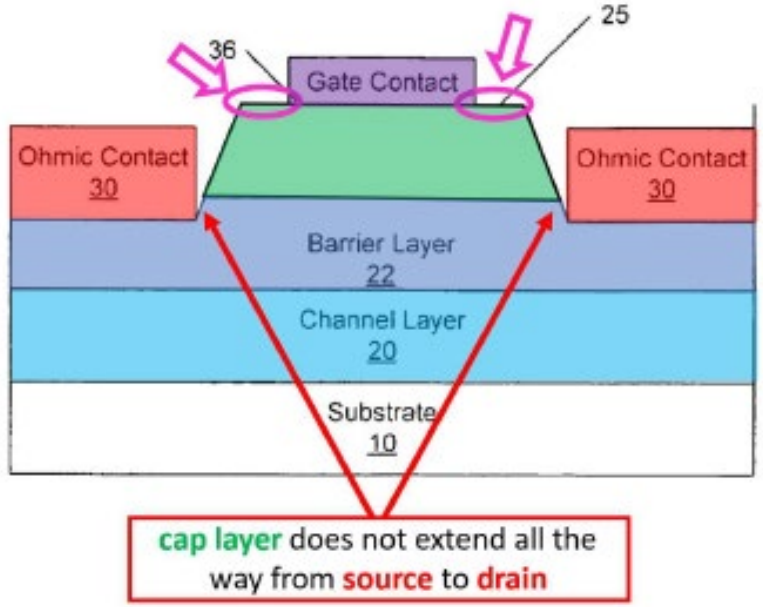
Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Saxler’s device is in enhancement mode when doped p-type without the recess

2A
The POR incorrectly contends modified Figure 1A would be inoperable in enhancement mode because its cap layer purportedly extends from source to drain

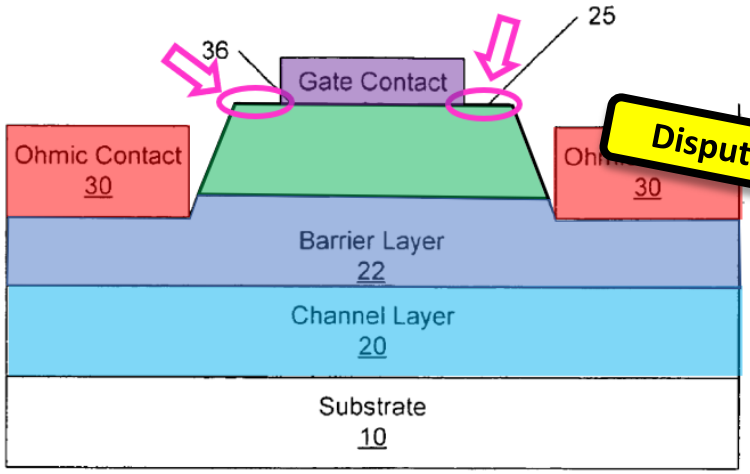
The Board noted that the cap layer *does not* extend from source to drain as Patent Owner alleged to argue the device non-operational. ’335 ID, 31.



Patent Owner is wrong. The cap layer does not extend from source to drain in modified Figure 1A. The barrier separates the cap layer from source and drain.

’335 POR, 22-26; ’335 Reply, 6-7.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



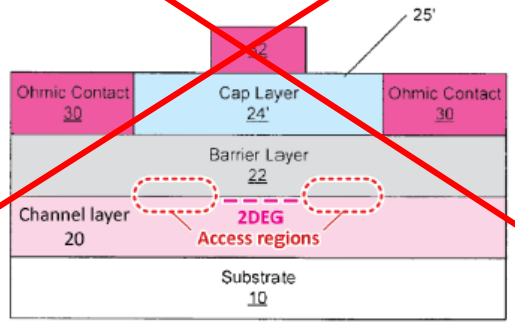
Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Saxler’s device is in enhancement mode when doped p-type without the recess

As acknowledged by Dr. Shealy, Saxler’s cap layer 34 in Fig. 1B extends completely from Source to Drain, including the access regions that are located between the S&G (source and gate) electrodes, as well as between the G&D (gate & drain) electrodes. EX2005 ¶117.



’335 POR, 22-26

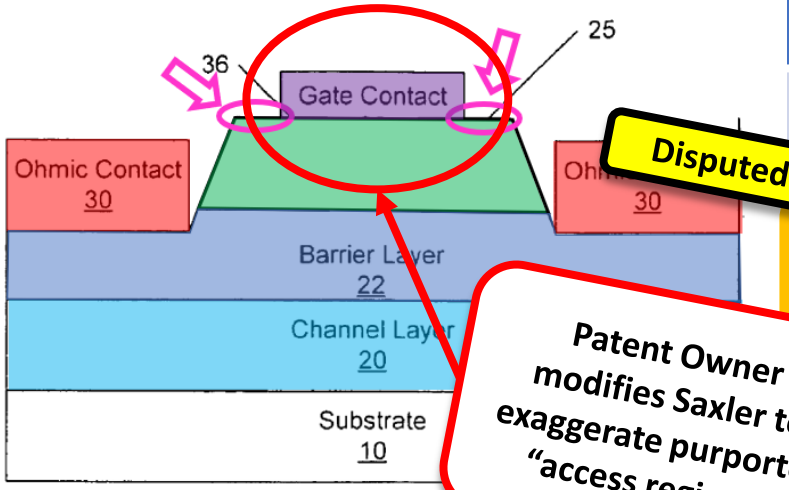
2A
The POR incorrectly contends modified Figure 1A would be inoperable in enhancement mode because its cap layer purportedly extends from source to drain

Patent Owner irrelevantly analyzes Figure 1B, where the cap extends from source to drain. This misunderstands the Petition, which shows removing the recess of Figure 1A would have been obvious.

’335 POR, 22-26; ’335 Reply, 7-8.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience



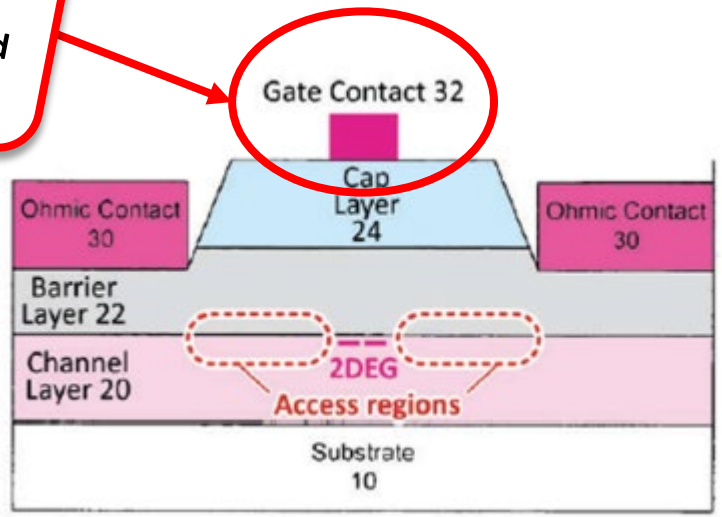
Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

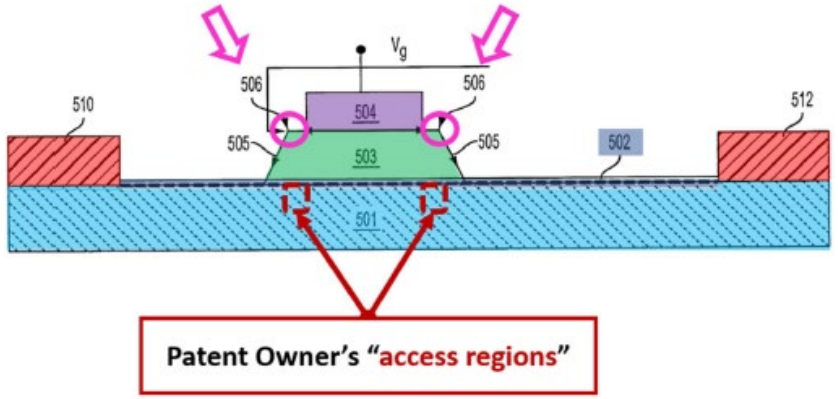
Disputed

Saxler’s device is in enhancement mode when doped p-type without the recess

Patent Owner modifies Saxler to exaggerate purported “access regions.”



Patent Owner’s theory of Saxler



Patent Owner’s theory applied to the ’335 patent

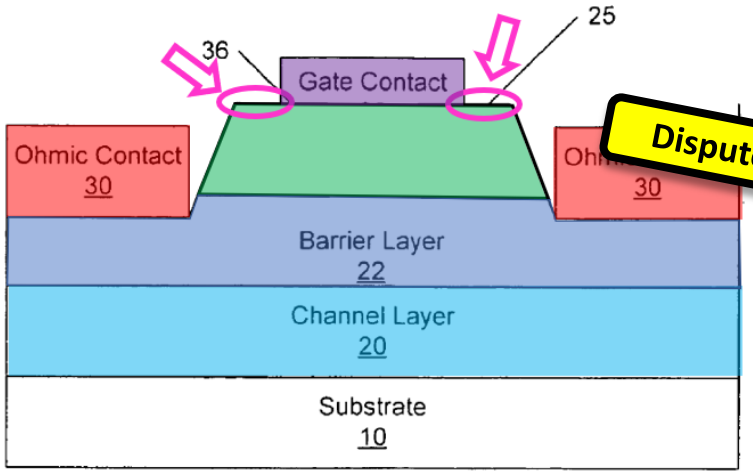
2B
The POR wrongly argues modified Figure 1A would be inoperable in enhancement mode because “access regions” remain depleted “even for positive gate voltage.”

’335 POR, 25-26; ’335 Reply, 7-9

Patent Owner’s “access region” theory contradicts the patent, which has the same geometry.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience



Saxler, Fig. 1A (modified).

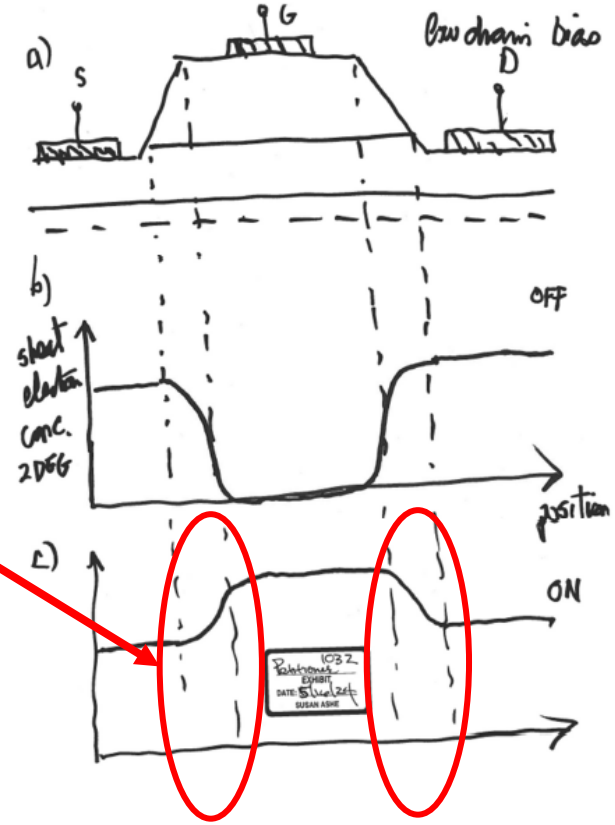
Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Saxler’s device is in enhancement mode when doped p-type without the recess

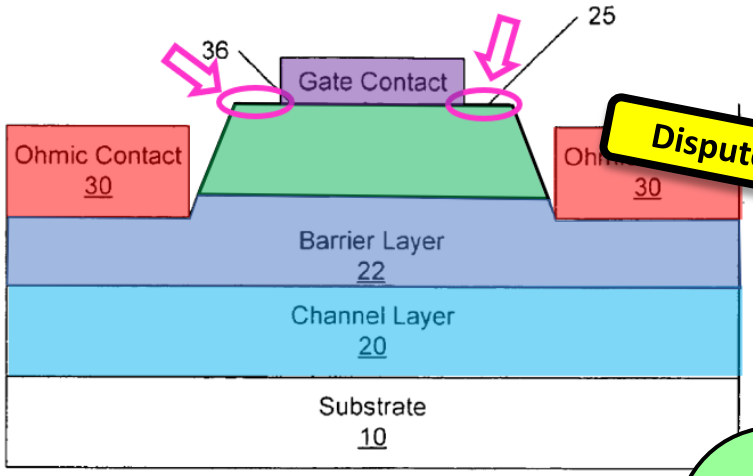
2B
The POR wrongly argues modified Figure 1A would be inoperable in enhancement mode because “access regions” remain depleted “even for positive gate voltage.”

Patent Owner ignored Dr. Shealy’s explanation describing how Figure 1A is in enhancement mode, which refutes Patent Owner’s depleted “access region” theory—these regions are not depleted when voltage is applied.



’335 POR, 25-26; ’335 Reply, 9-11; Ex. 1032; Ex. 2004, 104:9-105:19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Saxler’s device is in enhancement mode when doped p-type without the recess

2C
Patent Owner misreads Saxler to argue its p-type dopants function as “deep level dopants” and thus do not “act as acceptors.”

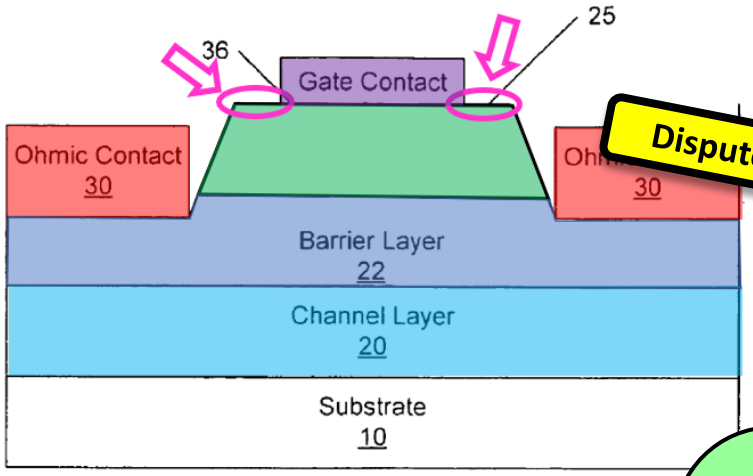
Patent Owner quotes Saxler at [0049] out of context to incorrectly conclude Saxler’s p-type dopants “do not act as [electron] acceptors” and cannot deplete the 2DEG, so Saxler’s “cap layer cannot function in enhancement mode.”

Paragraph [0049] explains the purpose of p-type doping of region 40 at the top of the cap layer: “the dopants at the outer surface of the device may segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations.” *Id.* ¶[0049] Indeed, Saxler points out that the dopants “segregate to dislocations,” rather than depleting the 2DEG. *Id.* Paragraph [0049] further explains that “a shallow dopant in the bulk crystal may have characteristics of a deep level when at a dislocation” which is “especially true in the case of p-type [...] dopants.” *Id.* Thus, the shallow acceptors of Saxler do not even act as acceptors once they “segregate to dislocations.” EX2005 ¶128. If the shallow dopants do not act as acceptors, the cap layer cannot function in enhancement mode. *Id.* That is, the dopants that Dr. Shealy envisions as regular, shallow p-type dopants, are in fact characteristics of “deep level” dopants. *Id.*

’335 POR, 24-25

’335 POR, 24-25; ’335 Reply, 11.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Saxler’s device is in enhancement mode when doped p-type without the recess

2C
Patent Owner misreads Saxler to argue its p-type dopants function as “deep level dopants” and thus do not “act as acceptors.”

Saxler at [0049] refers to p-type dopants at crystal “*dislocations*.” There, they act as “deep level dopants” to further reduce leakage. But p-type dopants act as shallow dopants “in the bulk crystal” and can deplete the 2DEG to function in enhancement mode.

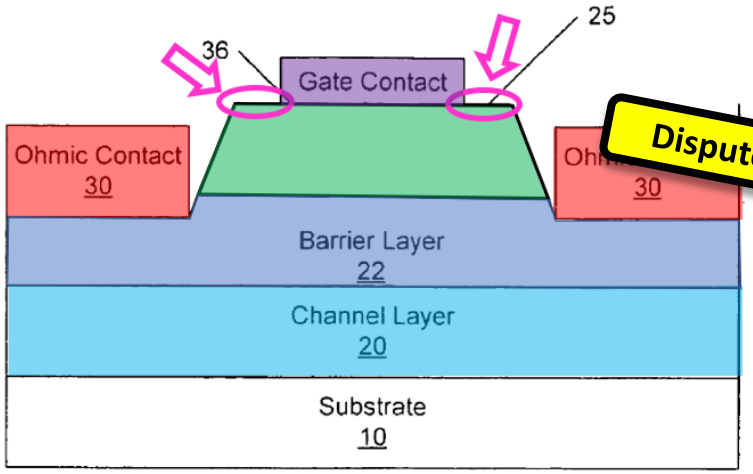
have characteristics of a deep level when at a dislocation.” *Id.* But *Saxler* never says p-type dopants do not function as shallow dopants at *other* locations. *Id. Saxler* specifically clarifies its “references to p-type ... dopants refer[] to the characteristics of the dopants *in the bulk crystal rather than when at a dislocation.*” *Id.* When *Saxler* describes p-typed doping in a sub-region or when doped throughout its cap layer (e.g., *Saxler*, [0013], [0069] [0071]), it describes shallow dopants in the bulk crystal, capable of depleting the 2DEG when the recess is removed. Petition, 25, 35-36; Shealy, [090], [108]

Patent Owner’s Sur-Reply does not refute Saxler’s clear disclosure that its p-type dopants act as p-type in the bulk crystal

’335 Reply, 11

’335 POR, 24-25; ’335 Reply, 11.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Patent Owner’s Arguments That Saxler is Not in Enhancement Mode Fail (2A-2C)

All of Patent Owner’s Arguments Fail

2A
~~The POR incorrectly contends modified Figure 1A would be inoperable in enhancement mode because its cap layer purportedly extends from source to drain~~

2B
~~The POR wrongly argues modified Figure 1A would be inoperable in enhancement mode because “access regions” remain depleted “even for positive gate voltage.”~~

2C
~~Patent Owner misreads Saxler to argue its p-type dopants function as “deep level dopants” and thus do not “act as acceptors.”~~

’335 POR, 24-25; ’335 Reply, 11.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience

Patent Owner only disputes the Saxler combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivation to modify Saxler

✓ Saxler’s modified Fig. 1A is in enhancement mode.

✓ A POSITA would have modified Fig. 1A based on Saxler’s teachings and for the benefits of enhancement mode.

All of Patent Owner’s Arguments Fail

See generally ’335 POR

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Patent Owner only disputes the Saxler combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivation to modify Saxler

See generally ’335 POR

’335 Patent Ground 1: Saxler renders obvious claims 1-7

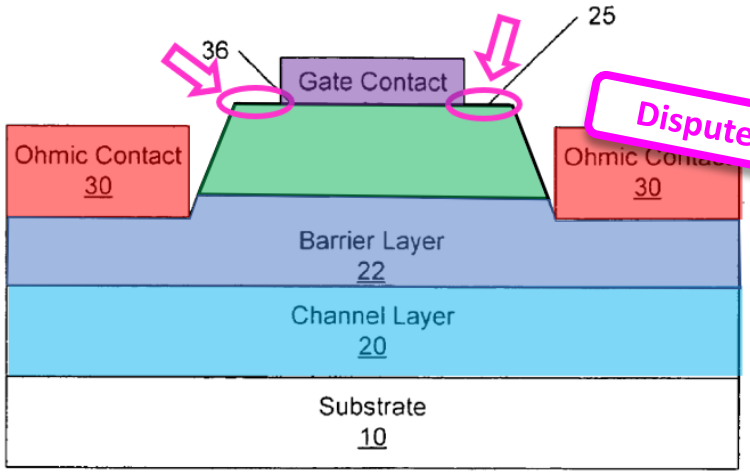
Patent Owner only disputes the Saxler combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivation to modify Saxler

✓ Saxler’s drawings disclose ledges with substantially equal widths

See generally ’335 POR

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

Disputed

✓ Saxler’s drawings disclose ledges with “substantially equal widths”

1. **Saxler’s Figure 1A with a recess and as modified without a recess plainly show “horizontal ledges” with “substantially equal widths” [*undisputed*]**
2. **“substantially equal” is not a precise term, so *Hockerson* does not apply.**

Patent Owner does not dispute that Saxler shows substantially equal ledges, only that the claims cannot be obvious over *Saxler*’s drawings under legal precedent (*Hockerson*)

At Institution, the Board reasoned “’substantially’ is a common approximation or term of degree in patent claims,” which Patent Owner did not dispute, so *Hockerson* does not apply, and drawings can disclose this limitation. ’335 ID, 38-39.

’335 Pet., 49-51.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

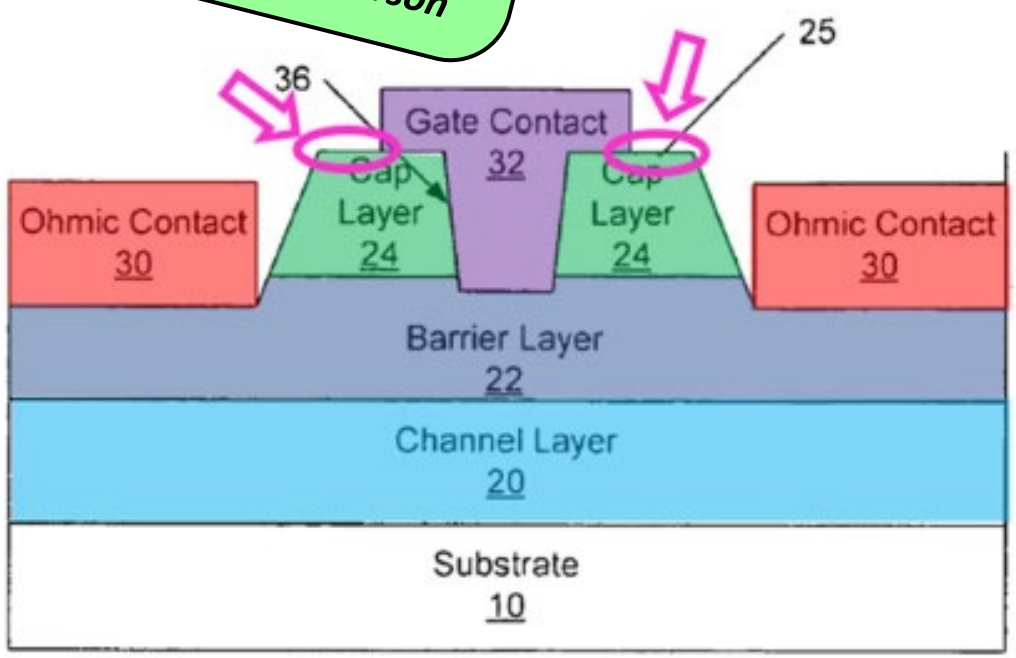
Innoscience

Patent Owner does not dispute that Saxler shows substantially equal ledges, only whether the claims are obvious over Saxler’s drawings under *Hockerson*

Disputed

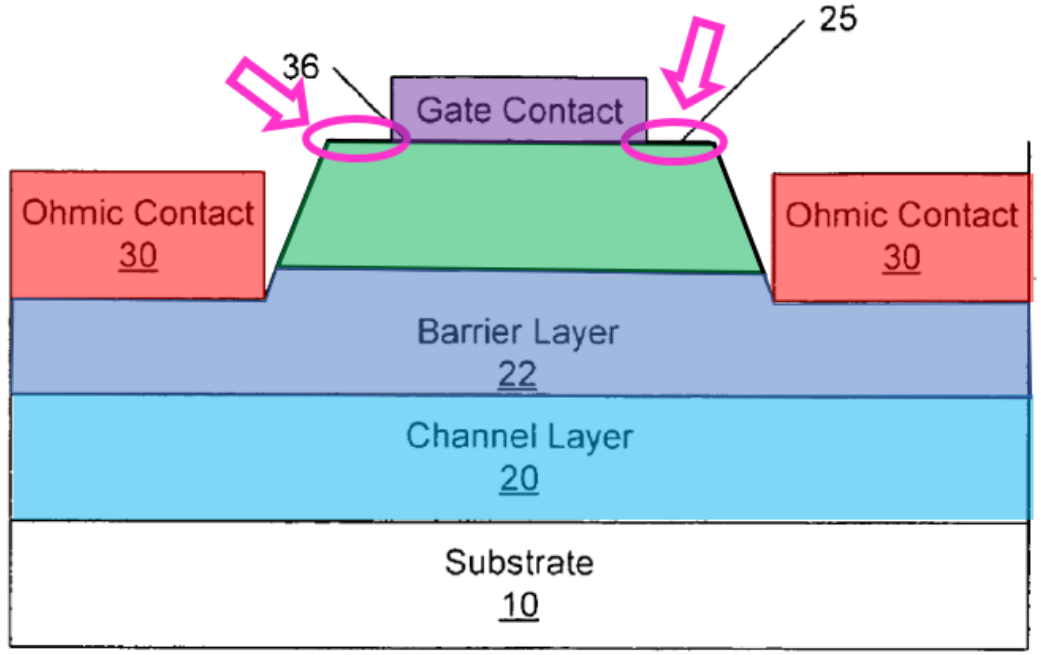
Saxler	Limitation
✓	**[1f]** wherein the **p-type gate material** comprises a pair of **horizontal ledges** that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of **horizontal ledges** having **substantially equal widths** from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

Saxler’s Figure 1A with a recess and as modified without a recess plainly show “horizontal ledges” with “substantially equal widths”



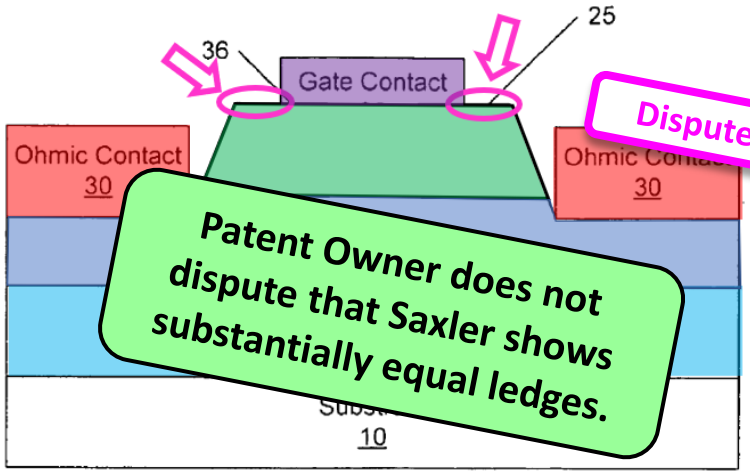
’335 Pet., 49-51.

Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

Patent Owner’s arguments fail

“substantially equal” is not a precise term, so *Hockerson* does not apply.

A
Patent Owner incorrectly argues Saxler’s figures cannot disclose “substantially equal widths” under *Hockerson*

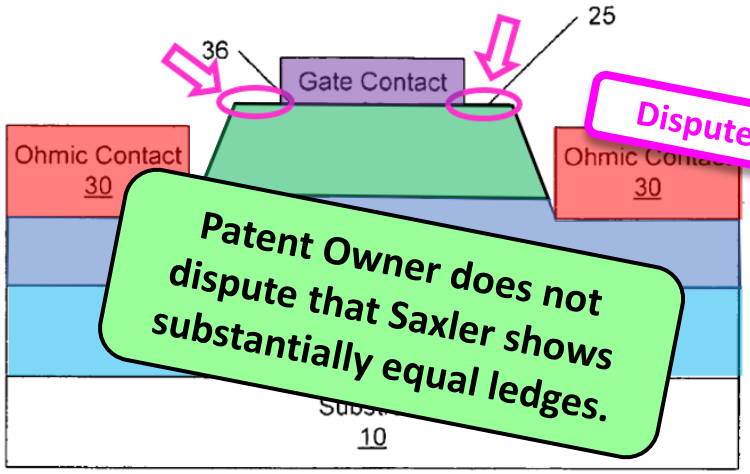
B
Patent Owner misunderstands *Ex Parte Bjorn* to inaccurately contend “substantially equal” cannot be disclosed by figures

C
Patent Owner relies on Saxler’s optional “offset” between the gate and source/drain to inaccurately contend Saxler does not disclose “substantially equal” ledges”

’335 Pet., 49-51; ’335 POR, 29-38; ’335 Reply, 14-19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

“substantially equal” is not a precise term, so *Hockerson* does not apply.

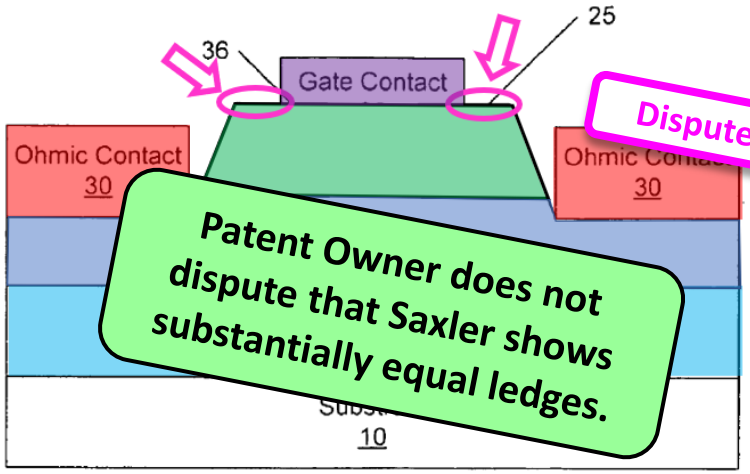
***Hockerson* holds that drawings not to scale cannot disclose precise proportions or dimensions. *Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000).**

A
Patent Owner incorrectly argues Saxler’s figures cannot disclose “substantially equal widths” under *Hockerson*

At Institution, the Board reasoned “‘substantially’ is a common approximation or term of degree in patent claims,” which Patent Owner did not dispute, so *Hockerson* does not apply, and drawings can disclose this limitation. ’335 ID, 38-39.

’335 Pet., 49-51; ’335 POR, 32; ’335 Reply, 15.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Patent Owner does not dispute that Saxler shows substantially equal ledges.

Saxler	Limitation
✓ Disputed	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

“substantially equal” is not a precise term, so *Hockerson* does not apply.

Hockerson does not extend to relative proportions, terms of degree, and approximation. Paper No. 8 at 2. Petitioners showed “substantially equal” is an approximation or term of degree, which the POR does not dispute. *Id.* at 4 (citing *Seattle Box Co., Inc. v. Indus. Crating & Packing, Inc.*, 731 F.2d 818, 826 (Fed. Cir. 1984); M.P.E.P. § 2173.05(b)(II)(D)); POR, 31-35 (no discussion of *Seattle Box* or M.P.E.P.). *Hockerson* does not apply.

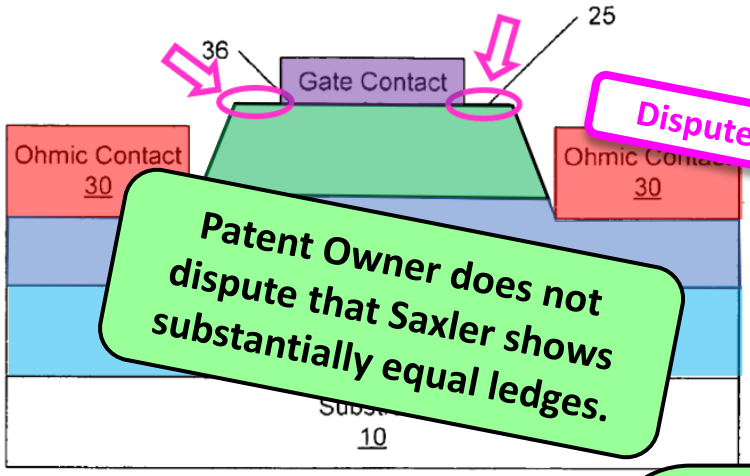
’335 Reply, 15

A
Patent Owner incorrectly argues Saxler’s figures cannot disclose “substantially equal widths” under *Hockerson*

At Institution, the Board reasoned that “‘substantially’ is a common approximation or term of degree in patent claims,” which Patent Owner did not dispute, so *Hockerson* does not apply, and drawings can disclose this limitation. ’335 ID, 38-39.

’335 Pet., 49-51; ’335 POR, 29-36; ’335 Reply, 15-19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Disputed

Patent Owner does not dispute that Saxler shows substantially equal ledges.

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

“substantially equal” is not a precise term, so *Hockerson* does not apply.

B
Patent Owner misunderstands *Ex Parte Bjorn* to inaccurately contend “substantially equal” cannot be disclosed by figures

Patent Owner misunderstands *Ex Parte Bjorn*’s discussion of “less than or substantially equal” to contend it focuses on the open ended “less than ... equal” requirement

In *Ex parte Bjorn*, the Board first addressed the limitation “*less than or substantially equal*” of independent claim 1 that was directed to a bone implant. *Id.* at *10 (emphasis added). The Board found that “claim 1 merely requires the abutment to have an exterior surface diameter that is ‘less than or substantially equal to the maximum thread diameter of the male screw section of the bone fixture.’ No particular dimensions or proportions are claimed.” *Id.* The limitation of “*less than or substantially equal*” was thus found to be open-ended. *Id.* (emphasis added).

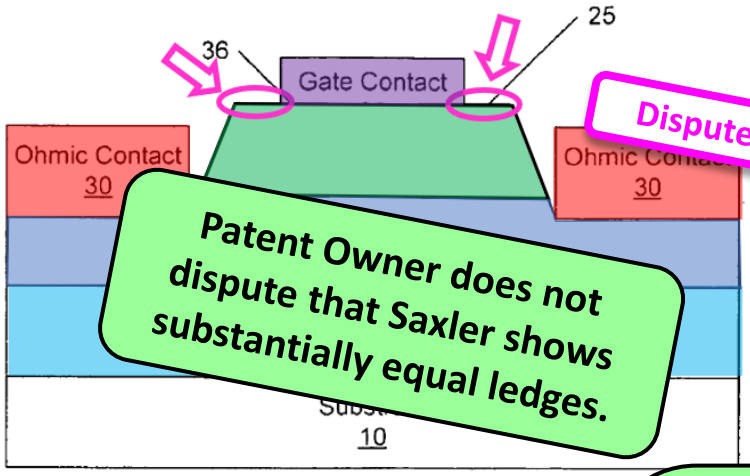
Ex Parte Bjorn does not support Patent Owner

’335 POR, 32

’335 Pet., 49-51; ’335 POR, 29-36; ’335 Reply, 15-19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience



Saxler, Fig. 1A (modified).

Patent Owner does not dispute that Saxler shows substantially equal ledges.

Saxler	Limitation
✓ Disputed	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

“substantially equal” is not a precise term, so *Hockerson* does not apply.

B
Patent Owner misunderstands *Ex Parte Bjorn* to inaccurately contend “substantially equal” cannot be disclosed by figures

Ex Parte Bjorn **repeatedly found prior art drawings not to scale showed screws with “substantially equal” diameters without mention of the *“less than ... equal”* requirement.**

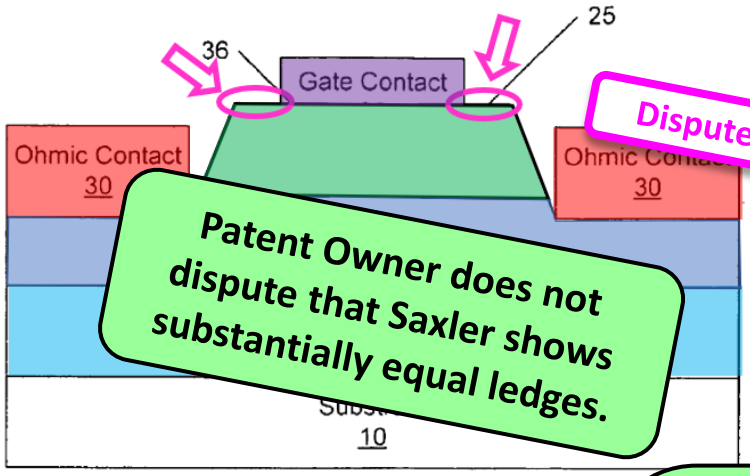
Parte Bjorn, 2019 WL 6173305 at *1. *Ex Parte Bjorn* first found *Hockerson* did not apply because “no particular dimensions” were claimed. *Id.* at *10-11. The Board then found numerous prior art figures not to scale from different references disclosed “substantially equal” diameters. *E.g.*, *id.* at *11 (e.g., noting certain figures show “diameters *substantially equal*” and still others “clearly show ... substantially equal” diameters), 17 (certain figure “clearly illustrates ... substantially equal” diameters). Here, the Board did not find the prior art showed “less than ... equal” diameters—the prior art showed “substantially equal” diameters. *Id.*

Ex Parte Bjorn supports Petitioner

’335 Reply, 16

’335 Pet., 49-51; ’335 POR, 29-36; ’335 Reply, 15-19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Disputed

Patent Owner does not dispute that Saxler shows substantially equal ledges.

Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

“substantially equal” is not a precise term, so *Hockerson* does not apply.

B

Patent Owner misunderstands *Ex Parte Bjorn* to inaccurately contend “substantially equal” cannot be disclosed by figures

***Ex Parte Bjorn* repeatedly found prior art drawings not to scale showed screws with “substantially equal” diameters without mention of the *“less than ... equal”* requirement.**

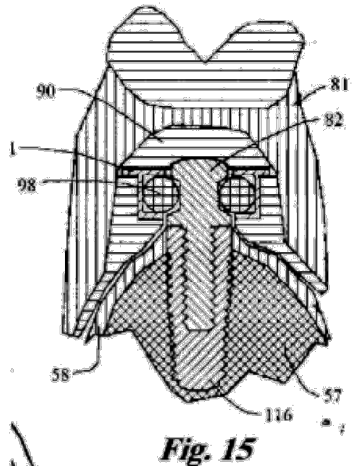


Fig. 15

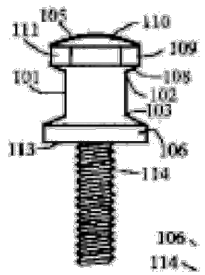


Fig. 19

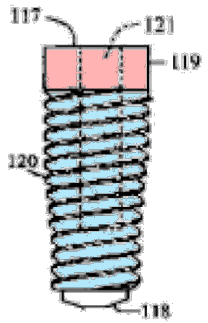


Fig. 22

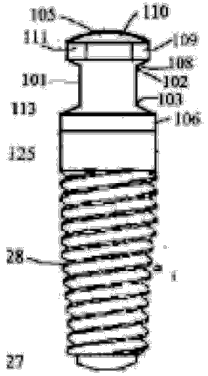
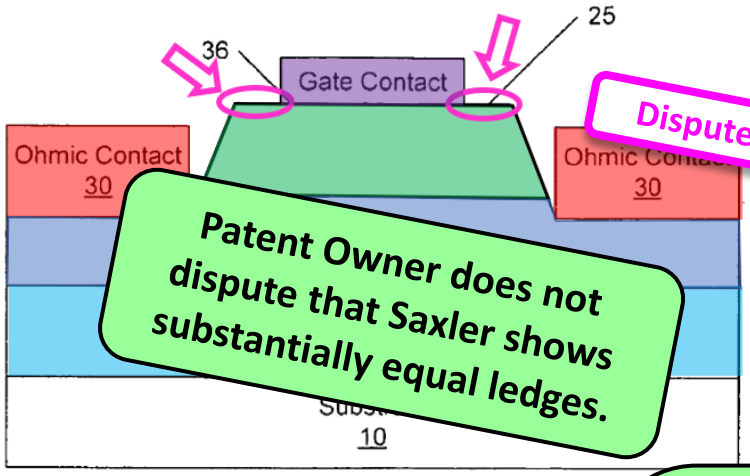


Fig. 29

’335 Pet., 49-51; ’335 POR, 29-36; ’335 Reply, 15-19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience



Saxler, Fig. 1A (modified).

Disputed

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

Patent Owner does not dispute that Saxler shows substantially equal ledges.

“substantially equal” is not a precise term, so *Hockerson* does not apply.

B
Patent Owner misunderstands *Ex Parte Bjorn* to inaccurately contend “substantially equal” cannot be disclosed by figures

Patent Owner focuses on analysis of a figure showing a *larger* diameter screw, where *Hockerson* applied. POR, 32; *Ex Parte Bjorn* at *17. But when the prior art showed “substantially equal” diameters, the Board found the limitation obvious.

The issue is whether Lazzara's abutment portion, which is ***larger*** in diameter than the maximum diameter of the bone fixture screw threads in Figure 9, can be considered “substantially equal to the maximum thread diameter of the male screw section of the bone fixture” as recited in claim 8.

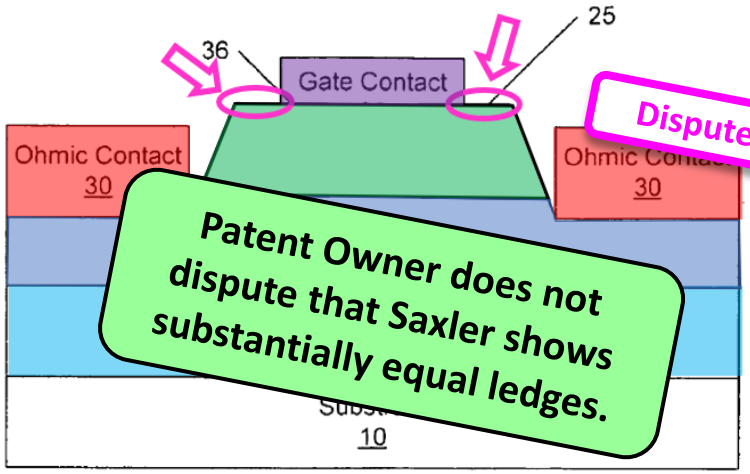
...

However, even if we determine what percentage or ratio of an oversized abutment diameter is permitted within the scope of the claim, the drawings cannot be relied on to disclose such precise or relative proportions. *See Hockerson-Halberstadt*, 222 F.3d at 956. The Specification indicates that “substantially equal” requires abutment diameter D1 to be very nearly equal to maximum thread diameter D2. **We cannot make that determination from Figure 9 of Lazzara, which illustrates the abutment diameter as larger than the maximum thread diameter**, but Figure 9 is not disclosed as being to scale or having any particular dimensions. Thus, we do not sustain the rejection of claim 8 or claim 10, which depends from claim 8.

Ex Parte Bjorn, 2019 WL 6173305 at *17.

’335 Pet., 49-51; ’335 POR, 29-36; ’335 Reply, 15-19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

Saxler’s optional “offset” between gate and source/drain does not contradict Figure 1A’s centered gate with ledges of substantially equal width

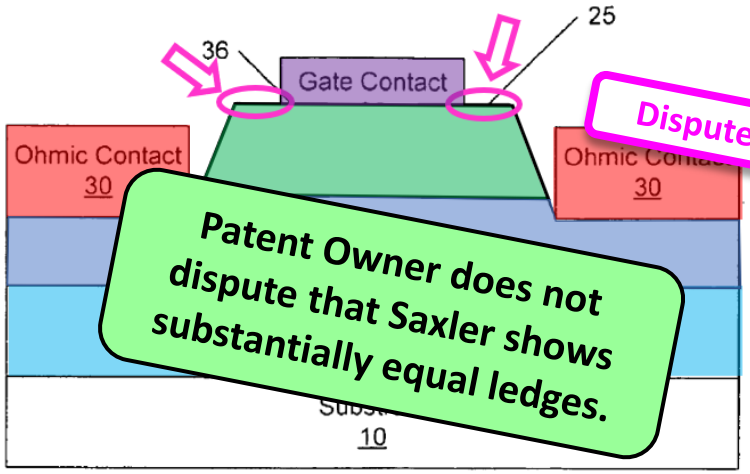
C
Patent Owner relies on Saxler’s optional “offset” between the gate and source/drain to inaccurately contend Saxler does not disclose “substantially equal” ledges”

The POR cites Saxler [0065], which uses non-limiting language (“the recess ***may*** be offset”) to describe an optional feature, which means other embodiments—like Figure 1A—would not have an offset. ’335 POR, 37-38**.**

Further, Saxler [0065] does not describe the relationship between the gate electrode and cap layer which defines the widths of the claimed ledges. It describes the spatial relationship between the gate and source/drain. Saxler, [0065].

’335 POR, 37-38; ’335 Reply, 18-19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

Patent Owner’s arguments fail

All of Patent Owner’s Arguments Fail

“…” is not a precise term, so *Hockerson* does not apply.

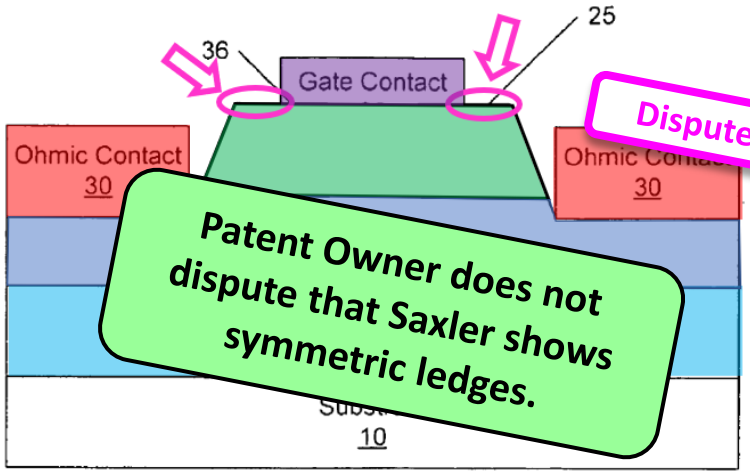
A
Patent Owner incorrectly argues Saxler’s figures cannot disclose “substantially equal widths” under *Hockerson*

B
Patent Owner misunderstands *Ex Parte Bjorn* to inaccurately contend “substantially equal” cannot be disclosed by figures

C
Patent Owner relies on Saxler’s optional “offset” between the gate and source/drain to inaccurately contend Saxler does not disclose “substantially equal” ledges”

’335 Pet., 49-50; ’335 POR, 29-38; ’335 Reply, 15-19.

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[7]** The enhancement mode GaN transistor according to claim 5, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

For the same reasons, *Hockerson* does not apply to claim 7’s “symmetric” ledges

All of Patent Owner’s Arguments Fail

At Institution, the Board invited the parties to brief whether *Hockerson* applies to claim 7’s “symmetric” ledges.

Petitioners Briefed this issue. But Patent Owner did not and thus forfeited any response. *See* ’335 POR; ’335 Sur-Reply.

Petitioners’ undisputed position shows the patent equates “substantially equal” and “symmetric.” *Hockerson* does not apply to “symmetric” for the same reasons as for “substantially equal.”

’335 ID, 38; ’335 Reply, 17-18.

ledges **506** on each side of the gate metal **504**. The pair of ledges **506** that extend past sidewalls of the gate metal **504** have equal or substantially equal widths, i.e., the respective ledges are symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material, which is due to the self-aligned manufacturing process.

’335 patent, 3:59-64.

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience

Patent Owner only disputes the Saxler combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivation to modify Saxler

✓ Saxler’s drawings disclose ledges with substantially equal widths

All of Patent Owner’s Arguments Fail

See generally ’335 POR

’335 Patent Ground 1: Saxler renders obvious claims 1-7

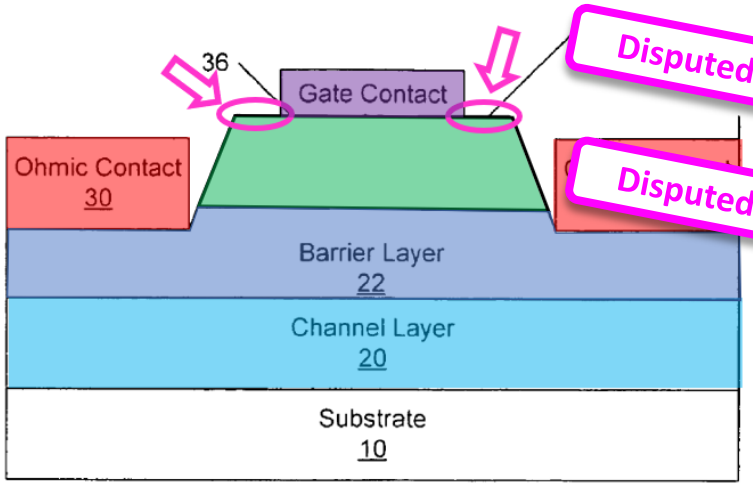
Patent Owner only disputes the Saxler combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivation to modify Saxler

✓ Saxler renders these limitations obvious because Saxler disclose the claimed structure and “self-aligned” is a product-by-process term

See generally ’335 POR

’335 Patent Ground 1: Saxler renders obvious claims 1-7



Saxler, Fig. 1A (modified).

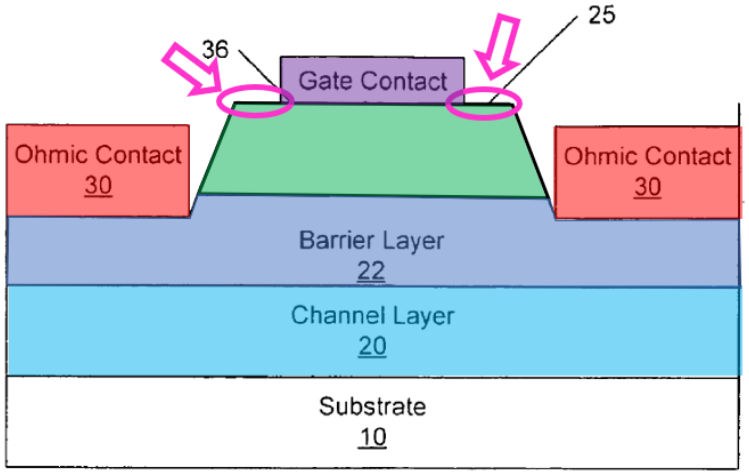
Saxler	Limitation
✓	**[2]** The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material **are** self-aligned.
✓	**[5f]** wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

✓ Saxler renders “**self-aligned**” **ledges** unpatentable because Saxler disclose the claimed structure and “**self-aligned**” is a product-by-process term.

’335 Pet., 51.

’335 Patent: Just Four Claim Features Disputed

Patent Owner only disputes the combinations of prior art shows *four* features of the ’335 patent



Saxler, Fig. 1A (modified).

Petitioner has shown the claims obvious over Saxler

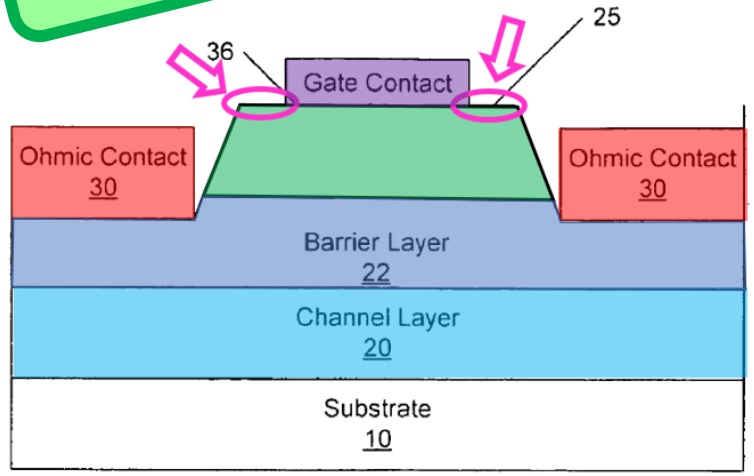
- ✓ [1p], [5p] **enhancement mode** (Saxler grounds)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned ledges** (all grounds)

All of Patent Owner’s Arguments Fail

’335 Patent Ground 1: Saxler renders obvious claims 1-7

Innoscience

Petitioner has shown the claims obvious over Saxler



Saxler, Fig. 1A (modified).

All of Patent Owner’s Arguments Fail

Saxler	Limitation
✓	**[1p]** An **enhancement-mode** GaN transistor, comprising:
✓	**[1a]** a **GaN layer**;
✓	**[1b]** a **barrier layer** disposed on the GaN layer with **a 2DEG region formed at an interface between the GaN layer and the barrier layer**;
✓	**[1c]** a **source contact** and a **drain contact** formed on the barrier layer;
✓	**[1d]** a **p-type gate material** formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the **source contact and drain contact**, respectively, and contacting the **barrier layer**; and
✓	**[1e]** a **gate metal** disposed on the **p-type gate material**, the **gate metal** having sidewalls extending towards the **p-type gate material**,
	[1f] wherein the **p-type gate material** comprises a pair of **horizontal ledges** that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of **horizontal ledges** having **substantially equal widths** from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.
No patentable weight	**[2]** The enhancement-mode GaN transistor according to claim 1, wherein the pair of **horizontal ledges** of the **p-type gate material** are **self-aligned**.

’335 Pet. at 24-51

’335 Patent Ground 2: Saxler-Yoshida renders obvious claims 1-7

Innoscience

Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	**Saxler** in view of the knowledge of a POSITA
2	1-7	§ 103	**Saxler** in view of Yoshida
3	2, 5-7	§ 103	**Saxler** in view of Yoshida, Beach, and Shenoy
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA
5	1-7	§ 103	**Yoshida** in view of Saxler
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy

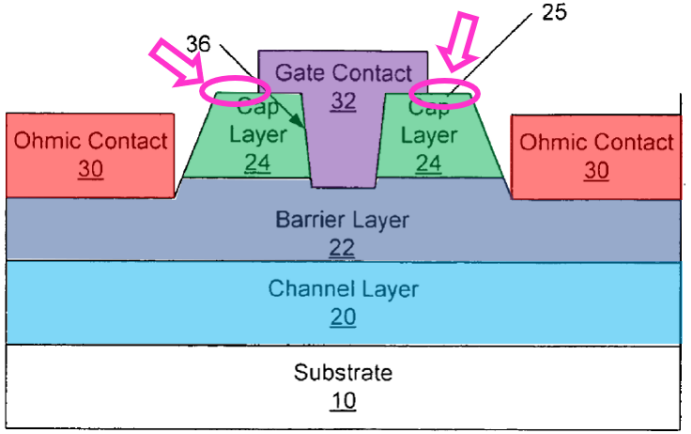
Ground 2 is the same as Ground 1 with the additional motivation added by Yoshida to make Saxler’s device enhancement mode.

It would have been obvious based on Yoshida to remove Saxler’s recess to receive the benefits of enhancement mode.

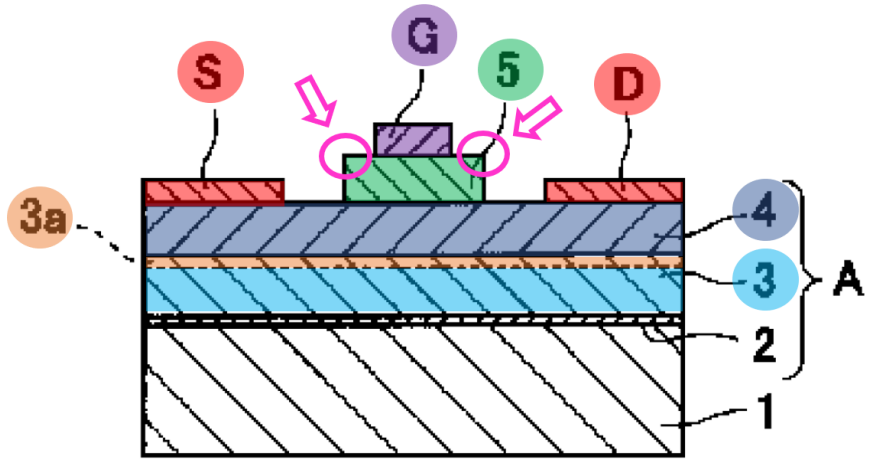
’335 Pet. at 16

’335 Patent Ground 2: Saxler-Yoshida renders obvious claims 1-7

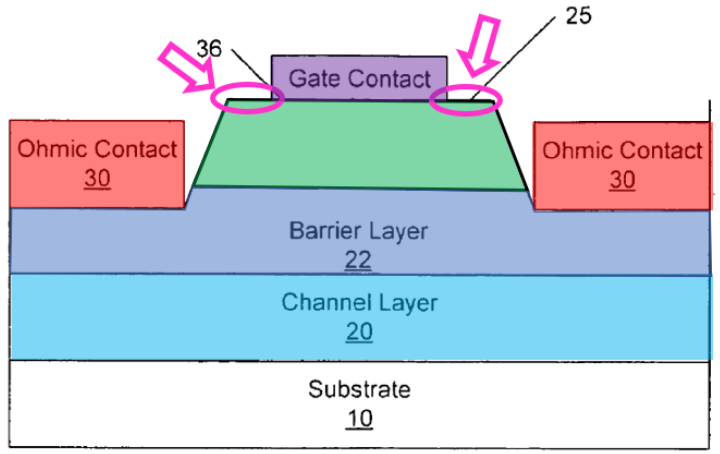
Saxler depicts a depletion mode device with a recessed gate



Yoshida depicts an enhancement mode device with every claim feature but the horizontally extended sidewalls

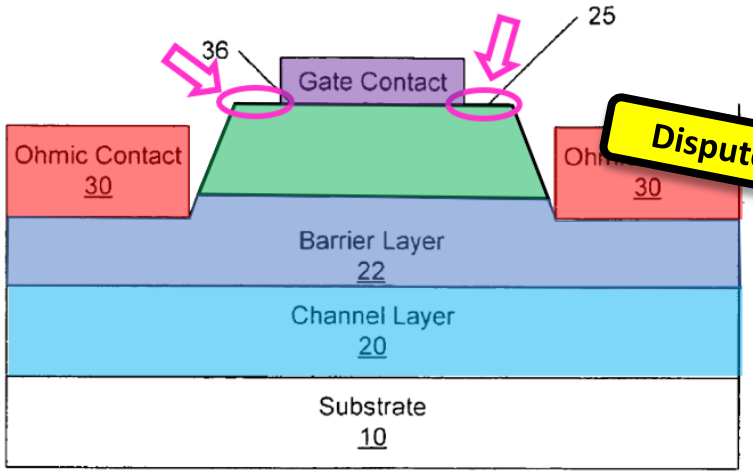


A POSITA would have removed Saxler’s recess based on Saxler’s express teachings and Yoshida’s teachings to achieve an enhancement mode device



’335 Pet., 28-35.

’335 Patent Ground 2: Saxler-Yoshida renders obvious claims 1-7



Saxler, Fig. 1A (modified).

Saxler	Limitation
✓	**[1p], [5p]** An **enhancement-mode** GaN transistor, comprising:

Disputed

Patent Owner’s Arguments Fail

Patent Owner is wrong that a POSITA would not modify Saxler’s recessed embodiment by removing the recess based on Yoshida

The only new argument Patent Owner presents is the alleged change to Saxler’s “principle of operation,” citing *In re Ratti*, 270 F.2d 810 (C.C.P.A. 1959)

Patent Owner’s reliance on *In re Ratti* is inapposite. POR, 46; 270 F.2d 810, 813 (C.C.P.A. 1959). There, the C.C.P.A. declined to combine references that “require[d] a substantial reconstruction and redesign” along with “change[s] in the basic principles” of operation. *In re Ratti*, 270 F.2d at 813. Here, a POSITA would have readily understood a simple substitution of *Saxler*’s recessed gate with *Yoshida*’s non-recessed gate in a p-type embodiment of Figure 1A would have predictably achieved enhancement mode. Petition, 25, 32-36; Shealy, [090], [102]-[106], [108]-[0109]. This does not change the “principle of operation”—*Saxler* teaches its recess is optional—and the Petition identified ample motivation to make the proposed combination, including simplifying manufacturing, decreasing costs, and receiving the benefits of a normally-off device suitable for high power applications. Petition, 32-36; Shealy, [102]-[106].

’335 Reply, 13.

Saxler teaches its recess is optional—the proposed modification does not alter its “principle of operation.”

At Institution, the Board agreed a POSITA would have reason to combine Saxler and Yoshida, “to take advantage of simplified manufacturing steps and reduced cost.” ’335 ID, 44.

’335 POR, 45-47; ’335 Reply, 12-13.

’335 Patent Ground 3: Saxler-Yoshida in view of Beach and Shenoy renders obvious claims 2, 5-7

Innoscience

Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	Saxler in view of the knowledge of a POSITA
2	1-7	§ 103	**Saxler** in view of Yoshida
3	2, 5-7	§ 103	**Saxler** in view of Yoshida, Beach, and Shenoy
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA
5	1-7	§ 103	Yoshida in view of Saxler
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy

The Board needs to Ground 3 of the ’335 Patent IPR only if the Board does not agree “self-aligned” is product by process.

This combination is relevant for the method of claim 3 of the ’347 Patent and will be addressed later below.

’335 Pet., 57-67.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7

Saxler Grounds

Yoshida Grounds

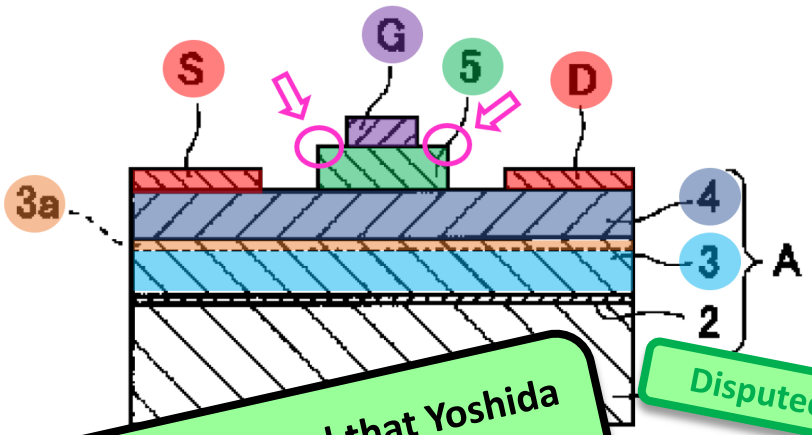
Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	Saxler in view of the knowledge of a POSITA
2	1-7	§ 103	**Saxler** in view of Yoshida
3	2, 5-7	§ 103	Saxler in view of Yoshida, Beach, and Shenoy
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA
5	1-7	§ 103	Yoshida in view of Saxler
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy

If the Board agrees on claim construction, to find all claims invalid over Yoshida (Ground 4), the Board need only:

- ✓ Agree horizontally extended sidewalls were obvious because perfectly vertical sidewalls were rare in practice when making real devices
- ✓ Agree *Yoshida’s* drawings can be relied on to disclose “substantially equal” ledges (no factual dispute, only a legal dispute that drawings can disclose this limitation)

’335 Pet., 67-88.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7



It is not disputed that Yoshida discloses an enhancement mode transistor.

Under Board’s construction, any horizontal extension of the p-GaN satisfies the claims

It is not disputed that Yoshida depicts ledges with “substantially equal widths,” only whether *Hockerson* applies

Yoshida	Limitation
✓	**[1p]** An enhancement-mode GaN transistor, comprising:
✓	**[1a]** a GaN layer;
✓	**[1b]** a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
✓	**[1c]** a source contact and a drain contact formed on the barrier layer;
✓	**[1d]** a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
✓	**[1e]** a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.
No patentable weight	**[2]** The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material **are** self-aligned.

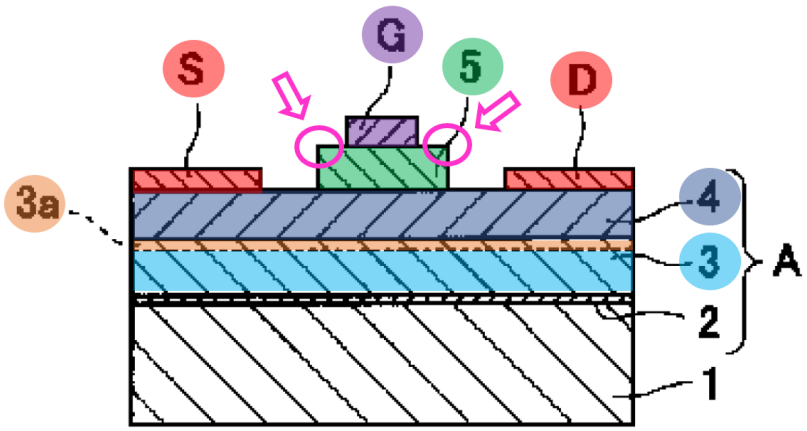
Disputed

Disputed

Disputed

’335 Pet., 67, 74-80; ’335 Reply, 24-25.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7



Yoshida, Fig. 1.

Yoshida	Limitation
✓	**[5p]** An enhancement-mode GaN transistor, comprising:
✓	**[5a]** a **GaN layer**;
✓	**[5b]** a **barrier layer** disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
✓	**[5c]** a **source contact** and a **drain contact** formed on the barrier layer;
✓	**[5d]** a **p-type gate material** formed above the barrier layer and between the source and drain contacts,
✓	**[5e]** **a gate metal** disposed on **the p-type gate material**,
✓	**[5f]** wherein the **p-type gate material** comprises: (i) a pair of **self-aligned ledges** that extend past sidewalls of the **gate metal** towards the **source contact** and **drain contact**, respectively; and
✓	**[5g]** ~~(ii)~~ **side surfaces that extend horizontally** towards the **source contact** and **drain contact**, respectively, and contact the **barrier layer.**

Disputed

Disputed

’335 Pet., 67, 74-80; ’335 Reply, 24-25.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7

Patent Owner only disputes the Yoshida combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1d], [5g] the **p-type gate material having side surfaces extending horizontally** (Yoshida alone)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivations to combine (grounds 2-3, 4-5)

’335 Pet., 67-88.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7

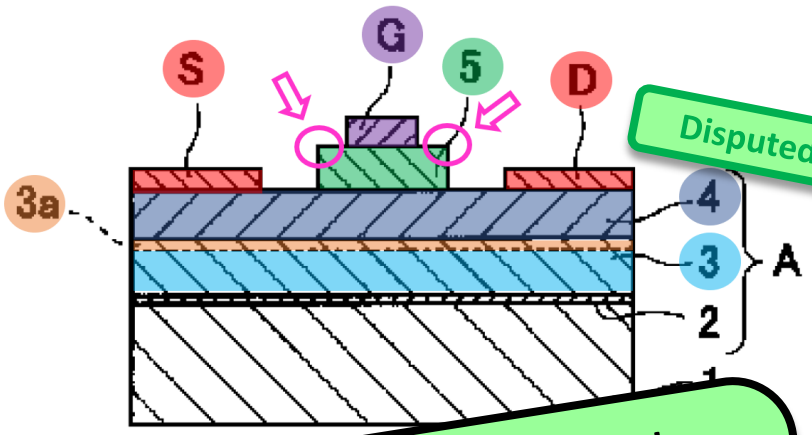
Patent Owner only disputes the Yoshida combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1d], [5g] the **p-type gate material having side surfaces extending horizontally** (Yoshida alone)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivations to combine (grounds 2-3, 4-5)

✓ Yoshida discloses “side surfaces extending horizontally” because they would extend “at least slightly on the bottom due to manufacturing tolerances” and perfectly vertical sidewalls were “rare in practice.”

’335 Pet., 67-88.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7



Disputed

Yoshida	Limitation
✓	**[1d]** a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
✓	wherein the p-type gate material comprises **[5g]** (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

At Institution, the Board found Petitioner’s evidence (Saxler, Uemoto, and Dr. Shealy’s declaration) supported argument a POSITA would understand Yoshida’s sidewalls to have a wider bottom surface than top. ’335 ID, 51.

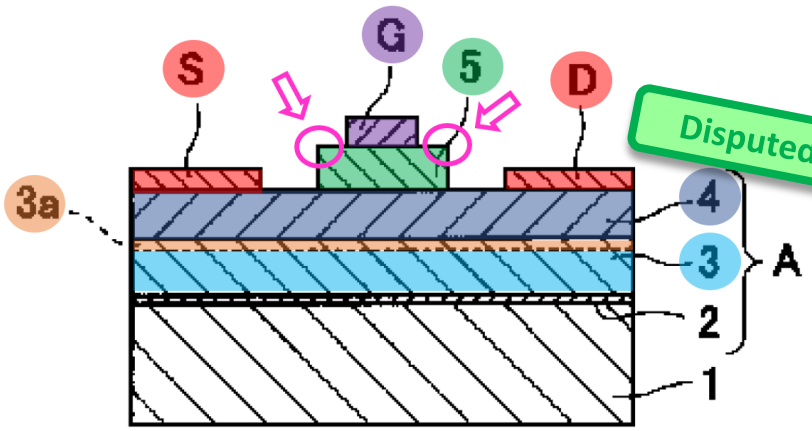
Under Board’s construction, any horizontal extension satisfies the claim

- ✓ **Yoshida renders obvious “side surfaces extending horizontally” because perfectly vertical sidewalls are rare in practice:**
  1. **Saxler states vertical sidewalls “typically” have tapered features**
  2. **Uemoto’s drawings show vertical sidewalls and sloped sidewalls when implemented**
  3. **Dr. Shealy explained they would extend “at least slightly on the bottom due to manufacturing tolerances” and perfectly vertical sidewalls were “rare in practice.”**

’335 Pet., 67-68; ’335 Shealy, [182] [203]-[205] (citing Saxler, [0042]; Uemoto, Figs. 1-2, 5).

’335 Pet., 67, 74-80; ’335 Reply, 24-25.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7



Yoshida, Fig. 1.

Disputed

Yoshida	Limitation
✓	**[1d]** a **p-type gate material** formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the **source contact** and **drain contact**, respectively, and contacting the **barrier layer**; and
✓	wherein the **p-type gate material** comprises **[5g]** (ii) **side surfaces that extend horizontally** towards the **source contact** and **drain contact**, respectively, and contact the **barrier layer.**

At Institution, the Board found Petitioner’s evidence (Saxler, Uemoto, and Dr. Shealy’s declaration) supported argument a POSITA would understand Yoshida’s sidewalls to have a wider bottom surface than top. ’335 ID, 51.

1. **Saxler states vertical sidewalls “typically” have tapered features**

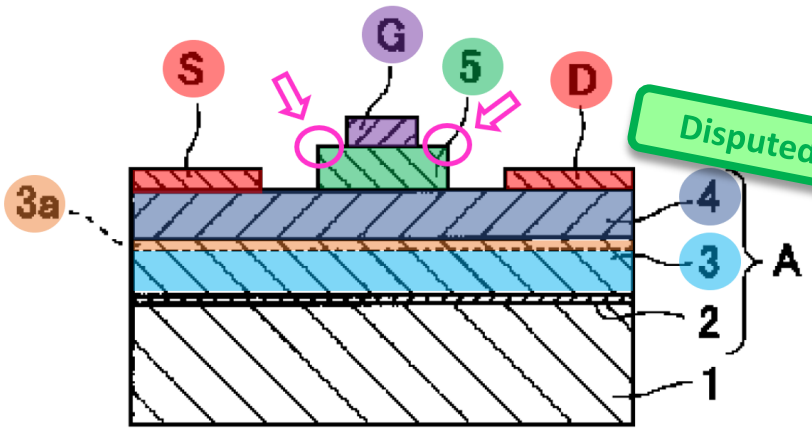
result, for example, from manufacturing. For example, an etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features. Thus, the regions

Saxler, [0042]

’335 Pet., 67, 74-78; ’335 Reply, 24-25.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7

Innoscience



Yoshida, Fig. 1.

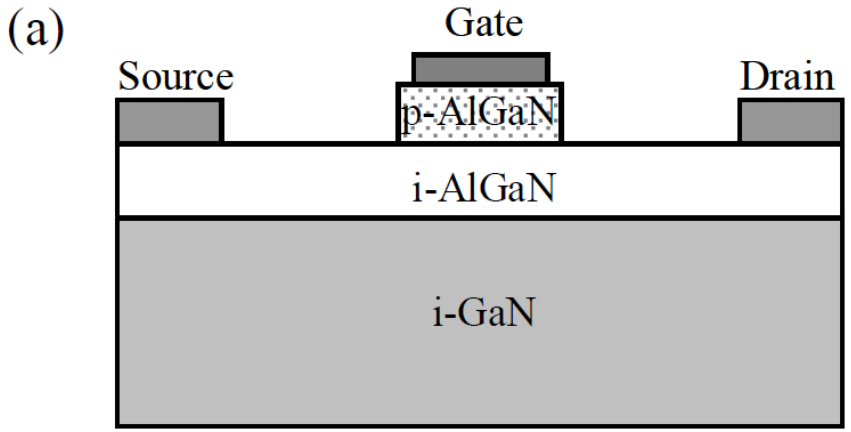
Disputed

Yoshida	Limitation
✓	**[1d]** a **p-type gate material** formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the **source contact** and **drain contact**, respectively, and contacting the **barrier layer**; and
✓	wherein the **p-type gate material** comprises **[5g]** (ii) **side surfaces that extend horizontally** towards the **source contact** and **drain contact**, respectively, and contact the **barrier layer.**

At Institution, the Board found Petitioner’s evidence (Saxler, Uemoto, and Dr. Shealy’s declaration) supported argument a POSITA would understand Yoshida’s sidewalls to have a wider bottom surface than top. ’335 ID, 51.

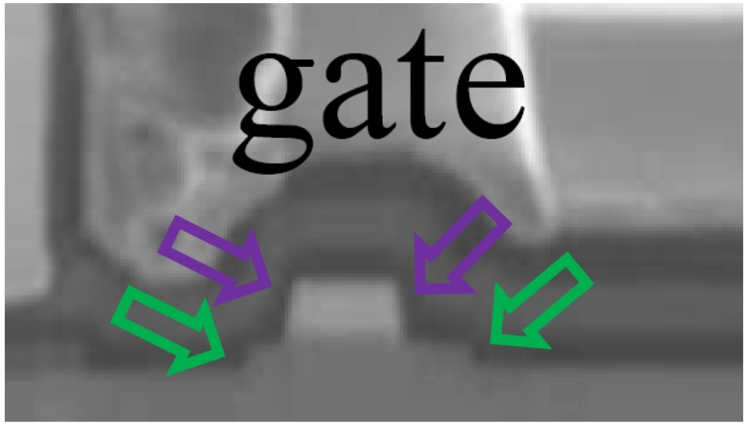
’335 Pet., 67, 74-78; ’335 Reply, 24-25.

2. Uemoto’s drawings show vertical sidewalls and sloped sidewalls when implemented



Uemoto, Fig. 1(a)

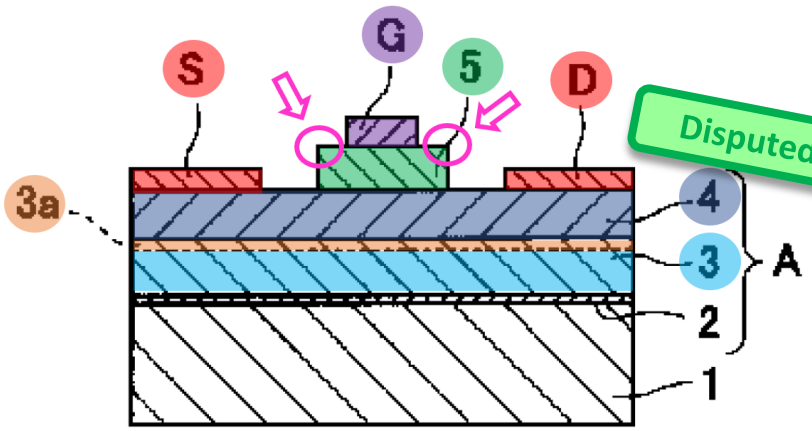
Drawing: vertical sidewalls



Uemoto, Fig. 5 (showing sloped sidewalls of the **p-AlGaN** layer and **gate metal**).

Implementation: horizontally extended sidewalls

’335 Patent Ground 4: Yoshida renders obvious claims 1-7



Yoshida, Fig. 1.

Yoshida	Limitation
✓	**[1d]** a **p-type gate material** formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the **source contact and drain contact**, respectively, and contacting the **barrier layer**; and
✓	wherein the **p-type gate material** comprises **[5g]** (ii) **side surfaces that extend horizontally** towards the **source contact** and **drain contact**, respectively, and contact the **barrier layer.**

Disputed

At Institution, the Board found Petitioner’s evidence (Saxler, Uemoto, and Dr. Shealy’s declaration) supported argument a POSITA would understand Yoshida’s sidewalls to have a wider bottom surface than top. ’335 ID, 51.

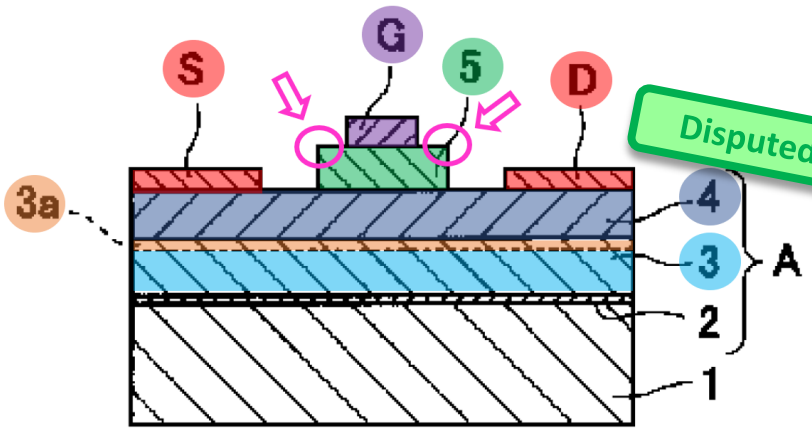
3. Dr. Shealy explained Yoshida’s sidewalls would extend “at least slightly on the bottom due to manufacturing tolerances” and perfectly vertical sidewalls were “rare in practice.”

[182] *Yoshida* discloses the arrangement of semiconductor layers and structures of claims 1-7, including the claimed ledges. Although *Yoshida* depicts that the walls of its p-type GaN material are vertical and not sloped as required by Limitation [1d] and Limitation [5g], it is my opinion that sloped sidewalls were common and obvious over *Yoshida*, at least because perfectly vertical sidewalls were rare in practice. Under Patent Owner’s construction of the slope terms (“p-

’335 Shealy, [0182]

’335 Pet., 67, 74-78; ’335 Reply, 24-25.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7



Yoshida, Fig. 1.

Disputed

Yoshida	Limitation
✓	**[1d]** a **p-type gate material** formed above the barrier layer, the **p-type gate material** having **side surfaces extending horizontally** towards the **source contact** and **drain contact**, respectively, and contacting the **barrier layer**; and
✓	wherein the **p-type gate material** comprises **[5g]** (ii) **side surfaces that extend horizontally** towards the **source contact** and **drain contact**, respectively, and contact the **barrier layer.**

Patent Owner irrelevantly cites the law of anticipation in a misplaced attempt to rebut the Petition’s reasoning that horizontally extended sidewalls would have been obvious in practice.

sidewalls slope outwards when implemented in practice. Petition, 67-68. Patent Owner mischaracterizes the Petition as asserting an inherency argument under 35 U.SC. § 102, inappropriately relying on caselaw addressing anticipation. POR, 61-62 (citing *In re Robertson,* 169 F.3d 743, 745 (Fed. Cir. 1999); *Continental Can Co. USA, Inc. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991); *Rexnord Indus., LLC v. Kappos*, 705 F.3d 1347, 1355 (Fed. Cir. 2013)). Unlike anticipation, obviousness permits supplementing a missing limitation “generally known” in the art. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1338-39 (Fed. Cir. 2020).

’335 Reply, 25

’335 Pet., 67, 74-78; ’335 Reply, 24-25.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7

Innoscience

Patent Owner only disputes the Yoshida combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1d], [5g] the **p-type gate material having side surfaces extending horizontally** (Yoshida alone)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivations to combine (grounds 2-3, 4-5)

All of Patent Owner’s Arguments Fail

✓ Yoshida discloses “side surfaces extending horizontally” because they would extend “at least slightly on the bottom due to manufacturing tolerances” and perfectly vertical sidewalls were “rare in practice.”

’335 Pet., 67, 74-78; ’335 Reply, 24-25.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7

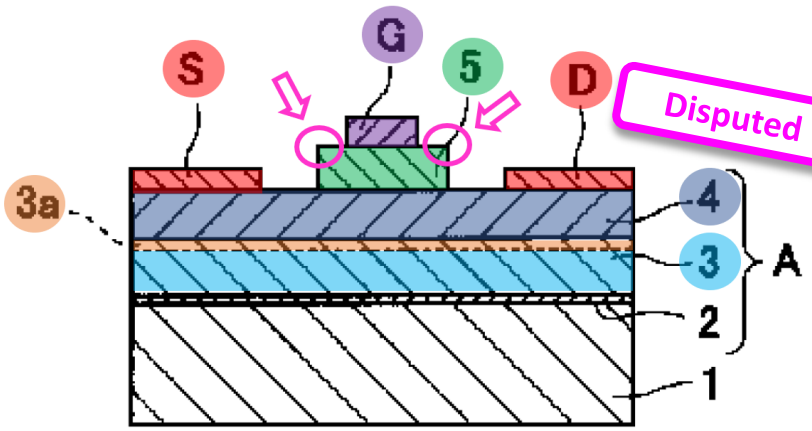
Patent Owner only disputes the Yoshida combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1d], [5g] the **p-type gate material having side surfaces extending horizontally** (Yoshida alone)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivations to combine (grounds 2-3, 4-5)

✓ Yoshida’s drawings disclose ledges with “substantially equal widths”

’335 Pet., 83-84; Reply, 14-19.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7



Yoshida, Fig. 1.

Saxler	Limitation
✓	**[1f]** wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively

Disputed

✓ Yoshida’s drawings disclose ledges with “substantially equal widths”

1. **Yoshida plainly shows “horizontal ledges” with “substantially equal widths” [*undisputed*]**
2. **“substantially equal” is not a precise term, so *Hockerson* does not apply.**

Patent Owner does not dispute that Yoshida shows substantially equal ledges, only that the claims cannot be obvious over Yoshida’s drawings under *Hockerson*

All of Patent Owner’s Arguments Fail For the Same Reasons as with Saxler

’335 Pet., 83-84; Reply, 14-19.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7

Innoscience

Patent Owner only disputes the Yoshida combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1d], [5g] the **p-type gate material having side surfaces extending horizontally** (Yoshida alone)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivations to combine (grounds 2-3, 4-5)

✓ Yoshida’s drawings disclose ledges with “substantially equal widths”

All of Patent Owner’s Arguments Fail For the Same Reasons as with Saxler

’335 Pet., 83-84; Reply, 14-19.

’335 Patent Ground 4: Yoshida renders obvious claims 1-7

Innoscience

Patent Owner only disputes the Yoshida combinations of prior art shows *three* features for claims 1-7 of the ’335 patent and the motivations to combine the references

- ✓ [1d], [5g] the **p-type gate material having side surfaces extending horizontally** (Yoshida alone)
- ✓ [1f] **horizontal ledges** with **substantially equal widths** (all grounds)
- ✓ [2], [5f] **self aligned horizontal ledges** (all grounds)
- ✓ Motivations to combine (grounds 2-3, 4-5)

✓ Yoshida renders “self-aligned” ledges unpatentable because Yoshida discloses the claimed structure and “self-aligned” is a product-by-process term.

All of Patent Owner’s Arguments Fail For the Same Reasons as with Saxler

’335 Pet., 84.

’335 Patent Ground 5: Yoshida-Saxler renders obvious claims 1-7

Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	Saxler in view of the knowledge of a POSITA
2	1-7	§ 103	**Saxler** in view of Yoshida
3	2, 5-7	§ 103	Saxler in view of Yoshida, Beach, and Shenoy
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA
5	1-7	§ 103	**Yoshida** in view of Saxler
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy

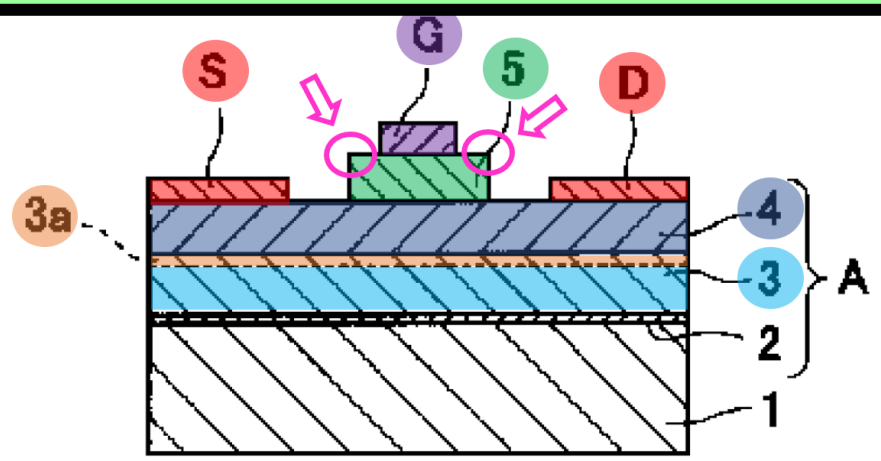
Saxler provides additional motivation to extend Yoshida’s sidewalls

- ✓ A POSITA would have incorporated Saxler’s known etching for sloped sidewalls in the p-GaN layer into Yoshida’s device to reduce gate leakage.

’335 Pet. at 16, 67-84

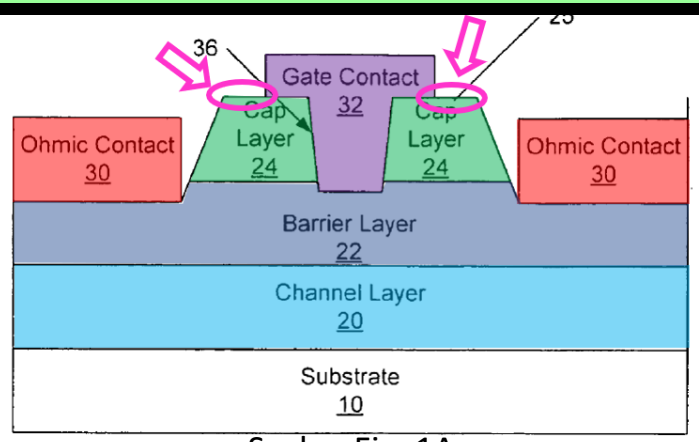
’335 Patent Ground 5: Yoshida-Saxler renders obvious claims 1-7

Yoshida depicts an enhancement mode device with every feature but the horizontally extended sidewalls in its p-GaN layer, which would have been present in practice



Yoshida, Fig. 1.

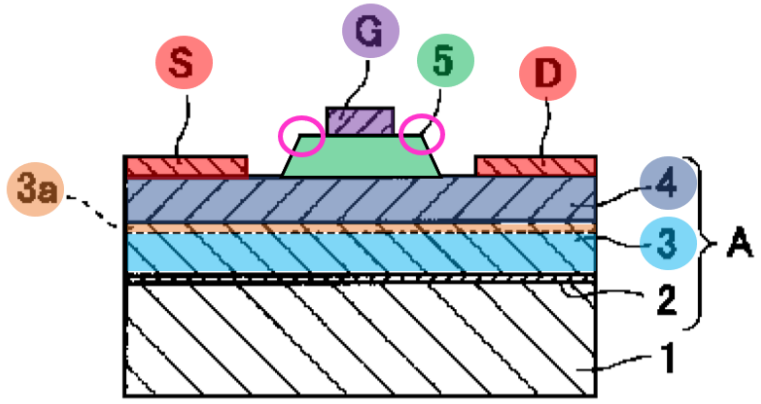
Saxler discloses etching sloped sidewalls for its p-GaN cap layer



Saxler, Fig. 1A.

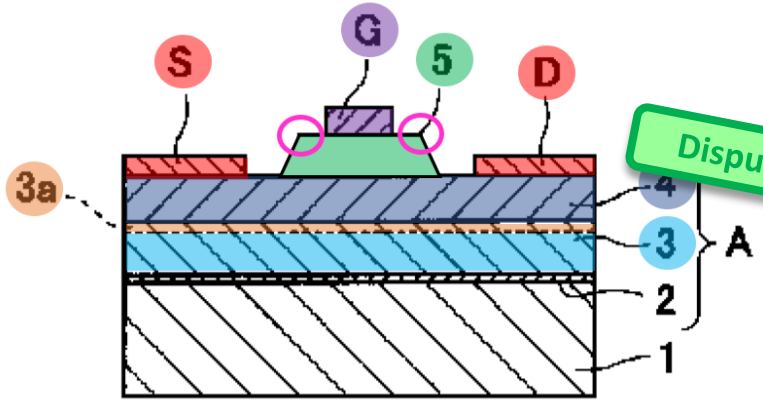
’335 Pet., 68-71.

A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage



Yoshida, Fig. 1 (modified).

’335 Patent Ground 5: Yoshida-Saxler renders obvious claims 1-7



Yoshida, Fig. 1 (modified).

Disputed

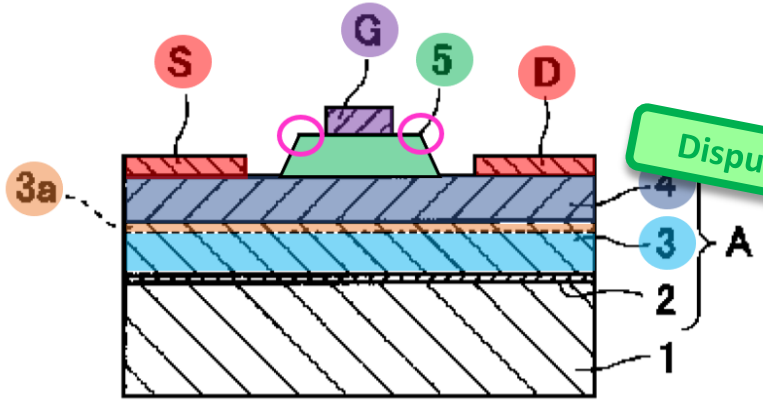
Yoshida-Saxler	Limitation
✓	**[1d]** a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
✓	wherein the p-type gate material comprises **[5g]** (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

✓ Saxler-Yoshida render obvious **horizontally extended sidewalls**

1. **Saxler provided a known option for shaping the sidewalls of Yoshida’s p-type layer 5.**
2. **Incorporating Saxler’s sloped sidewalls would have reduced gate leakage because they provide longer leakage paths.**

’335 Pet., 68-71.

’335 Patent Ground 5: Yoshida-Saxler renders obvious claims 1-7



Yoshida, Fig. 1 (modified).

Yoshida-Saxler	Limitation
✓	**[1d]** a ~~p-type gate material~~ formed above the barrier layer, the p-type gate material ~~having~~ side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
✓	wherein the p-type gate material comprises **[5g]** (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

Disputed

Patent Owner does not dispute the known benefits of longer leakage paths along sloped sidewalls to reduce gate leakage

- ✓ It was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage. ’335 Pet. 71; ’335 Shealy, [189]; Xu, 1; Kanda, [0013], [0027], [0144], [0157]
- ✓ A POSITA would have understood that the geometry of Saxler’s sloped sidewalls provided longer leakage paths than Yoshida’s vertical sidewalls, thereby lowering gate leakage. ’335 Pet. 71; ’335 Shealy, [189]
- ✓ **This improvement makes Saxler’s sloped sidewalls a suitable option, motivating the combination. *KSR*, 550 U.S. at 417; *Intel Corp. v. PACT XXP Schweiz AG*, 61 F.4th 1373,1379-81 (Fed. Cir. 2023).**

’335 Pet., 70-71.

’335 Pet., 70-71

’335 Patent Ground 6: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 2, 5-7

Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	Saxler in view of the knowledge of a POSITA
2	1-7	§ 103	**Saxler** in view of Yoshida
3	2, 5-7	§ 103	Saxler in view of Yoshida, Beach, and Shenoy
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA
5	1-7	§ 103	Yoshida in view of Saxler
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy

The Board needs to reach Ground 6 of the ’335 Patent IPR only if the Board does not agree “self-aligned” is product by process.

This combination is relevant for the method of claim 3 of the ’347 Patent and will be addressed later below.

’335 Patent: All claims invalid

Innoscience

Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art	
1	1-7	§ 103	**Saxler** in view of the knowledge of a POSITA	All Claims Invalid
2	1-7	§ 103	**Saxler** in view of Yoshida	All Claims Invalid
3	2, 5-7	§ 103	**Saxler** in view of Yoshida, Beach, and Shenoy	Claims Invalid
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA	All Claims Invalid
5	1-7	§ 103	**Yoshida** in view of Saxler	All Claims Invalid
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy	Claims Invalid

’335 Pet. at 29.

’347 Patent Invalidity Grounds

’347 Patent Invalidity Grounds

Innoscience

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103	*Saxler*, *Beach*, and *Shenoy*
2	1-3	§ 103	*Saxler*, *Yoshida*, *Beach*, and *Shenoy*
3	1-3	§ 103	*Saxler* and *Ahn*
4	1-3	§ 103	*Yoshida*, *Saxler*, *Beach*, and *Shenoy*
5	1-3	§ 103	*Yoshida* and *Ahn*

Saxler Grounds

Yoshida Grounds

Disputes regarding Saxler and Yoshida track disputes on the ’335 grounds

To find claims 1-3 invalid under the combinations, aside from disputes addressed for the ’335 patent, the Board need only agree:

- ✓ (i) make the Saxler, Saxler-Yoshida, or Yoshida-Saxler gate structure using the combination of Beach and Shenoy’s techniques; or
- ✓ (ii) make the Saxler or Yoshida gate structure using Ahn’s approach.

’347 Patent Invalidity Grounds

Innoscience

The Prior Art	Limitation
✓	**[1p]** A method for manufacturing an **enhancement-mode GaN transistor**, the method comprising:
✓	**[1a]** forming a **GaN layer**;
✓	**[1b]** forming a **barrier layer** on the **GaN layer**;
✓	**[1c]** depositing **source** and a **drain contacts** on the **barrier layer**;
✓	**[1d]** depositing a **p-type gate material** on the **barrier layer**;
✓	**[1e]** depositing a **gate metal** on the **p-type gate material**;
✓	**[1f]** forming a photoresist over the **gate metal**;
✓	**[1h]** wherein the step of etching the **p-type gate material** comprises forming side surface of **the p-type gate material that extend horizontally** towards the **source** and **drain contacts**, respectively, and contact the **barrier layer**; and
✓	**[1i]** etching the gate metal to form a pair of **ledges** on the **p-type gate material** below the gate metal.
✓	**[2]** The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.
✓	**[3]** The method according to claim 1, wherein the pair of **ledges** of the **p-type gate material** are **self-aligned**.

Disputed

Disputes for ’347 track disputes on the ’335 grounds

Disputed

Disputed

’335 Pet. at 29.

’347 Patent: Just Three Claim Features Disputed

Patent Owner only disputes the combinations of prior art shows *three* features for claims 1-3 of the ’347 patent and the motivations to combine the references

- ✓ [1p] **enhancement mode** (Saxler grounds)
- ✓ [1h] etching the p-type gate material comprises forming **side surfaces of the p-type gate material that extend horizontally** (Yoshida alone)
- ✓ [3] **self aligned ledges** (all grounds)
- ✓ Motivations to combine (all grounds)

At Institution, the Board found Petitioners’ evidence that p-type doping would provide an enhancement-mode transistor persuasive. ’347 ID, 31.

At Institution, the Board found Petitioner’s evidence (Saxler, Uemoto, and Dr. Shealy’s declaration) supported argument a POSITA would understand Yoshida’s sidewalls to have a wider bottom surface than top. ’347 ID, 47-48.

At Institution, the Board found the combinations with Beach and Shenoy and combinations with Ahn would have resulted in a self-aligned method. ’347 ID, 36, 50-51.

See generally ’347 POR

’347 Patent Grounds 1-2: Saxler (+Yoshida) renders obvious Claims 1-3

Innoscience

Saxler Grounds

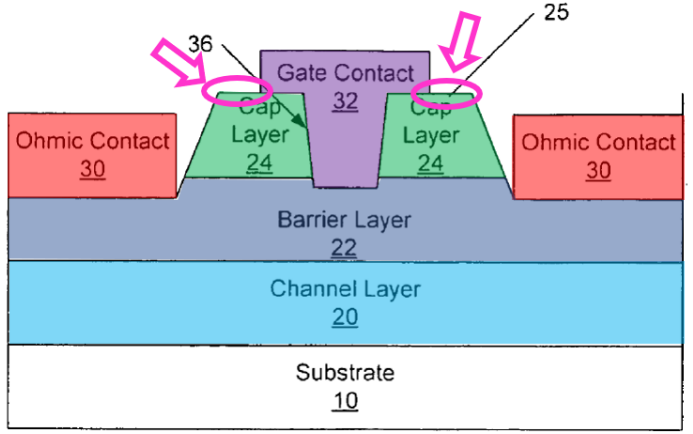
Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103	*Saxler*, *Beach*, and *Shenoy*
2	1-3	§ 103	*Saxler*, *Yoshida*, *Beach*, and *Shenoy*
3	1-3	§ 103	*Saxler* and *Ahn*
4	1-3	§ 103	*Yoshida*, *Saxler*, *Beach*, and *Shenoy*
5	1-3	§ 103	*Yoshida* and *Ahn*

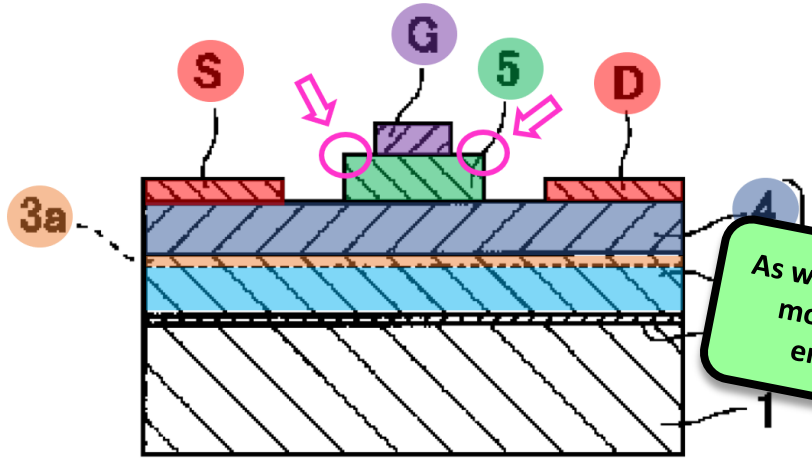
’347 Patent Grounds 1-2: Saxler (+Yoshida) renders obvious Claims 1-3

Innoscience

Saxler depicts a depletion mode device with a recessed gate



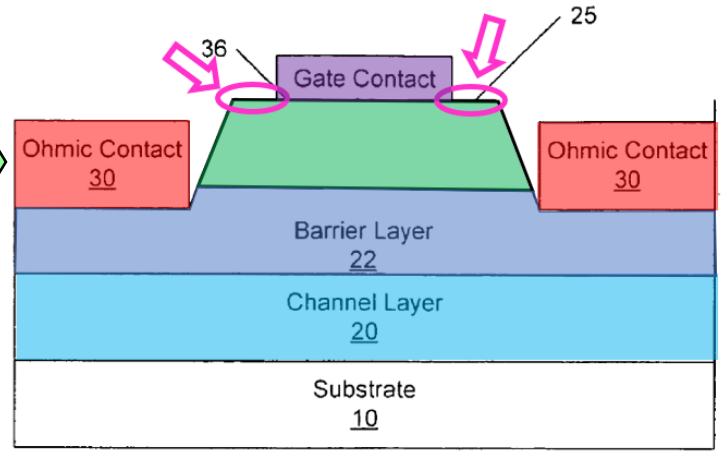
Yoshida depicts an enhancement mode device with every claim feature but the horizontally extended sidewalls



’347 Pet., 24-28, 51-56.

As with the ’335 patent, Yoshida provides additional motivation to make Saxler’s modified Fig. 1A in enhancement mode (’347 Patent, Ground 2)

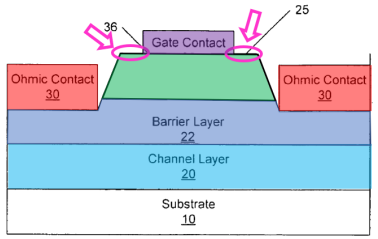
Target Structure:
Saxler’s Modified Fig. 1A
A POSITA would have removed Saxler’s recess based on Saxler’s express teachings (and Yoshida’s teachings (Ground 2)) to achieve the benefits an enhancement mode device



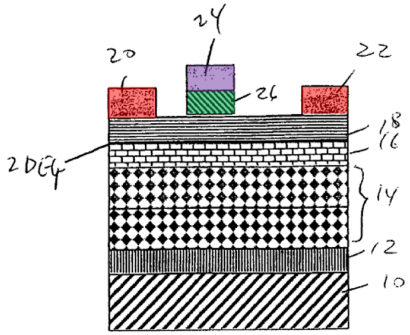
Innoscience

A POSITA would have combined Saxler (+Yoshida) Beach, and Shenoy to simplify the process and improve alignment

Target structure:
Modified Saxler Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Beach’s Single Mask

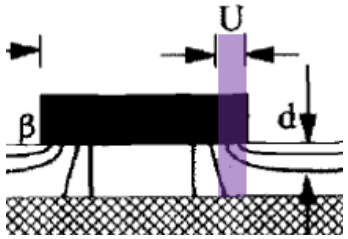


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

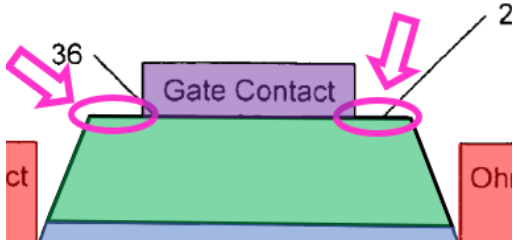
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Modified Saxler Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

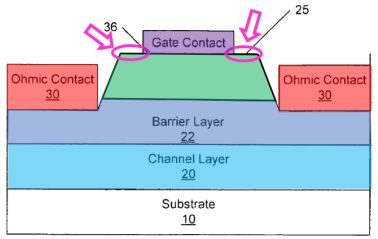
’347 Pet. at 28-35, 57; ’347 Reply 3-12.

’347 Patent Grounds 1-2: Saxler (+Yoshida) renders obvious Claims 1-3

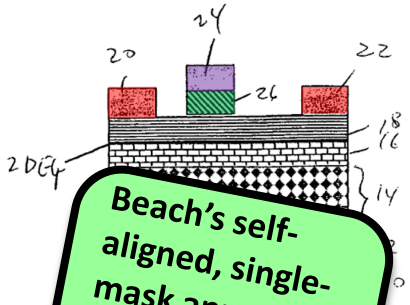
Innoscience

A POSITA would have combined Saxler (+Yoshida) Beach, and Shenoy to simplify the process and improve alignment

Target structure:
Modified Saxler Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Beach’s Single Mask



Beach’s self-aligned, single-mask approach is compatible with Saxler’s etching

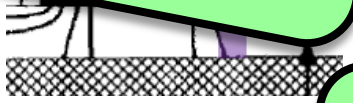
with Saxler’s etching to create sloped sidewalls

Saxler, Fig.

A POSITA would have used the known techniques of Beach and Shenoy to simplify Saxler-Yoshida process—they are suitable options.

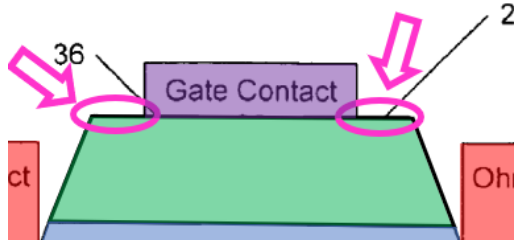
Shenoy’s Undercut

POSITA would have used Shenoy’s approach to etch the metal and form Saxler-Yoshida’s structure



Shenoy, Fig. 1.

Modified Saxler Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

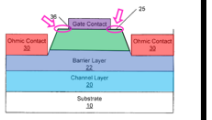
At Institution, the Board found the Saxler-Yoshida with Beach and Shenoy would have resulted in a self-aligned method. ’347 ID, 36.

’347 Pet. at 28-35, 57; ’3347 Reply 3-12.

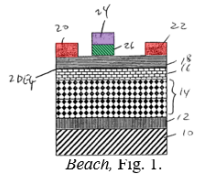
’347 Patent Grounds 1-2: Saxler (+Yoshida) renders obvious Claims 1-3

A POSITA would have combined Saxler (+Yoshida) Beach, and Shenoy to simplify the process and improve alignment

Target structure: Modified Saxler Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Beach’s Single Mask

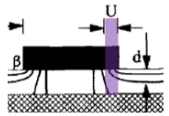


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

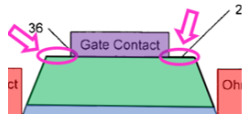
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Modified Saxler Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

Patent Owner’s Three Arguments Fail

A
The POR incorrectly contends the Petition did not provide the “specific process sequence” for the proposed combination. ’347 POR, 46.

B
Patent Owner misunderstands obviousness, citing inapposite case law to contend no motivation to combine Beach and Shenoy with Saxler or Saxler-Yoshida. ’347 POR, 2-3, 47, 48.

C
Patent Owner irrelevantly argues Beach etches n-type materials when Saxler has p-type. ’347 POR, 39.
Patent Owner inaccurately argues Beach’s approach would “cut off” Saxler’s sloped sidewalls. ’347 POR, 38-39.

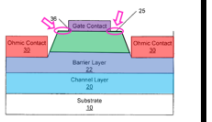
D
Patent Owner and Dr. Schubert incorrectly argue Shenoy’s undercut would etch the p-GaN layer. ’347 POR, 40-45.

’347 Pet. at 28-35, 57; ’347 Reply 3-12.

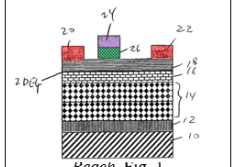
’347 Patent Grounds 1-2: Saxler (+Yoshida) renders obvious Claims 1-3

A POSITA would have combined Saxler (+Yoshida) Beach, and Shenoy to simplify the process and improve alignment

Target structure:
Modified Saxler Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Beach’s Single Mask

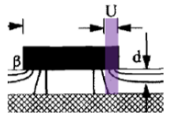


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

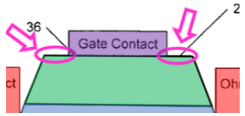
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Modified Saxler Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

A
The POR incorrectly contends the Petition did not provide the “specific process sequence” for the proposed combination. ’347 POR, 46.

The Petition explained a POSITA would have implemented Beach and Shenoy’s known masking and etching methods to make Saxler’s (or Saxler-Yoshida’s) gate structure

’347 Pet. at 30-35, 52-56; ’347 Reply, 13-20.

1. A POSITA would have used the techniques of Beach and Shenoy to simplify and improve Saxler’s (or Saxler-Yoshida’s) process

Smith, *Hu*, *Shenoy*, Ex. 1023), [0092] (citing *Smith*, [0042]). It would have been obvious to modify *Saxler* with *Beach*’s self-aligned technique and *Shenoy*’s isotropic etching to arrive at that same non-recessed gate structure, which would reduce steps and costs while improving reproducibility and symmetry of the gate structure layers. Shealy, [93]. A POSITA would have recognized this as a simple and predictable

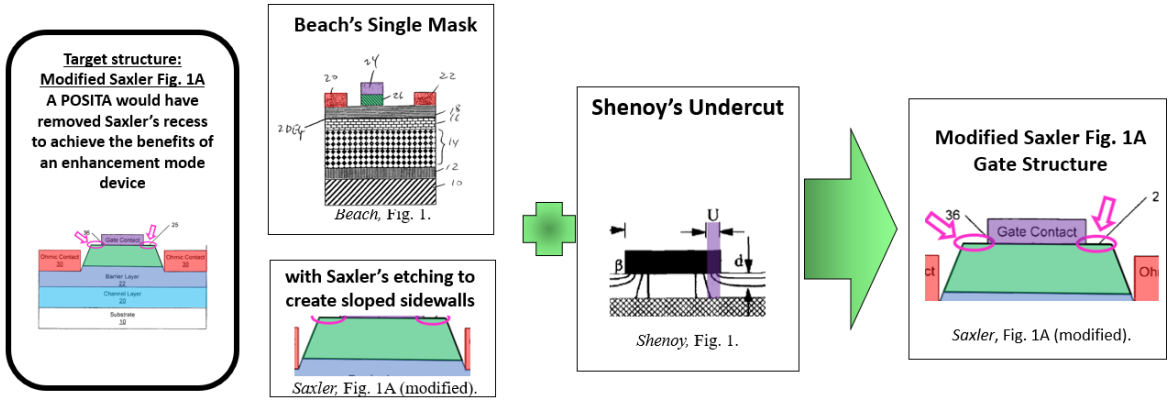
’347 Pet., 32

Thus, an ordinary artisan would have found it obvious to use *Beach*’s self-aligned method and *Shenoy*’s methods to undercut the gate electrode to create *Saxler*’s horizontal ledges. Shealy, [097]. That combination of steps was already known for creating stepped, stacked transistor gates. *Id.* (citing *Ahn*). A POSITA would have found the combination a simple substitution of *Beach*’s and *Shenoy*’s known methods that would be predictably implemented in *Saxler*’s flexible method of manufacturing to improve alignment and symmetry between layers and reduce steps and costs. *Id.* (citing *Saxler*, [0046], [0068]; *Sheppard*, [0058]).

’347 Pet., 34-35

’347 Patent Grounds 1-2: Saxler (+Yoshida) renders obvious Claims 1-3

A POSITA would have combined Saxler (+Yoshida) Beach, and Shenoy to simplify the process and improve alignment



B

Patent Owner misunderstands obviousness, citing inapposite case law to contend no motivation to combine Beach and Shenoy with Saxler or Saxler-Yoshida. ’347 POR, 2-3, 47, 48.

’347 Pet. at 28-35, 57; ’347 Reply 3-12.

1. A POSITA would have used the techniques of Beach and Shenoy to simplify and improve Saxler’s (or Saxler-Yoshida’s) process

Patent Owner misunderstands obviousness, citing inapposite case law

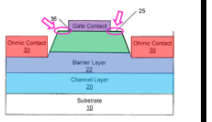
- *In re Dembiczak* applied teaching-suggesting-motivation test that KSR firmly rejected. 175 F.3d 994 (Fed. Cir. 1999)
- *InTouch* faulted the expert for providing vague conclusory testimony, finding she “simply opined what a skilled artisan could accomplish.” *InTouch Techs., Inc. v. VGo Commc’ns, Inc*, 751 F.3d 1327, 1348-49 (Fed. Cir. 2014)
- *ActiveVideo* similarly involved conclusory assertions. *ActiveVideo Networks, Inc., v. Verizon Commc’n, Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012)
- The Belden court decided the Board satisfied the requirement to address not what a POSITA “could have” done but “would have been motivated” to do. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015)

’347 Reply, 14-15

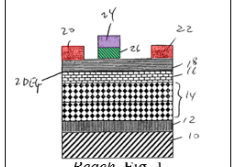
’347 Patent Ground 1: Saxler-Yoshida in view of Beach and Shenoy renders obvious claims 1-3

A POSITA would have combined Saxler (+Yoshida) Beach, and Shenoy to simplify the process and improve alignment

Target structure: Modified Saxler Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Beach’s Single Mask

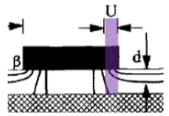


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

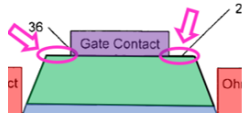
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Modified Saxler Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

C
Patent Owner irrelevantly argues Beach etches n-type materials when Saxler has p-type. ’347 POR, 39.
Patent Owner inaccurately argues Beach’s approach would “cut off” Saxler’s sloped sidewalls. ’347 POR, 38-39.

2. Beach’s self-aligned, single mask approach is compatible with Saxler’s etching

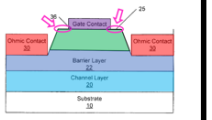
- **The combination relies on Beach for its use of a single mask to etch two layers, and it is irrelevant that Beach etches n-type materials.**
- **The combination would not “cut off” Saxler-Yoshida’s sloped sidewalls of the p-type GaN cap layer. The combination uses the same etching technique disclosed in Saxler to create sloped sidewalls when using Beach’s one-mask approach.**

’347 Pet. at 28-35; ’347 Reply 17-18.

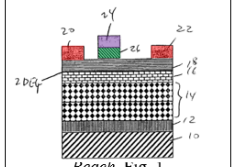
’347 Patent Ground 1: Saxler-Yoshida in view of Beach and Shenoy renders obvious claims 1-3

A POSITA would have combined Saxler (+Yoshida) Beach, and Shenoy to simplify the process and improve alignment

Target structure: Modified Saxler Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Beach’s Single Mask

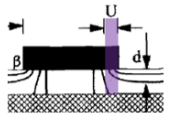


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

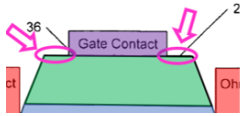
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



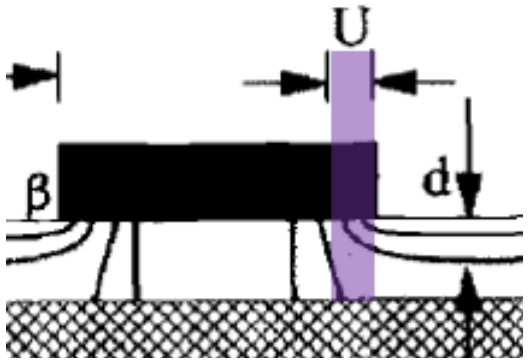
Shenoy, Fig. 1.

Modified Saxler Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

D
Patent Owner and Dr. Schubert incorrectly argue Shenoy’s undercut would etch the p-GaN layer. ’347 POR, 40-45.



Shenoy, Fig. 1.

’347 Pet. at 28-35, 57; ’347 Reply 3-12.

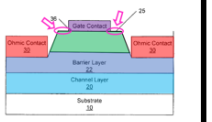
3. A POSITA would have used Shenoy’s approach to etch the metal and form Saxler-Yoshida’s structure

- **Dr. Schubert bases his opinion on the unsubstantiated belief that the p-GaN layer etches at the same rate as the gate metal. Ex. 2005, ¶ [174] (“the etching process proceeds in all directions at the same rate absent an insulator.”)**
- **His opinion is also premised on the incorrect statement that Saxler does not disclose passivating GaN material. Ex. 2005, ¶ [170].**
- **But Saxler repeatedly describes passivation. E.g., Saxler, Title, [0023]-[0025], [0067].**
- **Dr. Shealy explained the p-GaN material etches more slower than the gate metal, resulting in Saxler-Yoshida’s gate structure. Ex. 2004, 96:17-101:18.**

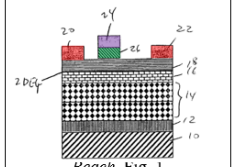
’347 Patent Grounds 1-2: Saxler (+Yoshida) renders obvious Claims 1-3

A POSITA would have combined Saxler (+Yoshida) Beach, and Shenoy to simplify the process and improve alignment

Target structure: Modified Saxler Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Beach’s Single Mask

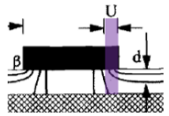


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

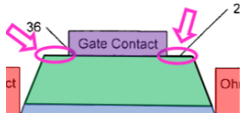
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Modified Saxler Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

Patent Owner’s Arguments Fail

All of Patent Owner’s Arguments Fail

A
The POR incorrectly contends the Petition did not provide the “specific process sequence” for the proposed combination. ’347 POR, 46.

B
Patent Owner misunderstands obviousness, citing inapposite case law to c… motivation to … and Shenoy … Saxler-Yoshida … 47.

C
Patent Owner irrelevantly argues Beach etches n-type materials when Saxler has p-type. ’347 POR, 39. … inaccurately

D
Patent Owner and Dr. Schubert incorrectly argue Shenoy’s undercut would etch the p-GaN layer. ’347 POR, 40-45.

At Institution, the Board found Saxler-Yoshida with Beach and Shenoy would have resulted in a self-aligned method. ’347 ID, 36.

’347 Pet., 25-26, 35-36; ’347 Reply, 2-11.; ’347 Shealy, [090]-[091], [108]-[109], [122]; Ex. 2004, 31:1-20, 37:7-21.

’347 Patent Ground 3: Saxler and Ahn Render Obvious Claims 1-3

Innoscience

Saxler Grounds

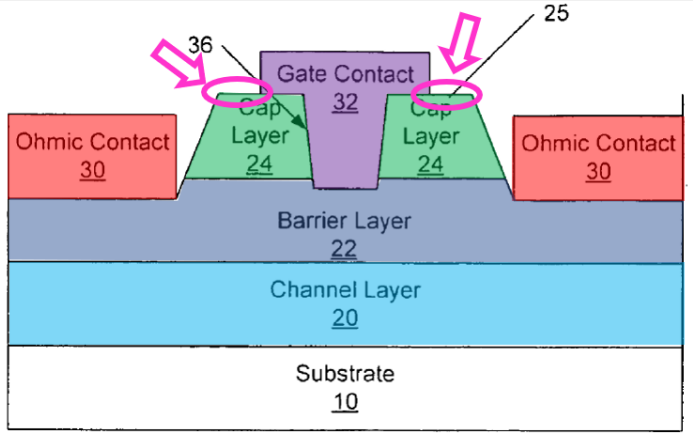
Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103	*Saxler*, *Beach*, and *Shenoy*
2	1-3	§ 103	*Saxler*, *Yoshida*, *Beach*, and *Shenoy*
3	1-3	§ 103	*Saxler* and *Ahn*
4	1-3	§ 103	*Yoshida*, *Saxler*, *Beach*, and *Shenoy*
5	1-3	§ 103	*Yoshida* and *Ahn*

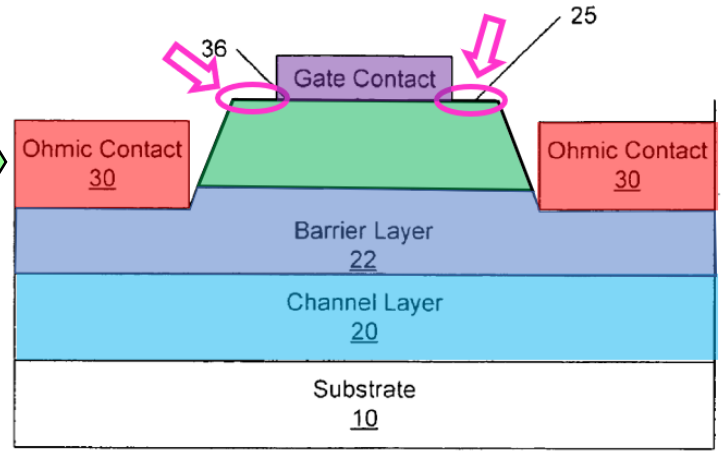
’347 Patent Ground 3: Saxler and Ahn Render Obvious Claims 1-3

Innoscience

Saxler depicts a depletion mode device with a recessed gate



Target Structure: Saxler-Yoshida
A POSITA would have removed Saxler’s recess based on Saxler’s express teachings and to achieve the benefits of an enhancement mode device.



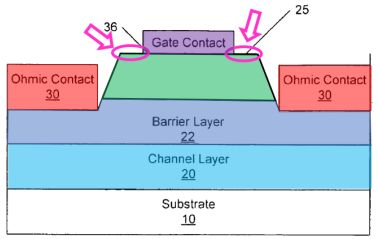
’347 Pet., 60-72.

Innoscience

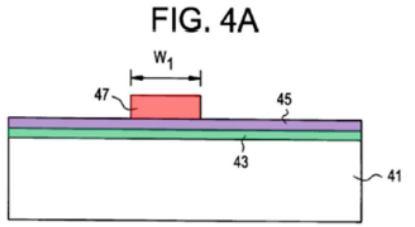
A POSITA would have made Saxler’s modified Fig. 1A using Ahn’s approach to simplify and improve alignment

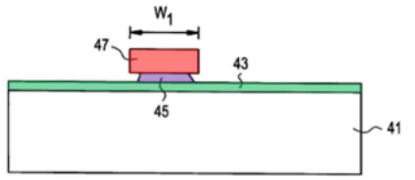
Target structure: Saxler’s modified Fig. 1A

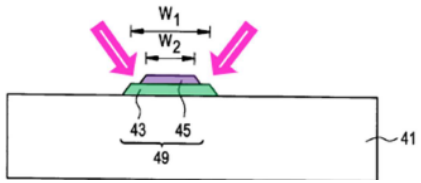
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Ahn’s approach

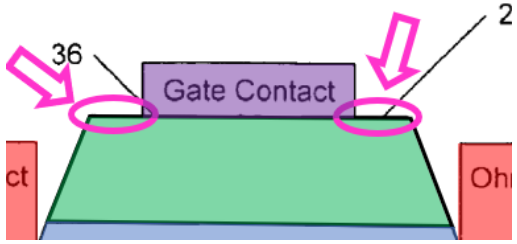






Ahn, Figs. 4A-4C.

Saxler’s modified Fig. 1A Gate Structure



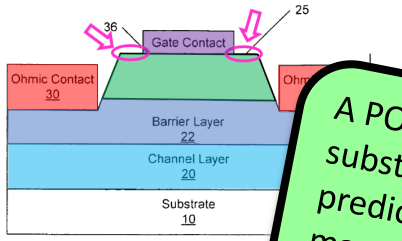
Saxler, Fig. 1A (modified).

’347 Pet., 60-72.

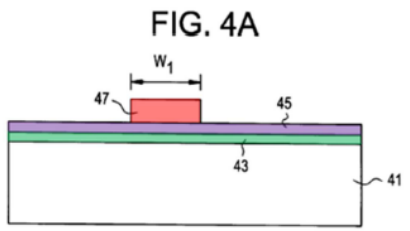
A POSITA would have made Saxler’s modified Fig. 1A using Ahn’s approach to simplify and improve alignment

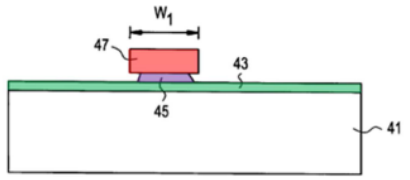
Target structure: Saxler’s modified Fig. 1A

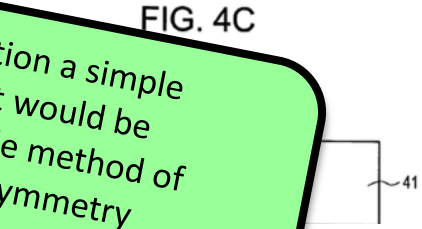
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device



Ahn’s approach

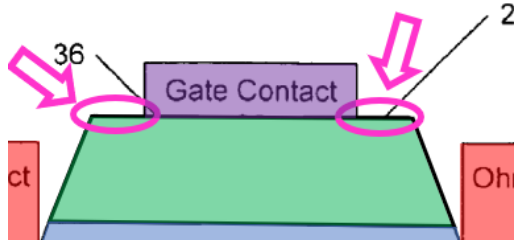






A POSITA would have found the combination a simple substitution of Ahn’s known methods that would be predictably implemented in Saxler’s flexible method of manufacturing to improve alignment and symmetry between layers while reducing manufacturing steps and costs.

Saxler’s modified Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

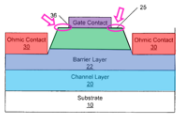
At Institution, the Board found the combinations with Ahn would have resulted in a self-aligned method. ’347 ID, 50-51.

’347 Pet., 60-72.

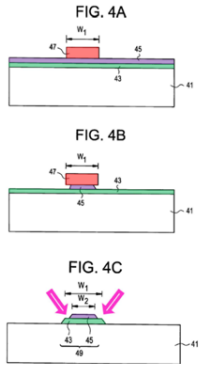
’347 Patent Ground 3: Saxler and Ahn Render Obvious Claims 1-3

A POSITA would have made Saxler’s modified Fig. 1A using Ahn’s approach to simplify and improve alignment

Target structure: Saxler’s modified Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device

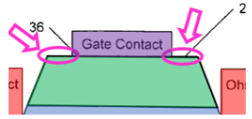


Ahn’s approach



Ahn, Figs. 4A-4C.

Saxler’s modified Fig. 1A Gate Structure



Saxler, Fig. 1A (modified).

Patent Owner’s Arguments Fail

A
Patent Owner’s misplaced criticism that Saxler is in a different field of endeavor and not a “thin film transistor” fails.

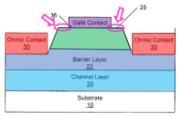
B
Patent Owner incorrectly argues Ahn’s method does not apply to Saxler.

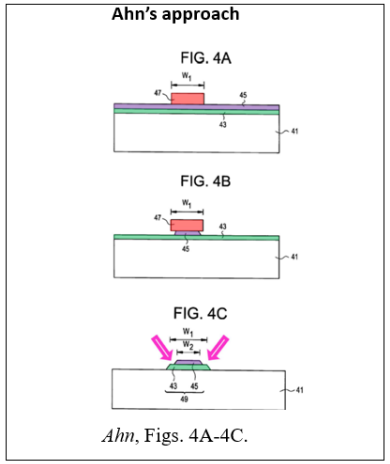
’347 Pet., 60-72; ’347 Reply, 21-23.

’347 Patent Ground 3: Saxler and Ahn Render Obvious Claims 1-3

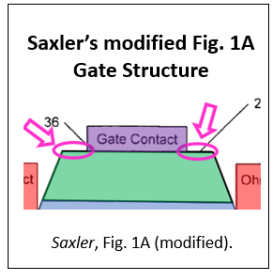
A POSITA would have made Saxler’s modified Fig. 1A using Ahn’s approach to simplify and improve alignment

Target structure: Saxler’s modified Fig. 1A
A POSITA would have removed Saxler’s recess to achieve the benefits of an enhancement mode device





Ahn, Figs. 4A-4C.



Saxler, Fig. 1A (modified).

Ahn’s approach simplifies Saxler’s methods and improves alignment and symmetry

The ’347 patent “generally relates to transistors,” including “heterojunction field effect transistors (HFET), high electron mobility transistors (HEMT), or modulation doped field effect transistors (MODFET).” ’347 patent, 1:20-58; ’347 Reply 26-28. Ahn relates to “thin-film” transistors, which also generally relates to transistors. Saxler relates to GaN HEMTs. Saxler, Abstract.

Ahn and Saxler thus both fall into this same field of endeavor. ’347 Pet., 60-64; ’347 Reply 26-28.

A Patent Owner’s misplaced criticism that Saxler is in a different field of endeavor and not a “thin film transistor” fails.

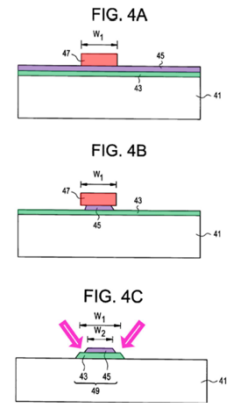
The Pre-Institution Petitioner’s Preliminary Reply showed *Ahn* is analogous art—it is in the same field of endeavor as and reasonably pertinent to the problem of the ’347 Patent. Paper No. 8.

’347 Pet., 60-72; ’347 Reply, 21-23.

’347 Patent Ground 3: Saxler and Ahn Render Obvious Claims 1-3

Innoscience

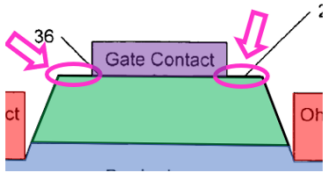
Ahn’s approach



Ahn, Figs. 4A-4C.

The Combination of Saxler and Ahn

Saxler’s Gate Structure



Saxler, Fig. 1A (modified).

Ahn’s approach simplifies Saxler’s methods and improves alignment and symmetry

Ahn discloses dry etching both layers under a single mask, then wet etching to undercut the top layer. Reply, 22-23; Ahn, 7:7-14; Shealy, [175]; Petition, 63-64.

Dr. Shealy explained the same approach would create Saxler’s gate structure because its cap layer would dissolve more slowly than its gate metal during the und. Reply, 22-23; Petition, 63-64; Shealy [174]-[175]; Ex. 2004, 96:17-101:18.

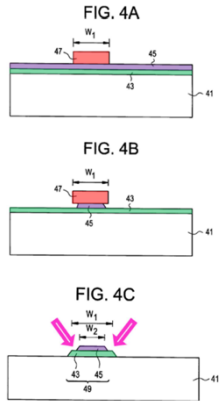
B
Patent Owner incorrectly argues Ahn’s method does not apply to Saxler.

’347 Pet., 60-72; ’347 Reply, 21-23.

’347 Patent Ground 3: Saxler and Ahn Render Obvious Claims 1-3

Innoscience

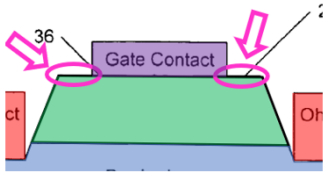
Ahn’s approach



Ahn, Figs. 4A-4C.

The Combination of Saxler and Ahn

Saxler’s Gate Structure



Saxler, Fig. 1A (modified).

Patent Owner’s Arguments Fail

All of Patent Owner’s Arguments Fail

A
Patent Owner’s misplaced criticism that Saxler is in a different field of endeavor and not a “thin film transistor” fails.

B
Patent Owner incorrectly argues Ahn’s method does not apply to Saxler.

’347 Pet., 60-72; ’347 Reply, 21-23.

’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

Innoscience

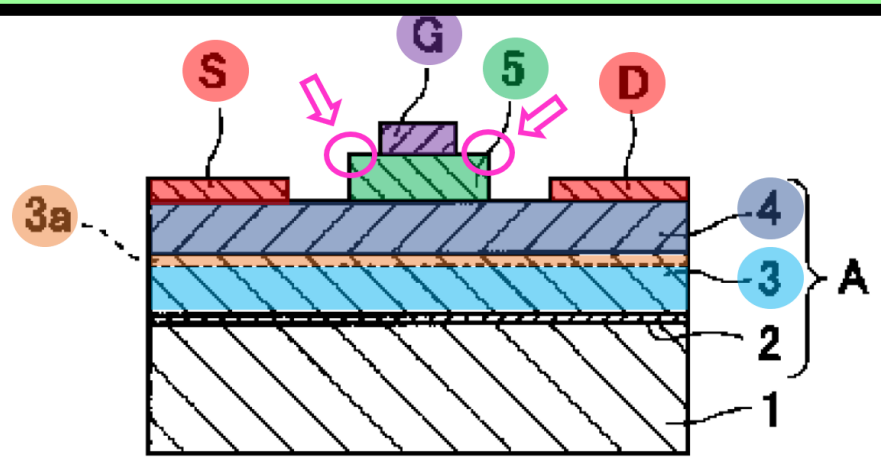
Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103	*Saxler*, *Beach*, and *Shenoy*
2	1-3	§ 103	*Saxler*, *Yoshida*, *Beach*, and *Shenoy*
3	1-3	§ 103	*Saxler* and *Ahn*
4	1-3	§ 103	*Yoshida*, *Saxler*, *Beach*, and *Shenoy*
5	1-3	§ 103	*Yoshida* and *Ahn*

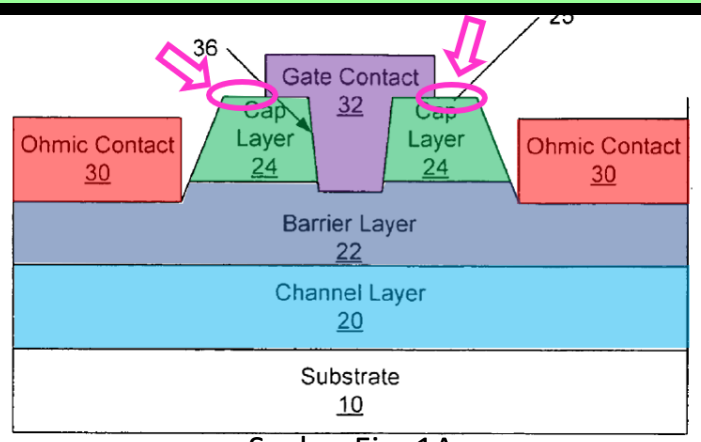
’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

Yoshida depicts an enhancement mode device with every feature but the horizontally extended sidewalls in its p-GaN layer, which would have been present in practice



Yoshida, Fig. 1.

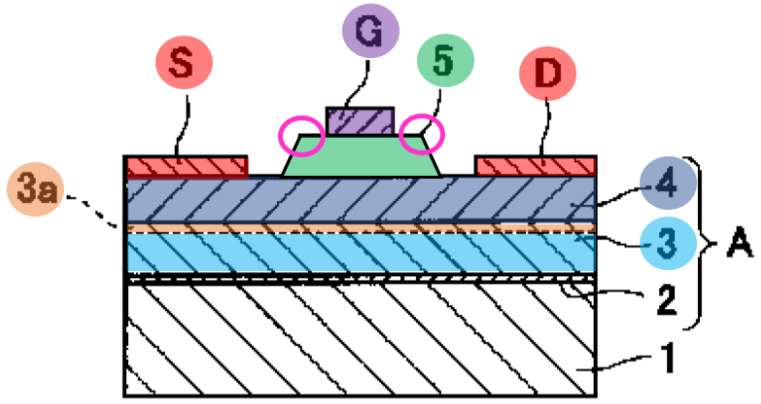
Saxler discloses etching sloped sidewalls for its p-GaN cap layer



Saxler, Fig. 1A.

’347 Pet., 72-80.

Target structure: Saxler-Yoshida
A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage

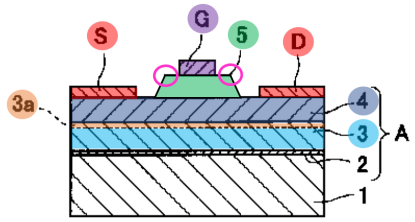


Yoshida, Fig. 1 (modified).

’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

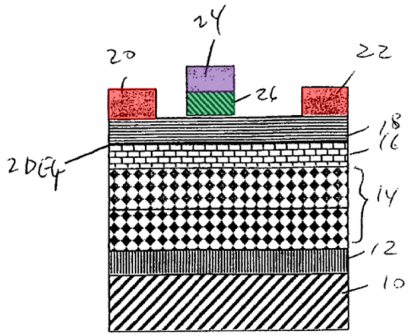
Target structure: Yoshida-Saxler

A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage



A POSITA would have combined Yoshida, Saxler, Beach, and Shenoy to simplify Yoshida-Saxler’s process and improve alignment

Beach’s Single Mask

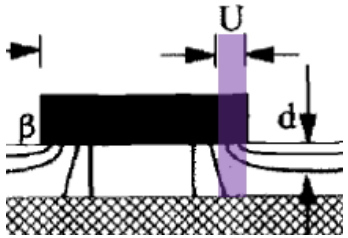


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

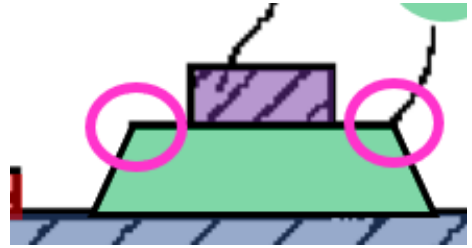
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Yoshida-Saxler’s Gate Structure



Yoshida, Fig. 1 (modified).

’347 Pet., 72-80; ’347 Reply, 23-26.

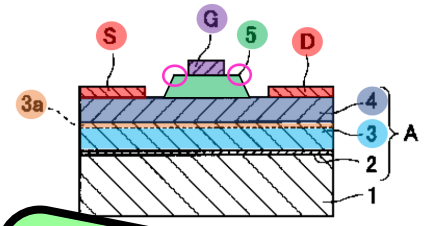
’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

Innoscience

A POSITA would have combined Yoshida, Saxler, Beach, and Shenoy to simplify Yoshida-Saxler’s process and improve alignment

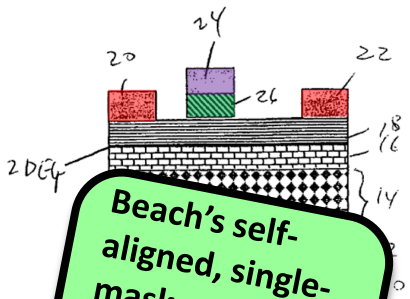
Target structure: Yoshida-Saxler

A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage



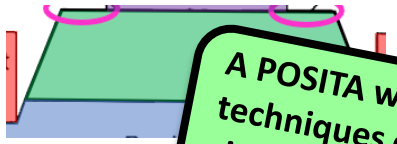
The Board correctly noted Yoshida has a flexible fabrication method. ’347 ID, 50.

Beach’s Single Mask



Beach’s self-aligned, single-mask approach is compatible with Saxler’s etching

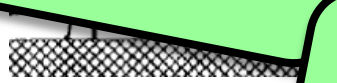
with Saxler’s etching to create sloped sidewalls



Saxler, Fig.

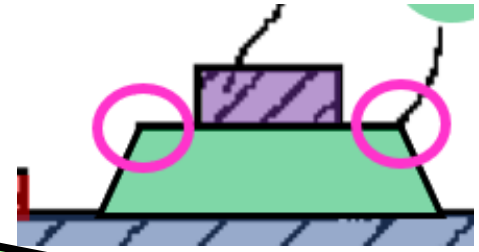
Shenoy’s Undercut

POSITA would have used Shenoy’s approach to etch the metal and form Yoshida-Saxler’s structure



Shenoy, Fig. 1.

Yoshida-Saxler’s Gate Structure



(modified).

A POSITA would have used the known techniques of Beach and Shenoy to simplify Yoshida-Saxler’s process—they are suitable options.

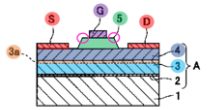
At Institution, the Board found the combinations with Beach and Shenoy would have resulted in a self-aligned method. ’347 ID, 36.

’347 Pet., 72-80; ’347 Reply, 23-26.

’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

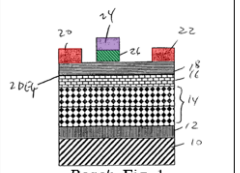
Innoscience

Target structure: Yoshida-Saxler
A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage



A POSITA would have combined Yoshida, Saxler, Beach, and Shenoy to simplify Yoshida-Saxler’s process and improve alignment

Beach’s Single Mask

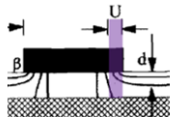


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

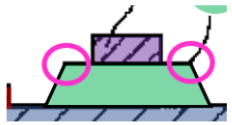
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Yoshida-Saxler’s Gate Structure



Yoshida, Fig. 1 (modified).

Patent Owner’s Three Arguments Fail

A
Patent Owner misunderstands obviousness, arguing “there would be no motivation to apply the ‘self-aligned technique of Beach” because Yoshida is allegedly specific in its masking and etching. ’347 POR, 55-56.

B
Patent Owner incorrectly argues Yoshida “teaches away” from the combination. ’347 POR, 56-57.

C
Patent Owner incorrectly alleges the Yoshida is a “gate-last” approach and the combination adds steps. POR, 5761.

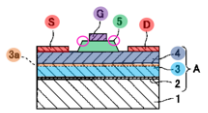
’347 Pet., 72-80; ’347 Reply, 23-26.

’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

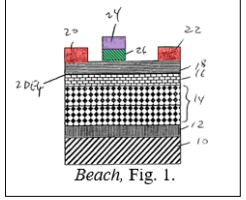
Innoscience

A POSITA would have combined Yoshida, Saxler, Beach, and Shenoy to simplify Yoshida-Saxler’s process and improve alignment

Target structure: Yoshida-Saxler
A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage



Beach’s Single Mask

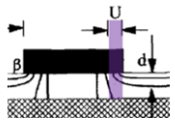


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

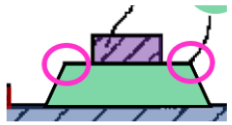
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Yoshida-Saxler’s Gate Structure



Yoshida, Fig. 1 (modified).

Beach and Shenoy’s approach simplifies Yoshida’s methods and improves alignment and symmetry

~~Due to this specificity in order, processes and explicitly expressed desire to achieve enhancement mode GaN transistors with sufficient electron mobility, a POSA would recognize that Yoshida’s method is *not* flexible. EX2005 ¶259.~~

’347 POR, 45

A Patent Owner misunderstands obviousness, arguing “there would be no motivation to apply the ‘self-aligned technique of Beach” because Yoshida is allegedly specific. ’347 POR, 55-56.

The Board correctly noted Yoshida has a flexible fabrication method. ’347 ID, 50.

KSR rejected Patent Owner’s rigid understanding that Yoshida’s gate formation is “specific” so a POSITA would not seek to change it. ’347 POR, 55-56; *KSR,* 550 U.S. at 418 (obviousness accounts for “inferences and creative steps”), 422 (A POSITA “is also a person of ordinary creativity, not an automaton.”).

A POSITA would have formed Yoshida’s gate “in any order” because a POSITA would have possessed ordinary creativity. Ex. 2004, 76:24-77:1; Shealy, [204]-[205]; KSR, 550 U.S. at 418, 422

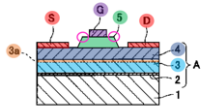
’347 Pet., 72-80; ’347 Reply, 23-26.

’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

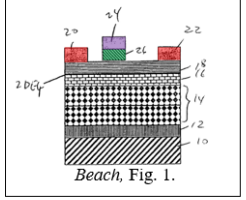
Innoscience

A POSITA would have combined Yoshida, Saxler, Beach, and Shenoy to simplify Yoshida-Saxler’s process and improve alignment

Target structure: Yoshida-Saxler
A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage



Beach’s Single Mask

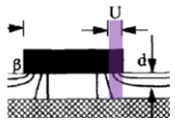


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

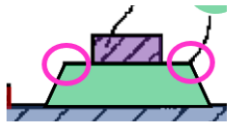
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Yoshida-Saxler’s Gate Structure



Yoshida, Fig. 1 (modified).

Yoshida does not teach away from alternative fabrication methods.

~~B. Yoshida teaches away from using other methods of manufacturing its gate~~

’347 POR, 56-57

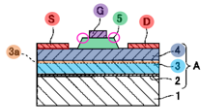
B
Patent Owner incorrectly argues Yoshida “teaches away” from the combination. ’347 POR, 56-57.

- Yoshida’s improvements arise from its structure, not its fabrication methods. Yoshida, [0009] (“Means for Solving the Problems”).
- Yoshida mentions “conventional photolithography and etching” but never disparages this approach—it even ***uses*** this approach. Yoshida, [0006], [0022].
- “[A] reference does not teach away if it ‘merely expresses a general preference for an alternative invention but does not criticize, discredit or otherwise discourage investigation into the invention claimed.” *UCB, Inc. v. Actavis Laby’s UT, Inc.*, 65 F.4th 679, 692 (Fed. Cir. 2023))

’347 Pet., 72-80; ’347 Reply, 23-26.

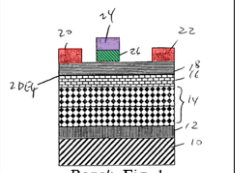
’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

Target structure: Yoshida-Saxler
A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage



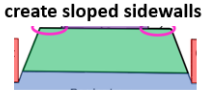
A POSITA would have combined Yoshida, Saxler, Beach, and Shenoy to simplify Yoshida-Saxler’s process and improve alignment

Beach’s Single Mask



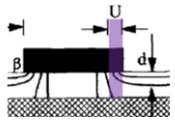
Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls



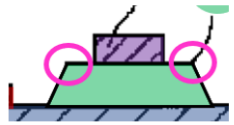
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Yoshida-Saxler’s Gate Structure



Yoshida, Fig. 1 (modified).

Yoshida’s gate structure can be made in any order

Yoshida specifies ***no order*** of gate and ohmic contact formation (Yoshida, [0022]), and it teaches ***finishing the gate before the ohmic contacts***. Ex. 2004, 76:1-80:16; Shealy, [204].

A POSITA would have formed Yoshida’s gate “in any order” because a POSITA would have possessed ordinary creativity. Ex. 2004, 76:24-77:1; Shealy, [204]-[205]; *KSR*, 550 U.S. at 418, 422.

C
Patent Owner incorrectly alleges the Yoshida is a “gate-last” approach and the combination adds steps. POR, 5761.

’347 Pet., 72-80; ’347 Reply, 23-26.

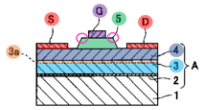
’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

Innoscience

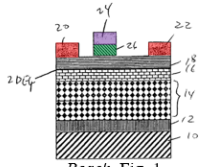
A POSITA would have combined Yoshida, Saxler, Beach, and Shenoy to simplify Yoshida-Saxler’s process and improve alignment

Target structure: Saxler-Yoshida

A POSITA would have implemented Saxler’s known option to etch sloped sidewalls in the p-GaN layer to reduce gate leakage



Beach’s Single Mask

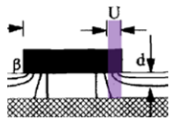


Beach, Fig. 1.

with Saxler’s etching to create sloped sidewalls

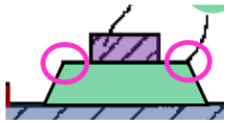
Saxler, Fig. 1A (modified).

Shenoy’s Undercut



Shenoy, Fig. 1.

Yoshida-Saxler’s Gate Structure



Yoshida, Fig. 1 (modified).

Patent Owner’s Three Arguments Fail

All of Patent Owner’s Arguments Fail

~~Patent Owner misunderstands obviousness, arguing “there would be no motivation to apply the ‘self-aligned technique of Beach” because “Yoshida is “specific”. ’347 POR, 55-56.~~

~~Patent Owner incorrectly argues Yoshida “teaches away” from the combination. ’347 POR, 56-57.~~

~~Patent Owner incorrectly alleges the Yoshida is a “gate-last” approach and the combination adds steps. POR, 5761.~~

’347 Pet., 72-80; ’347 Reply, 23-26.

’347 Patent Ground 5: Yoshida and Ahn Render Obvious Claims 1-3

Innoscience

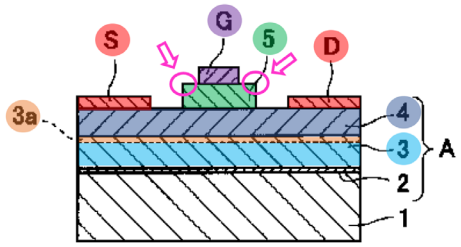
Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103	*Saxler*, *Beach*, and *Shenoy*
2	1-3	§ 103	*Saxler*, *Yoshida*, *Beach*, and *Shenoy*
3	1-3	§ 103	*Saxler* and *Ahn*
4	1-3	§ 103	*Yoshida*, *Saxler*, *Beach*, and *Shenoy*
5	1-3	§ 103	*Yoshida* and *Ahn*

A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.

Target structure:
Yoshida’s Device



Yoshida, Fig. 1.

Ahn’s approach

FIG. 4A

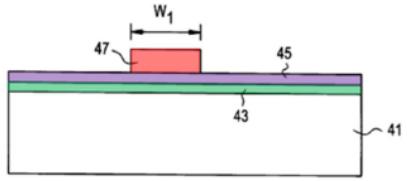


FIG. 4B

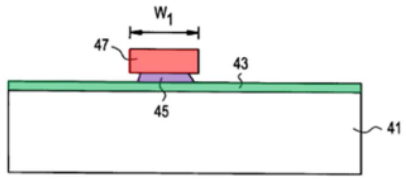
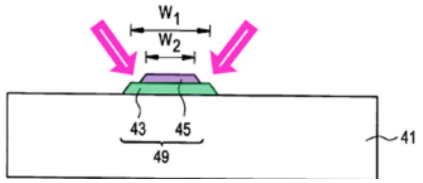
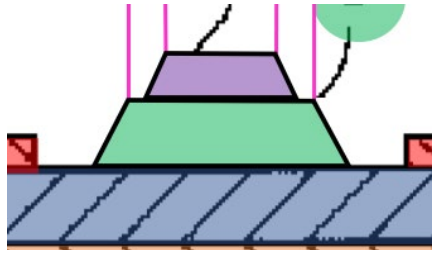


FIG. 4C



Ahn, Figs. 4A-4C.

Yoshida’s Gate Structure



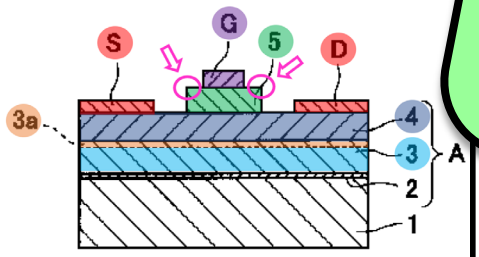
Yoshida, Fig. 1 (modified).

’347 Pet., 95-106; ’347 Reply, 26-28.

Innoscience

A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.

Target structure:
Yoshida’s Device

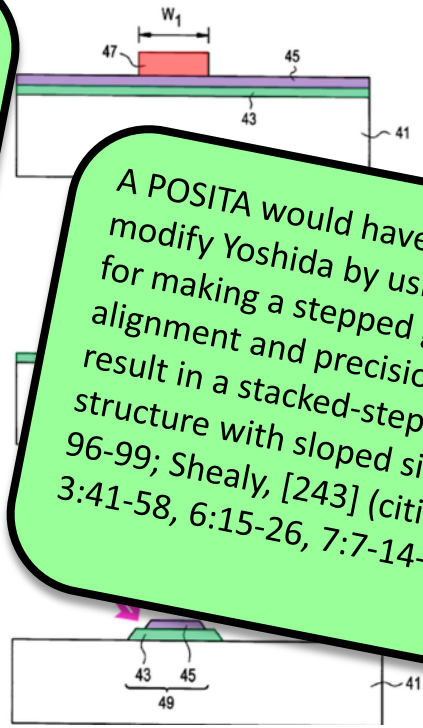


Yoshida, Fig. 1.

Ahn discloses dry etching both gate layers under a single mask, then wet etching to undercut the top layer, which would result in Yoshida’s structure. 347 Pet., 98; Ahn, 7:7-14; Shealy, [242]-[243].

Ahn’s approach

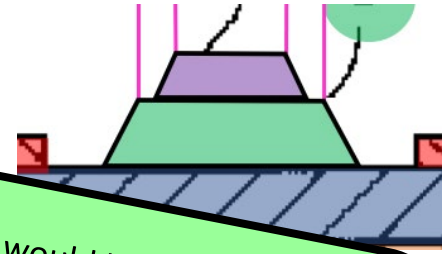
FIG. 4A



Ahn, Figs. 4A-4C.

A POSITA would have found it obvious to modify Yoshida by using Ahn’s approach for making a stepped gate to improve alignment and precision, which would result in a stacked-stepped gate structure with sloped sidewalls. ’347 Pet. 96-99; Shealy, [243] (citing *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C).

Yoshida’s Gate Structure



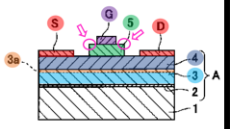
A POSITA would have found the combination a simple substitution of Ahn’s known methods that would be predictably implemented when making Yoshida’s device to improve alignment and symmetry between layers. Shealy, [244].

’347 Pet., 95-106; ’347 Reply, 26-28.

’347 Patent Ground 5: Yoshida and Ahn Render Obvious Claims 1-3

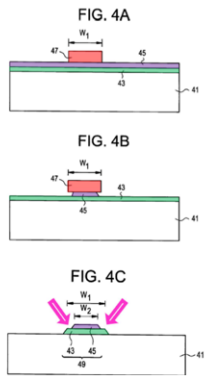
A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.

Target structure:
Yoshida’s Device



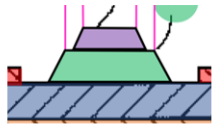
Yoshida, Fig. 1.

Ahn’s approach



Ahn, Figs. 4A-4C.

Yoshida’s Gate Structure



Yoshida, Fig. 1 (modified).

Patent Owner’s Four Arguments Fail

A
Patent Owner incorrectly alleges the Petition did not specify how to combine Yoshida and Ahn. ’347 POR, 63-66.

B
Patent Owner’s misplaced criticism that Yoshida is in a different field of endeavor and not a “thin film transistor” fails. ’347 POR, 67-69.

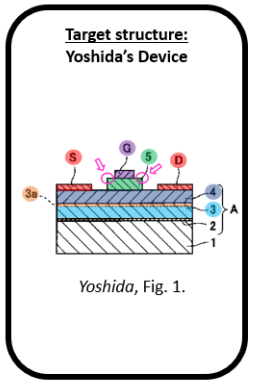
C
Patent Owner incorrectly argues Ahn’s method does not apply to Yoshida. POR, ’347 63-64, 67-69.

D
Patent Owner’s irrationally argues Yoshida already discloses symmetric ledges so has no reason to improve alignment and precision. ’347 POR, 65-66.

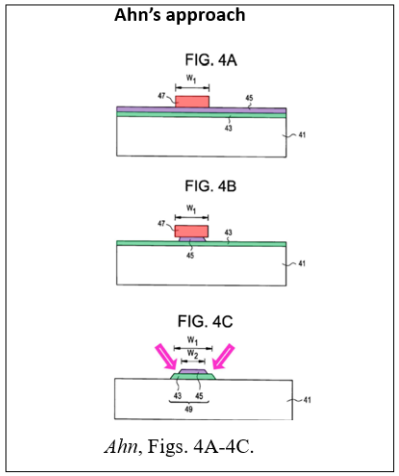
’347 Pet., 95-106; ’347 Reply, 26-28.

’347 Patent Ground 5: Yoshida and Ahn render obvious Claims 1-3

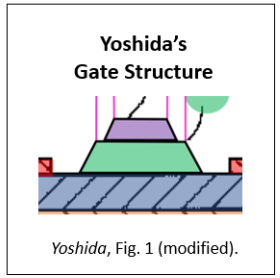
A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.



Yoshida, Fig. 1.



Ahn, Figs. 4A-4C.



Yoshida, Fig. 1 (modified).

The combination calls for using Ahn’s masking and etching to make Yoshida’s gate structure

A Patent Owner incorrectly alleges the Petition did not specify how to combine Yoshida and Ahn. ’347 POR, 63-66.

The Petition explained a POSITA would have implemented Ahn’s known masking and etching methods to make Yoshida’s gate structure

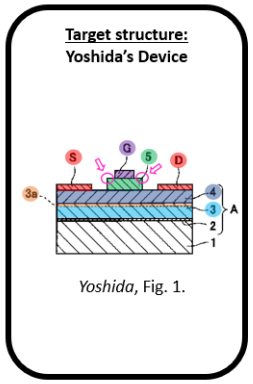
Ahn teaches many ways to obtain the *Yoshida* gate structure, including etching both simultaneously or etching them sequentially using combinations of conventional wet and dry etching techniques. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C; Shealy, [244]. For example, *Ahn* exploits differences between rates of dissolution of its layers to make the top gate layer narrower than the bottom. *Ahn*, 7:7-14-46; Shealy, [244]. A POSITA would have understood that *Yoshida*’s layer 5, which was a p-type doped semiconductor, would have had a slower rate of dissolution than its metallic gate contact and found it obvious to use *Ahn*’s approach. Shealy, [244]. *Ahn’s* methods result in symmetrically aligned layers. *Ahn*, 6:15-37, Fig. 4C; Shealy, [244]. A POSITA would have found the combination a simple substitution of *Ahn*’s known methods that would be predictably implemented when making *Yoshida*’s device to improve alignment and symmetry between layers. Shealy, [244].

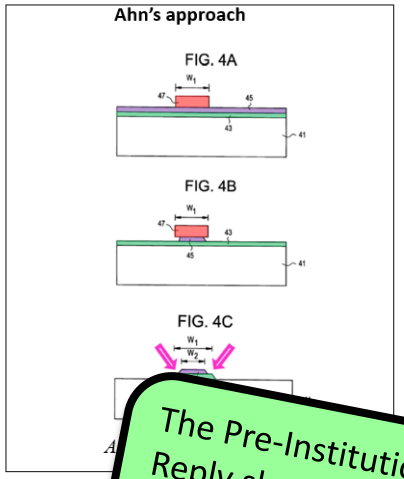
’347 Pet., 98-99

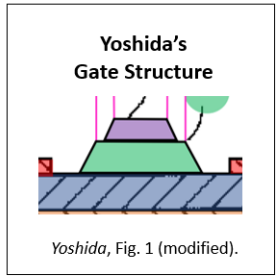
’347 Pet., 95-106; ’347 Reply, 26-28.

’347 Patent Ground 5: Yoshida and Ahn render obvious Claims 1-3

A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.







Ahn’s approach simplifies Yoshida’s methods and improves alignment and symmetry

The ’347 patent “generally relates to transistors,” including “heterojunction field effect transistors (HFET), high electron mobility transistors (HEMT), or modulation doped field effect transistors (MODFET).” ’347 patent, 1:20-58; ’347 Reply 26-28. Ahn relates to “thin-film” transistors, which also generally relates to transistors. Ahn, 1:1-10. Yoshida relates to GaN HEMTs. Yoshida, Abstract.

Ahn and Yoshida thus both fall into this same field of endeavor. ’347 Pet., 97-99; ’347 Reply 26-28.

The Pre-Institution Petitioner’s Preliminary Reply showed *Ahn* is analogous art—it is in the same field of endeavor as and reasonably pertinent to the problem of the ’347 Patent. Paper No. 8.

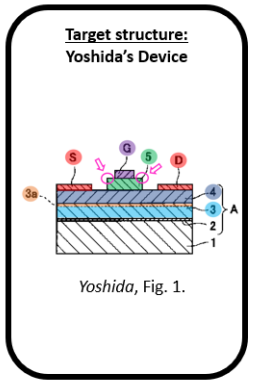
B
Patent Owner’s misplaced criticism that Yoshida is in a different field of endeavor and not a “thin film transistor” fails. ’347 POR, 67-69.

Patent Owner presents the same flawed argument as with Saxler and Ahn (Ground 3).

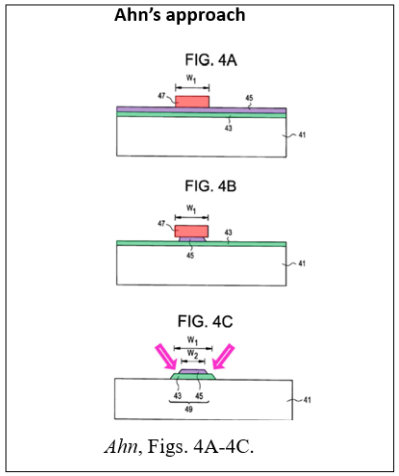
’347 Pet., 95-106; ’347 Reply, 26-28.

’347 Patent Ground 5: Yoshida and Ahn render obvious Claims 1-3

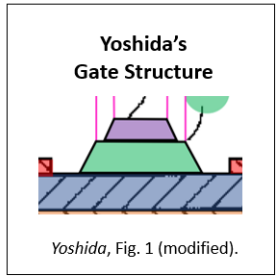
A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.



Yoshida, Fig. 1.



Ahn, Figs. 4A-4C.



Yoshida, Fig. 1 (modified).

Ahn’s approach simplifies Saxler’s methods and improves alignment and symmetry

Ahn discloses dry etching both layers under a single mask, then wet etching to undercut the top layer. ’347 Reply, 26-28; Ahn, 7:7-14; ’347 Pet., 97-99; ’347 Shealy, [241]-[244].

The same approach would create Saxler’s gate structure because its cap layer would dissolve more slowly than its gate metal. ’347 Reply, 26-28; ’347 Pet., 97-99; ’347 Shealy, [241]-[244]; Ex. 2004, 96:17-101:18.

C
Patent Owner incorrectly argues Ahn’s method does not apply to Yoshida. POR, ’347 63-64, 67-69.

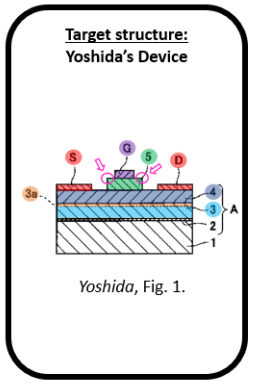
Patent Owner presents the same flawed argument as with Saxler and Ahn (Ground 3).

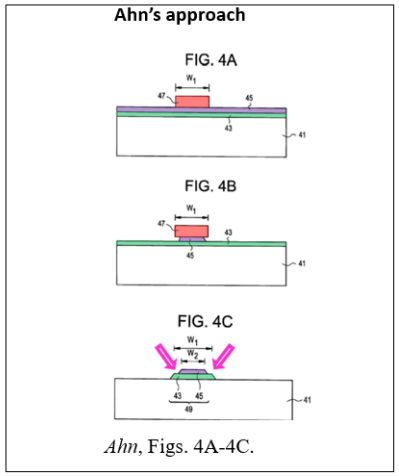
’347 Pet., 95-106; ’347 Reply, 26-28.

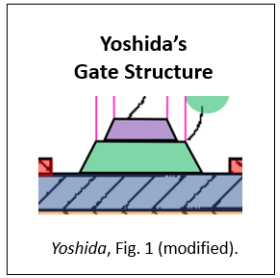
’347 Patent Ground 5: Yoshida and Ahn render obvious Claims 1-3

Innoscience

A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.







A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.

Ex. 1002, 29, 55. But *Ahn* would have provided a known and obvious way to create that same structure for *Yoshida*’s device. Shealy, [243]. A POSITA would have found it obvious to modify *Yoshida* by using *Ahn*’s approach for making a stepped gate in a thin-film transistor to improve alignment and precision, which would result in a stacked-stepped gate structure with sloped sidewalls. Shealy, [243] (citing *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C).

’347 Pet., 98

D
Patent Owner’s irrationally argues Yoshida already discloses symmetric ledges so has no reason to improve alignment and precision. ’347 POR, 65-66.

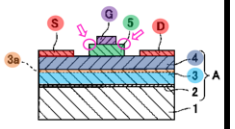
The Petition reasoned Ahn provided a known and obvious way to make Yoshida’s device—it is a suitable option. ’347 Pet., 98; ’347 Shealy, [243].

’347 Pet., 95-106; ’347 Reply, 26-28.

’347 Patent Ground 4: Yoshida-Saxler in view of Beach and Shenoy renders obvious claims 1-3

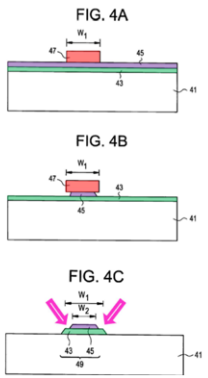
A POSITA would have combined Yoshida and Ahn to improve alignment and precision when making Yoshida’s gate structure.

Target structure:
Yoshida’s Device



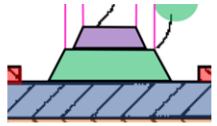
Yoshida, Fig. 1.

Ahn’s approach



Ahn, Figs. 4A-4C.

Yoshida’s Gate Structure



Yoshida, Fig. 1 (modified).

Patent Owner’s Four Arguments Fail

All of Patent Owner’s Arguments Fail

~~**A**~~
~~**Patent Owner incorrectly alleges the Petition did not specify how to combine Yoshida and Ahn. ’347 POR, 63-66.**~~

~~**B**~~
~~**Patent Owner’s misplaced criticism that Yoshida is in a different field of endeavor and not a “thin film transistor” fails. ’347 POR, 67-69.**~~

~~**C**~~
~~**Patent Owner incorrectly argues Ahn’s method does not apply to Yoshida. POR, ’347 63-64, 67-69.**~~

~~**D**~~
~~**Patent Owner’s irrationally argues Yoshida already discloses symmetric ledges so has no reason to improve alignment and precision. ’347 POR, 65-66.**~~

’347 Pet., 95-106; ’347 Reply, 26-28.

’347 Patent: All claims invalid

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Saxler Grounds

Yoshida Grounds

Ground	Challenged Claims	Basis	Prior Art	
1	1-3	§ 103	*Saxler*, *Beach*, and *Shenoy*	All Claims Invalid
2	1-3	§ 103	*Saxler*, *Yoshida*, *Beach*, and *Shenoy*	All Claims Invalid
3	1-3	§ 103	*Saxler* and *Ahn*	All Claims Invalid
4	1-3	§ 103	*Yoshida*, *Saxler*, *Beach*, and *Shenoy*	All Claims Invalid
5	1-3	§ 103	*Yoshida* and *Ahn*	All Claims Invalid

’335 and ’347 Patents: All claims invalid

Innoscience

Saxler Grounds

Yoshida Grounds

Ground	’335 Patent Challenged Claims	Basis	Prior Art
1	1-7	§ 103	**Saxler** in view of the knowledge of a POSITA
2	1-7	§ 103	**Saxler** in view of Yoshida
3	2, 5-7	§ 103	**Saxler** in view of Yoshida, Beach, and Shenoy
4	1-7	§ 103	**Yoshida** in view of the knowledge of a POSITA
5	1-7	§ 103	**Yoshida** in view of Saxler
6	2, 5-7	§ 103	**Yoshida** in view of Saxler, Beach, and Shenoy

All Claims Invalid

All Claims Invalid

Claims Invalid

All Claims Invalid

All Claims Invalid

Claims Invalid

Saxler Grounds

Yoshida Grounds

Ground	’347 Patent Challenged Claims	Basis	Prior Art
1	1-3	§ 103	*Saxler*, *Beach*, and *Shenoy*
2	1-3	§ 103	*Saxler*, *Yoshida*, *Beach*, and *Shenoy*
3	1-3	§ 103	*Saxler* and *Ahn*
4	1-3	§ 103	*Yoshida*, *Saxler*, *Beach*, and *Shenoy*
5	1-3	§ 103	*Yoshida* and *Ahn*

All Claims Invalid

All Claims Invalid

All Claims Invalid

All Claims Invalid

All Claims Invalid