

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01384
Patent 10,312,335 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Innoscence (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc., (collectively “Petitioner”) filed a Petition for an *inter partes* review (Paper 1 (“Pet.”)) challenging claims 1–7 of U.S. Patent No. 10,312,335 B2 (Ex. 1001 (“the ’335 Patent”)). Efficient Power Conversion Corporation (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). After receiving authorization from the Board, Petitioner filed a Reply to the Preliminary Response (Paper 8) and Patent Owner filed a Sur-reply (Paper 10).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons set forth below, we determine the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we institute an *inter partes* review.

B. *Related Matters*

The parties identify two matters involving the ’335 patent: *Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd*, 2:23-cv-04026-AB-AS (C.D. Cal. May 24, 2023) and *In the Matter of Certain Semiconductor Devices, and Methods of Manufacturing Same and*

C. The '335 Patent (Ex. 1001)

The '335 patent, titled “Gate with Self-aligned Ledge for Enhancement Mode GaN Transistors,” issued June 4, 2019, and is directed to “[a]n enhancement-mode GaN transistor with reduced gate leakage current between a gate contact and a [two-dimensional electron gas (2DEG)] region and a method for manufacturing the same.” Ex. 1001, codes (45), (54), (57).

The '335 patent explains that “GaN semiconductor devices are increasingly desirable because of their ability to switch at high frequency, to carry large current, and to support high voltages.” Ex. 1001, 1:30–32. Devices developed for high power/high frequency applications are based on structures that exhibit high electron mobility and are referred to as, *inter alia*, high electron mobility transistors (HEMT). Ex. 1001, 1:32–39. GaN HEMT devices typically include a nitride semiconductor with at least two nitride layers. Ex. 1001, 1:42–43. Different materials (e.g., AlGaN and GaN) on the semiconductor cause adjacent layers to have different band gaps and also cause polarization, which contributes to a conductive 2DEG region near the junction of the two layers, and allows charge to flow through the device. Ex. 1001, 1:43–53.

The '335 patent further explains that:

Because the 2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices. If the 2DEG region is depleted (*i.e.*, removed) below the gate at zero applied gate bias, the device can be an enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide and because they are easier to control with simple, low cost drive circuits. An

enhancement mode device requires a positive bias applied at the gate in order to conduct current.

Ex. 1001, 1:54–63.

Figure 2 of the '335 patent, reproduced below, depicts a prior art enhancement-mode GaN transistor.

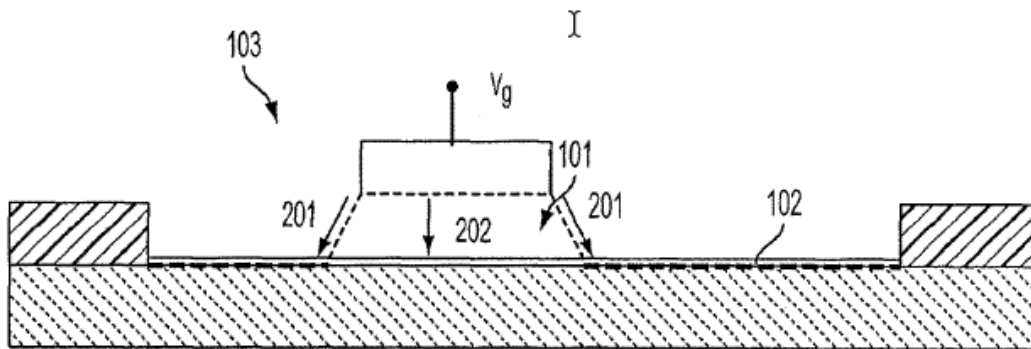


Figure 2 depicts a conventional enhancement-mode GaN transistor having gate 103 comprising p-type material 101, and a 2DEG region 102 under gate 103, with two gate leakage current paths 201 and 202. Ex. 1001, 1:64–2:8. According to the '335 patent, the gate leakage current is predominantly along gate edge path 201. Ex. 1001, 2:20–26.

The '335 patent depicts an embodiment of the claimed invention in Figure 5, reproduced below.

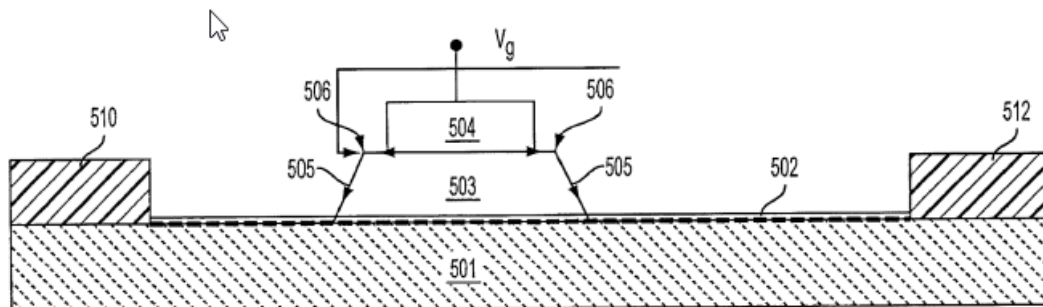


Figure 5 shows a schematic diagram of a transistor device including GaN base layer 501, barrier layer 502, source metal 510, drain metal 512, p-type gate material 503, gate metal 504, and horizontal ledges 506 on each side of gate metal 504. Ex. 1001, 3:37–59. The '335 patent states that ledges 506 “have equal or substantially equal widths, i.e., the respective ledges are symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material, which is due to the self-aligned manufacturing process.” Ex. 1001, 3:59–64.

Figure 5 also includes arrows showing gate current path 505 that travels horizontally along the ledges 506 and then follows the diagonal path along the edge of p-type gate material 503. Ex. 1001, 4:6–11. According to the '335 patent, this structure results in reduced gate leakage current compared to conventional gates without ledges. Ex. 1001, 4:12–13, 4:47–51, Fig. 8.

The '335 patent also describes an exemplary manufacturing process for forming a gate with self-aligned ledges and depicts the steps in Figures 6A–6C, reproduced below. Ex. 1001, 4:14–35, Figs. 6A–6C.

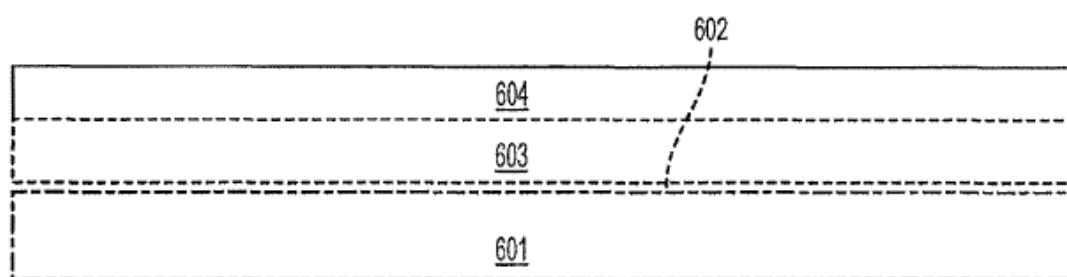


FIG. 6A

Figure 6A shows forming AlGaN barrier layer 602 on GaN base layer 601, forming a layer of p-type gate material 603 on barrier layer 602, and depositing gate metal 604 on p-type gate material 603. Ex. 1001, 4:14–22.

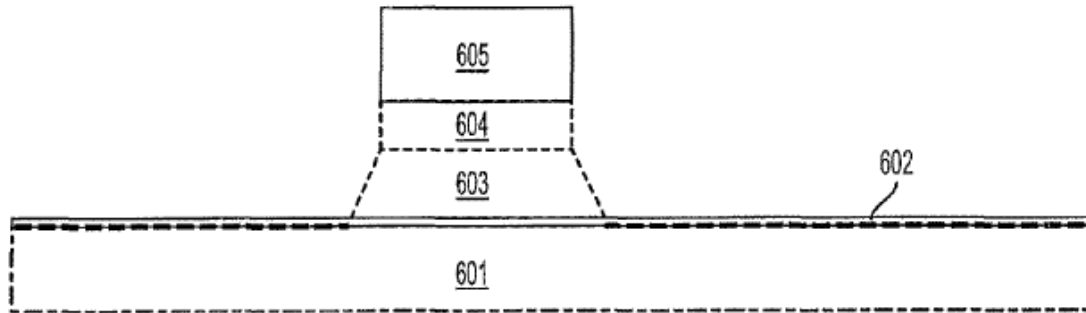


FIG. 6B

Figure 6B shows photoresist layer 605 deposited on gate metal 604, and the resulting structure after gate metal 604 and p-type gate material are etched. Ex. 1001, 4:23–26.

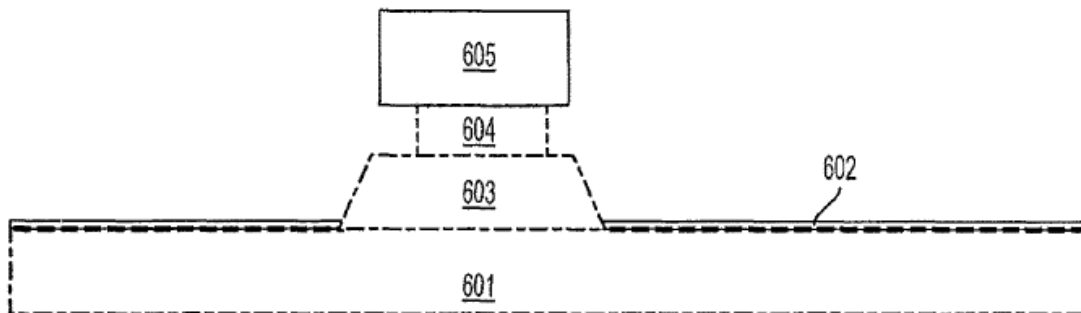


FIG. 6C

Figure 6C shows the resulting structure after gate metal 604 is etched isotropically such that gate metal 604 has a width less than the planar upper surface of p-type gate material 603. Ex. 1001, 4:26–29. According to the '335 patent, “[t]his second etching step results in the formation of the ledges 506 of the p-type gate material 603.” Ex. 1001, 4:29–31.

The '335 patent states that the self-aligned process illustrated in Figures 6A–6C is “vastly superior to forming gate ledges using separate

masks” due to the possibility of misalignment between the gate metal and p-type gate material when using a two-mask process. Ex. 1001, 4:52–63.

D. Illustrative Claims

Of the challenged claims, claims 1 and 5 are independent claims, and are reproduced below.

Claim 1:

[1p] An enhancement-mode GaN transistor, comprising:

[1a] a GaN layer;

[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[1c] a source contact and a drain contact formed on the barrier layer;

[1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and

[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

Ex. 1001, 5:5–25 (labels added to correspond with Petitioner’s designation of claim limitations (Pet. Claim Appendix)).

Claim 5:

[5p] An enhancement-mode GaN transistor, comprising:

[5a] a GaN layer;

[5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[5c] a source contact and a drain contact disposed on the barrier layer;

[5d] a p-type gate material formed above the barrier layer and between the source and drain contacts;

[5e] and a gate metal disposed on the p-type gate material,

[5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

[5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

Ex. 1001, 6:6–23 (minor formatting and labels added to correspond with Petitioner’s designation of claim limitations (Pet. Claim Appendix)).

E. Asserted Unpatentability Challenges

Petitioner asserts that claims 1–7 are unpatentable based on the following challenges:

Claims Challenged	35 U.S.C. §¹	Reference(s)/Basis
1–7	103	Saxler ²
1–7	103	Saxler, Yoshida ³
2, 5–7	103	Saxler, Yoshida, Beach, ⁴ Shenoy ⁵
1–7	103	Yoshida
1–7	103	Yoshida, Saxler
2, 5–7	103	Yoshida, Saxler, Beach, Shenoy

Petitioner relies on the declaration of James Richard Shealy, Ph.D. (Ex. 1003).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have had “at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field, and at least two years of experience in semiconductor device design and/or

¹ The relevant sections of the Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. Because the ’335 patent has an effective filing date prior to the effective date of the applicable AIA amendments, the pre-AIA version of § 103 applies.

² US 2006/0108606 A1, published May 25, 2006 (Ex. 1007).

³ JP H11-261053, published Sept. 24, 1999 (Ex. 1005 (original language); Ex. 1006 (certified English translation)).

⁴ US 2007/0007547 A1, published Jan. 11, 2007 (Ex. 1008).

⁵ R. V. Shenoy, et. al, *Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining*, J. ELECTROCHEM. SOC., Vol. 143, No. 2, 544, Feb. 1996 (Ex. 1013).

fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies.” Pet. 18 (citing Ex. 1003 ¶¶ 52–53). Petitioner also contends that “[a]dditional education could substitute for professional experience and vice versa.” Pet. 18. Patent Owner does not challenge Petitioner’s definition or offer its own. *See generally* Prelim. Resp.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner’s proposal regarding the level of ordinary skill in the art. Based on our review of the ’335 patent and the prior art of record, at this stage of the proceeding we determine that the definition offered by Petitioner comports with the qualifications a person would have needed to understand and implement the teachings of the ’335 patent and the prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown”) (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

B. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b). Under *Phillips*, claim terms are afforded “their ordinary and customary meaning.” *Phillips*, 415 F.3d at 1312. “[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the

context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

Petitioner argues that the Board should construe two claim terms:

(1) “side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer” recited in claims 1 and 5 (the “side surfaces” limitation), and (2) “self-aligned,” recited in claims 2 and 5. Pet. 18–24. Patent Owner contends that the Board does not need to engage in any pre-institution claim construction, but nevertheless provides responses to Petitioner’s arguments. Prelim. Resp. 6–14.

I. “side surfaces”

Petitioner contends that we should construe the “side surfaces” limitation to mean “side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer.” Pet. 19. According to Petitioner, this proposed construction “agrees with the disclosure of Lidow,” a patent listed in the priority chain of the ’335 patent.⁶ Pet. 20. In particular, Petitioner contends Lidow discusses the advantage of using sloped sidewalls to reduce gate leakage, and “specifically teaches that

⁶ The ’335 patent lists US Application No. 12/756,960, issued as US 8,404,508 B2 (“Lidow-508” (Ex. 3001)) on March 26, 2013, as a related application. Ex. 1001, code (60), 1:4–17. In the Petition, Petitioner cites to the published application, US 2010/0258843A1, published Oct. 14, 2010 (Ex. 1011). Petitioner disagrees that the ’335 patent properly claims priority to Lidow, and states that it intends to challenge the priority claim to Lidow in a separate *ex parte* reexamination proceeding. Pet. 15. Petitioner, however, states that for purposes of the Petition, it “assume[s] priority to the filing of the earliest application in the priority claim,” which includes Lidow. Pet. 15–16; Ex. 1001, code (60).

a ‘base that is more than 10% wider than the top’ advantageously ‘causes a longer path for electrons to travel between the gate metal 17 and the 2DEG along the pGaN side wall,’ thereby ‘result[ing] in lower gate leakage.’”

Pet. 20 (quoting Ex. 1011 (Lidow) ¶42). Petitioner asserts that Lidow provides no other guidance on how much slope is sufficient to achieve reduced gate leakage, and that Lidow’s disclosure of having a base that is more than 10% wider than the top distinguishes Lidow’s invention from prior art structures, because “few structures, if any, have perfectly vertical sidewalls in practice, even if depicted as vertical in functional diagrams.”

Pet. 21.

Petitioner further contends that its construction “adheres to the purpose of the ’335 patent—reducing gate leakage, including through the conventional method of sloping sidewalls to increase the length of the sidewall leakage path.” Pet. 20 (citing Ex. 1001, code (57), 1:21–26, 2:20–48, 3:65–4:12, 4:40–51, Figs. 2, 4, 7A–7B, 8). Petitioner also asserts that its proposed construction is consistent with the disclosure of the ’335 patent because Figures 5, 6C, and 7B of the ’335 patent depict gate material with sloped side surfaces whose bottom surface is approximately 30% wider (and thus more than 10% wider) than the top. Pet. 21–22 (citing Ex. 1001, Figs. 5, 6C, 7C; Ex. 1003 ¶ 75).

Patent Owner responds that Petitioner’s proposed construction improperly seeks to import limitations from the Specification into the claims. Prelim. Resp. 6. Patent Owner asserts that the challenged claims do not recite any numerical degree of horizontal extension for the side surfaces, and Petitioner’s only support for its proposed restriction comes from a single

embodiment in Lidow. Prelim. Resp. 6–7 (citing Lidow-508 (Ex. 3001), 5:23–28)⁷; Ex. 1001, 1:7–17. Accordingly, Patent Owner argues that:

there is no intrinsic evidence *defining* the horizontal extension of the side surfaces to have a minimum threshold value or unequivocally disavowing from the scope of the claims p-type gate materials where the side surfaces extend horizontally towards the source and drain contacts but where the bottom of those materials is less than 10% wider than the top.

Prelim. Resp. 7 (citing *Thorner v. Sony Computer Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015)).

Patent Owner also contends that there is no support for Petitioner’s proposed restriction that the claimed side surfaces must be “sloped.”

Prelim. Resp. 8–10. According to Patent Owner, a sloped side surface is only one example of the type of side surface encompassed by the plain and ordinary meaning of the claim language. Prelim. Resp. 8. Patent Owner contends that limiting the claim to sloped side surfaces would read out embodiments disclosed in Lidow, such as stepped side surfaces shown in Fig. 12 of Lidow-508, wherein the bottom is wider than the top.

Prelim. Resp. 8–9.

We first address Petitioner’s argument that “side surfaces” of the p-type gate material of independent claims 1 and 5 requires that the “bottom of the p-type gate material is more than 10% wider than the top of the material.” Pet. 19. We begin our analysis with the language of the claims themselves. *See Phillips*, 415 F.3d at 1312. Here, the claims do not recite

⁷ Patent Owner cites to the Lidow-508 patent itself, instead of the published application included in the record as Ex. 1011, which Petitioner cites to. The parties have not identified any difference between the two references.

any numerical degree of horizontal extension, let alone a requirement that the bottom of the p-type gate material must be more than 10% wider than the top of the material. Ex. 1001, 5:5–6:30. Thus, the plain language of the claims themselves does not support Petitioner’s proposed construction.

Of course, the claims do not stand alone, but rather, must be read in view of the specification, of which they are part. *Phillips*, 415 F.3d at 1313. Petitioner relies on a numerical value for horizontal extension disclosed in Lidow, which is incorporated by reference in the ’335 patent. Pet. 20 (citing Ex. 1011 ¶¶ 41–42, Fig. 8; Ex. 1003 ¶ 72). But Lidow’s disclosure of a numerical value (10%) is made in the context of discussing a single embodiment. Ex. 1011 ¶ 41. Lidow does not include a numerical value in its disclosure of other embodiments. *See, e.g.*, Ex. 1011 ¶¶ 43–51.

Petitioner’s argument that its proposed construction “accords with the ’335 patent’s disclosure” of figures depicting a p-type gate material that has a bottom base that is approximately 30% wider than the top is similarly unavailing. Pet. 21–22. Petitioner’s argument is based on its numerical size measurements made on Figures 5, 6C, and 7B of the ’335 patent. Pet. 21–22. Figures 5 and 6C, however, are schematic diagrams that contain no numerical values and may not be relied upon to show particular sizes in this context. *See In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977) (“Absent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value.”). Dr. Shealy contends that Figure 7B is an actual image of an etched gate structure (Ex. 1003 ¶ 75), but the ’335 patent makes clear that this is only a single, exemplary embodiment. Ex. 1001, 3:18–20. The ’335 patent also states, with regard to the embodiments disclosed in the Specification, that “[i]t is to be understood that other embodiments may be employed and that various

structural, logical, and electrical changes may be made.” Ex. 1001, 3:30–32. Thus, to the extent Petitioner’s size measurements are even accurate, we are not persuaded, based on the present record, that the “side surfaces” of the p-gate material recited in the independent claims should be construed to require that the bottom of the p-type gate material is more than 10% wider than the top of the material.

We reach a similar determination regarding Petitioner’s argument that we should construe the claims to require sloped sidewalls. Pet. 19–20. The claims do not expressly require a sloped side surface, and Petitioner does not direct us to any limiting language regarding sloped side surfaces in the Specification of the ’335 patent. Further, as Patent Owner points out (Prelim. Resp. 8–9), Lidow discloses embodiments wherein the gate material has stepped sidewalls, such that the bottom of the gate material is wider than the top. *E.g.*, Ex. 1011, Figs. 9–12, ¶¶ 43–44. Thus, Petitioner’s argument is not supported by Lidow’s disclosure. Therefore, on this record, Petitioner fails to demonstrate sufficiently that the claims should be limited by requiring the side surfaces to be sloped.

In view of the foregoing, for purposes of this Decision, we decline to adopt Petitioner’s proposed construction of the “side surfaces” limitation. After considering the arguments and information presented in the Petition and Preliminary Response, we determine that it is not necessary to further construe this term for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”)). The parties do not dispute that the language “side surfaces extending

horizontally” encompasses a gate material with sloped side surfaces as depicted in Figure 5 of the ’335 patent. Prelim. Resp. 29–30; Pet. 19–21. To the extent necessary, the parties are invited to address this limitation further during the course of this trial.

2. “self-aligned”

Claims 2 and 5 recite horizontal ledges that are “self-aligned.” Ex. 1001, 5:26–28 (claim 2), 6:18–19 (claim 5). According to Petitioner, “[i]n the ’335 patent, a ‘self-aligned’ ledge refers to a process for making the claimed gate structure and does not describe the structure itself.” Pet. 23 (citing Ex. 1001, 3:49–53 (referring to “ledges 506 that are created by a self-aligned process”), 3:65–4:39 (referring to a “self-aligned manufacturing process”)). As a result, Petitioner argues that claims 2 and 5 recite product-by-process steps in a device claim, which lend no patentable weight. Pet. 24 (quoting and citing *In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985) (“If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.”); citing *United Therapeutics Corp. v. Liquidia Techs., Inc.*, 74 F.4th 1360, 1373 (Fed. Cir. 2023) (“As these claims are product claims, they are anticipated by a disclosure of the same product irrespective of the processes by which they are made.”)).

Patent Owner acknowledges that the ’335 patent discloses a process for self-alignment, but argues that the term “self-aligned” as used in claims 2 and 5 is not a product-by-process limitation because it “connotes a specific structure to the claimed GaN transistor and imparts structural and functional differences onto the claimed GaN transistor” and therefore “the so-called process limitation is considered structural.” Prelim. Resp. 10–11.

According to Patent Owner, the Specification of the ’335 patent “explains

that the ‘primary benefit’ of self-alignment is that it ‘enable[s] the creation of a p-type gate with a minimum critical dimension (“CD”)’ and allows ledges to be created ‘that are symmetric to the gate metal disposed on the p-type gate material.’” Prelim. Resp. 12–13 (quoting Ex. 1001, 3:65–4:3).

Patent Owner thus argues that a person of ordinary skill in the art would understand the self-alignment process as imparting structural characteristics onto a transistor, and therefore the term “must be ‘interpreted in [its] structural sense.’” Prelim. Resp. 13 (quoting *In re Nordt*, 881 F.3d 1371, 1374–75 (Fed. Cir. 2018)).

Patent Owner also contends that even if the limitation is a product-by-process limitation, self-alignment is a feature that differentiates the claimed transistor from prior art, and, therefore, the process limitation is not irrelevant. Prelim. Resp. 11, 13 (citing *Greenliant Sys., Inc. v. Xicor LLC*, 692 F.3d 1261, 1268 (Fed. Cir. 2012)).

After considering the arguments and information presented in the Petition and Preliminary Response, we determine that we do not need to expressly construe this term for purposes of this Decision. *See Nidec*, 868 F.3d at 1017. Nevertheless, we provide the following analysis.

The law on product-by-process claims is well-established. “In determining validity of a product-by-process claim, the focus is on the product and not the process of making it.” *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1369 (Fed. Cir. 2009). “That is because of the already described, long-standing rule that an old product is not patentable even if it is made by a new process. As a result, a product-by-process claim can be anticipated by a prior art product that does not adhere to the claim’s process limitation.” *Id.* at 1370 (internal footnote omitted). The Federal Circuit has noted an exception to this general rule, stating that “[a]s we

recognized in *Amgen*, if the process by which a product is made imparts ‘structural and functional differences’ distinguishing the claimed product from the prior art, then those differences ‘are relevant as evidence of no anticipation’ although they ‘are not explicitly part of the claim.’” *Greenliant*, 692 F.3d at 1268.

In *Amgen*, the court held that the claimed product was not an old product made by a new process, but instead that the claimed product was new based on structural and functional differences between the claimed product and the prior art. *Amgen*, 580 F.3d at 1367 (holding that a protein (EPO) reproduced by recombinant technology was not anticipated by prior art urinary EPO because of evidence demonstrating that recombinant EPO can be distinguished from urinary EPO due to differences in carbohydrate composition). Here, however, it is not clear what structural or functional differences distinguish the claimed product made by a self-aligned process from a product made using a different process.

According to Patent Owner, the structural features imparted by the self-aligned process are (1) it “enable[s] the creation of a p-type gate with a minimum critical dimension (‘CD’)” and (2) “allows ledges to be created ‘that are symmetric to the gate metal disposed on the p-type gate material.’” Prelim. Resp. 12–13 (quoting Ex. 1001, 3:65–4:3). The ’335 patent, however, indicates that at least one other method can produce transistors with the same structural features. Ex. 1001, 4:52–63 (describing a process for forming gate ledges using separate masks instead of the self-aligned process disclosed in the ’335 patent). Thus, although using the self-aligned process may impart structural features, the evidence suggests those same structural features may be imparted using other processes, and it is not clear how a product made using the self-aligned process differs from a product

made using a different process. In other words, there is insufficient evidence on the present record demonstrating that a transistor having a p-type gate with a minimum CD and symmetric ledges—made using a self-aligned process—is **structurally different** from a transistor having a p-type gate with a minimum CD and symmetric ledges—made using a different process.

We recognize the '335 patent explains a self-aligned process may provide an advantage over other processes, i.e., by reducing or eliminating the “possibility of misalignment.” Ex. 1001, 4:60–63. But it is not clear how that purported advantage of the process translates into a new, structurally different product. Rather, the language in the Specification addresses making an old product using a new, more advantageous process. As a result, the evidence on the present record suggests that the recited product-by-process claims can be anticipated by a prior art product that does not adhere to the claim’s process limitation.

We also disagree with Patent Owner’s contention that *Pacira Pharms. Inc. v. eVenus Pharms. Labs., Inc.*, Nos. 22-00718 & 21-19829, 2023 WL 3841559, at *9 (D.N.J. June 6, 2023) is instructive in confirming that the term “self-aligned” connotes specific structure and is therefore not a product-by-process limitation. Prelim. Resp. 12. For example, as Patent Owner acknowledges, the court in *Pacira* relied on expert testimony regarding whether the disputed process informed a person of ordinary skill in the art about structural properties of the claimed invention. Prelim. Resp. 12 (citing *Pacira* at *10). On the present record, however, Patent Owner offers no such testimony in support of its arguments.

For all of the foregoing reasons, it is not clear, based on the evidence presented at this stage, that the self-aligned process imparts structural and

functional differences to products, and thereby creates new products instead of old products made using a new process. Rather, it appears to be simply another process used to prepare structural features that can be obtained in other ways. Accordingly, since the claims are product claims, the evidence Patent Owner presents on this record does not support a determination that “self-aligned” falls within the exception to the rule for product-by-process claims.

We invite the parties to address this limitation further during the course of this trial, particularly addressing whether the claimed enhancement-mode GaN transistor prepared by a self-aligned process is a new product or simply an old product formed by a new method. Additionally, we invite the parties to address how claims 1 and 2 are different, if at all, considering the Specification of the ’335 patent equates ledges that are “symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material,” the purported structural feature imparted by the self-aligned process, with ledges that have substantially equal widths, a limitation already present in claim 1. Ex. 1001, 3:59–64.

C. Overview of Asserted Prior Art

1. Saxler (Ex. 1007)

Saxler discloses Group III-nitride high electron mobility transistors and methods for forming those transistors. Ex. 1007 ¶¶ 1, 7. In particular, Saxler is directed to HEMTs that include “a non-uniform aluminum concentration AlGa_N based cap layer having a high aluminum concentration adjacent a surface of the cap layer that is remote from the barrier layer on which the cap layer is provided.” Ex. 1007, code (57). Saxler explains that having such a cap layer “may improve robustness of the device during processing and/or device operation” over conventional

devices. Ex. 1007 ¶ 47. Saxler also explains that HEMTs “may offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies.” Ex. 1007 ¶ 4.

Saxler discloses several embodiments of its claimed invention, including the transistors depicted in Figures 1A and 1B, reproduced below.

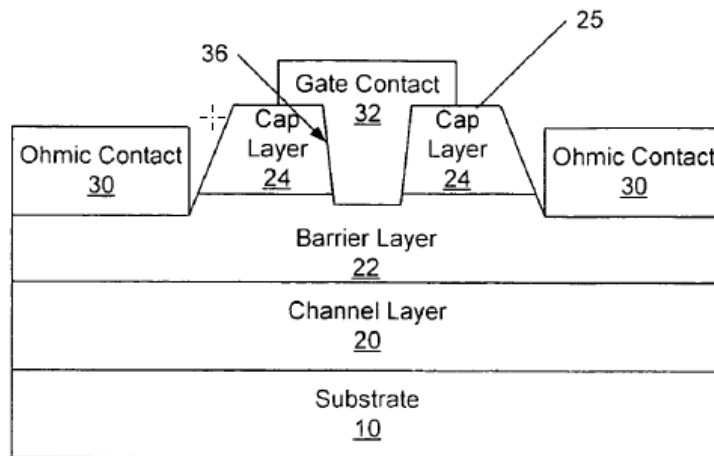


Figure 1A

Figure 1A of Saxler shows a cross-sectional schematic drawing illustrating a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24, and gate contact 32. Ex. 1007 ¶¶ 31, 57, 61, 66. In this embodiment, gate contact 32 occupies recess 36 in cap layer 24. Ex. 1007 ¶¶ 61, 66.

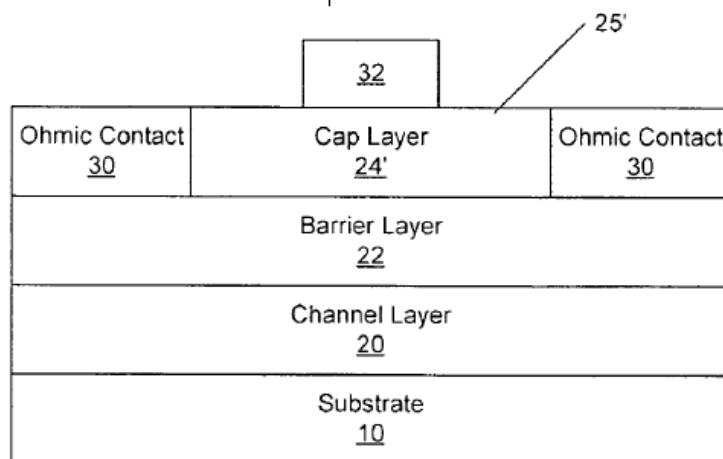


Figure 1B

Figure 1B of Saxler shows a cross-sectional schematic drawing illustrating a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24', and gate contact 32. Ex. 1007 ¶¶ 31, 57, 61, 66. In this embodiment, cap layer 24' does not have a recess, such that gate 32 is on cap layer 24'. Ex. 1007 ¶¶ 61, 66.

Saxler describes the features of its various embodiments, including those with a gate recess and those without a gate recess. *E.g.*, Ex. 1007 ¶¶ 66 (describing suitable gate materials), 70 (describing suitable n-type dopants), 71 (describing suitable p-type dopants). Saxler also discloses methods for making transistors according to the embodiments described in the specification. Ex. 1007 ¶¶ 6, 68.

2. Yoshida (Ex. 1006)

Yoshida discloses novel GaN-based HEMT structures that can operate under the application of high voltages and at higher speeds. Ex. 1006 ¶¶ 1, 8. Yoshida depicts the basic structure of its described invention in Figure 1, reproduced below.

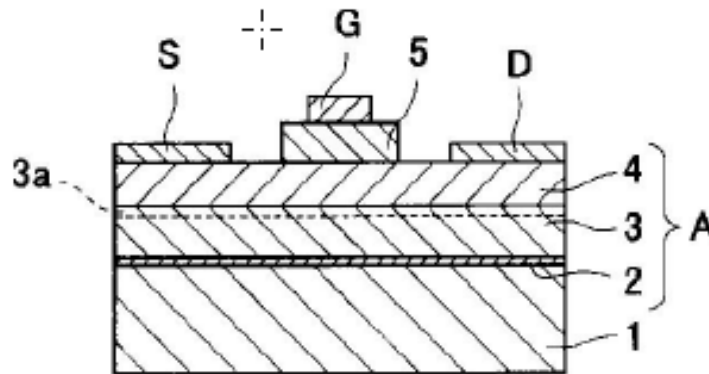


Figure 1 of Yoshida shows a cross-sectional view of a transistor having a stacked structure comprising buffer layer 2, i-type semiconductor layer 3, and n-type semiconductor layer 4 formed on semi-insulating substrate 1. Ex. 1006 ¶ 10. Figure 1 also shows gate electrode G on p-type semiconductor layer 5, as well as source electrode S and drain electrode D, all formed on n-type semiconductor layer 4. Ex. 1006 ¶ 10.

Yoshida discloses methods for fabricating the structure shown in Figure 1, including deposition and etching conditions. Ex. 1006 ¶¶ 19–23.

3. Beach (Ex. 1008)

Beach discloses a “normally OFF III-nitride power semiconductor device and a method for the fabrication thereof.” Ex. 1008 ¶ 9. Beach depicts an embodiment of its invention in Figure 1, reproduced below.

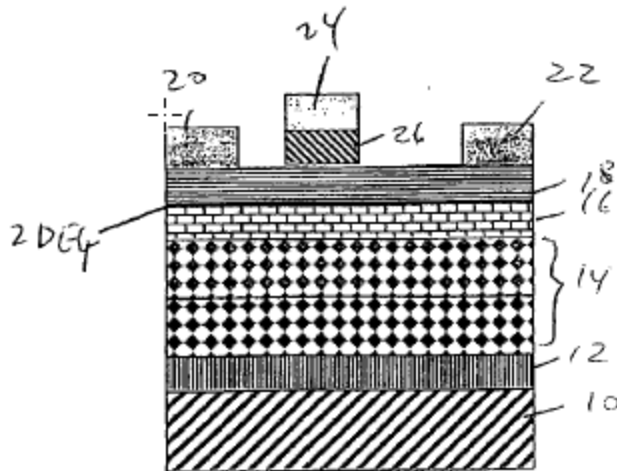


Figure 1 of Beach shows substrate 10, bonding layer 12, first III-nitride buffer body 14, first III-nitride semiconductor body 16, second III-nitride semiconductor body 18, first power electrode 20 and second power electrode 22, and gate arrangement 24, with gate barrier 26 disposed under gate arrangement 24 and over second III-nitride semiconductor body 18.

Ex. 1008 ¶¶ 31–32.

Beach describes a method for making the embodiment shown in Figure 1, wherein “[m]aterials for the gate arrangement are . . . deposited on gate barrier material 42 and the stack is patterned and etched to obtain gate arrangement 24 over gate barrier 26.” Ex. 1008 ¶ 40. Beach states that “the method as described results in a self-aligned gate arrangement.” Ex. 1008 ¶ 40. Beach further explains that a device made according to the first embodiment is advantageous because, *inter alia*, it is an enhancement-mode device and it includes “self-aligned gates.” Ex. 1008 ¶¶ 43–45.

4. Shenoy (Ex. 1009)

Shenoy pertains to the development of a “mathematical model to predict shape evolution during through-mask electrochemical

micromachining (EMM).” Ex. 1009, 2.⁸ Shenoy explains that EMM is “receiving increasing attention in microfabrication for patterning, shaping, and finishing.” Ex. 1009, 2. Shenoy further explains that in through-mask EMM, an exposed metal surface is removed by high-rate anodic metal dissolution, and etching can occur from a single side or both sides simultaneously. Ex. 1009, 2. According to Shenoy, “[t]he isotropic nature of the metal removal process leads to undercutting of the [photoresist] mask,” and “knowledge of the metal removal rates and undercutting of the photoresist is, therefore, essential in designing the photoresist mask.” Ex. 1009, 2.

Shenoy states that EMM provides cost and environmental advantages over other fabrication techniques, and therefore “the predictability and control of metal wall profile and undercut are of particular interest.” Ex. 1009, 2. In view of this, Shenoy investigates “the influence of the mask wall angle on the current distribution, the shape of the evolving cavity, and the etch factor.” Ex. 1009, 2.

D. Claims 1–7 – Alleged Obviousness in view of Saxler

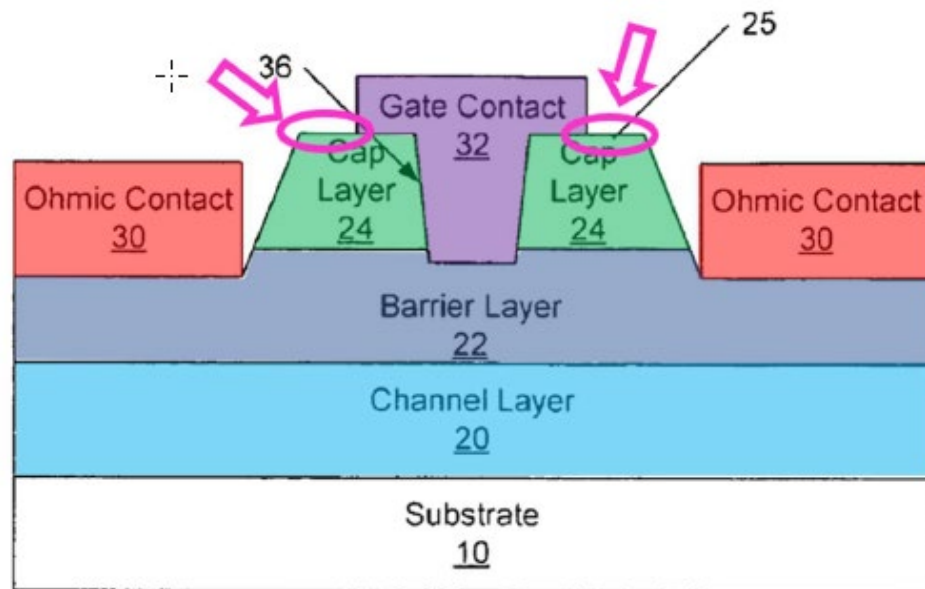
Petitioner contends claims 1–7 of the ’335 patent are unpatentable as obvious over Saxler in view of the knowledge of a person of ordinary skill in the art. Pet. 24–56. Patent Owner challenges Petitioner’s arguments. Prelim. Resp. 21–28.

⁸ Citations to Shenoy are to page numbers added by Petitioner.

I. Analysis

a) Claim 1

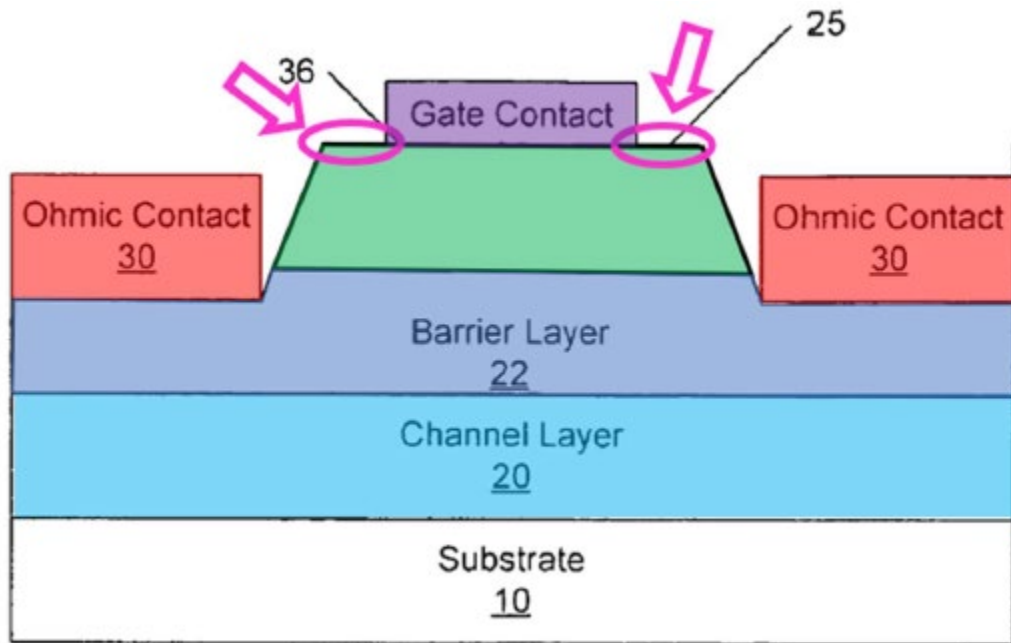
Petitioner contends Saxler discloses a GaN transistor with high breakdown voltage, as shown in Figure 1A, reproduced below with annotations from Petitioner.



Annotated Figure 1A of Saxler shows a cross-sectional schematic view of a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24, and gate contact 32. Petitioner has annotated Figure 1A to show channel layer 20 in light blue, barrier layer 22 in dark blue, cap layer 24 in green, gate contact 32 in purple, and source and drain contacts 30 in red. Pet. 5, 25.

Petitioner recognizes that Figure 1A of Saxler shows an embodiment where gate contact 32 is recessed so that it extends through cap layer 24 into barrier layer 22. Pet. 24–25. Petitioner, however, contends that Saxler also teaches that its gate contact may be non-recessed (i.e., flat). Pet. 25 (citing, *inter alia*, Ex. 1007 ¶¶ 52, 66), 31 (citing Ex. 1007 ¶¶ 12–13, 27, 52, 64, 70–71, 73, claims 3, 14, 21, 27, 31, 88, code (57)). In view of Saxler’s

disclosure that a recessed gate contact is optional, Petitioner asserts Saxler renders obvious a stacked gate structure having a gate contact and cap layer without a recess, as depicted in a modified version of Figure 1A, which is reproduced below.



Petitioner's modified version of Saxler Figure 1A shows gate contact 36 (in purple), without a recess, stacked on cap layer 32 (in green), formed on barrier layer 22 (in dark blue), which is on top of channel layer 20 (light blue) and substrate 10. Pet. 25–26. It also depicts source and drain contacts 30 (in red). Pet. 26.

Patent Owner asserts that the hypothetical structure depicted in modified Figure 1A of Saxler, which Petitioner relies upon, does not appear anywhere in Saxler, and is designed solely based on hindsight. Prelim. Resp. 22. According to Patent Owner, Saxler discloses two embodiments of its cap layer: a bifurcated recessed cap layer with slanted sidewalls shown in Figure 1A and a non-recessed cap layer depicted as a rectangular layer between the source and drain contacts, as shown in Figure 1B. Prelim. Resp.

21–22. Patent Owner contends that Saxler does not teach that these two embodiments can be combined or how to manufacture the combined embodiment. Prelim. Resp. 22.

Although the structure depicted in modified Figure 1A of Saxler does not itself appear in Saxler, Petitioner has provided sufficient argument and evidence that a person of ordinary skill in the art would have understood that Saxler suggests a stacked gate structure having a gate contact, a cap layer without a recess, and sloped sidewalls, as depicted in modified Figure 1A. Pet. 25–26, 39–41. First, as Petitioner and Dr. Shealy note, the ’335 patent itself recognizes that sloped sidewalls were known and conventional in the prior art. Pet. 39; Ex. 1003 ¶ 118; Ex. 1001, 1:42–2:26, Figs. 1, 2, 3A, 3B (all labeled as “PRIOR ART” and showing sloped sidewalls).

Next, Saxler describes embodiments of its claimed invention without a gate recess. *See* Ex. 1007 ¶¶ 12, 13, 27, 70, 73, claims 3, 14, 21, 27, 31, 88. For example, in paragraph 27, Saxler states that “[t]he transistor may further include a gate contact recessed into the AlN cap layer,” and also that “[t]he transistor may also include a gate contact on the AlN cap layer and not recessed into the AlN cap layer.” Ex. 1007 ¶ 27. Additionally, in its figures, Saxler discloses cap layer 24 with and without a recess. Ex. 1007, Figs. 1A, 1B. Saxler’s figures also depict gate contact 32 being formed in a gate recess of cap layer 24 (having a T shape as shown in Figure 1A) or on top of cap layer 24 (i.e., flat, as shown in Figure 1B). Moreover, Saxler states that the embodiments shown in the figures are exemplary, and its claimed invention should not be limited to those examples. Ex. 1007 ¶ 52.

Dr. Shealy states that in embodiments where a gate recess is not utilized, a person of ordinary skill in the art would have understood that Saxler has the structure shown in modified Figure 1A of Saxler. Ex. 1003

¶ 91. Dr. Shealy's testimony is consistent with the disclosure of Saxler, and Patent Owner does not offer conflicting testimony from a declarant.

For all of the foregoing reasons, based on the present record, we are persuaded by Petitioner's argument that Saxler at least suggests a stacked gate structure having a gate contact and cap layer without a recess, as depicted in modified Figure 1A of Saxler.

i. [1p]

Relying on the structure shown in modified Figure 1A, Petitioner contends Saxler discloses or renders obvious an "enhancement-mode GaN transistor," as recited in the preamble of claim 1. Pet. 35–36. In particular, Petitioner contends that Saxler discloses a doped GaN cap layer below the gate contact and above an AlGa_N barrier layer. Pet. 35 (citing Ex. 1007 ¶¶ 7–10, 46, 59–64, Figs. 1A, 1B; Ex. 1003 ¶ 108). Petitioner argues that a person of ordinary skill in the art would have understood Saxler's transistors to be enhancement-mode GaN transistors based on this gate structure when the cap is doped p-type. Pet. 35–36 (citing Ex. 1003 ¶¶ 108–109; Ex. 1021 ¶¶ 14, 40, 42, Fig. 1F).

Patent Owner argues that Saxler does not disclose or suggest an enhancement-mode device. Prelim. Resp. 16, 21–24. Patent Owner contends that Saxler explains the purpose of doping the cap layer is to reduce gate leakage along dislocations, and that a person of ordinary skill in the art would have understood this "is unrelated and distinct from creating an enhancement mode transistor." Prelim. Resp. 16. Patent Owner also asserts that even assuming Saxler discloses the hypothetical device depicted in modified Figure 1A, it would not function as an enhancement-mode device, stating that "it would be non-operational due to its inability to induce a 2DEG between the ohmic contacts." Prelim. Resp. 22.

According to Patent Owner, the cap layer in modified Figure 1A of Saxler reaches “all the way from source to drain,” depleting the access regions between the gate contact and each of the ohmic contacts, which results in the absence of 2DEG all the way from source to drain. Prelim. Resp. 23. Patent Owner thus asserts that the hypothetical transistor would always lack a 2DEG in the access regions and the 2DEG could not be induced in those regions. Prelim. Resp. 23. Patent Owner concludes that “[w]ithout a 2DEG, such a transistor will not work properly and could not be switched to its ON state, thereby rendering the hypothetical device non-functional as an enhancement-mode device.” Prelim. Resp. 24.

For the reasons discussed above, Petitioner has demonstrated sufficiently that Saxler suggests a stacked gate structure having a gate contact and cap layer without a recess, as depicted in modified Figure 1A of Saxler. Additionally, Petitioner presents declarant testimony supporting its argument that the structure depicted in modified Figure 1A is an enhancement-mode device when p-type dopants are placed in the cap layer below the gate and above an AlGaN barrier layer, as disclosed in Saxler. Ex. 1003 ¶ 108 (citing Ex. 1007 ¶¶ 7–10, 46, 59–64, Figs. 1A, 1B). Dr. Shealy also relies on disclosures in Sheppard, which is incorporated by reference in Saxler, to support his position that a person of ordinary skill in the art would have understood a transistor having the gate structure shown in modified Figure 1A to constitute a normally-off enhancement-mode GaN transistor. Ex. 1003 ¶ 109 (citing Ex. 1021 ¶¶ 14, 40, 42, 46, 68).

Patent Owner’s argument that a person of ordinary skill in the art would have recognized the purpose of doping in Saxler is unrelated to and distinct from creating an enhancement-mode device is unavailing at this stage of the proceeding. Prelim. Resp. 16. First, it comprises unsupported

attorney argument, which does not constitute evidence. *See Laitram Corp. v. Cambridge Wire Cloth Co.*, 919 F.2d 1579, 1583 (Fed. Cir. 1990).

Second, even if Patent Owner is correct about the purpose of doping—to reduce gate leakage along dislocations—its argument does not address the relevant question of whether or not doping the cap layer in Saxler actually creates an enhancement-mode transistor. The only evidence on the present record is Petitioner’s evidence suggesting that doping the cap layer would provide an enhancement-mode transistor, regardless of the purpose.

We also have concerns, at this stage of the proceeding, about Patent Owner’s arguments that the transistor depicted in modified Figure 1A is non-operational. *See* Prelim. Resp. 21–24. Once again, Patent Owner relies on unsupported attorney argument, which does not constitute evidence. Moreover, Patent Owner’s position is based on the assertion that the cap layer in the modified Figure 1 of Saxler reaches all the way from source to drain, depleting access regions between the gate contact and each of the ohmic contacts, resulting in the absence of 2DEG. Prelim. Resp. 23. Our review of modified Figure 1A of Saxler, however, indicates that the cap layer does not actually extend all the way from source to drain. Instead, there is at least some space between the end of the cap layer (in green) and the ohmic contacts (in red) occupied by the barrier layer (in dark blue). This undermines Patent Owner’s argument that the transistor would always lack a 2DEG in the access regions. Prelim. Resp. 24.

In view of the foregoing, we determine Petitioner has demonstrated sufficiently for purposes of institution that Saxler discloses an enhancement-mode transistor as recited in limitation [1p].⁹

ii. [1a]–[1c]

For limitation 1[a], which recites “a GaN layer” (Ex. 1001, 5:6), Petitioner contends Saxler discloses that channel layer 20 is a GaN channel layer. Pet. 36 (citing Ex. 1007 ¶¶ 7, 10, 16, 58, 69; Ex. 1003 ¶¶ 110–111).

Petitioner next argues that Saxler discloses limitation 1[b], which recites “a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer.” Ex. 1001, 5:7–9. Petitioner directs us to Saxler’s barrier layer 22, disposed on GaN channel layer 20, as well as Saxler’s disclosure of forming a 2DEG at the interface between channel layer 20 and barrier layer 22. Pet. 37–38 (citing Ex. 1007 ¶¶ 4, 59).

Petitioner next directs us to Saxler’s disclosure of ohmic contacts 30 on barrier layer 22 that “provide source and drain contacts” to demonstrate that Baxter satisfies limitation 1[c], which recites “a source contact and a drain contact formed on the barrier layer.” Ex. 1001, 5:10–11; Pet. 38–39 (quoting Ex. 1007 ¶ 65).

Patent Owner does not separately dispute Petitioner’s arguments and evidence that Saxler discloses limitations [1a]–[1c]. We have reviewed Petitioner’s arguments and evidence and determine that at this stage of the proceeding, Petitioner has sufficiently shown that Saxler discloses or suggests the subject matter recited in limitations 1[a]–[1c].

⁹ In view of this determination, we do not address whether the preamble is limiting. The parties may address that question further during the course of the trial.

iii. [1d]-[1e]

Limitation [1d] recites “a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer.” Ex. 1001, 5:12–15. Petitioner contends that Saxler discloses p-type gate material (cap layer 24) that resides above barrier layer 22, as limitation [1d] requires. Pet. 39–40. Petitioner also argues that in view of Saxler’s disclosure that a gate recess is optional, Saxler discloses or at least renders obvious a single p-type gate material with two side surfaces that extend horizontally towards the source and drain (i.e., sloped side surfaces), as shown in modified Figure 1A of Saxler. Pet. 40–41.

Petitioner likewise relies on Saxler’s disclosure of embodiments that lack a gate recess and do not bifurcate the cap layer into distinct portions to demonstrate that Saxler discloses limitation [1e], which recites “a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material.” Ex. 1001, 5:16–18. Petitioner asserts that for non-recessed gate embodiments, Saxler’s gate contact 32 is a gate metal formed on cap layer 24 (comprising p-type gate material), and the sidewalls of gate contact 32 extend vertically towards cap layer 24. Pet. 46–47 (citing Ex. 1007 ¶¶ 12–13, 27, 52, 64, 66, 70–71, 73; Ex. 1003 ¶ 128).

Patent Owner responds that Saxler does not disclose gate material having side surfaces extending horizontally towards the source contact and drain contact as recited in limitation [1d]. Prelim. Resp. 24. In particular, Patent Owner argues that Saxler “describes either a recessed gate with a bifurcated cap layer having sloped sidewalls, due to forming the gate recess, or a rectangular cap layer without sloped sidewalls.” Prelim. Resp. 24 (referring to Figs. 1A and 1B). Patent Owner further argues that there is no

motivation for a person of ordinary skill in the art to achieve a singular (i.e., non-recessed, non-bifurcated) p-type gate material with sloped sidewalls as depicted in the hypothetical device. Prelim. Resp. 25.¹⁰ According to Patent Owner, Saxler does not teach or describe the benefit of sloped walls, and Petitioner has not cited any evidence teaching benefits of elongated surface ledges prior to the priority date of the '335 patent for enhancement-mode GaN transistors with a p-type GaN gate. Prelim. Resp. 25. Additionally, Patent Owner contends that Saxler “chose to depict its non-recessed embodiment without sloped sidewalls, and therefore a [person of ordinary skill in the art] may have understood that forming the opening for the recessed gate – if anything – also formed the sloped sidewalls on the gate structure.” Prelim. Resp. 25–26. Patent Owner does not separately challenge Petitioner’s assertion that Saxler discloses the limitations in [1e].

We disagree with Patent Owner that Saxler’s disclosure is limited to the embodiments shown in Figures 1A and 1B. For the reasons discussed above, Petitioner has demonstrated sufficiently that Saxler suggests a stacked gate structure having a gate contact and cap layer without a recess and with sloped sidewalls, as depicted in modified Figure 1A of Saxler. Further, contrary to Patent Owner’s assertion otherwise, Petitioner and Dr. Shealy explain why a person of ordinary skill in the art would have had reason to remove the gate recess in Saxler Figure 1A, namely to “turn *Saxler’s* device into an enhancement mode device, thus realizing the benefits of reduced power consumption and suitability for high power applications.”

¹⁰ As noted above, it is undisputed that sidewalls having a sloped shape, e.g., as shown in Figure 5 of the '335 patent, “extend horizontally towards the source and drain contact” as recited in claim 1. Prelim. Resp. 29–30; Pet. 19–21.

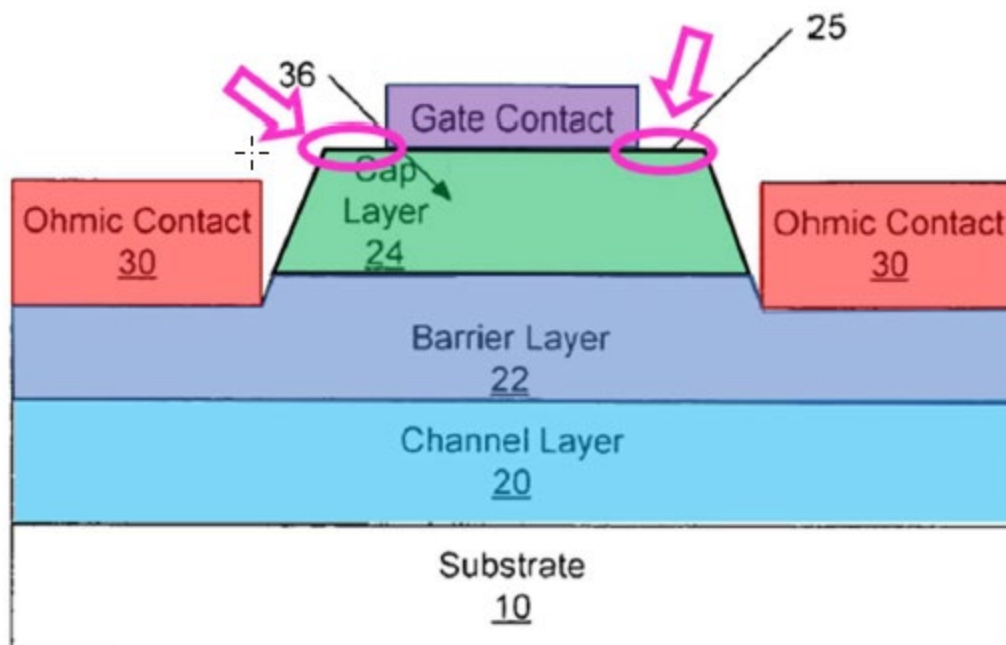
Pet. 33 (citing Ex. 1003 ¶¶ 57–63, 103). Finally, Patent Owner’s assertion that a person of ordinary skill in the art “may have understood that forming the opening for the recessed gate . . . also formed the sloped sidewalls on the gate structure” (Prelim. Resp. 26), is not only speculation, but unsupported attorney argument.

In view of the foregoing, we determine Petitioner has demonstrated sufficiently for purposes of institution that Saxler discloses or suggests the subject matter recited in limitation [1d]. Additionally, after reviewing the undisputed evidence and arguments Petitioner presents in the Petition regarding limitation [1e], we determine Petitioner has sufficiently shown that Saxler discloses or suggests the subject matter recited in limitation [1e].

iv. [1f]

Limitation [1f] requires “the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.” Ex. 1001, 5:19–25. Petitioner argues that Saxler “depicts its gate contact is narrower than its cap layer, thereby exposing horizontal ledges with substantially equal widths that extend past the respective sidewalls of the gate and toward the source and drain, as shown in Figure 1A” as well as modified Figure 1A of Saxler. Pet. 49–50 (emphasis omitted); *see also* Pet. 51 (stating that the ledges in modified Figure 1A “are symmetric on either side of the gate (i.e., having substantially equal widths)”) (citing Ex. 1003 ¶ 134).

To help illustrate this limitation, Petitioner provides a further annotated version of modified Figure 1A of Saxler, reproduced below.



This annotated version of modified Figure 1A of Saxler shows a cross-sectional view of a transistor with pink arrows and circles highlighting the horizontal ledges purported to have the substantially equal widths recited in limitation [1e]. Pet. 50.

Patent Owner contends that Saxler does not teach or disclose a pair of horizontal ledges that have substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, as limitation [1f] requires. Prelim. Resp. 26. Patent Owner acknowledges that modified Figure 1A of Saxler shows the sidewalls “are largely equidistant,” but argues that in practice, the process Saxler discloses for forming the ledges “will always lead to some unavoidable or accidental misalignment, and thus to unequal length ledges.” Prelim Resp. 26–27 (citing Ex. 1007 ¶¶ 64–66). Patent Owner further argues that Petitioner fails to identify any prior art teaching or disclosure, including in Saxler, that suggests ledges having substantially equal lengths, or a motivation to achieve ledges having substantially equal lengths. Prelim. Resp. 27–28.

In view of this, Patent Owner contends that Petitioner relies solely on the hypothetical diagram as evidence of ledges having substantial equal lengths, which is improper because “it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” Prelim. Resp. 26 (quoting *Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000)).

In its Reply, Petitioner contends that *Hockerson* does not apply because “substantially equal widths” does not require precise proportion or a particular size. Reply 1. Rather, Petitioner contends that “substantially equal” is an approximation or term of degree, and Petitioner directs us to several court decisions that have declined to extend *Hockerson* to relative proportions, terms of degree, and approximations. Reply 2–4 (citing multiple, non-binding cases distinguishing *Hockerson*).

Patent Owner responds by explaining that the technology at issue here relates to transistor dimensions that are nanometers in width, and argues that “[s]uch incredibly small widths cannot possibly be depicted in patent drawings.” Sur-reply 1; *see also* Sur-reply 2 (stating that “the claim limitation ‘substantially equal widths’ relates to a **precise** dimension - the microscopic width of a transistor gate ledge”). Patent Owner further argues that the teachings of the ’335 patent make it clear that the ledges of Saxler, formed using multiple masks, “**cannot** have substantially equal widths.” Sur-reply 1–2 (citing Ex. 1001, 4:52–63).

At this stage of the proceeding, based on the present record, we agree with Petitioner that the holding in *Hockerson* does not apply to the claim term “substantially equal” in the context of the ’335 patent. We are persuaded by Petitioner’s arguments and evidence that the term

“substantially” is a common approximation or term of degree in patent claims, and, therefore, “substantially equal” does not require a precise proportion or particular size. Reply 3–4 (citing *Seattle Box Co., Inc. v. Indus. Crating & Packing, Inc.*, 731 F.2d 818, 826 (Fed. Cir. 1984); M.P.E.P. § 2173.05(b)(II)(D)). Patent Owner does not directly dispute that “substantially” is a term of degree or an approximation. *See generally* Sur-reply 1–2. Rather, Patent Owner argues that “substantially equal widths” is a precise dimension because the technology of the ’335 patent deals with incredibly small widths. Sur-reply 1–2. Patent Owner, however, has not directed us to any authority that demonstrates we should treat the term “substantially” differently for purposes of the ’335 patent because the technology involves microscopic dimensions. As a result, we determine, for purposes of this Decision, that *Hockerson* does not apply to the claim term “substantially equal.”¹¹

Petitioner and Dr. Shealy contend that the horizontal ledges shown in modified Figure 1A, which is derived from Saxler’s figures and disclosure, have substantially equal lengths. Pet. 49 (citing Ex. 1007, Fig. 1A; Ex. 1003 ¶¶ 132–133). Patent Owner acknowledges that modified Figure 1A of Saxler shows sidewalls that are “largely equidistant” from the overlying gate metal. Prelim. Resp. 26. Thus, there does not appear to be a dispute that modified Figure 1A depicts horizontal ledges that have substantially equal lengths.

Additionally, Patent Owner offers no evidence supporting the assertion that a person of ordinary skill in the art would understand that

¹¹ Claim 7 requires self-aligned edges that are “symmetrical.” To the extent necessary, we invite the parties to address whether the holding in *Hockerson* applies to that claim term.

some unintended misalignment always occurs when forming transistors. Prelim. Resp. 26. But even if we were to agree with Patent Owner, there is insufficient evidence on this record to determine that “some unintended misalignment” would result in ledges that do not have “substantially equal lengths,” given that the phrase “substantially” is an approximation or term of degree.

We also disagree with Patent Owner’s assertion that the ’335 patent demonstrates ledges formed using multiple masks “cannot” have substantially equal widths. Sur-reply 1–2. The language Patent Owner relies on to support its assertion refers only to the possibility of misalignment using a two-mask process. Sur-reply 1–2; Ex. 1001, 4:52–63. We do not consider this language to mean that a two-mask process will always result in misalignment such that it is impossible to form ledges having substantially equal widths when using a two-mask process.

In view of the foregoing, we determine Petitioner has demonstrated sufficiently for purposes of institution that Saxler discloses or suggests the subject matter recited in limitation [1f].

v. Conclusion – claim 1

For all of the foregoing reasons, we determine Petitioner has demonstrated sufficiently for purposes of institution that Saxler discloses or suggests the subject matter recited in claim 1.

b) Claims 3 and 4

Claims 3 and 4 depend from claim 1. Ex. 1001, 5:29–6:5. Petitioner directs us to portions of Saxler that disclose or suggest the limitations in these claims. Pet. 52. At this stage of the proceeding, Patent Owner does not separately dispute that Saxler discloses or suggests the limitations in claims 3 and 4.

After reviewing the evidence and arguments Petitioner presents in the Petition, including the relevant portions of the supporting Shealy Declaration, we are persuaded Petitioner has established a reasonable likelihood of prevailing on its obviousness challenge with respect to these claims.

c) Claims 2 and 5–7

Claim 2, which depends from claim 1, independent claim 5, and claims 6 and 7, which depend from claim 5, each require ledges that are “self-aligned.” Ex. 1001, 5:26–28, 6:6–30. As discussed above, the parties dispute whether “self-aligned” is a product-by-process limitation, and we have deferred our decision on that issue at this stage to allow the parties to further address it during the course of trial. In view of this, and because it is not necessary for purposes of this Decision, we decline to further address Petitioner’s challenge that claims 2 and 5–7 are unpatentable as obvious in view of Saxler.

2. Conclusion

For all of the foregoing reasons, we determine Petitioner has established a reasonable likelihood of prevailing on its challenge that claims 1, 3, and 4 are unpatentable as obvious in view of Saxler.

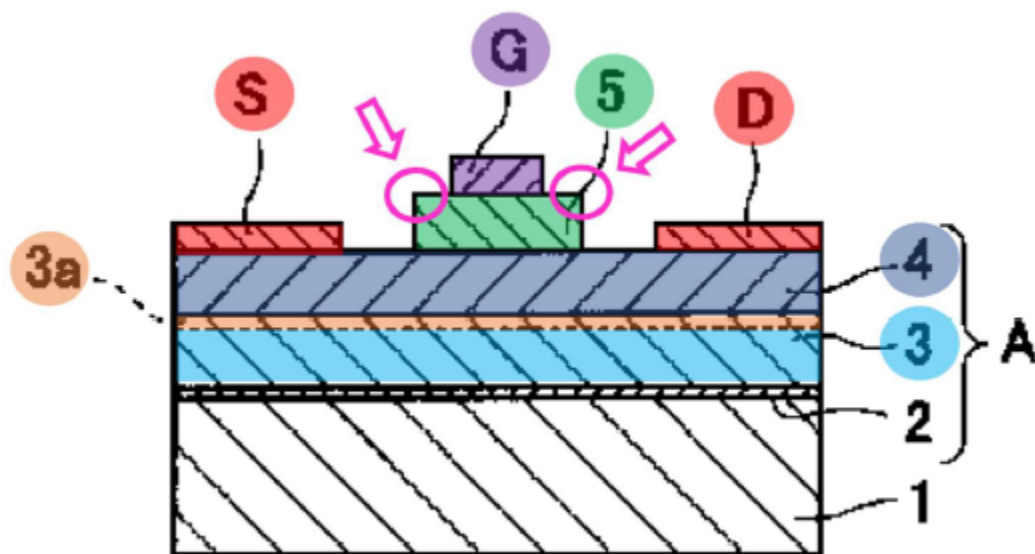
Because Petitioner has demonstrated a reasonable likelihood that at least one challenged claim of the ’335 patent is unpatentable over the prior art of record, we institute an *inter partes* review. And because we find some grounds sufficient for institution, we institute on all grounds in the petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1353 (2018) (“The agency cannot curate the claims at issue but must decide them all.”); *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute as requiring “a simple yes-or-no institution choice respecting a

petition, embracing all challenges included in the petition”). Nevertheless, in order to further guide the parties after institution, we provide the following observations.

E. Claims 1–7 – Alleged Obviousness in view of Saxler and Yoshida

Petitioner contends claims 1–7 of the ’335 patent are unpatentable as obvious over Saxler in view of Yoshida. Pet. 24–56. Patent Owner challenges Petitioner’s arguments. Prelim. Resp. 28–33.

Petitioner states that Yoshida discloses an enhancement-mode GaN transistor having the configuration shown in Figure 1, reproduced below with annotations from Petitioner. Pet. 27–28.



Annotated Figure 1 of Yoshida shows a cross-sectional view of a transistor having GaN layer 3 (highlighted in light blue) and n-type semiconductor layer 4 (highlighted in dark blue) formed over barrier layer 2 and substrate 1, with 2DEG 3a (highlighted in orange) forming at the interface of layers 3 and 4. Pet. 27–28; Ex. 1006 ¶ 10. Figure 1 also depicts source contact S and drain contact D (both highlighted in red) and a stacked gate structure

above semiconductor layer 4 consisting of gate metal G (highlighted in purple) overlaying GaN layer 5 (highlighted in green). Pet. 27–28; Ex. 1006

¶ 10. The stacked gate structure includes a pair of horizontal ledges (highlighted in pink) on either side of gate metal G. Pet. 27–28; Ex. 1006
¶ 10, Fig. 1.

Petitioner contends that implementing Yoshida’s non-recessed gate structure in Saxler’s gate structure would result in the same arrangement as Saxler’s non-recessed embodiment shown in modified Figure 1A of Saxler. Pet. 28–29. Petitioner relies on the same arguments discussed above regarding modified Figure 1A of Saxler to demonstrate the combined teachings of Yoshida and Saxler disclose or suggest all limitations in claims 1–7. Pet. 35–56.

Petitioner contends it would have been obvious to combine Saxler’s stacked gate structure with Yoshida’s non-recessed gate structure because (1) a person of ordinary skill in the art would have been familiar with a wide variety of stacked gate structures in GaN HEMT devices, including many without recessed gates, (2) Saxler repeatedly teaches that its gate recess is optional, and (3) a person of ordinary skill in the art would have removed Saxler’s gate recess to “turn Saxler’s device into an enhancement mode device, thus realizing the benefits of reduced power consumption and suitability for high power applications.” Pet. 32–33.

Petitioner also contends a person of ordinary skill in the art would have been motivated to use Yoshida’s non-recessed gate fabrication techniques to simplify manufacturing and decrease costs. Pet. 32. In particular, Petitioner contends that creating a gate recess requires complicated and exacting manufacturing processes which raises costs. Pet. 32. Petitioner asserts that a person of ordinary skill in the art would

have been familiar with methods for making stacked, stepped gate structures, and would have understood that these techniques are less complicated and cost less than methods for making recessed gate structures. Pet. 32.

Accordingly, Petitioner argues that a person of ordinary skill in the art would have “found the combination of Yoshida’s non-recessed gate arrangement in Saxler’s gate arrangement nothing more than the simple substitution of known elements to predictably yield an enhancement mode GaN HEMT device.” Pet. 34.

Patent Owner argues that the side surfaces of Yoshida’s p-type GaN layer are vertical, and therefore they do not extend horizontally towards the source and drain contact as claim 1 requires. Prelim. Resp. 30–31. This argument, however, is inapposite, as Petitioner does not rely on Yoshida’s structure alone to satisfy this limitation.

Patent Owner next contends that the combined teachings of Yoshida and Saxler do not disclose a pair of horizontal ledges that have substantially equal widths, again arguing that Petitioner improperly relies on patent drawings in Yoshida and Saxler to teach this limitation. Prelim. Resp. 31–32. For the reasons discussed above, we disagree with Patent Owner’s assertion that Petitioner’s reliance on the figures in Yoshida and Saxler is improper. *See* § II.D.1.a.iv, *supra*.

Patent Owner also contends that a person of ordinary skill in the art would not have been motivated to combine the teachings of Saxler and Yoshida. Prelim. Resp. 33. Patent Owner contends that Saxler and Yoshida are substantially different, as Saxler is directed to a device having a recessed-gate and is inoperable in enhancement-mode, whereas Yoshida discloses an operable, enhancement-mode transistor having a non-recessed

gate. Prelim. Resp. 33. Patent Owner thus argues that a person of ordinary skill in the art would not have been motivated to combine features from Saxler's device that cannot operate in enhancement-mode into Yoshida's operable enhancement-mode device "as what is favorable to enhancement mode operation could be detrimental to depletion mode, and vice versa." Prelim. Resp. 33.

As discussed above, however, we are persuaded, at this stage, by Petitioner's argument that that Saxler teaches or suggests an operable enhancement-mode device. *See* § II.D.1.a.i, *supra*. Additionally, Patent Owner's argument regarding modifications that "could be detrimental" to certain devices is not only speculation, but also comprised entirely of attorney argument. Finally, Patent Owner does not directly address Petitioner's arguments and accompanying evidence that a person of ordinary skill in the art would have had reason to combine the teachings of Saxler and Yoshida to take advantage of simplified manufacturing steps and reduced costs.

Based on the present record, Petitioner has sufficiently shown that Saxler and Yoshida disclose or suggest all of the limitations in claims 1, 3, and 4, and that a person of ordinary skill in the art would have had a reason to combine the teachings of Saxler and Yoshida with a reasonable expectation of success. Accordingly, we determine Petitioner has established a reasonable likelihood of prevailing on its challenge that claims 1, 3, and 4 are unpatentable as obvious in view of Saxler and Yoshida. For the same reasons as noted above, we decline to address Petitioner's challenge of claims 2 and 5–7 based on Saxler and Yoshida alone at this stage. *See* § II.D.1.c, *supra*.

F. Claims 2 and 5–7 – Alleged Obviousness in view of Saxler, Yoshida, Beach, and Shenoy

Petitioner argues that to the extent “self-aligned” is not a product-by-process limitation, the combination of Saxler, Yoshida, Beach, and Shenoy renders obvious the subject matter of claims 2 and 5–7. Pet. 57–67. In particular, Petitioner contends that Beach discloses a self-aligned method of making stacked gate structures in GaN HEMT devices using a single mask, and Shenoy discloses isotropic etching techniques for undercutting metal below photoresist masks. Pet. 57–58 (citing Ex. 1008 ¶¶ 40, 45, 54; Ex. 1009, 2–3). Petitioner contends it would have been obvious to make the stacked gate structure of the combined Saxler-Yoshida device using the methods of Beach and Shenoy. Pet. 59.

According to Petitioner, self-aligned techniques were common in the field as of the priority date of the ’335 patent, and Sheppard, incorporated by reference in Saxler to disclose methods of fabricating GaN transistors, describes a flexible approach to masking and etching. Pet. 61–62 (citing Ex. 1007 ¶¶ 46, 68; Ex. 1021 ¶ 58; Ex. 1003 ¶¶ 160–161). Petitioner further contends that a person of ordinary skill in the art would have created the Saxler-Yoshida stepped gate structure by using Beach’s self-aligned technique and Shenoy’s isotropic undercutting to improve reproducibility and symmetry of the gate contact with respect to the gate layer. Pet. 60–61. Petitioner also asserts Beach and Shenoy’s techniques reduce masking steps and costs. Pet. 61 (citing Ex. 1003 ¶ 159). Petitioner contends that using Beach’s manufacturing steps and Shenoy’s isotropic techniques would have involved simple substitutions that could be predictably implemented in Saxler’s flexible method of manufacturing. Pet. 63.

Patent Owner does not directly address Petitioner’s arguments and supporting evidence regarding improving reproducibility and symmetry, and reducing masking steps and costs. *See* Prelim. Resp. 34–39. Rather, Patent Owner argues that Beach’s gate-first fabrication process is incompatible with Saxler’s gate-last fabrication process and that the devices in Saxler and Beach have different structures such that the teachings of the references could not have been effectively combined. Prelim. Resp. 35. Patent Owner’s arguments, however, fail to account adequately for Saxler’s disclosure (via incorporating Sheppard by reference) of a flexible approach in forming devices. *See* Ex. 1021 ¶¶ 57–58. Moreover, we understand Petitioner’s argument to involve using Beach’s process instead of Saxler’s, not combining the steps of the two methods.

Patent Owner also argues that Beach’s self-aligned process does not include ledges, and “Petitioner does not address how a [person of ordinary skill in the art] would have proceeded to manufacture the ledges depicted in *Saxler* using the process described in *Shenoy* after a self-aligned etching process has already occurred.” Prelim. Resp. 37. According to Patent Owner, Petitioner fails to address the differences in structures and teachings between the asserted references. Prelim. Resp. 38.¹² In addition, Patent Owner contends that Shenoy describes electrochemical etching, a highly

¹² In the heading of Section VII.B of the Preliminary Response, Patent Owner states that Shenoy is non-analogous art, but does not include a proper analysis using the tests set forth in *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004). Petitioner provides a proper analogous art analysis in its Reply, which Patent Owner does not address in its Sur-reply. For purposes of this Decision, based on the undisputed arguments and evidence Petitioner presents in its Reply, we are persuaded that Shenoy is analogous art. Reply 5–10.

specialized method, and asserts that a person of ordinary skill in the art would not have considered the materials used and the structure etched in Shenoy to be related to Saxler or Beach. Prelim. Resp. 38–39.

After considering the parties’ arguments regarding Shenoy, we have some concerns about Petitioner’s treatment of that reference. Petitioner contends that Shenoy “discloses simple isotropic etching techniques for symmetrically undercutting metal layers below photoresist masks.” Pet. 63 (citing Ex. 1009, 2–3; Ex. 1003 ¶ 162). Dr. Shealy likewise states “*Shenoy* discloses techniques to isotropically etch and undercut metal layers below masks, which a [person of ordinary skill in the art] would understand would be one method of forming stepped gate structures.” Ex. 1003 ¶¶ 62, 153 (stating Shenoy describes “well known techniques of using isotropic etching to undercut the metal below photoresist masks”). It is not clear, however, what isotropic etching techniques, other than EMM, Shenoy discloses or suggests to a person of ordinary skill in the art. Petitioner and Dr. Shealy fail to direct us to evidence adequate to support the assertion that Shenoy broadly discloses multiple isotropic etching techniques. This is especially true considering Shenoy states that its “principal objective is to determine how deviations ($\pm 10^\circ$) in the mask wall angle affect the directionality of through-mask EMM.” Ex. 1009, 2.

Dr. Shealy also states that “Shenoy provides method[sic] to control the ‘undercut U,’ illustrated in Figure 1, which evolves symmetrically on both sides of a symmetric photomask such that the width of the etched metal structure is less than the photomask.” Ex. 1003 ¶ 153 (citing Ex. 1009, 2–3) (emphasis omitted). But the only discussion of symmetry on pages 2–3 in Shenoy appears in a section titled “Assumptions,” and refers to the “assumptions . . . made in the development of the model for shape evolution

during through-mask EMM.” Ex. 1009, 2. It is not evident how these pages of Shenoy, addressing assumptions for Shenoy’s model, support Dr. Shealy’s statement.

Furthermore, we agree with Patent Owner that there are structural differences between the patterned electrode shown in Figure 1 of Shenoy and the structure that results from Beach’s self-aligned process. Prelim. Resp. 37–39. Figure 1 of Shenoy and Figure 1 of Beach are reproduced below.

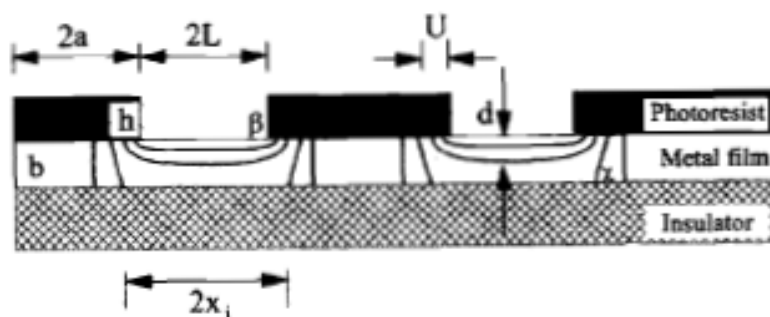


Figure 1 of Shenoy depicts a schematic diagram of a metal film supported on an insulator, and covered with patterned photoresist. Ex. 1009, 2.

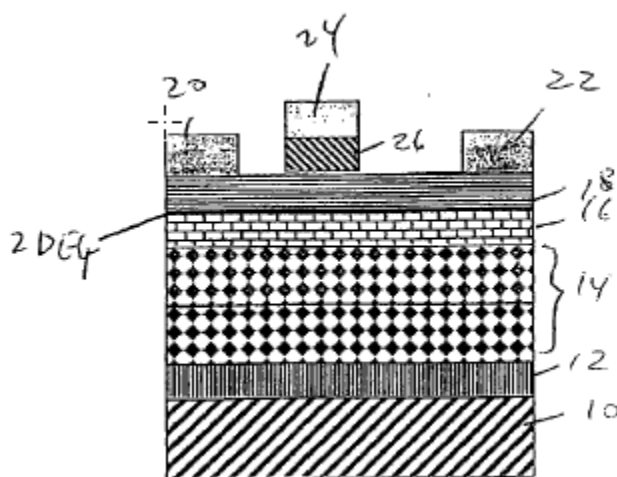


Figure 1 of Beach shows a cross-sectional view of a semiconductor device including substrate 10, bonding layer 12, first III-nitride buffer body 14, first III-nitride semiconductor body 16, second III-nitride semiconductor body

18, power electrodes 20, 22, gate barrier 26, and gate arrangement 24. Ex. 1008 ¶¶ 19, 31–32. According to Beach, gate barrier 26 is an alloy, preferably AlGaIn. Ex. 1008 ¶ 32.

Notably, the undercutting in Shenoy based on EMM refers to etching a metal layer beneath a photoresist and above an insulator. Ex. 1009, 2–3, Fig. 1. Petitioner does not explain sufficiently how Shenoy’s EMM technique would work on the stacked gate structure in Beach to etch only gate arrangement 24, positioned between a photoresist mask (assuming one is present) and an AlGaIn semiconductor layer, which is not an insulator, to form the self-aligned horizontal ledges required in the challenged claims.

Furthermore, Shenoy addresses “metal wall profile evolution” on pages 5–6, but neither Dr. Shealy nor Petitioner address these teachings. See Ex. 1009, 5–6. For example, Shenoy explains that “[t]he extent of the metal removal necessary to obtain a certain metal wall angle can be expressed in terms of the ratio of undercut to metal film thickness.” Ex. 1009, 6. Petitioner, however, does not address how or whether the mask wall angle or metal film thickness would affect undercutting in Beach’s structure when attempting to form symmetrical ledges.

For all of the foregoing reasons, we have concerns regarding Petitioner’s assertion that using Shenoy’s isotropic techniques would have been a simple substitution that could be predictably implemented in Saxler’s flexible method of manufacturing and combined with Beach’s methods. Pet. 63.

G. Claims 1–7 – Alleged Obviousness in view of Yoshida

Petitioner contends that Yoshida discloses or suggest the arrangement of semiconductor layers and structures recited in claims 1–7. Pet. 67–68.

Petitioner directs us to portions of Yoshida disclosing or suggest each limitation of the challenged claims. Pet. 71–88.

Regarding limitation [1d], which requires “p-type gate material having side surfaces extending horizontally towards the source contact and drain contact,” Petitioner acknowledges that Yoshida Figure 1 depicts the walls of its p-type GaN material as substantially vertical, but argues that a person of ordinary skill in the art “would know any constructed embodiment would necessarily extend at least slightly on the bottom due to manufacturing tolerances.” Pet. 67–68 (citing Ex. 1003 ¶¶ 182, 203–205), 75 (arguing a person of ordinary skill in the art “would have known a sidewall drawn vertically would have a slight slope when built in a practical device”).

In support, Petitioner directs us to Saxler’s disclosure that “an etched region illustrated as a rectangle will, typically, have *tapered*, rounded or curved features.” Pet. 76 (citing Ex. 1007 ¶ 42; Ex. 1003 ¶ 204). Additionally, Petitioner directs us to another prior art reference, Uemoto,¹³ that depicts its p-AlGaIn gate layer having vertical sidewalls in its drawings (e.g., Figure 1), but shows sloped sidewalls in an image of a device built according to the drawings. Pet. 76–77 (citing Ex. 1020, Figs. 1, 2, 5; Ex. 1003 ¶ 204). According to Petitioner, a person of ordinary skill in the art “would have recognized that *Yoshida*’s sidewalls would have had a taper in practical implementations, and Yoshida alone thereby renders obvious [1d].” Pet. 77–78.

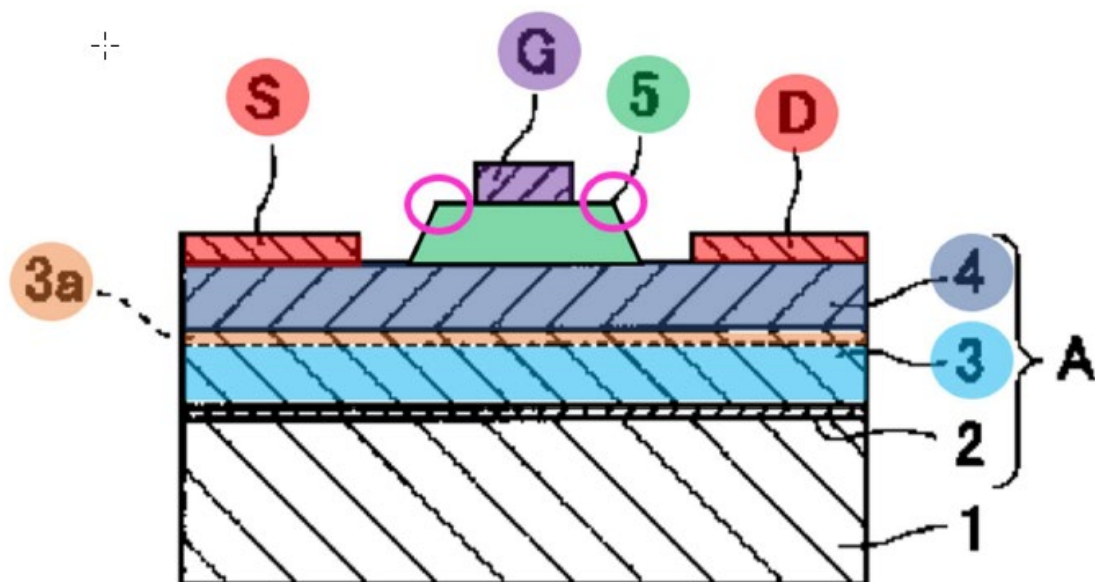
¹³ Uemoto et al., *A Normally-off AlGaIn/GaN Transistor with $R_{on}A=2.6\Omega\text{cm}^2$ and $BV_{ds}=640\text{V}$ Using Conductivity Modulation*, IEEE Paper, 2006 (Ex. 1020).

Patent Owner contends that “Petitioner provides no evidence that a [person of ordinary skill in the art] would understand the vertical side surfaces of the p-GaN layer (5) of *Yoshida* to have a wider bottom surface than top surface.” Prelim. Resp. 40. We disagree. Petitioner has directed us to at least some evidence in Saxler and Uemoto, as well as provided testimony from Dr. Shealy, all of which is unrebutted on this record.

Regarding the “substantially equal widths” limitation in [1f], Petitioner relies on Figure 1 of *Yoshida*. Pet. 83. Patent Owner relies on the same arguments discussed above regarding the impropriety of relying on patent figures alone for this limitation. Prelim. Resp. 32, 40. For the reasons discussed above, we disagree with Patent Owner’s assertion that Petitioner’s reliance on the figure in *Yoshida* improper. See § II.D.1.a.iv, *supra*.

H. Claims 1–7 – Alleged Obviousness in view of Yoshida and Saxler

Petitioner argues that to the extent *Yoshida* alone does not disclose or suggest “side surfaces extending horizontally towards the source contact and drain contact” as claim 1 requires, the combined teachings of *Yoshida* and Saxler satisfy this limitation in view of Saxler’s disclosure of sloped sidewalls. Pet. 68. Petitioner contends that implementing Saxler’s sloped sidewalls in *Yoshida*’s GaN layer 5 would result in the structure depicted in modified Figure 1 of *Yoshida*, reproduced below. Pet. 68–69.



Modified Figure 1 of Yoshida shows a cross-sectional view of a transistor having GaN layer 3 (highlighted in light blue) and n-type semiconductor layer 4 (highlighted in dark blue) formed over barrier layer 2 and substrate 1, with 2DEG 3a (highlighted in orange) forming at the interface of layers 3 and 4. Pet. 68–69. Figure 1 also depicts source contact S and drain contact D (both highlighted in red) and a stacked gate structure above semiconductor layer 4 consisting of gate metal G (highlighted in purple) overlaying GaN layer 5 (highlighted in green), modified to show sloped sidewalls. Pet. 68–69. The stacked gate structure includes a pair of horizontal ledges (highlighted in pink) on either side of gate metal G. Pet. 69.

Petitioner contends that modifying Yoshida to include Saxler’s sloped sidewalls “calls for nothing more than simple substitution . . . to predictably make an enhancement-mode GaN HEMT,” and that a person of ordinary skill in the art would have made the proposed modification to reduce gate leakage. Pet. 69–70 (citing Ex. 1003 ¶¶ 185–189). In particular, Petitioner contends that (1) sloped sidewalls were conventional, (2) the angle of Saxler’s sloped sidewall is typical for mesa structures, (3) Saxler discloses

conventional etching techniques for forming its sloped sidewalls, and (4) “[i]t was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage.” Pet. 70–71 (citing Ex. 1003 ¶¶ 185–189); Ex. 1014¹⁴, 1; Ex. 1019¹⁵ ¶¶ 13, 27, 144, 157, Fig. 12A).

Patent Owner again argues that Saxler is not an enhancement-mode device, and a person of ordinary skill in the art would not be motivated to incorporate features from Saxler’s recessed gate device, which cannot operate in enhancement-mode, into Yoshida’s operable enhancement-mode device. Prelim. Resp. 41–42 (repeating the argument that “what is favorable to enhancement mode operation could be detrimental to depletion mode, and vice versa”).

As discussed above, however, we disagree with Patent Owner’s contention that Saxler fails to disclose an operable enhancement-mode device. *See* § II.D.1.a.i, *supra*. Furthermore, Patent Owner’s arguments ignore Saxler’s teachings regarding non-recessed embodiments. Additionally, Patent Owner’s argument regarding modifications that “could be detrimental” to certain devices is not only speculation, but also comprised entirely of attorney argument. Finally, Patent Owner does not directly address Petitioner’s arguments and accompanying evidence regarding what was conventional and known in the art at the relevant time, such that a person of ordinary skill in the art would have had reason to combine the

¹⁴ Xu et al., *The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure*, IEEE ELECTRON DEVICE LETTERS, Vol. 28, No. 11, 942 (Nov. 2007).

¹⁵ Kanda et al., US 2005/0087763 A1, published Apr. 28, 2005.

teachings of Yoshida and Saxler to take advantage of Saxler's sloped sidewalls.

Based on the present record, we are persuaded by Petitioner's arguments and evidence that Yoshida and Saxler disclose or suggest all of the limitations in claims 1, 3, and 4, and that a person of ordinary skill in the art would have had a reason to combine the teachings of Yoshida and Saxler with a reasonable expectation of success. Accordingly, we determine Petitioner has established a reasonable likelihood of prevailing on its challenge that claims 1, 3, and 4 are unpatentable as obvious in view of Yoshida and Saxler. For the same reasons as noted above, we decline to address Petitioner's challenge of claims 2 and 5–7 based on Yoshida and Saxler alone at this stage. *See* § II.D.1.c, *supra*.

I. Claims 2 and 5–7 – Alleged Obviousness in view of Yoshida, Saxler, Beach, and Shenoy

Petitioner argues that to the extent “self-aligned” is not a product-by-process limitation, the combination of Yoshida, Saxler, Beach, and Shenoy renders obvious the subject matter of claims 2 and 5–7. Pet. 88–96. Petitioner and Patent Owner present arguments here that are similar to those discussed above in Section II.F, *supra*. Accordingly, we reach the same conclusion here as above.

III. CONCLUSION

Because Petitioner has demonstrated a reasonable likelihood that at least one challenged claim of the '335 patent is unpatentable over the prior art of record, we institute an *inter partes* review of all challenged claims. And because we find some grounds sufficient for institution, we institute on all grounds in the petition. *See SAS*, 138 S. Ct. at 1353 (2018); *PGS Geophysical*, 891 F.3d at 1360.

At this stage of the proceeding, we have not made a final determination with respect to the patentability of any challenged claim or any underlying factual or legal issue, including claim construction.

IV. ORDER

For the reasons given, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–7 of the '335 patent is instituted with respect to all grounds of unpatentability asserted in the Petition, commencing on the entry date of this Decision; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial.

IPR2023-01384
Patent 10,312,335 B2
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