

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

—
Case IPR2023-01384
U.S. Patent No. 10,312,335

PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

	Page
I. Introduction.....	1
II. The '335 Patent.....	4
III. Claim Construction.....	7
IV. Rebuttal to Statement of Facts.....	8
V. Level of Ordinary Skill in the Art	8
VI. Overview of the References Relied upon by Petitioner	9
A. Saxler.....	9
B. Yoshida.....	10
C. Beach	14
D. Shenoy	15
VII. Ground 1 (Claims 1-7) – Saxler Alone.....	16
A. A POSA would not consider the gate recess of Saxler as “optional” based on Saxler’s two distinct embodiments	16
B. Petitioner’s proposed modification of Saxler does not produce a operable method for manufacturing an enhancement mode transistor	22
C. Petitioner improperly relies upon Fig. 1A of Saxler as disclosing the pair of horizontal ledges “having substantially equal widths” recited in independent claim 1	29
D. Petitioner’s attempt to avoid the holding in <i>Hockerson</i> should be rejected	31
1. Saxler explicitly discloses that drawings are “schematics” and “their shapes are not intended to illustrate the precise shape of a region of a device”	35

2.	Saxler explicitly discloses that the gate electrode is to be “offset”	37
E.	Petitioner fails to show that the “self-aligned” ledges of claims 2 and 5 are obvious.....	38
VIII.	Ground 2 (Claims 1-7) – Saxler in view of Yoshida.....	44
A.	Saxler in view of Yoshida does not disclose “substantially equal ledges”	44
B.	Saxler in view of Yoshida does not disclose “self-aligned” ledges....	45
C.	A POSA would not modify the recessed embodiment of Saxler by removing the recess based on Yoshida	45
1.	A POSA would not modify Saxler by changing its principle operation.....	46
2.	A POSA would not modify Saxler in view of Yoshida for the very same reason that Saxler distinguishes from its recessed embodiment and non-recessed embodiment	47
D.	Petitioner’s modification of Saxler in view of Yoshida does not produce an enhancement mode transistor	47
IX.	Ground 3 (Claims 2 and 5-7) – Saxler in view of Yoshida, Beach, and Shenoy	48
A.	The etching in Beach is incompatible with Saxler.....	50
B.	The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges based on Petitioner’s reasoning.....	50
C.	A POSA would not have found it obvious to combine Saxler, Beach, and Shenoy	56
1.	Petitioner has not articulated a reason for POSA to combine all three references	56
2.	Petitioner fails to provide sufficient specifics on how the proposed method would actually be performed.....	57

3.	Petitioner mischaracterizes the method of Saxler as being “flexible” in alleging complete freedom to modify Saxler.....	57
X.	Ground 4 (Claims 1-7) – Yoshida Alone	59
A.	Yoshida does not disclose the pair of horizontal ledges have substantially equal widths of independent claim 1	59
1.	The schematic of Fig. 1 cannot be relied on to show “substantially equal ledges”	59
B.	Petitioner’s reliance on the inherency of horizontally extending sidewalls is misdirected.....	61
C.	Petitioner fails to address the “self-aligned” ledges of claims 2 and 5	62
XI.	Ground 5 (Claims 1-7) – Yoshida in view of Saxler.....	62
A.	Petitioner makes no additional argument with respect to the claimed “substantially equal widths”	62
B.	A POSA would not have modified Yoshida with the sloped sidewalls of Saxler.....	63
C.	The “self-aligned” ledges of claims 2 and 5 are absent from Yoshida.....	7
XII.	Ground 6 (Claims 2 and 5-7) – Yoshida in view of Saxler, Beach, and Shenoy	67
A.	In modifying Yoshida, Petitioner relies on contradictions and improper assumptions to allegedly arrive “at the same gate structure”	67
B.	The “self-aligned” technique of <i>Beach</i> would not produce the sloped sidewalls of Saxler-Yoshida, as relied on by Petitioner	68
C.	A POSA would not have any reason to form ledges after the self-aligned process of Beach.....	68

D.	The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges based on Petitioner’s reasoning.....	72
E.	Yoshida teaches away from using other methods of manufacturing its gate.....	73
F.	A POSA would not have found it obvious to combine Yoshida, Saxler, Beach, and Shenoy	74
XIII.	Reservation of Rights	74
XIV.	Conclusion	75

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>ActiveVideo Networks, Inc. v. Verizon Commc’n, Inc.</i> , 694 F.3d 1312 (Fed. Cir. 2012).....	57
<i>Amgen Inc. v. F. Hoffman-La Roche Ltd.</i> , 580 F.3d 1340 (Fed. Cir. 2009).....	39
<i>Continental Can Co. USA, Inc. v. Monsanto Co.</i> , 948 F.2d 1264 (Fed. Cir. 1991).....	61
<i>Ex parte Bjorn</i> , No. 2018-001567, 2019 WL 6173305 (P.T.A.B. Oct. 16, 2019)	3, 32, 35
<i>Go Med. Indus. Pty, Ltd. v. Inmed Corp.</i> , 471 F.3d 1264 (Fed. Cir. 2006).....	32
<i>Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.</i> , 222 F.3d 951 (Fed. Cir. 2000).....	2, 3, 31, 32, 33, 34, 35, 60, 74
<i>In re Gorman</i> , 933 F.2d 982 (Fed. Cir. 1991).....	58
<i>In re Ratti</i> , 270 F.2d 810, 123 USPQ 349 (CCPA 1959)	46
<i>In re Robertson</i> , 169 F.3d 743 (Fed. Cir. 1999).....	61
<i>In re Wright</i> , 569 F.2d 1124 (CCPA 1977)	3, 32, 33
<i>Microsoft Corporation v. Biscotti, Inc.</i> , 878 F.3d 1052 (Fed. Cir. 2017).....	18
<i>Mueller Sports Med., Inc. v. Sportstar Athletics, Inc.</i> , 385 F. Supp. 2d 775 (W.D. Wisc. 2005).....	34
<i>Net MoneyIN, Inc. v. VeriSign, Inc.</i> , 545 F.3d 1359 (Fed.Cir.2008).....	18
<i>Rexnord Indus., LLC v. Kappos</i> , 705 F.3d 1347 (Fed. Cir. 2013).....	62

Other Authorities

37 C.F.R. § 42.22(c).....	8
MPEP § 2143.01	46

TABLE OF PETITIONER’S EXHIBIT LIST

<u>Exhibit</u>	<u>Description of Exhibit</u>
1001	U.S. Patent No. 9,748,347 B2 to Cao et al. (“the ’347 patent”)
1002	Prosecution History of the ’335 patent
1003	Declaration of Dr. James Richard Shealy
1004	Curriculum Vitae of Dr. James Richard Shealy
1005	Japanese Patent Publication No. JP H11-261053 to Yoshida
1006	Certified Translation of Japanese Patent Publication No. JP H11 261053 to Yoshida (“Yoshida”)
1007	U.S. Patent Application Publication No. US 2006/0108606 A1 to Saxler et al. (“Saxler”)
1008	U.S. Patent Application Publication No. US 2007/0007547 A1 to Beach (“Beach”)
1009	R.V. Shenoy and M. Datta, Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining, 143 J. Electrochemical Soc’y, pp. 544-549 (1996) (“Shenoy”)
1010	U.S. Patent No. 5,905,274 to Ahn et al. (“Ahn”)
1011	U.S. Patent Application Publication No. US 2010/0258843 A1 to Lidow et al. (“Lidow”)
1012	U.S. Patent No. 9,748,347 to Cao et al. (“the ’347 patent”)
1013	Prosecution History of the ’347 patent
1014	Chua Xu et al., <i>The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure</i> , 28 IEEE Electron Device Letters, pp. 942-944 (2007) (“Xu”)

1015	U.S. Patent Application Publication No. US 2002/0066908 A1 to Smith (“Smith”)
1016	U.S. Patent Application Publication No. US 2006/0273347 A1 to Hikita et al. (“Hikita”)
1017	U.S. Patent Application Publication No. US 2009/0072272 A1 to Suh et al. (“Suh”)
1018	X. Hu et al., Enhancement mode AlGaIn/GaN HFET with selectively grown pn junction gate, 36 Electronics Letters, pp. 753-754 (2000) (“Hu”)
1019	U.S. Patent Application Publication No. US 2005/0087763 A1 to Kanda et al. (“Kanda”)
1020	Yasushiro Uemoto et al., <i>A Normally-off AlGaIn/GaN Transistor with $R_{onA}=2.6\Omega\text{cm}^2$ and $BV_{ds}=640\text{V}$ Using Conductivity Modulation</i> , 2006 International Electron Devices Meeting, IEEE (2006) (“Uemoto”)
1021	U.S. Patent Application Publication No. US 2006/0019435 A1 to Sheppard et al. (“Sheppard”)
1022	Order Granting Defendants’ Unopposed Motion for Stay Pending ITC Proceeding, Case No. 2:23-cv-04026-AB-AS, Central District of California (July 27, 2023)
1023	Dietrich W. Widmann, Metallization for Integrated Circuits Using a Lift-Off Technique, 11 IEEE Journal of Solid-State Circuits, pp. 466-471 (1976) (“Widmann”)
1024	RESERVED
1025	Declaration of Kelley Hayes Greenhill
1026	Declaration of Shauna Wiest
1027	International Publication No. WO 2005/057624 to Beach, published June 23, 2005 (“Beach-II”)

1028	Petitioner and Complainant’s Proposed Claim Construction, ITC 337 TA-1366
1029	C. S. Suh et al., “p-GaN/AlGaIn/GaN Enhancement mode HEMTs, 2006 64th Device Research Conference, June 2006, pp. 163-164 (“Suh 2006”)
1030	Excerpt of the Declaration of Dr. Eric Fred Schubert in Support of Complainant’s Opening Claim Construction Brief
1031	Excerpt of Complainant’s Supplemental Responses to Respondent’s Supplemental Invalidity Contentions

TABLE OF PATENT OWNER'S EXHIBIT LIST

<u>Exhibit</u>	<u>Description of Exhibit</u>
2001	Patent Owner's Notice of Deposition of Dr. James Shealy
2002	Diagram produced by Dr. James Shealy during Deposition on May 16, 2024
2003	Diagram produced by Dr. James Shealy during Deposition on May 16, 2024
2004	Certified Transcript of Oral Deposition of Dr. James Shealy
2005	Declaration of Dr. E. Fred Schubert
2006	Curriculum Vitae of Dr. E. Fred Schubert
2007	Petition for Inter Partes Review of U.S. Patent. No. 9,748,347
2008	Evidentiary Hearing Transcript, pages 741-984 (Inv. No. 337-TA-1366) (Public)
2009	Respondents' Post-Hearing Initial Brief (Inv. No. 337-TA-1366)

I. INTRODUCTION

On March 26, 2024, the Board issued a Decision (Paper 11) granting *inter partes* review of claims 1-7 of U.S. Patent No. 10,312,335 (the '335 patent") on each of six grounds raised by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. ("Petitioner").

All grounds raised in the Petition (Paper 1) allege obviousness of the challenged claims. The grounds (as summarized below) rely on one or more of U.S. Patent Application Publication 2006/0108606 ("Saxler")¹, Japanese Publication 2290799 ("Yoshida")², U.S. Patent Application Publication 2007/0007547 ("Beach")³, and non-patent literature entitled "*Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining*" ("Shenoy")⁴. Each of the grounds is fatally flawed and the patentability of the claims should be sustained for the reasons discussed herein.

Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	Saxler in view of knowledge of a POSITA
2	1-7	§ 103	Saxler in view of Yoshida
3	2, 5-7	§ 103	Saxler in view of Yoshida, Beach, and Shenoy

¹ Ex. 1007.

² Ex. 1006.

³ Ex. 1008.

⁴ Ex. 1009.

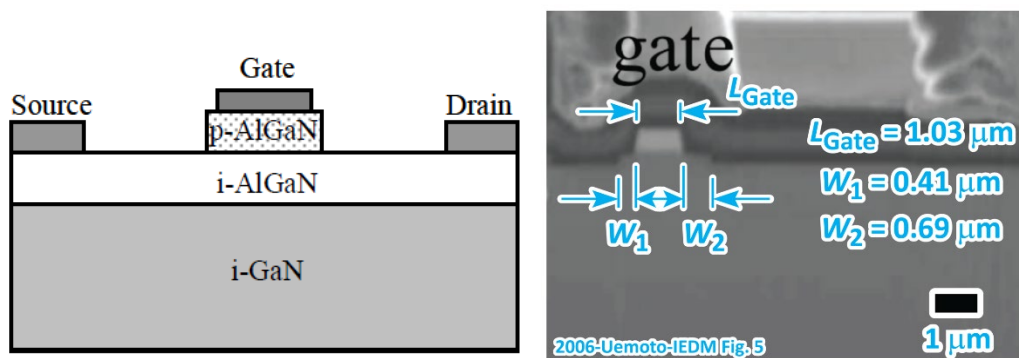
4	1-7	§ 103	Yoshida in view of knowledge of a POSITA
5	1-7	§ 103	Yoshida in view of Saxler
6	2, 5-7	§ 103	Yoshida in view of Saxler, Beach, and Shenoy

At the outset, Saxler and Yoshida present different devices that operate in different ways. Saxler is indisputably not an enhancement mode device. Yoshida, on the other hand, is an enhancement mode device. A POSA would not have been motivated to combine the two disparate references, much less combine additional prior art references as proposed by Petitioner.

In addition, both primary references disclose specific processes with specific process steps that could not have achieved the claimed structure, either alone or in combination. Notably, both primary references disclose “gate last” processes. The proposed combination of these references with Beach fails, because Beach discloses a “gate first” process, which would completely remove the ledges of Saxler and Yoshida.

Fatal to Petitioner’s arguments regarding both primary references is the simple fact that the Petitioner relies solely on schematic drawings that cannot be relied on to show “substantially equal widths.” *See, e.g., Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“Under our precedent, however, it is well established that patent drawings do not define the

precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.”); *see also In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977). Petitioner cites additional case law in an attempt to find an exception from *Hockerson* for the present case, but that very case law negates their argument. *Ex parte Bjorn*, No. 2018-001567, 2019 WL 6173305 *14 (P.T.A.B. Oct. 16, 2019) (finding “even if we determine what percentage or ratio of an oversized abutment diameter is permitted within the scope of the claim, the drawings cannot be relied on to disclose such precise or relative proportions” in addressing “substantially equal”). Petitioner further discredits the accuracy of the very schematics that they rely on to read on the present claims. Indeed, Dr. Shealy admitted, as he had to, that the ledges of Uemoto do not have “substantially equal widths,” even though Uemoto, like Saxler and Yoshida, represents the transistor with schematics illustrating a gate with a centrally aligned electrode contact.



Pet. 76 (EX1020, Fig. 1)

Pet. 76 (EX1020, Fig. 5 annotated)

Comparison of Uemoto's Drawing and Actual Device

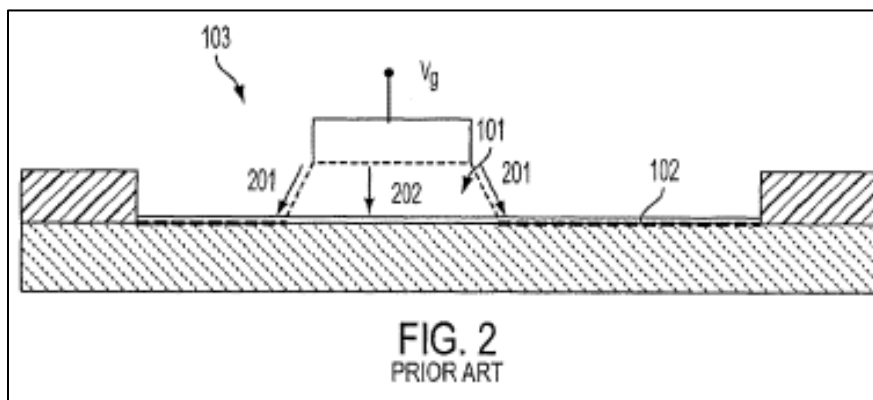
II. THE '335 PATENT

The '335 Patent issued on June 4, 2019 from an application filed on July 20, 2017. The '335 Patent arose from an application that was a divisional application from the application that became U.S. Patent No. 9,748,347. Therefore, the '335 Patent claims priority to a United States Provisional Applications filed on August 1, 2013, as well as claims priority through U.S. Patent No. 8,890,168 to a United States provisional patent application filed on April 8, 2009, which also led to the U.S. Pat. No. 8,404,508 (“the '508 Patent”).

The '335 Patent describes and claims an *enhancement mode* GaN (Gallium Nitride) MISFET (Metal Insulator Semiconductor Field Effect Transistor) with a self-aligned ledge. GaN transistor devices may be categorized into two different categories: (1) depletion-mode FETs and (2) enhancement-mode FETs. *See* EX2005 ¶37 (citing the '347 patent specification); *see also* '335 Patent at 1:54-63. Depletion-mode FETs maintain an “ON” state at zero gate-source voltage (normally ON), while enhancement mode FETs maintain an “OFF” state at zero gate source voltage (normally OFF). EX2005 ¶35. Depletion-mode FETs deplete the 2DEG located near the junction of two layers having different band gaps. *Id.* In the depletion-mode FETs, an electron channel that exists at zero gate voltage is depleted by applying a negative gate voltage, thereby turning the FET OFF. *Id.* Conversely, enhancement-mode FETs have no electron channel at zero gate voltage, but an

electron channel can be induced by applying a positive gate voltage, thereby turning the FET ON. *Id.*

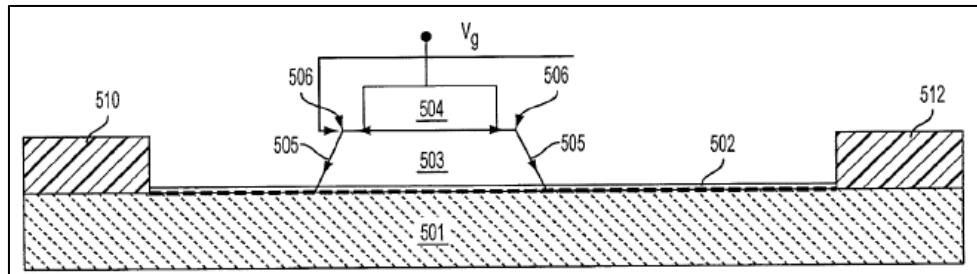
The '335 patent explains that a gate leakage current in GaN high electron mobility transistors occurs between the gate contact above gate material 101 and the 2DEG region 102 below and adjacent to the gate material along gate leakage current paths 201 (along the sidewalls of gate material 101) and 202 (through the bulk of gate material 101). *See* '335 patent FIG. 2 (reproduced below); 2:5-8. It was further identified that the gate leakage current of the prior art structure occurs predominantly along gate leakage current path 201, e.g., along the edge of the gate material. *See id.* at FIGs. 3A, 3B, and 4 (demonstrating that an increased number of gate p-type semiconductor sidewall edges increases the gate leakage current).



'335 Patent at Fig. 2

GaN FETs are known for their ability to carry greater current and withstand higher voltages than their silicon counterparts. EX2005 ¶28, 39. In particular, the '335 Patent, as shown below, innovatively teaches a gate structure with an elongated

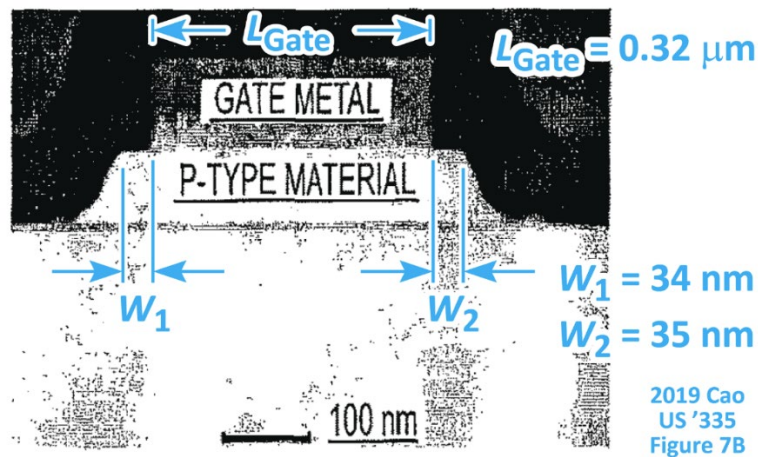
surface length that reduces the gate leakage from the device. *Id.* at ¶39. Due to the enhanced surface length of the elongated ledges and sidewalls of the device, there is a lower gate leakage during operation. *Id.* The gate leakage current can be reduced by lengthening the gate leakage current path at the edges of the gate p-type semiconductor material by including a pair of ledges that extend horizontally towards the source and drain contacts, as shown in Fig. 5 (reproduced below). *Id.* The '335 Patent describes the ledges as self-aligned. '335 Patent at 2:46-48.



'335 Patent at FIG. 5.

In FIG. 5 above, the gate p-type semiconductor material 503 is positioned below the gate metal 504 and above barrier layer 502. In some embodiments, the barrier layer is formed of AlGaN. *Id.* at 3:46-48. Gate p-type semiconductor material 503 includes ledges 506 on each side of gate metal 504. *Id.* at 3:49-54. The sidewalls of gate metal 504 define a width of the gate metal which is narrower than the width of the narrowest portion of gate p-type material 503. *Id.* at 3:59. The width of gate metal 504 being narrower than gate p-type material 503 effectively forms a pair of horizontal ledges 506 at the top of gate p-type material 503. *Id.* The

sidewalls, or edges, of the gate p-type material, which track reference number 505, extend respectively towards the source and drain material. *Id.* at 4:23-26; FIG. 5 In this embodiment, the narrowest portion of gate material 503 is at the top of the gate p-type material, from where the sidewalls of the gate p-type material descend towards the barrier layer, and the width of the gate p-type material increases. *Id.*; EX2005 ¶40.



'335 Patent, Fig. 7B (annotated)

III. CLAIM CONSTRUCTION

The preambles of claims 1 and 5 of the '335 patent recite "[a]n enhancement-mode GaN transistor, comprising..." The body of claims 1 and 5 recite "a p-type gate material formed above the barrier layer."

In an ITC proceeding on a related patent, Petitioner took the position that HEMT devices with a p-type gate material are enhancement mode. EX2008 at 936:17-937:2 ("If you design a device with p-type material as we've heard in this

litigation, it's enhancement-mode.”). Patent Owner agrees that this is generally true.

Accordingly, there is no dispute that claims 1 and 5 of the '335 patent cover “an enhancement-mode GaN transistor,” as explicitly recited in the preamble of both claims.

IV. REBUTTAL TO STATEMENT OF FACTS

Petitioner's alleged Statement of Material Facts (Pet. 18) is materially deficient and should be ignored. Petitioner failed to include any citations to the record supporting any of its alleged facts (*see* 37 C.F.R. § 42.22(c)), and therefore, the alleged facts should not be assumed into evidence, nor is it Patent Owner's responsibility to presuppose and rebut the unsupported allegations.

V. LEVEL OF ORDINARY SKILL IN THE ART

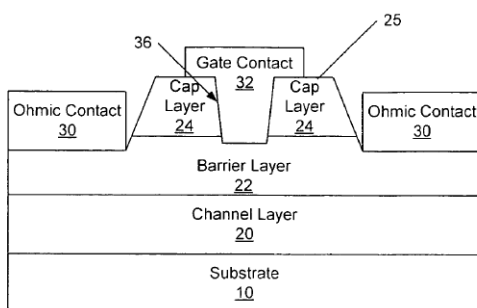
Based on the description in the '335 patent (and the '347 and '508 patents from which it claims priority) and the relevant art discussed during the prosecution history and cited on the patent, EPC submits that a person of ordinary skill in the art in the context of the '335 patent would have possessed at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN. EX2005 ¶20. Relevant graduate education could substitute for the professional work

experience. *Id.* Dr. Schubert opines, however, that the difference between Innoscience’s proposed POSA and EPC’s proposed POSA would not affect the outcome of this proceeding or change his opinion in any material manner. *Id.*

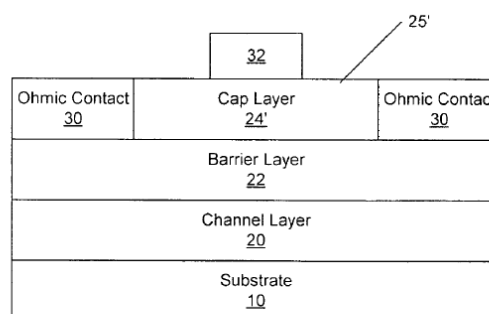
VI. OVERVIEW OF THE REFERENCES RELIED UPON BY PETITIONER

A. Saxler

Saxler describes two different high electron mobility transistors (HEMTs) – a recessed embodiment and a non-recessed embodiment. Both embodiments are depletion mode devices. EX2005 ¶54. The two embodiments are shown in Figures 1A and 1B (reproduced below).



EX1007, Fig. 1A



EX1007, Fig. 1B

As can be seen in Fig. 1A, the cap layer 24 of the recessed embodiment has two distinct regions on either side of the gate with slanted sidewalls. In Saxler’s non-recessed embodiment (Fig. 1B) the cap layer 24’ is a rectangle extending from ohmic contact 30 to ohmic contact 30. Saxler describes a number of structural and functional distinctions between the recessed embodiment and the non-recessed

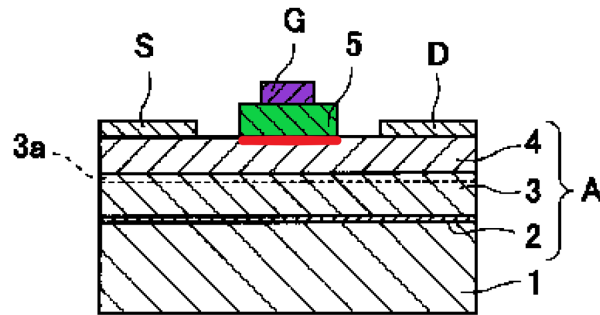
embodiment, including the shape, thickness, doping, and function of the cap layers. EX1007, Figs. 1A, 1B, 2A, 2B, ¶¶[0007], [0012], [0014], [0027], [0062], [0070], [0071], [0073], [0074], [0076], [0081]; EX2005 ¶55.

Saxler describes the general knowledge of a “gate-last” fabrication process in which the cap layer is layered and etched to form the source and drain contacts, followed by the gate contact being deposited. EX1007 ¶¶[0063]-[0066]; EX2005 ¶57 (illustrating the steps of Saxler’s process).

B. Yoshida

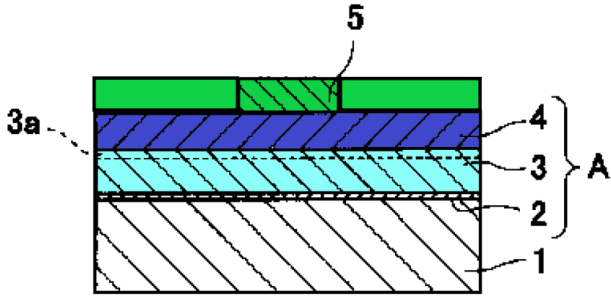
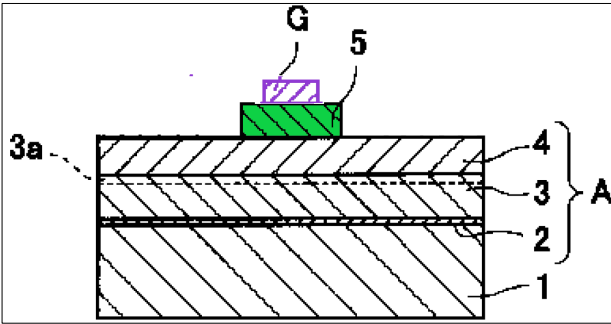
Yoshida discloses an enhancement-mode GaN HEMT having a semi-insulating substrate (1), a buffer (GaN) layer (2), an i-type semiconductor (GaN) layer (3), an n-type semiconductor (InGaN) layer (4), and a p-type GaN layer (5).

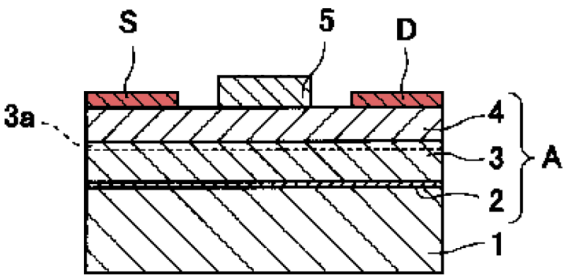
The layers are deposited to form a **pn junction** “immediately under the **gate electrode G**” to “enable[] voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility.” EX1006 ¶[0017].

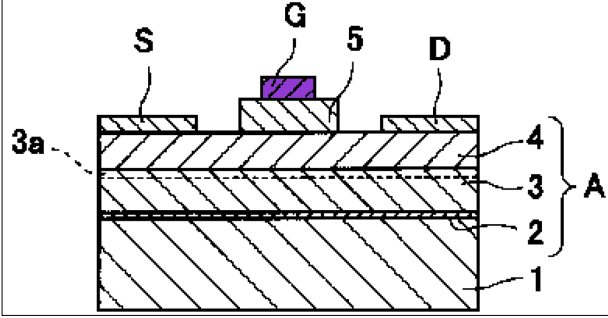


EX1007, Fig. 1 (annotated)

Like Saxler, Yoshida is formed by a “gate-last” process where the **p-type GaN layer 5** is deposited and etched to form the source and drain contacts S, D before **the gate electrode G** is deposited. EX2005 ¶13. More specifically Yoshida discloses “an etchant to etch away the **p-type GaN layer** except where the **gate electrode** was to be loaded.” EX1006 ¶[0022]. As Dr. Schubert explains (EX2005 ¶61), Yoshida’s process occurs in the following specific order:

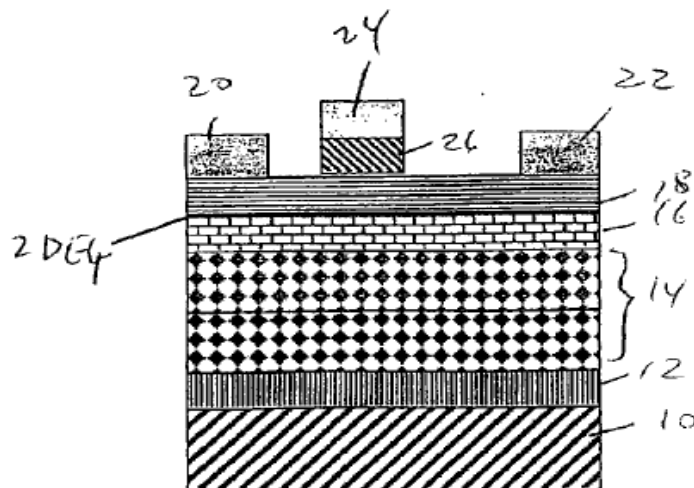
Step	Process
1	<p>A GaN buffer layer 2, an i-type GaN layer 3, an ntype AlGaIn layer 4, a p-type GaN layer 6 are deposited through epitaxial growth. EX1006 ¶¶[0019]-[0021].</p>  <p>EX1006, Fig. 1 (modified)</p>
2	<p>Dry etching was performed to etch away the p-type GaN layer “except where the gate electrode was to be loaded and exposing the n-type InGaIn layer 4”. EX1006 ¶[0022].</p>  <p>EX1006, Fig. 1 (modified)</p>

3	<p>An SiO₂ film is deposited to cover the entire surface, and after patterning with photoresist, the area including the part where the gate electrode was to be loaded was masked, leaving the portion where source and drain electrodes were to be loaded open.”</p> <p>EX1006 ¶[0022].</p>
4	<p>Al is deposited on the exposed ntype InGaN layer 4 to load source electrode S and drain electrode D. EX1006 ¶[0022].</p>  <p>EX1006, Fig. 1 (modified)</p>

5	<p>After etching away the masking and opening the SiO₂ film beneath it, the source electrode S and drain electrode G locations were masked with SiO₂ film, Au was deposited in the opening portions, and gate electrodes G were loaded above the p-type GaN layer 5. EX1006 ¶[0023].</p>  <p>EX1006, Fig. 1 (annotated)</p>
---	--

C. Beach

Beach describes a III-Nitride enhancement mode semiconductor device, including a gate barrier layer under the gate. EX1008, Abs., Title. Beach describes a transistor (as shown below) including substrate 10, bonding layer 12, first III-N buffer body 14, first III-N semiconductor body 16, second III-N semiconductor body 18, first and second power electrodes 20, 22, gate barrier 26, and gate arrangement 24. *Id.* ¶¶[0031]-[0032]; EX2005 ¶62.



EX1008, Fig. 1

Beach discloses that the gate structure of gate arrangement 24 and gate barrier 26 is patterned and etched to form a self-aligned gate arrangement. *Id.* Fig. 2F, ¶[0040]. Beach discloses that the gate structure is fabricated before the ohmic contacts 20, 22 are formed on the device (i.e., a gate-first process). *See, e.g., id.*; EX2005 ¶65.

D. Shenoy

Shenoy is an article exploring the theoretical shape evolution that occurs in through-mask electrochemical micromachining (EMM) through mathematical modeling. EX1009, Abstract. Shenoy is not directed to the formation of GaN based semiconductors and/or HEMTs. EX2005 ¶66. Shenoy further does not disclose nor suggest methods of manufacturing an enhancement-mode GaN transistor. *Id.* Shenoy further does not address self-aligned structures. *Id.*

Instead, Shenoy theoretically explores how deviations in photoresist mask wall angle affect the directionality of the subsequent etching process. EX2005 ¶67. Further, because Shenoy is based on a mathematical model, its disclosure relies upon theoretical assumptions that would not necessarily be applicable in practice, or true with respect to enhancement-mode GaN transistors and their applicable materials. *Id.* Particularly, Shenoy describes the shape of an ideal evolving EEM etching cavity but does not explicitly or implicitly instruct a POSA how to etch a GaN-based layer, any particular desired patterning designs, or methods or desires to achieve particular sidewall designs. *Id.* Instead, Shenoy is entirely ambivalent to any desired design. *Id.*

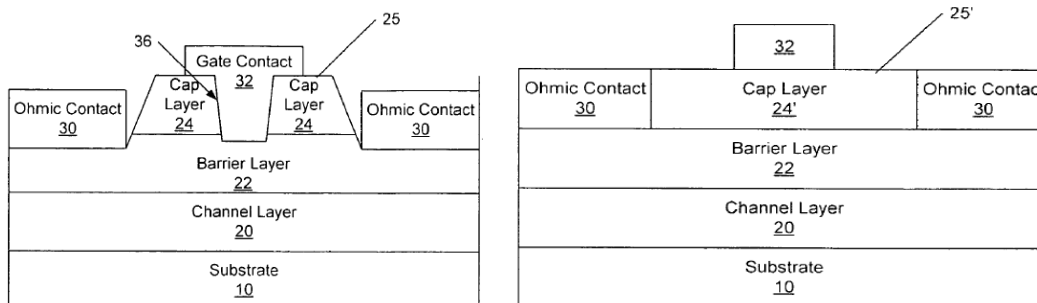
VII. GROUND 1 (CLAIMS 1-7) – SAXLER ALONE

A. A POSA would not consider the gate recess of Saxler as “optional” based on Saxler’s two distinct embodiments

Petitioner alleges that “although [Fig. 1A] depicts its gate recess may separate its cap layer into two portions in some embodiments, **the recess in Saxler’s cap layer 24 is optional**, and where not employed the cap is a continuous material. Shealy, [121].” Pet. 45. Patent Owner disagrees with this interpretation of Saxler.

Saxler discloses two distinct embodiments. A first recessed embodiment is illustrated in FIGS. 1A, 2B having a bifurcated recessed cap layer where the gate contact intersects and divides the cap layer. A second non-recessed embodiment is

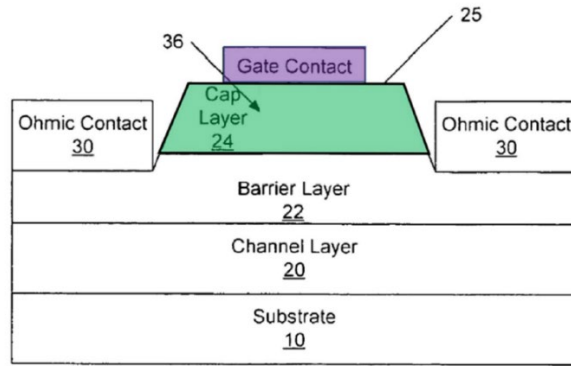
illustrated in FIGS. 1B, 2A with a non-recessed gate contact positioned on top of the cap layer. EX2005 ¶81.



EX1007, Fig. 1A

EX1007, Fig. 1B

In acknowledging that neither of Saxler’s embodiments meet the claim limitation, Petitioner proposes selectively modifying Saxler by removing the recess (36) in the cap layer (24) of Fig. 1A (the recessed embodiment) and copying and pasting the gate contact (32) from Fig. 1B (the non-recessed embodiment) on top of the modified cap layer (24). Pet. 26. Petitioner later refers to this “modified” rendition of Saxler as “where the gate is not utilized” (Pet. 26) or Saxler’s “non-recessed embodiment” (Pet. 30-32, 55, 56, 62). But the “modified” rendition is clearly not illustrated or supported by or suggested by Saxler. EX2005 ¶82.



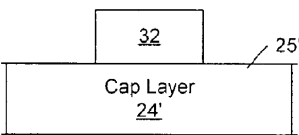
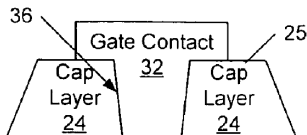
Pet. 41.

Prior art disclosure cannot be shown by “multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention.” *Microsoft Corporation v. Biscotti, Inc.*, 878 F.3d 1052, 1063 (Fed. Cir. 2017). Indeed, a reference “must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008).

Indeed, Petitioner’s cited passages of Saxler actually contradict Petitioner’s premise by highlighting the structural and functional distinction of the cap layer 24 in the recessed embodiment and the cap layer 24’ in the non-recessed embodiment. EX2005 ¶83.

For example, as relied on by Petitioner, ¶[0012] discloses “in particular embodiments of the present invention without a gate recess, the doped region extends into the cap layer from about 2.5 Å to about 50 Å” and “in particular embodiments of the present invention with a gate recess, the doped region extends

into the cap layer from about 20 Å to about 5000 Å.” EX1007 ¶[0012]. Petitioner alleges that, because the recessed embodiment and the non-recessed embodiment are described in the same paragraph, they are structurally equivalent except for the presence of the gate recess. EX2005 ¶84. However, ¶[0012] explicitly describes the embodiments as “particular embodiments of the present invention without a gate recess” and “particular embodiments of the present invention with a gate recess,” while distinguishing the depth of the doped regions between the non-recessed embodiment (about 2.5 Å to about 50 Å) and the recessed embodiment (20 Å to about 5000 Å). *Id.* Additional exemplary distinctions are summarized below.

Saxler Feature(s)	Non-Recessed Embodiment	Recessed Embodiment
Shape of cap layer and gate contact Fig. 1B, 1A, <i>see also</i> Fig. 2A, 2B		
Thickness of cap layer ¶[0027], <i>see also</i> ¶[0081]	“from about 2 Å to about 20 Å”	“from about 5 to about 5000 Å”
Level of doping of cap layer ¶[0071], <i>see also</i> ¶[0073]	“should be sufficiently high so as to reduce leakage current... and be the dominant ‘surface’ state but not so high as to [] introduce traps or leakage paths by becoming a conductive layer”	“a high level of p-type dopants may be provided such that the cap layer 34' may be provided as a conductive layer”

Dopant concentration of cap layer ¶[0012]	“from about 10^{18} to about 10^{21} cm^{-3} ”	“more heavily doped than 10^{21} cm^{-3} ”
Thickness of doped region ¶[0012], <i>see also</i> ¶[0014], [0070], [0071], [0073]	“into the cap layer from about 2.5 Å to about 50 Å”	“into the cap layer from about 20 Å to about 5000 Å”
Increased concentration of Al ¶[0007], <i>see also</i> ¶[0062]	“extends into the cap layer from about 2.5 Å to about 100 Å”	“extends into the cap layer from about 30 Å to about 1000 Å”

The cap layer of the recessed embodiment is thicker with a higher concentration of doping and a doping layer that extends further into the cap layer than the non-recessed embodiment. EX1007 Figs. 1A-B, ¶¶[0012], [0013], [0014], [0070], [0071], [0027], & [0081]; EX2005 ¶85. A POSA would understand that the non-recessed embodiment disclosed by Saxler is consistent with surface doping, and the maximum thickness of the doped region of the non-recessed embodiments is 250 times thinner than that of the recessed embodiments, with very limited overlap with respect to the range of the recessed embodiment. EX1007 ¶[0027]; EX2005 ¶87. Furthermore, the dopant concentration is further divergent between the two

embodiments. EX1007 ¶¶[0012], [0073]. Thus, Saxler does not provide any suggestion to POSA of the dopant concentration or the thickness of the dopant for Petitioner's hypothetical transistor. EX2005 ¶87. Simply put, Saxler provides absolutely no disclosure or suggestion of removing the recess from the recessed embodiment.

When asked about these structural and functional distinctions in Saxler, Dr. Shealy could not support his position that these passages disclose an "optional" gate recess. EX2004 at 38:12-19. ("It was pretty clear what was stated in those paragraphs").

Dr. Shealy further revealed that Petitioner's position, relies solely on paragraph [0052]. EX2004 at 38:12-25, 39:1-5. Dr. Shealy is of the opinion that paragraph [0052] of Saxler allows you to "take all the embodiments and bring in which ones you want, depending on what you're trying to accomplish." EX2004 at 39:3-5. This testimony reveals Petitioner's intention and hindsight -- Petitioner is trying to reengineer the recessed embodiment of Saxler to "accomplish" the claimed invention.

Petitioner's reliance on paragraph [0052] of Saxler as a substitute for motivation to modify (and its attendant expectation of success) is misplaced. Paragraph [0052] does NOT state that the disclosed embodiments of the recessed gate structure (FIGS. 1A, 2B) and non-recessed gate structure (FIGS. 1B, 2A) can

be freely modified to include or exclude a recessed gate. Rather, the paragraph only states that “**other** embodiments of the present invention may include or not include a gate recess.” EX2005 ¶97. Indeed, as noted above and as explained by Dr. Schubert, the features and parameters of the recessed and non-recessed embodiments are vastly different and, absent hindsight of claim 1, a POSA having read paragraph [0052] would have understood the “other embodiment” not having a gate recess to be the non-recessed structure depicted in Figure 1B. *Id.* ¶97-98. A POSA would not have understood it to mean the modified figure created by Petitioner because a POSA would have understood that additional process steps would be required to get from Figure 1B to the modified figure – none of which are provided by Petitioner. *Id.*

B. Petitioner’s proposed modification of Saxler does not produce a operable method for manufacturing an enhancement mode transistor

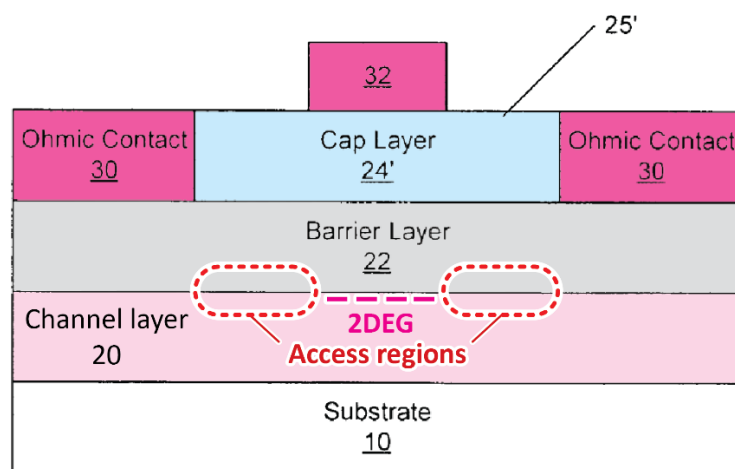
Saxler discloses depletion-mode transistors, not enhancement-mode transistors. EX2005 ¶114; EX1003 ¶[0055] (“Saxler does not use the phrase ‘enhancement-mode’”).

Indeed, Petitioner acknowledges that the recessed embodiment disclosed by Saxler is not enhancement-mode due to the recessed gate structure. Pet. 55-56; EX1003 ¶[0146] (“with the recess, Saxler’s device is not enhancement-mode (always off)”; EX2004 at 59:5-10 (“as it's drawn, it would be a depletion-mode

device”).

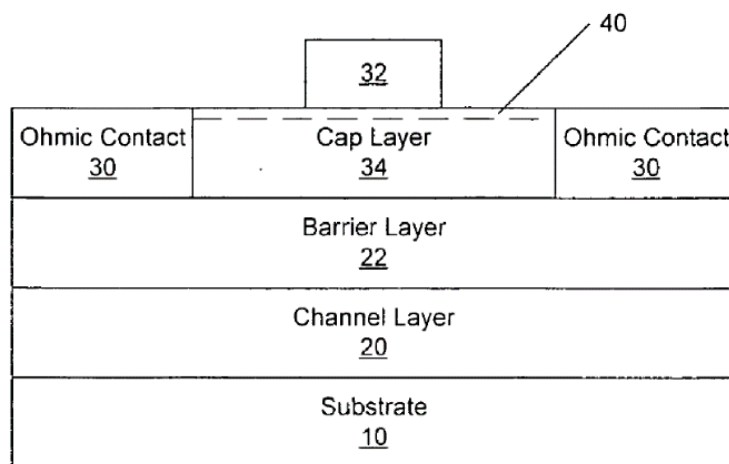
Petitioner concedes that the non-recessed transistor of FIG. 1B would not be a functional enhancement-mode transistor because the cap layer 24' extends from ohmic contact 30 to ohmic contact 30. EX2004 at 53:13-19 (“1B is a strange cartoon... I've never seen a device built that way, where the sides of the Ohmics are able to butt up against the cap layer -- you're not going to be able to fabricate that”); 65:16-18 (“that structure, as shown, would have these shunt problems I was talking about”). Dr. Shealy later contradicts himself, stating that it can be enhancement-mode. EX2004 at 66:19-68:11.

As acknowledged by Dr. Shealy, Saxler's cap layer 34 in Fig. 1B extends completely from Source to Drain, including the access regions that are located between the S&G (source and gate) electrodes, as well as between the G&D (gate & drain) electrodes. EX2005 ¶117.



When a voltage is applied to the gate electrode, a 2DEG is induced substantially below the gate electrode but, importantly, not under the entirety of the cap layer 24' of Saxler (that is, not all the way from Source to Drain). As a result, the transistor, if enhancement mode, could never be switched ON. *Id.* at 118.

Indeed, all of the embodiments disclosed in Saxler are depletion-mode transistors. For example, Saxler discloses with reference to Figure 2A, “the doped region 40 may be doped with p-type dopants so as to provide a p-n junction between the doped region and the cap layer 34 and the gate contact 32 is provided directly on the doped region 40 so as to provide a Junction HEMT (JHEMT).” EX1007 ¶[0072]. As acknowledged by Dr. Shealy, the disclosed JHEMT is depletion mode and not enhancement mode. EX2004 at 72:1-15.



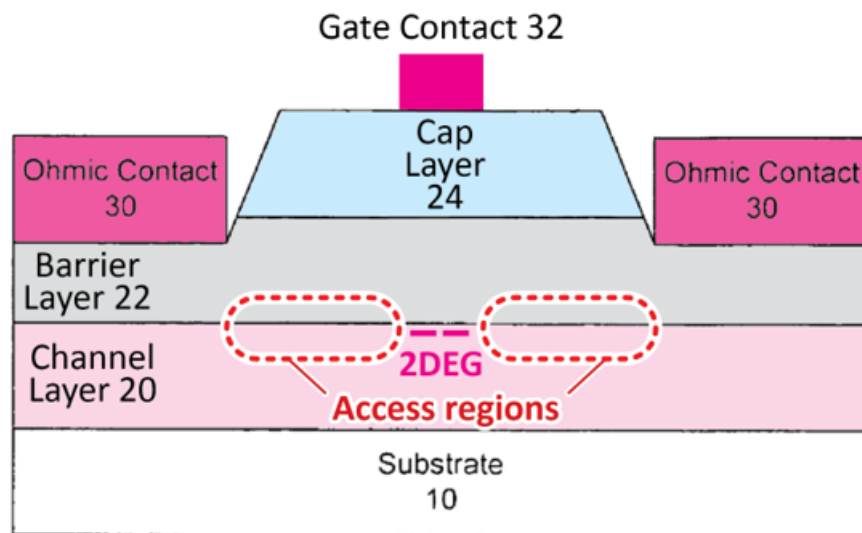
EX1007, Fig. 2A

Paragraph [0049] explains the purpose of p-type doping of region 40 at the top of the cap layer: “the dopants at the outer surface of the device may segregate to

dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations.” *Id.* ¶[0049] Indeed, Saxler points out that the dopants “segregate to dislocations,” rather than depleting the 2DEG. *Id.* Paragraph [0049] further explains that “a shallow dopant in the bulk crystal may have characteristics of a deep level when at a dislocation” which is “especially true in the case of p-type [...] dopants.” *Id.* Thus, the shallow acceptors of Saxler do not even act as acceptors once they “segregate to dislocations.” EX2005 ¶128. If the shallow dopants do not act as acceptors, the cap layer cannot function in enhancement mode. *Id.* That is, the dopants that Dr. Shealy envisions as regular, shallow p-type dopants, are in fact characteristics of “deep level” dopants. *Id.* This fact would be perceived as problematic and de-motivating by a POSA, because, contrary to Dr. Shealy’s assertions, “deep levels” are generally not suitable to deplete a 2DEG. *Id.* As a result, a POSA would be discouraged taking the path Dr. Shealy envisions.

Petitioner’s unsupported hypothetical transistor cannot be a functional enhancement-mode transistor based at least on the geometry of the cap layer, which, like FIG. 1B extends substantially from source to drain (and including the access regions). The geometry of the cap layer 24 prevents the transistor from working in enhancement-mode because the access regions would remain depleted of free electrons (and thus the access regions are electrically resistive), even for a positive gate voltage, thereby making it impossible to switch the transistor to its ON state.

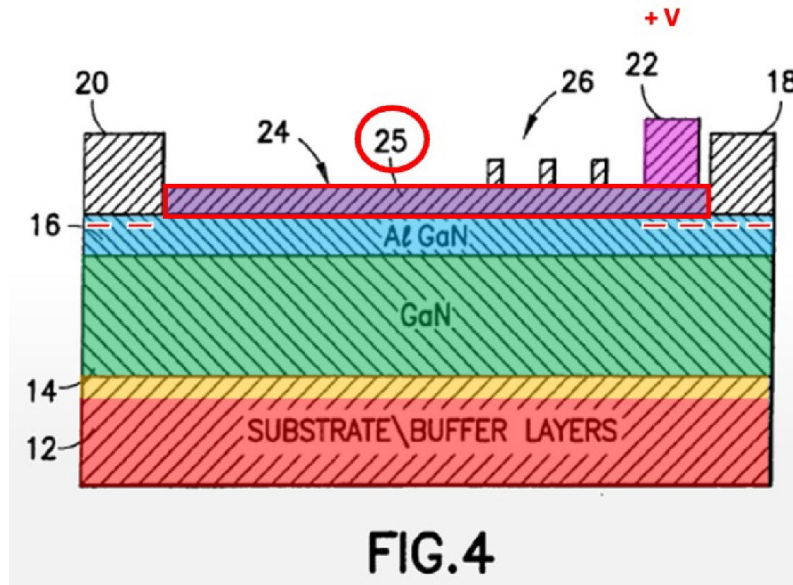
This fact is illustrated by the figure below. The 2DEG cannot extend across the access regions, and therefore cannot extend from ohmic contact 30 to ohmic contact 30. EX2005 ¶122.



EX2005 ¶

Petitioner confirmed this operation in a related ITC proceeding between the parties. There, for a transistor that has a GaN layer that extends from source to drain, Petitioner agreed that the 2DEG is not reconstituted between the source and the drain when a positive voltage—necessary for enhancement-mode operation—is applied to the gate. EX2008 at 938:1-10. When such a positive voltage (+v) is applied, as shown below, the 2DEG (represented as red dash “—”) is *only* reconstituted under the gate, which is insufficient to turn the device ON because the 2DEG is not continuous between the source and drain contacts. *Id.* Petitioner’s expert in the ITC proceeding, Dr. Lebby, admitted as much during his redirect examination at trial,

referring to the image below, noting that “...you can establish a 2DEG with a positive voltage on an enhancement-mode, and the question here is, is that the 2DEG doesn’t – **it’s not continuous all the way from the source to the drain...**” *Id.* at 938:5-10 (emphasis added); *see also*, EX2009 at 41-42.

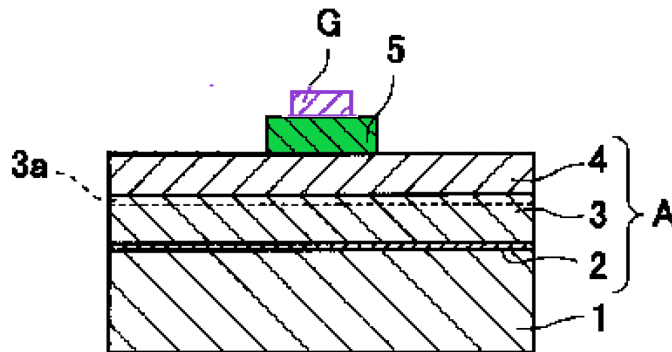


EX2009, 41

Even assuming that Dr. Shealy is correct in that it would be possible to apply a sufficiently high voltage to replenish the electrons in the access regions, a POSA would not produce an enhancement-mode circuit in this manner. EX2005 ¶124.

Conversely, cap layers in depletion mode transistors can extend substantially the entire length between the ohmic contacts because the transistor is normally ON and the cap layer only needs to pinch off the current by depleting the 2DEG under the gate to turn the transistor OFF. *Id.* ¶125. On the other hand, enhancement mode transistors are normally OFF, and the situation is reversed, and the 2DEG must be

replenished under the p-type gate material. *Id.* Dr. Shealy’s theory that a sufficiently high voltage could replenish electrons in the 2DEG from source to drain is not practical. As disclosed, for example, in Yoshida, enhancement mode transistors are designed to provide voltage control with a small amount of carrier injection. EX1006 ¶[0017]. This is produced in Yoshida by “etch[ing] away the p-type GaN layer except where the gate electrode was to be loaded and exposing the n-type InGaN layer 4.” EX1006 ¶[0022]. Thus, a POSA would understand that the gate material is designed in an enhancement-mode transistors such that only a small portion of the 2DEG needs to be replenished to turn it ON.



EX1005, Fig. 1

Moreover, Petitioner’s expert from the ITC proceeding, Dr. Lebby, admitted that he has no quantitative basis for his theory that a sufficiently high voltage could replenish electrons in the 2DEG; he conceded that he has neither modeled nor simulated any part of this theory. EX2008, 938:19-939:8. Dr. Lebby’s vague instructions to a POSA are to “play with” various aspects, with the admitted caveat

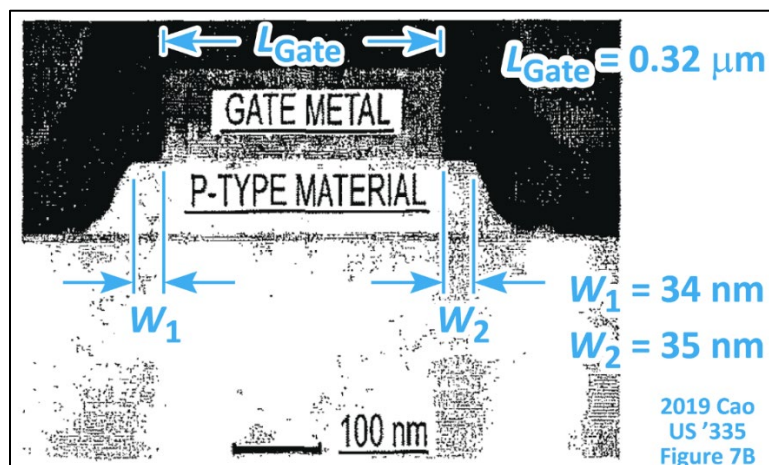
that even if such a device were to exist (and it does not), it would have “lots of leakage” due to the massive amount of voltage passing through the gate. *Id.* at 939:5-8. That is precisely why a POSA would not have been motivated to apply such a high voltage. EX2005 ¶127.

Thus, a POSA would have no reason to convert the depletion mode transistor of Saxler, having the cap layer 24 extending entire or substantially entirely between the ohmic contacts, to an enhancement mode transistor. The modification proposed by Petitioner, even if possible, would require excessive voltage to be applied to turn the transistor ON (assuming that it would even turn ON), undesirable for transistors. EX1006 ¶[0017].

C. Petitioner improperly relies upon Fig. 1A of Saxler as disclosing the pair of horizontal ledges “having substantially equal widths” recited in independent claim 1

Petitioner devotes a single sentence in the Petition with respect to a fundamental feature of the ‘335 patent, i.e., “a pair of horizontal ledges having substantially equal widths.” Pet. 51. With respect to this feature, Petitioner simply points to Fig. 1A of Saxler, asserting that “[t]hese ledges are symmetric on either side of the gate (i.e., having substantially equal widths.)” *Id.* But the “substantially equal width” ledges described in the ‘335 patent are **nanometer** widths and could not be depicted in patent drawings without an exploded view of the gate, annotated with dimensions. EX2005 ¶354.

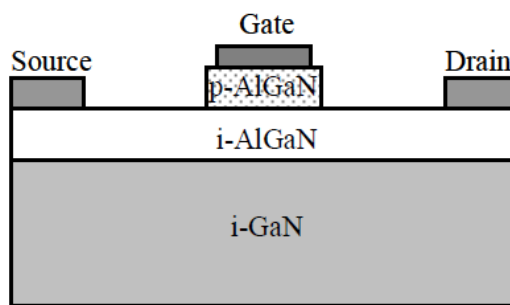
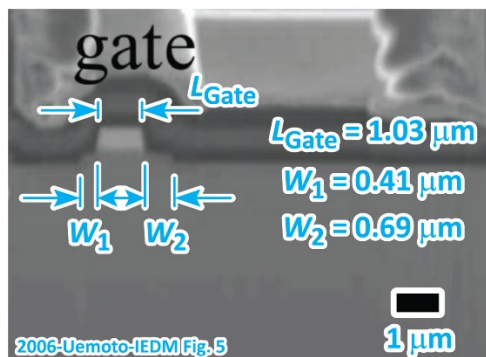
The self-aligned, single mask process of the '335 patent achieves horizontal ledges of “substantially equal widths”:



'335 Patent, Fig. 7B (annotated)

As shown above, the ledges of the '335 patent have “substantially equal widths” – i.e., they only differ in 1 nm, which is 1 billionth of a meter, an incredibly small dimension. They are not exactly equal, but they are certainly “substantially equal”, given the dimensions at issue.

In contrast, the ledges of the Uemoto, shown below left, differ substantially, with the $0.69 \mu m$ width of the ledge on the right, W_2 , being 68% larger than the $0.41 \mu m$ width of the ledge on the left. EX1020, Fig. 5 (annotated). In reality, the horizontal ledges of Uemoto, made with a two-mask process, as opposed to a self-aligned, single mask process, clearly do NOT have ledges of “substantially equal width”, yet the patent drawing of Uemoto, which Petitioner relies upon, shows ledges that are substantially equal in width:



EX1020, Fig. 5 (annotated)

EX1020, Fig. 1

The patent drawing in Saxler, Fig. 1A, like Fig. 1 of Uemoto above, appears on its face to disclose equal width ledges, but does not disclose “a pair of ledges having substantially equal widths” within the meaning of the ‘335 patent. This is not surprising, since the “substantially equal width” ledges of the ‘335 patent include nanometer ledge-width differences that could not be depicted in Fig. 1A of Saxler or Fig. 1 of Uemoto. EX2005 ¶354.

D. Petitioner’s attempt to avoid the holding in *Hockerson* should be rejected

In *Hockerson*, the Federal Circuit held that “patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” *Hockerson-Halberstadt, Inc. v. Avia Group, Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000). It is further established that “arguments based on measurements of a drawing are of little value” if there is no written description in the specification of quantitative values or no indication that the drawings are to scale. *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977); *Go Med.*

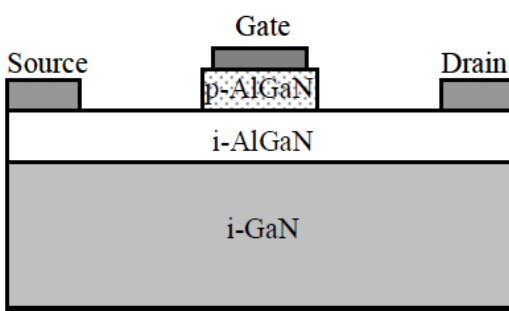
Indus. Pty, Ltd. v. Inmed Corp., 471 F.3d 1264, 1271 (Fed. Cir. 2006).

Petitioner attempts to apply an exception to the general rule of *Hockerson* with its selective citation to *Ex parte Bjorn*, No. 2018-001567, 2019 WL 6173305 (P.T.A.B. Oct. 16, 2019). Pet. Prelim. Reply 2. However, a careful reading of *Ex parte Bjorn* undermines Petitioner’s argument.

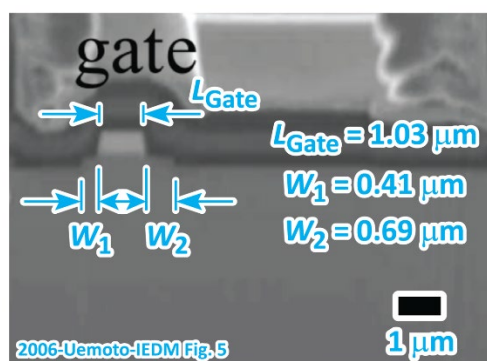
In *Ex parte Bjorn*, the Board first addressed the limitation “less than or substantially equal” of independent claim 1 that was directed to a bone implant. *Id.* at *10 (emphasis added). The Board found that “claim 1 merely requires the abutment to have an exterior surface diameter that is ‘less than or substantially equal to the maximum thread diameter of the male screw section of the bone fixture.’ No particular dimensions or proportions are claimed.” *Id.* The limitation of “less than or substantially equal” was thus found to be open-ended. *Id.* (emphasis added).

In addressing another claim in the same patent, however, the Board found that a rejection based on drawings not disclosed as being to scale or having any particular dimension cannot be relied on for meeting the claim term “*substantially equal.*” *Id.* at 17. The Board reasoned that “even if we determine what percentage or ratio of an oversized abutment diameter is permitted within the scope of the claim, *the drawings cannot be relied on to disclose such precise or relative proportions*”; thus, the Board followed *Hockerson*’s general rule when analyzing the phrase “substantially equal.” *Id.* (emphasis added).

Hockerson's general rule makes sense. The Board need not look any further than *Uemoto*, which is relied on by Petitioner, and discussed above. The schematic figures of *Uemoto* appear to show substantially equal widths. See EX1020, Fig. 1 (reproduced below). The actual device, however, varies significantly from the simple patent drawing as shown in Figure 5 of the *Uemoto*, reproduced below for comparison.



EX1020, Fig. 1



Pet. 92 (EX1020, Fig. 5 annotated)

When asked whether the actual ledges were substantially equal, Dr. Shealy responded “no.” EX2004 at 94:14-22. Indeed, any proposition that *Uemoto* discloses a gate structure having substantially equal ledges based on the schematic of Fig. 1 would be of “little value.” *Hockerson*, 222 F.3d at 956 (citing *In re Wright* 569 F.2d at 1127). The same deficiency is present in Petitioner’s invalidity position based on *Saxler* in relying on Fig. 1A.

Petitioner’s other cases are inapposite. For example, Petitioner cites *Presidio Components*” (IPR2015-01330, Paper No. 11 at 11 (P.T.A.B. Dec. 3, 2015), that

addresses “co-extensive length and width dimensions, top and bottom surfaces, and two ends, wherein the ‘first and second dielectric layers combine to enclose the first electrode layer and to describe a margin outward of the first electrode layer end.’” Pet. Prelim. Reply 2-4. The term “co-extensive” that defines a margin is not relevant to the term “*substantially equal*”, as held in *Hockerson*. The Court in *Presidio Components* also goes into a detailed discussion of the specification in providing evidence that the features are supported by the drawings, which Petitioner fails to do. Indeed, Petitioner has failed to provide any reasoning in how *Presidio Components* is relevant to Petitioner’s argument and Petitioner fails to address any nexus.

Petitioner next cites *Mueller Sports Med., Inc. v. Sportstar Athletics, Inc.*, 385 F. Supp. 2d 775, 777 (W.D. Wisc. 2005) that addresses written description support of an under-eye device that “*substantially cover[s]*” the cheekbone. Pet. Prelim. Reply 3. This limitation is clearly directed to a spatial relationship. Although the term “*substantially*” is used in *Mueller Sports Medicine*, “*cover[ed]*” is clearly a spatial relationship between two objects akin to “above”, “below”, or “outside” which are readily relied on for support in patent drawings. Petitioner fails to address how the spatial relationship of “*cover[ed]*” relates to two dimensions being “*equal*.”

Petitioner further cites *Drop Stop*, which addressed “generally oval” and “aligned longitudinally” and Qualcomm that addressed “substantially oblong.” Pet.

Prelim. Reply 4. The terms “generally oval” and “substantially oblong” are shapes and “aligned longitudinally” is an orientation of two object, clearly none of which are “precise proportions” or “particularly sizes” as held in *Hockerson*. Furthermore, Petitioner fails to address how these shapes or orientation limitations are relevant to two dimensions being “substantially equal.”

Indeed, in the cases cited by Petitioner, the court analyzed the technology of the patent and to what extent the patent drawings actually represent the actual device. For example, in *Ex parte Bjorn*, the court provides substantial discussion on how a screw of the patent in question must have certain dimensions to be screwed into a fixture in addressing “*less than or substantially equal*” from independent claim 1. *Ex parte Bjorn*, No. 2018-001567, 2019 WL 6173305 at *10-11. Petitioner fails to provide an analysis of case law that would require the Board to make an exception to the general rule set forth by *Hockerson*.

To the contrary, as repeatedly stated by Petitioner, Dr. Shealy, and Saxler, it is well known (a “principle”) that transistor schematics as relied on by Petitioner are not representative of an actual transistor with geometrical dimensions (and their ratios) drawn to scale. Pet. 75-76; EX1007 ¶[0042].

1. Saxler explicitly discloses that drawings are “schematics” and “their shapes are not intended to illustrate the precise shape of a region of a device”

Petitioner’s reliance on the *Saxler*’s figures is further frustrated by *Saxler*’s

own description of its figures as “schematics” throughout the disclosure. EX1007 ¶¶[0031]-[0036], [0042], [0052]. Indeed, Saxler specifically discloses that “the regions illustrated in the figures are schematic in nature and **their shapes are not intended to illustrate the precise shape of a region of a device.**” EX1007 ¶[0042] (emphasis added). Therefore, the disclosure of Saxler explicitly belies Petitioner’s assertion relating to the preciseness of the figures. Petitioner selectively and inconsistently relies upon Saxler’s teachings regarding the preciseness of shapes.

Petitioner relies on a statement in the same paragraph of Saxler ([0042]) to support its assertion that, due to manufacturing tolerances, lines illustrated to be vertical are typically in fact not vertical. Ex. 1007 ¶[0042] (“an etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features.”). In other words, according to Petitioner, while the patent drawings should be relied on to show ledges of “substantially equal widths” ledges, the drawings should *not* be relied on to show vertical sidewalls.

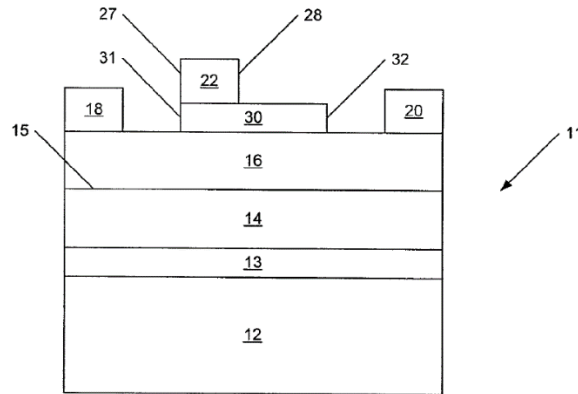
Furthermore, at his deposition, Dr. Shealy specifically stated that “the vertical scale of these diagrams is exaggerated, so you could see details of the epitaxial layer.” EX2001, 56:26-57:1. That is consistent with both Figs. 1A and 1B which show that the ohmic contacts 30 have the same thickness as the cap layer 34 (Fig. 1B), which, according to Dr. Shealy, “would rarely be the case.” EX2004 at 60:17-18. With further reference to Fig. 1B, Dr. Shealy states that “you’re not going to be

able to fabricate that... some sort of crude design. But there's no way to place Ohmic contacts and butt them up against that cap layer with no gap in between, as shown." EX2004 at 53:20-25. Dr. Shealy characterizes Fig. 1B of Saxler "a strange cartoon." EX2004 at 53:13.

Thus, on the one hand, Dr. Shealy and Petitioner substantially discredit the schematics of Saxler as being inaccurate. On the other hand, Petitioner bases its invalidity position on the unreasonable premise that the only aspects in Saxler's schematics that can be relied on are the precise dimensions of the ledges and the sidewalls shown in Fig. 1A. Petitioner cannot have it both ways.

2. Saxler explicitly discloses that the gate electrode is to be "offset"

The only disclosure in Saxler of the relative position of the gate contact recess 36 is that "the recess may be offset between the source and drain contacts such that the recess, and subsequently the gate electrode 32, is closer to the source contact than the drain contact." EX1007 ¶[0065]. This offset positioning is further consistent with Smith, as expressly incorporated by reference. EX1007 ¶[0042]. Smith explicitly discloses that the gate electrode is intentionally aligned or substantially aligned with the source-side of the source-side segment of the GaN cap segment 30, and if not "may be detrimental to the device." EX1015 ¶¶[0041]-[0042].



EX1015, Fig. 3

Thus, while *Saxler* provides no disclosure of the gate electrode being directly aligned with a central axis of the cap layer, it does disclose that, although not shown in the drawings, the gate electrode is intentionally “offset... closer to the source contact than the drain contact.” EX1007 ¶[0065]. This intentional “offset” belies Petitioner’s assertion that the Saxler’s device has “substantially equal ledges.”

E. Petitioner fails to show that the “self-aligned” ledges of claims 2 and 5 are obvious

Petitioner argues that claims 2 and 5, which recite that the horizontal ledges of the gate material are “self-aligned”, recite product-by-process steps, which lend no patentable weight. Pet. 24.

As the Board noted in the Institution Decision, p. 17, the law on product-by-process claims is well-established: “In determining validity of a product-by-process claim, the focus is on the product and not the process of making it.” *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1369 (Fed. Cir. 2009).

In the present case, the structural features imparted by the self-aligned process

allows ledges to be created that are “substantially symmetric” with respect to the gate metal disposed on the p-type material. ‘335 Patent at 3:65-4:3.

Importantly, contrary to the statement in the Institution Decision at 18, the ‘335 patent does **not** indicate that at least one other method can produce transistors that are “substantially symmetric” within the meaning of the ‘335 patent. The process for forming gate ledges using separate masks instead of the self-aligned process disclosed in the ‘335 patent cannot produce ledges that are “substantially symmetric” because of the misalignment that naturally results from a two-mask process. EX2005 ¶50.

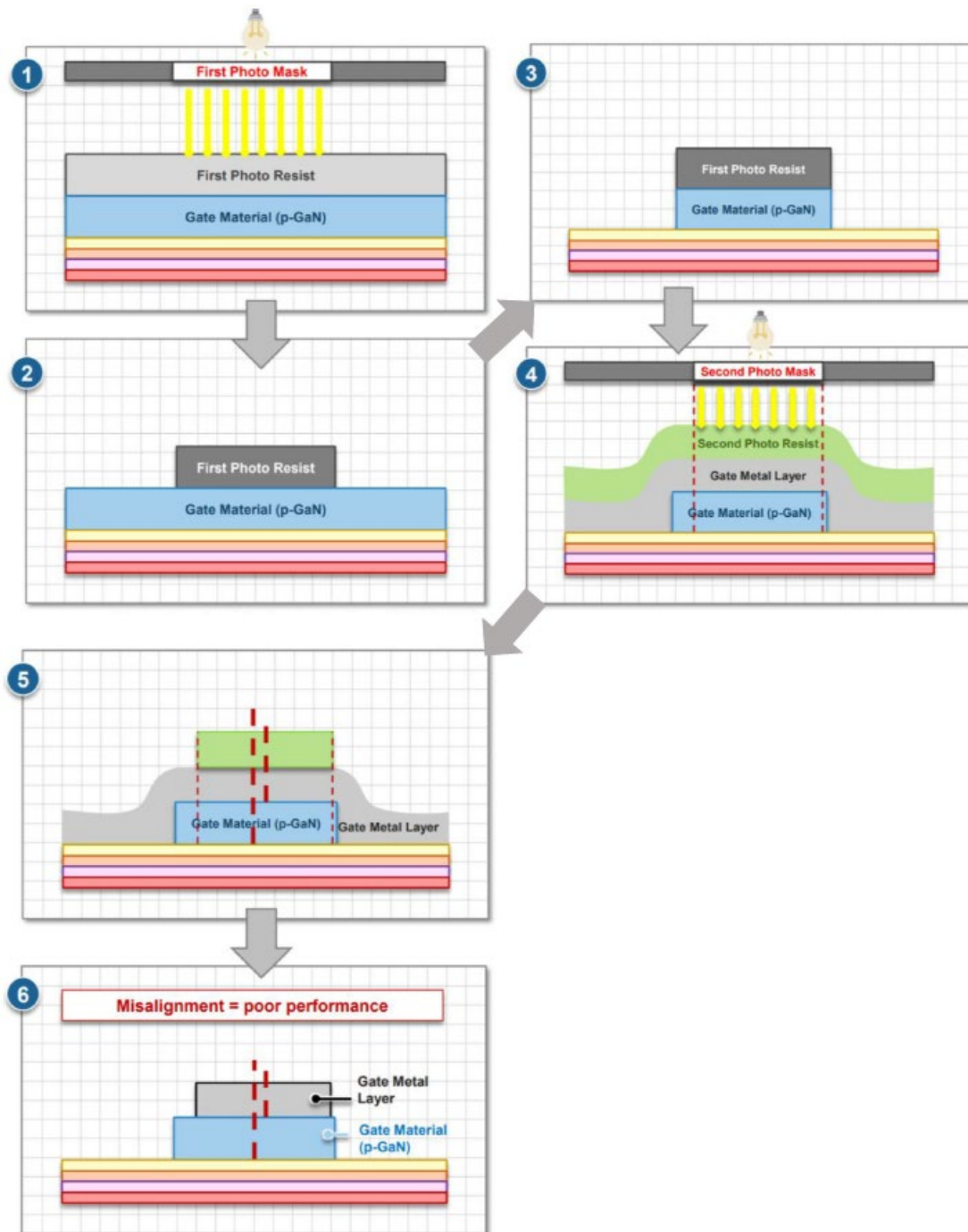
More specifically, in a self-aligned process, such described in the ’335 patent, a single photo mask is used to pattern and etch more than one feature, thereby resulting in a self-aligned structure in which two features (in the ‘335 patent, the gate metal and the underlying gate material) are automatically aligned with one another. EX2005 ¶49. The self-aligned structure is achieved because the single photo-mask pattern is used to pattern the photoresist which is then used to pattern (by etching) the first layer as the etching process proceeds downward from the top of the wafer towards the substrate. *Id.* After the first layer has been etched, the photoresist can either remain or be removed because the first etched layer has now been etched to accord with the pattern transferred from the photo mask. *Id.* Then, the second layer/feature is etched with either the photoresist and/or the top layer/feature serving

to protect the portion of the second layer/feature from being etched. *Id.* Through these steps, the top layer/feature and the second layer/feature share the same pattern from the photo mask and are automatically aligned (“self-aligned”) with each other. *Id.* For example, with respect to the ’335 patent, the patent teaches using a single photo mask to pattern and etch both the gate metal and the gate semiconductor material. ’335 Patent at 4:14-34.

Self-aligned processes provide multiple benefits to the transistor due to the lack of overlay errors. EX2005 ¶50. Due to such a process, the minimal critical dimension (CD), e.g., the smallest dimension possible, as limited by photolithography, can be achieved for the gate contact. *Id.* Without such a process, the gate semiconductor material (or other layers) below the gate metal had to be wider than the gate metal to accommodate for expected misalignment that occurs when more than one photo mask is used. *Id.* For example, because a feature must first be etched using a first photo mask, and then a subsequent photo mask would need to be aligned to that etched first feature to pattern and etch the second feature. *Id.* Such second alignment generally results in misalignment thereby requiring a wider gate semiconductor material than is desired or necessary to accommodate the two sequentially fabricated patterns. *Id.* In short, naturally there is some alignment error when using two photo masks, thereby causing overlay deviations (overlay deviations and overlay errors are used synonymously). *Id.*

The above misalignment issue is solved by the '335 patent, which uses one photo mask to pattern multiple features and avoid misalignment, thereby only requiring the gate semiconductor material to be as wide as the desired width of the gate metal, because the gate metal can be above the same width gate semiconductor material post etching. EX2005 ¶50.

The following graphical representations illustrate the differences between a self-aligning process/self-aligned structure versus a two photo-mask process, which cannot result in ledges having “substantially equal widths” because of inevitable misalignment. An example of a form of misalignment is shown on the right due to the double photo-mask process. As can be seen below in renditions from Dr. Schubert (EX2005 ¶50), the two-photo-mask process results in the centers of the two features, specifically, the gate metal and gate semiconductor material, being out of alignment.

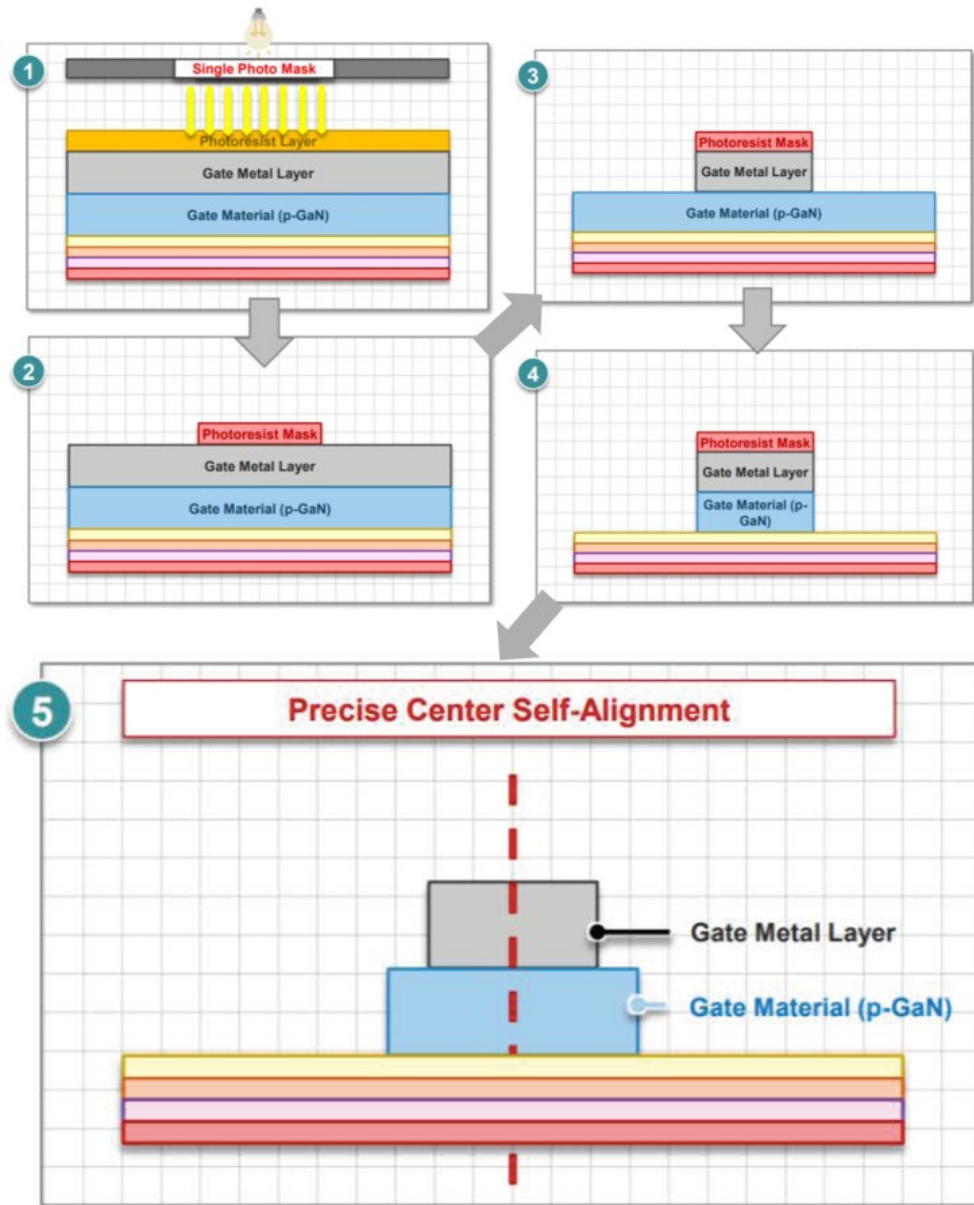


EX2005 ¶50

In contrast, the '335 patent describes a single photo-mask process that achieves a self-aligned gate structure. **Importantly, this process advantageously results in a self-aligned gate structure with ledges of “substantially equal**

widths”, which is otherwise not achievable. EX2005 ¶51.

A graphic representation of an embodiment of the process resulting in a self-aligned gate structure disclosed in the '335 patent is shown below:



EX2005 ¶51

With respect to the above figure, step 1 illustrates: the post-epitaxial structure that includes transition layers under a gate semiconductor material, a gate metal, and

a photoresist layer, the application and exposure of the photoresist layer using a single photo mask to pattern the photoresist layer in a photolithography process (step 1), completion of the photolithography process of the photoresist (step 2), an etching step resulting in an etched gate metal using the patterned photoresist (step 3), an etching step resulting in an etched gate semiconductor material (step 4) self-aligned with the gate metal, and an etch step resulting in a shaped gate metal and removal of the photoresist layer (step 5). EX2005 ¶52.

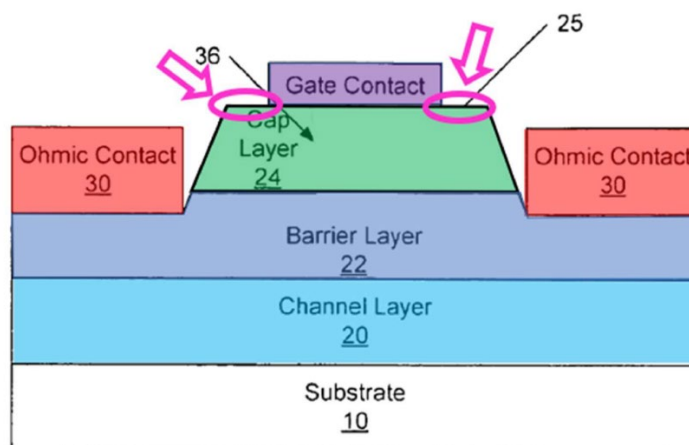
Saxler does not disclose a self-aligned process, so it is clear that Saxler does not disclose “self-aligned” ledges. This is acknowledged by Dr. Shealy. EX2004 at 55:1-7 (“we bring in the self-aligned with other references: Beach and Ahn”). But neither Beach nor Ahn is cited with respect to the “self-aligned” ledges in Ground 1.

VIII. GROUND 2 (CLAIMS 1-7) – SAXLER IN VIEW OF YOSHIDA

A. Saxler in view of Yoshida does not disclose “substantially equal ledges”

Petitioner alleges “Saxler in view of Yoshida also renders obvious [1f] (Ground 2). Shealy, [134]. Saxler-Yoshida’s gate contact is narrower than its cap layer, thereby exposing horizontal ledges that extend past the respective sidewalls of the gate and toward the source and drain. Yoshida, [0022]-[0023], Fig. 1; Saxler, [0046], Figs. 1A-1F; Shealy, [134]. These ledges are symmetric on either side of

the gate (i.e., having substantially equal widths). Shealy, [134].” Pet. 50-51.



Pet. 51

Yoshida has a similar depiction of horizontal ledges as Saxler. Petitioner relies on the same hypothetical structure and reasoning from Ground 1. Pet. 28. Thus, Ground 2 fails for the same reasons as Ground 1. §VII.C-D.

B. Saxler in view of Yoshida does not disclose “self-aligned” ledges

Petitioner jointly addresses claim 2 and element [5f] for Grounds 1 and 2. Pet. 51, 54. Ground 2 fails with respect to claim 2 and element [5f] for at least the reasons provided in §VII.E.

C. A POSA would not modify the recessed embodiment of Saxler by removing the recess based on Yoshida

Petitioner asserts that, like Saxler, “Yoshida also discloses and depicts a very similar device with a p-type gate material without a gate recess.” Pet. 24-25. Petitioner therefore reasons that Yoshida provides the motivation to remove the recess of Saxler Fig. 1A. *Id.* Fig. 1A of Saxler and Yoshida are not “the same layers performing the same functions.” Dr. Shealy concedes that the recessed embodiment

of Saxler is not functionally equivalent to the enhancement-mode transistor of Yoshida (“with the recess, Saxler’s device is not enhancement-mode (always off).” EX1003 ¶[0103]. Indeed, the cap layer of Saxler extends entirely or substantially the entire length between ohmic contacts, consistent with depletion-mode and not enhancement-mode (§§VI.A, VII.B), while Yoshida discloses an enhancement-mode transistor (§VI.B). There are a number of additional divergent parameters provided to the recessed embodiment of Saxler, for example as discussed in §VII.A. Thus, at least according to Dr. Shealy, Saxler and Yoshida would not have “the same layers performing the same functions” as alleged by Petitioner.

1. A POSA would not modify Saxler by changing its principle of operation

As acknowledged by Dr. Shealy, the recessed embodiment of Saxler is a depletion-mode transistor. EX1003 ¶103; EX2004, 59:5-10. As discussed herein, depletion-mode transistors have completely different structure, function, and applications from enhancement-mode transistors. EX2005 ¶¶35, 185.

The proposed modification or combination of the prior art cannot change the principle operation of the primary reference. MPEP § 2143.01; *In re Ratti*, 270 F.2d 810, 813, 123 USPQ 349, 352 (CCPA 1959).

Petitioner’s assertion that Yoshida provides the motivation to “remove the gate recess to turn Saxler’s device into an enhancement-mode device” (Pet. 55-56)

fails because it would be non-obvious and improper to change the principle operation of Saxler (from depletion mode to enhancement mode). EX2005 ¶¶35, 185.

2. A POSA would not modify Saxler in view of Yoshida for the very same reason that Saxler distinguishes from its recessed embodiment and non-recessed embodiment

Petitioner's assertions are also inconsistent with the disclosure of Saxler. As further discussed in §IV.A, Saxler describes a number of distinguishing structural and functional aspects, including the cap layer being thicker, with a higher concentration of doping, and a doping layer that extends further into the cap layer in the recessed embodiment compared to the non-recessed embodiment. EX1017, Figs. 1A, B, 2A, 2B, and ¶¶7, 12, 14, 27, 62, 70, 71, 73, 74, 76, 81. Thus, Saxler would not remove the recess from the recessed embodiment in view of Yoshida for the very same reasons that Saxler does not disclose a non-recessed embodiment with the parameters of the recessed embodiment. Saxler's embodiments are distinct without any reason to "mix and match", and Yoshida does not rectify this deficiency in Petitioner's argument.

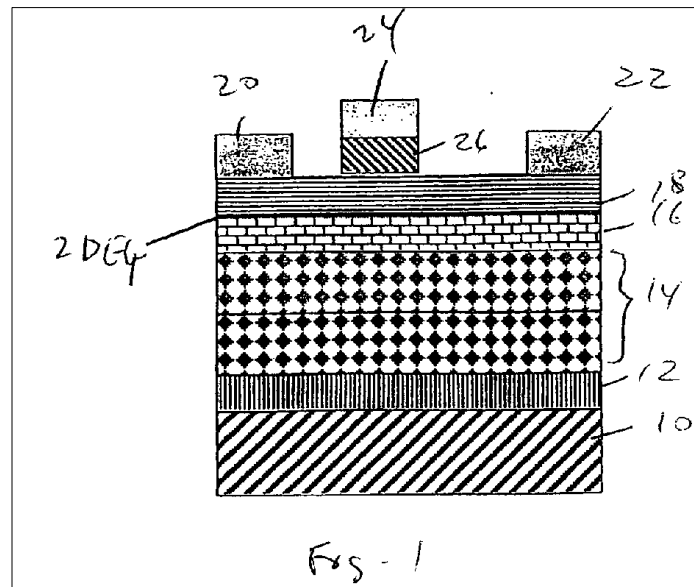
D. Petitioner's modification of Saxler in view of Yoshida does not produce an enhancement mode transistor

Petitioner jointly addresses element [1p] for Grounds 1 and 2. Pet. 35-36. Thus, Petitioner's argument with respect to element [1p] fails for the reasons provided in §VII.B.

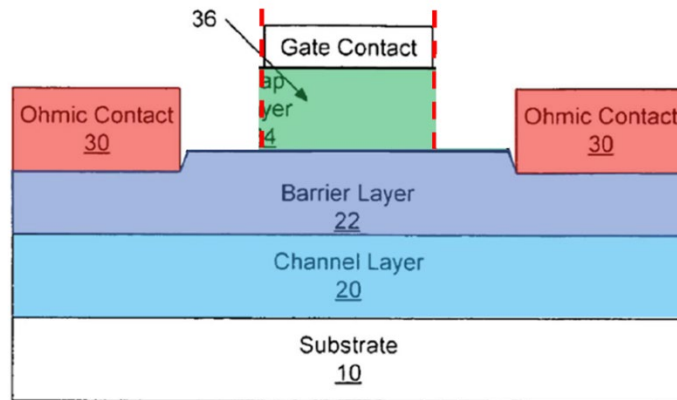
IX. GROUND 3 (CLAIMS 2 AND 5-7) – SAXLER IN VIEW OF YOSHIDA, BEACH, AND SHENOY

In Ground 3, Petitioner cites the same structure as Ground 2, again relying heavily on the schematics. Ground 3 fails for the same reasons discussed above, and for the additional reasons discussed below.

As Dr. Shealy acknowledged in his deposition, applying Beach's self-aligned technique would either cut off or not form the horizontally extending side surfaces that Petitioner relies on from Fig. 1A of Saxler and in the hypothetical transistor, as illustrated below. EX2005 ¶145. Dr. Schubert agrees that the sidewalls would be cut off, as shown below. EX2005 ¶¶145, 207.



Beach Fig. 1



Beach applied to Saxler modified Fig. 1A

Indeed, Dr. Shealy explained “what Beach figure shows is a -- you know, it's drawn as a vertical wall. It's an idealized drawing, of course. Well, one would expect it to have some curvature.” EX2004 at 87:15-19. Dr. Shealy’s testimony is directly undercuts Petitioner’s assertion that “Saxler discloses such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure.” Pet. 35. Applying the Beach self-aligned technique to Saxler would not produce the sloped sidewalls as illustrated in Saxler, but would rather produce intentionally vertical sidewalls with, according to Dr. Shealy, potentially “some curvature.” EX2005 ¶146.

Moreover, importantly, although not shown in Petitioner’s representation (Pet. 45), applying the Beach self-aligned technique to Saxler would also cut off the Saxler’s ledges, as shown in the above schematic. EX2005 ¶¶145, 207.

A. The etching in Beach is incompatible with Saxler

Furthermore, the etching technique of Beach is incompatible with those of Saxler. Beach discloses N-polar (nitrogen-polar) technology (¶10), while Saxler discloses Ga-polar (gallium-polar) technology. The two polarities cannot be combined, mixed, or synthesized, because they are mutually exclusive opposites. Due to the N-polar orientation of Beach, a POSA would not have used Beach as guidance to modify the teachings of Saxler. Further, the devices described in each reference are substantially different, and the teachings of Beach would not have been incorporated by a POSA into the structure and method of manufacture described in Saxler. EX2005 ¶156.

B. The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges based on Petitioner's reasoning

Petitioner alleges that “it would have been obvious to combine Saxler with Beach and Shenoy’s techniques of masking and etching the gate metal and p-type gate material using a single photomask when making Saxler’s non-recessed GaN HEMT device. Pet. 43-44.

Shenoy involves electrochemical etching – etching with an applied voltage, an applied electric field, and an electrical current flowing. EX2005 ¶158. However, because the method of Shenoy is performed under very controlled conditions, a POSA would not have considered Shenoy to modify the teachings of Saxler as

modified by Beach. *Id.* Indeed, electrochemical etching can only be used in conjunction with conductive materials and insulator materials. *Id.*

More specifically, the process of Shenoy in forming the undercut U on the metal film is explicitly dependent on the positioning of the metal film on an underlying insulator and in isolation of other components that could be etched. EX2005 ¶159. As further discussed in the “Model Development”, Shenoy discloses “the metal film thickness ratio determines **the extent to which EMM must proceed before the underlying insulator is exposed... Once the insulator is exposed, metal dissolution continues in the lateral direction leading to a change in metal wall angle, γ .**” EX1009 at 1; EX2005 ¶160.

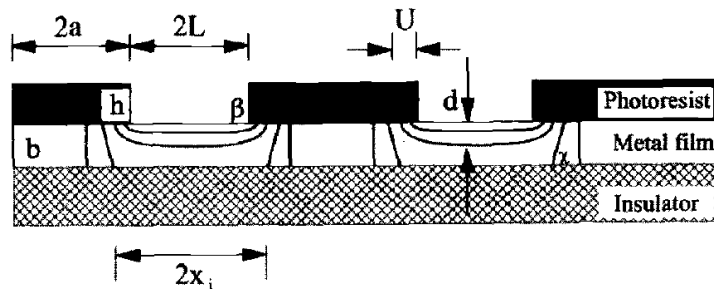
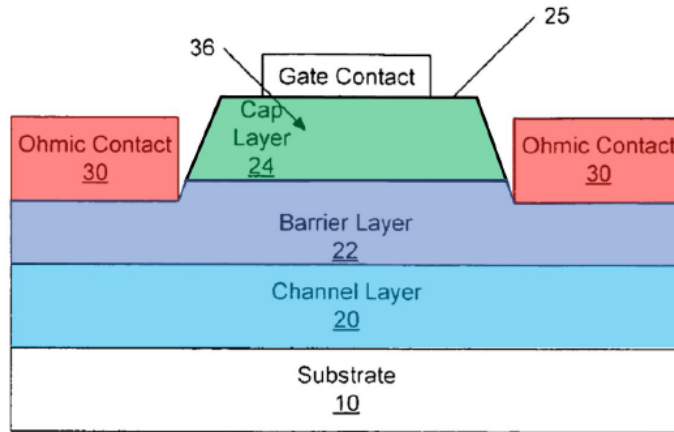


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

EX1009, Fig. 1

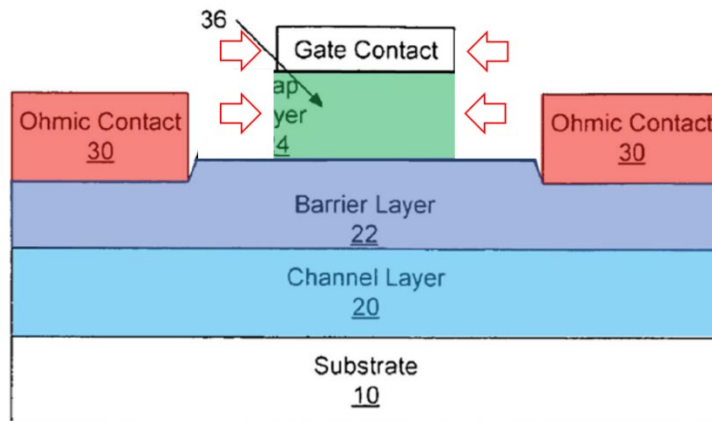
A POSA would not have modified the method of Saxler as modified by Beach and further based on Shenoy because the cap layer 24 and gate contact 32 of Saxler would already be in place on the transistor and etched by the technique of Beach to expose the side layers of the gate contact (32). EX2005 ¶162.



Pet. 45

In an attempt to support Petitioner’s position, Shealy alleges “gallium nitride is a pretty tough material to etch, and a lot of these etches will not etch it. So that – that’s again like Shenoy: The insulator is not being etched in Shenoy.” EX2004 at 99:18-21.

However, as Dr. Shealy apparently recognizes, gallium nitride is not an insulator. Shenoy specifically models the etching based on current distribution and not “tough[ness].”



Pet. 54 (showing etching of Shenoy)

Furthermore, Shealy is referring to “liquid metal etches” when mentioning “a lot of these etches” (EX2004 at 97:11-13, 9:14-17), which are not cited in the petition and thus have no bearing to the present claims. EX2005 ¶165.

Shenoy specifically relies on “Faraday’s law” and “Laplace’s equation” (EX1009 at 3) that equally apply to metals as well as semiconductors, thereby elucidating that the metal as well as the semiconductor is being etched away when Shenoy is applied to the transistor of Saxler. EX2005 ¶166.

Shenoy specifically models the etching based on equation 5, as reproduced below.

The current distribution at the anode has been combined with Faraday’s law to determine the evolution of the metal surface. The rate, r , at which the anodic surface recedes is

$$r = \frac{M\theta}{nF\rho} i \quad [5]$$

where M is the molecular weight of the metal, n is the metal dissolution valence, ρ is the density of the metal film, F is Faraday’s constant, and θ is the current efficiency of metal dissolution which is assumed to be constant at 100%.

EX1009, 3

In applying equation 5, the current distribution i would be zero for insulators (such as SiO₂), thereby showing that no etching would occur in the insulator (SiO₂) underlying Shenoy’s metal layer, consistent with Shenoy’s proposed results. EX2005 ¶¶168. However, a current distribution would occur in the gallium nitride

because it is not an insulator, thus etching would occur contrary to Petitioner's proposed modification. EX2005 ¶168.

In further addressing gallium nitride, Dr. Shealy alleges that “this is a p-type semiconductor doped with magnesium, and it would normally have holes. But because of these side surfaces, the holes are depleted away from the surface where the etching is occurring. And what that means is, is that the semiconductor layer behaves as an insulator just like Shenoy's structure, because there are no mobile charges near the etching region in the semiconductor.” EX2004 at 99:4-13.

However, neither Saxler nor Beach teach any passivating of the GaN material. According to Dr. Schubert, the cap layer of Saxler would still be conductive and thus be etched. However, even assuming that Dr. Shealy is correct, the side surfaces that would have been etched by Beach in the proposed modification are not relevant to the method of Shenoy. EX2005 ¶170. Rather, the spread or undercutting is induced by an underlying insulator. EX1009 at 1; EX2005 ¶170.

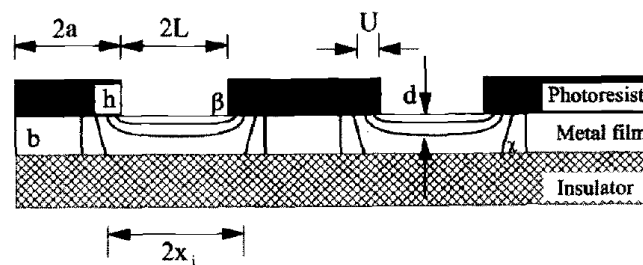
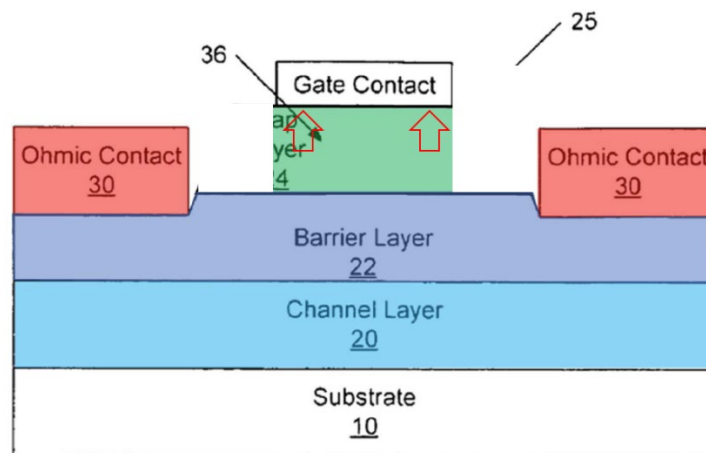


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

EX1009, Fig. 1

The etched sidewalls that Dr. Shealy is referring to would not underlie the gate contact. EX2005 ¶171. Rather, when comparing the mathematic setup of the Shenoy to the transistor of Saxler, the portion of the cap layer 34 underly the gate contact 32 in Saxler would actually be the surfaces pointed out in red below. *Id.* These surfaces would not have been etched by the self-aligned process of Beach. *Id.* Those same surfaces of the cap layer 34 are also relied on by Petitioner for the claimed ledges. *Id.*



Pet. 45 (annotated)

Even taking Dr. Sheely’s reasoning (which is incorrect), the ledges of the cap layer 34 would still “have holes” because it would not have been etched (EX2004 at 99:4-13) and thus not act as an insulator. Therefore, the underlying ledges of the cap layer 34 would be etched along with the gate contact in the etching process of Shenoy, thus not be retained. EX2005 ¶172.

Therefore, in addition to Beach, the actual teaching of Shenoy undercuts Petitioner’s motivation in “Saxler discloses such sloped sidewalls with the claimed

ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure.” Pet. 35. Applying the EMM etching of Shenoy would etch at least the alleged ledges of the cap layer 34 in Saxler that would underlie the gate contact in Petitioner’s proposed method. EX2005 ¶173. Thus, applying the method of Shenoy would not produce the hypothetical structure of Saxler, as alleged by Petitioner. What will happen is unpredictable at best. Shenoy’s etching process is not a selective etching with the exclusion of perfect insulators. EX2005 ¶174.

C. A POSA would not have found it obvious to combine Saxler, Beach, and Shenoy

1. Petitioner has not articulated a reason for POSA to combine all three references

Petitioner does not articulate a reason to combine Saxler, Beach, and Shenoy, and has left it to Patent Owner and the Board to fill in the gaps between the proposed combinations of Saxler with Beach and Shenoy. Petitioner’s failure to explain a reason to combine all three references undermines Patent Owner’s ability to respond to the obviousness contentions. EX2005 ¶177. It is well established that an “obviousness ground, in particular, cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with rational underpinning to support the legal conclusion of obviousness.” *TQ Delta, LLC*, 942 F.3d at 1359 (*quoting KSR* 550 at 418) (internal quotation marks omitted).

2. Petitioner fails to provide sufficient specifics on how the proposed method would actually be performed

Importantly, Petitioner has not provided a fabrication process sequence, neither in a narrative nor pictorial manner. Petitioner repeatedly relies on reasoning such as “no more than simple substitution” and “known methods that would be predictably implemented” (Pet. 34), but never gives the specific process sequence. By doing so, Petitioner attempts to avoid the conflicts and incompatibilities that arise from the proposed combinations being addressed. EX2005 ¶178.

Dr. Shealy’s testimony on obviousness was a conclusory statement that a person of ordinary skill in the art would have known, based on an alleged “simple substitution” of various claimed steps, how to combine any of a number of references to achieve the claimed inventions. This is not sufficient and is “fraught with hindsight bias.” *ActiveVideo Networks, Inc. v. Verizon Commc’n, Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012).

3. Petitioner mischaracterizes the method of Saxler as being “flexible” in alleging complete freedom to modify Saxler

Petitioner alleges “Sheppard, incorporated to disclose methods of fabricating GaN HEMTs (Saxler, [0046], [0068]), describes a flexible approach to masking and etching. It notes that ‘operations described as multiple steps could be combined into a single step’ (and vice versa), making the choice of Beach’s manufacturing steps no more than simple substitutions. Sheppard, [0058]; Shealy, [095].” Pet. 34.

However, “flexibility” is no substitute for motivation. Furthermore, splitting a single described step into multiple steps or combining multiple described steps into a single step as described by Shepperd does not support Petitioner’s proposed reverse engineering of Saxler’s process. EX2005 ¶181.

For example, Saxler does not disclose any “self-aligned” structures. Thus, there would be no motivation to apply the “self-aligned” technique of Beach. §IV.C. This is further evident from Petitioner’s reliance on the “self-aligned” technique of Beach for an intermediate step before applying the Shenoy process. Furthermore, the process of Shenoy cannot be implemented into the process of Saxler as modified by Beach without undue experimentation, as discussed in §IV.D. Thus, recreating the process of Saxler by piecing together 1) some steps of Saxler, 2) some steps of Beach, and 3) some steps of Shenoy (in no specified order) to arrive at the claimed invention goes far beyond any alleged “flexible” approach as suggested by Sheppard. EX2005 ¶182. It is impermissible simply to engage in a hindsight reconstruction of the claimed invention, using the applicant’s structure as a template and selecting elements from the references to fill the gaps. *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991).

Throughout Ground 1, Petitioner continues to apply Dr. Shealy’s “mix and match” rationale to “take all the embodiments and bring in which ones you want, depending on what you’re trying to accomplish.” EX2005 ¶183. However, this

rationale actually requires substantial modifications and improper hindsight according to “what you’re trying to accomplish.” *Id.*

For at least those reasons, *Saxler* in view of *Beach* and *Shenoy* does not render obvious claims 1-3 of the ’347 Patent. EX2005 ¶184.

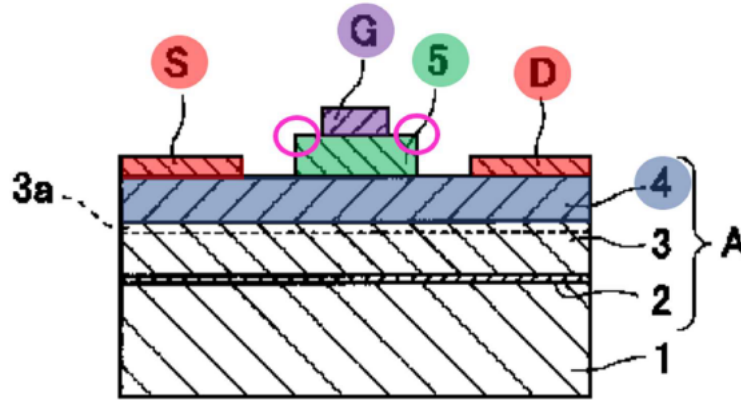
X. GROUND 4 (CLAIMS 1-7) – YOSHIDA ALONE

In Ground 4, Petitioner again improperly relies on a patent drawing as disclosing the claimed “ledges having substantially equal widths,” this time relying upon Fig. 1 of Yoshida. Pet. 83. With respect to the claimed horizontally extending sidewalls, Petitioner ignores the vertical sidewalls shown in Fig. 1 of Yoshida, and asserts that the claimed horizontally extending sidewalls are inherent. Pet. 75-79.

A. Yoshida does not disclose the pair of horizontal ledges have substantially equal widths of independent claim 1

1. The schematic of Fig. 1 cannot be relied on to show “substantially equal ledges”

Petitioner alleges “Yoshida’s **gate electrode** is narrower than **layer 5**, thereby exposing **horizontal ledges** that extend past the respective sidewalls of the **gate electrode** and toward the **source** and **drain**. Yoshida, [0022]-[0023], Fig. 1; Shealy, [214]. These ledges are symmetric on either side of the gate metal (i.e., having substantially equal widths). Yoshida, Fig. 1; Shealy, [214]. Yoshida thus discloses this element (Ground 4).” Pet. 83.



Pet. 83

For the same discussed in §VII.C before with respect to Saxler, Petitioner improperly relies upon patent drawings, asserting that Yoshida Fig. 1 discloses substantially symmetric ledges. Pet. 83. For the same reasons discussed in §VII.D, Petitioner argument fails in view of *Hockerson*.

Moreover, at his deposition Dr. Shealy discredited the accuracy of transistor schematics. EX2004 at 53:13, 53:16-25, 56:24-57:1, 60:17-18, 82:16-19. Yoshida itself demonstrates that patent drawings are not drawn to scale, and cannot be relied upon for dimensions. Layers 3 and 4 of Yoshida are shown in the schematic of Fig. 1 as having the same thickness, while Yoshida explicitly discloses that layer 3 is 10 times thicker than layer 4. EX1006 ¶¶[0020]-[0021]. At his deposition, Dr. Shealy specifically stated that the schematic of Fig. 1 of Yoshida cannot be relied on for its accuracy. (“Figure 1 [of Yoshida] doesn't appear like what's described in 23, because the SiO₂ isn't shown there. And it obviously was removed to get to that figure.”) EX2004 at 82:16-19.

B. Petitioner's reliance on the inherency of horizontally extending sidewalls is misdirected

With respect to the claimed horizontally extending sidewalls, Petitioner makes an inherency argument, asserting that manufacturing tolerances result in sidewalls extending horizontally are inherent in failing to provide motivation. Pet. 75-78. However, inherency is not proven “by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Not only must the missing descriptive matter be “necessarily” contained in the prior art reference, its inherent presence must also be so recognized by one of ordinary skill in the art. *Continental Can Co. USA, Inc. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991).

Petitioner fails to make such a case, and only engages in the exercise of probabilities or possibilities. Indeed, in his deposition, Dr. Shealy acknowledges the possibility of vertical sidewalls. EX2004 at 46:3-5. Dr. Shealy also acknowledges the possibility of achieving an “undercut” (EX2004 at 47:6-10) so that the sidewalls are formed extending inwardly; e.g., forming a gate material having whereby the top of the gate material is wider than the bottom of the gate material – exactly the opposite of what the claims require. Dr. Shubert agrees that vertical and undercut sidewalls are a possibility, such that horizontally extending sidewalls are not “necessarily” or “inherently” present in Yoshida. EX2005 ¶¶287-294 (further

examining Uemoto). *Rexnord Indus., LLC v. Kappos*, 705 F.3d 1347, 1355 (Fed. Cir. 2013).

C. Petitioner fails to address the “self-aligned” ledges of claims 2 and 5

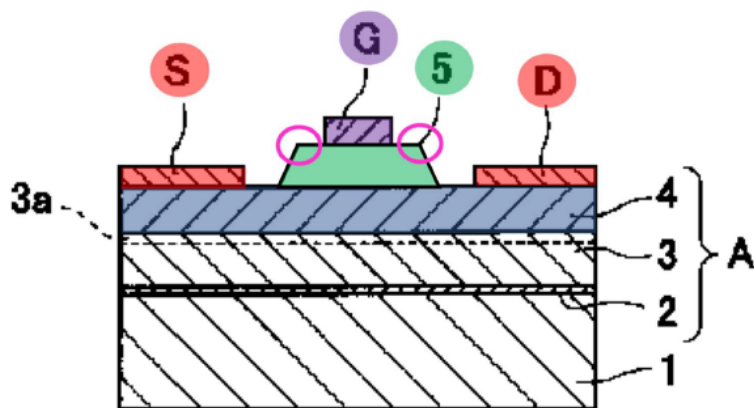
Similar to Grounds 1-3, Petitioner alleges that claim 2 is drawn to a device but is a product-by-process claim for ‘self-aligned’ ledges, which lends no patentable weight (Pet. 84) and “claim 5 is drawn to a device but [5f] includes a product-by-process element by requiring “self-aligned” ledges, which lends no patentable weight” (Pet. 86).

But, as explained in Section VII.E, the self-aligned process of the ‘335 patent advantageously results in a self-aligned gate **structure** with ledges of “substantially equal widths”, which is otherwise not achievable. Since Saxler does not disclose a self-aligned process, it is clear that Saxler does not disclose “self-aligned” ledges (“ledges of substantially equal widths”).

XI. GROUND 5 (CLAIMS 1-7) – YOSHIDA IN VIEW OF SAXLER

A. Petitioner makes no additional argument with respect to the claimed “substantially equal widths”

Similar to Ground 4, Petitioners alleges “the combination of Yoshida and Saxler also renders obvious [1f] (Ground 5).” Pet. 83.



Pet. 83

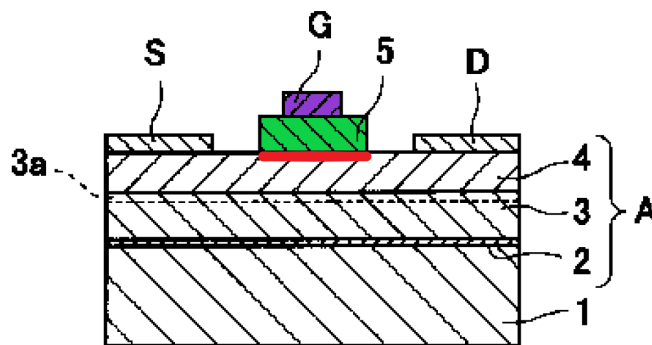
However, Petitioner provides no additional reasoning in Ground 5, that is not in Ground 4. Therefore, Ground 5 is insufficient for at least the reasons set forth above with respect to Ground 4 in §X.A.⁵

B. A POSA would not have modified Yoshida with the sloped sidewalls of Saxler

Petitioner alleges that “it would have been obvious to modify Yoshida’s transistor with the sloped sidewalls of Saxler’s capping layer to reduce gate leakage. Shealy, [185]-[189]. The combination calls for nothing more than the simple substitution of Saxler’s sidewalls to predictably make an enhancement-mode GaN HEMT. *Id.* And a POSITA would have recognized Saxler’s sidewalls would have reliably reduced Yoshida’s gate leakage, making the combination obvious. *Id.*” Pet.

⁵ In Ground 4, Petitioner relies on the statement that “Yoshida thus discloses this element” in referring to the “substantially equal widths” [1f]. Pet. 83. Ground 5 simply states “the combination of Yoshida and Saxler also renders obvious [1f].” Pet. 83. However, Petitioner provides no obviousness rationale with respect to the “substantially equal widths” [1f].

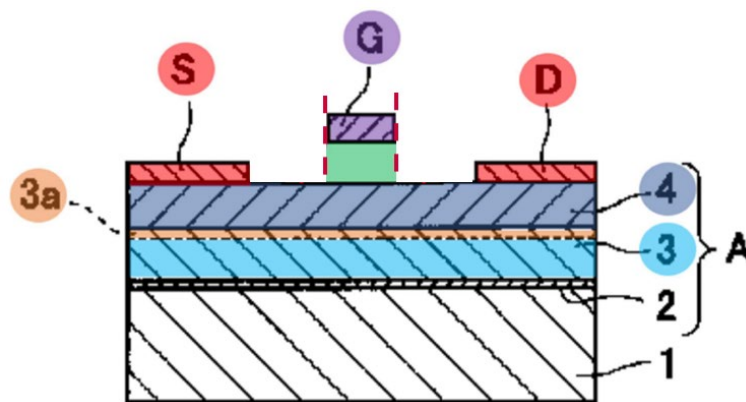
As discussed above in §VI.B, the gate structure of Yoshida is formed by a specific process where the p-type GaN layer 5 is layered and “etch[ed] away... except for where the gate electrode was to be loaded” (prior to loading the gate electrode G). EX1006 ¶[0022]. The transistor of Yoshida is assembled to position the pn junction of a p-type GaN layer 5 “immediately under” the gate electrode G for “voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility.” *Id.* ¶17. EX2005 ¶432.



EX1006, Figs. 1 (annotated)

Thus, Yoshida teaches away from adding the alleged sloped sidewalls of Saxler’s capping layer to the p-type GaN layer 5 because doing so would intentionally widen the **pn junction** relative to the gate electrode G creating misalignment, thus reducing “voltage control” by increasing the required amount of

carrier injection and reducing high-speed electron mobility. EX2005 ¶432. Indeed, the tapered sidewalls added from Saxler would just provide excessive surface area that cannot receive the gate electrode G, contrary to the intentional shape of the p-type GaN layer 5 of Yoshida. EX1006 ¶[0022] (“etch[ed] away... except for where the gate electrode was to be loaded”). EX2005 ¶433.

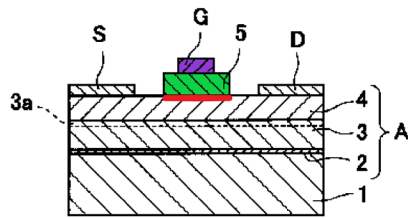


Pet. 73 (annotated)

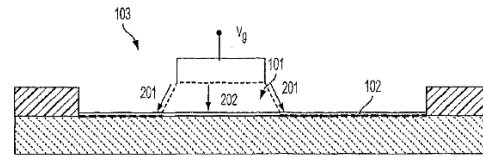
Furthermore, as discussed above in §§VI.A, VII.B-C and addressed by Dr. Shealy, the recessed embodiment of Saxler as relied on by Petitioner is not an enhancement-mode transistor (EX1003 ¶[0146]) and thus does not provide any guidance on “predictably mak[ing] an enhancement-mode GaN HEMT” as relied on by Petitioner. EX2005 ¶434. The cap layer of Saxler extends substantially the entire width between the source and the drain (EX1007, Fig. 1A) while Yoshida intends to limit the width of its p-type GaN layer (EX1006 ¶[0022]). EX2005 ¶434.

Petitioner cites additional prior art and Applicant’s own specification. Pet. 71. However, none of the references discloses an enhancement-mode GaN HEMT

with both ledges and horizontally extending sidewalls. EX2005 ¶435. In other words, Yoshida arguably has ledges for loading the gate electrode but limits the width of its p-type GaN layer (EX1006 ¶[0022]), while Fig. 2 of the present application has horizontally extending sidewalls but no ledges (because it is self-aligned). A POSA would not apply the horizontally extending sidewalls of Fig. 2 to the gate-last structure of Yoshida in forming both ledges and horizontally side walls because it would undesirably increase the **pn junction** reducing “voltage control” by increasing the required amount of carrier injection and reducing high-speed electron mobility. EX1006 ¶[0022]. EX2005 ¶435.



EX1006, Figs. 1 (annotated)



‘335 Patent, Fig. 2

Thus, a POSA would not modify the enhancement-mode transistor of Yoshida with tapered sidewalls from the depletion-mode transistor of Saxler nor the self-aligned process from the present application. Any such modification would be improperly based on hindsight. EX2005 ¶436.

C. The “self-aligned” ledges of claims 2 and 5 are absent from Yoshida

Similar to Grounds 1-3, Petitioner alleges that claim 2 is drawn to a device but is a product-by-process claim for ‘self-aligned’ ledges, which lends no patentable weight (Pet. 84) and “claim 5 is drawn to a device but [5f] includes a product-by-process element by requiring “self-aligned” ledges, which lends no patentable weight” (Pet. 86).

But, as explained in Section VII.E, the self-aligned process of the ‘335 patent advantageously results in a self-aligned gate **structure** with ledges of “substantially equal widths,” which is otherwise not achievable. Since Yoshida does not disclose a self-aligned process, it is clear that Yoshida does not disclose “self-aligned” ledges.

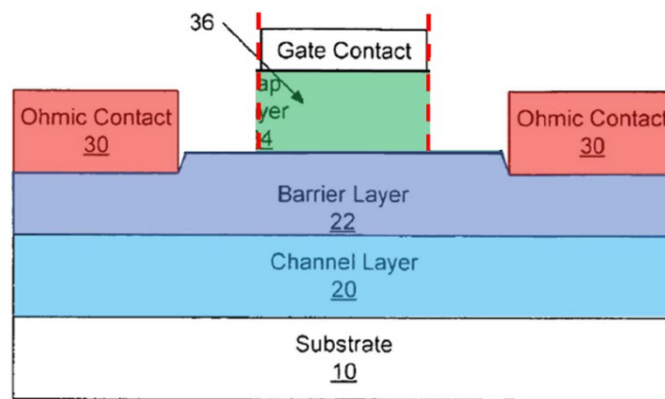
XII. GROUND 6 (CLAIMS 2 AND 5-7) – YOSHIDA IN VIEW OF SAXLER, BEACH, AND SHENOY

A. In modifying Yoshida, Petitioner relies on contradictions and improper assumptions to allegedly arrive “at the same gate structure”

Petitioner alleges “a POSITA would have found it obvious to modify Yoshida-Saxler by using Beach’s self-aligned technique and Shenoy’s isotropic etching to arrive at that same gate structure, which would have improved efficiency by eliminating masking and etching steps and would have ensured symmetry of the gate metal with respect to the p-gate material.”

B. The “self-aligned” technique of *Beach* would not produce the sloped sidewalls of Saxler-Yoshida, as relied on by Petitioner

Petitioner alleges that “a POSITA would have found it obvious to use Beach’s approach to create Yoshida-Saxler’s gate structure,.” Pet. 91. However, as further above in §VII.E and as acknowledged by Dr. Shealy, applying Beach’s self-aligned technique would either cut off or not form the horizontally extending “sloped” side surfaces that Petitioner relies on from Fig. 1A of Saxler. EX2005 ¶¶145, 207. Importantly, applying Beach’s self-aligned technique would also cut off the ledges.

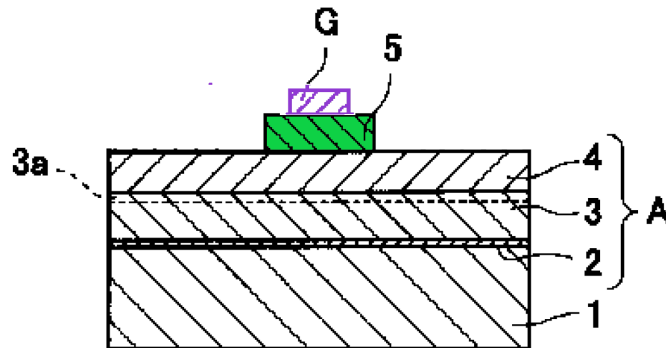


Beach applied to Saxler modified Fig. 1A

C. A POSA would not have any reason to form ledges after the self-aligned process of Beach

Petitioner alleges “a POSITA would have found it obvious to use Beach and Shenoy’s techniques to self-align the p-type gate material and gate metal and isotropically etch the gate metal using a single mask to obtain self-aligned ledges, resulting in the same gate structure that Yoshida-Saxler discloses.” Pet. 72.

As discussed in §VI.B, the transistor of Yoshida is formed by a process where the p-type GaN layer 5 is layered and “etch[ed] away... except for where the gate electrode was to be loaded” (prior to loading the gate electrode G). EX1006 ¶[0022]; EX2005 ¶251.



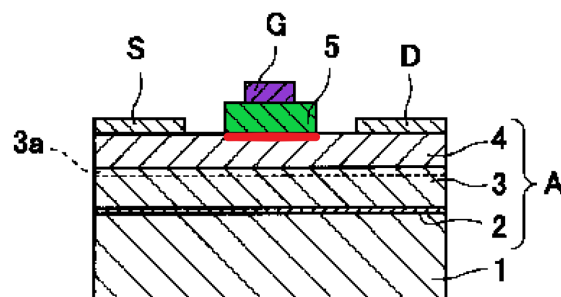
EX1005, Fig. 1 (annotated)

Although the p-type GaN layer 5 is illustrated as being formed wider than the gate G, that structure is typical for processes where the p-type GaN layer 5 is patterned before the gate electrode G is loaded to provide a wider platform to ensure that the gate electrode is received on the p-type GaN layer 5 without overhang. ‘335 Patent at 4:52-54; EX2005 ¶267.

This is consistent with the references that Petitioner cites to show a pair of ledges, where the ledges are common when the base is patterned before the electrode metal is deposited. EX1011 Fig. 1, ¶[0006] (“processed with two different photo masks”); EX1018 at Fig. 1, Page 1 (“Transistors were then fabricated with... source-drain contacts... Ni/Au contacts were then deposited over the selective area grown

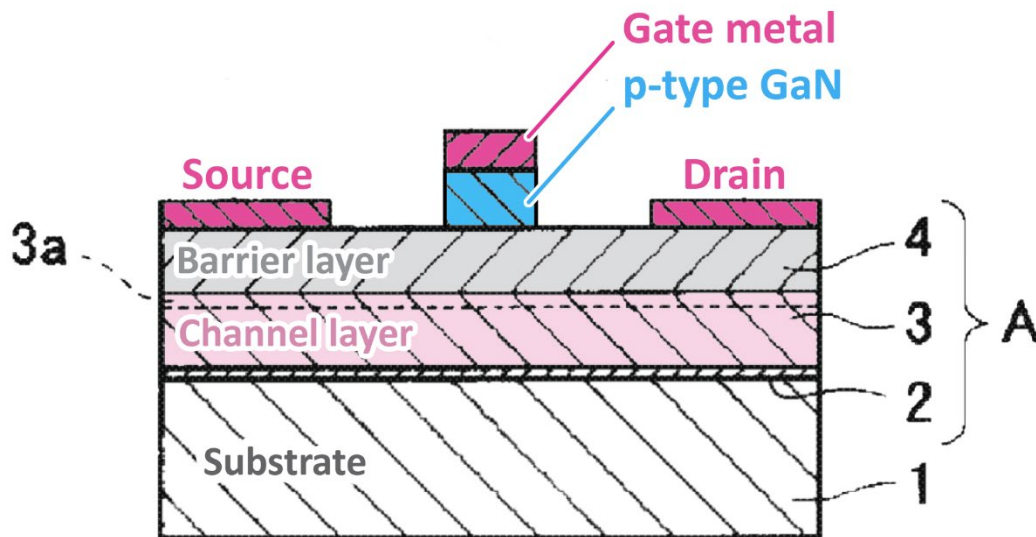
p-GaN regions.”); EX1017, Figs. 5-6; ¶[0056] (“Referring to FIG. 5, the *p*-type Al_zGaN cap layer 11 is etched to define a gate region where the *p*-type Al_zGaN cap 11 is located. Referring to FIG. 6, a gate 17 with a Schottky contact... are formed on the Ga-face to form an assembly.”); EX1007 Fig. 1A, 1B, ¶¶61-65; EX2005, ¶268.

Yoshida does not describe any operational function of the illustrated ledges after the gate electrode is loaded. Rather, as previously discussed, the transistor of Yoshida is assembled to locate the **pn junction** of a *p*-type GaN layer 5 “immediately under” **the gate electrode G** for “voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas (2DEG) layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility.” EX1006 ¶[0017]. This is obtained in the gate-last approach of Yoshida by “etch[ing] away the *p*-type GaN layer except for where the gate electrode was to be loaded.” EX1006 ¶[0022]. EX2005 ¶¶269-270.



EX1005, Fig. 1 (annotated)

If a POSA were to modify the process of Yoshida to incorporate the “self-aligned” technique of Beach, this “self-aligned” technique would achieve what Yoshida intends. The p-type GaN layer 5 would be “etch[ed] away... except for where the gate electrode was [] loaded” because the gate electrode G would be self-aligned with the p-type GaN layer 5. EX1006 ¶[0022]. Thus, the pn junction of a p-type GaN layer 5 would be “immediately under” the gate electrode G. EX1005 ¶[0017]. The direct alignment of the gate electrode G with the pn junction would optimize “voltage control with a small amount of carrier injection” as is the intended result of Yoshida. EX1005 ¶[0017]; EX2005 ¶271.



EX1008, Fig. 1 (modified with self-aligned etch of Beach)

Thus, a POSA would have no reason or motivation to perform additional etching steps to form the claimed ledges that have no disclosed operational function after the gate metal G is loaded on the p-type GaN layer 5. Indeed, Petitioner

provides no motivation or reasoning for a POSA to perform additional etching steps to form ledges that have no disclosed operational function after the gate electrode G is loaded on the p-type GaN layer 5. EX2005 ¶269.

Indeed, the unnecessary etching would just add manufacturing cost and steps, producing a less efficient method, contrary to motivations relied on by Petitioner. Pet. 32, 35, 48, 54-56, 64, 77; EX1003 ¶¶[0093], [0205] (“eliminating masking and etching steps,” “reduc[ing] steps and costs” and predictably creating the “stacked gate structure more efficiently”). Petitioner merely relies on the depiction of Yoshida in Fig. 1, which is a schematic of a transistor formed by the p-type GaN layer 5 being etched before the gate electrode G. EX2005 ¶273.

Furthermore, selectively etching the gate electrode G after being loaded on the p-type material 5 would be contrary to the intention of Yoshida because it would intentionally reduce the width of the gate electrode G relative to the pn junction creating non-overlapping segments of the pn junction, thus reducing “voltage control” by increasing the required amount of carrier injection. EX2005 ¶274.

D. The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges based on Petitioner’s reasoning

As addressed in §IX.B, a POSA would not apply the mathematic model to Yoshida in view of Saxler. Furthermore, the mathematical model would not produce the structure as alleged by Petitioner because it would etch at least the ledges as

relied on by Petitioner.

E. Yoshida teaches away from using other methods of manufacturing its gate

Yoshida distinguishes its process from forming the gate structure with “conventional photolithography and etching” in that the transistors produced by those “conventional” methods “cannot be said to have sufficient electron mobility to meet recent demands for still higher speed operations.” EX1006 ¶¶[0006], [0008]. EX2005 ¶278.

Thus, Yoshida directly contradicts Petitioner’s statement that “a POSITA would have been familiar with many ways to create Yoshida-Saxler’s stepped gate structure and would have used these methods interchangeably.” (Pet. 89), where Yoshida expressly distinguishes its method from “conventional photolithography and etching.” EX1006 ¶¶[0006], [0008]. EX2005 ¶320.

This configuration and functionality are not produced by prior art relied on by Petitioner, specifically Saxler, Shenoy, and Ahn, that are directed to producing completely different transistors or even theoretical mathematical models as discussed herein. EX2005 ¶322.

For at least these reasons, Petitioner’s proposed reverse engineering of Yoshida in ground 6 in “trying to accomplish” (EX2004 at 41:24-42:1) the claimed invention fails. EX2005 ¶438.

F. A POSA would not have found it obvious to combine Yoshida Saxler, Beach, and Shenoy

1. Petitioner improperly relies upon the schematic of Fig. 1 in Yoshida

Ground 6, like Grounds 4 and 5, is based again on the schematic of Fig. 1 of Yoshida. Pet. 88 (“resulting in the same gate structure that Yoshida-Saxler discloses”). However, that premise is improper as further discussed with reference to the related transistor schematic as discussed in §VII.D. *Hockerson*, 222 F.3d at 956 (Fed. Cir. 2000).

2. Petitioner’s obviousness assertion lacks motivation

In again relying on Saxler, Beach and Shenoy in addition to Yoshida, Petitioner’s argument has similar deficiencies in motivation as further discussed in §IV.F.

XIII. RESERVATION OF RIGHTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if IPR is instituted. Similarly, Patent Owner does not concede any underlying contentions in the Petition and reserves the right to rebut any such contention later. Further, Patent Owner is not limited to the arguments presented in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments,

not presented herein.

XIV. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and no *inter partes* review should be instituted.

Dated: June 18, 2024

Respectfully submitted,

/Walter D. Davis, Jr./
Walter D. Davis, Jr. (Reg. No. 45,137)
walter.davis@blankrome.com
Blank Rome LLP
1825 Eye St NW
Washington, DC 20006
Tel: 202-420-2200
Fax: 202-420-2201

Counsel for Patent Owner

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 13,369 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

Dated: June 18, 2024

Respectfully submitted,

/Walter D. Davis, Jr./
Walter D. Davis, Jr. (Reg. No. 45,137)

Counsel for Patent Owner

CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S RESPONSE** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

Innoscence-EPC-IPRs@finnegan.com

Dated: June 18, 2024

Respectfully submitted,

/Walter D. Davis, Jr./
Walter D. Davis, Jr. (Reg. No. 45,137)

Counsel for Patent Owner