Filed: September 20, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD., AND INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01382
U.S. Patent 9,748,347

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 9,748,347

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Ex. 1019	U.S. Patent Application Publication No. US 2005/0087763 A1 to Kanda et al. ("*Kanda*")
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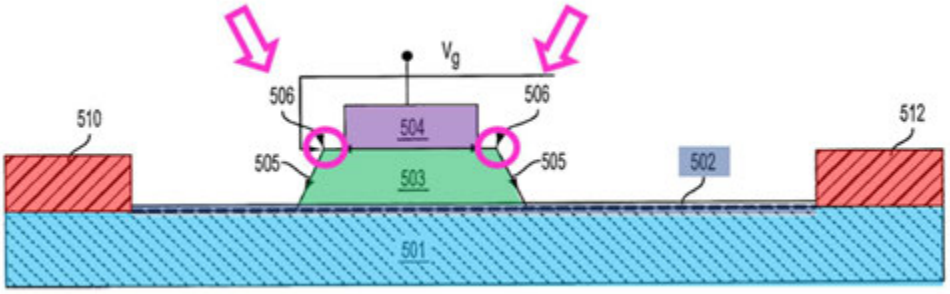
Exhibit	Description
Ex. 1029	C. S. Suh et al., "p-GaN/AlGaN/GaN Enhancement-Mode HEMTs, 2006 64th Device Research Conference, June 2006, pp. 163-164 ("*Suh 2006*")

*Emphasis added herein unless otherwise noted.

I. Introduction

Petitioners request *inter partes* review and cancellation of claims 1-3 of U.S. Patent No. 9,748,347 ("the '347 patent") (Ex. 1001).

Independent claim 1 recites a conventional method for manufacturing an enhancement-mode gallium nitride (GaN) high electron mobility transistor (HEMT) device. The transistor includes a **GaN channel layer** below an **AlGaN barrier** and a stacked gate structure that rests on the **barrier** layer between **source** and **drain electrodes**. That gate structure has two layers: a **p-type gate material** with sloped sidewalls below an overlying **gate metal** contact. The patent claims using a photoresist over the gate metal, then etching the **gate metal** and **p-type gate material**. The '347 patent admits that ***all*** these features were conventional. Ex. 1001, 1:19-2:25, Figs. 1-2, 3A-3B; Shealy, [044]-[046].



Ex. 1001, Fig. 5.[1]

[1] All figures in this Petition containing color are annotated.

The claims also require etching the gate metal a second time to form a pair of horizontal **ledges** on the p-type gate material's surface—the ***sole point*** of alleged novelty. But the patent admits such ledges were ***also*** conventional, long found in the prior art, and made using different, interchangeable methods. *Lidow,* Fig. 1. *Yoshida* shows just such ledges in a GaN HEMT with a p-type GaN gate cap (*Yoshida*, Fig. 1). So does *Hu*. *E.g., Hu*, Fig. 1. And *Smith*. *Smith*, Fig. 3. And *Saxler*. *Saxler*, Figs. 1A, 2B, [0052]. And *Suh*. *Suh*, Fig. 6.

The Board should institute and cancel claims 1-3.

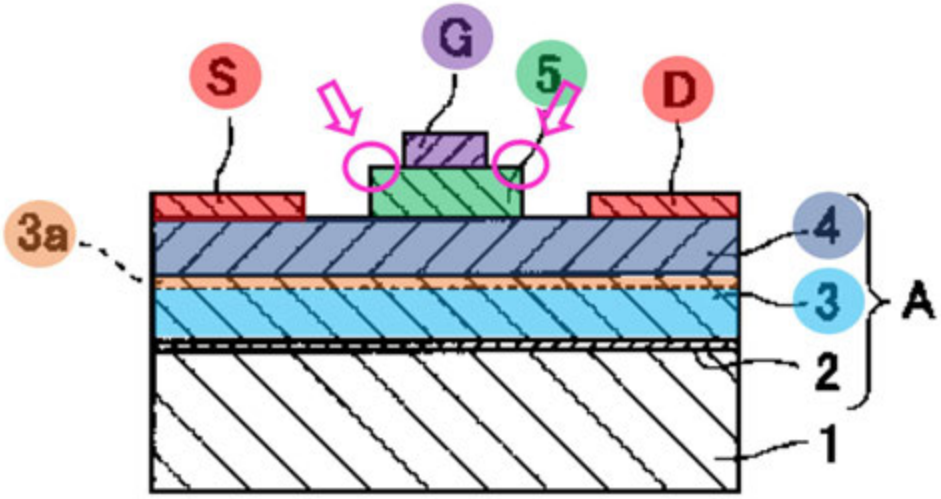
II. Technological Background

GaN power transistors have a large band gap, which increases breakdown voltage and makes them attractive for high-power applications. Ex. 1001, 1:25-44; Shealy, [055]. They were well known long before the '347 patent. *E.g.*, *Smith*, [0004]-[0010]. Conventional transistors include **GaN channel** and **AlGaN barrier** layers (with a **two-dimensional electron gas (2DEG) region** at their heterojunction), **source** and **drain electrodes**, and a gate structure including **GaN materials** under a **gate metal**. Ex. 1001, 1:24-2:21; *Yoshida*, Abstract; *Suh*, [0002]-[0005], [0015], Figs. 1, 6-7; Shealy, [055].

Enhancement-mode GaN transistors are normally off, meaning no drain current flows through the 2DEG without positive voltage on the gate. Ex. 1001, 1:45-48, 1:59-64; *Hu*, 1; Shealy, [056]. These devices achieve normally-off state in

part with a **GaN layer**, often p-type, in the gate structure under a **gate metal**, which increases the gate voltage to a positive value. Ex. 1001, 1:45-48, 1:59-64; *Hu*, 1; Shealy, [056].

Example GaN HEMT arrangements in publications ranging from 1999 through 2009, the earliest claimed priority date of the '347 patent, are shown below. Shealy, [057]. Note the **horizontal ledges** at the surface of the **p-type GaN gate materials**:



Yoshida, Fig. 1 (1999).

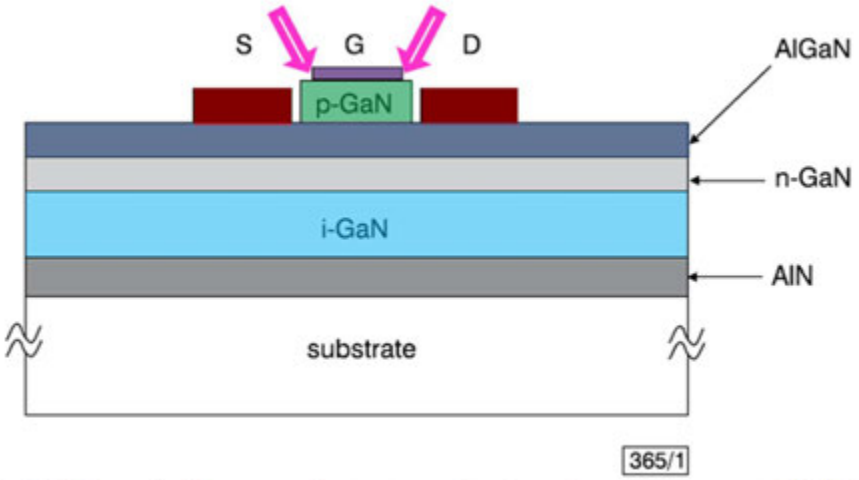


Fig. 1 *Schematic diagram of structure of pn junction regrown gate HFET*

Hu, Fig. 1 (2000).

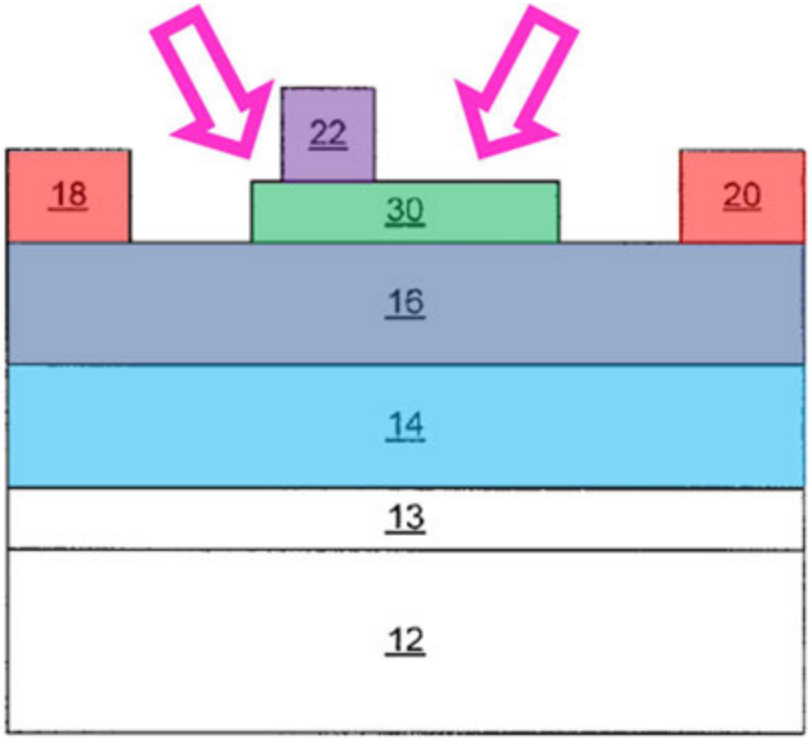
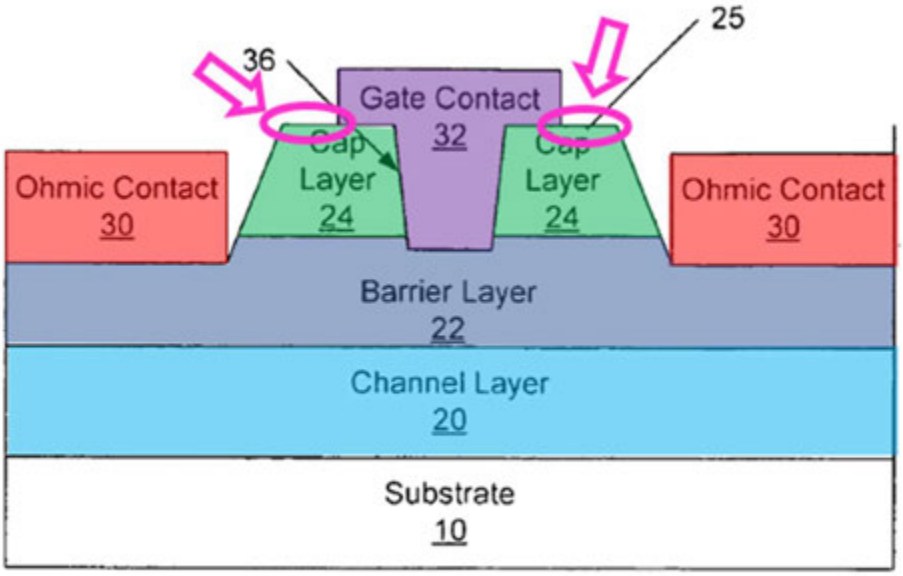
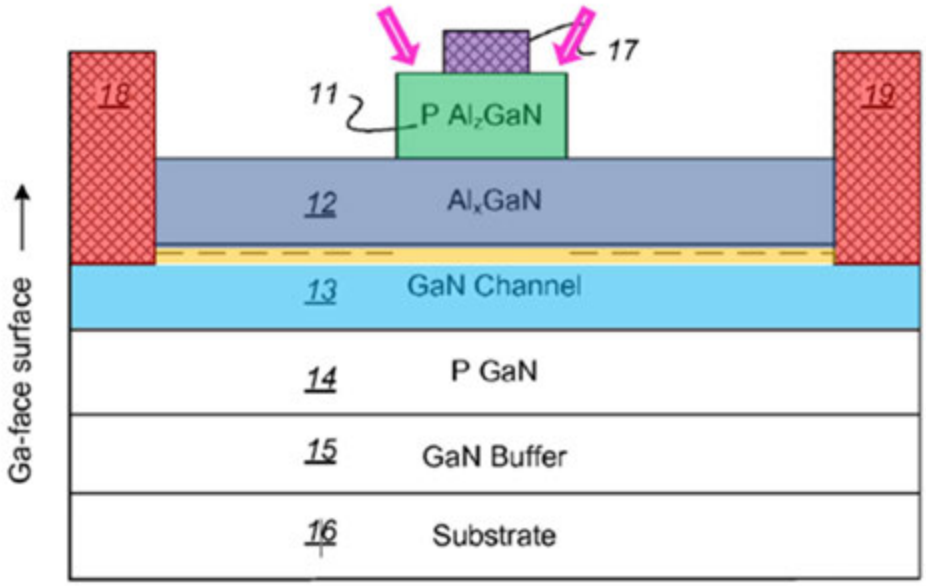


Figure 5B

Smith, Fig. 5B (2002).



Saxler, Fig. 1A (2006).



Suh, Fig. 6 (2009).

As these examples illustrate, the sole point of alleged novelty of the '347 patent, making **ledges** at the surface of **p-type GaN gate materials**, was common—as were the other claim features. Shealy, [058].

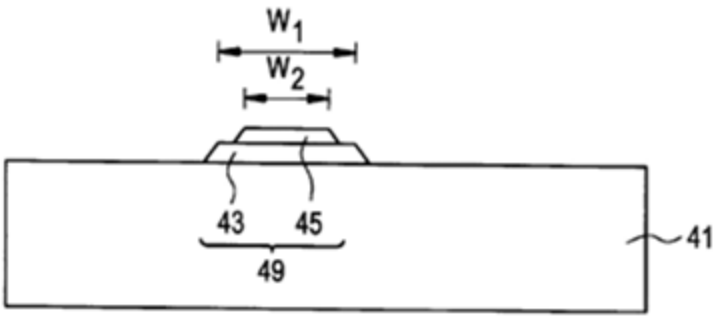
The prior art included many different methods of manufacturing these devices. Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Yoshida*, *Kanda*, *Hu*, *Smith*, *Suh*, *Shenoy*, Ex. 1023). For example, single-mask techniques to self-align stacked gate structures were long-known. Shealy, [059] (citing *Beach*, [0040]). Conventional etching techniques achieved sloped sidewalls, which were known to increase leakage paths. Shealy, [059] (citing Ex. 1001, 1:49-2:3, Fig. 2; *Saxler*, [0064], Figs. 1A-1B; *Ahn*; *Xu*; *Sheppard*, [0044]). And it was conventional for decades to undercut photomasks by isotropically etching metals. Shealy, [059] (citing *Shenoy*, 1).

A POSITA would have known many methods for making stepped gate structures with **ledges**, including (i) sequential masking and etching techniques, (ii) lift-off techniques, and (iii) self-aligned techniques. Shealy, [060] (citing *Yoshida*, [0022]-[0023]; *Hu*, 1; *Smith*, [0040]-[041]; *Saxler*, [0064]-[0066]; *Suh*, [056]). For example, *Yoshida* discloses sequential masking and etching the p-type GaN **layer 5**, then depositing the **gate electrode**. *Yoshida*, [0022]-[0023]; Shealy, [060]. *Hu* grows gate layers in "selective areas defined by opening in an SiO_2 mask." *Hu*, 1 (sequential masking and etching); Shealy, [060]. *Kanda* forms stepped gate structures using lift-off. *Kanda*, [0091], [0110], [0123], [0137], [0151], Figs. 2C, 5C, 7C, 9D, 11D; Shealy, [060]. *Smith* fabricates its gate structure by patterning the **GaN cap layer**, etching to remove portions, then forming a **gate electrode**

(sequential masking and etching). *Smith*, [0040]-[0041]; Shealy, [060]. *Smith* also uses ***self-aligned*** techniques. *Smith*, [0041]-[0044], Figs. 6A-6C; Shealy, [060]. *Saxler* discloses sequential masking and etching to form its stacked gate structure. *Saxler*, [0064]-[0066]. *Suh* likewise etches "to define a gate region where the p-type AlGaN cap 11 is located," and depositing the gate on top. *Suh*, [0056] (sequential masking and etching); Shealy, [060].

Beach makes a self-aligned two-layer gate structure using a single photomask. *Beach*, [0040], [0045], [0054]; Shealy, [061]. *Ahn*, published in 1999, uses one mask and isotropic and anisotropic etching to create stacked stepped gate structures with sloped sidewalls. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C; Shealy, [061].

FIG. 4C



Ahn, Fig. 4C.

In addition, long before the '347 patent, *Shenoy* isotropically etched and undercut metal layers below masks, which a POSITA would understand would be

one option for stepped gates. *Shenoy*, 2-3; Shealy, [062]. Lift-off had similarly been known for decades for creating steps. Shealy, [062] (citing Ex. 1022).

Typical GaN HEMT devices thus included every feature and manufacturing method claimed in the '347 patent. Shealy, [055]-[063].

III. The '347 Patent

A. Overview

1. The alleged invention

The '347 patent describes and claims a method of manufacturing an enhancement-mode GaN power transistor. Ex. 1001, 1:19-23, 2:29-53, Fig. 5, claims 1-3; Shealy, [044]. It asserts that conventional GaN HEMT devices suffered from high leakage between the gate and 2DEG region. Ex. 1001, 1:17-2:25; Shealy, [044]. The '347 patent admits that conventional GaN enhancement-mode devices included **a GaN channel layer**, **an AlGaN barrier layer**, **source** and **drain electrodes**, and a gate structure consisting of a **p-type GaN layer with sloped sidewalls** to address gate leakage (identifying **leakage path 201**) and an overlying **gate metal**—all features in the '347 patent claims. Ex. 1001, 1:17-2:25, Figs. 1-2, 3A-3B, claims 1-7; Shealy, [044].

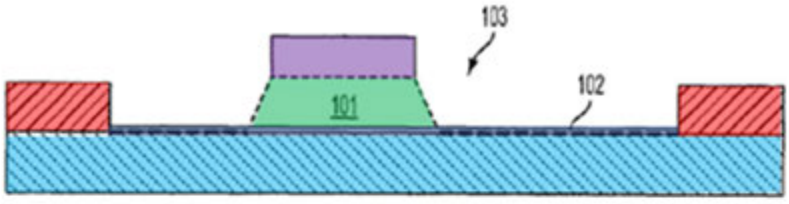


FIG. 1
PRIOR ART

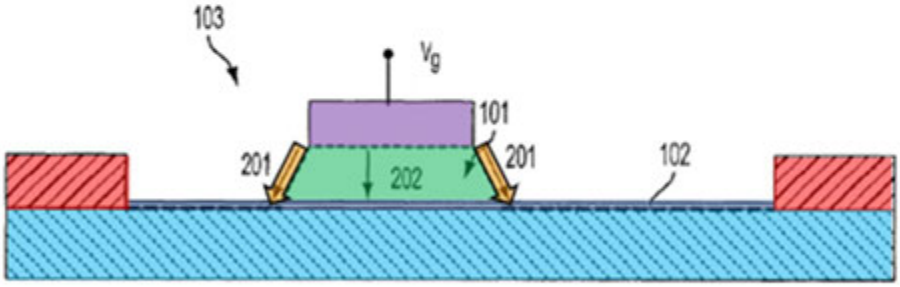


FIG. 2
PRIOR ART

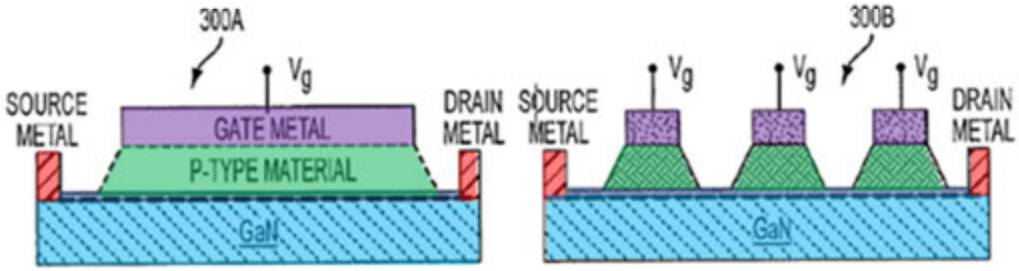


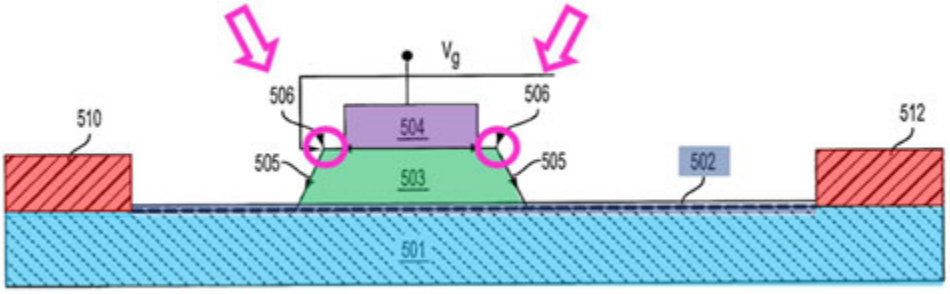
FIG. 3A
PRIOR ART

FIG. 3B
PRIOR ART

Ex. 1001, Figs. 1-2, 3A-3B.

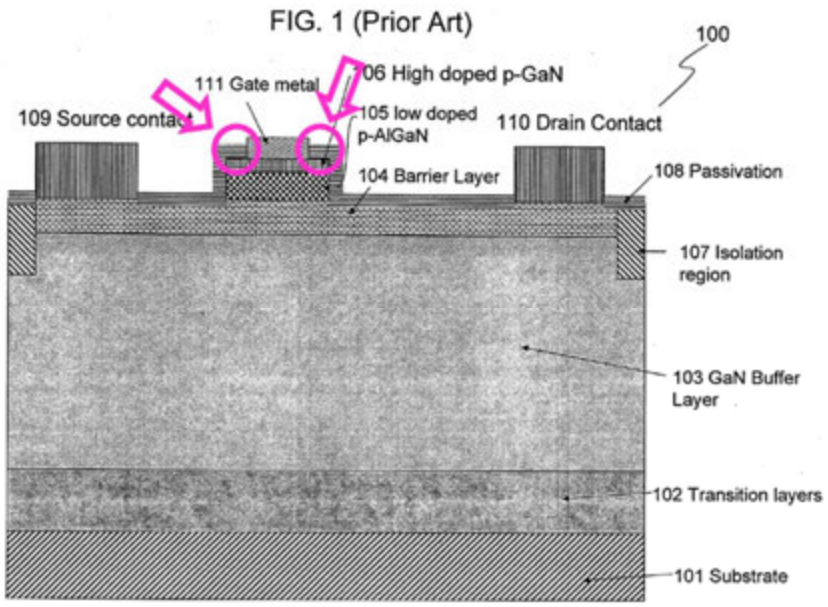
To address gate leakage, the '347 patent adds ***just one purportedly novel structure***: a pair of **ledges** on the p-type gate material, on either side of the gate metal. Ex. 1001, 2:29-53, 3:60-4:7, 4:40-51, Figs. 1-2, 3A-3B, 4-5, 7A-7B, 8, claims 1-7; Shealy, [045]. It also asserts advantages to making these ledges using a

"self-aligned" technique employing a single photomask. EX. 1001, 3:60-4:12, 4:46-57.



Ex. 1001, Fig. 5.

Lidow, the prior application, admits these ledges were known. *Lidow*, Fig. 1; §III.B; Shealy, [046].



Lidow, Fig. 1.

2. Self-aligned ledges

In some embodiments, the '347 patent makes its **ledges** using a self-aligned process:

1. Forming a **GaN layer** , **AlGaN layer** , and **p-type gate material**.
2. Depositing the **gate metal**.
3. Applying a **photoresist**.
4. Etching the **gate metal**.
5. Etching the **p-type gate material**.
6. Etching the **gate metal** again, undercutting the same **photomask.**

Ex. 1001, 4:8-33, claim 3, Figures 6A-6C; Shealy, [047].

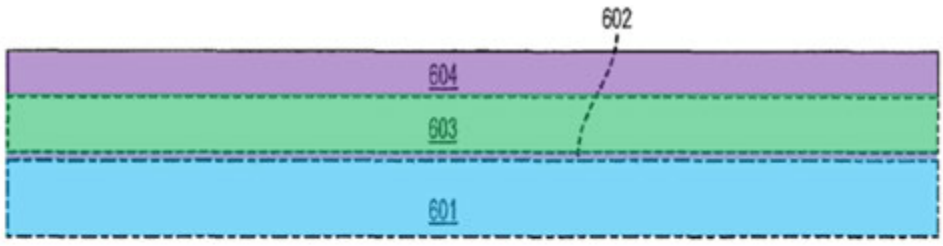


FIG. 6A

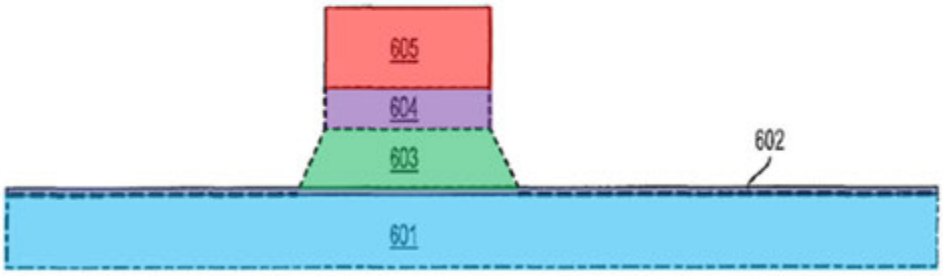


FIG. 6B

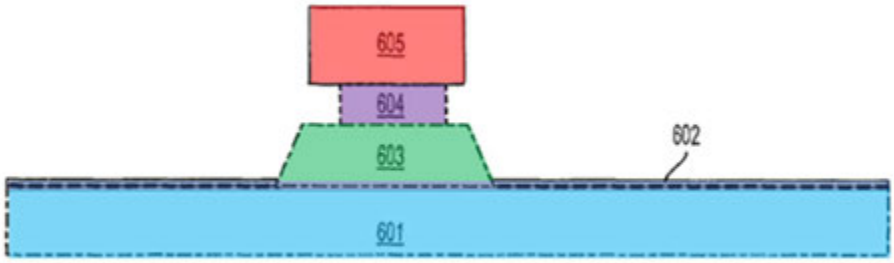


FIG. 6C

Ex. 1001, Figs. 6A-6C.

B. Prosecution History

The '347 patent claims priority to U.S. Provisional Patent Application No. 61/860,976, filed August 1, 2013. Ex. 1001, cover, p. 2. It also claims priority as a continuation-in-part to U.S. Application No. 13/838,792 which was a division of U.S. Application No. 12/756,960, filed April 8, 2010, and claims priority to U.S. Provisional Patent Application No. 61,167,777, filed April 8, 2009. *Id.* But this second priority claim was only raised after the Examiner rejected the claims over the alleged priority application, *Lidow* (U.S. 2010/0258843A1, Ex. 1011), which was, disclosed as admitted prior art *by the applicant* before making the belated priority claim. Ex. 1002, 95-128, 250.

Incredibly, despite already admitting *Lidow* was prior art through an IDS, the applicant reversed its previous representation and instead *claimed priority as a continuation-in-part to Lidow itself*, utilizing a "Petition for ***Unintentionally*** Delayed Domestic Benefit Claim," including the required sworn statement by the

prosecuting attorney that the "entire delay" was "unintentional," and that the petition was filed "immediately upon discovery." Ex. 1002, 104-05, 118-19. This petition was filed over a year after the applicant corrected domestic priority for filing receipt errors on the same day it submitted *Lidow* as prior art (Ex. 1002, 250, 282-90), and months after the Office cited *Lidow* as invalidating prior art (Ex. 1002, 227-34). The Office nonetheless granted the Petition without investigating the basis for the attestation of unintentional delay, Ex. 1002, 95-103, and the parent eventually issued as the '347 patent, *id.*, 1.

Because of this history, Petitioners disagree that the '347 patent properly claims priority to U.S. Application Nos. 12/756,960, 13/838,792, and 61/860,976, and contend it is unenforceable for inequitable conduct by the prosecuting attorney in submitting a false petition. But for the acceptance of this false petition, *Lidow* is invalidating prior art. Petitioners intend to challenge this priority claim in a separate *Ex Parte* Reexamination (EPR) proceeding.

For purposes of this petition, however, Petitioners nevertheless assume priority to the earliest priority filing date, April 8, 2009.

Also, for purposes of this petition alone, Petitioners assume that the earliest application supports the claims just as the Examiner found support *Lidow* supported the claims after applicant broadened them by removing the "isotropically etching" requirement, discussed in detail below. Ex. 1002, 52, 75-76, 85-86.

After determining the claims had support in *Lidow*, the Examiner rejected them over *Hikita* (Ex. 1016) and U.S. Patent Publication No. 2006/0157735. Ex. 1002, 50-54. Both references had ledges but neither included sloped sidewalls in its gate structure (although they do under patent owner's new construction, described below). *Id.* The Examiner thus indicated a dependent claim directed to making sloped p-type gate material sidewalls would be allowable, and the applicant amended the independent claim accordingly to receive an allowance. Ex. 1002, 44-48, 55.

Notably, the '347 patent was allowed without specifically disclosing a method to etch the gate metal to obtain the claimed ledges because such methods were well within a POSITA's ability. Shealy, [050], [059]-[062] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Yoshida*, *Kanda*, *Hu*, *Smith*, *Suh*, *Shenoy*, Ex. 1023); Ex. 1002, 25-30, 44-55, 74-76, 80-99. The applicant argued that *Lidow* at [0044]-[0045] and Fig. 10 supports "etching" the gate metal to form ledges. Ex. 1002, 76. But *Lidow* only states that "[f]ollowing the step shown in FIG. 3C, the wafer is placed back in an etching machine that only etches the gate metal layer 17, without etching any other part of the device," resulting in the structure of Figures 9-10. *Lidow*, [0043]-[0045]. This does not explain ***how*** the metal is etched to create the claimed **ledges**. Shealy, [050].

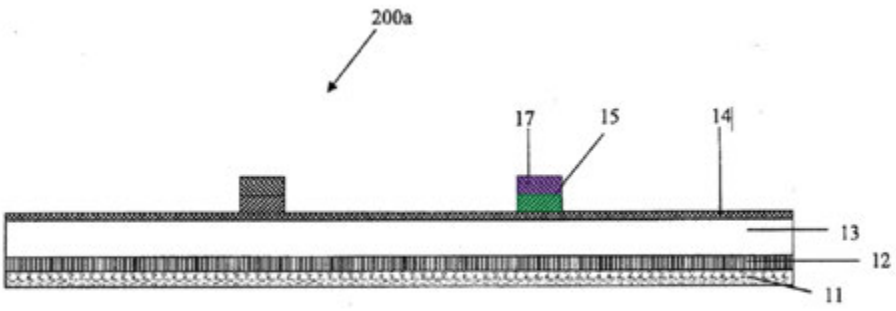


FIG. 3C

Lidow, Fig. 3C.

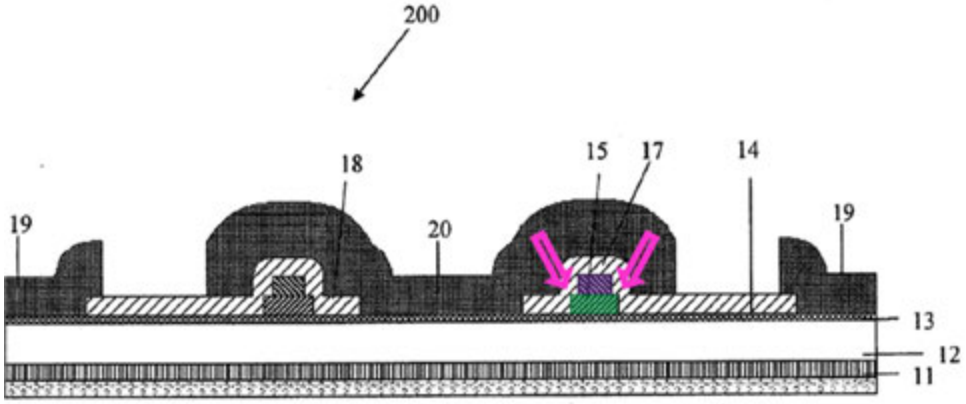
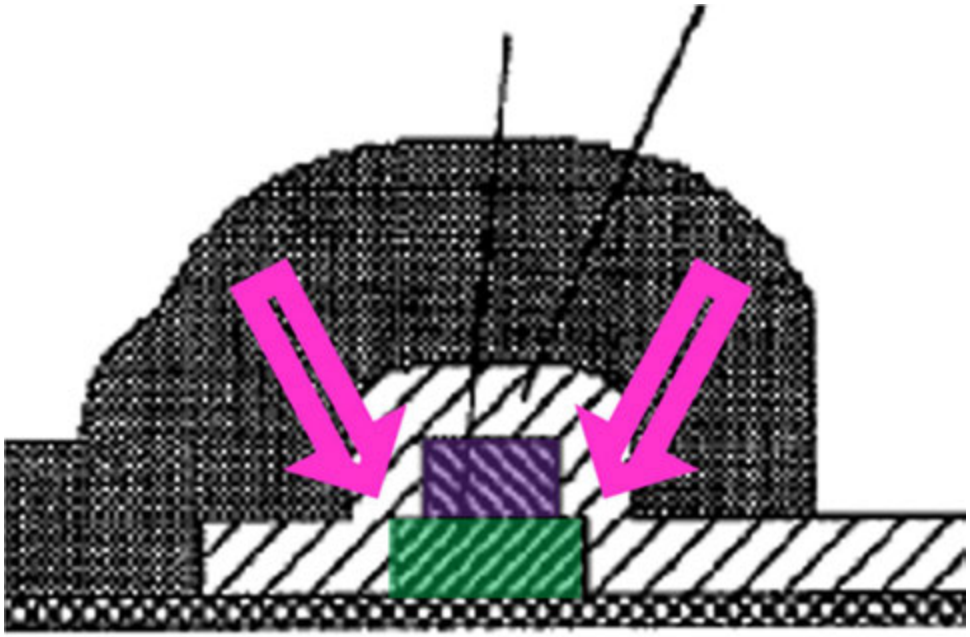


FIG. 9

Lidow, Fig. 9.



Id. (excerpted).

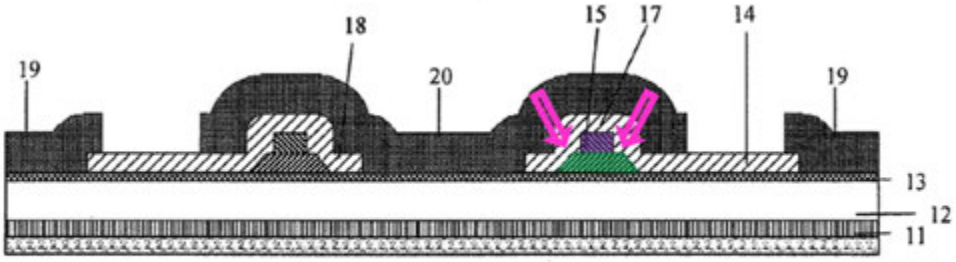


FIG. 10

Lidow, Fig. 10.

The Examiner allowed the claims on the next action, noting the combination of the sloped sidewalls and ledges as the reason for allowance. Ex. 1002, 23-30.

IV. Statement of Precise Relief Requested

A. Prior Art

Yoshida (Ex. 1005, Ex. 1006), which published September 24, 1999, is prior art under pre-AIA 35 U.S.C. § 102(b).
Saxler (Ex. 1007), which published May 25, 2006, is prior art under pre-AIA 35 U.S.C. § 102(b).
Beach (Ex. 1008), which published January 11, 2007, is prior art under pre-AIA 35 U.S.C. § 102(b).
Shenoy (Ex. 1009), which published February 22, 1996, is prior art under pre-AIA 35 U.S.C. § 102(b).
Ahn (Ex. 1010), which issued May 18, 1999, is prior art under pre-AIA 35 U.S.C. § 102(b).

B. Challenges

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103	*Saxler*, *Beach*, and *Shenoy*
2	1-3	§ 103	*Saxler*, *Yoshida*, *Beach*, and *Shenoy*
3	1-3	§ 103	*Saxler* and *Ahn*
4	1-3	§ 103	*Yoshida*, *Saxler*, *Beach*, and *Shenoy*
5	1-3	§ 103	*Yoshida* and *Ahn*

V. Statement of Facts

Pursuant to 37 C.F.R. § 42.22(c), the following statement of facts set forth the state of enchantment mode GaN transistors at the time of the '347 patent's earliest claimed priority date of April 8, 2009.

1. Before April 8, 2009, the following were known:
    a. forming a GaN layer;
    b. forming a barrier layer on the GaN layer;
    c. depositing source and drain contacts on the barrier layer;
    d. depositing a p-type gate material on the barrier layer;
    e. depositing a gate metal on the p-type gate material;
    f. forming a photoresist over the gate metal;
    g. etching the gate metal, and;
    h. etching the p-type gate material to form side surfaces that slope towards the source and drain contacts.
2. Before April 8, 2009, the following were known :
    a. 1.a.-1.g (above);
    b. etching the p-type gate material; and
    c. including a pair of ledges on the p-type gate material below the gate metal.
3. Before April 8, 2009, self-aligned gate structures were known.

VI. Level of Ordinary Skill

A person of ordinary skill in the art ("POSITA") with respect to the '347 patent would have possessed at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design and/or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Shealy, [052]-[053]. Additional education could substitute for professional experience and vice versa. *Id.*

A. Claim Construction

The Board construes claims using the standard of *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b); *CUPP Comput. AS v. Trend Micro Inc.*, 53 F.4th 1376, 1380 (Fed. Cir. 2022). Under this standard, claim terms receive their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the specification, prosecution history, and extrinsic evidence. *Phillips*, 415 F.3d at 1314-19. Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.,* 868 F.3d 1013, 1017 (Fed. Cir. 2017).

B. "forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer" [claim 1]

In a related matter, the parties proposed:

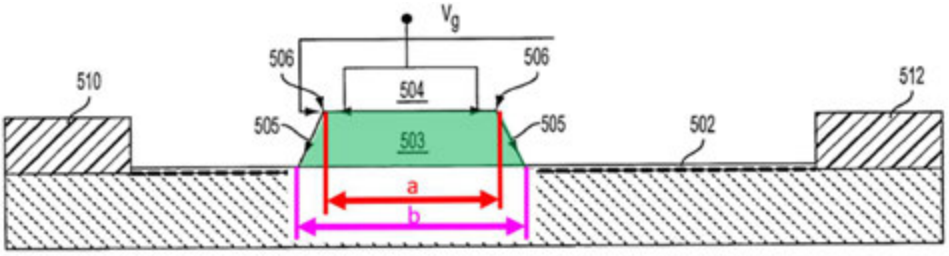
Petitioners'	**Patent Owner's**
"forming side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer"	"forming side surfaces of the p-type gate semiconductor material *such that the bottom of the material*, which contacts the barrier layer, *is wider than the top of the material*"

Ex. 1028.

The challenged claims are unpatentable under both constructions because a 10% slope will be wider on the bottom than the top, so this term need not be construed. But to the extent the Board construes the term, Petitioners' proposed construction should apply, because the prior application, *Lidow*, describes the 10% wider base to enable the leakage protection function of this element. §III.B; Shealy, [070]-[074]. *Lidow* specifically teaches that a "base that is more than 10% wider than the top" advantageously "causes a longer path for electrons to travel between the gate metal 17 and the 2DEG along the pGaN side wall," thereby "result[ing] in lower gate leakage." *Lidow*, [0042].

The construction thus enables the purpose of the element—reducing gate leakage, including through the conventional method of sloping the sidewalls to increase the length of sidewall leakage path 201. Ex. 1001, Abstract, 1:19-23, 2:15-43, 3:60-4:7, 4:34-45, Figs. 2, 4, 7A-7B, 8; Shealy, [073]. *Honeywell Int'l Inc. v. Univ. Avionics Sys. Corp.*, 488 F.3d 982, 990 (Fed. Cir. 2007) (construing claim to be consistent with the "purpose of" the limitation); *KEYnetik, Inc. v. Samsung Elecs. Co., Ltd.*, 837 F. App'x 786, 793 (Fed. Cir. 2020) (reversing Board construction that would "eviscerate[] the purpose of the invention").

The construction likewise accords with the specification, which only shows sloped side surfaces whose bottom surface is more than 10% wider than the top (approximately 30% wider). Ex. 1001, Figs. 5, 6C, 7B; Shealy, [073].



Ex. 1001, Fig. 5.

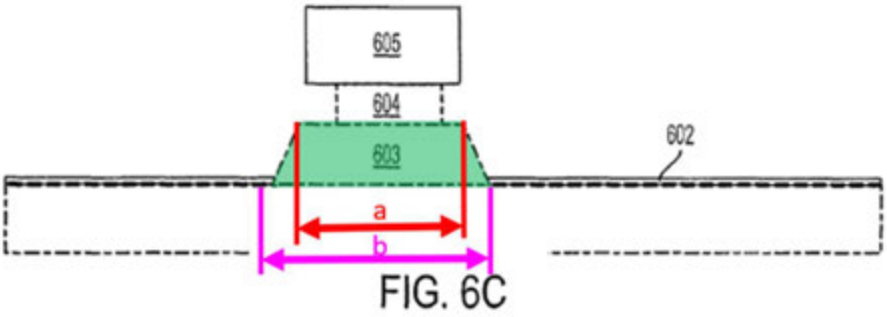


FIG. 6C

Ex. 1001, Fig. 6C.

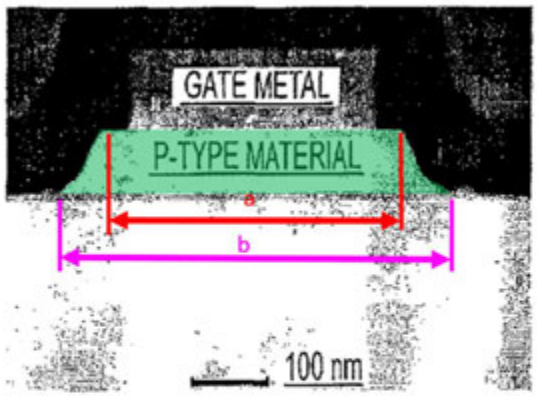


FIG. 7B

Ex. 1001, Fig. 7B

All combinations meet Petitioner's construction. Shealy, [074]. If Patent Owner's broader construction is accepted, the patent is also unpatentable under all grounds and further unpatentable under Grounds 4-5 because *Yoshida* alone renders obvious sloped sidewalls. *Id.*

C. "etching the gate metal and the p-type gate material" [claim 1]

In a related matter, parties proposed:

Petitioners'	Patent Owner's
"*using the photoresist to* etch the gate metal and the p-type gate material"	"Etching the gate metal *and etching* the p-type gate material."

The challenged claims are unpatentable under both constructions because both materials will be etched under either construction. The Board need not construe this term.

D. "etching the gate metal to form a pair of ledges" [claim 1]

In a related matter, the parties proposed:

Petitioners'	Patent Owner's
"*after the etching of the gate metal and the p-type gate material*, etching the gate metal to form a pair of ledges"	"*Performing a process during which gate metal is removed and two ledges are created*."

The challenged claims are unpatentable under both constructions because the process of etching the metal a second time to form ledges removes gate metal. The Board need not construe this term.

VII. Ground 1: *Saxler* in View of *Beach* and *Shenoy* Renders Obvious Claims 1-3

A. Overview of Ground 1

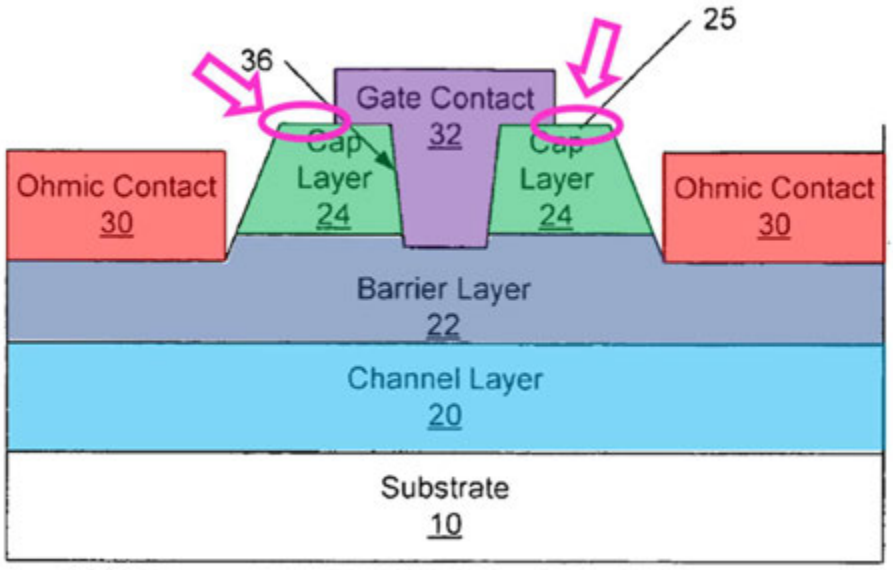
Saxler discloses making its GaN HEMT using a sequence of steps, and its device includes every feature of devices according to the method of the '347 patent's claims, including ledges and sloped sidewalls. *Saxler* masks and etches the p-type gate material and gate metal to form the gate structure. Although not explicitly disclosed, a POSITA would have understood that *Saxler* uses a photomask to etch the gate because *Saxler* requires precise positioning achievable using this conventional approach. Further, a POSITA would have found it obvious modify *Saxler*'s methods with *Beach*'s techniques of self-aligning the p-type gate material and gate metal and *Shenoy*'s approach to isotropically etch the gate metal using a single mask, resulting in the *Saxler*'s same gate structure.

1. *Saxler*

Saxler discloses making a GaN transistor with high breakdown voltage by:

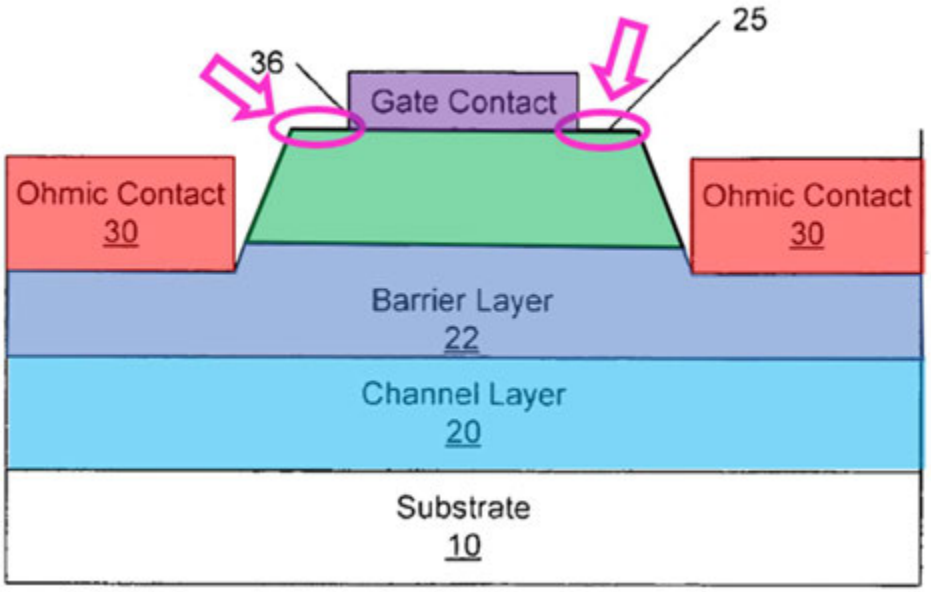
1. Forming the **channel layer**, **barrier layer**, and **cap layer.**
2. Masking and etching the **cap layer** to expose the **barrier layer**, creating sloped sidewalls.
3. Depositing the **source and drain contacts.**
4. Forming a **gate contact**.

Saxler, [0057]-[0066]; Shealy, [080].



Saxler, Fig. 1A.

Saxler's gate contact may be recessed or non-recessed (i.e., flat). *Saxler*, [0052], [0066]. Where the gate recess is not utilized, *Saxler* would result in the following structure. Shealy, [081].



Saxler, Fig. 1A (modified).

Saxler's **channel layer 20** is GaN over silicon, and *Saxler*'s **barrier layer 22** is a Group III-nitride such as AlGaN. *Saxler*, [0057]-[0060]; Shealy, [082]. The stacked gate structure above the **barrier layer 22** consists of a **cap layer** and metallic **gate contact**. *Saxler*, [0061]-[0063], [0066], [0071]-[0073], [0076], [0087]; Shealy, [082]. The **cap** layer may include p-type GaN, doped in a subregion or throughout. *Saxler*, [0013], [0069], [0071], [0073]; Shealy, [082].

Sheppard, incorporated by *Saxler* to provide methods of fabricating *Saxler*'s GaN HEMTs (*Saxler*, [0046], [0068]), describes a similar process. *Sheppard*, [0044]-[0051], Figs. 1A-1F; Shealy, [083]. This effectively makes *Sheppard* part of *Saxler*'s disclosure. *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906 (Fed. Cir. 2018) ("Incorporation by reference provides 'a method for integrating material from various documents into a host document[] . . . by citing such material in a manner that makes clear that the material is effectively part of the host document as if it were explicitly contained therein.'" (alteration in original) (quoting *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000)).

Saxler also incorporates *Smith* by reference to disclose methods of making gate structures. *Saxler*, [0087]. *Smith* explicitly discloses using "conventional photolithographic techniques and mask alignment tools" to precisely position the gate contact close to or flush with the cap layer using a single mask, including a non-"self-aligned" technique and a "self-aligned" technique. *Smith*, [0041]-[0044],

Fig. 4A-4C, 5A-5B, 6A-6C, claim 25; Shealy, [084]. *Smith* is therefore also part of *Saxler*. *Paice,* 881 F.3d at 906.

Smith discloses non-recessed gate electrodes in stacked structures similar to *Saxler*'s recessed stacked gate structure. *Smith*, [0033], [0041], Figs. 3, 5B. It identifies that "there is no benefit to recessing the gate down to the barrier layer" in GaN HEMT devices. *Smith*, [0010]; Shealy, [085]. And although it briefly discloses using T-shaped gate electrodes for "microwave and RF" applications (*Smith*, [0017], [0034], claim 20), *Smith* otherwise only describes and depicts stacked gate structures having a **GaN cap layer** with a non-recessed **gate electrode** (*Smith*, [0033]-[0037], [0039]-[0043], claim 1, Figs. 3, 4A-4C, 5A-5B); Shealy, [085]. Like *Saxler*, *Smith*'s GaN HEMT also includes a **GaN channel layer**, **AlGaN barrier layer**, and **source** and **drain electrodes**. *Smith*, [0030]-[0037], [0041]; Shealy, [085]. A POSITA would thus have understood non-recessed electrodes were a suitable option for *Saxler*'s cap. Shealy, [085].

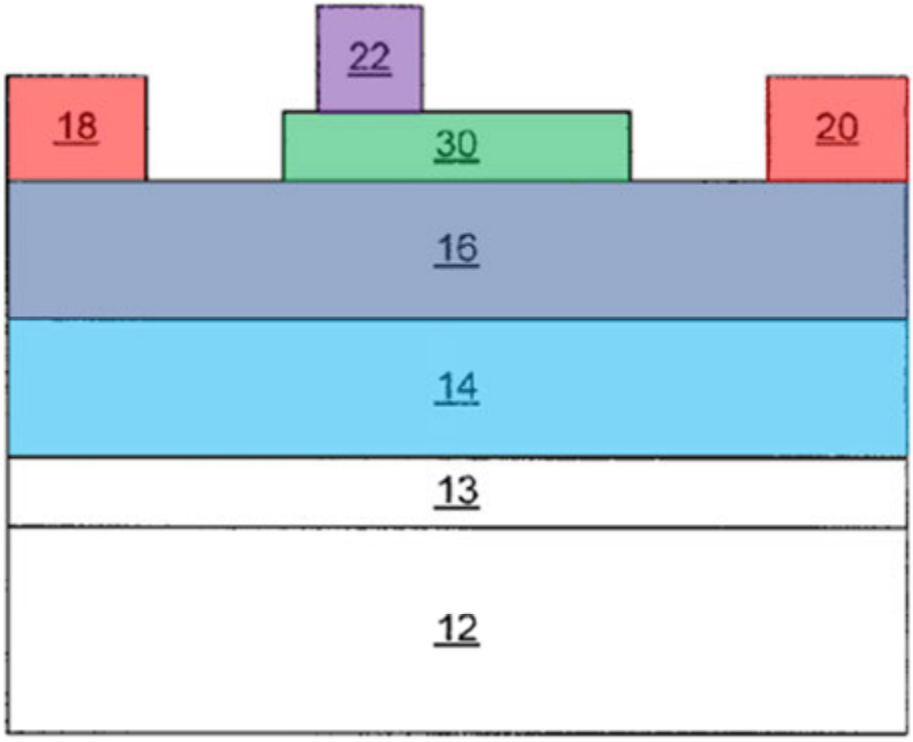


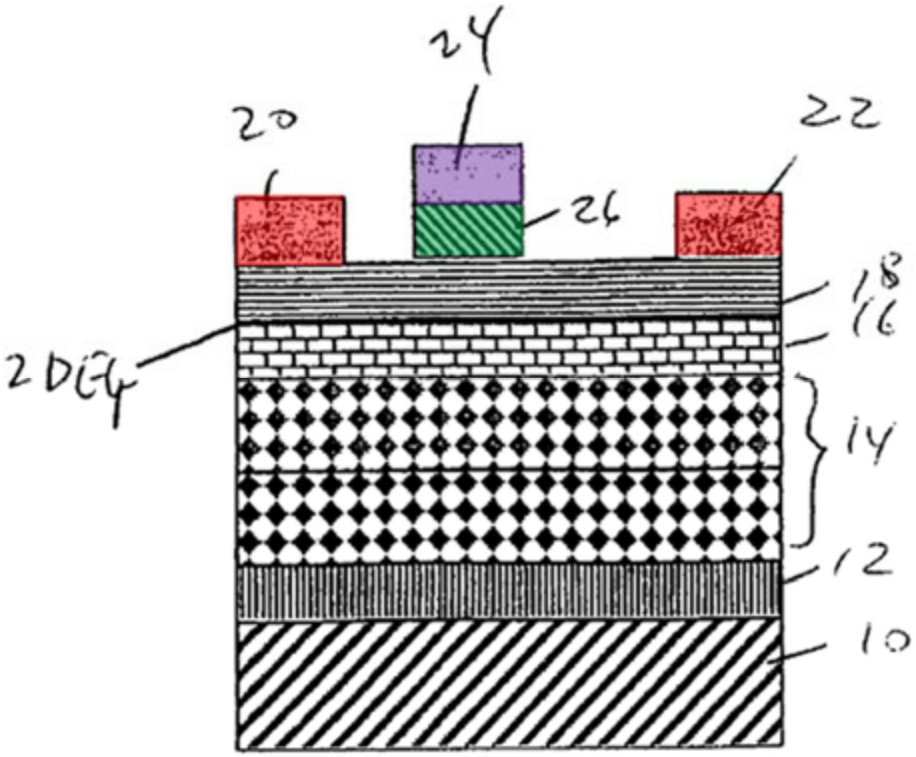
Figure 5B

Smith, Fig. 5B.

2. Beach

Beach discloses GaN enhancement-mode devices. *Beach*, Abstract, [0003]-[0018]. *Beach* teaches a self-aligned method of making stacked gate structures using a single mask. *Beach*, [0040], [0045], [0054]; Shealy, [086]. *Beach* discloses "self-aligned" gates made using steps to deposit and pattern layers with a single mask to arrive at **gate barrier 26** and **gate arrangement 24** above a p-n junction and between **power electrodes**, as shown below. *Beach*, [0040], [0045]; Shealy, [086]. A POSITA would have understood *Beach*'s "self-aligned" techniques used a single

photomask, as described in another Beach publication. *Beach-II*, [0047]-[0048], Figs. 1D-1E; Shealy, [086]. Such self-aligned techniques were common in the field at the time. Shealy, [086]. *Beach*'s "gate arrangement 24" includes a **gate electrode**, and **gate barrier 26** is a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Shealy, [086].



Beach, Fig. 1.

3. *Shenoy*

Shenoy discloses isotropic etching to undercut metal below photoresists. *Shenoy*, 2-3; Shealy, [087]-[088]. Its controls "**undercut U**" (Figure 1), to evolve symmetrically such that the etched metal is narrower than the photomask. *Shenoy*, 2-3; Shealy, [087]. *Shenoy*'s methods were conventional for etching metals in semi-

conductors as of the relevant date of the '347 patent. Shealy, [087] (citing *Shenoy* and noting it published "over a decade" before the claimed priority date).

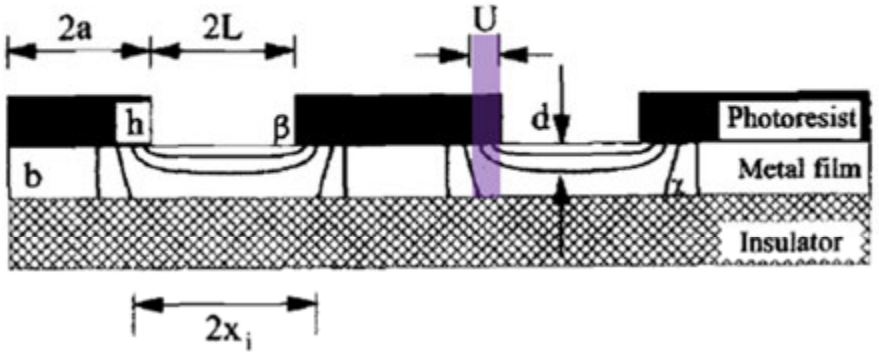


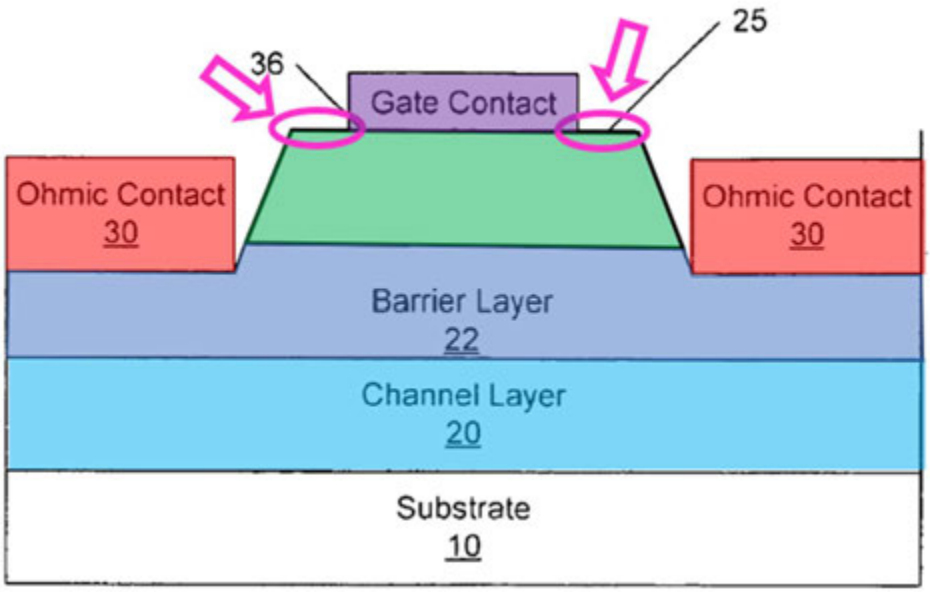
Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

Shenoy, Fig. 1.

At least as of April 8, 2009, and as early as its publication date of February 22, 1996, *Shenoy* was publicly available and disseminated. *Shenoy*, 1; Ex. 1025, ¶¶16-26 (Declaration of Kelley Hazel); Shealy, [088]. A POSITA designing GaN transistors routinely accessed similar scholarly articles and would have looked to *Shenoy* for its metal etching techniques. Shealy, [088].

4. Combination of *Saxler*, *Beach*, and *Shenoy*

The combination would yield the same structure as the non-recessed *Saxler* embodiment. Shealy, [089].



Saxler, Fig. 1A (modified).

5. Motivation to Combine

A POSITA would have found it obvious to make the stacked gate structure of *Saxler*'s non-recessed embodiments using *Beach*'s and *Shenoy*'s methods. Shealy, [090]-[098].

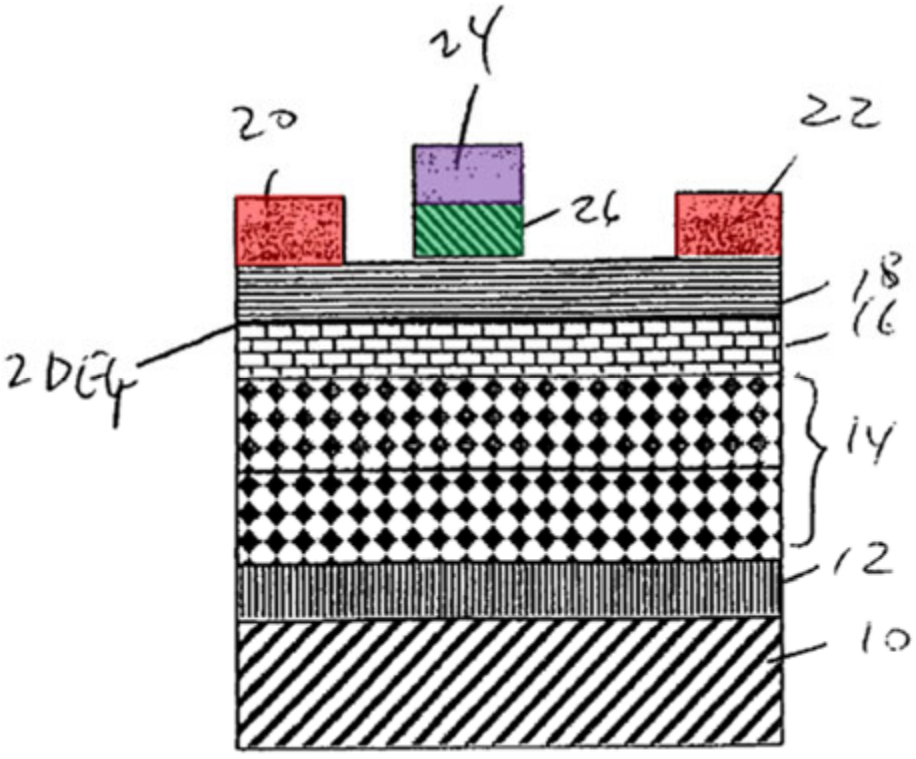
As explained above, *Saxler* makes its stacked gate structure by masking and etching the cap layer, removing the mask, then depositing the gate contact. *Saxler*, [0064]-[0066], Figs. 1A-1B; §VII.A.1; Shealy, [091]. A POSITA would have understood a second mask would be used to deposit the gate contact, then removed, because *Saxler* uses two masks in its recessed embodiments, which is also *Smith*'s non "self-aligned" approach (incorporated by reference to disclose methods of

making gate structures (*Saxler* [0046], [0068], [0087])). §§VII.B.8, VII.B.10; Shealy, [0091] (citing *Smith*, [0041], Figs. 4A-4C; *Saxler*, [0065]-[0066]).

A POSITA would have been motivated to simplify this process and reduce costs by using fewer masking steps. *Id. Smith* teaches a "self-aligned" approach that does not include a pair of horizontal ledges, and a POSITA would have been motivated to look for methods of using that self-aligned approach to precisely make symmetric ledges. *Smith*, [0042]; Shealy, [0092].

A POSITA would have known many ways to create *Saxler*'s stepped gate structure in its non-recessed embodiments and would have used them interchangeably. §II; Shealy, [060]-[062] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*, Ex. 1023), [0092] (citing *Smith*, [0042]). It would have been obvious to modify *Saxler* with *Beach*'s self-aligned technique and *Shenoy*'s isotropic etching to arrive at that same non-recessed gate structure, which would reduce steps and costs while improving reproducibility and symmetry of the gate structure layers. Shealy, [93]. A POSITA would have recognized this as a simple and predictable combination in light of *Smith*'s self-alignment techniques to create its stacked gate structure, which has one flush sidewall between cap layer and gate contact. *Smith*, [0041]-[0044], Figs. 4A-4C, 5A-5C, 6A-6C; Shealy, [93]. *Ahn* discloses this same approach for making a stepped gate in a thin-film transistor. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C; Shealy, [093].

Beach's method of uses a single mask ensures alignment of layers. *Beach*, [0040], [0045], [0054]; Shealy, [094]. *Beach*'s gate structure includes the "gate arrangement 24," which comprises a gate electrode, and an underlying "gate barrier 26," a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Shealy, [094]. *Beach*'s process (i) deposits "**gate barrier 26**" and "**gate arrangement 24**" layers, (ii) patterns the stack with a mask, (iii) etches to obtain the stack, and (iv) deposits **power electrodes**. *Beach*, [0040]; Shealy, [094]. This approach used a single photomask. Shealy, [094] (citing *Beach-II*, [0047]-[0048]). Such self-aligned techniques were common. *Id.*



Beach, Fig. 1.

It would have been obvious to create *Saxler*'s gate structure with *Beach*'s approach for improved alignment between layers. Shealy, [0095] (*citing Beach*, [0040], Fig. 1; *Shenoy*, 2-3). It would have been obvious to look to *Beach* for its simple methods of making stacked gate structures. *Id. Sheppard*, incorporated to disclose methods of fabricating GaN HEMTs (*Saxler*, [0046], [0068]), describes a flexible approach to masking and etching. It notes that "operations described as multiple steps could be combined into a single step" (and vice versa), making the choice of *Beach*'s manufacturing steps no more than simple substitutions. *Sheppard*, [0058]; Shealy, [095].

While *Beach* does not create the **horizontal ledges** of *Saxler*, *Shenoy* does. As previously explained, *Shenoy* discloses simple isotropic etching techniques for symmetrically undercutting metal layers below photoresists. *Shenoy*, 2-3; Shealy, [096]; §VII.A.3.

Thus, an ordinary artisan would have found it obvious to use *Beach*'s self-aligned method and *Shenoy*'s methods to undercut the **gate electrode** to create *Saxler*'s **horizontal ledges**. Shealy, [097]. That combination of steps was already known for creating stepped, stacked transistor gates. *Id.* (citing *Ahn*). A POSITA would have found the combination a simple substitution of *Beach*'s and *Shenoy*'s known methods that would be predictably implemented in *Saxler*'s flexible method

of manufacturing to improve alignment and symmetry between layers and reduce steps and costs. *Id.* (citing *Saxler*, [0046], [0068]; *Sheppard*, [0058]).

It would have been simple and predictable to use *Beach*'s and *Shenoy*'s known techniques, which were among the many ways to obtain *Yoshida-Saxler*'s gate structure. Shealy, [098]. The '347 patent was allowed without disclosing any particular method to etch the gate metal and obtain the claimed ledges because such methods were well within a POSITA's ability. Shealy, [057]-[063], [098]; Ex. 1002, 25-30, 44-55, 74-76, 80-99; §§II, III.B. For example, lift-off and isotropic etching were well within the level of ordinary skill. §II; Shealy, [057]-[063], [098]. As a reason for allowance, the Examiner identified that the cited art did not disclose forming sloped sidewalls of its p-type gate material in structures that also had ledges. Ex. 1002, 29, 55. But *Saxler* discloses such sloped sidewalls with the claimed ledges, and *Beach* and *Shenoy* would have provided a known, obvious way to create that structure. §§VII.A.1, VII.A.4-VII.A.5; Shealy, [098].

B. Independent Claim 1

1. [1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

To the extent it is limiting, *Saxler* discloses or at least renders obvious the preamble. Shealy, [099]-[100]. *Saxler* discloses a GaN high-mobility transistor that includes a p-type doped GaN cap layer below the gate and above an AlGaN barrier layer. *Saxler*, [0007]-[0010], [0013], [0046], [0059]-[0064], Figs. 1A, 1B; Shealy,

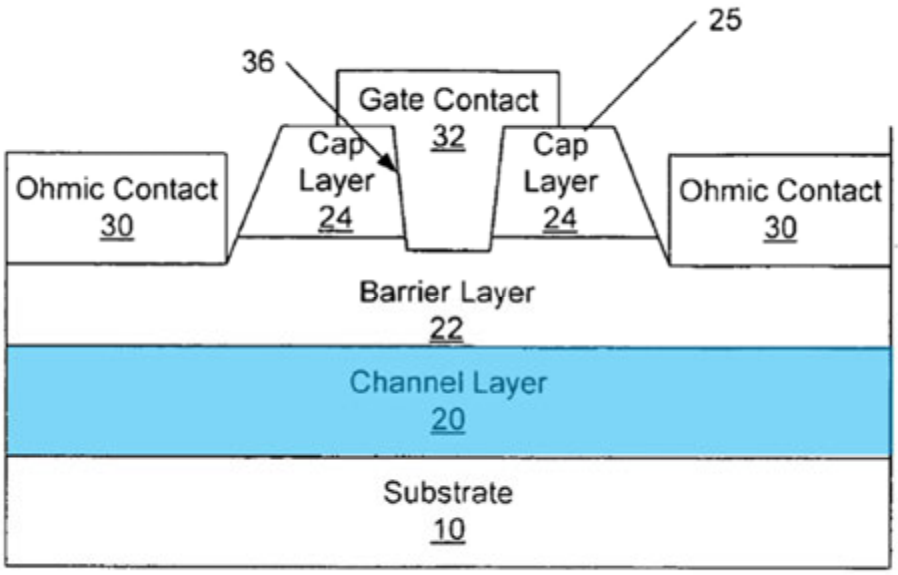
[099]. This constitutes a normally off enhancement-mode GaN transistor. Shealy, [099]. *Saxler* discloses methods for making this transistor. Saxler, [0053]-[0066], Figs. 1A-1B.

A POSITA would have understood that *Saxler*'s transistors were enhancement-mode GaN transistors at least because of their gate structure. Shealy, [100]. For example, *Sheppard*, which *Saxler* expressly incorporates (*Saxler*, [0046], [0068]), likewise discloses a GaN high-mobility transistor that includes a doped GaN cap layer below the gate and above an AlGaN barrier layer, where the cap layer "moves the top surface of the device physically away from the channel, which may reduce the effects of the surface," constituting a normally off enhancement-mode GaN transistor when the cap is doped p-type. *Sheppard*, [0014], [0040], [0042], Fig. 1F; Shealy, [100].

2. [1a] forming a GaN layer;

The '347 patent admits [1a] was conventional. Ex. 1001, 1:37-2:21, Figs. 1-2, 3A-3B; Shealy, [101].

Saxler discloses a **GaN channel layer**. *Saxler*, [0007], [0010], [0016], [0057]-[0058], [0069], Figs. 1A-1F; Shealy, [101]-[102]. It describes methods to form the GaN channel layer. *Saxler*, [0057]; Shealy, [102].

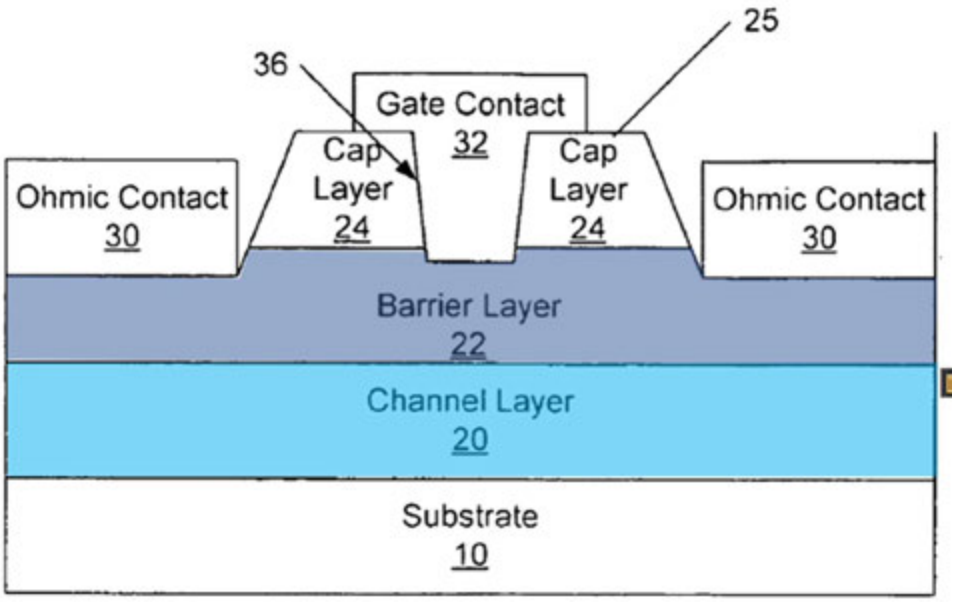


Saxler, Fig. 1A.

3. [1b] forming a barrier layer on the GaN layer;

The '347 patent admits [1b] was conventional. Ex. 1001, 1:27-2:21, Figs. 1-2, 3A-3B; Shealy, [103].

Saxler discloses [1b]. Shealy, [103]-[105]. *Saxler*'s **barrier layer 22** is formed on its GaN **channel layer**. *Saxler*, Abstract, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B.



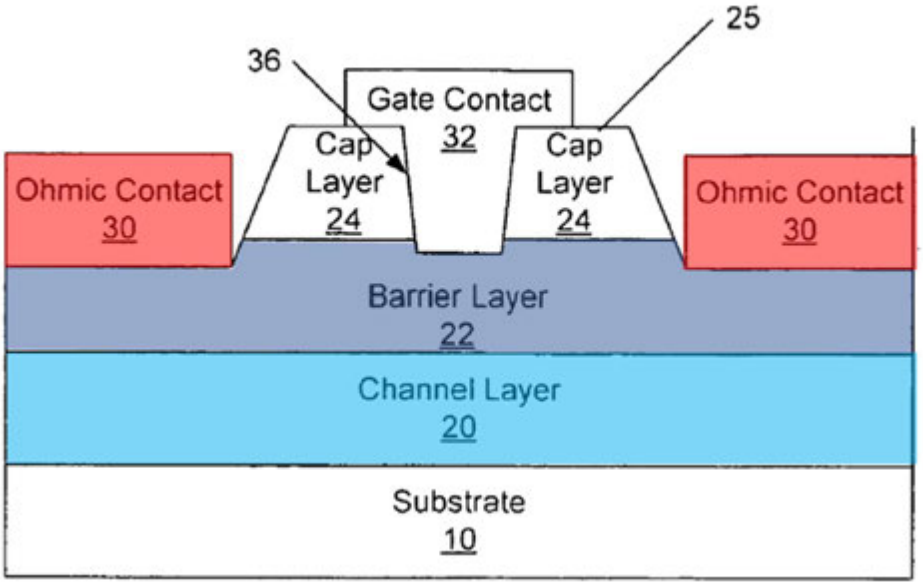
Saxler, Fig. 1A.

Saxler's barrier layer may be an AlGaN layer. *Saxler*, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B; Shealy, [105]. The '347 patent likewise discloses that the claimed barrier layer may be an AlGaN layer. Ex. 1001, 1:37-58, 3:32-43, 4:10-16.

4. [1c]: depositing source and drain contacts on the barrier layer;

The '347 patent admits [1c] was conventional. Ex. 1001, 1:59-2:14, Figs. 1-2, 3A-3B; Shealy, [106].

Saxler discloses "ohmic contacts 30" may be "**source** and **drain contacts**" formed on barrier layer 22. *Saxler*, [0065], Figs. 1A, 2B; Shealy, [106]-[107].

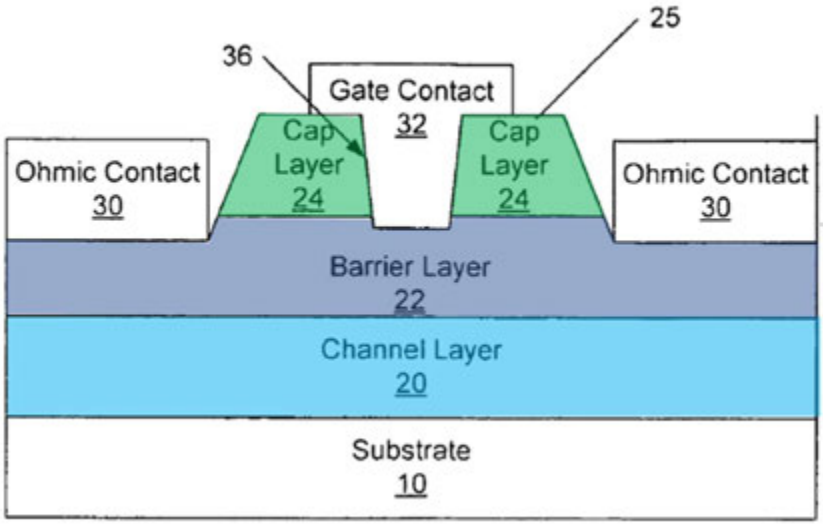


Saxler, Fig. 1A.

5. [1d]: depositing a p-type gate material on the barrier layer,

The patent admits [1d] was conventional. Ex. 1001, 1:37-2:21, Figs. 1-4, 7A; Shealy, [108].

Saxler discloses [1d]. Shealy, [108]-[109]. *Saxler*'s **cap layer** is a p-type gate material on the AlGaN **barrier layer**. *Saxler*, [0010], [0013], [0059]-[0063], [0069], [0071], [0073], Figs. 1A, 2B; Shealy, [109]. The **cap layer** "may be … formed by *deposition*." Saxler, [0061].

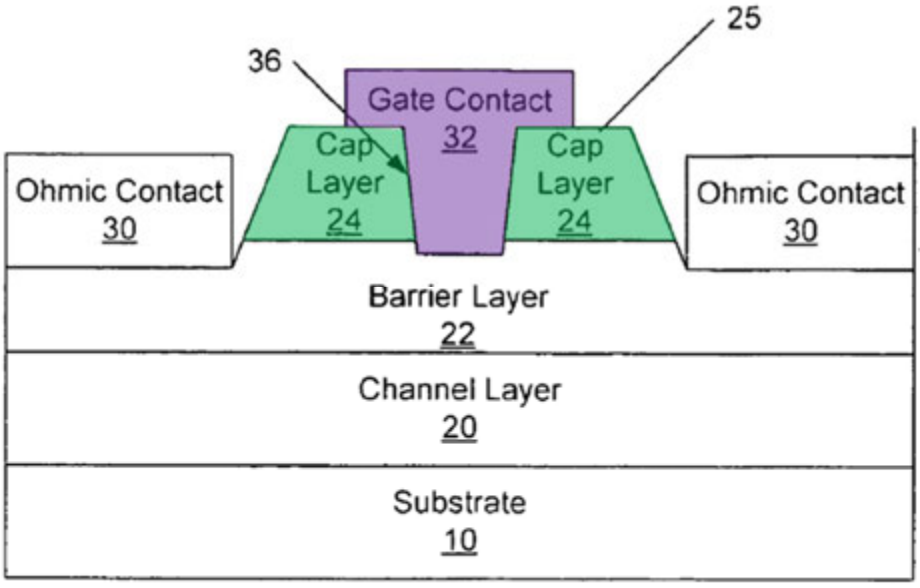


Saxler, Fig. 1A.

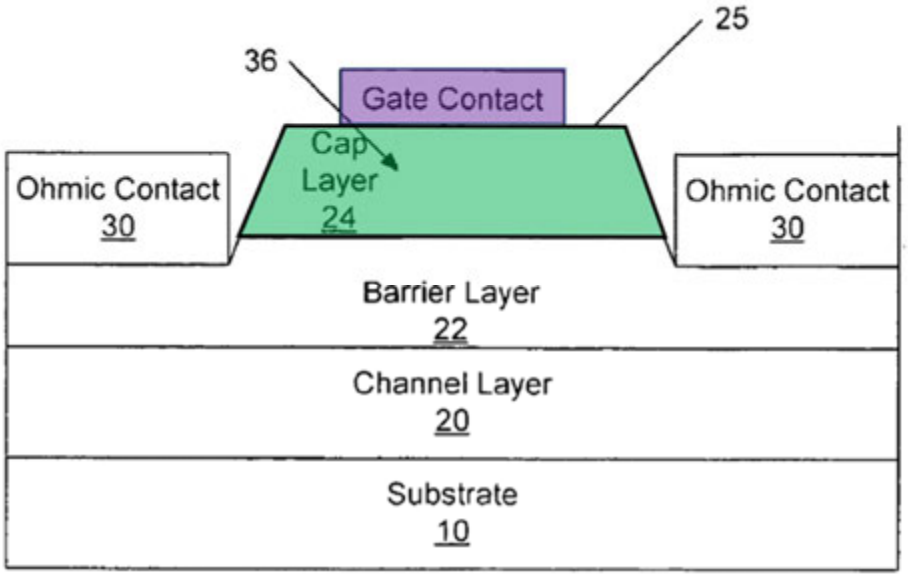
6. [1e]: depositing a gate metal on the p-type gate material;

The patent admits [1e] was conventional. Ex. 1001, 1:24-2:21, Figs. 1-4, 7A; Shealy, [110].

Saxler renders obvious [1e]. Shealy, [110]-[111]. *Saxler*'s **gate contact** is a gate metal (e.g., "Ni, Pt, $NiSi_x$, Cu, Pd, Cr, W and/or WSiN") formed on its **cap layer**. *Saxler*, [0066], Figs. 1A, 2B; Shealy, [111]. As explained, in some embodiments *Saxler* lacks a gate recess and does not separate the **cap layer** into distinct portions. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; §VII.B.9; Shealy, [111].



Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

7. [1f]: forming a photoresist over the gate metal;

Lidow, the prior application, admits [1f] was conventional because ledges in a "conventional enhancement-mode transistor" are made using separate masks for the p-type gate material and gate metal. *Lidow*, [0006], Fig. 1; Shealy, [112].

It would have been obvious to form a photoresist over the gate metal in view of *Saxler*. §VII.A.1; Shealy, [112]-[115]. *Saxler* precisely positions its gate contact on the cap layer. *Saxler*, [0065], Figs. 1A-1B, 2A-2B. A POSITA would have understood conventional masking and etching techniques involving a photoresist over the gate metal would have achieved such precision. §VII.A.1; Shealy, [080]-[085] (citing *Saxler*, *Smith*, *Sheppard*) [113]. This was just one of many known methods for forming stacked, stepped gate structures. §II; Shealy, [060]-[062] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [113]).

Further, *Saxler, Beach* and *Shenoy* also render obvious [1f]. Shealy, [114]-[115]. *Beach* forms a photoresist over the gate metal when "the stack is patterned and etched to obtain gate arrangement 24 over gate barrier 26." *Beach*, [0040]; *Beach-II*, [0047]-[0048]; Shealy, [114]. *Shenoy* also discloses a photoresist over a metal electrode. *Shenoy*, 1.

It would have been obvious to combine *Saxler* with *Beach* and *Shenoy*'s techniques of using a single photomask over *Saxler*'s gate metal when making *Saxler*'s non-recessed device. §VII.A.5; Shealy, [115].

8. [1g]: etching the gate metal and the p-type gate material,

Lidow, the prior application, admits [1g] was conventional under Patent Owner's construction because ledges in a "conventional enhancement-mode transistor" are made using separate masks for the p-type gate material and gate metal, thereby admitting it was known to "etch[] the gate metal and etch the p-type gate material" (Patent Owner's construction). *Lidow*, [0006], Fig. 1; Shealy, [116]; §VI.C.

Saxler discloses or at least renders obvious this limitation under both parties' constructions. §VI.C; Shealy, [117]-[119]. Saxler discloses etching the cap layer "to expose the underlying barrier layer" then placing source and drain contacts. *Saxler*, [0064], Figs. 1A-1B. *Saxler* also discloses or at least renders obvious etching the gate metal using the same photoresist. As explained, a POSITA would have understood depositing *Saxler*'s gate contact would have involved masking and etching the gate metal to precisely position it. §§VII.A.1, VII.B.7; Shealy, [080]-[085], [091] (citing *Smith*, [0041], Figs. 4A-4C; *Saxler*, [0065]-[0066]), [117].

Saxler, Beach and *Shenoy* also render obvious [1g]. Shealy, [118]-[119]. *Beach* uses one mask to etch the gate metal and p-type gate material. *Beach*, [0040]; *Beach-II*, [0047]-[0048], Shealy, [118]. *Shenoy* discloses the same. *Shenoy*, 1.

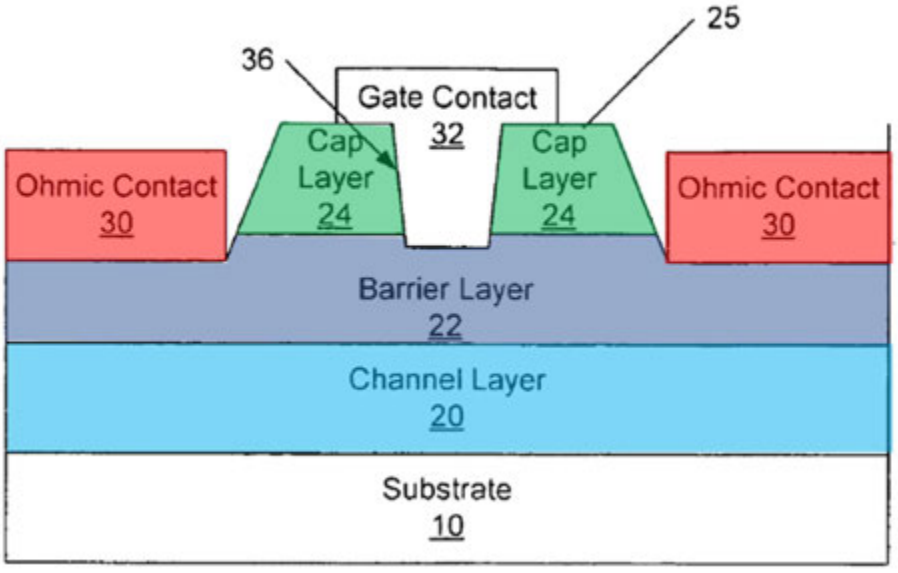
It would have been obvious to combine *Saxler* with *Beach* and *Shenoy*'s techniques of masking and etching the gate metal and p-type gate material using a

single photomask when making *Saxler*'s non-recessed GaN HEMT device. §VII.A.5; Shealy, [119].

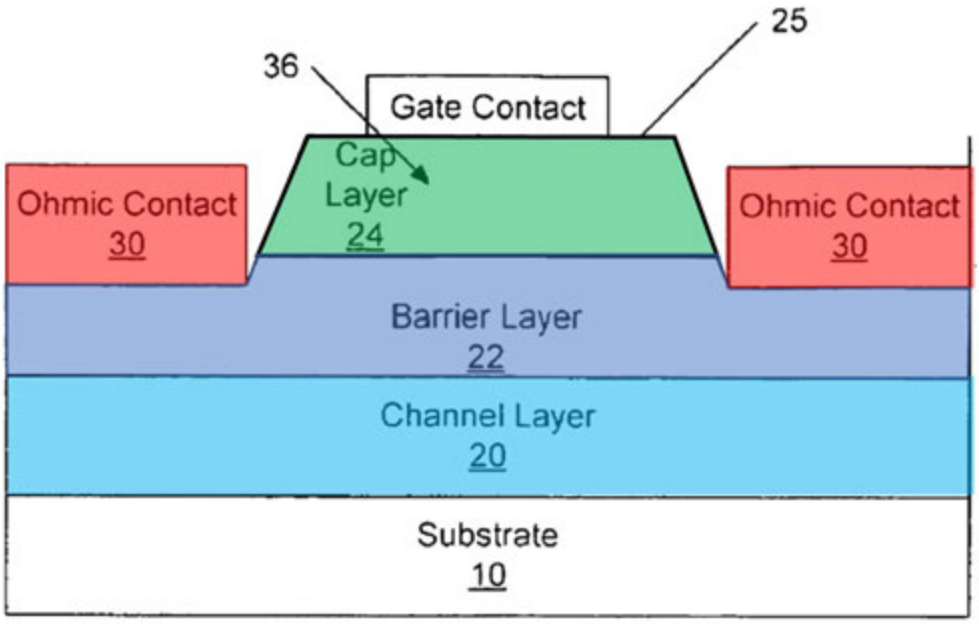
9. [1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

The '347 patent admits [1h] was conventional. Ex. 1001, 1:37-2:21, Figs. 1-2, 3A-3B; Shealy, [120].

Saxler discloses [1h]. Shealy, [120]-[123]. *Saxler* etches the **cap layer** "to expose the underlying **barrier layer**" and place the source and drain contacts. *Saxler*, [0064], Figs. 1A-1B; Shealy, [120]. The sidewalls of the **cap layer** extend horizontally towards **source** and **drain contacts** and contact the **barrier layer** in both recessed and non-recessed embodiments. Shealy, [120].



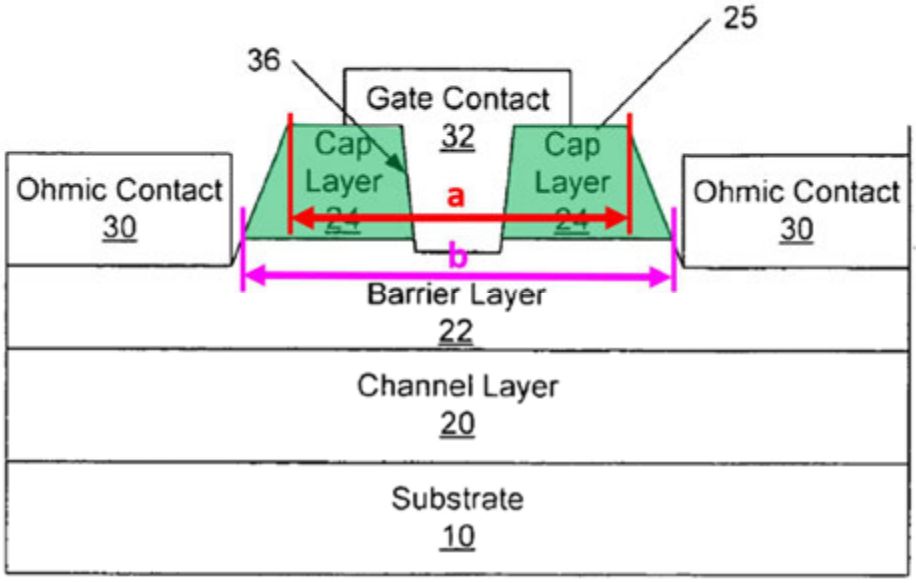
Saxler, Fig. 1A.



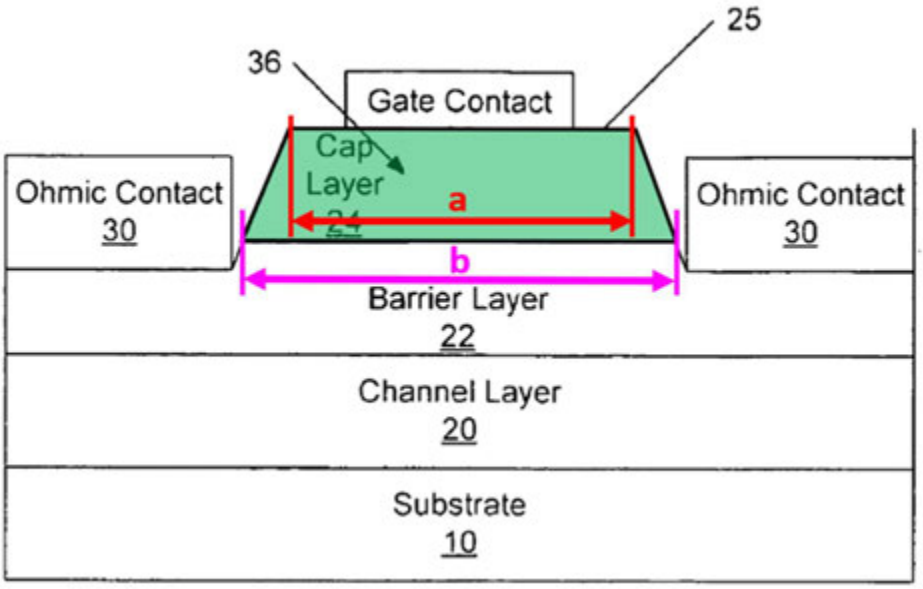
Saxler, Fig. 1A (modified).

Saxler discloses "side surface**s** of ***the*** p-type gate material." Although it depicts its gate recess may separate its cap layer into two portions in some embodiments, the recess in *Saxler*'s cap layer 24 is optional, and where not employed the cap is a continuous material. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; Shealy, [121].

Saxler also discloses both parties' construction of the side surfaces limitation. *Saxler*, [0064], Figs. 1A, 2B; §VI.B; Shealy, [123]. In either its recessed or non-recessed embodiments, the bottom of the **cap layer** (length "**b**," below) is more than 10% wider than the top (length "**a**"). Shealy, [123].



Saxler, Fig. 1A.

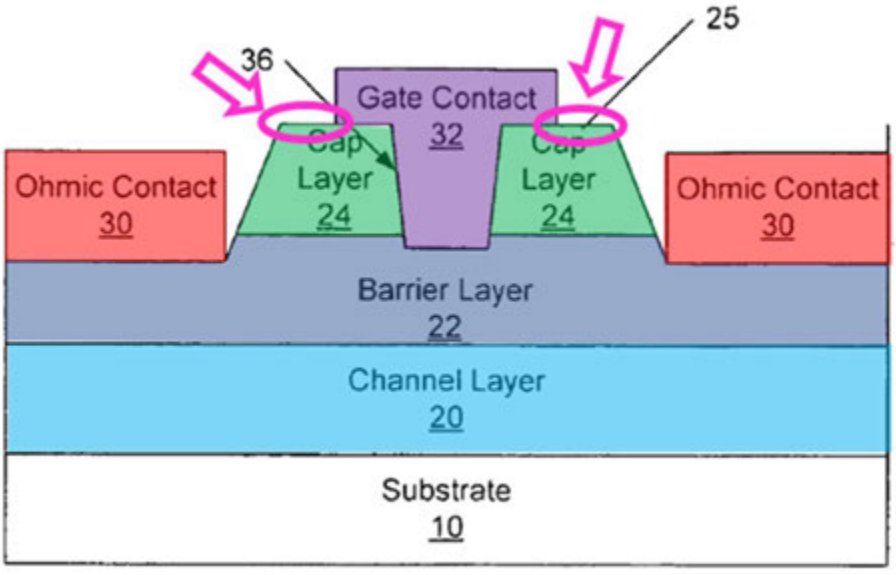


Saxler, Fig. 1A (modified).

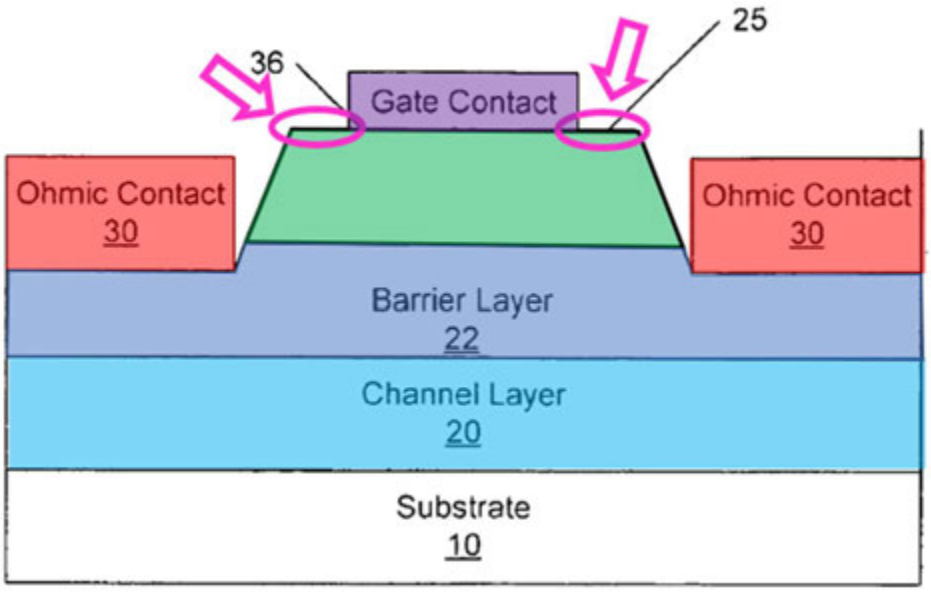
10. [1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

[1i] is the only feature of independent claim 1 that the '347 patent does not acknowledge is found in the prior art. Ex. 1001, 1:19-2:21, Figs. 1-4, 7A; Shealy, [124]. Yet under Patent Owner's construction (§VI.C), *Lidow,* the prior application, notes this approach was conventional, stating that ledges in a "conventional enhancement-mode transistor" are made using separate masks for the p-type gate material and gate metal. *Lidow*, [0006], Fig. 1; Shealy, [124].

Saxler, Beach and *Shenoy* render [1i] obvious under either construction. Shealy, [124]-[127]. *Saxler* depicts its **gate contact** is narrower than its **cap layer**, thereby exposing **horizontal ledges** on the **cap layer**. *Saxler*, Fig. 1F. Shealy, [125]. *Saxler*'s non-recessed embodiments include these same features. §VII.A.1; Shealy, [080]-[085], [125].



Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

Saxler renders obvious making these **ledges** by etching the gate metal. Shealy, [126]. As explained, a POSITA would have found it obvious use one mask to etch the gate metal and cap layer to precisely place the gate and reduce manufacturing steps and costs. §§VII.A.1, VII.B.7-VII.B.8; Shealy, [126].

Further, *Saxler, Beach* and *Shenoy* render obvious [1f]. *Shenoy* discloses methods of isotropically etching the gate metal to form symmetric undercuts of a photomask. *Shenoy*, 1-2; §VII.A.3; Shealy, [127]. This technique, applied to the mask of *Beach*, would have generated the pair of **ledges** on *Saxler*'s cap layer. Shealy, [127]. In light of the many known ways to generate *Saxler*'s ledges, it would

have been obvious to use *Beach*'s and *Shenoy*'s methods to build *Saxler*'s structure. §VII.A.5; Shealy, [057]-[063], [127].

C. [Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.

Claim 2 recites nothing more than that the gate metal is narrower than the p-type gate material, which is already required to form the **ledges** of [1i]. *Saxler*, [0014], [0046], claims 1, 18, 20, 29, Fig. 1F; Shealy, [128]. As explained for [1i], *Saxler, Beach* and *Shenoy* render obvious the features of claim 2. §VII.B.10; Shealy, [128].

D. [Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.

The combination of *Saxler*, *Beach*, and *Shenoy* renders obvious Claim 3. Shealy, [129]-[132].

Beach discloses a stacked "***self-aligned*** gate arrangement" using a single photomask to etch both the "gate arrangement 24" (gate electrode) and the underlying "gate barrier 26" (GaN semiconductor) that is the same "self-aligned" process depicted in the '347 patent at Figures 6A-6B. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Ex. 1001, 4:8-20; §§III.A.1, VII.A.2, VII.A.5; Shealy, [130].

Shenoy discloses etching a photomask to isotropically undercut the metal layer below the photomask that is the same process depicted in Figures 6B-6C of the

'347 patent. *Shenoy*, 2-3; Ex. 1001, 4:17-33; §§III.A.1, VII.A.3, VII.A.5; Shealy, [130].

It would have been obvious to use *Beach*'s self-alignment method and *Shenoy*'s undercutting techniques to predictably make *Saxler*'s gate structure, improving alignment. §VII.A.5; Shealy, [131].

VIII. Ground 2: *Saxler* in view of *Yoshida*, *Beach*, and *Shenoy*

A. Overview of Ground 2

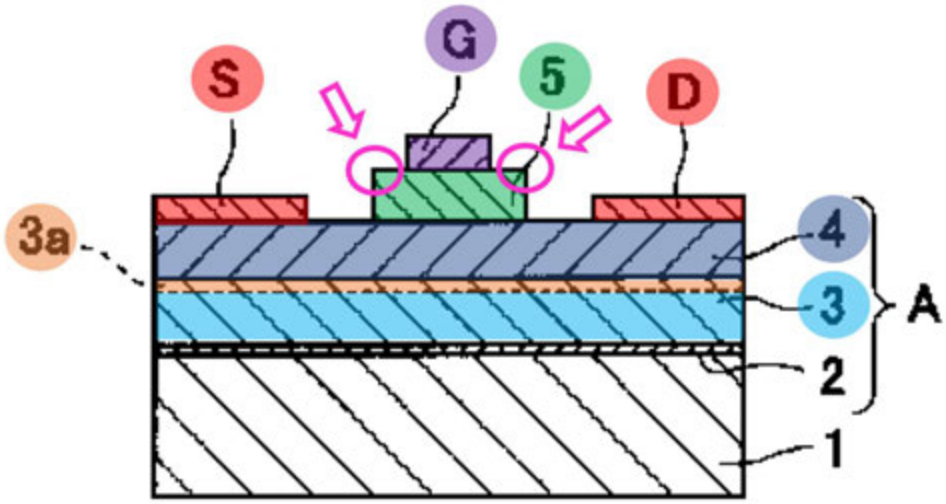
Saxler's recessed gate is optional. However, *Yoshida* also discloses and depicts a similar device having a p-type gate material without a gate recess, further rendering this modification obvious.

1. *Yoshida*

Yoshida discloses a normally-off enhancement-mode GaN transistor having a p-type GaN layer below the gate that "enables voltage control with a small amount of carrier injection." *Yoshida*, [0017], [0015], Fig. 1; Shealy, [134]. *Yoshida* declares it improves breakdown voltages over prior art GaN transistors. *Yoshida*, [0008]-[0009]; Shealy, [134].

As shown below, *Yoshida*'s **layer 3** is a GaN grown over silicon nitrate like *Saxler*'s channel layer, and **layer 4** is an n-type semiconductor, with **2DEG 3a** forming at their interface. *Yoshida*, Abstract, [0010], [0013], [0019]; Shealy, [135]. *Yoshida* includes a **source** and **drain** contact. *Yoshida*, Abstract, [0009].

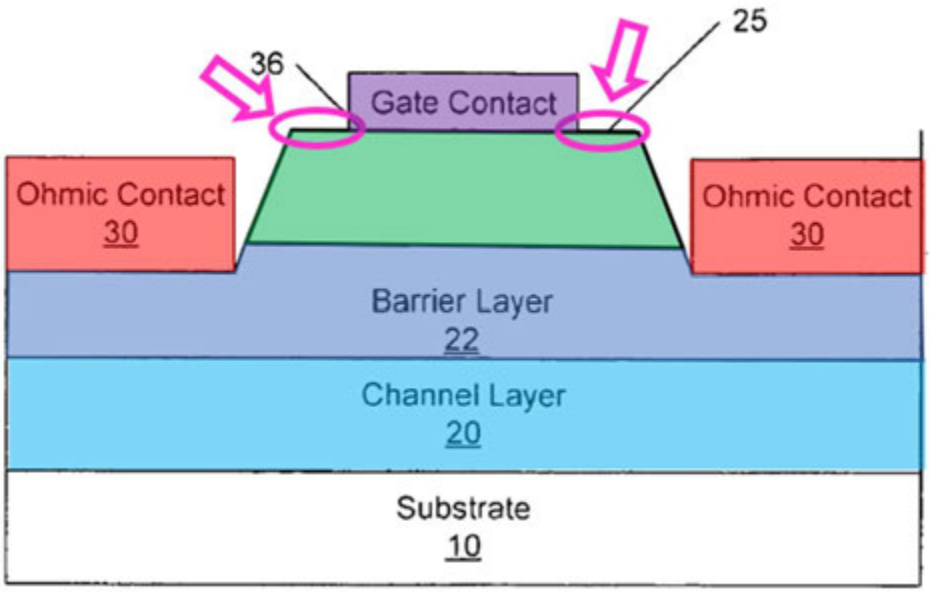
Yoshida also discloses a stacked gate structure consisting of a **doped GaN layer** above the **semiconductor layer 4** and an overlying **gate metal**. *Yoshida*, Abstract, [0015]; Shealy, [136]. Its gate structure includes a pair of **horizontal ledges** on either side of the gate metal. *Yoshida*, Fig. 1; Shealy, [136].



Yoshida, Fig. 1.

2. The Combination of *Saxler* in View of *Yoshida*

Implementing *Yoshida*'s non-recessed gate in *Saxler*'s stacked gate structure results in the following combined structure, which is the same arrangement as *Saxler*'s non-recessed embodiment. Shealy, [137].



Saxler, Fig. 1A (modified).

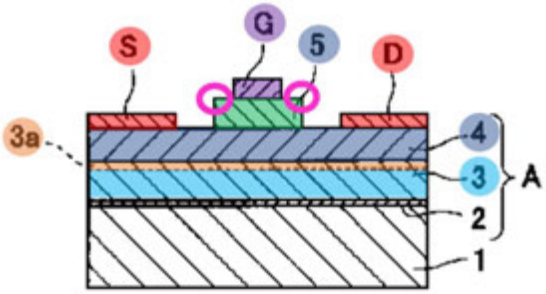
In the combination, *Beach* and *Shenoy* would be used to form *Saxler*-*Yoshida*'s gate structure. Shealy, [138].

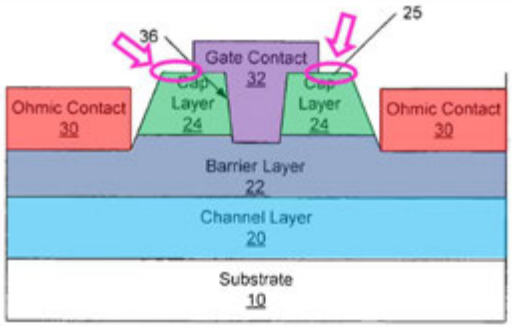
3. Motivation to Combine

a. *Saxler* and *Yoshida*

It would have been obvious to implement *Yoshida*'s non-recessed gate in *Saxler*'s stacked gate structure. Shealy, [139]-[149].

Saxler and *Yoshida* disclose compatible enhancement-mode GaN HEMT devices comprising the same layers performing the same functions, including a stacked gate structures having a cap layer and gate metal. Shealy, [140]. Both describe gallium nitride HEMTs with improved breakdown voltages over the prior art. *Yoshida*, [0008]-[0009]; *Saxler*, [0006], [0007]-[0030]; Shealy, [140]. They use the same arrangement of layers, as the below comparison illustrates. Shealy, [140].



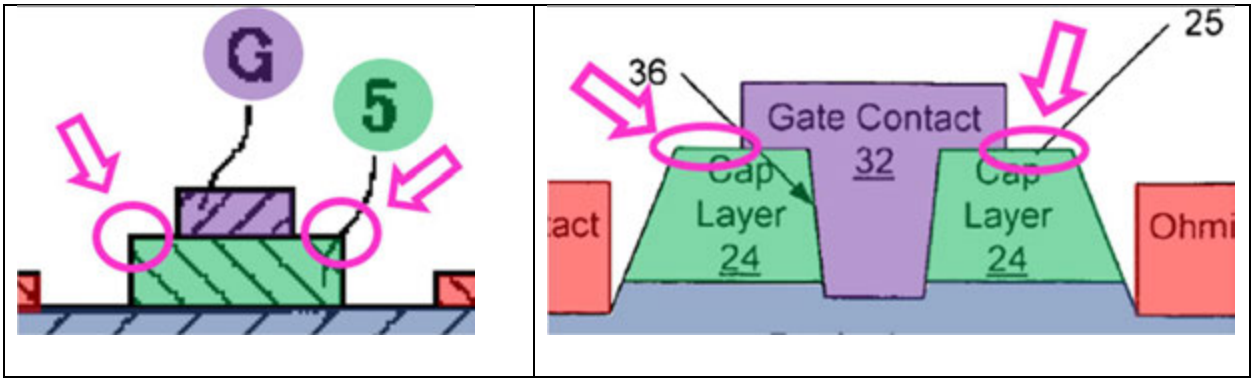


Yoshida, Fig. 1, *Saxler*, Fig. 1A

Yoshida's **layer 3** is GaN over a silicon substrate, as is *Saxler*'s **channel layer 20**. *Yoshida*, [0012], [0019]; *Saxler*, [0057]-[0058]; Shealy, [141]. *Yoshida*'s **layer 4** is an n-type semiconductor, just like embodiments of *Saxler*'s **barrier layer 22**. *Yoshida*, Abstract, [0010], [0013]; *Saxler*, [0059]-[0060]; Shealy, [141]. Both have **2DEG regions** formed at the junction of these two layers. *Yoshida*, [0016]; *Saxler*, [0004], [0006], [0008]. Both have **source**, **drain**, and **gate metal** contacts. *Yoshida*, Abstract, [0009]; *Saxler*, [0065]-[0066]. And both disclose a **doped layer** above the **barrier** and in contact with the **gate metal**. *Yoshida*, Abstract, [0015]; *Saxler*, [0069], Figs. 1A, 2B; Shealy, [141].

The specific form of their stacked gate differs between references but performs the same function—to control voltage "with a small amount of carrier injection" and "enable[] control of current flowing between channels" at high voltage. *Yoshida*, [0017]; *Saxler*, [0065]; Shealy, [142].

In the pictured *Saxler* embodiment, the metal may occupy a recess in the cap layer. *Saxler*, Abstract, [0007]-[0008], Figs. 1A, 2B, Shealy, [143]. *Yoshida*'s gate metal, in contrast, sits flush on top of layer 5. *Yoshida*, Fig. 1; Shealy, [143].



Yoshida, Fig. 1, *Saxler*, Fig 1A.

Saxler repeatedly discloses that this gate recess is optional. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88. But to the extent Patent Owner disagrees *Saxler*'s disclosure that the use of the recess is optional alone renders this structure obvious (Ground 1), *Yoshida* further renders it obvious (Ground 2). Shealy, [144].

A POSITA would have found it obvious to combine *Saxler*'s gate structures with *Yoshida*'s gate structure and accompanying fabrication techniques. Shealy, [145]. For example, a POSITA would have known many methods of making such stacked, stepped structures (§II) and combined *Saxler* and *Yoshida* to simplify manufacturing and decrease costs. *Id. Saxler* references and incorporates *Sheppard* (Ex. 1021) as disclosing "[s]uitable structures and techniques for fabricating GaN-

based HEMTs" according to *Saxler*'s purported invention. *Saxler*, [0046] (referencing Ser. No. 10/897,726), [0068] (same). *Sheppard* discloses complicated and exacting manufacturing processes to create a gate recess and deposit the gate metal. *Saxler*, [0043], [0046]-[0051], [0053]-[0056], Figs. 1C-1F, 2A-2B, Fig. 3. Its GaN cap layer may be "about 2 nm to 500 nm thick," and the thin AlGaN underlying barrier layer is between "0.1 nm and about 40 nm." GaN. *Saxler*, [0040], [0042]; Shealy, [145]. Accordingly, tolerances when manufacturing the gate recess are extremely small. Shealy, [145]. This raises complexity and costs of manufacturing to avoid costly out-of-tolerance defects. *Id*.

To avoid these problems, a POSITA would have been motivated to use *Saxler*'s non-recessed gate contact in its stacked gate structure in combination with *Yoshida*'s gate structure and accompanying fabrication techniques. Shealy, [147]. A POSITA would have recognized this as a suitable option for solving such problems. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007); *Intel Corp. v. PACT XXP Schweiz AG*, 61 F.4th 1373, 1379-81 (Fed. Cir. 2023). A POSITA would have known a wide variety of stacked gate structures in GAN HEMT devices, including many without recessed gates. Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [145].

A POSITA would have further been motivated to remove the gate recess to turn *Saxler*'s device into an enhancement-mode device, thus realizing the benefits

of reduced power consumption and suitability for high power applications. *Suh*, 1; Shealy, [146]. *Saxler* recognizes still other HEMT structures would be compatible with its disclosure, including *Smith*'s non-recessed devices which it incorporates by reference. §VII.A.1; *Saxler*, [0087]; Shealy, [148].

In view of the many options for stacked gate structures in GaN HEMT, including non-recessed stacked gate structures that *Saxler* expressly discloses, a POSITA would have found the substitution of *Yoshida*'s non-recessed gate arrangement for *Saxler*'s gate arrangement nothing more than the simple substitution of known elements to predictably yield an enhancement-mode GaN HEMT device. Shealy, [149].

a. *Saxler-Yoshida*, *Beach*, and *Shenoy*

Further, it would have been obvious to use the methods of *Beach* and *Shenoy* to fabricate the *Saxler-Yoshida* gate structure for the same reasons discussed with respect to using *Beach* and *Shenoy* to make the non-recessed *Saxler* structure. §VII.A.5; Shealy, [090]-[098], [150]. The *Saxler-Yoshida* gate structure is the same as the non-recessed *Saxler* structure. §VIII.A.2; Shealy, [150]. The combination of *Saxler-Yoshida* with *Beach* and *Shenoy* would have been obvious to predictably improve gate alignment and symmetry while reducing manufacturing steps and costs. §VII.A.5; Shealy, [150].

B. Independent Claim 1

1. [1p]

Saxler discloses [1p]. §VII.B.1; Shealy, [151].

2. [1a]

Saxler discloses [1a]. §VII.B.2; Shealy, [152].

3. [1b]

Saxler discloses [1b]. §VII.B.3; Shealy, [153].

4. [1c]

Saxler discloses [1c]. §VII.B.4; Shealy, [154].

5. [1d]

Saxler discloses [1d]. §VII.B.5; Shealy, [155].

6. [1e]

Saxler discloses [1e]. §VII.B.6; Shealy, [156].

7. [1f]

Saxler, *Beach* and *Shenoy* render obvious [1f]. §VII.B.7; Shealy, [157]-[158].

Saxler-Yoshida, *Beach* and *Shenoy* also render obvious [1f]. Shealy, [158]. The *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments. §VIII.A.2; Shealy, [158]. It would have been obvious to combine *Saxler-Yoshida* with *Beach* and *Shenoy,* disclosing [1f] for the same reasons explained for *Saxler*, *Beach*, and *Shenoy*. §§VIII.A.3, VII.B.7; Shealy, [112]-[115], [158].

8. [1g]

Saxler, Beach and *Shenoy* render obvious [1g]. §VII.B.8; Shealy, [159]-[160].

Saxler-Yoshida, *Beach* and *Shenoy* also renders obvious [1g] under either construction. Shealy, [160]. The *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments. §VIII.A.2; Shealy, [160]. It would have been obvious to combine *Saxler-Yoshida* with *Beach* and *Shenoy,* disclosing [1g] for the same reasons. §§VIII.A.3, VII.B.8; Shealy, [116]-[119], [160].

9. [1h]

Saxler and *Beach* renders obvious [1h]. §VII.B.9; Shealy, [161]-[162].

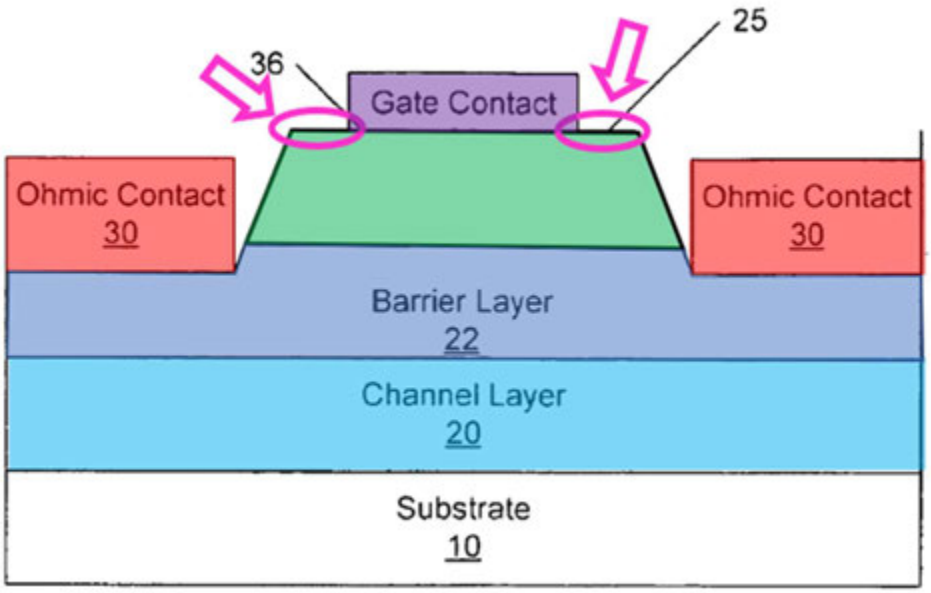
Saxler-Yoshida also renders obvious this limitation. Shealy, [162]. The *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments. §VIII.A.2; Shealy, [162]. It would have been obvious to combine *Saxler-Yoshida*, disclosing [1h] for the same reasons. Shealy, [162]; §§VIII.A.3, VII.B.9; Shealy, [120]-[123], [162].

10. [1i]

Saxler, Beach and *Shenoy* render obvious [1i]. §VII.B.10; Shealy, [163]-[164].

Saxler-Yoshida, Beach and *Shenoy* also renders obvious this limitation under either construction. Shealy, [164]. The *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments.

§VIII.A.2; Shealy, [164]. It would have been obvious to combine *Saxler-Yoshida* with *Beach* and *Shenoy,* disclosing [1i] for the same reasons. §§VIII.A.3, VII.B.10; Shealy, [124]-[127], [164].



Saxler, Fig. 1A (modified).

C. [Claim 2]

As explained, claim 2 does not further limit claim 1 because its requirements are included in [1i]. §VII.C; Shealy, [165]. *Saxler-Yoshida*, *Beach* and *Shenoy* render obvious claim 2 as explained for [1i]. §VIII.B.10; Shealy, [124]-[127], [165].

D. [Claim 3]

Saxler, Beach and *Shenoy* render obvious claim 3. §VII.D; Shealy, [129]-[132], [166].

Saxler-Yoshida, Beach and *Shenoy* also renders obvious this limitation. Shealy, [167]. The *Saxler-Yoshida* combination discloses the same stacked, stepped

gate structure as the non-recessed *Saxler* embodiments. §VIII.A.2; Shealy, [167]. It would have been obvious to combine *Saxler-Yoshida* with *Beach* and *Shenoy,* disclosing claim 3 for the same reasons. §§VIII.A.3, VII.D; Shealy, [129]-[132], [167].

IX. Ground 3: *Saxler* in view of *Ahn*

A. Overview of Ground 3

To the extent *Saxler* alone does not explicitly disclose masking and etching the gate contact or self-aligned etching, *Ahn* renders this obvious.

1. Ahn

Ahn uses a single mask with isotropic and anisotropic etching to create stacked gate structures having stepped features and sloped sidewalls. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4A-4C; Shealy, [169]. *Ahn*'s **top layer gate metal** and **underlying layer** are etched using a single **photomask** to have sloped sidewalls and a pair of horizontal **ledges** on either side of the **top gate metal**. *Id*. *Ahn* etches **top layer gate metal** and **underlying layer** to different thicknesses W_1 and W_2 to create those ledges, which improve performance and prevent deterioration. *Ahn*, 4:39-59, 5:21-27, 5:63-6:26, 7:24-31; Shealy, [169]. Its layers are symmetric, and their side surfaces preferably have an "inclined shape." *Ahn*, 6:12-37, Fig. 4C; Shealy, [169].

FIG. 4A

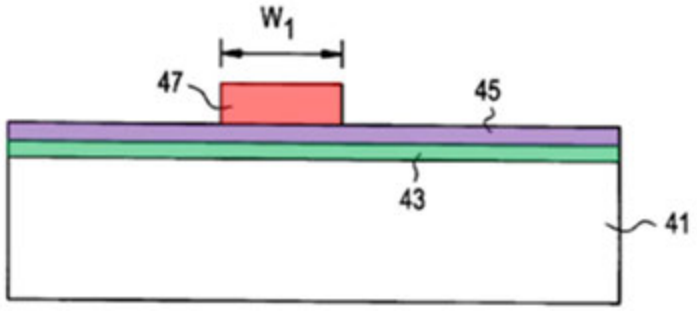


FIG. 4B

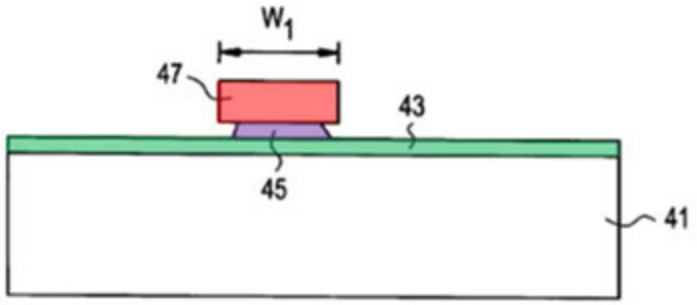
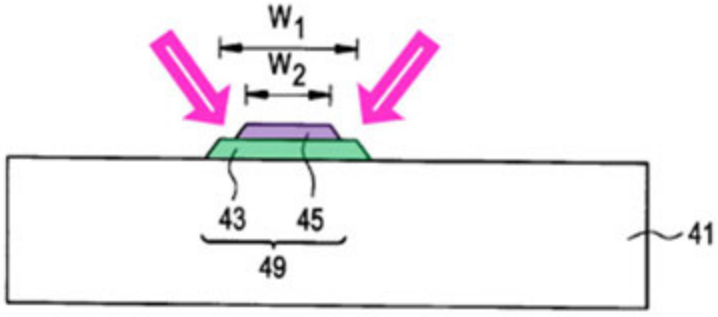


FIG. 4C



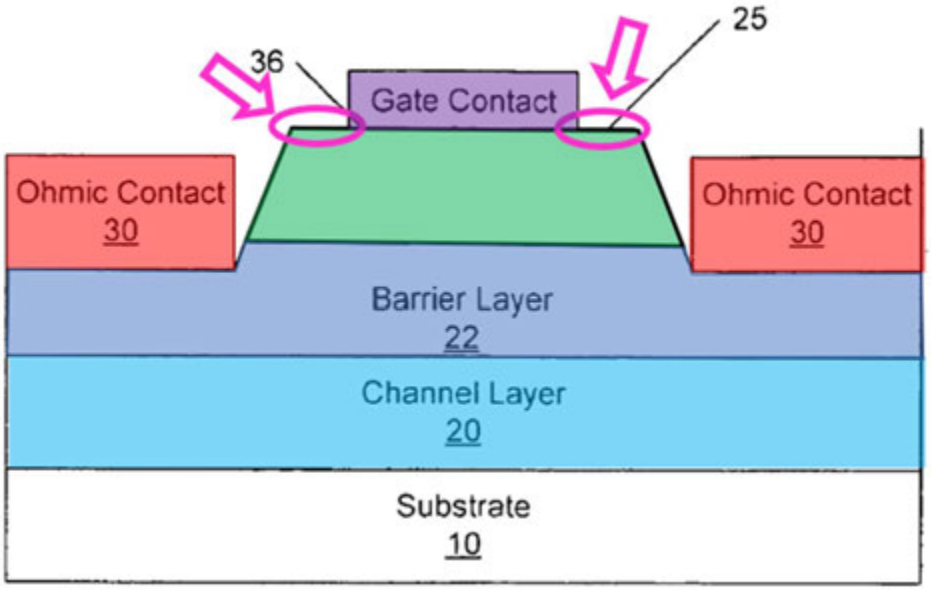
Ahn, Figs. 4A-4C.

Ahn teaches using a **single mask** to obtain this same structure in a variety of ways, including: (i) perform an anisotropic dry etch to obtain sloped sidewalls then etch the gate metal isotropically (*Ahn*, 7:7-14); (ii) etch both layers simultaneously with

a solution that etches the top layer more quickly (*Ahn*, 7:15-30); or (iii) dry etch the first layer and wet etch the second layer (*Ahn*, 7:31-46). Shealy, [170]. Although *Ahn* is directed to semiconductor transistors in liquid crystal displays, the transistor gate structure is analogous to those in GaN HEMT devices. Shealy, [170].

2. Combination of *Saxler* and *Ahn*

The combination would yield the same structure as the non-recessed *Saxler* embodiment:



Saxler, Fig. 1A (modified).

3. Motivation to Combine

A POSITA would have found it obvious to make the *Saxler*'s non-recessed stacked gate structure using *Ahn*'s methods of forming a transistor gate. Shealy, [172]-[176].

Saxler produces its stacked gate structure by masking and etching the cap layer, removing the mask, then depositing the gate contact. *Saxler*, [0064]-[0066], Figs. 1A-1B; §VII.A.1; Shealy, [173]. A POSITA would have understood a second mask would be used to deposit the gate metal. Shealy, [0091] (citing *Saxler*, [0065]-[0066]; *Smith*, [0041]-[0044], Figs. 4A-4C, 6A-6C), [173]. A POSITA would have been motivated to simplify this process and reduce costs by using fewer masks. *Id.*

A POSITA would have known many ways to create *Saxler*'s stepped gate structure in its non-recessed embodiments and would have used these methods interchangeably. Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [174]; §II. The '347 patent was allowed without disclosing any particular method to obtain the claimed ledges because their manufacture was well within the skill level of a POSITA. Ex. 1002, 25-30, 44-55, 74-76, 80-99; §§II, III.B; Shealy, [057]-[063], [174]. A POSITA would have found it obvious to modify *Saxler* with *Ahn*'s approach for making a stepped gate in a thin-film transistor to improve alignment. Shealy, [174] (citing *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C).

Ahn teaches many ways to obtain the non-recessed *Saxler* gate, including etching both layers simultaneously, or etching them sequentially using combinations of conventional wet and dry etching techniques. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C; Shealy, [175]. For example, *Ahn* exploits differences

between rates of dissolution of its layers to make the top gate layer narrower than the bottom. *Ahn*, 7:7-14-46; Shealy, [175]. A POSITA would have understood that *Saxler*'s cap layer, which was a p-type doped semiconductor, would have had a slower rate of dissolution than its metallic gate contact and found it obvious to use *Ahn*'s approach to arrive at a non-recessed, stepped gate structure. Shealy, [175]. *Ahn's* methods result in symmetrically aligned layers. *Ahn*, 6:15-37, Fig. 4C; Shealy, [175]. *Ahn* teaches that its single-mask approach is "preferred," and that it leads to symmetrically aligned layers with ledges of "substantially the same width" for "best results." *Ahn*, 4:52-49, 5:55-62, 6:27-37, 7:15-46; Shealy, [175].

A POSITA would have found the combination a simple substitution of *Ahn*'s known methods that would be predictably implemented in *Saxler*'s flexible method of manufacturing to improve alignment and symmetry between layers while reducing manufacturing steps and costs. Shealy, [176] .

B. Independent Claim 1

1. [1p]

Saxler discloses [1p]. §VII.B.1; Shealy, [177].

2. [1a]

Saxler discloses [1a]. §VII.B.2; Shealy, [178].

3. [1b]

Saxler discloses [1b]. §VII.B.3; Shealy, [179].

4. [1c]

Saxler discloses [1c]. §VII.B.4; Shealy, [180].

5. [1d]

Saxler discloses [1d]. §VII.B.5; Shealy, [181].

6. [1e]

Saxler discloses [1e]. §VII.B.6; Shealy, [182].

7. [1f]

Saxler and *Ahn* render obvious [1f]. Shealy, [183]. *Ahn* forms "**photoresist 47**" over the **top gate metal** layer before etching. *Ahn*, 5:55-6:36, 7:7-46; Shealy, [183].

FIG. 4A

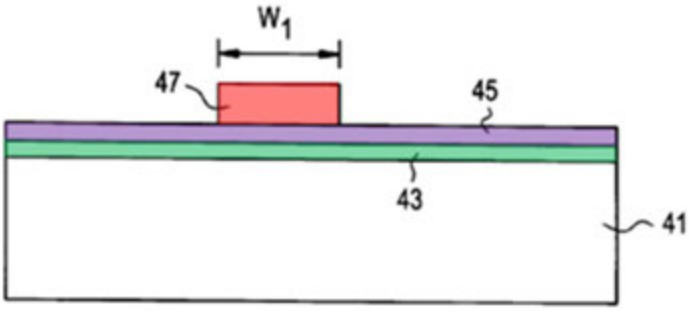
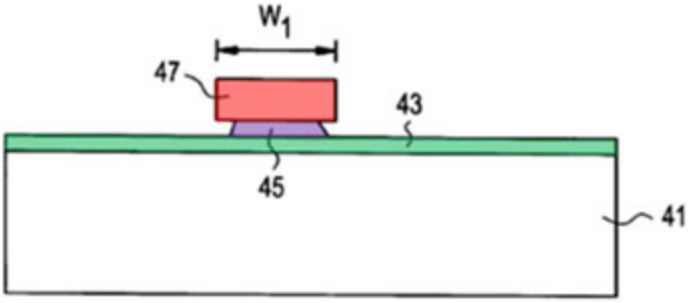


FIG. 4B



Ahn, Figs. 4A-4B.

It would have been obvious to make *Saxler*'s gate structure with *Ahn*'s approach to using a single a photomask over the gate metal. §IX.A.3; Shealy, [183].

8. [1g]

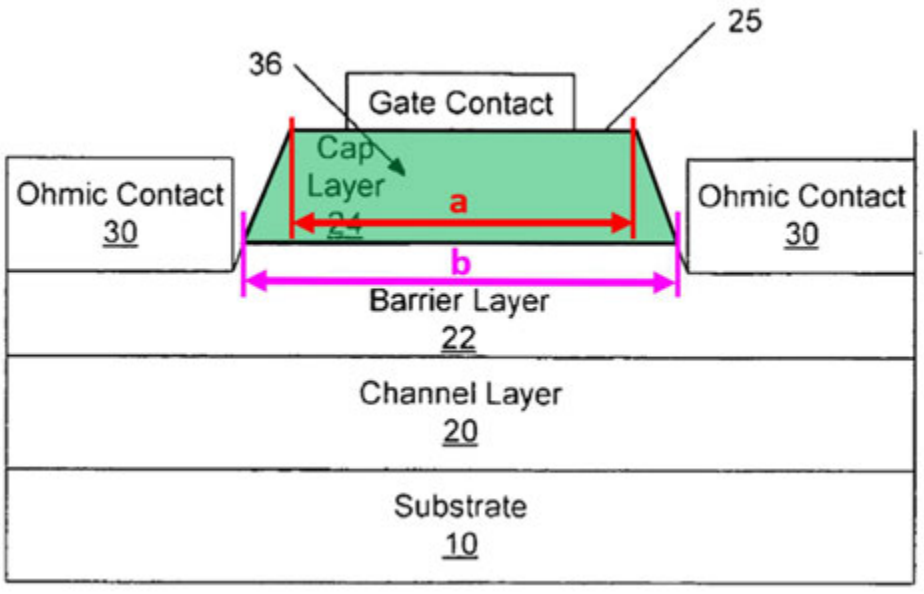
Saxler and *Ahn* render obvious [1g] under either construction. Shealy, [184]-[185]. *Ahn* etches both layers of its gate structure. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C; Shealy, [184]. *Ahn* discloses several ways to do so using ***one mask***, including: (i) perform an anisotropic dry etch to obtain sloped sidewalls then etch the gate metal isotropically (*Ahn*, 7:7-14); (ii) etch both layers simultaneously with a solution that etches the top layer more quickly (*Ahn*, 7:15-30); and (iii) dry etch the first layer and wet etch the second layer (*Ahn*, 7:31-46). Shealy, [184]. *Ahn* teaches that its single-mask approach is "preferred," and that it leads to symmetrically aligned layers with ledges of "substantially the same width" for "best results." *Ahn*, 4:52-49, 5:55-62, 6:27-37, 7:15-46; Shealy, [184].

It would have been obvious to make *Saxler*'s gate structure with *Ahn*'s approach of using a single a photomask over the gate metal and etching both *Saxler*'s gate metal and its cap layer. §IX.A.3; Shealy, [172]-[176], [185].

9. [1h]

Saxler and *Ahn* render obvious [1h]. Shealy, [186]. In the combination, *Saxler*'s **cap layer** would be etched using conventional techniques to obtain its

sloped sidewalls extending towards **source** and **drain contacts** and contacting the **barrier layer**, as shown below. *Saxler* and *Sheppard*, incorporated by reference to disclose methods of forming gate structures (*Saxler* [0046] (referencing Ser. No. 10/897,726), [0068] (same))), each describe using several conventional techniques to etch the cap layer and generate the slope sidewalls shown in their figures. *Saxler*, [0064], Figs. 1A-1B; *Sheppard*, [0044], Figs. 1B-1C. Shealy, [186]. The layers of *Ahn*'s gate structure also have sloped sidewalls. *Ahn*, Fig. 4C; Shealy, [186]. It would have been obvious to combine *Saxler*'s techniques with *Ahn*'s single mask processes to differentially etch multiple metal layers to obtain the **cap layer**'s sloped sidewalls in a stacked structure. *Ahn*, 5:55-6:36, 7:7-46; §IX.A.3; Shealy, [186]. The width of the bottom layer is more than 10% wider than the top, satisfying either parties' construction. Shealy, [186].



Saxler, Fig. 1A (modified).

10. [1i]

Saxler and *Ahn* render obvious this limitation under either construction. Shealy, [187]-[188]. *Ahn* etches its **top layer gate metal** under a **photoresist** such that is narrower than the **underlying layer** to form a pair of **ledges** on either side of the **top gate metal**. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C; Shealy, [187]. Although not depicted, in some embodiments, *Ahn* etches the top layer as a second step to narrow the top layer after first etching both layers of its gate structure. *Ahn*, 7:7-14; Shealy, [188]. *Ahn* teaches that its single-mask approach is "preferred," and that it leads to symmetrically aligned layers with ledges of "substantially the same width" for "best results." *Ahn*, 4:52-49, 5:55-62, 6:27-37, 7:15-46; Shealy, [188].

FIG. 4A

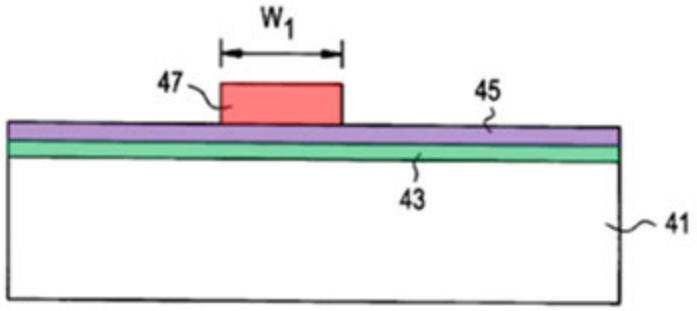


FIG. 4B

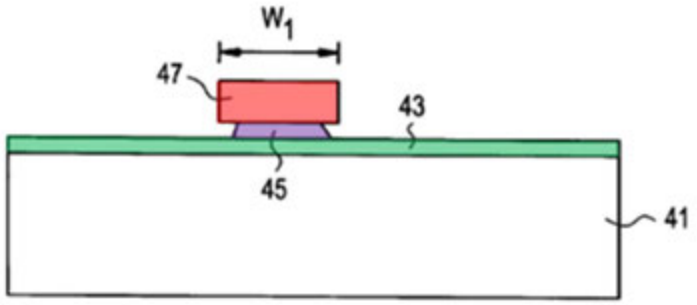
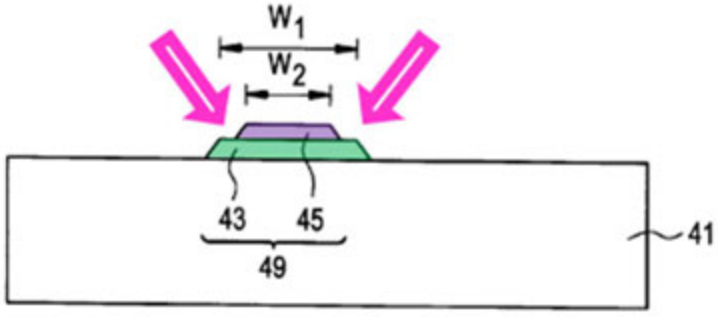


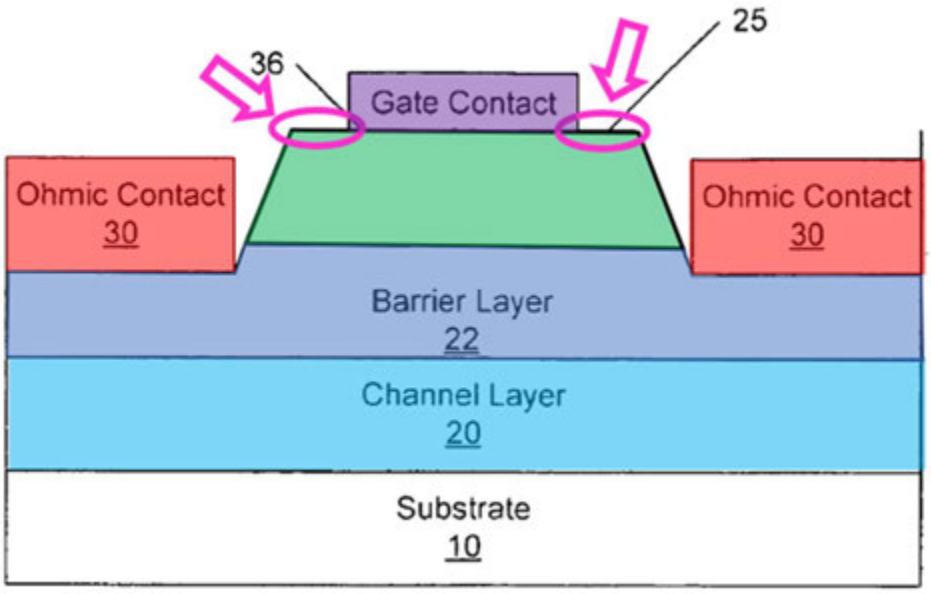
FIG. 4C



Ahn, Figs. 4A-4C.

It would have been obvious to combine *Saxler*'s techniques with *Ahn*'s single mask processes to differentially etch multiple metal layers to obtain a narrower gate

contact and ledges on an underlying in a stacked structure. *Ahn*, 5:55-6:36, 7:7-46; §IX.A.3; Shealy, [172]-[176], [189].



Saxler, Fig. 1A (modified).

C. [Claim 2]

As explained, claim 2 does not further limit claim 1 because its requirements are included in [1i]. §VII.C; Shealy, [189]. *Saxler* and *Ahn* renders obvious claim 2 as explained for [1i]. §IX.B.10; Shealy, [187]-[189].

D. [Claim 3]

The combination of *Saxler* and *Ahn* renders obvious Claim 3. Shealy, [190]-[192].

Ahn uses a **single mask** to etch a gate having a **top metal layer** and **underlying layer** with horizontal **ledges**, which is a "self-aligned" process. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C; Shealy, [191]. It discloses multiple ways to etch two

layers under a single photomask and arrive at this same stacked, stepped gate structure. *Ahn*, 7:7-46; Shealy, [191].

FIG. 4A

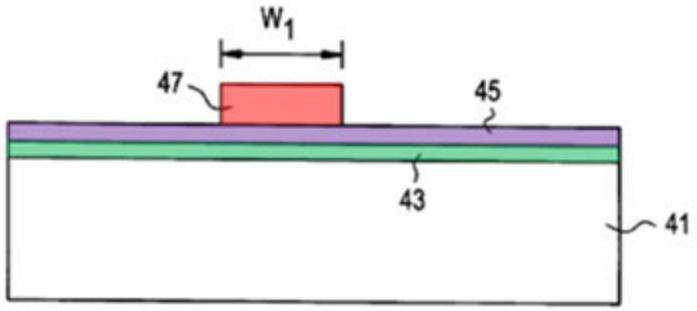


FIG. 4B

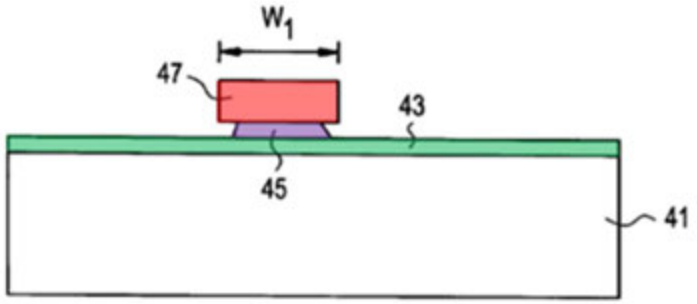
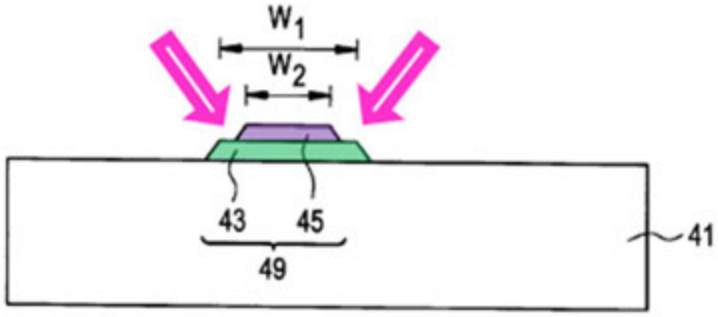


FIG. 4C



Ahn, Figs. 4A-4C.

It would have been obvious and predictable to combine *Saxler*'s techniques with *Ahn*'s single mask processes to make *Saxler*'s gate structure. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C; §IX.A.3; Shealy, [172]-[176], [192].

X. Ground 4: *Yoshida* in view of *Saxler*, *Beach*, and *Shenoy* Renders Obvious Claims 1-2

A. Overview of Ground 4

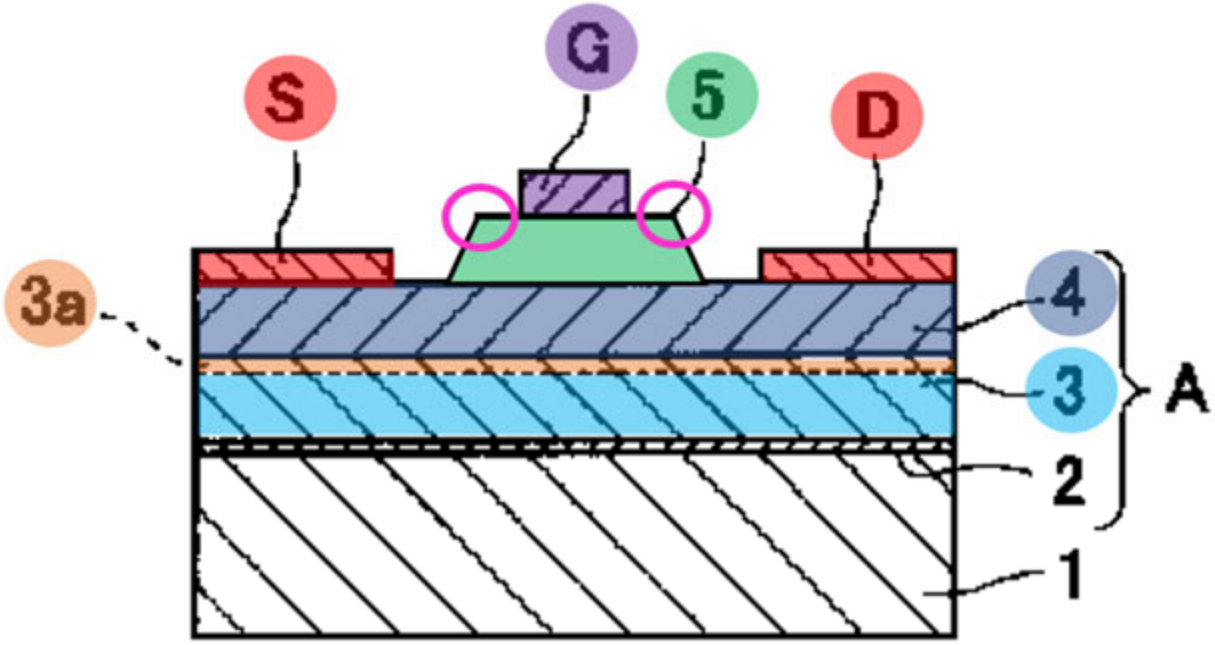
The combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* renders obvious claims 1-3. Shealy, [193]-[237].

As explained above and below, *Yoshida* discloses the arrangement of semiconductor layers and structures produced by the method of claim 1, including the claimed ledges, but depicts its p-type gate material with vertical sidewalls. *Saxler* also disclose the structure made according to the method of claim 1, including the ledges and sloped sidewalls on its cap layer (e.g., Ground 1). The references are compatible, and their combination would have been a simple substitution to predictably make *Yoshida*'s same GaN HEMT device but with *Saxler*'s sloped sidewalls.

Further, a POSITA would have found it obvious to use *Beach* and *Shenoy*'s techniques to self-align the p-type gate material and gate metal and isotropically etch the gate metal using a single mask to obtain self-aligned ledges, resulting in the same gate structure that *Yoshida-Saxler* discloses.

1. Ground 4: *Yoshida* in view of *Saxler*, *Beach*, and *Shenoy*

Implementing *Saxler*'s **sloped sidewalls** in *Yoshida*'s **layer 5** results in the following combined structure. Shealy, [196]. In the combination, the gate structure would have been made using *Beach* and *Shenoy*'s techniques. *Id.*



Yoshida, Fig. 1 (modified).

2. Ground 4: Motivation to Combine

a. *Yoshida-Saxler*

It would have been obvious to modify *Yoshida*'s transistor with the sloped sidewalls of *Saxler*'s capping layer to reduce gate leakage. Shealy, [197]. The combination calls for nothing more than the simple substitution of *Saxler*'s sidewalls to predictably make an enhancement-mode GaN HEMT. *Id.* And a POSITA would

have recognized *Saxler*'s sidewalls would have reliably reduced *Yoshida*'s gate leakage, making the combination obvious. *Id.*

The references are compatible for reasons explained in Ground 2. §VIII.A.3; Shealy, [198]. In view of these many similarities, it would have been obvious to incorporate *Saxler*'s known sloped **cap layer** sidewalls into *Yoshida* p-type **layer 5**. Shealy, [198]. Sloped sidewalls were conventional, as the '347 patent admits. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A; Shealy, [198]. The '347 patent provides "conventional schematic[s] [of an] enhancement-mode GaN transistor" depicting just such sloped sidewalls. Ex. 1001, 1:17-2:21, Figs. 1-4, 7A; Shealy, [198]. The angle of *Saxler*'s sloped sidewall is typical for known mesa structures. Shealy, [198] (citing *Xu*, *Kanda*, *Widman*). It would have been a simple substitution of *Yoshida*'s vertical sidewalls with *Saxler*'s sloped sidewalls to predictably yield an enhancement-mode GaN HEMT. *Id.*

A POSITA would have readily understood how to implement the combination. Shealy, [199]. *Saxler* discloses conventional etching techniques for straightforwardly forming its sloped sidewalls. *Id.* (citing *Saxler*, [0064]). *Yoshida* also forms its p-type **layer 5** through etching. *Yoshida*, [0021]-[0023]; Shealy, [199]. It would have been a simple substitution to employ *Saxler*'s etching approach to predictably shape *Yoshida*'s sidewalls. Shealy, [199].

Accordingly, a POSITA would have recognized that *Saxler* provided a known option for shaping the sidewalls of *Yoshida*'s p-type **layer 5**, and the combination would have been obvious.

A POSITA would have additionally recognized that *Saxler*'s sloped sidewalls would have beneficially reduced *Yoshida*'s leakage losses and found the combination obvious. Shealy, [201]. It was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage. *Id.* (citing *Xu*, 1; *Kanda*, [0013], [0027], [0144], [0157], Fig. 12A). The '347 patent itself recognizes that capping structures in prior art enhancement-mode GaN transistors with sloped sidewalls had a known "gate leakage current path 201 [that] flows along the sidewall of the p-type gate material 101." Ex. 1001, 1:59-2:3, Fig. 2. A POSITA would have understood that the geometry of *Saxler*'s sloped sidewalls provided longer leakage paths than *Yoshida*'s vertical sidewalls, thereby lowering gate leakage. Shealy, [201] (citing *Xu*, *Kanda*). That improvement makes *Saxler*'s sloped sidewalls a suitable option, motivating the combination. *KSR*, 550 U.S. at 417 (a motivation arises when a known technique that "improve[d] one device … would improve similar devices in the same way."); *Intel*, 61 F.4th at 1379-81.

A POSITA would have found it obvious to form a photoresist over the gate metal to etch the gate metal and achieve the gate structure of the *Yoshida-Saxler*

device. Shealy, [202]. *Yoshida* and *Saxler* teach interchangeable methods of forming stacked, stepped gate structure, which were among numerous techniques a POSITA would have known. §II; Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [202]. *Yoshida* deposits its **gate electrode** in an opening etched into a SiO_2 mask but does not explicitly disclose forming a photoresist on the gate and etching the gate metal. *Yoshida*, [0022]-[0023]; Shealy, [202]. Yet as explained for Ground 1, a POSITA would have found it obvious to form a single photoresist over the gate metal to etch the gate metal and the underlying layer in view of *Saxler* to position the gate metal precisely and reliable. §§VII.A.1, VII.B.7; Shealy, [080]-[085], [112]-[115], [202]. And for the same reasons, it would have been obvious to do so in the combination of *Yoshida-Saxler*. Shealy, [202].

b. *Yoshida-Saxler* in view of *Beach* and *Shenoy*

A POSITA would have found it obvious to make the stacked gate structure of the *Yoshida-Saxler*'s GaN HEMT device using the methods of *Beach* and *Shenoy* for the same reasons explained for *Saxler* alone or the *Saxler-Yoshida* device. §§VII.A.5, VIII.A.3; Shealy, , [090]-[098], [139]-[150], [203]-[209].

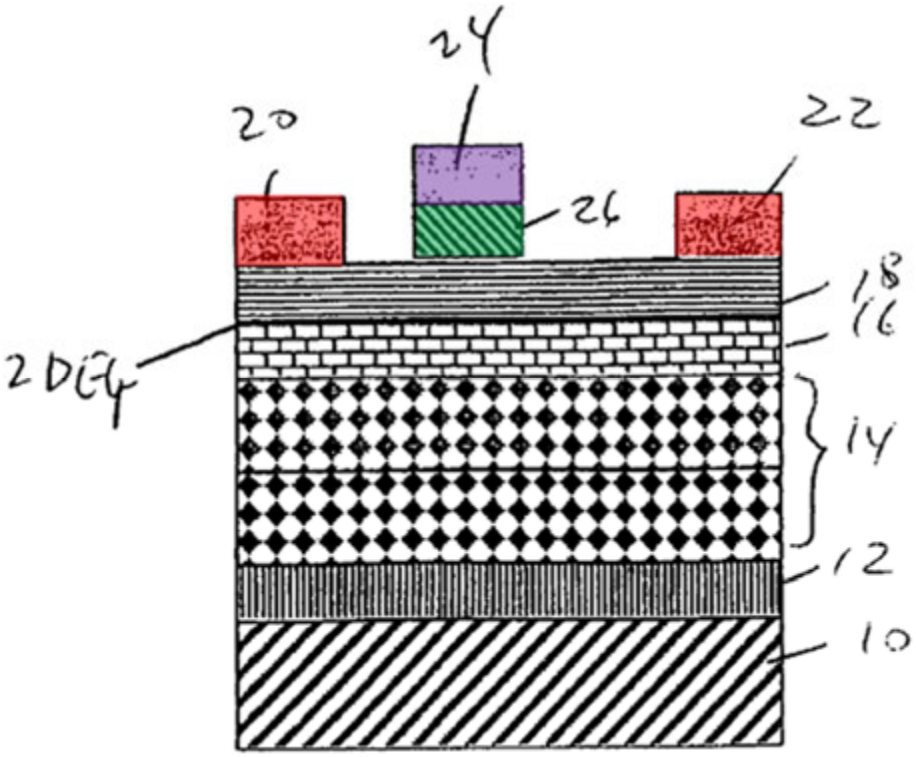
The *Yoshida-Saxler* combination uses a sequence of steps to arrive at a stacked gate structure with p-type GaN layer and a gate electrode. *Yoshida*, [0021]-[0022]; Shealy, [204]. Specifically, *Yoshida* discloses: (i) depositing a p-type GaN layer 5 onto AlGaN layer 4 (*Yoshida*, [0021]); (ii) dry etching the "p-type layer except

where the gate electrode was to be loaded" (*Yoshida*, [0022]); (iii) depositing an SiO_2 film over the entire surface (*id.*); (iv) patterning with a photoresist, and masking where the gate electrode was to be loaded (*id.*); (v) depositing source and drain electrodes (*id.*); (vi) "etching away the masking and opening the SiO2 film (*Yoshida*, [0023]); (vii) masking the source and drain electrodes; and (viii) depositing Au to form the gate electrode (*id.*). Shealy, [204]. That process thus requires at least two masks. Shealy, [204]. In the *Yoshida-Saxler* combination, etching step (ii) would simply employ *Saxler*'s conventional etching techniques to create sloped sidewalls and would employ *Saxler*'s techniques to position the gate metal, which are similar to *Beach*'s techniques. *Saxler*, [0064]; §X.A.2.a; Shealy, [204].

A POSITA would have known many ways to create *Yoshida-Saxler*'s stepped gate structure and would have used these methods interchangeably. §II; Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [205]. The '347 patent was allowed without disclosing any particular method to obtain the claimed ledges because their manufacture was well within the skill level of a POSITA. Ex. 1002, 25-30, 44-55, 74-76, 80-99; §§II, III.B; Shealy, [057]-[063], [205]. A POSITA would have found it obvious to modify *Yoshida-Saxler* by using *Beach*'s self-aligned technique and *Shenoy*'s isotropic etching to arrive at that same gate structure, which would have improved efficiency by eliminating masking and etching steps and would have ensured symmetry of the gate metal with respect to the

p-gate material. Shealy, [205]. A POSITA would have understood *Beach*'s "self-aligned" techniques would have used a single photomask, as described in greater detail in another *Beach* publication. *Beach-II*, [0047]-[0048], Figs. 1D-1E; Shealy, [205]. This approach was known—*Ahn* discloses this same approach for making a stepped gate in a thin-film transistor with symmetrically aligned layers. *Ahn*, Abstract, 3:41-58, 6:15-37, 7:7-14, Fig. 4C; Shealy, [205]. A POSITA would have found *Beach* and *Shenoy*'s methods obvious and predictable in light of *Smith*, incorporated into *Saxler* by reference to disclose methods of making gate structures (*Saxler*, [0087]), which also uses a "self-aligned" technique. *Smith*, [0041]-[0044], claim 25; §VII.A.1; Shealy, [205].

Beach teaches a more efficient method of making stacked gate structures in GaN HEMT devices using fewer steps because it uses a single mask. *Beach*, [0040], [0045], [0054]; Shealy, [206]. *Beach*'s gate structure includes the "gate arrangement 24," which comprises a gate electrode, and an underlying "gate barrier 26," a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Shealy, [206]. *Beach*'s process (i) deposits "**gate barrier 26**" and "**gate arrangement 24**" layers, (ii) patterns the stack with a mask, (iii) etches to obtain the stack, and (iv) deposits **power electrodes**. *Beach*, [0040]; Shealy, [206]. Such self-aligned techniques were common in the field as of relevant date. Shealy, [206].



Beach, Fig. 1.

A POSITA would have found it obvious to use *Beach*'s approach to create and symmetrically align *Yoshida-Saxler* gate structure for improved performance. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3; Shealy, [207].

Beach does not disclose steps to create the **horizontal ledges** of *Yoshida-Saxler*'s stacked gate structure following its self-aligned process. But as previously explained, *Shenoy* discloses simple isotropic etching techniques for symmetrically undercutting metal layers below photoresist masks. *Shenoy*, 2-3; Shealy, [208]; §VII.A.3.

Thus, an ordinary artisan would have found it obvious to use *Beach*'s self-aligned method of making *Yoshida-Saxler*'s stacked gate structure in a GaN HEMT

and use *Shenoy*'s methods to undercut the **gate electrode** and create *Yoshida-Saxler*'s **horizontal ledges**. Shealy, [209]. A POSITA would have found the combination a simple substitution of *Beach*'s and *Shenoy*'s known methods to predictably create *Yoshida-Saxler*'s stacked gate structure more efficiently and symmetrically. *Id.*

B. Independent Claim 1

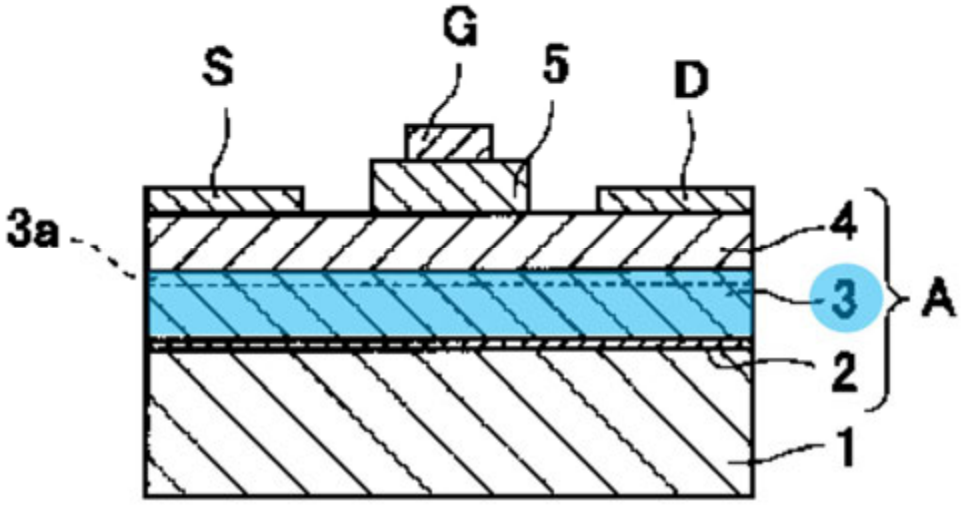
1. [1p]

To the extent it is limiting, *Yoshida* discloses [1p]. Shealy, [210]. For example, *Yoshida* discloses manufacturing a GaN high-mobility transistor that includes a p-type GaN layer below the gate, which "enables voltage control with a small amount of carrier injection," constituting a normally off enhancement-mode GaN transistor. *Yoshida*, Abstract, [0015], [0017], Fig. 1; Shealy, [210].

2. [1a]

[1a] was conventional. §VII.B.2 ; Shealy, [211].

Yoshida discloses [1a]. *Yoshida* forms "layer 3," which is a GaN layer. *Yoshida*, Abstract, [0010]-[0012], [0019]-[0020]; Shealy, [211]. *Yoshida* teaches that "i-type GaN is [a] particularly preferrable" embodiment of "**layer 3**," which is an intrinsic or undoped GaN. *Yoshida*, Abstract, [0012], Fig. 1; Shealy, [211].

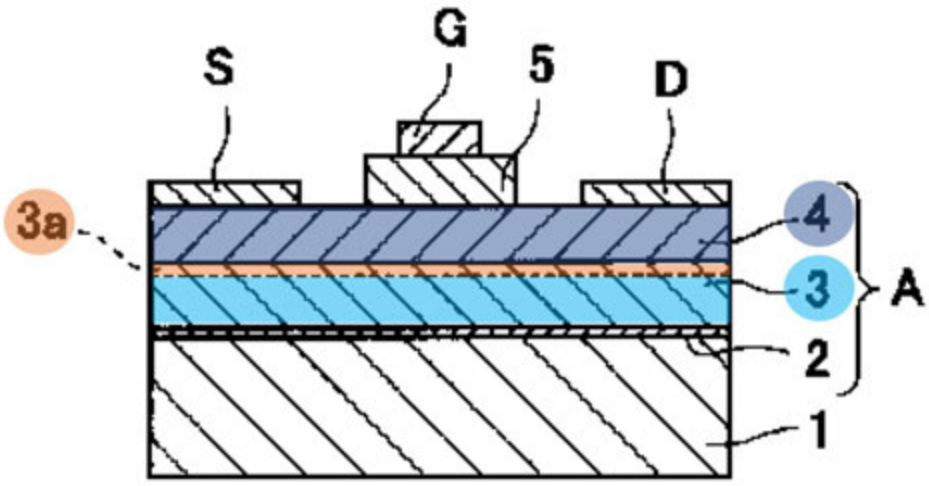


Yoshida, Fig. 1.

3. [1b]

[1b] was conventional. §VII.B.3 ; Shealy, [212].

Yoshida discloses [1b]. Shealy, [212]-[213]. *Yoshida*'s "**layer 4**" is a barrier layer formed on GaN "**layer 3**." *Yoshida*, Abstract, [0010], [0013], [0019]-[0021], Fig. 1. A "**two-dimensional electron gas layer 3a** is formed at the heterojunction interface" of **layer 4** and **layer 3**. *Yoshida*, [0016]; Shealy, [212].



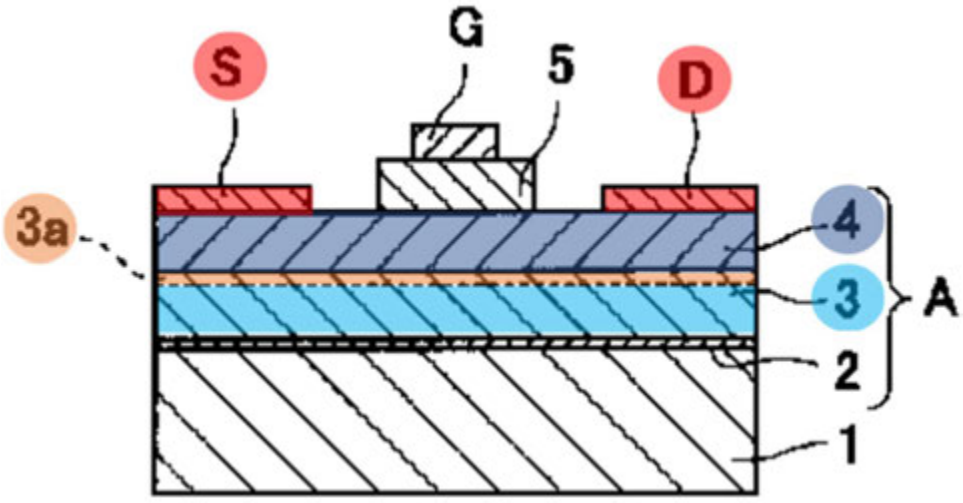
Yoshida, Fig. 1.

Yoshida identifies that "n-type AlGaN is [a] favorable" choice for **layer 4**. *Yoshida*, Abstract, [0010], [0013], Fig. 1; Shealy, [213]. The '347 patent likewise discloses that the claimed barrier layer may be an AlGaN layer, which is covered in dependent claims. Ex. 1001, 1:37-58, 3:32-43, 4:8-16, claims 3, 6; Shealy, [213].

4. [1c]

[1c] was conventional. §VII.B.4 ; Shealy, [214].

Yoshida discloses **source** and **drain electrodes** (contacts) that are "directly loaded" (deposited) on barrier **layer 4**. *Yoshida*, Abstract, [0014], [0022], Figs. 1-2, 3A-3B; Shealy, [214].

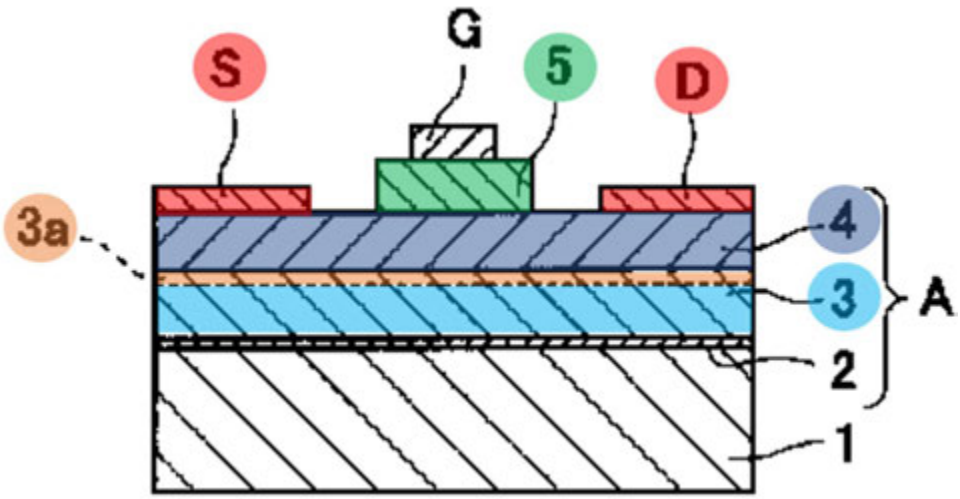


Yoshida, Fig. 1.

5. [1d]

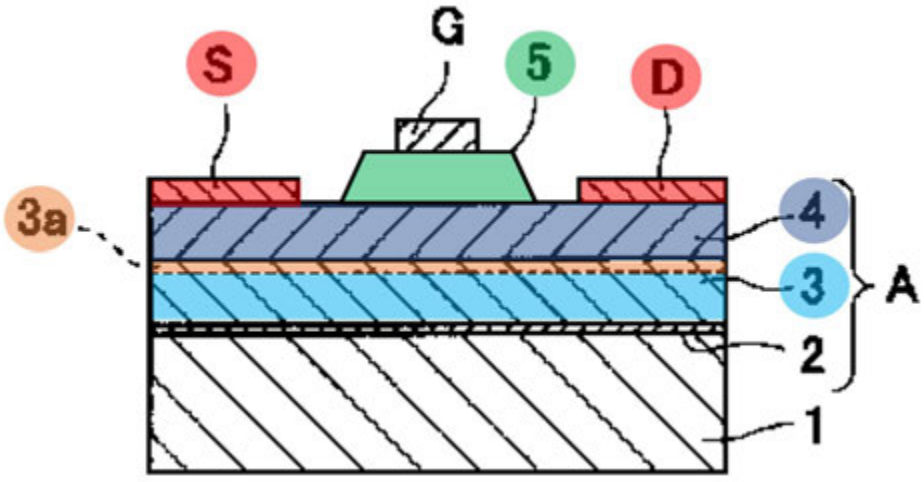
[1d] was conventional. §VII.B.5 ; Shealy, [215].

Yoshida discloses this limitation. *Yoshida*'s **layer 5** is "a p-type gate material" that is deposited on the **barrier layer**. **Layer 5** may be a single- or double-layer comprising a "p-type GaN." *Yoshida*, Abstract, [0009], [0015], [0018], claim 2; Shealy, [215].



Yoshida, Fig. 1.

Yoshida-Saxler likewise renders obvious this limitation. Shealy, [216]. *Saxler* discloses depositing a **cap layer** on the **barrier layer**. *Saxler*, [0010], [0013], [0059]-[0063], [0069], [0071], [0073], Figs. 1A, 2B; §VII.B.5 ; Shealy, [216].



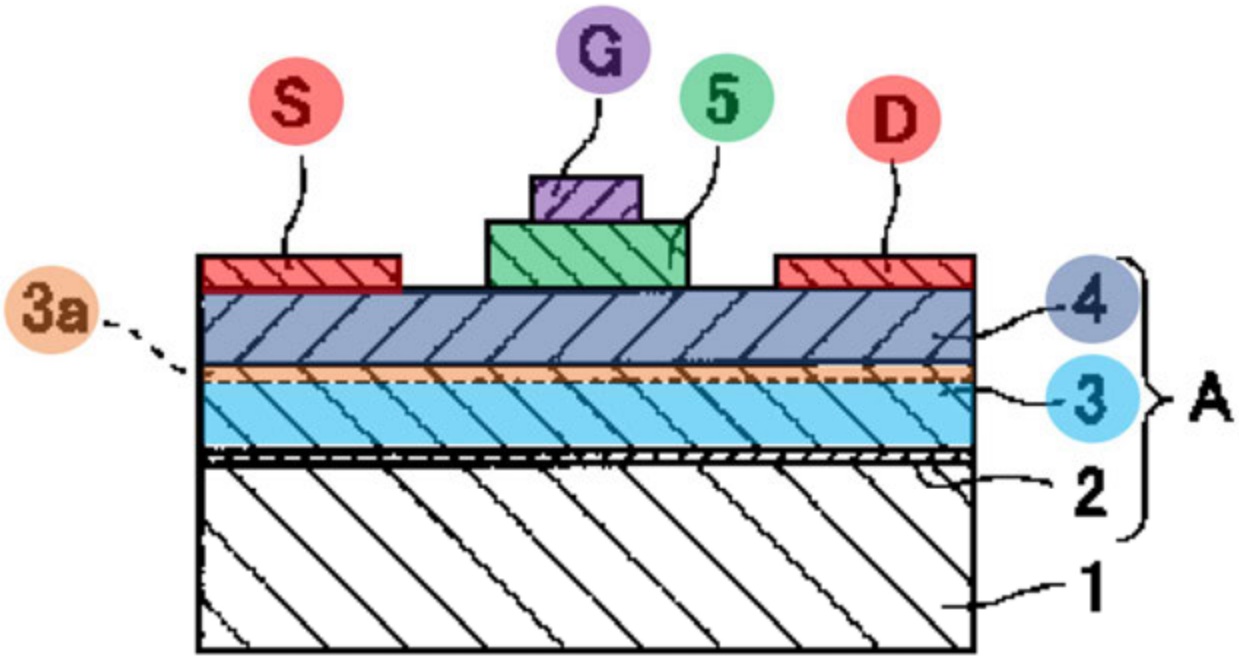
Yoshida, Fig. 1 (modified).

It would have been obvious to combine these references to deposit a **layer 5** with sloped sidewalls on the **barrier layer**. §X.A.2; Shealy, [216].

6. [1e]

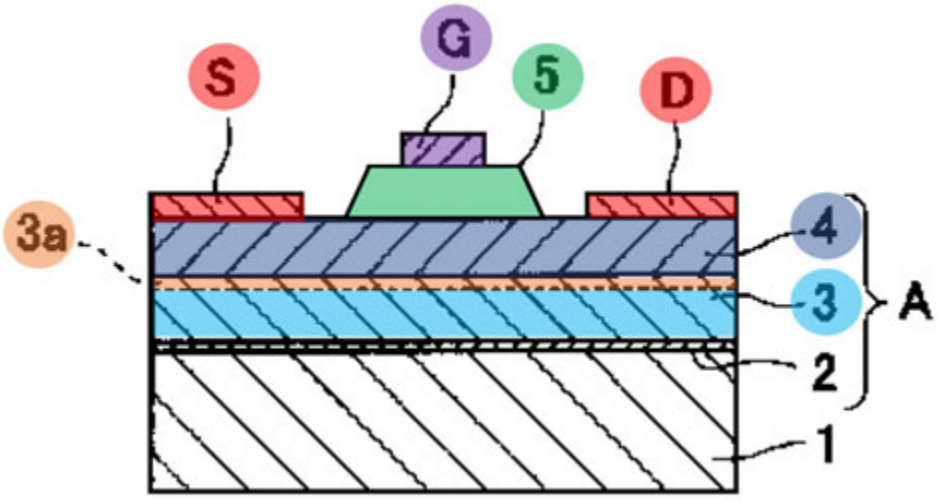
[1e] was conventional. §VII.B.6 ; Shealy, [217].

Yoshida discloses [1e]. *Yoshida*'s "**gate electrode**" is a metal (e.g., "Au/Pt, Al") deposited on p-type **layer 5**. *Yoshida*, Abstract, [0006], [0009]-[0010], [0016], [0022]-[0023], claim 1, Fig. 1; Shealy, [217].



Yoshida, Fig. 1.

Yoshida-Saxler likewise renders obvious this limitation. Shealy, [218]. *Saxler*'s **gate contact** is a gate metal (e.g., "Ni, Pt, $NiSi_x$, Cu, Pd, Cr, W and/or WSiN") formed on its **cap layer** in non-recessed embodiments. *E.g.*, *Saxler*, Abstract, [0052], [0066], Figs. 1A, 2B; §VII.B.6; Shealy, [218].



Yoshida, Fig. 1 (Modified).

It would have been obvious to combine these references to deposit a **gate electrode**, which is a metal (e.g., "Au/Pt, Al") deposited on a p-type **layer 5** with sloped sidewalls.§X.A.2; Shealy, [218].

7. [1f]

[1f] was conventional. §VII.B.7 ; Shealy, [219].

Yoshida-Saxler renders obvious forming a photoresist over the gate metal. The references teach interchangeable methods to achieve their stacked, stepped gate structures that render obvious this limitation. §§II; X.A.2; Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [219]. *Yoshida* deposits its **gate electrode** in an opening etched into a SiO_2 mask but does not explicitly disclose forming a photoresist on the gate and etching the gate metal. *Yoshida*, [0022]-[0023]; Shealy, [219]). Yet as explained for Ground 1, a POSITA would have found it obvious to mask and etch the gate metal in view of *Saxler* to

precisely and reliably position the gate metal. §§VII.A.1, VII.B.7; Shealy, [219]. And for the same reasons, it would have been obvious to do so in the *Yoshida-Saxler* combination. §X.A.2; Shealy, [219].

Yoshida-Saxler, Beach and *Shenoy* also render obvious [1f]. Shealy, [220]. *Beach* discloses forming a photoresist over the gate metal, specifying that "the stack is patterned and etched to obtain gate arrangement 24 over gate barrier 26." *Beach*, [0040]; Shealy, [220]. *Shenoy* also discloses a photoresist over a metal electrode. *Shenoy*, 1.

It would have been obvious to make *Yoshida-Saxler*'s gate structure with *Beach*'s and *Shenoy*'s approach to using a single a photomask over the gate metal with isotropic etching. §X.A.2; Shealy, [197]-[209], [221].

8. [1g]

[1g] was conventional. §VII.B.8 ; Shealy, [222].

Yoshida-Saxler renders obvious [1g] under either construction. *Id. Yoshida* deposits then etches **layer 5**. *Yoshida*, [0021]-[0022]; Shealy, [222]. And as explained for [1f], in the *Yoshida-Saxler* combination it would have been obvious to mask and etch the gate metal to position the gate metal precisely and reliably. §X.B.7; Shealy, [222].

Yoshida-Saxler, *Beach* and *Shenoy* also render obvious [1g] under both constructions. Shealy, [223]-[224]. *Beach* discloses using a single mask when

etching the gate metal and p-type gate material, specifying that both layers of "the stack [are] patterned and etched to obtain gate arrangement 24 over gate barrier 26." *Beach*, [0040]; Shealy, [223]. *Shenoy* discloses the same. *Shenoy*, 1.

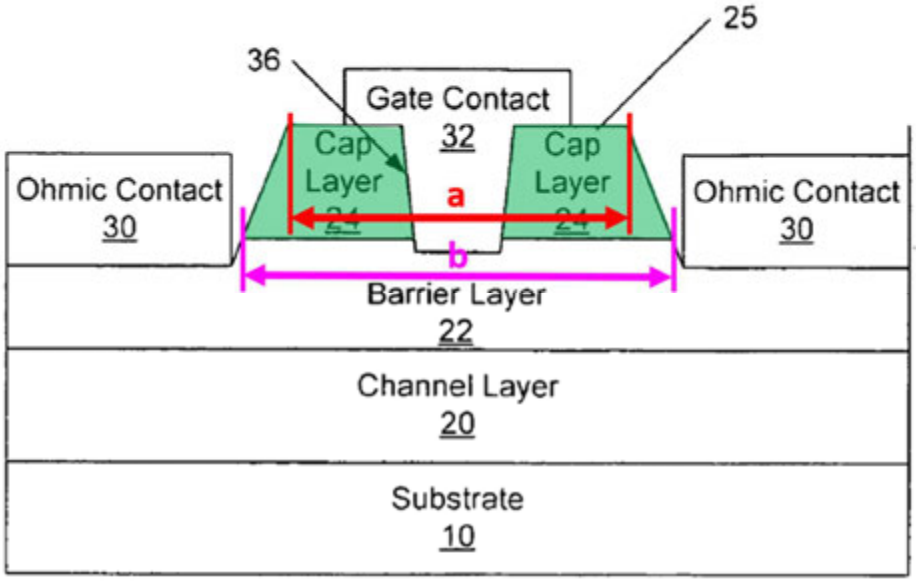
It would have been obvious and predictable to make *Yoshida-Saxler*'s gate structure with *Beach*'s and *Shenoy*'s approach to using a single a photomask over the gate metal with isotropic etching. §X.A.2; Shealy, [224].

9. [1h]

[1h] was conventional. §VII.B.9 ; Shealy, [225].

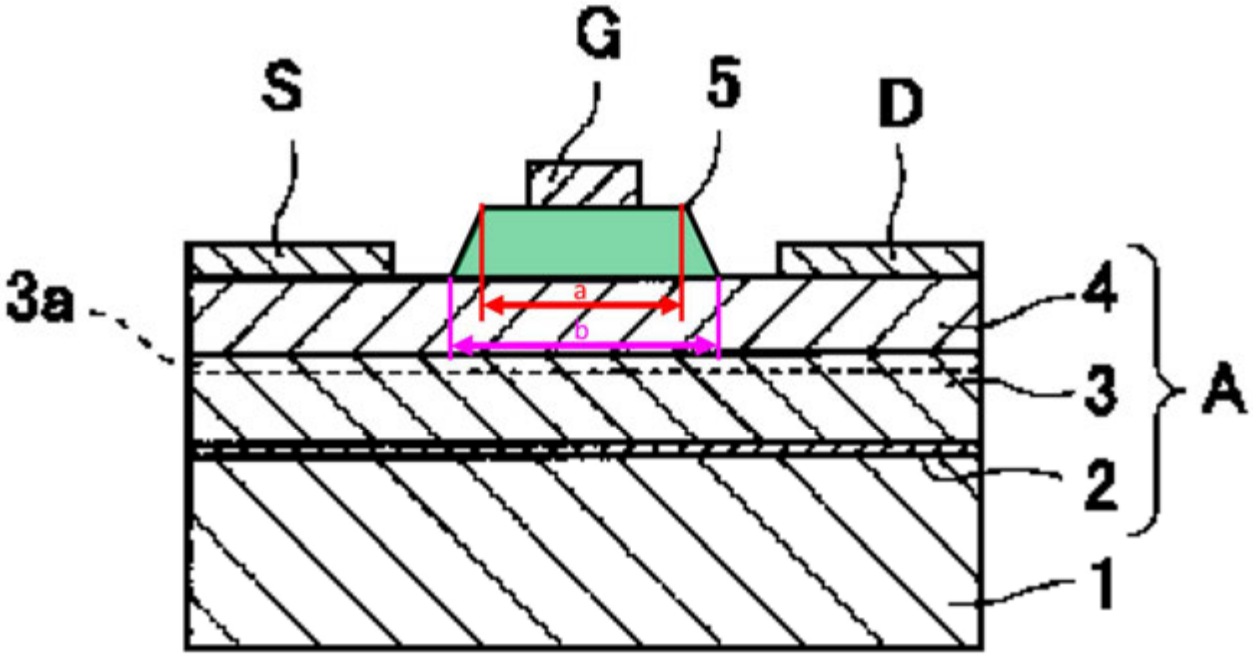
Yoshida-Saxler renders obvious this limitation. Like *Yoshida*'s **layer 5**, *Saxler*'s **cap layer** is a p-type gate material that may be doped p-type in a subregion or throughout the layer. *Saxler*, [0013], [0069], [0071], [0073]; Shealy, [225]. The **cap layer** resides above an AlGaN **barrier layer**, just like *Yoshida*'s **layer 5** and as claim 1 of the '347 patent requires. *Saxler*, [0010], [0059]-[0063], Figs. 1A, 2B; Shealy, [225]. The **cap layer** may take several forms, including "p-type dopant," which may be doped in a region of the cap layer or incorporated throughout. *Saxler*, [0069]; Shealy, [225].

Saxler's **cap layer** has side surfaces extending horizontally towards the **source** and **drain contact**. §VII.B.9; *Saxler*, [0064], Figs. 1A, 2B; Shealy, [226].



Saxler, Fig. 1A.

As explained above, it would have been obvious to combine the sloped sidewalls of *Saxler*'s doped **cap layer** into *Yoshida*'s p-type **layer 5** such that they horizontally extended towards the **source** and **drain contacts** in the *Yoshida-Saxler* device, resulting in the sloped structure under either construction, where the bottom of the **p-type gate material** (length "**b**," below) is more than 10% wider than the top (length "**a**"). §X.A.2; Shealy, [227].

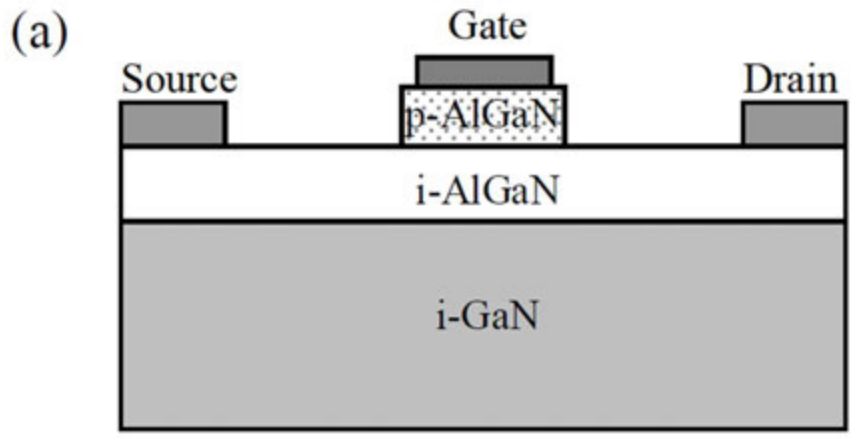


Yoshida, Fig. 1 (modified).

In addition, *Yoshida-Saxler*, *Beach* and *Shenoy* render obvious [1h]. Shealy, [228]. It would have been obvious to make *Yoshida-Saxler*'s gate structure with *Beach*'s approach to using a single a photomask over the gate metal.§X.A.2; Shealy, [197]-[209], [228].

Further, *Yoshida* alone renders obvious sloped sidewalls that extend horizontally towards source and drain contacts under Patent Owner's construction. Shealy, [229]-[230] (citing *Saxler*, [0042]; U*emoto*, Figs. 1-2, 5). Although *Yoshida* draws substantially vertical sidewalls of p-type **layer 5**, a POSITA would have known a sidewall drawn vertically would have a slight slope when built in a practical device. *Id*. For example, *Saxler* notes that, in practice, "an etched region illustrated as a rectangle will, typically, have ***tapered***, rounded or curved features." *Saxler*,

[0042]; Shealy, [230]. As another example, a 2006 IEEE paper on a GaN HEMT with a similar gate structure to *Yoshida* depicts its p-AlGaN gate layer having vertical sidewalls in its drawings (Fig. 1) but shows sloped sidewalls extending horizontally towards source and drain contacts in a microscope image of a device built according to the drawings. *Uemoto*, Figs. 1-2, Fig. 5; Shealy, [230].



Uemoto, Fig. 1(a) (drawing).

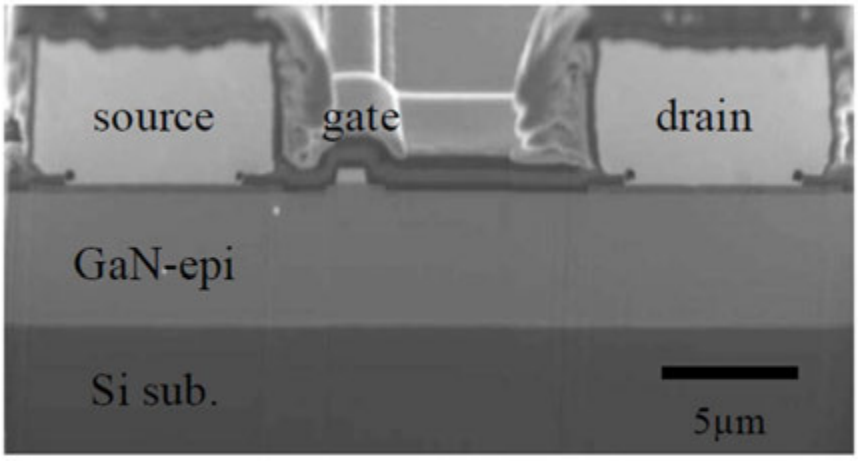
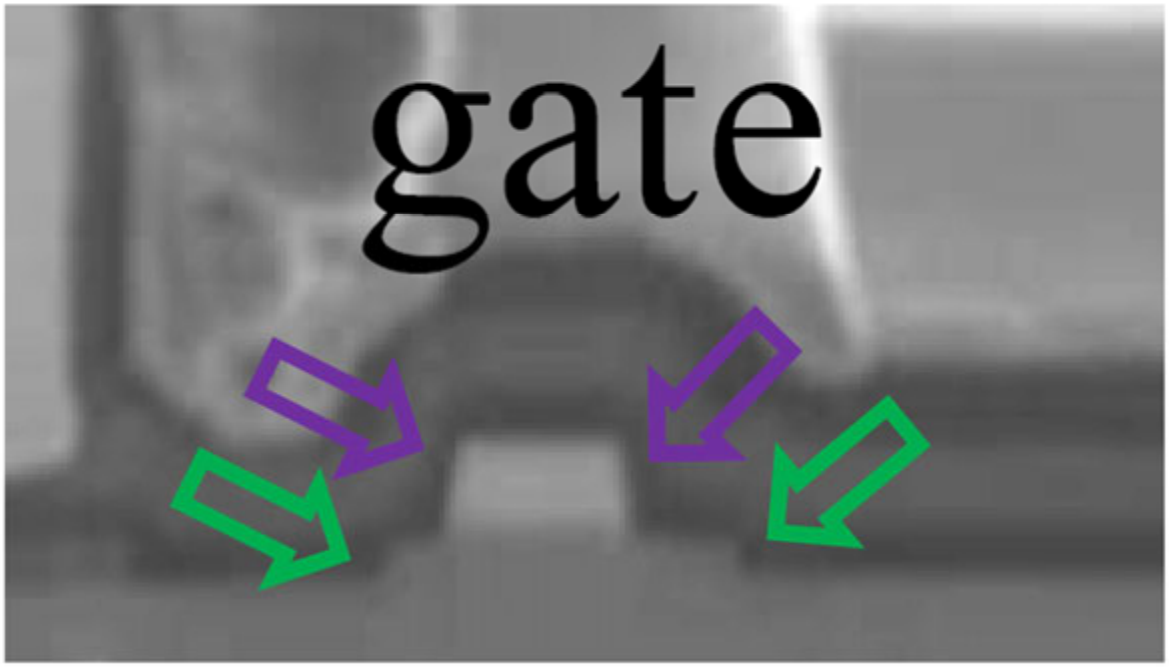


Fig.5 Cross sectional SEM image of GIT on a Si substrate.

Uemoto, Fig. 5 (microscope image).

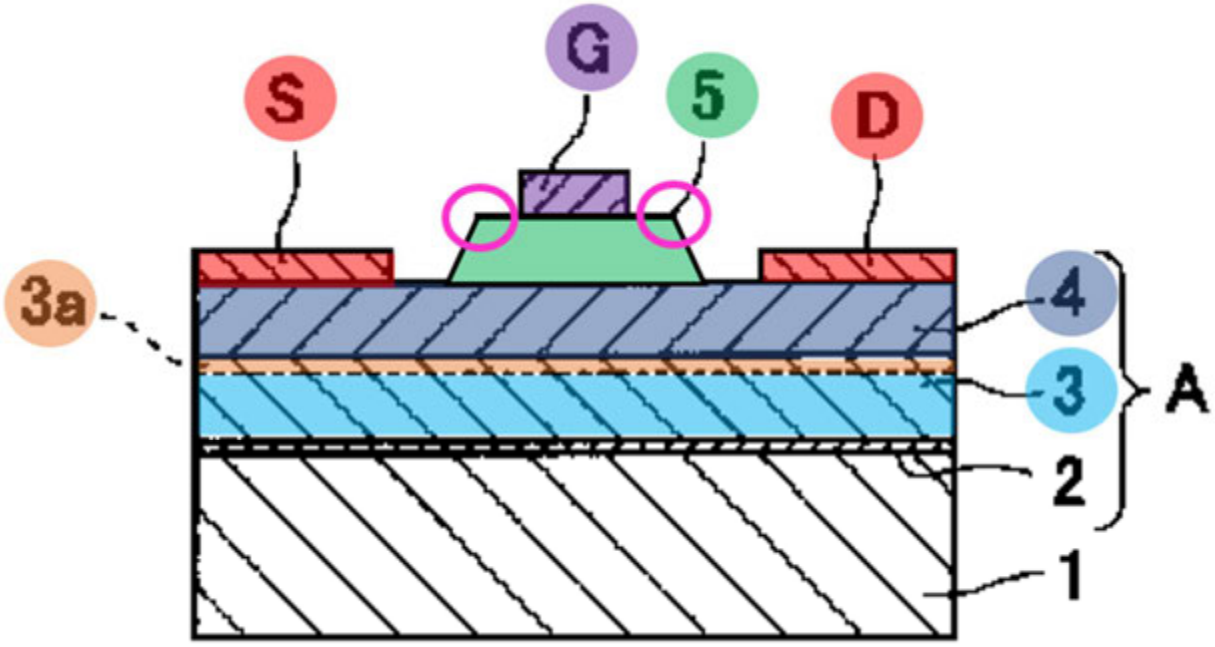


Uemoto, Fig. 5 (showing sloped sidewalls of the **p-AlGaN** layer and **gate metal**).

10. [1i]

[1i] was conventional. §VII.B.10 . Shealy, [231].

Yoshida-Saxler renders obvious [1i] under both constructions. *Id.* The combination yields the stacked, stepped gate structure having a pair of **ledges**, as shown below, and it would have been obvious over *Yoshida-Saxler* to form those ledges by masking and etching the gate metal using a single mask, as explained. §§X.A.1-X.A.2, X.B.7-X.B.9; Shealy, [197]-[209], [231].



Yoshida, Fig. 1(modified).

In addition, *Yoshida-Saxler*, *Beach* and *Shenoy* render obvious etching the gate metal to form the **ledges** of [1i] under either construction. Shealy, [232]. A POSITA would have known numerous common techniques to form the ledges of *Yoshida-Saxler* after etching the gate metal and cap layer using a single photomask, including lift-off, and would have found implementing *Beach*'s and *Shenoy*'s techniques obvious. *E.g.*, Ex. 1023; §II; Shealy, [232]. As explained, *Shenoy* discloses methods of isotropically etching the gate metal to form symmetric undercuts of a photomask. Shealy, [232]; *Shenoy*, 1-2. This technique would have generated the pair of **ledges** on *Yoshida-Saxler*'s **layer 5**. Shealy, [232]. It would have been obvious and predictable to combine *Yoshida-Saxler*'s techniques with

Beach's single mask process and *Shenoy*'s isotropic etching to arrive at the *Yoshida-Saxler* structure. §X.A.2; Shealy, [197]-[209], [232].

C. [Claim 2]

As explained, claim 2 does not further limit claim 1 because its requirements are included in [1i]. §VII.C; Shealy, [233]. *Yoshida-Saxler*, *Beach*, and *Shenoy* renders obvious claim 2 as explained for [1i]. §X.B.10; Shealy, [233].

D. [Claim 3]

The combination of *Yoshida-Saxler*, *Beach*, and *Shenoy* renders obvious Claim 3. Shealy, [234]-[237].

Beach discloses a stacked "***self-aligned*** gate arrangement" using a single photomask to etch both the "gate arrangement 24" (gate electrode) and the underlying "gate barrier 26" (GaN semiconductor) that is the same "self-aligned" process depicted in the '347 patent at Figures 6A-6B. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Ex. 1001, 4:8-20; §§III.A.1, VII.A.2, VII.A.5, (X.A.2 Shealy, [235].

Shenoy discloses etching a photomask to isotropically undercut the metal layer below the photomask that is the same process depicted in Figures 6B-6C of the '347 patent. *Shenoy*, 2-3; Ex. 1001, 4:17-33; §§III.A.1, VII.A.3, VII.A.5, X.A.2; Shealy, [236]..

It would have been obvious to use *Beach*'s self-alignment method and *Shenoy*'s undercutting techniques to predictably make *Yoshida-Saxler*'s gate structure, improving alignment. §X.A.2; Shealy, [237].

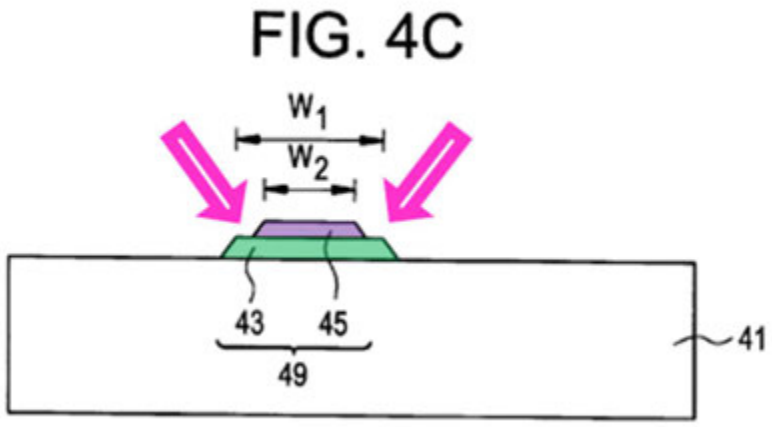
XI. Ground 5: *Yoshida* in view of *Ahn*

A. Overview of Ground 5

Yoshida and *Ahn* render claims 1-3 obvious. Shealy, [238]-[262]. A POSITA would have found it obvious to use *Ahn*'s techniques to self-align the p-type gate material and gate metal and isotropically etch the gate metal using a single mask to obtain the gate structure of *Yoshida*.

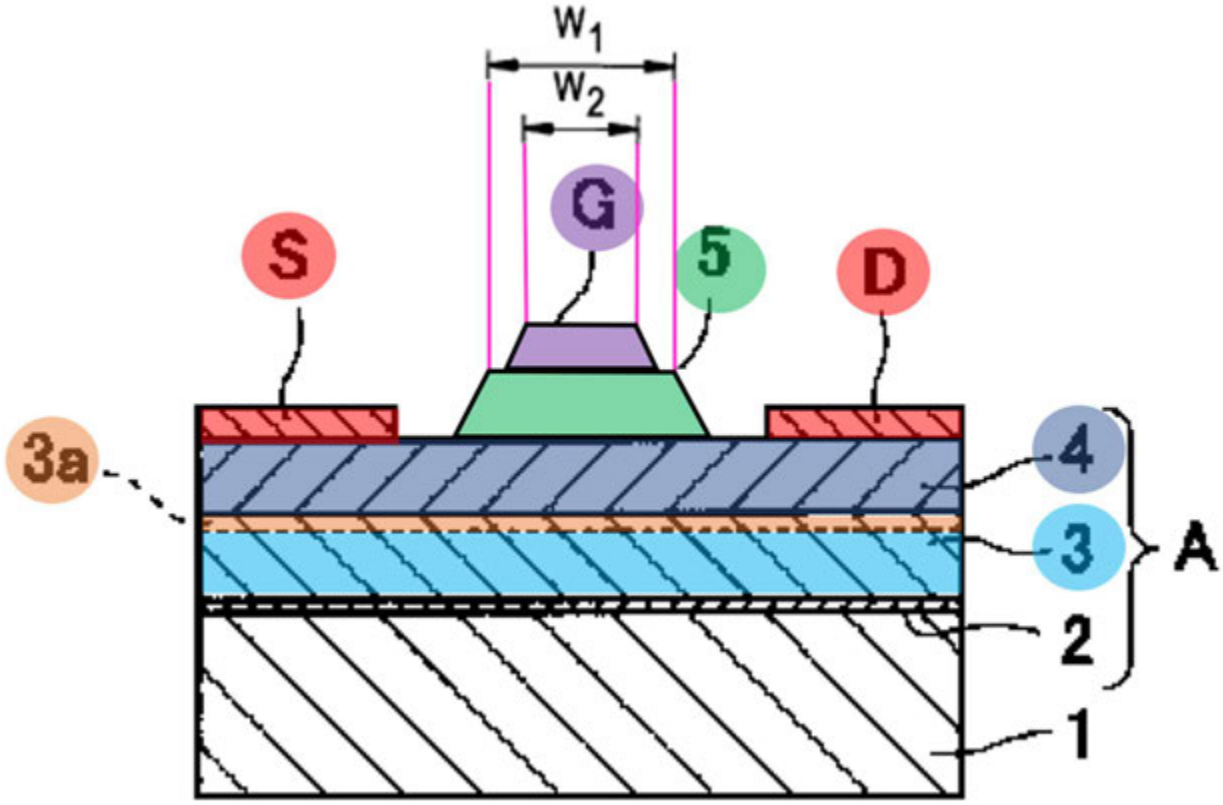
1. Ground 5: The Combination of *Yoshida* and *Ahn*

Ahn depicts sloped sidewalls of an **underlying layer** and **top gate layer** in a stacked gate structure having a pair of **ledges** on either side of the **top gate layer**. Shealy, [239]; *Ahn*, Figs. 4A-4C. *Ahn* etches layers to different thicknesses W_1 and W_2 to create those ledges, finding this structure improves performance and prevents deterioration. *Ahn*, 4:39-59, 5:21-27, 5:63-6:26, 7:24-31; Shealy, [239]. Its layers are symmetric and side surfaces preferably have an "inclined shape." *Ahn*, 6:12-37, Fig. 4C; Shealy, [239].



Ahn, Fig. 4C.

Using *Ahn*'s techniques to create *Yoshida*'s gate structure would lead to the following device, which is substantially the same as *Yoshida*'s original device but with the widths W_1 and W_2 and inclined sidewalls of *Ahn*'s device. Shealy, [240].



Yoshida, Fig. 1 (modified).

2. Ground 5: Motivation to Combine

A POSITA would have found it obvious to make the stacked gate structure of *Yoshida*'s gate electrode and layer 5 with sloped sidewalls using *Ahn*'s methods of forming a transistor gate. Shealy, [241]-[244].

A POSITA would have known many ways to create *Yoshida*'s stepped gate structure and would have used these methods interchangeably. §II; Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [242]. The '347 patent was allowed without disclosing any particular method to etch the gate metal and obtain the claimed ledges because such methods were well within the skill

level of a POSITA. Ex. 1002, 25-30, 44-55, 74-76, 80-99; §§II, III.B; Shealy, [057]-[063], [242]. Appropriate methods such as lift-off when removing the photomask or isotropic etching were well within the level of ordinary skill. §II; Shealy, [243]. As a reason for the allowance, the Examiner identified that the cited art did not disclose forming sloped sidewalls of its p-type gate material in structures that also had ledges. Ex. 1002, 29, 55. But *Ahn* would have provided a known and obvious way to create that same structure for *Yoshida*'s device. Shealy, [243]. A POSITA would have found it obvious to modify *Yoshida* by using *Ahn*'s approach for making a stepped gate in a thin-film transistor to improve alignment and precision, which would result in a stacked-stepped gate structure with sloped sidewalls. Shealy, [243] (citing *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C).

Ahn teaches many ways to obtain the *Yoshida* gate structure, including etching both simultaneously or etching them sequentially using combinations of conventional wet and dry etching techniques. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C; Shealy, [244]. For example, *Ahn* exploits differences between rates of dissolution of its layers to make the top gate layer narrower than the bottom. *Ahn*, 7:7-14-46; Shealy, [244]. A POSITA would have understood that *Yoshida*'s layer 5, which was a p-type doped semiconductor, would have had a slower rate of dissolution than its metallic gate contact and found it obvious to use *Ahn*'s approach. Shealy, [244]. *Ahn's* methods result in symmetrically aligned layers. *Ahn*, 6:15-37,

Fig. 4C; Shealy, [244]. A POSITA would have found the combination a simple substitution of *Ahn*'s known methods that would be predictably implemented when making *Yoshida*'s device to improve alignment and symmetry between layers. Shealy, [244].

B. Independent Claim 1

1. [1p]

Yoshida discloses [1p]. §X.B.1; Shealy, [245].

2. [1a]

Yoshida discloses [1a]. §X.B.2; Shealy, [246].

3. [1b]

Yoshida discloses [1b]. §X.B.3; Shealy, [247].

4. [1c]

Yoshida discloses [1c]. §X.B.4; Shealy, [248].

5. [1d]

Yoshida discloses [1d]. §X.B.5; Shealy, [249].

6. [1e]

Yoshida discloses [1e]. §X.B.6; Shealy, [250].

7. [1f]

Yoshida and *Ahn* render obvious [1f]. Shealy, [251].

Ahn forms "**photoresist 47**" over the **top gate metal** layer before etching. *Ahn*, 5:55-6:36, 7:7-46; Shealy, [252].

FIG. 4A

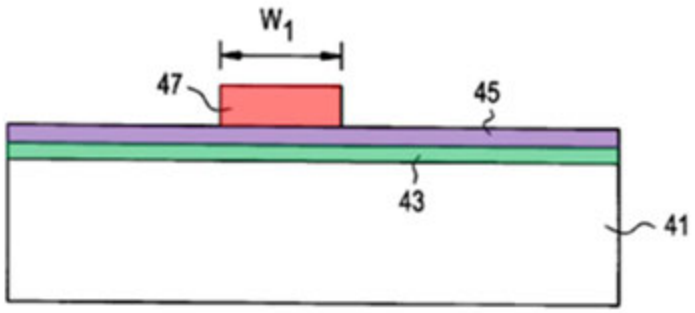
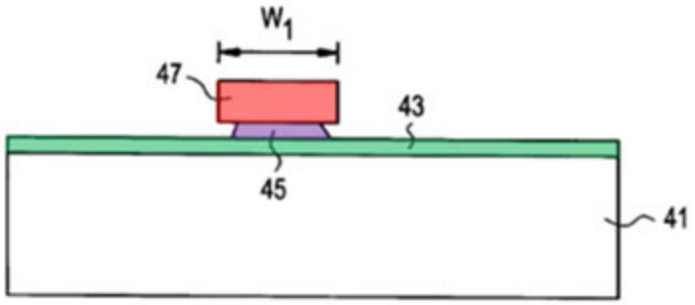


FIG. 4B



Ahn, Figs. 4A-4B.

Ahn emphasizes that the single-mask approach improves symmetry and reduces masking steps. *Ahn*, 5:55-62, 6:27-37, 7:16-46, Figs. 4A-4C; Shealy, [252].

It would have been obvious and predictable to make *Yoshida*'s gate structure with *Ahn*'s approach to using a single a photomask over the gate metal. §XI.A.2; Shealy, [241]-[244], [253].

8. [1g]

Yoshida in view of *Ahn* renders obvious [1g] under either construction. Shealy, [253]-[254].

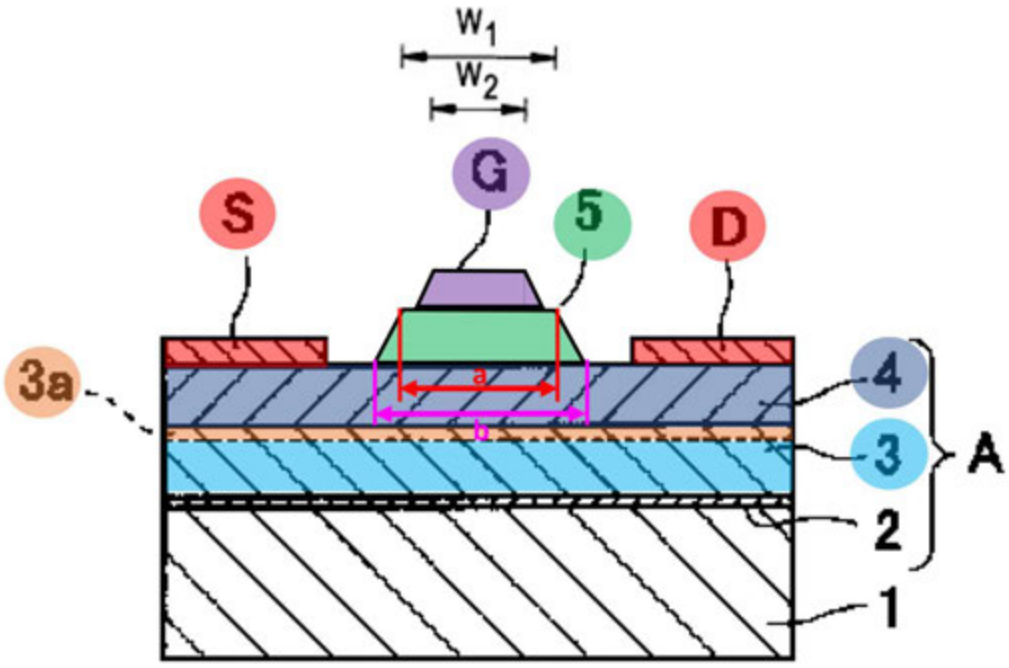
Ahn etches its top layer gate metal and its underlying layer. *Ahn*, 5:55-6:36, 7:7-46; Shealy, [254]. It would have been obvious and predictable to make *Yoshida*'s gate structure with *Ahn*'s approach of using a single a photomask over the gate metal. §XI.A.2; Shealy, [254].

9. [1h]

Yoshida and *Ahn* render obvious [1h]. Shealy, [255]-[257].

First, *Yoshida* alone renders this limitation obvious because at least slightly sloped sidewalls are common—few structures, if any, have perfectly vertical sidewalls in practice, even if depicted as vertical in functional diagrams. Shealy, [256] (citing *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5; §X.B.9).

Further, it would have been obvious and predictable to combine *Yoshida* techniques with *Ahn*'s single mask processes to differentially etch multiple metal layers to obtain a narrower gate contact and ledges on an underlying in a stacked structure, with improved reproducibility, precision, and symmetry. *Ahn*, 5:55-6:36, 7:7-46; §XI.A.2; Shealy, [241]-[244], [257]. *Yoshida-Ahn* renders the sidewalls of [1h] obvious under either parties' construction. §§VI.B, XI.A; Shealy, [257].



Yoshida, Fig. 1 (modified).

10. [1i]

Yoshida and *Ahn* also render obvious [1i] under both constructions. Shealy, [258]-[259]. *Ahn* etches its **top layer gate metal** under a **photoresist** such that is narrower than the **underlying layer** to form a pair of **ledges** on either side of the **top gate metal**. *Ahn*, 5:55-6:36, 7:7-46; Shealy, [258].

FIG. 4A

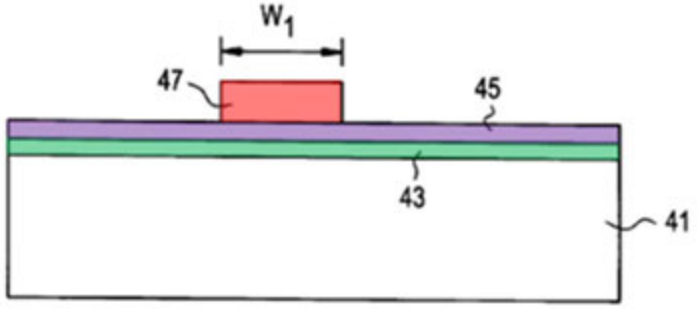


FIG. 4B

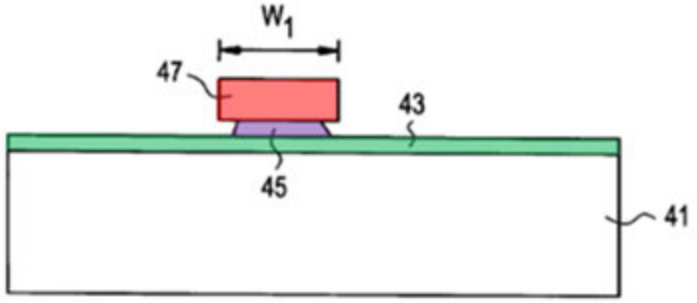
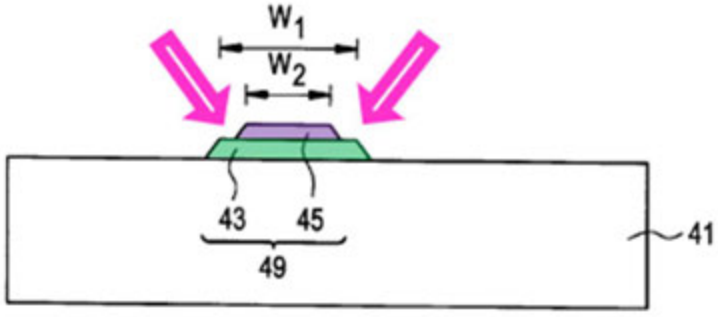


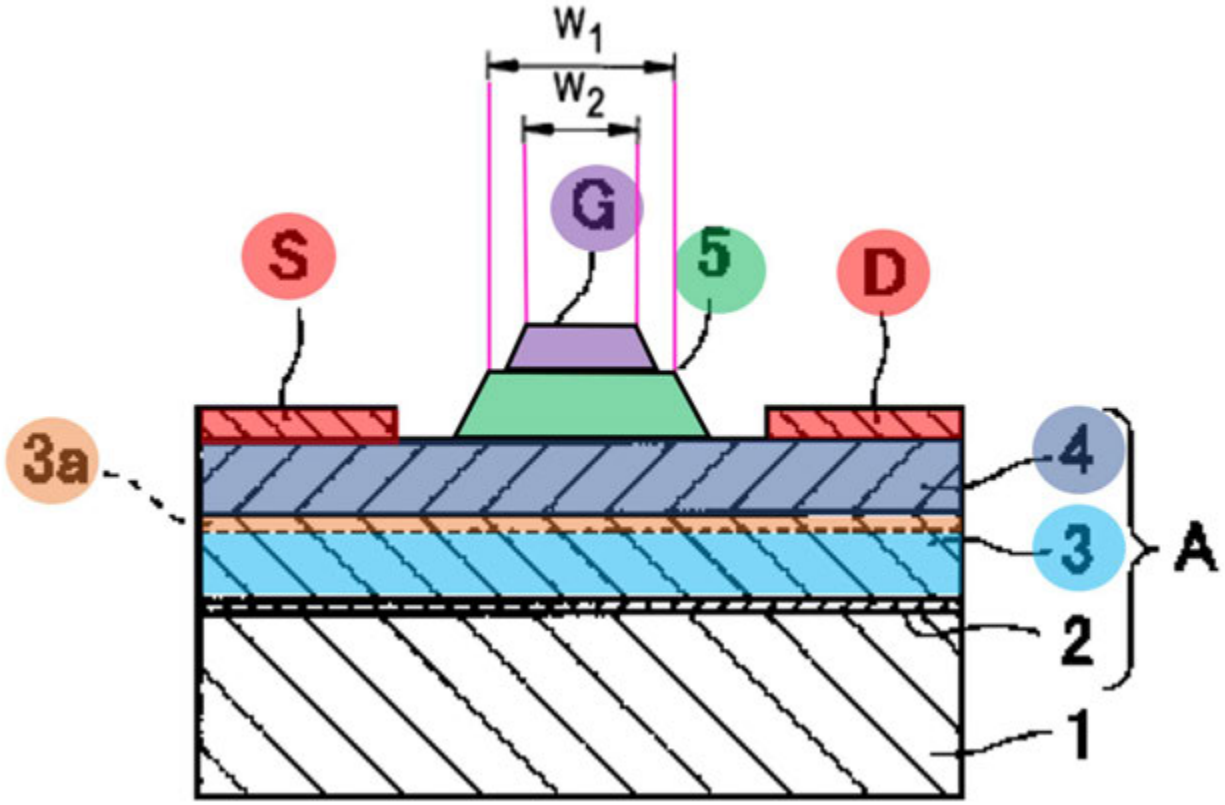
FIG. 4C



Ahn, Figs. 4A-4C.

It would have been obvious to combine *Yoshida*'s techniques with *Ahn*'s single mask processes to differentially etch multiple metal layers and obtain a

narrower gate contact and ledges on an underlying in a stacked structure. *Ahn*, 5:55-6:36, 7:7-46; §XI.A.2; Shealy, [259].



Yoshida, Fig. 1 (modified).

C. [Claim 2]

As explained, claim 2 does not further limit claim 1 because its requirements are included in [1i]. §VII.C; Shealy, [260]. *Yoshida* and *Ahn* render obvious claim 2 as explained for [1i]. §XI.B.10; Shealy, [260].

D. [Claim 3]

Yoshida and *Ahn* render obvious Claim 3. Shealy, [261]-[263].

Ahn uses a **single mask** to etch a gate having a **top metal layer** and **underlying layer** with horizontal **ledges**, which is a "self-aligned" process. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C; Shealy, [261]. It discloses multiple ways to etch two layers under a single photomask and arrive at this same stacked, stepped gate structure. *Ahn*, 7:7-46; Shealy, [262].

FIG. 4A

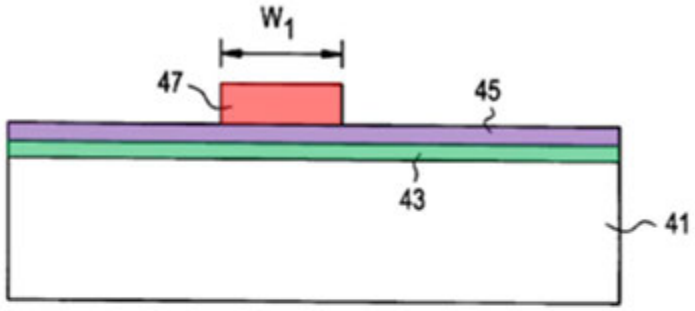
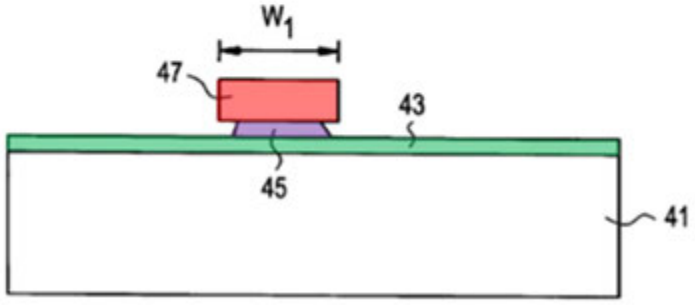
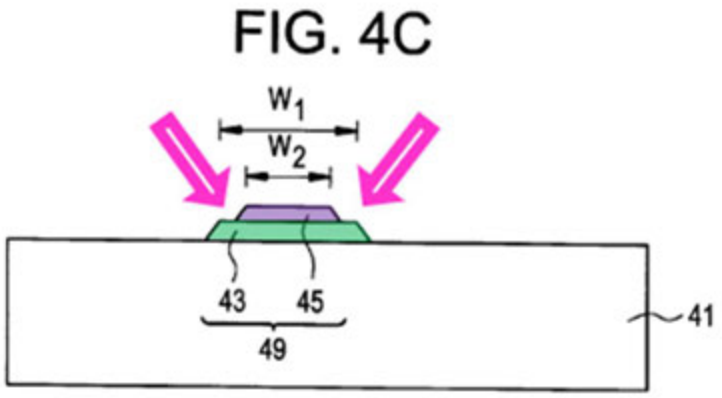


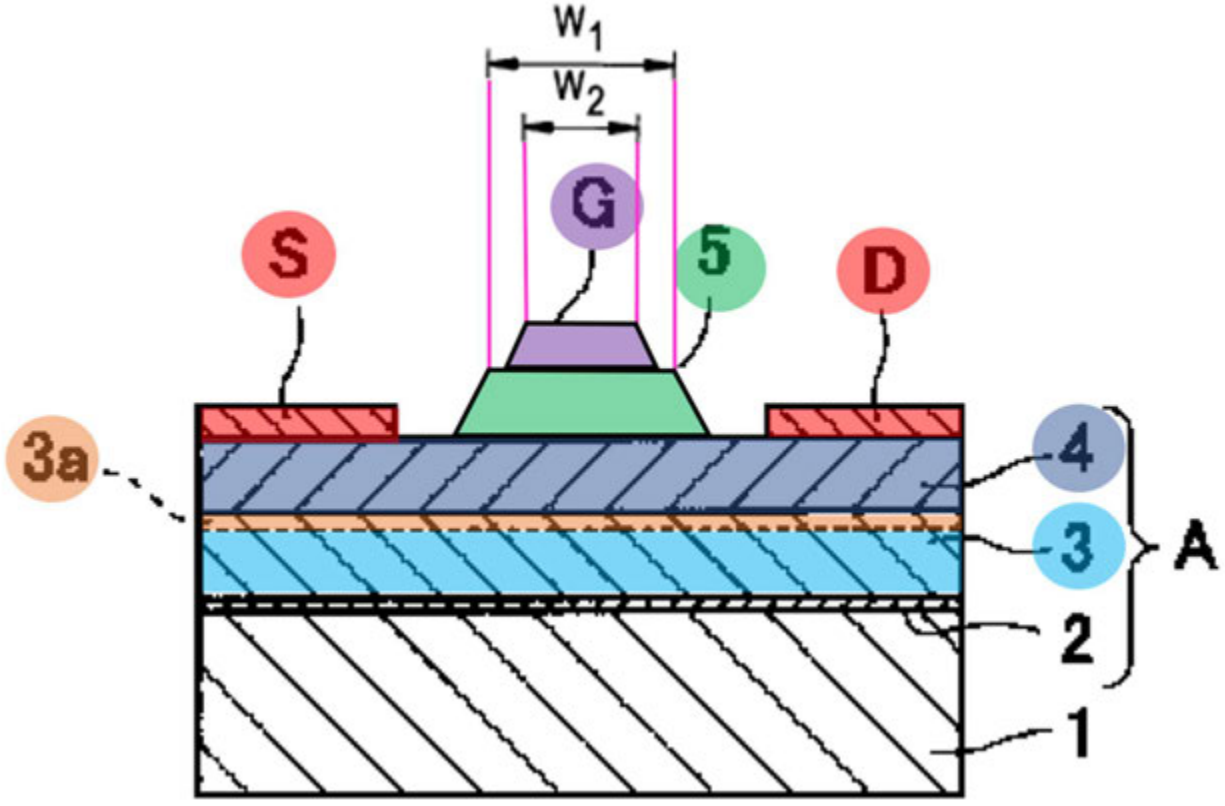
FIG. 4B





Ahn, Figs. 4A-4C.

It would have been obvious and predictable to combine *Yoshida*'s techniques with *Ahn*'s single-mask, self-aligned processes to differentially etch multiple metal layers to obtain sloped edges in a stacked structure. *Ahn*, 5:55-6:36, 7:7-46; §XI.A.2; Shealy, [241]-[244], [263].



Yoshida, Fig. 1 (modified).

XII. Discretionary Denial Is Not Warranted

A. *Fintiv* Denial Is Improper

In view of the Office's interim guidance dated June 21, 2022 ("Interim Procedures"), *Fintiv* does not apply to this case. The Interim Procedures state "the PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding," so the parallel ITC Investigation does not implicate *Fintiv*. Interim Procedures, 7.

Moreover, the *Fintiv* factors in view of the parallel district court action weigh strongly in favor of institution because the district court case has minimal investment from the Court or Parties, does not have a trial date, and has been stayed. *Efficient Power Conversion Corp. v. Innoscience (Zhuhai) Tech. Co.*, No. 2:23-cv-04026, Dkt. 26 (C.D. Cal. July 27, 2023).

B. 35 U.S.C. § 325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017), favor institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8-11 (PTAB Feb. 13, 2020) (precedential).

Advanced Bionics, step 1, and *Becton, Dickinson* factors (a), (b), and (d) favor institution because none of the references in this Petition were before the Office

during prosecution. Ex. 1002; Ex. 1001. The references are also not cumulative of the prosecution prior art because cited art teaches all claims.

In a forthcoming EPR request, Petitioners intend to challenge the '335 patent's priority claim to *Lidow* and earlier patent applications for inequitable conduct. §III.B. Any such EPR does not weigh against institution of this IPR Petition because the proceedings present no overlap in issues or grounds—this IPR assumes priority to April 8, 2009. *Id.*

XIII. Mandatory Notices

A. Real Party-in-Interest

Petitioners and real parties-in-interest are Innoscience (Suzhou) Technology Company, Ltd., Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc.

B. Related Matters

To the best of Petitioners' knowledge, the '347 patent is involved in:

Name	Number	Court	Filed
Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd.; Innoscience, Inc.; Innoscience America, Inc.	2:23-cv-04026-AB-AS	CDCA	May 24, 2023
In the Matter of Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same	337-TA-1366	ITC	May 26, 2023

The '347 patent is related to U.S. Patent Nos. 8,404,508; 8,890,168; and 10,312,335.

C. Lead and Back-Up Counsel

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Petitioners consent to electronic service at the email addresses listed above.

XIV. Standing

The ’347 patent is available for IPR and Petitioners are not barred or estopped from requesting IPR.

XV. Conclusion

Petitioners request institution of *inter partes* review and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: September 20, 2023

/Lionel M. Lavenue/
Lionel M. Lavenue (Reg. No. 46,859)
Lead Counsel

CLAIM APPENDIX

1. **[1p]** A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

[1d] depositing a p-type gate material on the barrier layer;

[1e] depositing a gate metal on the p-type gate material;

[1f] forming a photoresist over the gate metal;

[1g] etching the gate metal and the p-type gate material,

[1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

[1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

2. The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.

3. The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.

37 C.F.R. § 42.24(D) CERTIFICATION

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), Petitioner certify that this petition complies with the requirements of 37 C.F.R. § 42.24. Excluding parts of this Petition exempted under § 42.24(a), this Petition contains 13,927 words, as measured by the word-processing system used to prepare this paper.

Dated: September 20, 2023 By: /Lionel Lavenue/
Lionel Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), the undersigned certifies that on September 20, 2023, a copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent 9,748,347, the associated Powers of Attorney, and Exhibits 1001-1011, 1014-1023, 1025-1029, were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's Patent Center website for the '347 patent:

Dipu Doshi
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1825 Eye Street, NW
Washington, DC 20006

Dated: September 20, 2023

By:/Daniel E. Doku/
Daniel E. Doku
Litigation Legal Assistant
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, LLP