Before the Honorable Clark S. Cheney
Chief Administrative Law Judge

In the Matter of **CERTAIN SEMICONDUCTOR DEVICES, AND METHODS OF MANUFACTURING SAME AND PRODUCTS CONTAINING THE SAME**	**Investigation No. 337-TA-1366**

RESPONDENTS' POST-HEARING INITIAL BRIEF

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TABLE OF ABBREVIATIONS

Abbr.	Full description
HEMT	high electron mobility transistor
2DEG	two-dimensional electron gas
GaN	gallium nitride
Si	silicon
Mg	magnesium
AlGaN	aluminum gallium nitride
MOCVD	metal-organic chemical vapor deposition
H	hydrogen
V	volt
MOSFET	metal-oxide-semiconductor field-effect transistor
N	nitride
Tr. __	Transcript of Evidentiary Hearing, February 26-March 1, 2024
Markman Tr. __	Transcript of Markman Hearing and Case Management Conference, October 13, 2023

TABLE OF FREQUENTLY CITED EXHIBITS

Ex. No.	Full description
JX-0014	U.S. Patent No. 8,350,294
JX-0015	U.S. Patent No. 8,404,508
RX-0073	U.S. Patent Application Publication No. 2008/0087915A1 to Uemoto et al. ("*Uemoto*")
RX-0011	U.S. Patent Application Publication No. 2006/0145189A1 to Beach ("*Beach189*")
RX-0079	Japanese Patent Application Publication No. JP2006253224A to Kigami et al. ("*Kigami*")
RX-0041	U.S. Patent Application Publication No. 2006/0273347 to Hikita et al. ("*Hikita*")
RX-0288	U.S. Patent No. 7,238,560 to Sheppard et al. ("*Sheppard*")
RX-0286	International Patent Application Publication No. WO 2005/057624 to Beach ("*Beach624*")

AGREED UPON NOMENCLATURE FOR '508 CLAIM 1[1]

Claim	Limitation
[1pre]	A method of forming an enhancement mode GaN transistor, the method comprising:
[1a]	nucleating and growing transition layers on a substrate;
[1b]	growing an III Nitride EPI layer over the transistor layers;
[1c]	growing an III Nitride barrier layer over the EPI layer;
[1d]	growing a GaN layer with acceptor type dopants over the barrier layer;
[1e]	depositing a gate contact layer on the doped GaN layer;
[1f]	applying a gate photo resistant pattern;
[1g]	etching away the gate contact layer outside the gate region;
[1h]	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
[1i]	removing the gate photo resistant pattern;
[1j]	depositing a dielectric layer;
[1k]	applying a contact photo resistant pattern;
[1l]	etching the dielectric layer to open the drain and source contact area;
[1m]	removing the contact photo resistant pattern;
[1n]	depositing an Ohmic contact metal;
[1o]	applying a metal photo resistant pattern;
[1p]	etching the Ohmic contact metal;
[1q]	removing the metal photo resistant pattern; and
[1r]	performing rapid thermal annealing to form Ohmic drain and source contacts.

[1] CALJ Cheney: "Why don't y'all put some kind of translation in your brief so that I know the nomenclature that's used at trial in comparison to what your opponent used so that I can compare apples to apples." Tr. 62:18-21.

GROUND RULE 14.1 CERTIFICATION

Counsel for Respondents certifies this post-hearing initial brief, which addresses those issues on which Respondents bear the burden of proof, complies with the word-count limit set by Ground Rule 14.1 and includes 19,963 words as measured by the word count feature of Microsoft Word.

Respondents will address in its post-hearing responsive brief those issues and evidence raised in the post-hearing initial briefs of Complainant and the Commission Investigative Staff. *See* Ground Rule 14.2. Respondents may also address any other issues in accordance with the Chief Administrative Law Judge's instructions given during the evidentiary hearing. Tr. 1263:2-7.

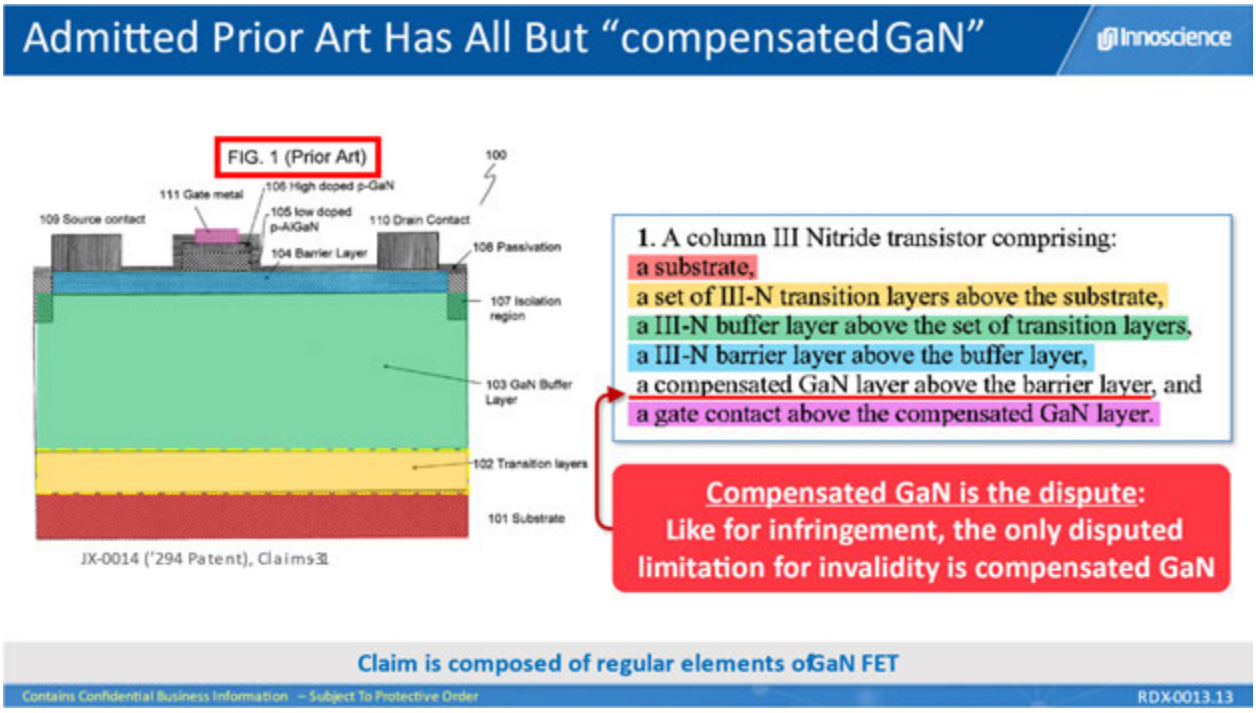
I. INTRODUCTION AND BACKGROUND: BOTH ASSERTED PATENTS ARE INVALID IN VIEW OF PRIOR ART

Complainant EPC alleges infringement of two patents, U.S. Patent Nos. 8,350,294 ("the '294 patent") and 8,404,508 ("the '508 patent"), but both patents are invalid in view of the prior art, precluding a finding of violation.

A. The '294 Patent Is Invalid in View of Prior Art

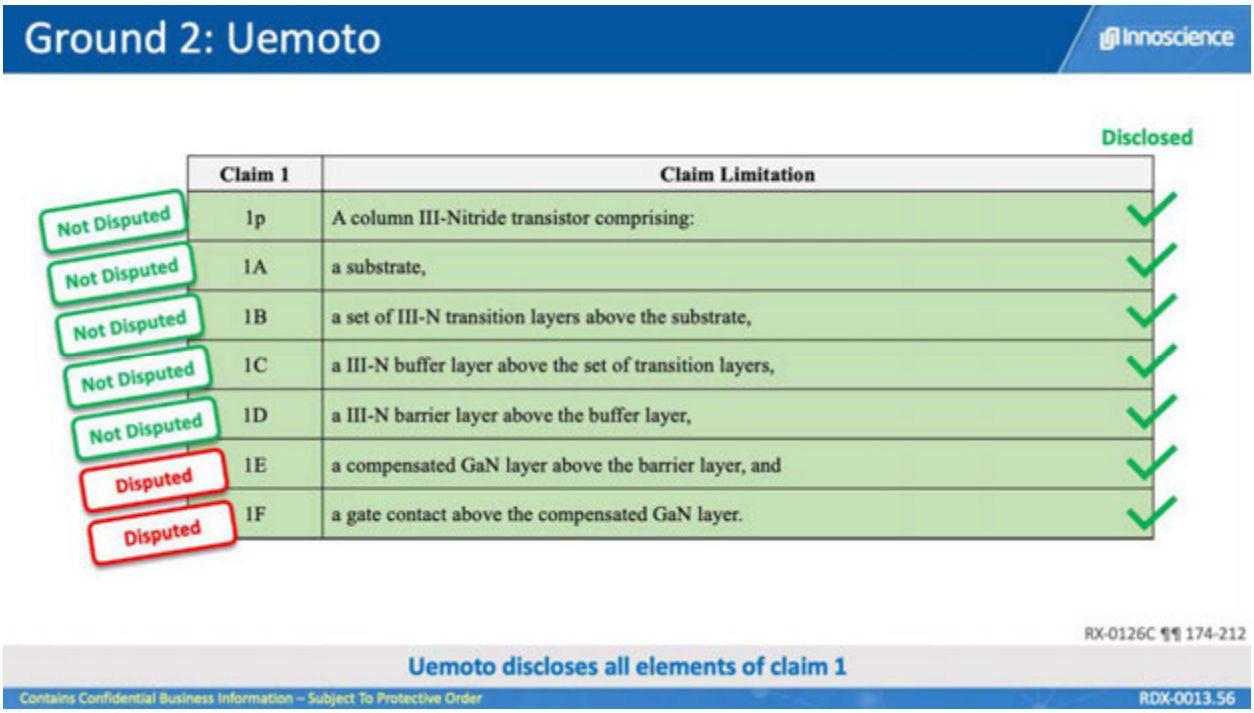
1. All Elements of the '294 Patent Are *Admitted* Prior Art Except "Compensated GaN Layer," Which Was Well Known in the Art

First, the ***'294 patent*** claims a narrow, ultimately impractical, change over otherwise admitted prior art. The patent claims the use of an insulating "compensated GaN layer" instead of a conductive p-type GaN (pGaN) layer in a GaN based transistor to reduce gate leakage current (hereinafter "gate leakage" or "leakage"). But the prior art shows that the "compensated GaN layer" approach of the '294 patent was not new and, at best, was an obvious modification to existing devices. Forming compensated GaN layers and incorporating compensated GaN layers into transistors were known for many years before the '294 patent. For example, years before the '294 patent was filed, while working for a previous employer, one of the inventors (Dr. Robert Beach) of the '294 patent had applied for a patent (*Beach189*), which also used a "compensated GaN" layer. This inventor never disclosed his previous application to the USPTO during the '294 patent examination, but his previous patent application—undisputedly prior art—explicitly discloses use of a "compensated GaN" in a transistor. And other prior art also demonstrates that the structure of the '294 patent and the claimed use of hydrogen to passivate GaN (and create a "compensated GaN layer") was well known.



RDX-0013.13

As Dr. Lebby explained during the Evidentiary Hearing, and EPC did not dispute, the only disputed element of claim 1 of the '294 patent is the "compensated GaN layer" present in claim elements [1e] and [1f]. Tr. (Lebby) 851:1-13; *see also id.* 856:25-4; 876:17-24; *see generally* Tr. (Schubert) 947:17-957:9. The prior art, specifically (1) *Uemoto* and (2) *Beach189* discloses this "compensated GaN layer," along with the other elements, and therefore invalidates claim 1. Further, (1) *Uemoto* and (2) *Beach189* in view of *Kigami* discloses all elements of claims 2 and 3. As shown in the figures below, and as will be described in the following sections, *Uemoto* renders obvious claims 1-3.



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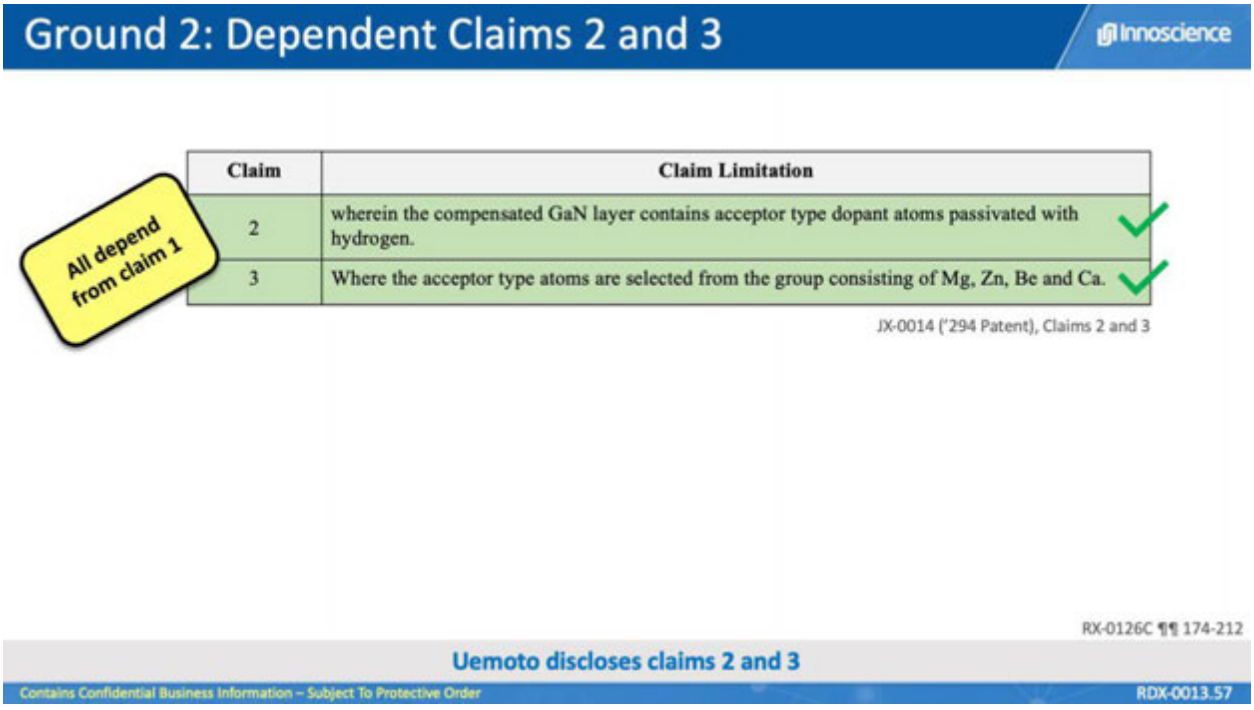

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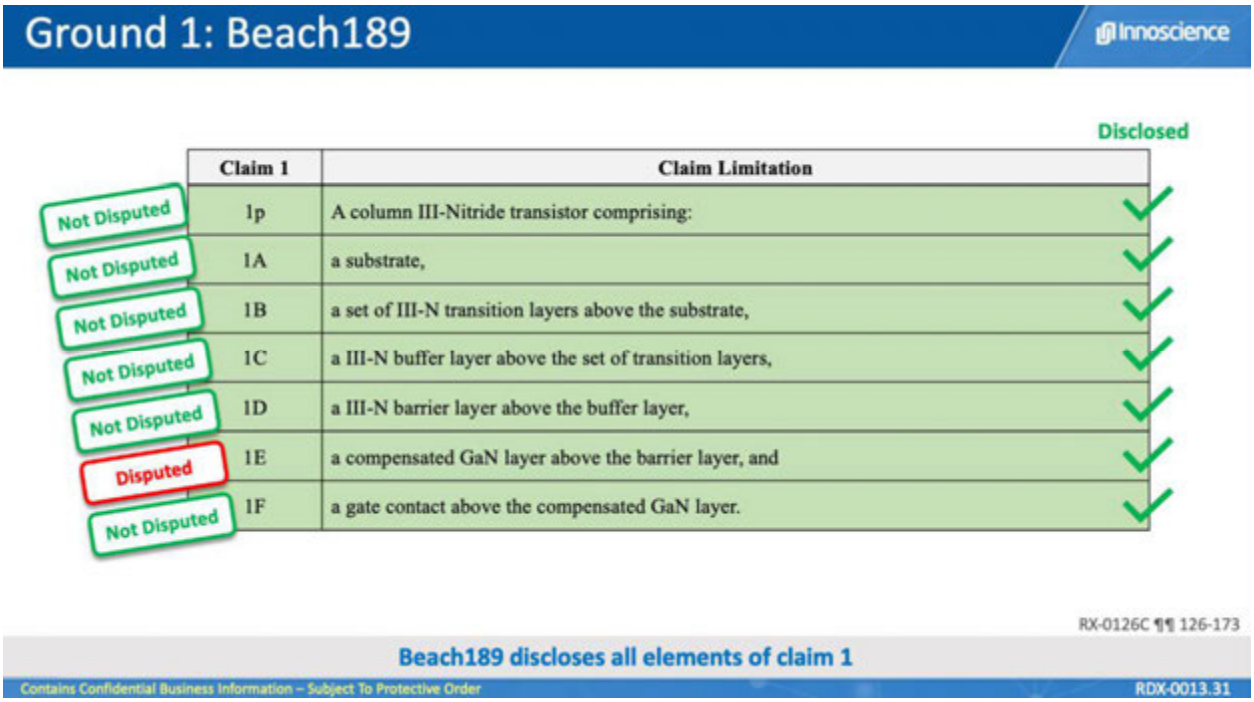
And, as shown in the figure below, and as will be described in the following sections, *Beach189* also discloses all elements of claim 1.

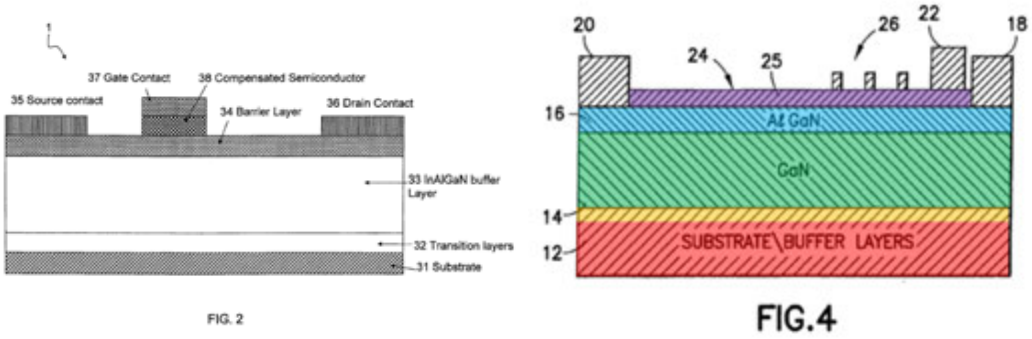


RDX-0013.31

Therefore, the '294 patent is invalid over the prior art.

2. EPC's Expert *Agrees* "Compensated GaN" Is Found in Prior Art

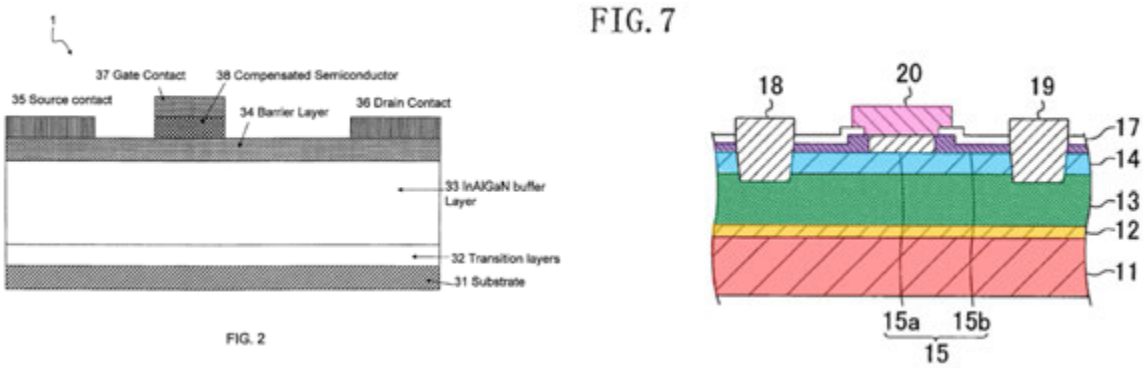
During the Evidentiary Hearing, Dr. Lebby testified that both *Beach189* and *Uemoto* disclose the single disputed element of the '294 patent. As shown in the two figures below, *Beach189* explicitly discloses this allegedly novel "compensated GaN layer." On the left, Figure 2, from the '294 patent, discloses a "compensated semiconductor 38." JX-0014 Fig 2. On the right, Figure 4, from *Beach189*, discloses this same compensated GaN layer 25 by referring to this layer with the unicorn words, "compensated GaN." RX-0011 ¶ [0026] ("[U]ltra resistive field plate 25 [is] formed with a highly electrically resistive material, such as . . . ***compensated GaN***)" (emphasis added).



RDX-0013.11; JX-0014 Fig. 2 (left); RDX-0013.23; RX-0011 Fig. 4 (right) (annotated)

EPC's argument is that the "compensated GaN" of *Beach189* is different from the "compensated GaN" of the '294 patent, even though both references use the exact same unicorn words and describe the material in the same way. Tr. (Schubert) 950:16-951:8. In describing the features of this layer, the '294 patent states that the "compensated semiconductor layer 38 is a highly compensated semi-insulating material." JX-0014 3:47-48. And as Dr. Lebby described during the Evidentiary Hearing, the ultra resistive field plate 25 of *Beach189*, which is made from compensated GaN, is also semi-insulating. Tr. (Lebby) 938:15-939:4. Therefore, *Beach189* invalidates claim 1.

In addition, *Uemoto* discloses the disputed "compensated GaN layer," as shown in the two figures below. As described above, Figure 2 of the '294 patent discloses "compensated semiconductor 38." JX-0014 Fig 2. Shown below, Figure 7, from *Uemoto*, discloses the same compensated GaN layer 15b. RX-0073 Fig. 7. As Dr. Schubert admitted, this "layer 15b is gallium nitride, contains magnesium and hydrogen, is passivated, and is non-conductive. So in that sense, it meets the claim term 'compensated gallium nitride.'" Tr. (Schubert) 1033:21-1034:7.



RDX-0013.11; JX-0014 Fig. 2 (left); RDX-0013.53; RX-0073 Fig. 7 (right) (annotated)

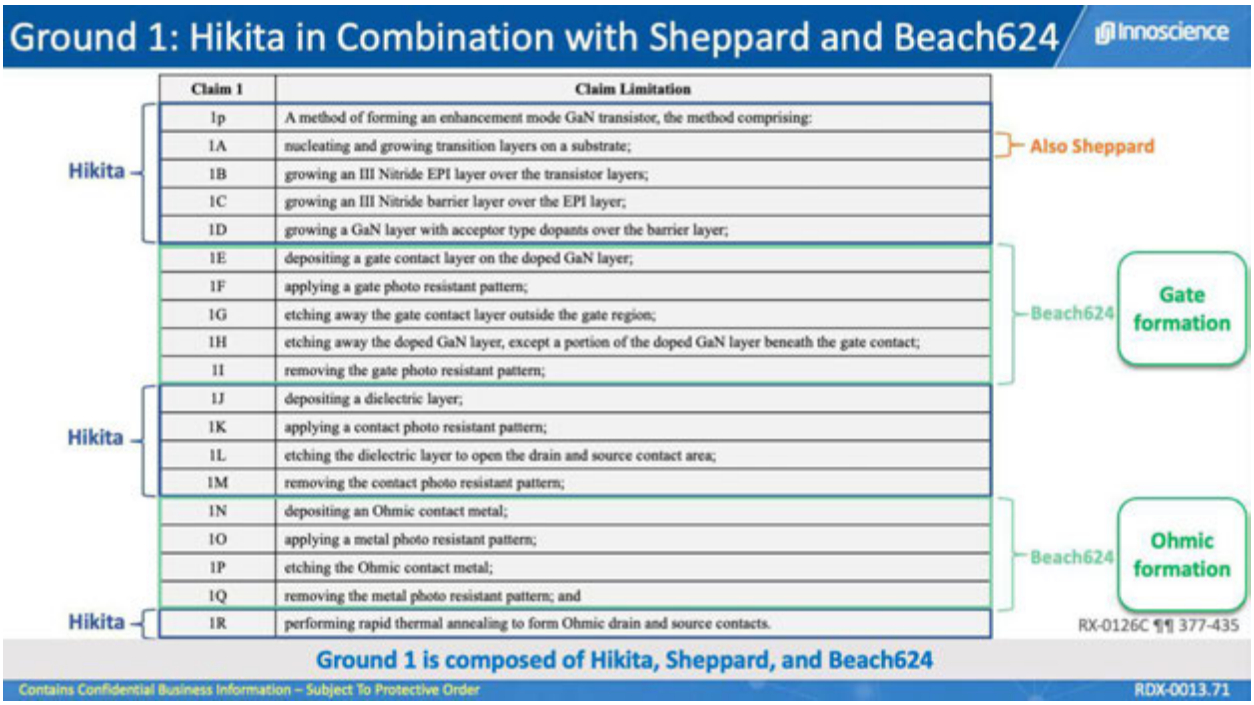
EPC does not dispute that *Uemoto* discloses a compensated GaN layer. Tr. (Schubert) 964:1-7, 1033:21-1034:7. Instead, EPC incorrectly argues that 15b is not under the gate contact. But Dr. Schubert ***admitted*** that at least "a sliver of region 15B" ***is under*** gate electrode 20. Tr. (Schubert) 965:3-19 ("[T]he gate electrode is above a small region of layer 15b."); *see also id.* 966:21-24. Based on Dr. Schubert's own testimony, region 15b is under the gate contact, and thus satisfies the requirements of claim 1, making claim 1 invalid in view of *Uemoto*.

B. The '508 Patent Is Also Invalid in View of Prior Art

1. All Elements of the '508 Patent Were Known in the Art

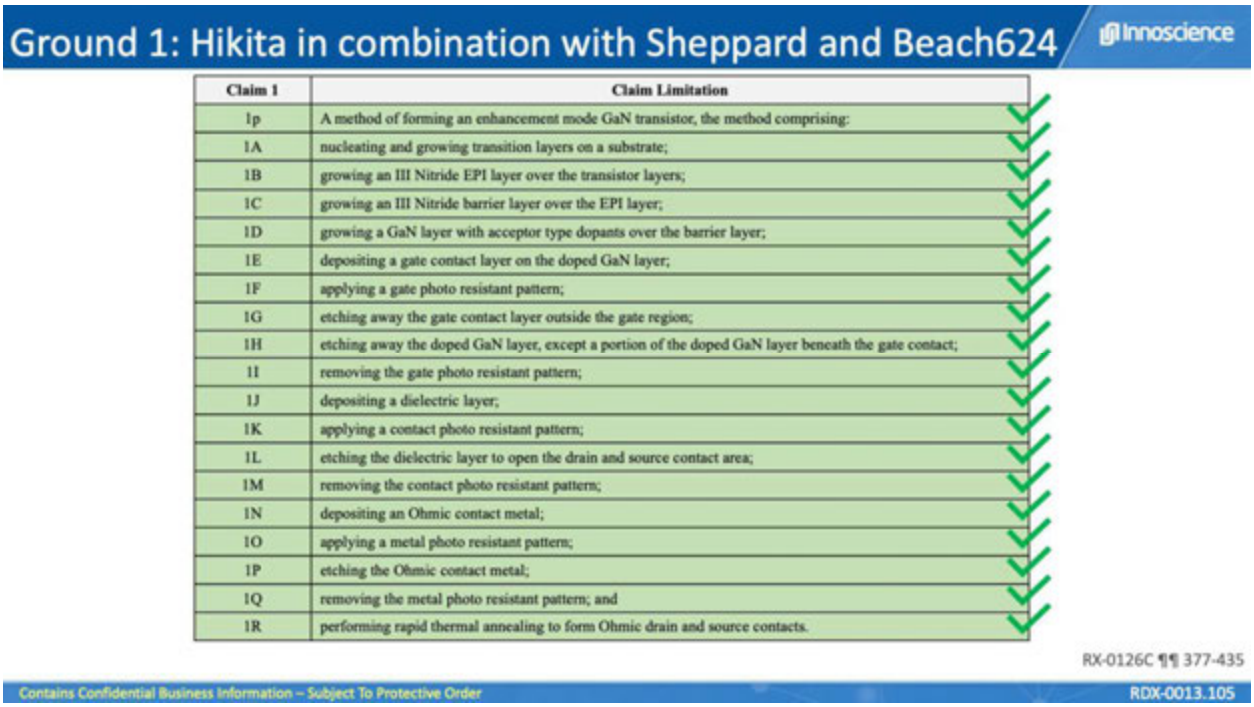
Turning second to the ***'508 patent***, this patent is entirely about a prior art device, the known normally-off GaN transistor. Rather than claiming a new device, the '508 patent claims a specific allegedly new method of manufacture, one way (but not all ways) to make a "self-aligned" gate wherein the gate metal and the underlying p-type GaN layer are etched together and thus their edges are aligned to each other. But self-aligned processes had been used in the manufacture of transistors for decades. Indeed, Robert Beach had previously used the same "self-aligned" technique, aligning the gate contact and doped GaN layer to each other, as shown by *Beach624*.

As Dr. Lebby explained during the Evidentiary Hearing, all elements of claim 1 can be found in the prior art, specifically, *Hikita*, *Sheppard*, and *Beach624*. Tr. (Lebby) 895:6-913:21. The figure below shows where each element of claim 1 can be found in the prior art.



RDX-0013.71

As shown in the figure below, *Hikita, Sheppard*, and *Beach624* show that the method of the '508 patent was obvious over the prior art.



RDX-0013.105

2. EPC's Expert *Agrees* All Elements of Asserted Claim 1 Are Found in Prior Art

While the '508 patent appears more complex at first glance, claim 1 is simply comprised of elements that were known in the prior art, as shown by the figures above. Even EPC admits as much, and instead only argues (1) the '508 patent allegedly teaches a gate-first process, (2) *Beach624* discloses using separate gate photo resistant and metal photo resistant patterns, and (3) there is a lack of motivation to combine *Hikita* and *Beach624*. Tr. (Schubert) 972:12-23; 1004:5-11. None of these three arguments rebut the clear and convincing evidence the combination renders the claim obvious.

With respect to (1), EPC ***never proposed*** a construction of claim 1 that required the claim elements to occur in a specific order, and the claim itself does not require a gate first process. The only order the patent emphasizes is the order of the gate stack itself, which EPC argues can be performed in ***any*** order. EPC's contradictory, and late, position on "gate first" is wrong.

With respect to (2), EPC provides a narrow reading of *Beach624,* assuming incorrectly that one photoresist pattern must be used to form the gate and ohmic contacts simultaneously. But the figures show two different photoresist patterns are used to separately form the gate and ohmic contact. RDX-0013.102; RX-0286 Figs. 1D, 1E. Further, nothing in the claim limits these patterns from being applied simultaneously, so this attack is a strawman.

Finally, with respect to number (3), EPC misinterprets the combination and applies an incorrect analysis that is contrary to the law. In particular, EPC does not attack Dr. Lebby's actual combination, but rather Dr. Schubert's "understanding" of the combination. This "understanding" incorrectly assumes the gate would be deposited after, or on top of, the dielectric layer. But *Hikita*, as Dr. Lebby explained, describes etching the doped GaN layer **before** depositing a dielectric layer. Tr. (Lebby) 910:3-14; Tr. (Schubert) 996:13-20; RX-0041, ¶ [0061] ("The source electrode 409, the drain electrode 410 and the gate electrode 411 may be formed before formation of the SiN film 408"); Figs. 8C, 8D. That ordering is preserved in Dr. Lebby's combination, but not Dr. Schubert's manufactured "understanding." Indeed, on cross examination, Dr. Schubert acknowledged that *Hikita* disclosed depositing the dielectric layer **after depositing the gate metal**. Tr. (Schubert) 1029:14-1030:7. As all the elements of the only asserted claim were known in the art, and EPC's attacks on the motivations to combine fail, claim 1 is invalid as obvious.

As the evidence shows and as summarized herein, both asserted patents are invalid. Innoscience respectfully requests that the CALJ so hold.

C. Procedural History of the Investigation

This Investigation instituted on July 3, 2023, based on EPC's May 26, 2023 Complaint, as supplemented, which alleged infringement of certain claims of U.S. Patent Nos. 8,350,294 (''the '294 patent''); 8,404,508 (''the '508 patent''); 9,748,347 (''the '347 patent''); and 10,312,335 (''the '335 patent''). 88 Fed. Reg. 42756 (Jul. 3, 2023). On December 13, 2023, and February 12,

2024, the CALJ issued Order Nos. 9 and 12, respectively granting EPC's motions to terminate the '347 patent and the '335 patent from the investigation. EPC continues to assert claims 1-3 of the '294 patent and claim 1 of the '508 patent.

The Evidentiary Hearing took place on February 26 through March 1, 2024. The Final Initial Determination is currently due June 3, 2024, and the Target Date is October 3, 2024.

D. The Private Parties

1. Respondents

Innoscience (Zhuhai): Innoscience (Zhuhai) Technology Company, Ltd. Is a Chinese corporation that has a principal place of business and headquarters at No. 39, Jinyuan 2nd Road, High-Tech Zone, Zhuhai, Guangdong, 519099 China.

Innoscience America: Innoscience America, Inc. is a California corporation that has its principal place of business at 5451 Great America Pkwy, Ste 125, Santa Clara, CA 95054.

Innoscience (Zhuhai) and Innoscience America are collectively referred to as "Innoscience" or "Respondents" herein.

2. Complainant

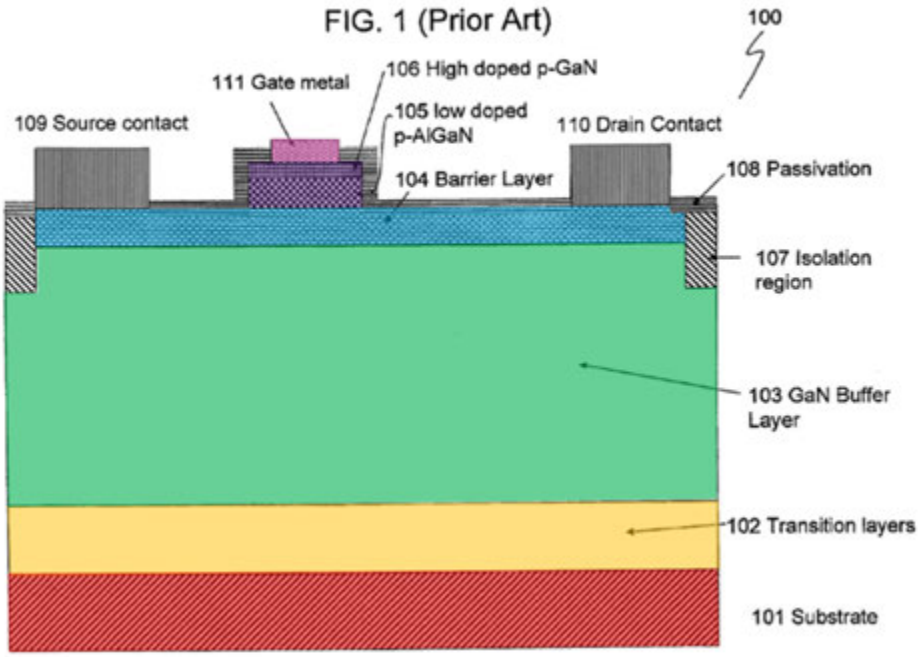
Complainant Efficient Power Conversion Corporation ("Complainant" or "EPC") is a Delaware corporation with its headquarters and principal place of business located at 909 N. Pacific Coast Highway, Suite 230, El Segundo, CA 90245.

E. The Patents-at-Issue

1. Overview of the '294 Patent: All Elements Are *Admitted* as Prior Art, Except "Compensated GaN"

The '294 patent issued on January 8, 2013. JX-0014 Cover. The patent issued from an application that was submitted on April 8, 2010, which claimed priority to provisional application 61/167,792 submitted on April 8, 2009. *Id.*

The ’294 patent relates to a “transistor with a compensated GaN layer or a semi-insulating GaN layer below the gate contact and above the barrier.” JX-0014 1:16-18. The ’294 patent concedes that GaN transistors were “prior art.” JX-0014 1:55-2:2, Fig. 1. The ’294 patent also concedes that “conventional enhancement mode GaN transistor[s]” formed with a **substrate**, **transition layers**, **buffer layer**, **barrier layer**, **p-type layers**, and contacts for **gate** and **source/drain** were known in the prior art. JX-0014 1:55-2:2. Figure 1 of the ’294 patent, which is labeled “Prior Art” and reproduced with color coding below, illustrates the admitted prior art.



RDX-0012C.12; RDX-0013.13; JX-0014 FIG. 1

The ’294 patent describes Figure 1 as “a cross-section of a prior art transistor” for “a conventional enhancement mode GaN transistor device.” JX-0014 1:55-2:23. The ’294 patent describes the Admitted Prior Art (“APA”) as including a “**substrate 101** that can be composed of silicon (Si), silicon carbide (SiC), sapphire, or other material, **transition layers 102** typically composed of AlN and AlGaN that is about 0.1 to about 1.0 μm in thickness, **buffer material 103** typically composed of GaN that is about 0.5 to about 10 μm in thickness, **barrier material 104**

typically composed of AlGaN where the Al to Ga ratio is about 0.1 to about 0.5 with thickness from about 0.005 to about 0.03 μm, **p-type AlGaN 105, heavily doped p-type GaN 106**, … and **gate metal 111** typically composed of a nickel (Ni) and gold (Au) metal contact over a **p-type GaN gate**." JX-0014 1:55-2:9.

The '294 patent purports to address leakage issues in APA transistors, stating that forming a "compensated" or a "semi-insulating" layer "below the gate contact" could reduce leakage. JX-0014 2:3-9, 3:17-21, 3:63-67. The patent pinpoints its "invention" as the formation of a compensated layer through passivation, emphasizing that "[t]he critical step . . . that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen." JX-0014 3:43-45. Tr. (Schubert) 433:7-22; *see also* Tr. (Lidow) 103:2-19.

The '294 patent presents different transistor embodiments that include either "compensated" or "semi-insulating" layers. The first embodiment has a **substrate**, **transition**, **buffer**, **barrier**, gate of (elements the patent notes were already present in conventional prior art transistors), and a "**[c]ompensated semiconductor layer 38** [that] preferably comprises AlGaN or GaN with a deep level passivated p-type impurity" below the gate (substituting a p-type layers). JX-0014 3:10-11. Figure 2, reproduced and color-coded below, illustrates the first embodiment which includes such a compensated semiconductor layer:

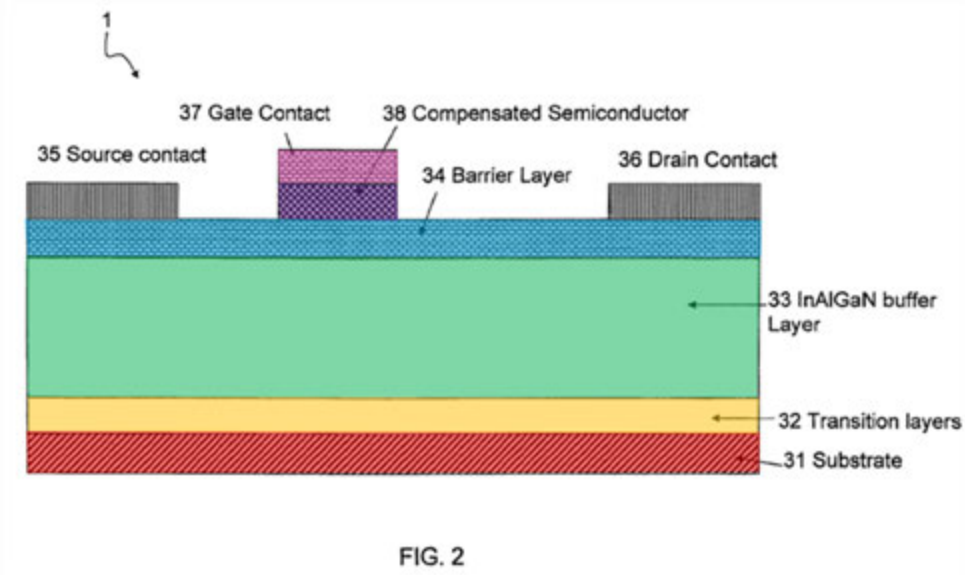


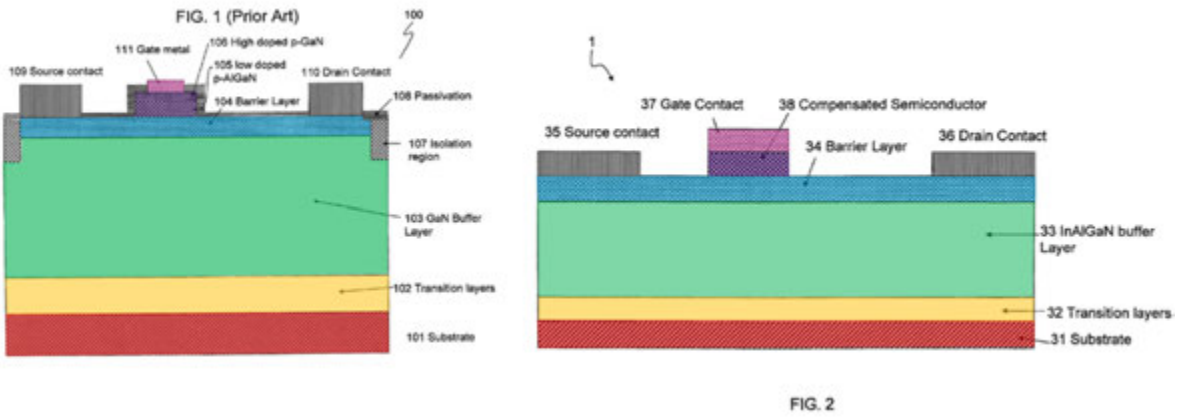
FIG. 2

JX-0014 Fig. 2

As the patent notes, the only notable difference between the APA and the alleged invention in this embodiment is the use of a passivation step to compensate the capping layer below the gate metal; the other relevant features remain the same. JX-0014 3:43-52. Specifically, the patent identifies a passivation step for the formation of the compensated layer as the key element distinguishing from the prior art, stating that "[t]he critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen." JX-0014 3:43-45.

Comparing the first embodiment with the APA, both shown in the figures below, illustrates this minor difference. On the right, the alleged invention includes a "compensated semiconductor" layer (labeled as element 38) under the gate contact. The APA structure on the left, however, includes doped p-type layers (labeled as elements 105 and 106). The substrate, transition layers, buffer layer, barrier layer, and gate metal, remain the same between the two structures.[2]

[2] Figures 1 and 2 also have a different label for the buffer layer, with FIG. 1 labeling "103 GaN Buffer Layer" while FIG. 2 labels "33 InAlGaN buffer layer." But the labeling only reflects an embodiment of the patent and refers to a generic formulation. JX-0014 2:63-65. The patent and



RDX-0012C.12; RDX-0013.13; JX-0014 Figs. 1 (left) and 2 (right)

The second, third, and fourth embodiments of the ’294 patent are substantially similar to the first embodiment, except they include “a semi-insulating layer 39 in place of the compensated semiconductor layer 38” (JX-0014 3:56-57) and, optionally, “a confinement layer . . . above the semi-insulating layer” (JX-0014 4:32-33) or “a spacer layer 49 beneath semi-insulating layer” (JX-0014 4:65-66). These additional embodiments relate solely to variations of the layers between the gate metal and the barrier layer.

EPC asserts claims 1-3 of the ’294 patent. The asserted claims are reproduced below:

Claim	Limitation
[1pre]	A column III Nitride transistor comprising:
[1a]	a substrate,
[1b]	a set of III-N transition layers above the substrate,
[1c]	a III-N buffer layer above the set of transition layers,
[1d]	a III-N barrier layer above the buffer layer,
[1e]	a compensated GaN layer above the barrier layer, and
[1f]	a gate contact above the compensated GaN layer.
[2pre]	The transistor of claim 1,
[2a]	wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
[3pre]	The transistor of claim 2,

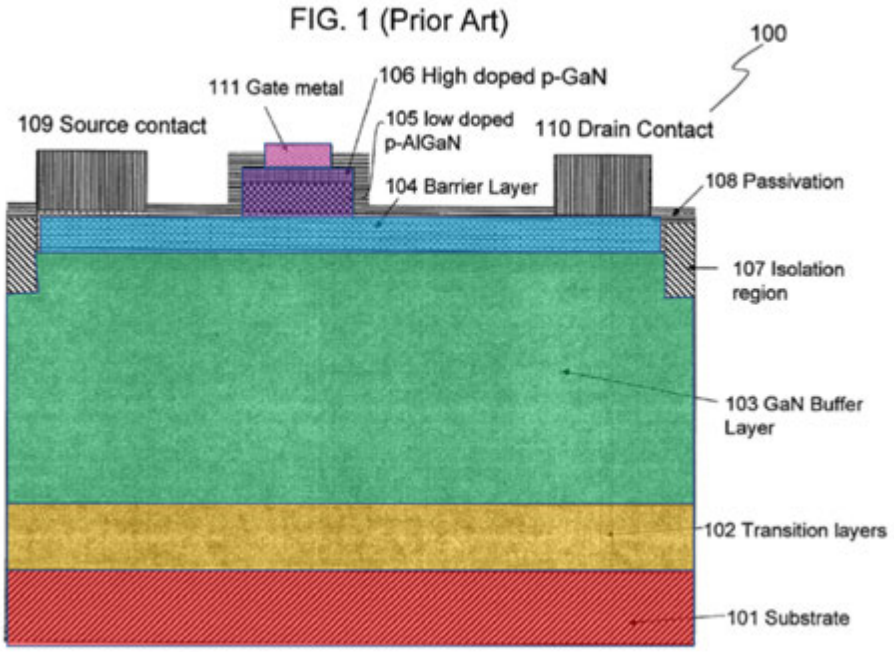
claims are clear the buffer layer is “made of a III Nitride material,” which “can be composed of $In_xAl_yGa_{1-x-y}N$ where $x+y \leqq 1$,” including GaN. JX-0014 3:12-15.

Claim	Limitation
[3a]	where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.

2. Overview of the '508 Patent: The Device Itself Is Admitted Prior Art, While the "Present Invention" Is About the Process of Self-Aligning the Gate Metal and Doped GaN Materials

The '508 patent issued on March 26, 2013. JX-0015 Cover. The patent issued from an application that was filed on April 8, 2010, and claims priority to a provisional application that was filed on April 8, 2009. *Id.* The '508 patent is entitled "Enhancement mode GaN HEMT device and method for fabricating the same."

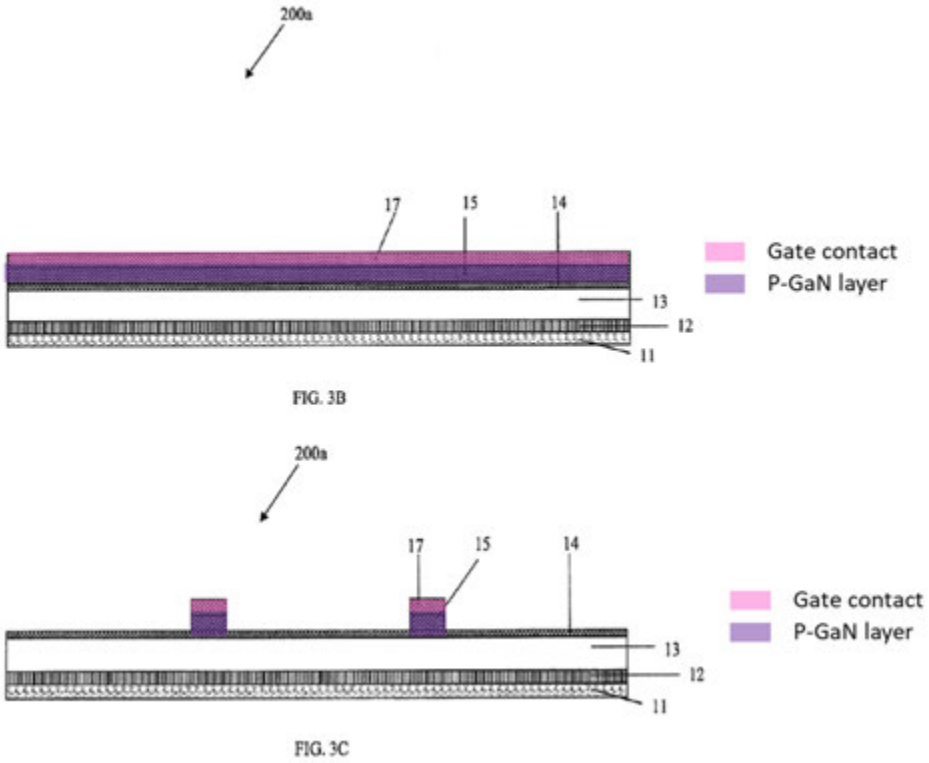
The '508 patent admits the basic features of an enhancement-mode GaN transistor were conventional and well known, as Figure 1 below shows. JX-0015 1:32-64. The '508 patent describes "a conventional enhancement mode GaN transistor device 100 which includes substrate 101 which can be either sapphire or silicon, transition layers 102, un-doped GaN material 103, un-doped AlGaN material 104, source ohmic contact metal 109, drain ohmic contact metal 110, p-type AlGaN or p-type GaN material 105, heavily doped p-type GaN material 106, and gate metal 111." JX-0015 1:58-64.



RDX-0013.69; JX-0015 Fig. 1 (annotated)

The ’508 patent is instead directed to a method of forming a GaN-based transistor by self-aligning a doped GaN layer with the gate contact. The specification makes clear that using a self-aligned process to form the doped GaN layer and gate contact is essential to the purported invention of the ’508 patent. *See* JX-0015 Abstract (“[T]he gate III-V compound and the gate metal are **formed with a single photo mask process to be self-aligned** and the bottom of the gate metal and the top of the gate compound have the same dimension.”), 2:15-17 (“It would be desirable to provide an enhancement mode GaN transistor structure with a **self-aligned gate** which avoids the above-mentioned disadvantages of the prior art.”), 3:1-6 (“The present invention is an enhancement mode GaN HEMT device with a gate metal material and a doped GaN or AlGaN material that are **self-aligned**, and a method for making such a device. The materials are **patterned and etched using a single photo mask**, which reduces manufacturing costs.”).

The ’508 patent states, “**The present invention is** an enhancement mode GaN HEMT device with **a gate metal material and a doped GaN or AlGaN material that are self-aligned**, and a method for making such a device.” JX-0015 3:1-4. To achieve self-alignment, the patent explains that “[t]he materials are patterned and etched using a single photo mask.” JX-0015 3:4-6. Figures 3B and 3C below illustrate a self-aligned process in which gate metal 17 and p-type GaN gate layer 15 are self-aligned.



RDX-0013.89; JX-0015 Figs. 3B, 3C (annotated)

In every embodiment provided by the ’508 patent, the doped GaN layer and gate contact are self-aligned, which the ’508 patent describes as having the same dimension at the point of contact of these layers. *See* JX-0015 Abstract (“[T]he gate III-V compound and the gate metal are formed with a single photo mask process to be self-aligned and the **bottom of the gate metal and the top of the gate compound have the same dimension**.”), 3:10-17, 4:6-10, 4:20-25, 4:55-59, 5:4-17, 5:23-30, 5:38-45, 5:52-58, 5:61-6:1, 6:15-21, Figs. 2, 3A-3E, 4, 5A-5E, 6, 7A-7F, 8-12.

In addition to structures with the same dimension at the point of contact between the gate contact and doped GaN layer, the ’508 patent also describes embodiments in which additional etching of the gate contact is performed after first forming a self-aligned gate contact and doped GaN layer. *See* JX-0015 Figs. 9, 10, 12. The ’508 patent makes clear that in those embodiments the gate contact and doped GaN layer are self-aligned at an intermediate step of the process before additional etching of the gate contact is performed. JX-0015 5:38-45 (fifth embodiment), 5:52-58 (sixth embodiment), 6:15-21 (eighth embodiment).

EPC asserts claim 1 of the ’508 patent. The asserted claim is reproduced below:

Claim	Limitation
[1pre]	A method of forming an enhancement mode GaN transistor, the method comprising:
[1a]	nucleating and growing transition layers on a substrate;
[1b]	growing an III Nitride EPI layer over the transistor layers;
[1c]	growing an III Nitride barrier layer over the EPI layer;
[1d]	growing a GaN layer with acceptor type dopants over the barrier layer;
[1e]	depositing a gate contact layer on the doped GaN layer;
[1f]	applying a gate photo resistant pattern;
[1g]	etching away the gate contact layer outside the gate region;
[1h]	etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
[1i]	removing the gate photo resistant pattern;
[1j]	depositing a dielectric layer;
[1k]	applying a contact photo resistant pattern;
[1l]	etching the dielectric layer to open the drain and source contact area;
[1m]	removing the contact photo resistant pattern;
[1n]	depositing an Ohmic contact metal;
[1o]	applying a metal photo resistant pattern;
[1p]	etching the Ohmic contact metal;
[1q]	removing the metal photo resistant pattern; and
[1r]	performing rapid thermal annealing to form Ohmic drain and source contacts.

II. U.S. PATENT NO. 8,350,294

A. Claim Construction for the '294 Patent: Compensated GaN Is at Least Nonconductive or Semi-Insulating

The parties dispute the construction of the term "compensated GaN layer" as recited in element [1e] of claim 1 of the '294 patent. The proposed constructions are:

Term	EPC	Innoscience	Staff
"a compensated GaN layer" (Claim 1, '294 Patent)	A semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor) Not a "product-by-process" limitation.	"a doped GaN layer formed with a step to passivate its impurities" which is a "product-by- process" limitation.	"a GaN layer in which one type of impurity cancels the electric effects of another type of impurity"

At the Markman Hearing, the CALJ provided preliminary opinions on the term's construction. The CALJ indicated he is "not inclined to construe this as a product-by-process claim" and "not inclined to insert gate material into the construction." Markman Tr. 136:2-4. The CALJ also signaled he is inclined to apply a plain and ordinary meaning, indicating that he is "inclined to just use the words of the claim" and suggested the term's construction "is just going to be plain and ordinary meaning and you have a fact dispute over whether enough compensation has happened." *Id.* 136:9-13, 291:15-18.

Although the parties do not agree on the plain and ordinary meaning of "compensated GaN layer," the parties agree on what a "compensated GaN layer" is not: it is undisputed that conductive p-type GaN ("pGaN") is not "compensated GaN." The parties agree that a "compensated GaN" is passivated and a nonconductive or semi-insulating p-type GaN ("pGaN"). CDX-0002C.3; Tr. (Schubert) 433:7-22.

B. Invalidity of the ’294 Patent: Both Grounds Invalidate All Three Asserted Claims

The evidence shows that the asserted claims of the ’294 patent are invalid under 35 pre-AIA U.S.C. §§ 102 and 103.

1. Priority Date

The relevant priority date for the ’294 patent, as well as the date from which to apply the perspective of a POSITA for the ’294 patent, is April 8, 2009. JX-0014 Cover. Thus, pre-AIA 35 U.S.C. § 102 applies.

2. Level of Ordinary Skill

A POSITA for both the ’294 and ’508 patents would have had at least a bachelor’s degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Tr. (Lebby) 847:16-848:9. This definition is undisputed as EPC did not present a different definition during the Evidentiary Hearing.

3. Overview of the Prior Art

The following references, either alone or in combination, invalidate claims 1-3 of the ’294 patent:

- **RX-0073:** U.S. Patent Application Publication No. 2008/0087915A1 to Uemoto et al. (“*Uemoto*”)
- **RX-0011:** U.S. Patent Application Publication No. 2006/0145189A1 to Beach (“*Beach189*”)
- **RX-0079:** Japanese Patent Application Publication No. JP2006253224A to Kigami et al. (“*Kigami*”)

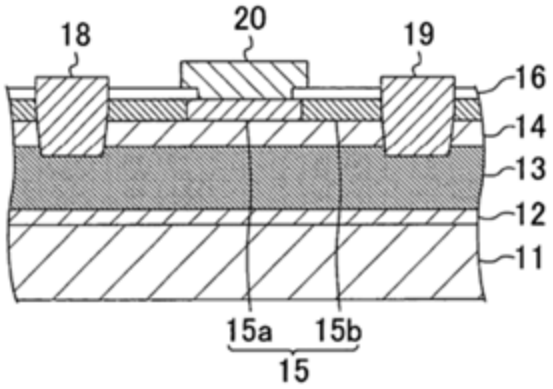
Each of the above references qualifies as prior art.

a. *Uemoto* (US2008/0087915A1, RX-0073)

Uemoto is a U.S. patent publication published on April 17, 2008, that was filed on July 24, 2007. RX-0073 Cover. Thus, *Uemoto* is prior art under pre-AIA § 102(a), as EPC does not dispute. *See* Tr. (Schubert) 949:8-19.

Uemoto discloses III-nitride transistors formed with multiple nitride layers, and it describes the formation of transistors with source, gate, and drain electrodes. RX-0073 ¶¶ [0031]-[0035]; Tr. (Lebby) 873:21-874:2. Figure 1 below illustrates an embodiment of a transistor structure discussed in *Uemoto*.

FIG. 1



RDX-0013.43; RX-0073 Fig. 1

According to *Uemoto*, the layer 15 can be formed having two regions: a control region 15a (with active impurities) and a highly resistive region 15b (where hydrogen inactivates or passivates impurities). RX-0073 ¶¶ [0015], [0033], FIG. 1. *Uemoto* discloses that the selective formation of the high resistive region 15b with hydrogen diffusion reduces leakage current between the gate and the drain and improves the transistor performance by making it more stable. *Id.* ¶¶ [0059], [0063]-[0064], Figs. 7-8.

b. *Beach189* (US2006/0145189A1, RX-0011)

Beach189 is a U.S. patent application publication that published on July 6, 2006. RX-0011 Cover. Thus, *Beach189* is prior art under pre-AIA § 102(b), as EPC does not dispute. The inventor of *Beach189* is the same inventor Robert Beach identified on the '294 patent. *Compare* RX-0011 Cover *with* JX-0014 Cover. During the examination of the '294 patent, however, Robert Beach did not disclose his previous *Beach189* patent application to the USPTO. JX-0014 Cover; *see generally* JX-0004.

Beach189 relates to a III-nitride transistor, describing "a III-nitride heterojunction power semiconductor device" and a "typical III-nitride power semiconductor device [that] includes a drain electrode, a source electrode and a gate electrode [that] controls the current." RX-0011 ¶¶ [0002]-[0003]. *Beach189* describes a method to improve the transistor's performance using a "field relaxation feature [that] includes an ultra resistive field plate." RX-0011 ¶¶ [0004]-[0006]. *Beach189* discloses that the "ultra resistive field plate 25" is "formed with a highly electrically resistive material, such as, silicon rich SiN, ***compensated GaN*** or the like material." RX-0011 ¶ [0026] (emphasis added); *see also* RX-0011 Claim 7 ("field plate is comprised of a compensated III-nitride semiconductor"). In FIG. 4, reproduced below, *Beach189* illustrates an embodiment showing such a field plate (element 25), along additional elements such as a substrate, buffer layers, and gate electrode. RX-0011 ¶¶ [0026], [0040]-[0044].

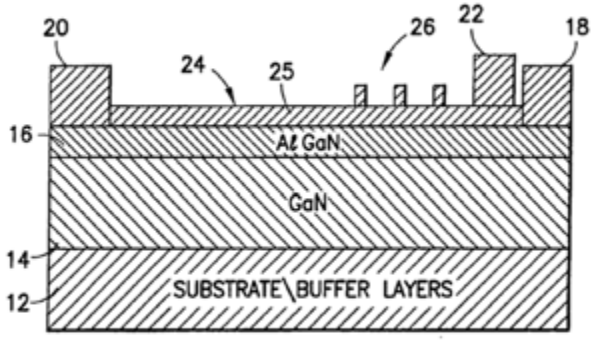


FIG.4

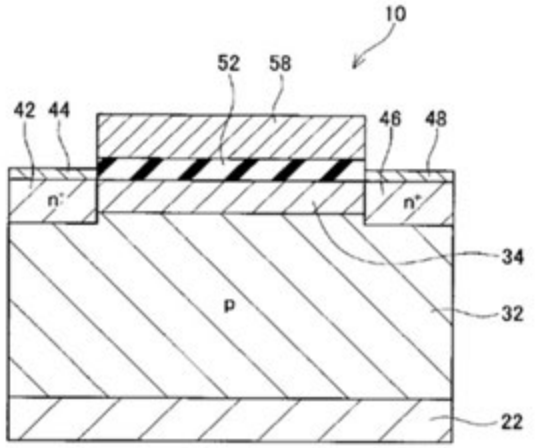
RDX-0013.19-25; RX-0011 Fig. 4

c. *Kigami* (JP2006253224A, RX-0079)

Kigami is a Japanese patent application publication published on September 21, 2006. RX-0079 Cover. Thus, *Kigami* is prior art under pre-AIA § 102(b).

Kigami discloses normally-off III-nitride transistors. RX-0079 ¶¶ [0001]-[0005]. *Kigami* teaches that III-nitride transistors can be improved by introducing hydrogen into GaN layers to passivate impurities. RX-0079 ¶¶ [0007], [0022]. *Kigami* discloses techniques to introduce hydrogen in GaN layers using an ionized hydrogen gas. RX-0079 ¶ [0026], Fig. 5. *Kigami* describes that the introduced hydrogen forms a composite with magnesium, inactivating the magnesium impurities, improving the breakdown, frequency, and threshold characteristics. RX-0079 ¶¶ [0007], [0022], [0023], [0029]. Figure 1, reproduced below, illustrates *Kigami*'s transistor structure.

FIG. 1



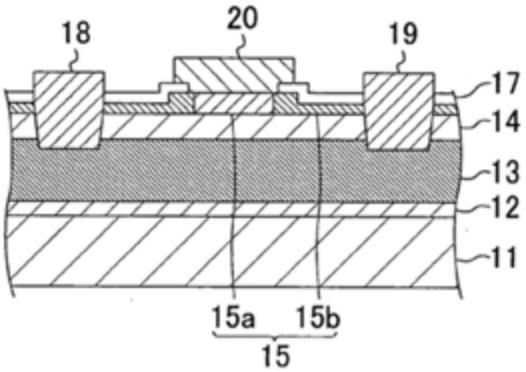
RDX-0013.34; RX-0079 Fig. 1

4. *Uemoto* Ground: *Uemoto* Renders Claims 1-3 Obvious

a. [1pre]: A column III Nitride transistor

To the extent the preamble is limiting, *Uemoto* discloses it. Tr. (Lebby) 874:14-22; RDX-0013.45. *Uemoto* discloses "nitride semiconductor transistors" made with "III Nitride materials." RX-0073 ¶¶ [0005], [0031]-[0032]; Tr. (Lebby) 874:16-22. *Uemoto*'s Figure 7, reproduced below, illustrates "a cross sectional view showing a nitride semiconductor transistor." RX-0073 Fig. 7.

FIG. 7



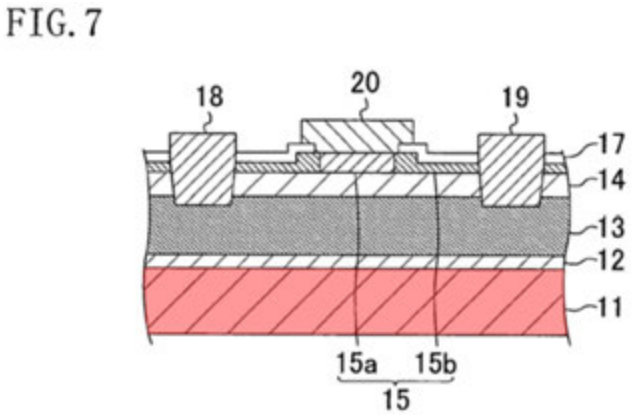
RDX-0013.45; RX-0073 Fig. 7

EPC does not dispute *Uemoto* discloses the preamble [1pre] of claim 1, challenging instead a hypothetical "non-functioning transistor embodiment." Tr. (Lebby) 874:18-22. The claim,

however, does not require any functionality. JX-0014 Claim 1. And there is no evidence that any of *Uemoto*'s disclosed embodiments are "non-functioning." *See* RX-0073. Further, "[a] prior art reference does not need to be fully functional to quality as prior art; indeed, a prior art reference 'need not work' and may even be 'inoperative.'" *Metso Mins., Inc. v. Powerscreen Int'l Distribution, Ltd.*, 526 F. App'x 988, 955 (Fed. Cir. 2013) (citation omitted).

b. [1a]: a substrate

Uemoto discloses [1a]. Tr. (Lebby) 874:24-875:6; RDX-0013.46. EPC does not dispute that *Uemoto* satisfies [1a]. Tr. (Lebby) 875:1-6. *Uemoto* discloses "a substrate 11 [that] is made of silicon," the same material the '294 patent associates with [1a]. RX-0073 ¶ [0031]; Tr. (Lebby) 875:1-6. *Uemoto*'s Figure 7 below highlights **substrate 11**.



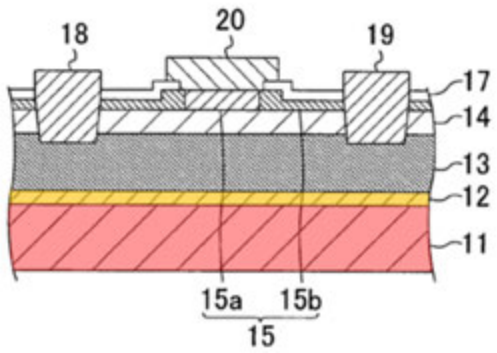
RDX-0013.46; RX-0073 Fig. 7 (annotated)

c. [1b]: a set of III-N transition layers above the substrate

Uemoto renders obvious [1b]. Tr. (Lebby) 875:9-17; RDX-0013.47. EPC does not dispute that *Uemoto* satisfies [1b]. Tr. (Lebby) 875:11-22. *Uemoto* discloses or at least renders obvious [1b] by describing a "buffer layer 12 of AlN having a thickness of 100 nm is formed on the principal plane of the substrate 11," which is formed with the same material as the transition layers described in the '294 patent. RX-0073 ¶ [0031]; Tr. (Lebby) 875:9-17. *Uemoto*'s **buffer layer 12**,

located above **substrate 11**, teaches or suggests the claimed III-N transition layers as highlighted in Figure 7 below.

FIG. 7

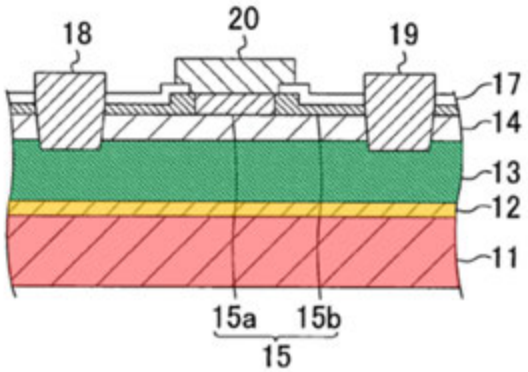


RDX-0013.47; RX-0073 Fig. 7 (annotated)

d. [1c]: a III-N buffer layer above the set of transition layers

Uemoto discloses [1c]. Tr. (Lebby) 875:19-876:2; RDX-0013.48. EPC does not dispute *Uemoto* satisfies [1c]. Tr. (Lebby) 875:21-876:2. *Uemoto* discloses "[a] first nitride semiconductor layer 13 [(buffer layer)] of undoped GaN . . . formed on the buffer layer 12." RX-0073 ¶ [0032]; Tr. (Lebby) 875:21-876:2. *Uemoto*'s semiconductor layer 13 is formed with the same material the '294 patent associates with a "buffer layer." JX-0014 3:12-15 ("Buffer layer 33 and barrier layer 34 are made of a III Nitride material.") *Uemoto*'s Figure 7 below highlights **semiconductor layer 13**, which is located above **buffer layer(s) 12**.

FIG. 7

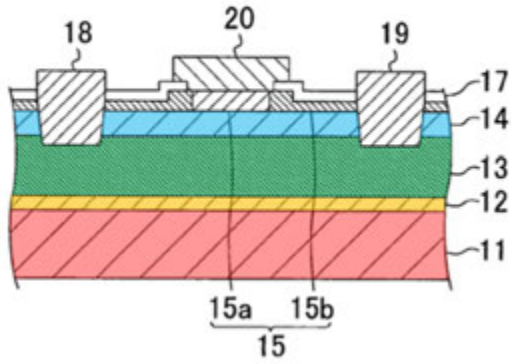


RDX-0013.48; RX-0073 Fig. 7 (annotated)

e. [1d]: a III-N barrier layer above the buffer layer

Uemoto discloses [1d]. Tr. (Lebby) 876:4-13; RDX-0013.49. EPC does not dispute that *Uemoto* satisfies [1d]. Tr. (Lebby) 876:6-7. *Uemoto* discloses "a second nitride semiconductor layer 14 of undoped AlGaN" (barrier layer) formed above the first nitride semiconductor layer 13. RX-0073 ¶ [0032]; Tr. (Lebby) 876:6-13. *Uemoto*'s second nitride semiconductor layer 14 is formed with the same material the '294 patent associates with the "barrier layer." JX-0014 3:12-15 ("Buffer layer 33 and barrier layer 34 are made of a III Nitride material.") *Uemoto*'s Figure 7 below highlights **semiconductor layer 14**, which is located above **semiconductor layer 13**.

FIG. 7



RDX-0013.49; RX-0073 Fig. 7 (annotated)

f. Expert Opinions Regarding Disputed Elements: [1e]: a compensated GaN layer above the barrier layer and [1f]: a gate contact above the compensated GaN layer

Uemoto discloses or at least renders obvious limitations [1e] and [1f]. Tr. (Lebby) 876:15-879:14; RDX-0013.50-54. Taken together, limitations [1e] and [1f] require two structural components (a compensated GaN layer and a gate contact) and one positional component (the compensated GaN layer must be above the barrier layer and below the gate contact).

i. Structural Component: "compensated GaN layer"

While the parties have competing constructions for "compensated GaN," there is no dispute that "compensated GaN" is at least passivated and resistive. *See e.g.*, Tr. (Lidow) 103:13-19; Tr.

(Schubert) 433:7-22; 435:8-13; Tr. (Lebby) 858:5-15. *Uemoto*, therefore, indisputably discloses "a compensated GaN layer" under any construction. Tr. (Lebby) 876:15-878:7.

Uemoto discloses a "third nitride semiconductor layer 15" including "a high resistive region 15b in which Mg is not activated." RX-0073 ¶¶ [0033], [0063]; Tr. (Lebby) 876:17-877:3. *Uemoto* explains that third nitride semiconductor layer 15 is Mg-doped and that 15b includes Mg passivated with H to inactivate the Mg and make the layer highly resistive. RX-0073 ¶¶ [0033], [0049], [0063]; Tr. (Lebby) 877:16-25.

EPC admits 15b is "p-doped, passivated and a resistive region," and therefore is indisputably "compensated GaN," as claimed. Tr. (Schubert) 960:4-10; 960:20-23. Indeed, Dr. Schubert testified that *Uemoto*'s "layer 15b is gallium nitride, contains magnesium and hydrogen, is passivated, and is non-conductive. So in that sense, it meets the claim term 'compensated gallium nitride.'" Tr. (Schubert) 1033:21-1034:7. There is no dispute, *Uemoto*'s region 15b is "compensated gallium nitride." *Id.* 964:1-7; 1033:21-1034:7.

ii. Structural Component: "gate contact"

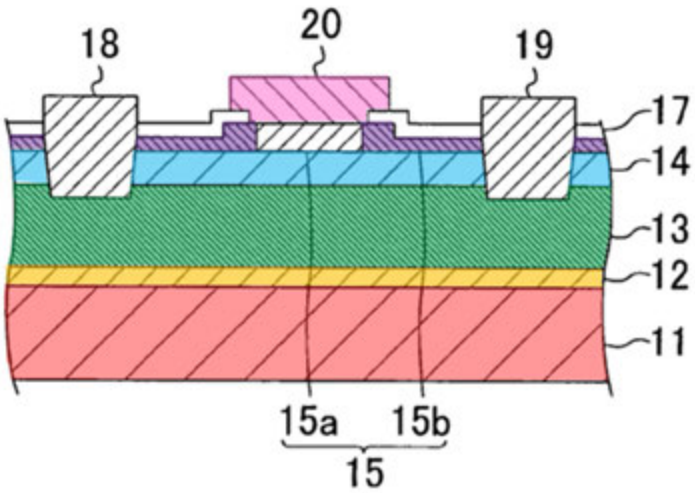
Uemoto discloses a "gate contact." Tr. (Lebby) 878:9-879:14. *Uemoto* discloses "gate electrode 20" that is located above semiconductor layer 15 (including high resistive **region 15b**). RX-0073 ¶¶ [0034], [0056], [0062]; Tr. (Lebby) 878:9-879:14. EPC does not dispute that *Uemoto*'s **gate electrode 20** is the "gate contact" as recited in [1f]. *See* Tr. (Schubert) 965:3-13; 966:21-24.

iii. Positional Component: compensated GaN layer "above the barrier layer"; and gate contact "above the compensated GaN layer"

Uemoto discloses layer 15 is a GaN layer and "[o]n the second nitride semiconductor layer 14," the barrier. RX-0073 ¶¶ [0033], [0054]; Tr. (Lebby) 877:5-12. Figure 7, annotated below, shows that *Uemoto*'s **layer 15b** (compensated GaN layer) is above the **semiconductor layer 14**

(barrier layer); and **gate electrode 20** is above **layer 15b** (compensated GaN layer). Tr. (Lebby) 878:9-879:14.

FIG. 7

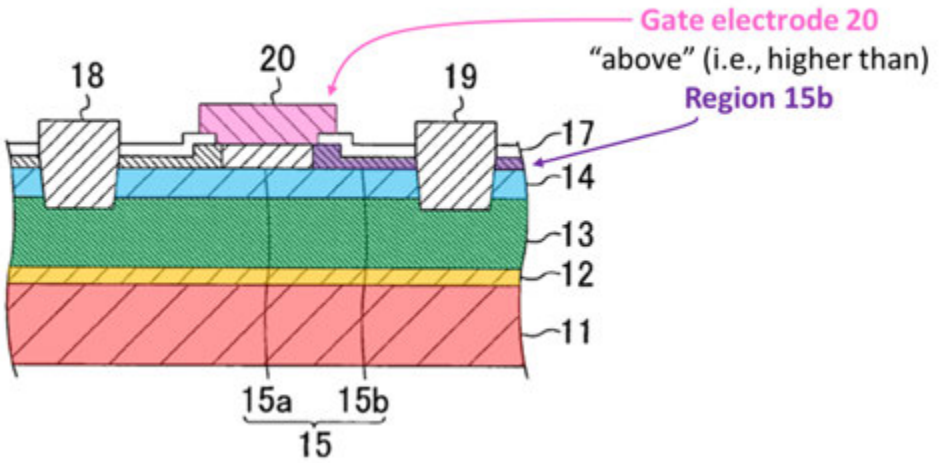


RDX-0013.53; RX-0073 Fig. 7 (annotated)

EPC's only dispute with the entirety of the *Uemoto* ground is that *Uemoto* fails to disclose the positional requirement of "a gate contact above the compensated GaN layer." Tr. (Schubert) 963:5-16; *see id.* 1034:4-25 (Dr. Schubert admitting *Uemoto*'s 15b is the claimed "compensated GaN" but alleging it is not positioned as in the claim).

First, EPC is wrong. *Uemoto*'s "gate contact [is] above the compensated GaN layer;" specifically, region 15b. Tr. (Lebby) 878:11-879:14. In the '294 patent, the claims use the term "above" as a preposition, to convey the spatial relationship between the claimed layers—meaning no more than "higher than." JX-0014 5:11-6:27; *See EMI Grp. N. Am., Inc. v. Cypress Semiconductor Corp.*, 68 F. Supp. 2d 421, 431 (D. Del. 1999) (construing "above" as "higher than, but not necessarily directly in contact with"); *Terlep v. Brinkman Corp.*, Case No. 02-cv-5127, 2004 U.S. Dist. LEXIS 28453, at *12 (W.D. Ark. Mar. 23, 2004) (construing "above" as "in a higher place than or overhead").

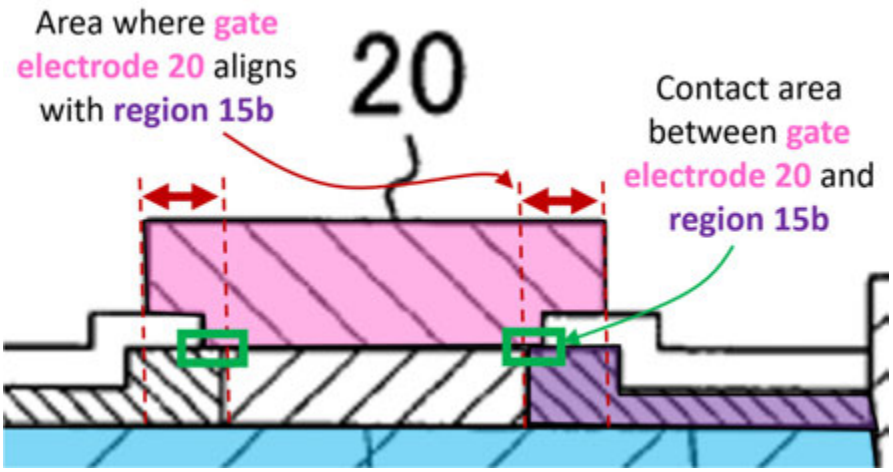
As shown below in *Uemoto*'s FIG. 7, *Uemoto* meets the positional requirements of claim 1 because *Uemoto*'s **gate electrode 20** is "above" (i.e., higher than) **region 15b** (the compensated GaN). Tr. (Lebby) 878:24-879:14.



RDX-0013.53; RX-0073 FIG. 7 (annotated)

Second, EPC's interpretation requiring direct contact between the gate contact and compensated GaN layer to satisfy the "above" limitation is wrong. Previous constructions of the term "above" rejected EPC's requirement. *Infection Prevention Techs., LLC v. Lumalier Corp.*, Case No. 10-cv-12371, 2012 WL 3248232, at *20 (E.D. Mich. Aug. 8, 2012) (adopting construction of "above" based on plain meaning and rejecting modifications based on horizontal and vertical alignment).

Third, even as voicing disagreement with the positioning disclosed in *Uemoto*, Dr. Schubert admitted *Uemoto*'s gate contact is above its compensated GaN layer 15b, admitting that "a sliver of region 15B" is under gate electrode 20. Tr. (Schubert) 965:3-19; *see also id.* 966:21-24. Or, phrased differently, admitting that gate electrode 20 is above a sliver of region 15b—**thus admitting the claim's position requirement is met or at least suggested and rendered obvious**.



RDX-0013.54; RX-0073 FIG. 7 (zoomed in and annotated)

g. [2p]: The transistor of claim 1

As discussed in Section II.B.4.a-f, a POSITA would have recognized that *Uemoto* obviates all limitations of claim 1, which are also included in claim 2. *Supra* § II.B.4.a-f.

h. [2a]: wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen

Uemoto discloses [2a] because *Uemoto* teaches that "acceptor type dopant atoms passivated with hydrogen" in region 15b of semiconductor layer 15, as claim 2 recites. Tr. (Lebby) 880:16-882:1. *Uemoto* discloses a layer 15 doped with magnesium, which a POSITA would have understood to be an acceptor because it is a p-type impurity. RX-0073 ¶ [0046]; Tr. (Lebby) 880:19-881:5. *Uemoto* also explains that, in layer 15 (including specifically **region 15b**), hydrogen inactivates/passivates the magnesium: "hydrogen from the hydrogen diffusion film 17 is supplied during a thermal treatment for selectively inactivating impurities." RX-0073 ¶¶ [0063], [0049]; Tr. (Lebby) 881:10-19. EPC does not dispute that region 15b is "passivated with hydrogen." Tr. (Schubert) 964:1-5; *see also id.* 961:22-962:6. Therefore, *Uemoto* discloses element [2a].

i. [3p]: The transistor of claim 2

As discussed in Section II.B.4.g-h, a POSITA would have recognized that *Uemoto* discloses all elements of claim 2, which are also included in claim 3. *Supra* § II.B.4.g-h.

j. [3a]: where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca

Uemoto discloses [3a] by describing *Uemoto*'s acceptor type dopant atoms are magnesium, disclosing that "layer 15 is . . . doped with magnesium (Mg)." RX-0073 ¶ [0033]; Tr. (Lebby) 882:3-11. EPC does not dispute that *Uemoto* discloses that layer 15b is "doped with magnesium" and "passivated with hydrogen." Tr. (Schubert) 964:1-5; *see also id.* 961:22-962:6.

Uemoto, therefore, discloses that region 15b is doped with Mg acceptors.

5. *Beach189* Ground: *Beach189* Anticipates Claim 1, and *Beach189* in View of *Kigami* Renders Claims 2 and 3 Obvious

a. Claim 1 is anticipated by *Beach189*

i. [1pre]: A column III Nitride transistor

To the extent [1pre] is limiting, *Beach189* discloses it. Tr. (Lebby) 854:4-13; RDX-0013.19.

Beach189 discloses a "III-nitride power semiconductor device includes a drain electrode, a source electrode and a gate electrode disposed between the drain electrode and the source electrode" and that the "gate electrode controls the current between the source electrode and the drain electrode." RX-0011 ¶¶ [0002]-[0003]. A POSITA would have understood such a device is a transistor. Tr. (Lebby) 854:9-13. EPC does not dispute *Beach189* discloses [1pre].

EPC wrongly asserts, however, that *Beach189* discloses a hypothetical non-functioning enhancement-mode transistor. Tr. (Lebby) 856:11-18; Tr. (Schubert) 948:22-5. No evidence supports EPC's allegation, and EPC is wrong for three reasons.

First, the claim does not require any particular functionality, let alone an enhancement-mode or a depletion-mode, but is instead drawn to a structure of a transistor. JX-0014 Claim 1. In fact, as Dr. Lebby explained, *Beach189* discloses both an enhancement-mode and a depletion-mode device. Tr. (Lebby) 936:7-937:2; RX-0011 ¶ [0044].

Second, an anticipatory prior art reference does not need to be fully functional to qualify as prior art; indeed, a prior art reference need not work and may even be inoperative. *Metso*, 526 F. App'x at 995.

Third, as explained in Sections II.B.5.a.vi and viii below, *Beach189* device would function properly as an enhancement-mode device. RDX-0100.4-6; Tr. (Lebby) 937:4-944:3.

ii. [1a]: a substrate

Beach189 discloses [1a]. Tr. (Lebby) 854:15-23; RDX-0013.20. EPC does not dispute *Beach189* discloses [1a]. Tr. (Lebby) 856:11-18.

Beach189 discloses a "support body 12 [that] is a combination of a substrate material." RX-0011 ¶ [0041], [0025]. Figure 4 below highlights the **substrate** in support body 12.

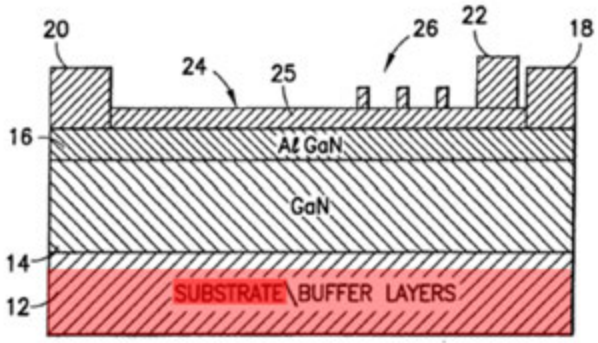


FIG.4

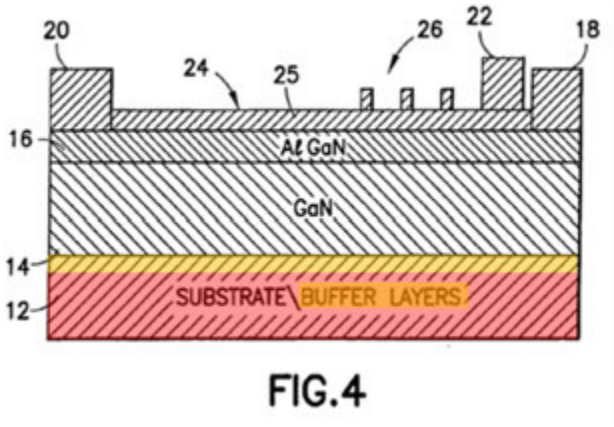
RDX-0013.20; RX-0011 Fig. 4 (annotated)

iii. [1b]: a set of III-N transition layers above the substrate

Beach189 discloses [1b]. Tr. (Lebby) 854:24-855:9; RDX-0013.21. EPC does not dispute *Beach189* discloses [1b]. Tr. (Lebby) 856:11-18.

Beach189 discloses [1b] because its transistors include "buffer layers" positioned over the substrate. RX-0011 ¶¶ [0041]-[0042]. *Beach189* specifies the buffer layers can be implemented with "a multi-layer or graded transitional III-nitride semiconductor body may also be used as a

buffer layer without deviating from the scope and the spirit of the present invention." RX-0011 ¶ [0042]. Figure 4 below shows *Beach189*'s **buffer layers** above **the substrate**.

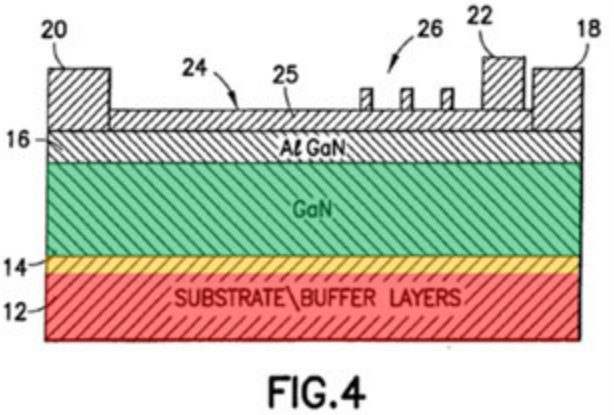


RDX-0013.21; RX-0011 Fig. 4 (annotated)

iv. [1c]: a III-N buffer layer above the set of transition layers

Beach189 discloses [1c]. Tr. (Lebby) 855:11-22; RDX-0013.22. EPC does not dispute *Beach189* discloses [1c]. Tr. (Lebby) 856:11-18.

Beach189 discloses "a first III-nitride semiconductor body 14" that employes the same material the '294 patent associates with the claimed "buffer layer." RX-0011 ¶¶ [0025], [0040], [0043]. Figure 4 below highlights *Beach189*'s **first III-nitride semiconductor body 14**, which is located above the **buffer layers**.



RDX-0013.22; RX-0011 Fig. 4 (annotated)

v. [1d]: a III-N barrier layer above the buffer layer

Beach189 discloses [1d]. Tr. (Lebby) 855:25-856:10; RDX-0013.23. EPC does not dispute *Beach189* satisfies [1b]. Tr. (Lebby) 856:11-18.

Beach189 discloses "a second III-nitride semiconductor body 16," which is located above the first III-nitride semiconductor body 14 and is formed with the same material and the same functionality that the '294 patent associates with the claimed "barrier layer." RX-0011 ¶¶ [0025], [0040]. Figure 4 below shows *Beach189*'s **second III-nitride semiconductor body 16**, which is located above the first III-nitride **semiconductor body 14**.

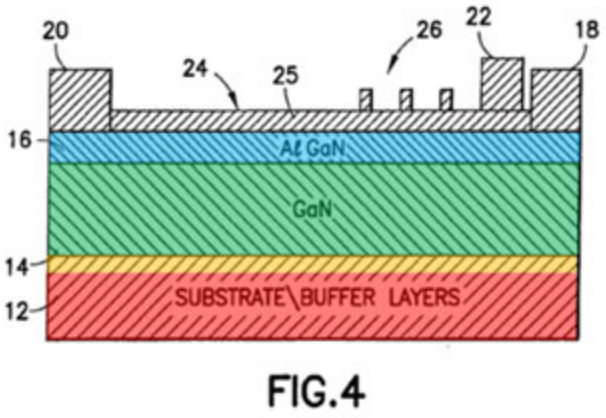


FIG.4

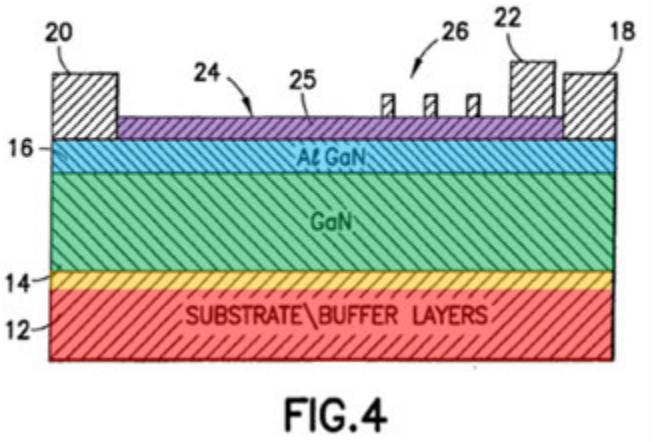
RDX-0013.23; RX-0011 Fig. 4 (annotated)

vi. [1e]: a compensated GaN layer above the barrier layer

Beach189 discloses [1e] under any contending construction because it expressly discloses "compensated GaN" that is "ultra resistive." RX-0011 ¶ [0026]; Tr. (Lebby) 856:23-857:24; RDX-0013.24-28; Tr. (Schubert) 1016:22-1017-5. While the parties have competing constructions for "compensated GaN," there is no dispute that "compensated GaN" is at least resistive. Tr. (Schubert) 433:7-22; Tr. (Lebby) 858:5-15.

Beach189 discloses **a field plate** formed with "compensated GaN" above **semiconductor body 16**. RX-0011 ¶¶ [0025]-[0026]. For example, *Beach189* discloses that "field relaxation

feature 24 is an ultra resistive field plate 25 formed with a highly electrically resistive material, such as, silicon rich SiN, ***compensated GaN*** or the like material." RX-0011 ¶ [0026] (emphasis added); *see also* RX-0011 Claim 7 ("field plate is comprised of a compensated III-nitride semiconductor"). The same term is used by the same inventor to describe the layer. Tr. (Lebby) 856:25-857:24. Figure 4 below, illustrates *Beach189*'s **field plate 25**.



RDX-0013.24-25; RX-0011 Fig. 4 (annotated)

As Dr. Schubert admits, a "compensated GaN" is passivated and a nonconductive or semi-insulating p-type GaN ("pGaN"). CDX-0002C.3; Tr. (Schubert) 433:7-22; *see also id.* 1016:22-1017-5 (Dr. Schubert agreeing that *Beach189* expressly discloses a "compensated GaN" as one exemplary material of the highly resistive field plate 25.) Thus, *Beach189*'s "ultra resistive" and "highly electrically resistive" field plate 25 formed with ***compensated GaN*** meets limitation [1e] under any proposed construction.

vii. [1f]: a gate contact above the compensated GaN layer

Beach189 discloses [1f]. Tr. (Lebby) 865:14-866:7; RDX-0013.29. EPC does not dispute the *Beach189*'s **gate structure 22** is the "gate contact" as recited in [1f]. Tr. (Schubert) 953:25-954:6.

Beach189 discloses a "gate structure 22," which is located above field plate 25 and has the same materials the '294 patent specifies for the gate contact. RX-0011 ¶¶ [0025], [0028], [0040], Fig. 4. *Beach189*'s Figure 4, annotated in color below, highlights **gate structure 22**, which is located above **field plate 25**.

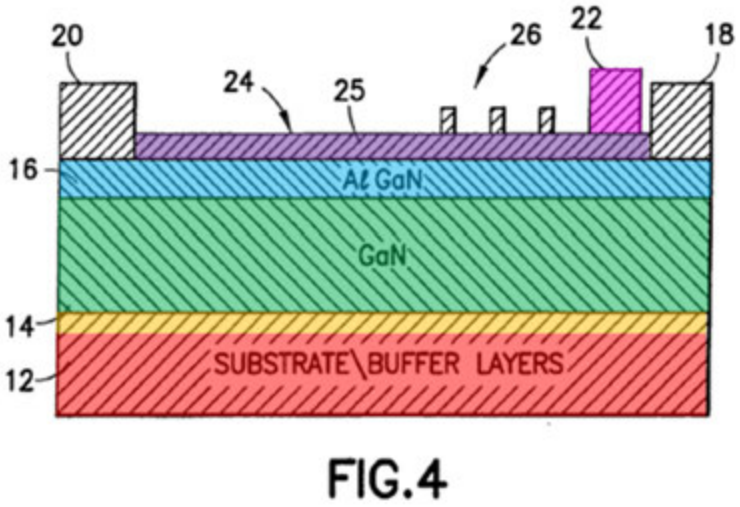


FIG.4

RDX-0013.29; RX-0011 Fig. 4 (annotated)

viii. Expert Opinions: EPC's arguments are meritless

EPC has only two, equally meritless arguments against *Beach189*'s compensated GaN field plate 25. First, EPC argues that *Beach189*'s field plate 25 is not a "compensated GaN layer" (despite being explicitly named as such in the reference) because the field plate must be electrically conductive, otherwise it would be non-functional as a "field plate." Second, EPC argues that, if the field plate 25 is p-type doped and passivated with hydrogen, *Beach189*'s device would be non-functioning enhancement mode device. Both arguments fail.

(a) *Beach189*'s field plate is compensated and ultra resistive

EPC first wrongly alleges that "field plate 25" cannot be a "compensated GaN layer" (although it is expressly disclosed in *Beach189* as "compensated GaN") because the field plate

must be electrically conductive. Tr. (Schubert) 951:3-8. Without relying on anything in the disclosure of *Beach189*, EPC argues abstractly that "compensated GaN" field plate 25 in *Beach189* must be electrically conductive to perform its stated purpose of improving breakdown voltage, while the "compensated GaN" in the '294 patent must be semi-insulating, which would not have a conductivity suitable for a field plate. *Id.*; *see generally id.* 951:12-952:25. EPC's transparent attempts to distinguish the "compensated GaN" in *Beach189* from the "compensated GaN" in the '294 patent cannot pass muster.

First, *Beach189*'s ultra resistive compensated GaN field plate ***is ultra resistive compensated GaN based on the express disclosure of the reference***—regardless of whether the transistor would function fully and efficiently. A prior art reference does not need to be fully functional to qualify as prior art; indeed, a prior art reference need not work and may even be inoperative. *Metso*, 526 F. App'x at 995; *see also Geo. M. Martin Co. v. All. Mach. Sys. Int'l LLC*, 618 F.3d 1294, 1302 (Fed. Cir. 2010) ("Even if a reference discloses an inoperative device, it is prior art for all that it teaches.") (citation omitted).

Second, EPC's fabricated and unsupported requirement for field plates to be conductive, or have metal-like conductivity, is wrong and contradicts the express disclosure of *Beach189* and Dr. Beach's description of his own patent. RX-0011 ¶ [0026]; Tr. (Lebby) 860:6-17. *Beach189* makes clear that the "field plate" is not conductive but "ultra resistive" and "formed with a highly electrically resistive material." RX-0011 ¶ [0026]. *Beach189* specifies the "field plate" is formed with "compensated GaN," not with a metal or metal-like material. *Id.* ("In the preferred embodiment of the present invention, field relaxation feature 24 is an ultra resistive field plate 25 formed with a highly electrically resistive material, such as, silicon rich SiN, compensated GaN or the like material."); *id.* [0006]-[0007] ("In one embodiment of the present invention the field

relaxation feature includes an ultra resistive field plate. . . . The field plate may formed with a silicon rich SiN, or a compensated IIInitride semiconductor."). And in describing *Beach189*, Dr. Beach made clear that *Beach189* discloses "the way that you relax those electric fields at the corner of field plates ***by putting a highly resistive layer*** between either a source field plate or a gate metal such that the fields are spread out evenly." Tr. (Beach) 376:7-23. EPC's attempt to require *Beach189*'s field plate to be conductive ignores at best and contradicts at worst *Beach189*'s clear description of this layer as "ultra resistive" and "composed of a highly electrically resistive material" that *Beach189* specifically names as "compensated GaN," indicating it is not intended to be conductive, and cannot change the clear statements in the reference. RX-0011 ¶ [0026].

Third, field plates are not limited to conductive elements. Tr. (Lebby) 860:6-17. Even textbooks, such as Dr. Pearton's (RX-0075), describe non-conductive field plates, using for example silicon oxide, a common dielectric material. Tr. (Schubert) 1019:20-1020:13; RX-0075.205-207 ("Field Plate Termination"); *see also* RX-0075.208 (describing a "SiO_2 field plate"). Pearton explains that this dielectric, non-conductive, field plate mitigates breakdown issues. RX-0075.205-207; Tr. (Schubert) 1019:25-1020:13. The exemplary dielectric field plate in Pearton uses the same structure with a metal overlap as *Beach189*. *Compare* RX-0011 Fig. 2 *with* RX-0075 Fig. 3.13. Both *Beach189* and Dr. Pearton's textbook describe breakdown happening because large fields develop at the gate edge. *Compare* RX-0011 ¶ [0004], *with* RX-0075.206. Both mitigate that problem by using the same field plate structure, with the textbook structure using a SiO_2 field plate, and *Beach189* using a field plate made of "ultra resistive" / "highly electrically resistive" "Si-rich SiN or compensated GaN." *Compare* RX-0011 ¶ [0026], Fig. 2, *with* RX-0075.205-207, Figs. 3.13-3.15. Even Dr. Schubert admits, SiO_2 is insulating, not conductive. Tr.

(Schubert) 1019:25-1020:13. Contrary to EPC's belief, field plates (including the ultra resistive field plate in *Beach189*) need not be conductive. Tr. (Lebby) 860:6-17.

Indeed, the field plate in *Beach189* cannot be conductive. If the field plate of *Beach189* were conductive, as Dr. Schubert maintains, the gate 22 and drain 20 in Figure 2 of *Beach189* would short-circuit, which is contrary to the purpose of improving gate-drain breakdown. *See* RX-0011 Abstract, ¶¶ [0003]-[0004]. Dr. Schubert admitted. Tr. (Schubert) 1019:7-15 (Q: "And if element 25 were electrically conductive, because it has a contact with the source and a contact with the drain, it would create a leakage current path, wouldn't it?" A: "It would create a source-drain leakage current path, correct." Q: "And depending on the conductivity of element 25, it could create a short-circuit, couldn't it?" A: "In an extreme case, yes."). Instead, as the reference itself states, this layer is made of "compensated GaN,"—insulating, not conductive.

(b) *Beach189* discloses a fully functional enhancement-mode transistor, but that is irrelevant to the anticipation inquiry

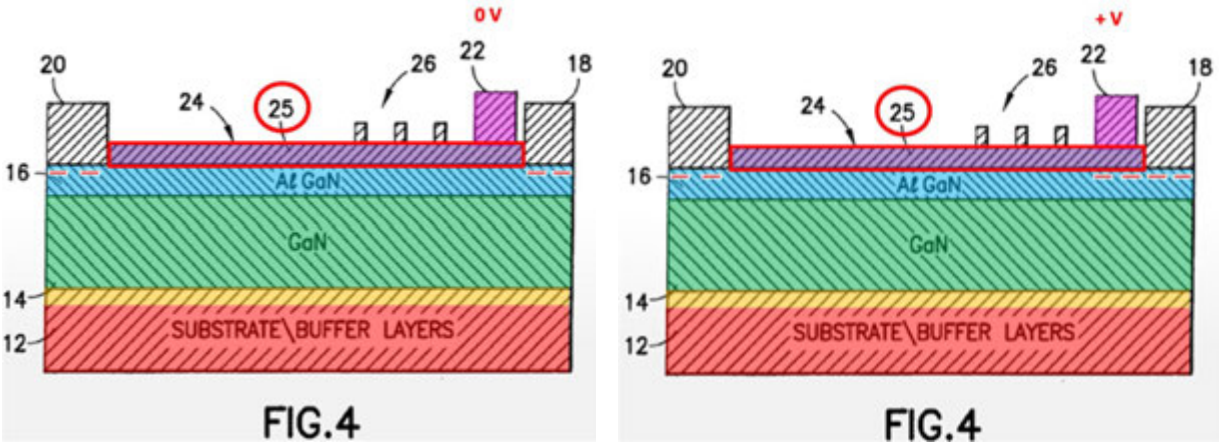
Second, EPC wrongly argues that if the field plate 25 is p-type doped and passivated with hydrogen *Beach189*'s device would be a non-functioning enhancement mode device. Tr. (Schubert) 954:11-955:3.

First, as noted a prior art reference does not need to be fully functional to anticipate a claim. *Metso*, 526 F. App'x at 995; *see also Geo. M. Martin*, 618 F.3d at 1302.

Second, the claim ***does not require*** an enhancement-mode transistor, but is instead drawn to a transistor structure generally. JX-0014 Claim 1. Dr. Schubert agrees. Tr. (Schubert) 1016:6-13. Regardless, as Dr. Lebby explained, *Beach189* discloses both an enhancement-mode and a depletion-mode device. RX-0011 ¶ [0044]; Tr. (Lebby) 936:7-937:2 ("Paragraph 44 is interesting because the highlighted area, quote, the gate electrode may be exposed of n-type or p-type silicon and it goes on to say any design conductivity and so if you design a device with n-type material

then it is a depletion-mode," and "[i]f you design a device with p-type material as we've heard in this litigation, it's enhancement-mode.").

Third, the *Beach189* device with p-type doped field plate passivated with hydrogen would function as an enhancement-mode device. RDX-0100.4-6; Tr. (Lebby) 937:4-944:3. Dr. Lebby illustrated this. In the left figure below, when **0 V** is applied to the gate electrode 22, the 2DEG (annotated as red '–' signs) "will be depleted underneath layer 25, which is the compensated GaN layer as taught by Beach." RDX-0100.4; Tr. (Lebby) 937:11-18. And then, as shown in the right figure below, when a positive voltage **+ v** is applied, the 2DEG will be formed close to the gate electrode 22 but may not be continuous all the way from the source electrode to the drain electrode. RDX-0100.5; Tr. (Lebby) 938:5-10. It appears that EPC's argument is based on this point—the 2DEG may not be fully established from source to drain when a positive voltage is applied to the gate. Tr. (Lebby) 938:5-10.



RDX-0100.4-5

However, as Dr. Lebby ***further*** explained during the Evidentiary Hearing, simply increasing the gate voltage (e.g., up to **+++ v** instead of **+ v**, as shown below) ***would*** form the 2DEG under the other part of the plate 25, and thus establish the 2DEG all the way from the source to the drain. RDX-0100.6; Tr. (Lebby) 938:15-939:8. A POSITA would have thus understood that

applying a sufficiently high gate voltage would make *Beach189* device a functional enhancement-mode transistor. *Id.* 943:18-944:3.

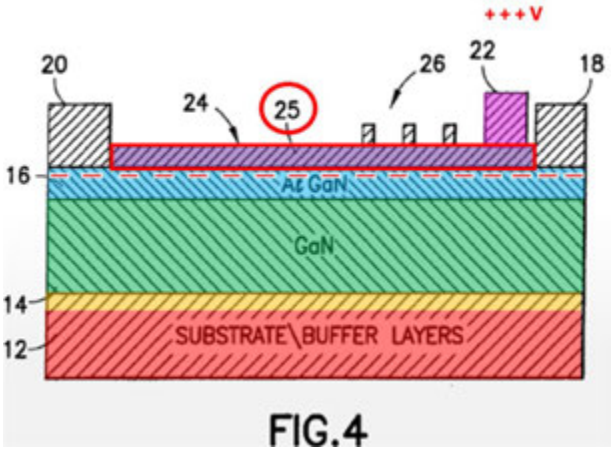


FIG.4

RDX-0100.6

EPC's argument that the "compensated GaN" in *Beach189* is different than the "compensated GaN" in [1e] is facially antithetical and makes no sense; particularly here where the term was used by the same inventor and the inventor testified that the "compensated GaN" term would have been plainly understood by anyone in the field. JX-0018C 159:8-16. Further, as the CALJ indicating during the Markman Hearing, the "compensated GaN layer" language in the claim does not require any "gate structure." Markman Tr. 291:10-12. And even if it had to, *Beach189* field plate is below the gate, forming part of the gate structure. Tr. (Lebby) 866:2-7.

b. Claims 2 and 3 are rendered obvious by *Beach189* and *Kigami*

i. Motivation to Combine for Claims 2 and 3: A POSITA would have been motivated to form *Beach189*'s compensated GaN using *Kigami*'s process for doping the GaN with magnesium and passivating the magnesium with hydrogen

A POSITA would have been motived to apply *Kigami*'s hydrogen passivation and magnesium doping to *Beach189*'s compensated GaN. While *Beach189* discloses "compensated GaN," which is admittedly p-doped and passivated, *Beach189* itself includes no express disclosure of how to dope or passivate the GaN to form the compensated GaN. A POSITA would, therefore,

have been motivated to look for additional disclosures for how to form the compensated GaN, including *Kigami*—which teaches a standard process for magnesium doping and hydrogen passivation. Tr. (Lebby) 868:10-869:7; RDX-0013.35; RX-0011 ¶ [0026]; RX-0079 ¶ [0026].

Beach189 discloses transistors with a "field plate" that is "ultra resistive" and formed with a "highly electrically resistive material," for example, a "compensated GaN." RX-0011 ¶ [0026]. Although methods for making such compensated III-nitride layers were well-known in the art (RX-0003.34; JX-0018C 159:8-16 (Dr. Beach, a coinventor of the '294 patent, testifying that "anybody skilled in the art would know how to grow a compensated gallium nitride layer"); RX-0079 ¶¶ [0007]-[0012], RX-0073 ¶ [0015]), *Beach189* does not specify any particular method for forming the disclosed compensated GaN field plate. Thus, a POSITA would have been motivated to form the *Beach189* field plate using methods that, like *Kigami*'s method to form highly resistive GaN by hydrogenating pGaN, yielded a "highly electrically resistive" III-nitride, GaN, or similar material—compensated GaN. RX-0079 ¶ [0007]; Tr. (Lebby) 868:10-869:20.

A POSITA would have been motivated to employ *Kigami*'s hydrogenation of Mg doped layers (RX-0079 ¶ [0026]) to form the highly resistive "compensated GaN" taught in *Beach189* (RX-0011 ¶ [0026]) because:

- **a.** *Beach189* and *Kigami* are closely related, both disclosing III-nitride transistors and fabrication techniques to improve them. Tr. (Lebby) 870:5-12; RDX-0013.37;
- **b.** The application of *Kigami* to *Beach189* would simply be combining prior art elements according to known methods to yield predictable results of forming a highly resistive field plate. Tr. (Lebby) 870:13-22; RDX-0013.37;

c. The application of *Kigami* to *Beach189* would be applying a known technique to a known device that is ready for improvement. Tr. (Lebby) 870:22-871:4; RDX-0013.37;

d. A POSITA would have applied *Kigami*'s method for forming a highly resistive semiconductor layer in the *Beach189* device with a reasonable expectation of success. Tr. (Lebby) 871:5-11; RDX-0013.37.

ii. Expert Opinions Regarding Claims 2 and 3: EPC argument against the motivation to combine fails as EPC misinterprets the claims and the prior art references

For claims 2 and 3, EPC does not dispute that the combination of *Beach189* and *Kigami* discloses the elements of the dependent claims. *See generally* CDX-0003C.15-19. EPC contends only that a POSITA would not have applied *Kigami*'s teachings to *Beach189*. Tr. (Schubert) 959:14-21. EPC alleges that applying *Kigami*'s technique to *Beach189* would have been "counter-intuitive"—contradicting Dr. Beach's admission that "anybody skilled in the art would know how to grow a compensated gallium nitride layer." *Id.* 955:24-957:9. EPC also alleges that *Kigami*'s techniques are not applicable to *Beach189* because the "field plate"—which *Beach189* describes as "ultra resistive . . . formed with a highly electrically resistive material"—should be interpreted as conductive. *Id.* 958:5-11. EPC is wrong.

First, it would not be counter-intuitive to apply *Kigami*'s teaches to *Beach189* because *Kigami* teaches, motivates, and suggest applying its technique to improve the transistor characteristics. Tr. (Lebby) 868:10-869:7; *see, e.g., Schwendimann v. Neenah, Inc*., 82 F.4th 1371, 1381 (Fed. Cir. 2023) (affirming motivation to combine when the references share a common goal of improving characteristics and references expressly teaches advantages).

Second, without supporting evidence, EPC alleges that it would have been counterintuitive "to passivate and thereby cancel acceptors in a GaN layer below the gate contact – after first introducing those acceptors as dopants – to create a device." Tr. (Schubert) 955:24-957:9. But that exact sequence—introducing the acceptor dopants, and then passivating the very acceptor dopants with hydrogen to cancel the effect of those acceptors—is precisely what *Kigami* teaches is beneficial to transistor performance. Tr. (Lebby) 871:16-24. *Kigami* teaches that its hydrogenation of pGaN below the gate contact technique improves III-nitride transistors, like the one *Beach189* discloses, explaining that it can stabilize the threshold voltage, improve the breakdown voltage, and improve frequency operation. RX-0079 ¶¶ [0026]-[0029]. This type of hydrogen passivation process was well-known at the time of invention. Other references, including Dr. Beach's own thesis, also teach that the hydrogen passivation of pGaN is beneficial, not counterintuitive. *See* RX-0003.141; RX-0073; RX-0079; RX-0079. A coinventor, Dr. Beach, admits that anybody skilled in the art would know how to grow a compensated gallium nitride layer. JX-0018C 159:8-16. Even Dr. Schubert's (EPC's expert) book (RX-0255) makes clear that far from being "counter-intuitive," using hydrogen implantation to make highly resistive III-V materials was well known by the mid-1990s. RX-0255.402 ("Hydrogen implantation is a process that is widely used to render III-V semiconductors highly resistive.") EPC's unsupported allegations of a counterintuitive combination, plainly contradicted by the prior art references, should be dismissed. *See Intercontinental Great Brands LLC v. Kellogg N. Am. Co.*, 118 F. Supp. 3d 1022, 1035–36 (N.D. Ill. 2015), aff'd, 869 F.3d 1336 (Fed. Cir. 2017) (dismissing arguments of a counterintuitive combination when the evidence did not support them).

Third, as explained in Sections II.B.5.a.vi and viii above, nothing in *Beach189* requires the "field plate" to be conductive. *See generally* RX-0011. To the contrary, *Beach189*

unmistakably specifies the "field plate" is "ultra resistive . . . formed with a highly electrically resistive material," ***not*** a conductive material. RX-0011 ¶ [0026]. Indeed, *Beach189*'s field plate cannot be conductive because, it would short-circuit the *Beach189* transistor, which is contrary to the purpose of improving voltage breakdown. *Supra* §II.B.5.a.viii; Tr. (Schubert) 1019:7-15. EPC's argument that a "field plate" must be understood in the context of a conductive metal not only contradicts *Beach189*'s explicit teachings but also has no technical support. RX-0011 ¶¶ [0026], [0040].

A POSITA would thus have been motivated to apply *Kigami*'s teachings to form *Beach189*'s "field relaxation feature" with an "ultra-resistive field plate." Tr. (Lebby) 868:10-869:7; 870:5-871:11.

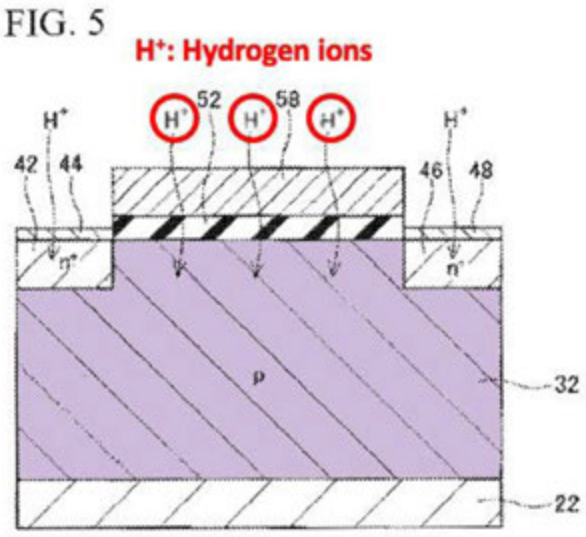
iii. [2p]: The transistor of claim 1,

As discussed in Section II.B.5.a, *Beach189* discloses all elements of claim 1, which are also included in claim 2.

iv. [2a]: wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen

A POSITA would have found it obvious that *Beach189*'s "compensated GaN" would be formed with acceptor type atoms (like Mg) that are passivated with hydrogen as taught by *Kigami*. Tr. (Lebby) 871:16-872:4; RDX-0013.38.

Kigami discloses a GaN semiconductor layer, which contains magnesium. RX-0079 ¶¶ [0007]-[0008], [0024]. *Kigami* further discloses a process for passivating (inactivating) the magnesium atoms (acceptor type dopants) in the GaN semiconductor layer with hydrogen. *Id.* ¶¶ [0010]-[0012], [0026], Fig. 5. Dr. Schubert admits that *Kigami* discloses that the p-type impurities, like magnesium, are passivated with the hydrogen atoms. Tr. (Schubert) 1022:16-22; 1024:14-17.



RDX-0013.38; RX-0079, Fig. 5 (annotated)

A POSITA would have known that a "compensated GaN" layer could be formed by *Kigami*'s process of passivating a Mg-doped GaN layer with hydrogen. RX-0079 ¶¶ [0007]-[0012], [0024]-[0026]; RX-0003.34, 125. As Dr. Beach, a coinventor of the '294 patent, acknowledges, "anybody skilled in the art would know how to grow a compensated gallium nitride layer." JX-0018C 159:8-16. A POSITA would have been motivated to form *Beach189*'s "compensated GaN" **field plate 25** using *Kigami*'s method of fabricating a highly resistive GaN layer by doping that layer with magnesium and passivating it with hydrogen. *Supra* §II.B.5.b.i-ii. When the **field plate 25** is formed using *Kigami*'s method, it would "contain[] acceptor type dopant atoms" (the Mg dopants *Kigami* teaches) "passivated with hydrogen" (using a hydrogenation step as also taught in *Kigami*). Tr. (Lebby) 871:16-872:4.

EPC, however, argues that claim 2 is not obviated by the *Beach189* and *Kigami* combination, arguing that *Kigami*'s passivation is done for a different purpose and in a different layer. Tr. (Schubert) 959:14-21. But the purpose of the passivation is not, it cannot be, a claim limitation. *Marrin v. Griffin*, 599 F.3d 1290, 1294 (Fed. Cir. 2010) ("For apparatus claims . . . generally patentability 'depends on the claimed structure, not on the use or purpose of that

structure.'") (citing *Catalina Marketing Int'l v. Coolsavings.com, Inc.*, 289 F.3d 801, 809 (Fed. Cir. 2002)). And, in any event, *Kigami*'s purpose of passivation aligns with *Beach189*'s objective of forming a field relaxation feature with a highly resistive field plate. RX-0011 ¶ [0026]; RX-0079 ¶ [0012]; Tr. (Lebby) 868:10-869:7. EPC also alleges that it would have been counterintuitive to apply *Kigami*'s technique to *Beach189*'s device. Tr. (Schubert) 955:24-957:9. But there is nothing counterintuitive about it because that exact sequence—introducing the acceptor dopants, and then passivating the very acceptor dopants with hydrogen to cancel the effect of those acceptors—is precisely what *Kigami* expressly discloses. *Supra* §II.B.5.b.i-ii; Tr. (Lebby) 871:16-24; RX-0079 ¶¶ [0024]-[0026].

Further, *Kigami*'s disclosure is not limited to passivation of a single layer, as EPC contends, because *Kigami* teaches adjusting "the region into which the hydrogen atoms are to be introduced," which Dr. Schubert agrees. Tr. (Schubert) 1024:4-17; RX-0079 ¶ [0026]. Further, EPC misunderstands or misrepresents the proposed *Kigami* and *Beach189* combination. The proposed combination is the application of *Kigami*'s technique to form highly resistive material to form *Beach189* "compensated GaN layer," not the substitution of layers or the inclusion of one of *Kigami*'s layers into *Beach189*'s device. *Supra* §II.B.5.b.i-ii.

Therefore, even if *Beach189* itself does not provide explicit details about its "compensated GaN," a POSITA would have found it obvious to use "compensated GaN" that includes Mg passivated by hydrogen as recited for element [2a].

v. [3p]: The transistor of claim 2

As discussed in Section II.B.5.b.i-iii, *Beach189* in combination with *Kigami* teaches all elements of claim 2, which are also included in claim 3.

vi. [3a]: where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca

A POSITA would have found it obvious that an example of the acceptor type atoms is Mg. Tr. (Lebby) 872:7-15; RDX-0013.40.

Kigami discloses a GaN semiconductor layer, which is doped with a p-type impurity (acceptor type dopant), magnesium. RX-0079 ¶¶ [0012] ("The p-type impurity preferably is magnesium."), [0024] ("Next, the semiconductor layer 32 of gallium nitride (GaN), which contains magnesium, is formed on the sapphire substrate 22 using the metalorganic vapor-phase epitaxial (MOCVD) method."). *Kigami* further discloses a process for passivating the magnesium with hydrogen. *Id.* ¶¶ [0010]-[0012], [0026], Fig. 5. Dr. Schubert admits that *Kigami*'s GaN semiconductor layer 32 includes magnesium, which is passivated with the hydrogen. Tr. (Schubert) 1021:10-21; 1022:16-22.

A POSITA would have known that a "compensated GaN" layer includes hydrogen-passivated magnesium. RX-0079 ¶¶ [0007]-[0012]; RX-0003.34, 141; JX-0018C 159:8-160:3 (Dr. Beach testifying that "anybody skilled in the art would though how to grow a compensated gallium nitride layer" and "[a]s you can see in our device there are two methods demonstrated that are common . . . a second is a compensated using magnesium compensated with hydrogen"), 179:2-8 (Dr. Beach testifying that "[i]t was known that magnesium hydrogen complex is are formed during the growth process"), 186:19-187:14 (Dr. Beach testifying that "although we ta[l]ked about hydrogen you could have said I want to compensate my magnesium with oxygen or I could have compensated it with some other [dopants]"). A POSITA would have found it obvious that *Beach189*'s "compensated GaN" would be formed with "acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca." Tr. (Lebby) 872:7-873:11. As explained above, a POSITA would have found it obvious to apply *Kigami*'s techniques to form **field plate 25**. When

the **field plate 25** is formed using *Kigami*'s method, it would contain hydrogen-passivated Mg dopants. RX-0079 ¶ [0012] (describing "[t]he p-type impurity preferably is magnesium").

EPC's arguments against the combination of *Beach189* and *Kigami* fails as discussed with respect to claim 2 above. *Supra* §II.B.5.b.i-iii. EPC does not raise any other arguments specific for claim 3. Accordingly, element [3a] would have been obvious.

6. EPC Fails to Show Secondary Considerations

EPC as the patent owner bears the burden of demonstrating secondary considerations may render a claim nonobvious. *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1373 (Fed. Cir. 2018) ("[A] patentee bears the burden of production with respect to evidence of secondary considerations of nonobviousness"). Therefore, to the extent EPC does not raise secondary considerations in its initial post-hearing brief, it has waived the issue. Ground Rule 14.1 ("Any contentions for which a party has the burden of proof that are not set forth in detail in the post-hearing initial brief shall be deemed abandoned or withdrawn.") Nevertheless, no secondary considerations support a finding of nonobviousness.

a. Claim 1: Secondary considerations irrelevant as Claim 1 is invalid over a single reference

Secondary considerations are irrelevant to the invalidity analysis for claim 1 because all elements of claim 1 are disclosed by *Uemoto* alone in the *Uemoto* ground, and *Beach189* alone in the *Beach189* ground. "[O]bviousness requires analysis of secondary considerations of nonobviousness, while secondary considerations are not an element of a claim of anticipation." *Cohesive Technologies, Inc. v. Waters Corp.*, 543 F.3d 1351, 1364 (Fed. Cir. 2008); *Allergan, Inc. v. Sandoz Inc.*, 818 F. Supp. 2d 974, 1004 (E.D. Tex. 2011) ("Evidence of secondary considerations, such as unexpected results or commercial success, is irrelevant to the 35 U.S.C. § 102 analysis."); *see also Trustees of Columbia Univ. in City of New York v. Illumina, Inc.*, 620

F. App'x 916, 931 (Fed. Cir. 2015) (rejecting patentee's secondary consideration argument because "each of the features claimed to be responsible for the commercial success of the invention was disclosed in a single prior art reference.").

b. Claims 2 and 3: EPC fails to tie secondary considerations to claim elements

EPC has not shown secondary considerations tied to claims 2 and 3 of the '294 patent. EPC appears to argue that there was a long-felt but unrealized need for the invention disclosed in the '294 patent. CDX-0003C.52. But Dr. Schubert's *general* descriptions about purported advantages of GaN enhancement-mode devices over silicon MOSFET power devices fail to satisfy EPC's burden to show evidence of secondary considerations of nonobviousness. *See generally* Tr. (Schubert) 1009:18-1011:15.

i. Alleged Nexus

For "secondary considerations" to be relevant, there must be a nexus between the claim elements and the alleged secondary considerations. *See Fox Factory, Inc. v. SRAM, LLC*, 944 F.3d 1366, 1373 (Fed. Cir. 2019). For nexus to exist, the alleged secondary consideration must be limited to the features of the claimed invention and not due to an unclaimed feature of the device or some other consideration and the patentee bears the burden that a nexus exists. *Id.* EPC has not, cannot, connect its alleged secondary considerations to the specific element of claim 2 and 3 of the '294 patent. For example, claim 2 recites the compensated GaN layer contains "acceptor type dopant atoms passivated with hydrogen." JX-0014, claim 1. Dr. Schubert, however, has failed to provide any opinion, let alone any evidence, about the nexus between the alleged long-felt but unrealized need and the claim element—a GaN layer having *acceptor type dopant atoms* and also *passivated with hydrogen*. *See generally* Tr. (Schubert) 1009:18-1011:15. Similarly, Dr. Schubert

has not provided any opinion why using a certain types of acceptor type dopants, like magnesium, solved the alleged long-felt need. *Id.*

EPC alleges that there is nexus between the claims of the '294 patent and the secondary consideration (the long-felt but unrealized need) because "[t]he technology of the '294 patent results in low leakage current and also reduced capacitance of the gate electrode, and that helps with respect to the switching speed," which is "what makes that transistor a success story." Tr. (Schubert) 1011:7-15. But EPC has failed to provide any evidence how the specific elements of claims 2 and 3 are connected to the alleged long-felt but unrealized need. EPC's analysis of *general* descriptions in the patent for purported reduced leakage and reduced capacitance fails to establish the required nexus between the claims and the secondary considerations.

Further, no nexus can be established between the purported long-felt need and EPC's products because they include many more features than the ones claimed in the '294 patent. EPC has not addressed the features recited in claims 2 and 3 of the '294 patent or presented any analysis of why the alleged secondary consideration are limited to the features of the claims 2 and 3 and not to other features or unclaimed features of the device. *See generally* Tr. (Schubert) 1009:18-1011:15. EPC only generally alleges that EPC's transistor is "a success story." Tr. (Schubert) 1011:11-15. EPC's bare assertion fails to establish connection to the claims 2 and 3 of the '294 patent.

Therefore, EPC has not shown nexus between its alleged secondary considerations and the claims of the '294 patent.

ii. Alleged Failure of Others and Long Felt Need

To support secondary considerations based on a long-felt need and failure of others, a patentee needs to show objective evidence that a problem existed in the art for a long period of time without solution. *See Nike, Inc. v. Adidas AG*, 955 F.3d 45, 54 (Fed. Cir. 2020). Multiple

factors guide this analysis, including the persistency of the problem, recognition of the problem by those skill in the art, and lack of satisfaction by others. *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1325 (Fed. Cir. 2004).

EPC's allegations that others failed and/or that there was a long felt need for the patented technology appear to be more generally directed toward enhancement-mode GaN transistors, technology EPC did not invent, not the specific invention claimed in the '294 patent. Tr. (Schubert) 1009:21-1010:23. For example, Dr. Schubert praises the advantages of GaN devices over silicon MOSFET devices. Tr. (Schubert) 1009:21-1010:6. But that is irrelevant because the GaN transistor devices were available long before the '294 patent. The '294 patent itself concedes that GaN transistors were "prior art." JX-0014 1:55-2:2, Fig. 1.

Without any support Dr. Schubert also alleges that an enhancement-mode "transistor has not been available until the invention of the '294 patent and the invention of the '508 patent arrived and have provided a viable switching transistor that the field was longing for." Tr. (Schubert) 1010:13-23. He is wrong. EPC did not invent the enhancement-mode GaN transistor. As discussed in Sections II.B.5.a.vi and viii above, *Beach189* disclosed an enhancement-mode transistor using a compensated GaN layer. RX-0011 ¶ [0044]; Tr. (Lebby) 936:7-937:2. Others had already published solutions for improving the gate leakage in III-nitride transistors, including the use of hydrogen passivation, the control of different thicknesses in the layers of the transistors, and techniques for doping to enhance the resistivity of the material. *See e.g.*, RX-0079; RX-0011; RX-0073. Even the '294 patent recognizes, normally-off (enhancement-mode) transistors were already known at the time of invention. JX-0014 Fig. 1. EPC has not identified evidence that the purported inventive features of the '294 patent addressed a long-term problem and that it was unresolved.

EPC has provided no evidence that a POSITA would have recognized the invention of the ’294 patent addressed a problem that had been persistent for a long time. Therefore, EPC has not shown the ’294 patent resolved a long-felt need and failure of others.

III. U.S. PATENT NO. 8,404,508

A. Claim Construction for the ’508 Patent: Not at Issue for Invalidity

There are two unresolved disputed terms for the ’508 patent that are relevant to nonburden issues. These two terms are listed below:

(1) “applying a gate photo resistant pattern; etching away the gate contact layer outside the gate region; etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact; removing the gate photo resistant pattern” (claim 1), as the chart below summarizes.

EPC	Respondents	The Staff
There are 4 distinct steps.	“applying a gate photo resistant pattern; using the gate photo resistant pattern to etch away the gate contact layer outside the gate region; using the gate photo resistant pattern to etch away the doped GaN layer in all regions extending outside the gate contact; removing the gate photo resistant pattern”	Steps must be performed in order.

(2) “depositing a gate contact layer on the doped GaN layer” (claim 1), as the chart below summarizes:

EPC	Respondents
depositing a gate contact layer above the doped GaN layer	requires direct contact between the "gate contact layer" and the "doped GaN layer."

Additionally, at the Markman hearing, the parties agreed that the term "etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact" means "etching away the doped GaN layer where it is not beneath the gate contact, without etching beneath the gate contact." Markman Tr. 153:13-155:18.

B. Invalidity of the '508 Patent

The asserted claim is invalid as rendered obvious over the prior art under 35 pre-AIA U.S.C. § 103.

1. Priority Date

The relevant priority date for the '508 patent, as well as the date from which to apply the perspective of a POSITA for the '508 patent, is April 8, 2009. JX-0015 Cover. Thus, pre-AIA § 102 applies.

2. Level of Ordinary Skill

The level of ordinary skill for the '508 patent is the same as the '294 patent, and undisputed. *Supra* § II.B.2.

3. Overview of the Prior Art

The following references render claim 1 obvious:

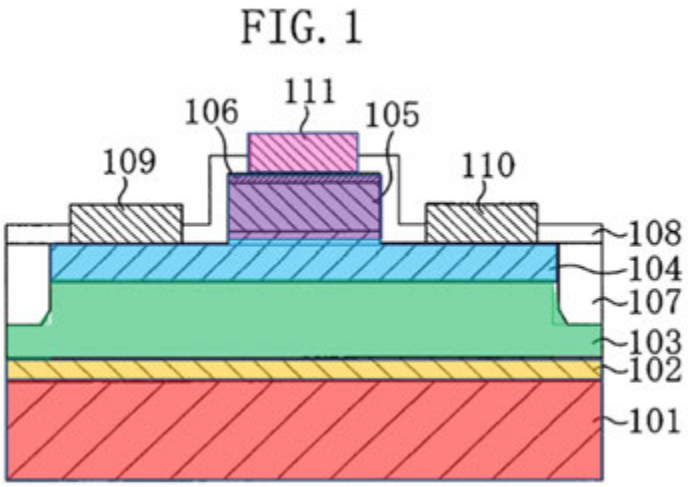
- **RX-0041**: U.S. Patent Application Publication No. 2006/0273347 to Hikita et al. ("*Hikita*")
- **RX-0288**: U.S. Patent No. 7,238,560 to Sheppard et al. ("*Sheppard*")
- **RX-0286**: International Patent Application Publication No. WO 2005/057624 to Beach ("*Beach624*")

Each of the above references qualifies as prior art.

a. *Hikita* (U.S. Patent Appl. Pub. No. 2006/0273347)

Hikita was published on December 7, 2006, which more than a year before the '508 patent's earliest possible priority date of April 8, 2009. RX-0041 Cover. Thus, *Hikita* is prior art under pre-AIA § 102(b). As discussed below, *Hikita* in view of *Sheppard* and *Beach624* renders obvious claim 1.

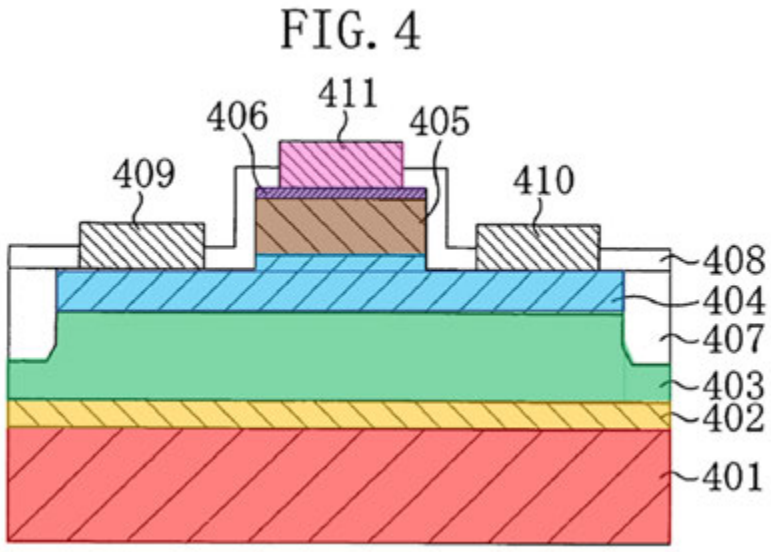
Hikita discloses an enhancement-mode GaN transistor, which means it is "normally OFF." *Id.* ¶¶ [0011], [0038]. *Hikita*'s enhancement-mode GaN transistor includes a substrate 101, a buffer layer 102, an undoped GaN layer 103, an undoped AlGaN layer 104, and a p-type GaN layer 105, a heavily doped p-type GaN layer 106, a gate electrode 111, source electrode 109, and drain electrode 110. *Id.* ¶¶ [0033]-[0035]; Tr. (Lebby) 895:18-896:3. These elements appear in the annotated version of Figure 1 below.



RX-0041 Fig. 1 (annotated).

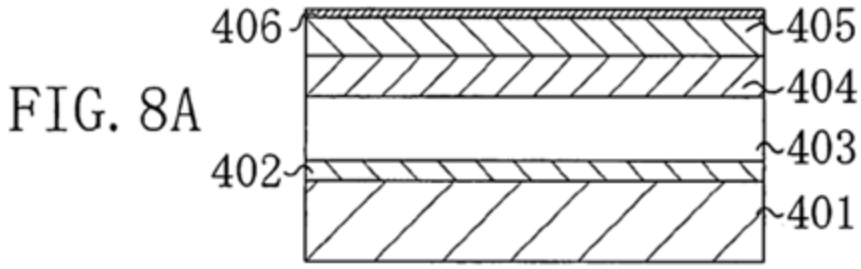
Hikita also discloses a very similar transistor structure having just one doped p-type GaN layer 105 instead of two doped p-type GaN layers 105 and 106 as shown in Figure 1 above. *Id.* ¶ [0040]. *Hikita* explains "it is not necessary that the heavily doped p-type GaN layer 106 is provided." *Id.* ¶ [0040].

Hikita further discloses a transistor structure having a doped p-AlGaN layer 405 instead of doped p-GaN layer 105. *Id.* ¶¶ [0048]-[0049]. In that embodiment, *Hikita* describes an enhancement-mode GaN transistor with a substrate 401, a buffer layer 402, an undoped GaN layer 403, an undoped AlGaN layer 404, and a p-type AlGaN layer 405, a heavily doped p-type GaN layer 406, a gate electrode 411, source electrode 409, and drain electrode 410. *Id.* ¶¶ [0048]-[0049]. These elements appear in in the annotated version of Figure 4 below.



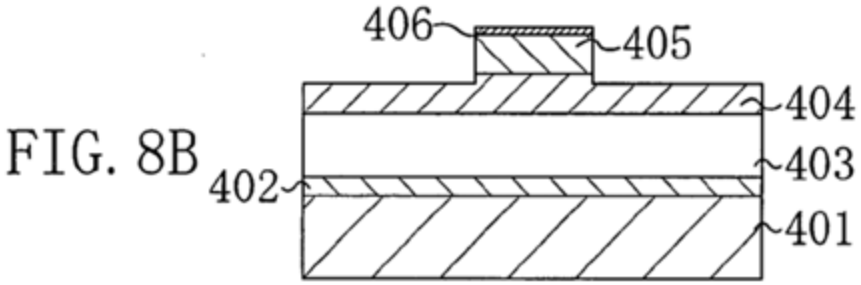
***Id.* Fig. 4 (annotated).**

Additionally, *Hikita* describes processes to form such GaN transistors, as Figures 8A-8F show, for example. *Id.* ¶ [0013]; Tr. (Lebby) 895:18-896:3. First, epitaxial layers grow on a substrate 101/401, as in Figure 8A. RX-0041 ¶ [0033]. This includes growing buffer layer 102/402, undoped GaN layer 103/403, undoped AlGaN layer 104/404, p-GaN layer 105 or a p-type AlGaN layer 405, and optional p-type GaN layer 106/406 (in that order) on a substrate. *Id.* ¶¶ [0013], [0033], [0056].



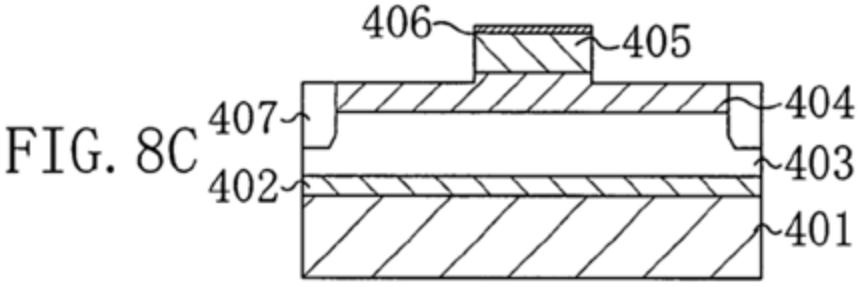
RDX-0013.95; RX-0041 Fig. 8A.

Second, layer 105/405 and p-type GaN layer 106/406, collectively, are etched away except in the gate region, as Figure 8B shows below. RX-0041 ¶¶ [0035], [0057].



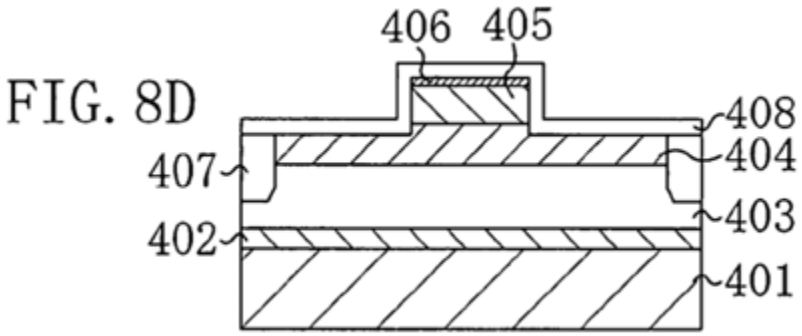
RDX-0013.95; RX-0041 Fig. 8B.

Third, an isolation region 407 is formed by implanting boron into parts of the undoped AlGaN layer 104/404 and undoped GaN layer 103/403, blocking the remaining regions of the device with photoresist, as in Figure 8C. RX-0041 ¶¶ [0036], [0058].



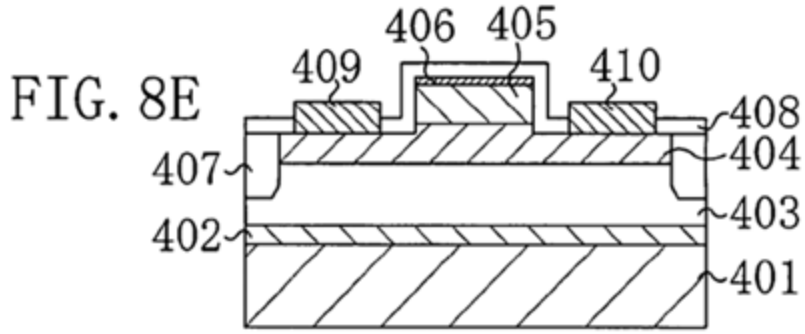
RDX-0013.95; RX-0041 Fig. 8C.

Fourth, a SiN film 108/408 is formed to cover the upper surface of the wafer, as in Figure 8D below. RX-0041 ¶¶ [0034], [0037], [0059].



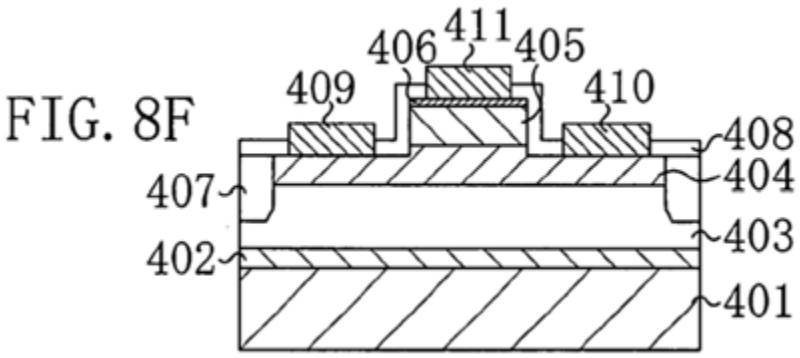
RDX-0013.95; RX-0041 Fig. 8D.

Fifth, openings are formed in SiN film 108/408, and source electrode 109/409 and drain electrode 110/410 are formed in those openings, as in Figure 8E below. RX-0041 ¶¶ [0034], [0037], [0060]. The source and drain electrodes are then annealed. *Id.* ¶ [0060]. *Hikita* does not specify if these steps are done through an etching or liftoff process. *Id.* ¶¶ [0034], [0037], [0060].



RDX-0013.95; RX-0041 Fig. 8E.

Finally, an opening is formed in the upper surface of SiN film 108/408, and a gate electrode 111/411 is formed in the opening, as Figure 8F shows below. RX-0041 ¶¶ [0013], [0061]. The result is an enhancement-mode GaN transistor structure like the one below.



RDX-0013.95; RX-0041 Fig. 8F.

b. *Sheppard* (U.S. Patent No. 7,238,560)

Sheppard was issued on July 3, 2007, which is more than a year before the '508 patent's earliest possible priority date of April 8, 2009. RX-0288 Cover. Thus, *Sheppard* is prior art under pre-AIA § 102(b). As discussed below, *Hikita* in view of *Sheppard* and *Beach624* renders obvious claim 1.

Sheppard discloses growing a channel layer 20, a barrier layer 22, and a cap layer 24 on a substrate 10 to form a GaN transistor, as Figure 3 shows below. *Id.* 6:45-8:54; Tr. (Lebby) 896:5-17. *Sheppard* also teaches that the GaN transistor can include multiple transition layers (not shown) on the substrate. RX-0288 6:58-7:7, 7:25-32; Tr. (Lebby) 896:5-17. *Sheppard* explains that the additional transition layers provide a strain balancing effect. RX-0288 6:58-7:7.

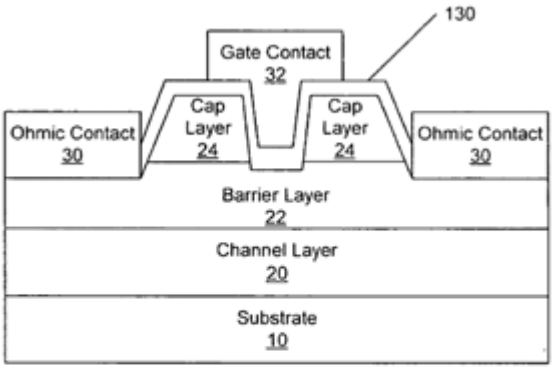


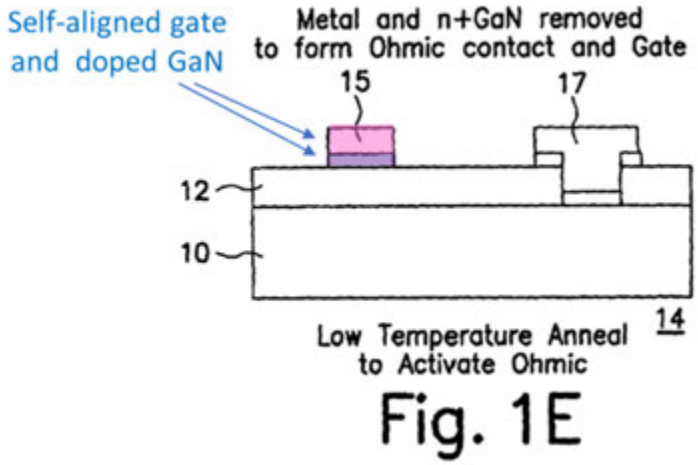
Figure 3

***Id.* Fig. 3.**

c. *Beach624* (International Patent Appl. Pub. No. WO 2005/057624)

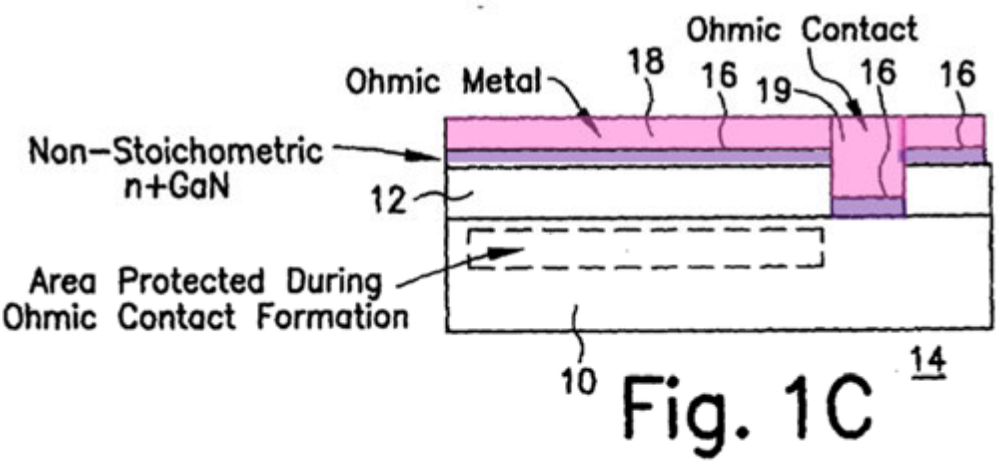
Beach624 was published on June 23, 2005, which more than a year before the '508 patent's earliest possible priority date of April 8, 2009. RX-0286 Cover. Thus, *Beach624* is prior art under pre-AIA § 102(b). As discussed below, *Hikita* in view of *Sheppard* and *Beach624* renders obvious claim 1.

Beach624 discloses a GaN device including a GaN layer 10, an AlGaN layer 12, a doped GaN layer 16, a gate contract 15, and an ohmic contact 17. *Id.* ¶¶ [0040]-[0049]; Tr. (Lebby) 896:19-897:2. Annotated Figure 1E below illustrates these features. As this figure shows, the gate contact 15 is self-aligned with the doped GaN layer immediately underneath it. RX-0286 ¶¶ [0047]-[0048]; Tr. (Lebby) 896:19-897:2.



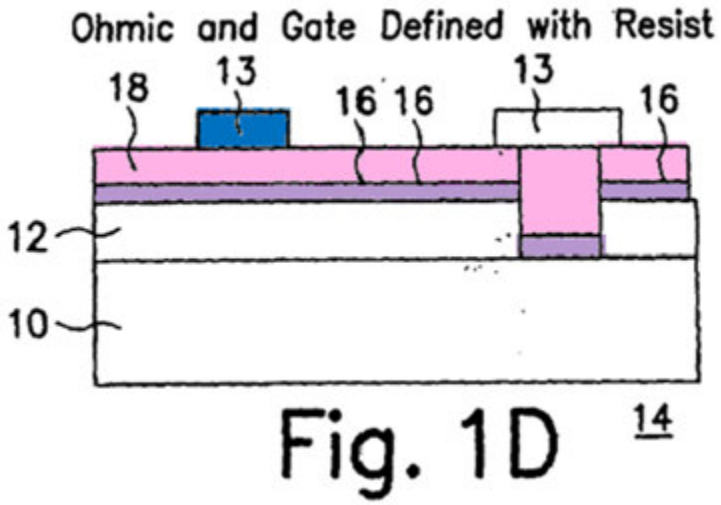
RDX-0013.92; RX-0286 Fig. 1E (annotated).

Dr. Schubert admits that *Beach624* removes metal and n+GaN to form the ohmic contacts. Tr. (Schubert) 973:14-21. *Beach624* discloses patterning the self-aligned gate and doped GaN layer by the following steps. First, deposit Ohmic material 18 over doped GaN layer 16, as Figure 1C shows below. RX-0286 ¶ [0045].



RDX-0013.100; RX-0286 Fig. 1C (annotated).

Second, pattern a photoresist 13 over ohmic material 18, as Figure 1D shows below. RX-0286 ¶ [0047].



RDX-0013.101; RX-0286 Fig. 1D (annotated).

Third, etch **ohmic material 18** and **doped GaN layer 16** using the gate photoresist pattern, as Figure 1E shows below. RX-0286 ¶¶ [0047], [0049].

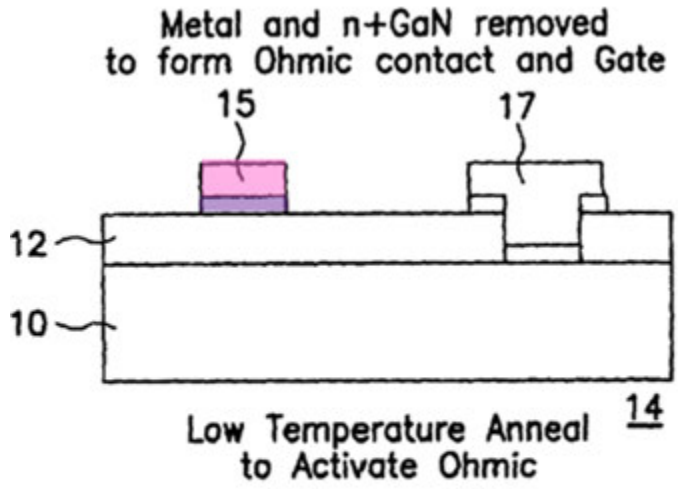


Fig. 1E

RDX-0013.102; RX-0286 Fig. 1E (annotated).

Finally, remove the photoresist 13, as Figure 1E shows above. RX-0286 ¶ [0049].

Beach624 also discloses applying an ohmic contact photoresist pattern to form the ohmic source/drain contacts. As Figures 1D and 1E show below, *Beach624* discloses applying an ohmic contact photoresist pattern over ohmic material 18, and then etching the ohmic material 18 away except where protected by the ohmic contact photoresist pattern. After etching ohmic material 18, photoresist 13 is removed, leaving behind an ohmic contact 17. *Id.* ¶ [0047].

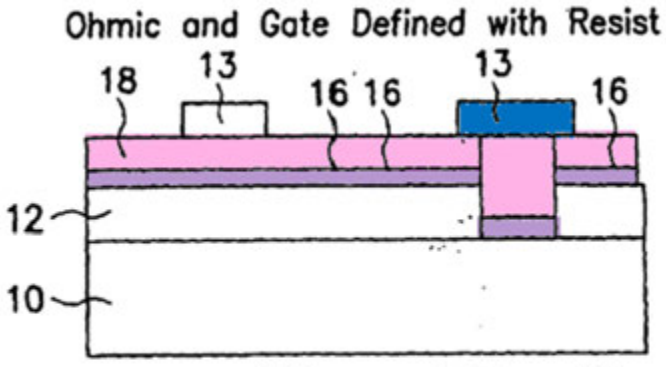
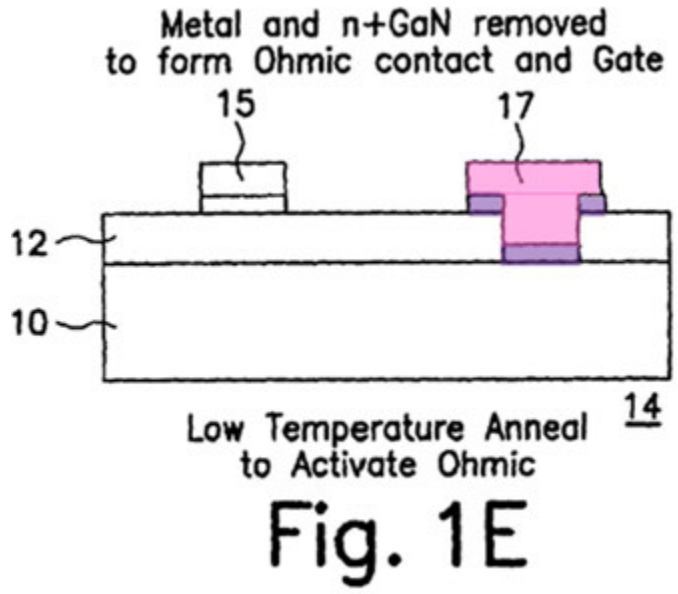


Fig. 1D



RDX-0013.102; RX-0286 Figs. 1D, 1E (annotated).

4. *Hikita* Ground Invalidates Claim 1: *Hikita* in View of *Sheppard* and *Beach624* Renders Claim 1 Obvious.

Hikita in view of *Sheppard* and *Beach624* renders claim 1 obvious. Tr. (Lebby) 890:8-891:5. *Hikita* discloses the structure of the device in claim 1, including a substrate, a transition layer, an EPI layer, a barrier layer, a p-GaN layer, gate metal, and source and drain contacts. *Id.* 895:18-896:3. While *Hikita* does not explicitly disclose forming multiple transition layers ([1a]), *Sheppard* renders this obvious. *Id.* 896:5-17. *Hikita* also does not explicitly disclose the masking steps to form the gate contact and ohmic contacts in claim 1, but *Beach624* discloses these masking processes. *Id.* 899:23-900:1. It would have been obvious to use *Beach624*'s masking processes to form *Hikita*'s device. *Id.* 907:17-910:24.

a. A POSITA would have been motivated to form *Sheppard*'s multiple transition layers in *Hikita*'s transistor

Hikita discloses nucleating and growing a transition layer on a substrate to form an enhancement-mode GaN transistor. RX-0041 ¶¶ [0013], [0033]. A POSITA would have found it obvious to grow multiple transition layers from *Hikita* alone, as growing multiple layers was

common in the art. Tr. (Lebby) 904:23-905:9. Further, a POSITA would have found it obvious to nucleate and grow multiple transition layers on a substrate based on *Sheppard*'s teachings. *Id*. 905:11-21.

Hikita teaches growing a transition layer (an AlN buffer layer 102) over a substrate 101 by epitaxial growth. RX-0041 ¶¶ [0013], [0033]. *Hikita* explains that substrate 101 is sapphire, for example. RX-0041 ¶¶ [0045], [0056]. *Sheppard* teaches growing multiple transition layers on the sapphire substrate. RX-0288 7:19-32. *Sheppard* further explains that providing "strain balancing transition layer(s)," in addition to an "AlN buffer layer," on a sapphire substrate provides a strain balancing effect. *Id*. 6:58-7:7, 7:19-24.

A POSITA would have been motivated and found it obvious to grow multiple transition layers when making *Hikita*'s device structure, as *Sheppard* teaches. Tr. (Lebby) 905:11-21. *Hikita* and *Sheppard* are both directed to forming GaN transistors with a multilayered epitaxial structure. RX-0041 ¶¶ [0033], [0034]; RX-0288 6:45-8:54.

b. A POSITA would have been motivated to use *Beach624*'s processes for forming the gate and ohmic contacts in *Hikita*

i. Elements [1e] through [1i] – Gate Formation

Hikita discloses forming a gate contact over a p-type GaN layer to produce an enhancement-mode GaN transistor. RX-0041 ¶ [0061], Figs. 8E-8F. A POSITA would have found it obvious to form *Hikita*'s gate contact using the etching technique of *Beach624*—depositing a gate contact layer, applying a gate contact photoresist pattern, etching the gate contact layer outside the gate region, and removing the gate contact photoresist pattern. Tr. (Lebby) 907:17-910:24.

Hikita discloses forming a gate contact over a p-type GaN layer in an opening of in a SiN film. RX-0041 ¶ [0061], Figs. 8E-8F; Tr. (Lebby) 907:20-23. *Beach624* discloses the steps of depositing a gate contact layer over a doped GaN layer, applying a gate contact photoresist pattern,

etching the gate contact layer outside the gate region, and removing the gate contact photoresist pattern to form the gate contact. RX-0286 ¶¶ [0045], [0047]-[0049], Figs. 1C-1E; Tr. (Lebby) 907:23-25.

A POSITA would have been motivated to use *Beach624*'s etching technique to form the gate contact in *Hikita*. Tr. (Lebby) 908:4-909:8. A POSITA would have understood that there were only two alternative techniques that could be used to pattern *Hikita*'s gate contact in the designated region, which had been known and used in the semiconductor industry for decades—etching or liftoff. *Id.* 908:4-11. Indeed, the '508 patent itself recognizes these two alternative techniques for gate formation. JX-0015 2:3-5 ("The second mask is used to form the gate metal either by patterning and lifting off the gate metal or by patterning and etching the gate metal."). Given this limited choice, a POSITA would certainly have chosen etching for the known benefits etching provided. And *Hikita* already suggests using etching to form its gate. Tr. (Lebby) 908:12-18.

Beach624 discloses an etching technique. *Id.* 908:18-19. The *Beach624* etching technique involves depositing a gate contact layer, patterning a photoresist in the gate region, etching away the gate contact layer outside the gate region, and removing the gate contact photoresist pattern. RX-0286 ¶¶ [0045], [0047]-[0049].

The alternative technique is called liftoff, which involves forming a photoresist pattern on the surface outside the gate region, depositing a gate contact layer, and removing the photoresist together with the portions of the gate contact layer above it, leaving the gate contact in the exposed gate region. Tr. (Lebby) 909:20-23.

Metal etching was routine, conventional, and well understood in the art at the time of the invention. *Id.* 908:20-909:8. Further, metal etching was used in high volume production and led to a high patterning precision, while lift-off was used in small scale production. *Id.* In view of these

two available techniques, each of which has its own pros and cons, a POSITA would have found it obvious to use the *Beach624* etching technique as part of a simple and routine design choice frequently encountered when patterning any metal layer. *Id*. 907:17-910:24. A POSITA would have been motivated to use *Beach624*'s etching technique to form the gate contact in *Hikita*'s device because the *Beach624* etching technique offers several advantages, including higher production volume and higher patterning precision, compared to the lift-off technique. *Id.* 908:20-909:8. A POSITA thus would have been motivated to use *Beach624*'s etching technique to form *Hikita*'s gate contact when favoring performance over simplicity in choosing between these two competing techniques. *Id.* 908:20-909:8.

A POSITA also would have reasonably expected success when performing *Beach624*'s etching technique to form *Hikita*'s gate contact. *Id.* 909:25-910:24. As explained above, the etching technique was well known and conventional decades before the '508 patent. Additionally, the material used for *Hikita*'s gate contact is palladium (Pd), and a POSITA would have understood that etching Pd was common in the semiconductor industry and presented no special issues. RX-0041 ¶¶ [0034], [0061]. A POSITA would have understood the benefits of forming *Hikita*'s gate contact using etching technique described by *Beach624*, according to the known, routine process of transferring a photoresist pattern by etching. Using *Beach624*'s etching technique to etch *Hikita*'s gate contact would have involved nothing more than applying conventional techniques in their ordinary and expected manner, because using the etching technique to form a patterned metal layer in a semiconductor device was routine, conventional, and well understood in the art. Tr. (Lebby) 909:25-910:24. Thus, a POSITA would have reasonably expected to succeed in using *Beach624*'s etching technique to pattern *Hikita*'s gate contact. *Id.* 909:25-910:24.

ii. Elements [1e] through [1i] – Self-Aligned Process

The parties agree that under any proposed construction for elements [1e] through [1i], the claim requires a self-aligned process. Tr. (Lebby) 884:2-10, 884:11-21; Tr. (Schubert) 970:3-11. *Beach624* discloses a self-aligned process, which is not disputed by EPC. RX-0286 ¶¶ [0045], [0047]-[0049], Figs. 1C-1E. A POSITA would have found it obvious to implement *Beach624*'s self-alignment process to form self-aligned gate contact and doped GaN layers in *Hikita*'s device. Tr. (Lebby) 907:17-910:24.

A POSITA would have been motivated and found it obvious to use *Beach624*'s self-alignment process to form the gate contact and p-type GaN layers in *Hikita*'s device. *Hikita* and *Beach624* are both directed to a method for forming a GaN-based transistor. RX-0041 ¶¶ [0013], [0033], [0038], [0040], [0055]-[0061]; RX-0286 ¶¶ [0002], [0017]-[0018]. Like *Hikita*, *Beach624* discloses a GaN-based device with multiple epitaxial layers of III-nitride material. RX-0286 ¶¶ [0040]-[0043]. Also like *Hikita*'s device, *Beach624*'s device has a gate contact 15 and ohmic contacts 17. RX-0286 ¶¶ [0048]-[0049]. To improve *Hikita*'s device and its manufacture, a POSITA would have been motivated to use the *Beach624*'s self-alignment process to pattern *Hikita*'s gate contact and doped GaN layers. Tr. (Lebby) 907:17-910:24.

A POSITA would have been motivated to use the *Beach624* self-alignment process to form the gate contact and p-type GaN layer in *Hikita*'s device because *Beach624*'s self-alignment process effectively achieves *Hikita*'s objective that the doped GaN layer is removed except the gate region. RX-0041 ¶¶ [0035], [0057]; Tr. (Lebby) 907:17-910:24. A POSITA would have recognized that *Beach624*'s self-alignment process automatically achieves alignment between the gate contact and the doped GaN layer, thereby improving gate alignment in *Hikita*'s device while simplifying and speeding its manufacture. RX-0286 Fig. 1E; RX-0041 Fig. 1; Tr. (Lebby) 907:17-910:24. A POSITA would have appreciated that self-aligned gate and doped GaN layers are

desirable in GaN devices, and he or she would have been motivated to implement *Beach624*'s self-alignment process to achieve a self-aligned gate arrangement in *Hikita*'s device. Tr. (Lebby) 907:17-910:24.

A POSITA also would have been motivated to use the *Beach624*'s self-alignment process to form the gate contact and p-type GaN layers in *Hikita*'s device because *Beach624*'s self-alignment process simplifies *Hikita*'s process, which patterns the gate contact and doped GaN layer separately. *Id*. 910:9-24. Compared to *Hikita*'s process, which applies two separate photoresist layers and two separate alignment steps to pattern the gate contact and doped GaN layer, *Beach624*'s self-alignment process uses a single photoresist layer and a single alignment step to pattern the gate contact and doped GaN layer. RX-0286 ¶ [0047]. A POSITA would have understood that eliminating one of those photoresist patterning sequences would simplify the manufacturing process and reduce manufacturing costs. Tr. (Lebby) 908:20-909:8. Accordingly, a POSITA would have been motivated to use *Beach624*'s self-alignment process to produce *Hikita*'s device because doing so would simplify the manufacturing process and save cost. *Id*. 908:20-909:8

A POSITA also would have reasonably expected to succeed in applying *Beach624*'s self-alignment process to pattern *Hikita*'s gate contact and p-type GaN layer. *Id*. 909:25-910:24. Applying a single photoresist to pattern the gate contact and doped GaN layer was well known and conventional when the '508 patent was filed. *Id*. 909:10-23. Additionally, both *Hikita*'s and *Beach624*'s devices use GaN for the layer underneath the gate contact. *Hikita*'s device could have been formed easily by using the self-alignment process described by *Beach624*, according to the known, routine process of transferring a photoresist pattern by etching. *Id*. Using *Beach624*'s self-alignment process to pattern *Hikita*'s gate contact and doped GaN layer would have required

nothing more than applying conventional techniques in their ordinary and expected manner, because patterning different layers in a GaN-based transistor using the same photoresist pattern was routine, conventional, and well understood in the art. *Id*. 909:10-910:24. Dr. Lebby explained that, to incorporate the self-aligned process to form *Hikita*'s gate structure, a POSITA would have simply implemented *Beach624*'s self-alignment process at step Figure 8A of *Hikita*, such that the self-aligned gate structure is formed before the ohmic contacts. *Id*. 910:15-24. *Hikita* expressly teaches forming the gate contact before the formation of the dielectric layer, enabling to incorporate *Beach624*'s self-alignment process at step Figure 8A of *Hikita*. *Id*. 910:3-14; RX-0041, ¶ [0061] ("the gate electrode 411 may be formed before formation of the SiN film 408"). Thus, a POSITA would have reasonably expected to succeed in using *Beach624*'s self-alignment process to pattern *Hikita*'s gate contact and p-type GaN layer. *Id.*

iii. Elements [1n] through [1r] – Ohmic Formation

Hikita discloses forming source and drain ohmic contacts in openings of a dielectric layer to produce an enhancement-mode GaN transistor. RX-0041 ¶¶ [0034], [0060], Figs. 8A-8F. A POSITA would have found it obvious to form *Hikita*'s ohmic source and drain contacts by performing the steps of depositing an ohmic contact metal, applying a metal photoresist pattern, etching the ohmic contact metal, and removing the metal photoresist pattern, as *Beach624* teaches. Tr. (Lebby) 912:21-913:3.

Hikita discloses forming ohmic source and drain contacts in openings of in a SiN film. RX-0041 ¶¶ [0034], [0060], Figs. 8D-8E. To form the ohmic contact metal, *Beach624* teaches the steps of depositing an ohmic contact metal, applying a metal photoresist pattern, etching the ohmic contact metal, and removing the metal photoresist pattern. RX-0286 ¶¶ [0045], [0047]-[0049], Figs. 1C-1E. This is essentially the same etching technique discussed above with respect to

forming *Hikita*'s gate contact, the difference being that the etching technique is used to form the ohmic source and drain contacts instead of the gate contact. Tr. (Lebby) 912:21-913:3.

A POSITA would have been motivated and found it obvious to use *Beach624*'s etching technique to form *Hikita*'s ohmic source and drain contacts for the same reasons discussed above with respect to forming *Hikita*'s gate contact. *Id*. 912:21-913:3. Like the gate contact, a POSITA would have understood the two competing techniques available to pattern *Hikita*'s ohmic source and drain contacts in the designated regions were the *Beach624* etching technique and liftoff. Again, a POSITA would have been motivated to use *Beach624*'s etching technique to form the ohmic source and drain contacts in *Hikita*'s device because the etching technique offers several advantages compared to lift-off, such as better control and removal of unwanted metal material, as explained in the previous section. *Id*. 907:17-910:24. In addition, a POSITA would have understood that the etching process would be desirable when as in *Hikita*, the ohmic contacts are to be annealed. RX-0041 ¶ [0060]. A POSITA thus would have been motivated to use *Beach624*'s etching technique to pattern *Hikita*'s source and drain contacts when favoring performance over simplicity in choosing between these two competing techniques. Tr. (Lebby) 907:17-910:24.

A POSITA also would have reasonably expected to succeed in applying *Beach624*'s etching technique to pattern *Hikita*'s ohmic source and drain contacts. *Id*. 912:21-913:3. As explained above, the etching technique was well-known and conventionally used for decades before the '508 patent. *Id*. 908:4-11. Additionally, the materials used to make *Hikita*'s ohmic source and drain contacts are Titanium (Ti) and Aluminum (Al), and a POSITA would have understood that etching of Ti and Al was commonly done in the semiconductor industry and presented no special issues. RX-0041 ¶¶ [0034], [0060]. *Hikita*'s ohmic source and drain contacts could be formed easily by applying the *Beach624* etching technique according to the known,

routine process of transferring a photoresist pattern by etching. Tr. (Lebby) 912:21-913:3. Using *Beach624*'s etching technique to etch *Hikita*'s ohmic source and drain contacts would have required nothing more than applying conventional techniques in their ordinary and expected manner, because using the etching technique to pattern metal layers in a semiconductor device was routine, conventional, and well understood in the art. *Id*. 908:18-19. Thus, a POSITA would have reasonably expected to succeed in using *Beach624*'s etching technique to pattern *Hikita*'s ohmic source and drain contacts. *Id*. 912:21-913:3.

c. [1pre]: A method of forming an enhancement mode GaN transistor

To the extent the preamble is limiting, *Hikita* discloses it. *Id*. 902:25-903:4.

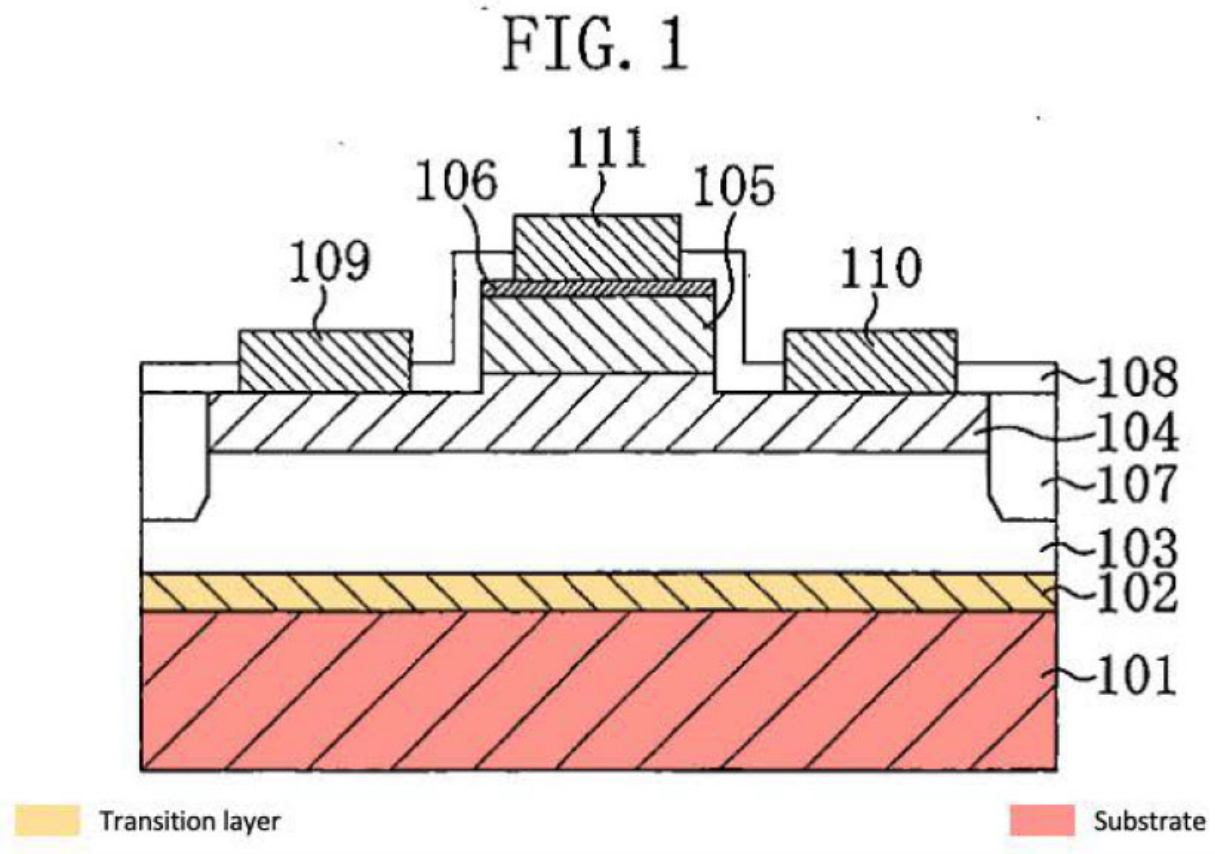
Hikita discloses a "normally OFF type" (enhancement mode) GaN transistor with a p-type GaN layer below the gate. RX-0041 ¶ [0038], Fig. 1. A POSITA would have understood that, with such structure, *Hikita*'s transistor is an enhancement-mode GaN transistor. Tr. (Lebby) 903:2-4. The '508 patent also confirms that "Enhancement mode devices are normally off." JX-0015 1:48-51.

Hikita further discloses a method of forming such an enhancement-mode GaN transistor, including growing epitaxial layers over a substrate and etching the p-type GaN layer with dry etching. RX-0041 ¶¶ [0013], [0035], [0055]-[0061], Figs. 8A-8F.

d. [1a]: nucleating and growing transition layers on a substrate

Hikita in view of *Sheppard* renders obvious nucleating and growing transition layers on a substrate. Tr. (Lebby) 903:6-12; 904:23-905:9. *Hikita* discloses an aluminum nitride buffer layer 102 on a substrate 101. RX-0041 ¶¶ [0033].

The manufacture of *Hikita*'s device involves growing an epitaxial AlN buffer layer 102 over a substrate 101, as Figure 1 shows below. *Id*. ¶¶ [0013], [0033]. *Hikita* also teaches that the substrate 101 is sapphire. *Id.* ¶¶ [0045], [0056].



RDX-0013.82; RX-0041 Fig. 1 (annotated).

The AlN buffer layer 102 is a transition layer because it is an intermediate layer between the substrate 101 and the undoped GaN layer 103. Tr. (Lebby) 903:8-12. The '508 patent describes the claimed transition layers as being located directly above the substrate and underneath the undoped GaN layer. JX-0015 3:26-29. *Hikita* discloses applying a MOCVD method to form the transition layer (AlN buffer layer 102) on the sapphire substrate. RX-0041 ¶¶ [0033], [0056]. A POSITA would have understood that forming a transition layer on a sapphire substrate using

MOCVD involves nucleating and growing transitions layer on the substrate. *See* RX-0288 7:29-32 (explaining that "the channel layer and/or buffer nucleation and/or transition layers may be deposited by MOCVD").

Although *Hikita* does not explicitly disclose growing multiple transition layers on a substrate, *Sheppard* does. *Sheppard* discloses a GaN transistor with multiple transition layers on a sapphire substrate. *Id*. 7:19-24. *Sheppard* teaches that providing an "AlN buffer layer" and additional "strain balancing transition layer(s)" will "provide an appropriate crystal structure transition" between the substrate and the remainder of the device. *Id*. 6:58-7:7. *Sheppard* also incorporates by reference U.S. Patent Application Publication No. 2003/0102482, which describes multiple transition layers for strain balancing. *Id*. 6:62-7:7. The '508 patent also admits that forming multiple transition layers on a substrate was known. JX-0015 1:53-64. And the '294 patent, filed on the same day as the '508 patent, also admits that it was "conventional" to include multiple transition layers over a sapphire substrate. JX-0014 1:55-60.

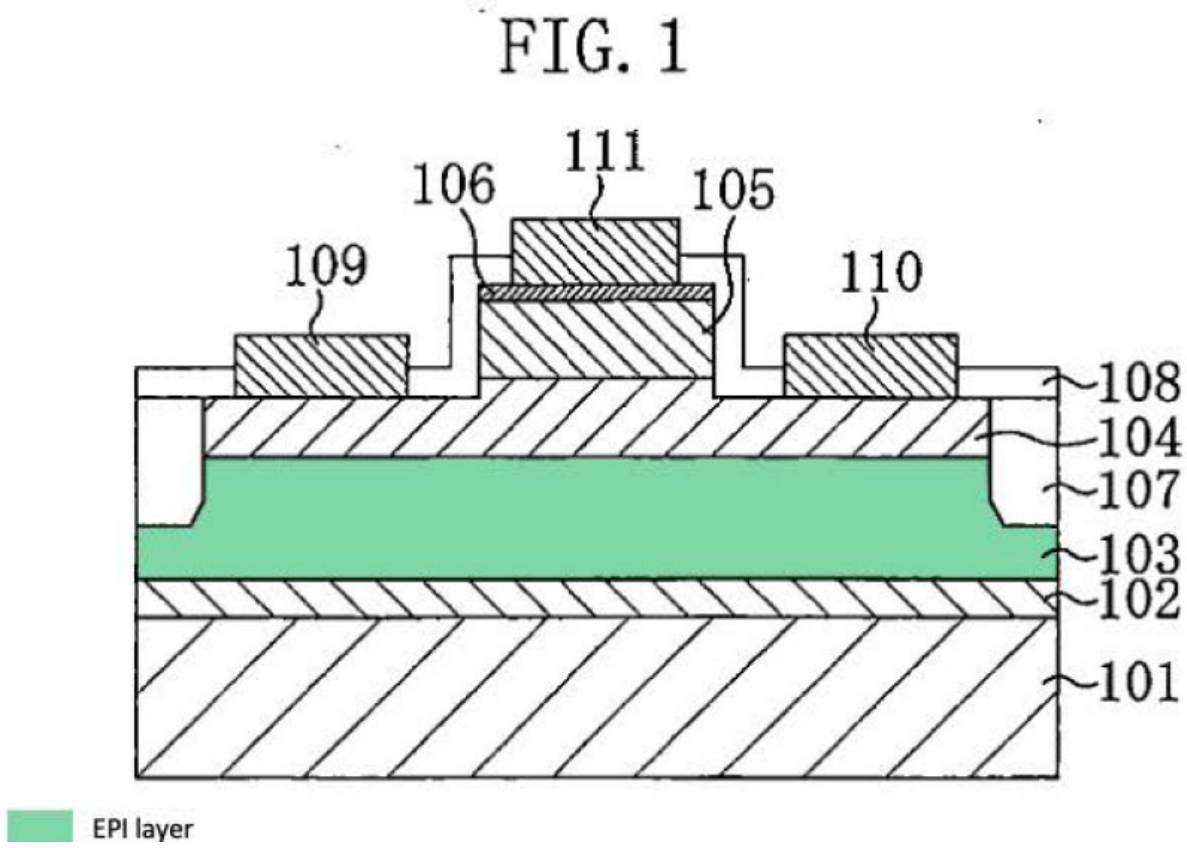
As explained in Section III.B.4.a, a POSITA would have been motivated and found it obvious to nucleate and grow multiple transition layers in *Hikita*'s device, as *Sheppard* teaches, because both *Hikita* and *Sheppard* disclose growing GaN on dissimilar substrates, such as silicon, sapphire, or silicon carbide. Tr. (Lebby) 905:11-21.

e. [1b]: growing an III Nitride EPI layer over the transistor layers

Hikita discloses growing an III Nitride EPI layer over the transition layers. *Id*. 903:14-20.

The manufacture of *Hikita*'s device structure includes epitaxially growing an undoped GaN layer 103 (the claimed "III Nitride EPI layer") over the buffer layer 102 (a transition layer), Figure 1 shows below. RX-0041 ¶¶ [0013], [0033], [0056]. A POSITA would have understood that the

undoped GaN layer is an III Nitride EPI layer because Gallium Nitride (GaN) is a III-Nitride material, and it is epitaxially grown to make transistors. Tr. (Lebby) 903:14-20.



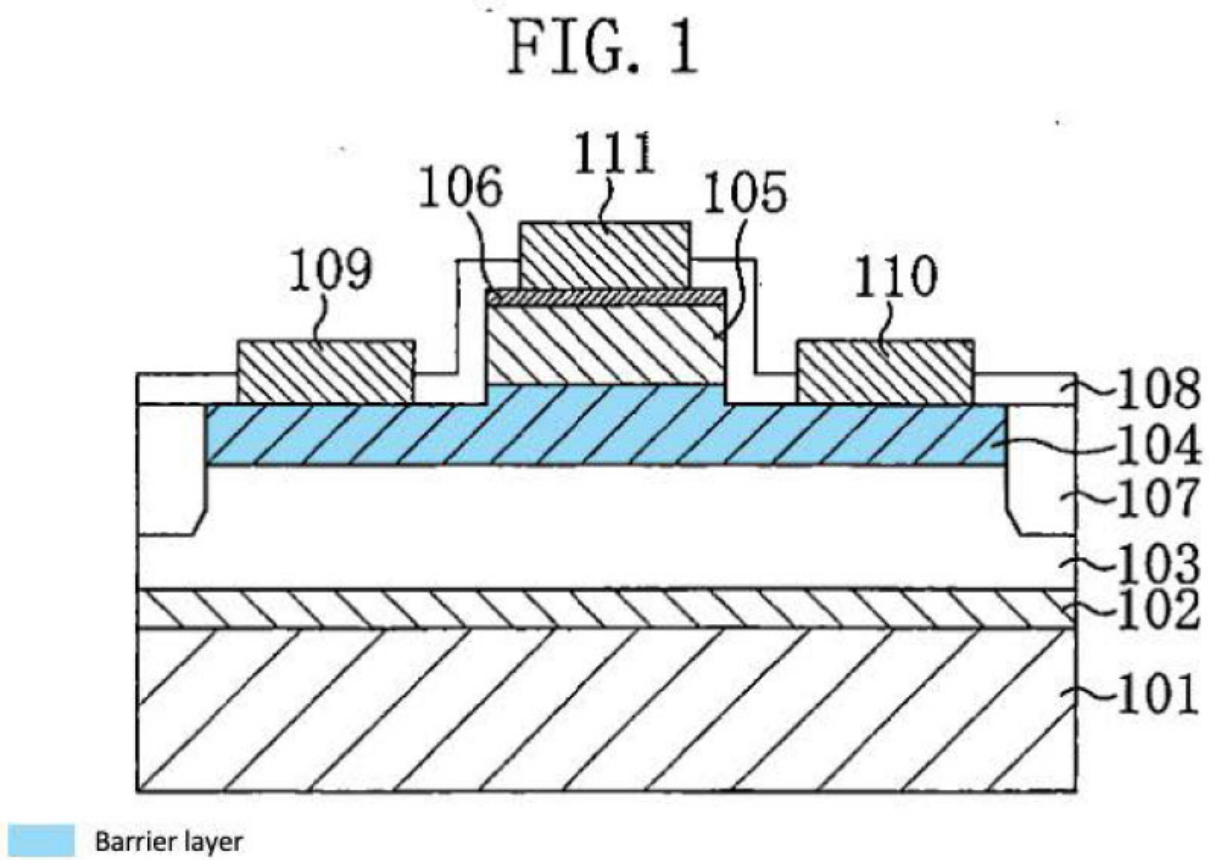
RDX-0013.83; RX-0041 Fig. 1 (annotated).

f. [1c]: growing an III Nitride barrier layer over the EPI layer

Hikita discloses growing a III Nitride barrier layer over the EPI layer. Tr. (Lebby) 903:22-904:2.

The manufacture of *Hikita*'s device structure involves growing an undoped AlGaN layer 104 (the claimed "barrier layer") over the undoped GaN layer 103 (the claimed "EPI layer"), as Figure 1 shows below. RX-0041 ¶¶ [0013], [0033], [0056]. A POSITA would have understood that *Hikita*'s undoped AlGaN layer 104 is a barrier layer because a two-dimensional electron gas forms just below bottom surface of the undoped AlGaN layer 104 where it interfaces with the

undoped GaN layer 103. *Id*. ¶¶ [0034], [0038]. A POSITA would have understood that AlGaN is a III Nitride material. Tr. (Lebby) 903:22-904:2.



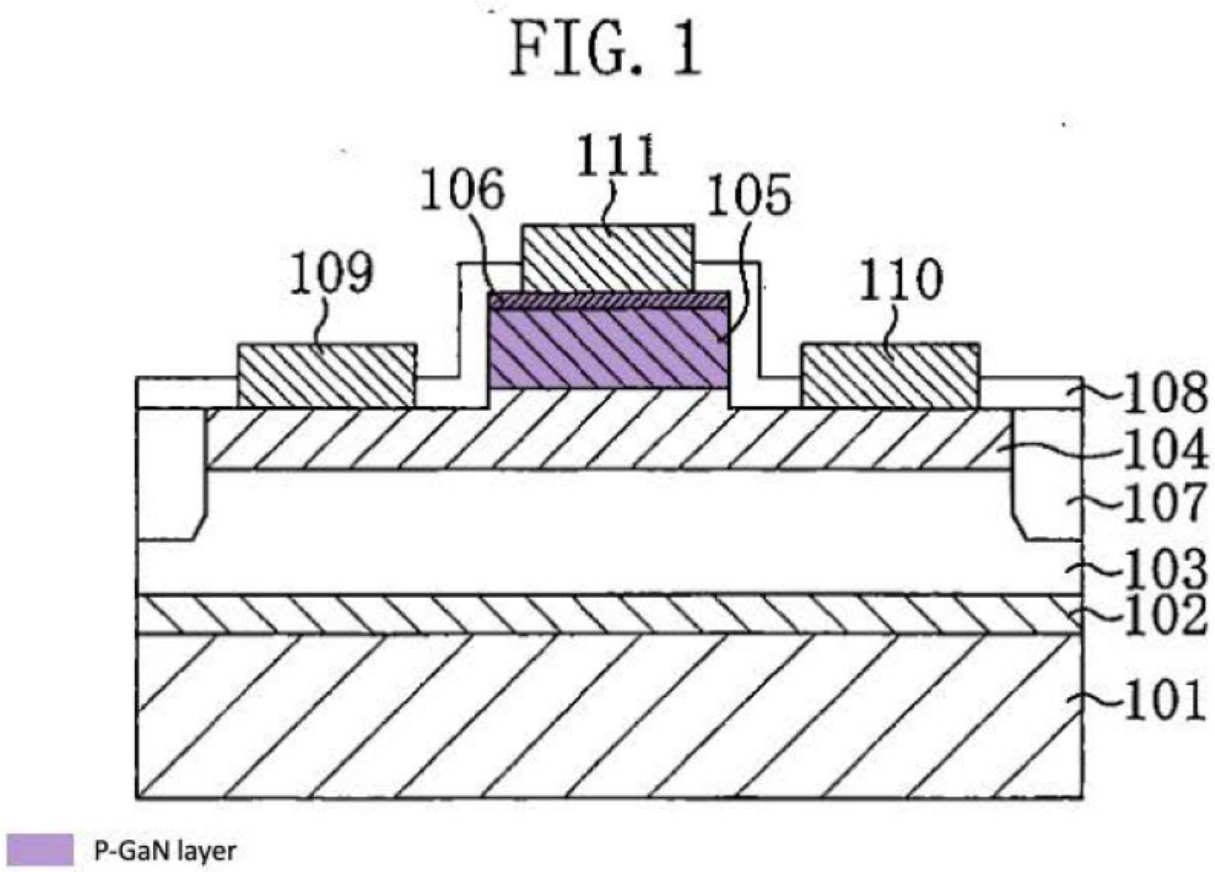
RDX-0013.84; RX-0041 Fig. 1 (annotated).

g. [1d]: growing a GaN layer with acceptor type dopants over the barrier layer

Hikita discloses growing a GaN layer with acceptor type dopants over the barrier layer. Tr. (Lebby) 904:4-14.

The manufacture of *Hikita*'s device involves growing a p-type GaN layer 105 and, optionally, a heavily doped p-type GaN layer 106 over the undoped AlGaN layer 104 (the claimed "barrier layer"), as Figure 1 shows below. RX-0041 ¶¶ [0013], [0033], [0056]. A POSITA would

have understood that these p-type GaN layers contain p-type dopants, otherwise known in the art as "acceptors." Tr. (Lebby) 904:4-14.



RDX-0013.85; RX-0041 Fig. 1 (annotated).

Hikita also discloses a transistor structure having just one p-type GaN layer 105 instead of two p-type GaN layers 105 and 106. *Hikita* states that "it is not necessary that the heavily doped p-type GaN layer 106 is provided." RX-0041 ¶ [0040].

h. [1e] through [1i]:
[1e] depositing a gate contact layer on the doped GaN layer;
[1f] applying a gate photo resistant pattern;
[1g] etching away the gate contact layer outside the gate region;
[1h] etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
[1i] removing the gate photo resistant pattern;

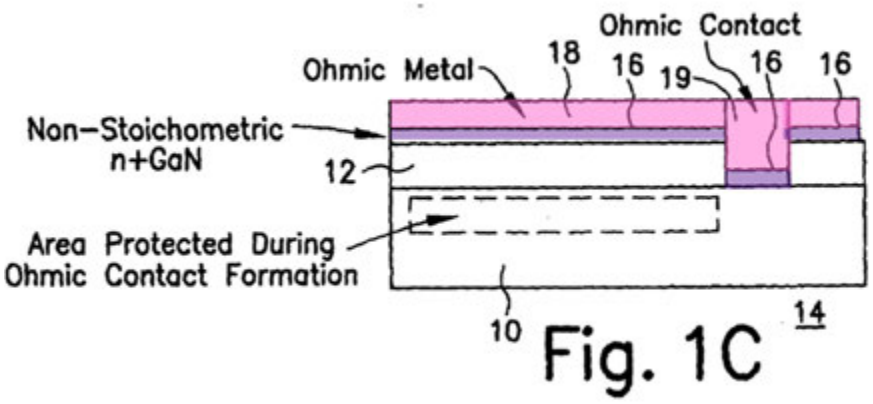
Hikita in view of *Beach624* renders obvious elements [1e] through [1i] under any proposed construction because the combination discloses performing the steps in order as a self-aligned process. Tr. (Lebby) 905:23-907:15.

Hikita explains that, to form the gate contact, part of the SiN film provided on the heavily doped p-type GaN layer is removed, and the gate contact is formed in the opening. RX-0041 ¶ [0061]. Figures 8E and 8F below show forming gate contact 411 in an opening of SiN film 408. Alternatively, the gate contact may be formed before formation of the SiN film. *Id*. ¶ [0061]. Either way, a POSITA would have understood that, to form *Hikita*'s gate contact, either the etching technique (including elements [1e], [1f], [1g], [1h], [1i]) or the liftoff technique was used. Tr. (Lebby) 908:2-909:8. *Hikita* explains that, to form p-type GaN layers 105 and 106, the portions of those p-type GaN layers "located in other part [sic] than a gate region [are] removed by selective etching." RX-0041 ¶ [0035]. Although *Hikita* may not explicitly disclose using self-aligned process to pattern the p-GaN layer and gate contact layer, *Beach* does.

RDX-0013.96; RX-0041 Figs. 8E (left, annotated), 8F (right, annotated)

Beach624 discloses a self-aligned etching technique to form a gate contact.

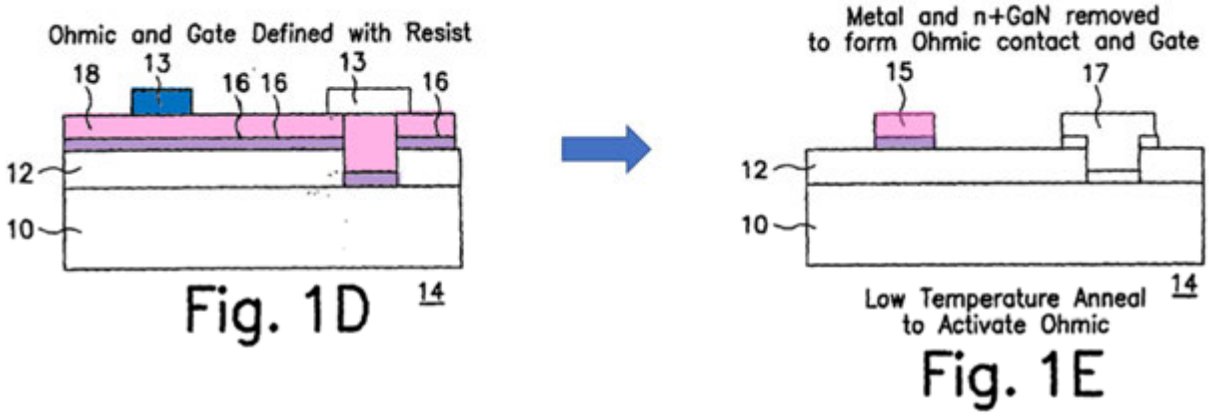
First (element [1e]), *Beach624* discloses depositing an ohmic material 18 (the claimed "gate contact layer") on a doped GaN layer 16, i.e., element [1e], as shown below. RX-0286 ¶ [0045] (explaining that "[m]aterial 18 [is] deposited over layer 16"); Tr. (Lebby) 906:8-19.



RDX-0013.90; RX-0286 Fig. 1C (annotated)

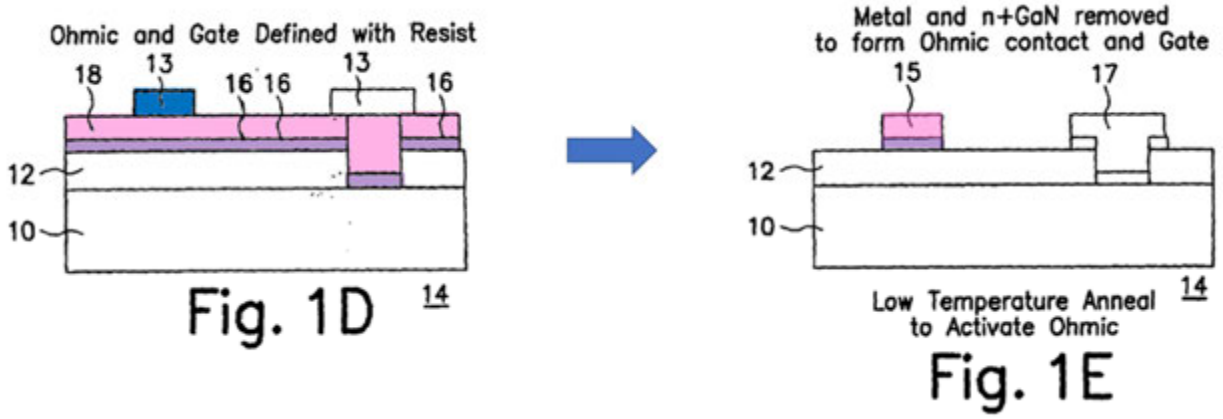
Second (element [1f]), *Beach624* discloses patterning a gate photoresist layer 13 on the wafer, i.e., step [1f], as shown below. RX-0286 ¶ [0047] (explaining that "resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17"); Tr. (Lebby) 906:21-4.

Third (element [1g]), *Beach624* discloses etching away the gate contact layer outside the gate region, i.e., step [1g], as shown below. RX-0286 ¶ [0047] ("After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13."); Tr. (Lebby) 907:6-15.



RDX-0013.92; RX-0286 Figs. 1D, 1E (annotated)

Fourth (element [1h]), *Beach624* teaches using the same photoresist pattern to perform step [1g], i.e., etching away the gate contact layer outside the gate region, and step [1h], i.e., etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact, as shown below. RX-0286 ¶ [0047] ("After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13."). By using a single photoresist pattern, the gate contact 15 and doped GaN layer 16 are self-aligned, as Figure 1E below shows. Tr. (Lebby) 905:22-907:15.



RDX-0013.92; RX-0286 Figs. 1D (left, annotated), 1E (right, annotated)

Fifth (element [1i]), *Beach624* discloses removing the gate photoresist pattern, i.e., step [1i]. RX-0286 ¶ [0049] (explaining that "[a]fter material 18 has been removed from device 14 in regions not covered by photoresist 13, photoresist 13 is stripped off"). Figure 1E above shows that the photoresist 13 is removed. Tr. (Lebby) 907:6-15.

Thus, *Beach624* teaches all steps of elements [1e] through [1i], using a single gate photoresist pattern to form both the gate contact and doped GaN layer in a self-aligned process. *Id*. 905:22-907:15.

As explained in Section III.B.4.b, a POSITA would have been motivated and found it obvious to apply *Beach624*'s self-alignment process to pattern *Hikita*'s gate contact and p-GaN

layer. Thus, *Hikita* in view of *Beach624* renders obvious elements [1e] through [1i] under both Staff's and Innoscience's constructions. *Id*. 905:22-907:15.

i. [1j] through [1m]:
[1j] depositing a dielectric layer;
[1k] applying a contact photo resistant pattern;
[1l] etching the dielectric layer to open the drain and source contact area;
[1m] removing the contact photo resistant pattern;

Hikita discloses elements [1j] through [1m]. *Id*. 911:4-16.

First (element [1j]), *Hikita* explains that, after patterning the p-type GaN layer, a "SiN film 108" is deposited to cover "an upper surface of the transistor," as shown below. RX-0041 ¶¶ [0034], [0037], [0059]. A POSITA would have understood that SiN (silicon nitride), the same dielectric material described in the '508 patent, is a common dielectric material. JX-0015 3:57-58. Thus, *Hikita* discloses step [1j], i.e., depositing a dielectric layer. Tr. (Lebby) 911:6-16.

Second (elements [1k]-[1m]), *Hikita* further discloses the use of etching to transfer openings for drain and source contacts into the dielectric layer (SiN film 108), as Figures 8D and 8E below show. RX-0041 ¶¶ [0034], [0060].

RDX-0013.98; RX-0041 Figs. 8D (left, annotated), 8E (right, annotated)

A POSITA would have understood that etching the SiN film to form openings in *Hikita*'s device requires (1) patterning a contact photoresist layer to expose only the areas of the SiN film where the openings are to be formed, (2) etching to transfer the photoresist pattern into the SiN layer, and (3) removing the contact photoresist after the openings are formed. This always has been the standard process to pattern a dielectric material in the semiconductor industry, and a POSITA

would have understood this is the process *Hikita* discloses for creating openings in the SiN film. RX-0288 8:55-67 (using a mask pattern to form openings in a cap layer 24 for the ohmic contacts), Figs. 1B-1D. Thus, *Hikita* discloses steps [1j]-[1m], i.e., depositing a dielectric layer, applying a contact photo resistant pattern, etching the dielectric layer to open the drain and source contact area, and removing the contact photo resistant pattern. Tr. (Lebby) 911:4-16.

j. [1n] through [1q]:
[1n] depositing an Ohmic contact metal;
[1o] applying a metal photo resistant pattern;
[1p] etching the Ohmic contact metal;
[1q] removing the metal photo resistant pattern; and

Hikita in view of *Beach624* renders obvious elements [1n] through [1q]. *Id*. 911:22-913:13.

Hikita further discloses forming the ohmic source and drain contacts in the openings of the SiN film, as Figures 8D and 8E below illustrate. RX-0041 ¶¶ [0034], [0060]. A POSITA would have understood that, to form the ohmic source and drain contacts in *Hikita*'s transistor, either the etching technique, or the liftoff technique would be used. For the reasons explained above, a POSITA would have been motivated to use an etching technique, like that of *Beach624* to form and pattern the source and drain ohmic contacts in *Hikita*.

RDX-0013.98; RX-0041 Figs. 8D (left, annotated), 8E (right, annotated)

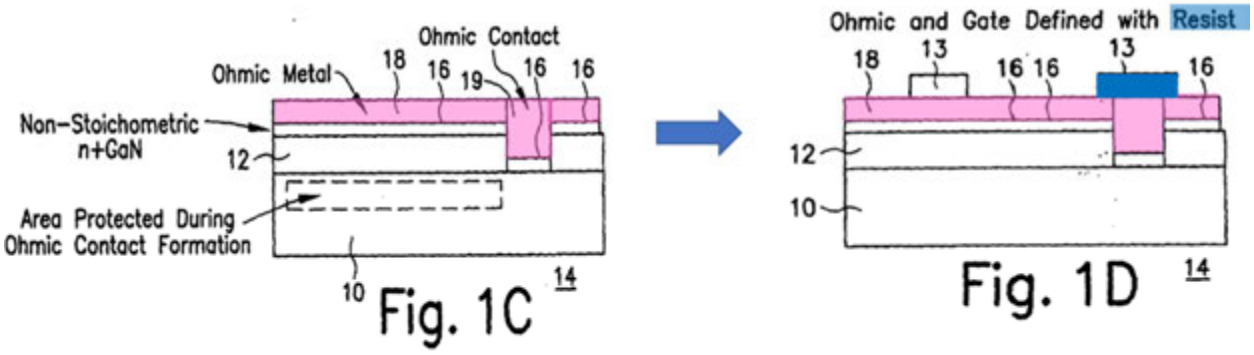
Beach624 teaches using the etching technique to form ohmic contacts.

First (element [1n]), *Beach624* teaches that an ohmic contact metal 18 is deposited over the wafer, including in Ohmic contact window 11, as Figures 1B and 1C below show. RX-0286 ¶ [0045] (explaining that "[m]aterial 18 deposited over layer 16 and in ohmic contact window 11

. . . may be an ohmic metal"). Thus, *Beach624* teaches step [1n], depositing an ohmic contact metal. Tr. (Lebby) 911:22-912:19.

RDX-0013.100; RX-0286 Figs. 1B (left, annotated), 1C (right, annotated)

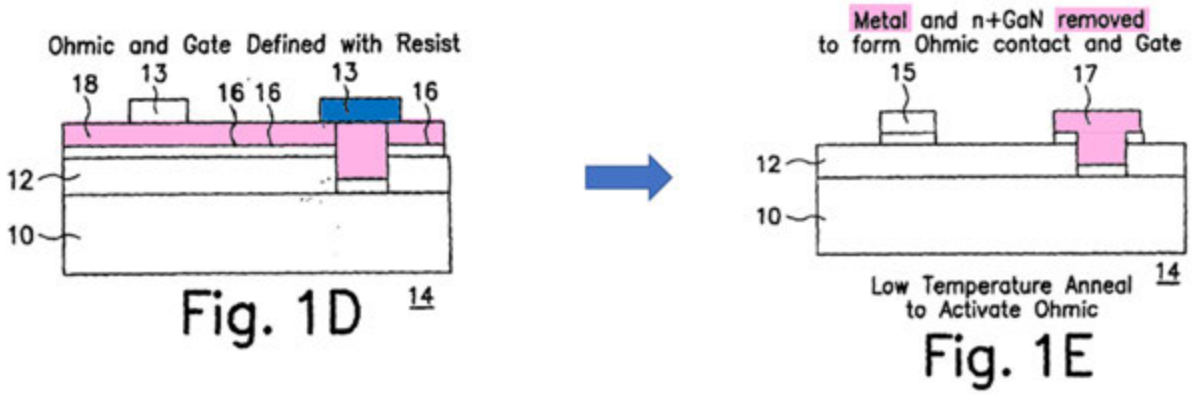
Second (element [1o]), *Beach624* teaches that a metal photoresist layer 13 is deposited and patterned over the ohmic contact metal 18, as Figures 1C and 1D below show. RX-0286 ¶ [0047] (explaining that "resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17"). Thus, *Beach624* teaches step [1o], i.e., applying a metal photoresist pattern. Tr. (Lebby) 911:22-912:19.



RDX-0013.100 (left); RDX-0013.101 (right);
RX-0286 Figs. 1C (left, annotated), 1D (right, annotated)

Third (element [1p]), *Beach624* teaches that the ohmic contact metal 18 is etched except the portion protected by metal photoresist pattern 13, as Figures 1D and 1E below show. RX-0286 ¶ [0047] ("After the deposition of photoresist layer 13, material 18 is removed, as by etching,

except where protected by photoresist 13."). Thus, *Beach624* teaches step [1p], i.e., etching the ohmic contact metal. Tr. (Lebby) 911:22-912:19.



RDX-0013.102; RX-0286 Figs. 1D (left, annotated), 1E (right, annotated).

Fourth (element [1q]), *Beach624* teaches that the metal photoresist pattern 13 is removed, as figure 1E above shows. RX-0286 ¶ [0049] ("After material 18 has been removed from device 14 in regions not covered by photoresist 13, photoresist 13 is stripped off"). Thus, *Beach624* teaches step [1q], i.e., removing the metal photo resistant pattern. Tr. (Lebby) 911:22-912:19.

Thus, *Beach624* teaches steps [1n] through [1q], i.e., using the *Beach624* etching technique to pattern the ohmic contact metals, **which Dr. Schubert admits**. Tr. (Schubert) 996:8-12.

As explained in Section III.B.4.b, a POSITA would have been motivated and found it obvious to apply *Beach624*'s etching technique to pattern *Hikita*'s ohmic source and drain contacts.

k. [1r]: performing rapid thermal annealing to form Ohmic drain and source contacts.

Hikita further discloses performing "heat treatment . . . in an N_2 atmosphere at 650° C" to form the Ohmic source and drain contacts. RX-0041 ¶¶ [0060]. Thus, *Hikita* discloses performing thermal annealing to form ohmic drain and source contacts. A POSITA would have understood that this step is a rapid thermal anneal (RTA)—a routine and conventional way to activate such ohmic contacts in GaN semiconductor processing long before the '508 patent was filed. Tr.

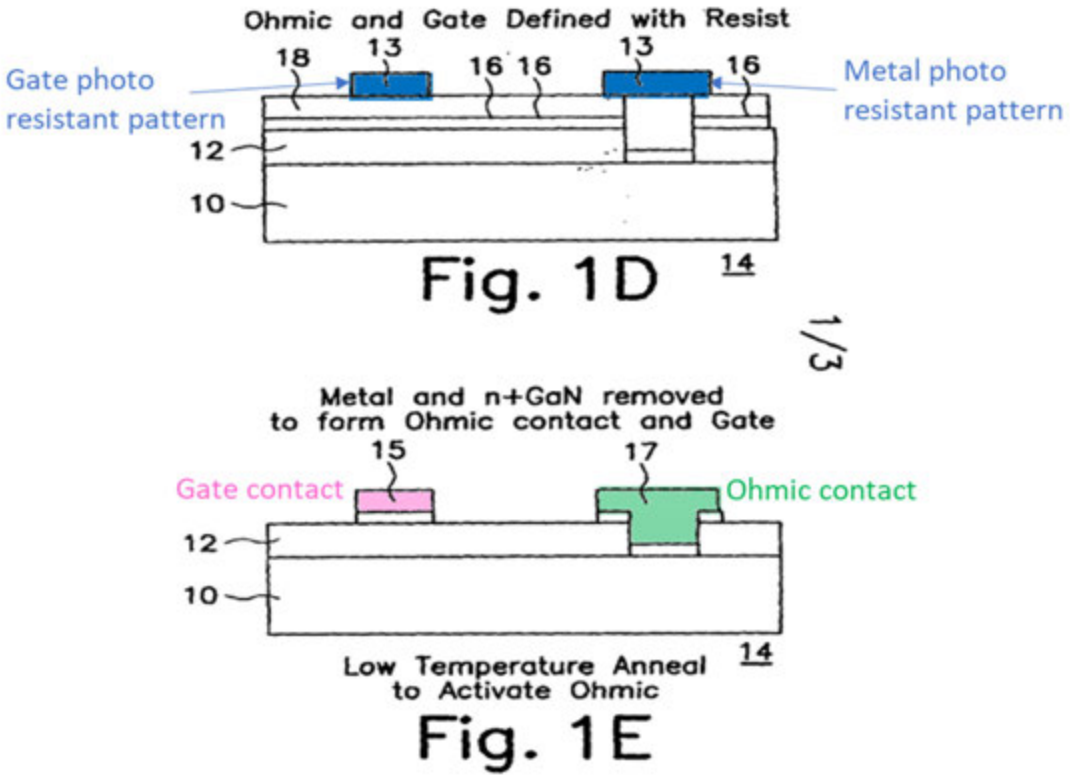
(Lebby) 913:6-13; RX-0288 10:21-38. Therefore, a POSITA would have assumed *Hikita* describes a rapid thermal anneal. *Id.* 913:6-13. Accordingly, a POSITA would have understood that *Hikita* discloses element [1r].

l. Expert Opinions: EPC fails to rebut Dr. Lebby's invalidity analysis as EPC misinterpret the claims, the prior art, and the proposed combination

EPC disputes only a single claim requirement—whether *Beach624* discloses separate gate photo resistant and metal photo resistant patterns—contradicting the disclosure of *Beach624*. The only other disputes raised by EPC misinterpret the claim as requiring a gate-first process and misinterpret the proposed combination of *Hikita* and *Beach624*.

i. *Beach624* discloses or at least suggests both a "gate photo resistant pattern" and a "metal photo resistant pattern"

Dr. Schubert argues that *Beach624* does not teach both a "gate photo resistant pattern" and a "metal photo resistant pattern" because both patterns are labeled with the same number (13) in *Beach624*. Tr. (Schubert) 1007:23-1008:9. Dr. Schubert appears to apply a formalist approach in reading *Beach624*'s disclosure. Although both the "gate photo resistant pattern" and "metal photo resistant pattern" are labeled with the same number (13), it is clear in *Beach624* that they are two different patterns placed at different locations, one to pattern the gate and another to form the ohmic contact, as shown below.



RDX-0013.102; RX-0286 Figs. 1D (annotated), 1E (annotated).

In *Beach624*, two different photoresist patterns are used to separately form the gate and ohmic contact. Further, nothing limits these patterns from being applied simultaneously, although it would be obvious to a POSITA to apply them sequentially as an option. Tr. (Lebby) 891:16-24.

ii. The claim does not require a gate-first process

Dr. Schubert wrongly argues that the claim requires a "gate-first" process where the gate is formed before the ohmic contacts, and a POSITA would not be motivated to combine *Hikita* and *Beach624* to arrive at a "gate-first" process. Tr. (Schubert) 972:12-23; 1004:5-11. A process claim is not limited to a certain order of steps unless "the claim language, as a matter of logic or grammar, requires that the steps be performed in the order written, or the specification directly or implicitly requires an order of steps." *Mformation Technologies, Inc. v. Research in Motion Ltd.*, 764 F.3d 1392, 1398 (Fed. Cir. 2014). Neither the claim nor the specification requires a "gate-first" order. Claim 1 does not recite any order requiring the gate be formed before the ohmic

contacts. Nor does the '508 patent specification require or emphasize any importance of forming the gate first before other components of the device—rather the specification focuses on self-alignment, the alleged point of novelty. *See* JX-0015 3:1-4 ("**The present invention is** an enhancement mode GaN HEMT device with **a gate metal material and a doped GaN or AlGaN material that are self-aligned**, and a method for making such a device."); Tr. (Lebby) 891:20-24. Dr. Schubert's "gate first" argument has no support in the claim or specification.

iii. Even if Hikita suggests using a liftoff technique, it would have been obvious to instead implement *Beach624*'s etching technique

Dr. Schubert also wrongly argues that *Hikita* discloses a lift-off process to form the gate contact and ohmic contacts, and a POSITA would not have been motivated to use an etching process as *Beach624* discloses. Tr. (Schubert) 1002:23-1003:17. This is wrong for two reasons: 1) *Hikita* does not expressly disclose using a liftoff technique and 2) the proposed combination relies on the improvement of *Beach624*'s etching technique.

First, EPC misinterprets the disclosure of *Hikita*. *Hikita* makes no express mention of a lift-off process to form the gate contact and ohmic contacts. RX-0041 ¶¶ [0060], [0061].

Second, even if *Hikita* suggested a lift-off technique to form the gate contact and ohmic contacts, Respondents have proved a motivation to combine *Beach624*'s **etching technique** to form *Hikita*'s gate contact and ohmic contacts. As explained above, a POSITA would have been motivated to use *Beach624*'s etching technique to form *Hikita*'s gate contact and ohmic contacts when favoring performance over simplicity in choosing between these two competing techniques. *Hikita* does not suggest that performing an etching process or lift-off was critical to its method to form a GaN transistor, variations of such was a matter of design choice. Without more, when only two equally viable approaches available, either would seem to be obvious. *See Acco Brands Corp. v. Fellowes, Inc.*, 813 F.3d 1361, 1367 (Fed. Cir. 2016) (finding motivation to combine where

there are only two ways to combine prior art elements and one fell within the claims); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense."). Tr. (Lebby) 907:17-910:24; 912:21-913:3. Moreover, an obviousness showing "does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention." *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) ("It's not necessary to show that a combination is 'the best option, only that it be a suitable option.'") (quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014)); *Novartis Pharms. Corp. v. West-Ward Pharms. Int'l Ltd.*, 923 F.3d 1051, 1059 (Fed. Cir. 2019) (quoting *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004)). The fact that *Beach624*'s etching technique provides certain performance benefits provides sufficient motivation for a POSITA to adopt it to form *Hikita*'s gate contact and ohmic contacts. Tr. (Lebby) 907:17-910:24; 912:21-913:3.

EPC's argument about liftoff is merely an attack on *Hikita* individually and not the proposed combination, rendering this argument inapposite and insufficient to overcome the proposed combination. *In re Keller*, 642 F.2d 413, 426 (C.C.P.A. 1981) ("[O]ne cannot show non-obviousness by attacking references individually where . . . the rejections are based on combinations of references.").

iv. *Beach624* is an enhancement mode device contrary to Dr. Schubert's assertion, but that is irrelevant to the proposed combination

Dr. Schubert wrongly argues that *Beach624* teaches a depletion mode device, and therefore, a POSITA would not have been motivated to combine *Hikita* with *Beach624*. Tr.

(Schubert) 997:10-999:1. This argument does not address Respondents' combination. Respondents do not propose combining the entire device of *Beach624* with *Hikita*, but only the etching process or the self-aligned process to form the gate structure. Indeed, bodily incorporation of one reference into another is not required, rather, "the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d at 425. Here, it suggests that etching gate and ohmic contacts using the steps claimed was obvious.

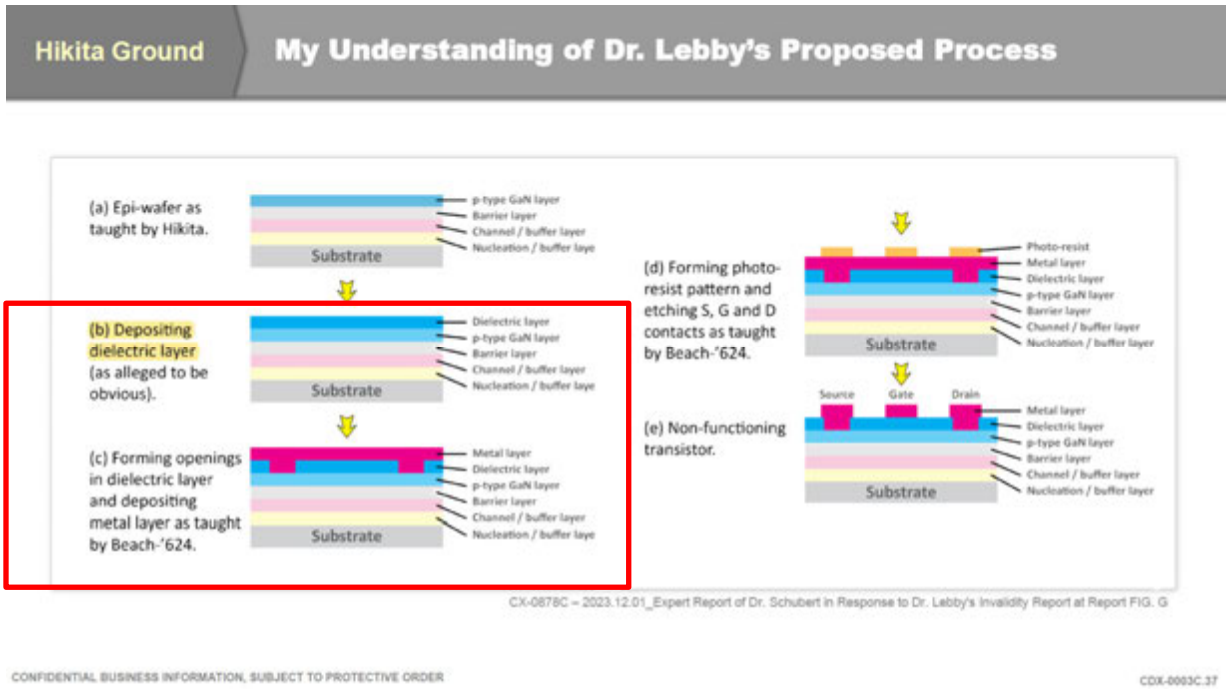
Both enhancement mode and depletion mode devices can be made with the same types of fabrication steps. Whether *Beach624* teaches an enhancement mode or depletion mode device is irrelevant to Respondents' combination of *Hikita* and *Beach624*. A POSITA would not have ignored a prior art reference simply because it was designed to solve a slightly different problem, especially where the technique is equally applicable. *KSR,* 550 U.S. at 418 ("the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.").

Regardless, as even Dr. Schubert acknowledged, *Beach624* teaches both an enhancement mode and a depletion mode device because *Beach624* refers to a "nominally off device" throughout the specification. RX-0286, ¶¶ [0004], [0008], [0012]; Tr. (Schubert) 1025:12-23. Therefore, contrary to Dr. Schubert's argument, *Beach624* does teach an enhancement mode device and a POSITA would have been further motivated to combine *Hikita* with *Beach624*.

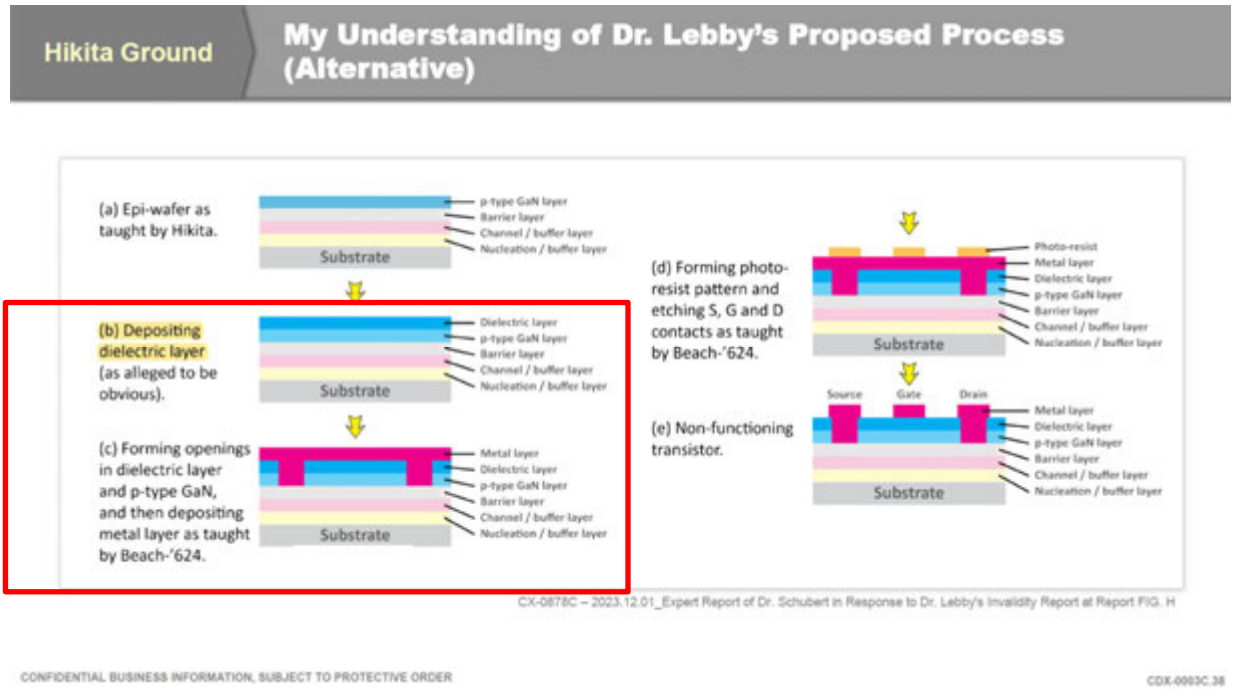
v. When combined as Dr. Lebby proposed, the combination of *Hikita* and *Beach624* is functional—the dielectric is deposited after the gate metal

Dr. Schubert finally wrongly argues that the combination of *Hikita* and *Beach624* is nonfunctional based on his incorrect reading of the proposed combination. Tr. (Schubert) 995:22-997:8. Dr. Schubert's insistence that the combination of *Hikita* and *Beach624* results in a

nonfunctional transistor is premised entirely on his error in interpreting the combination as depositing the dielectric layer ***before*** depositing the gate metal, as he shows in two incorrect figures:



CDX-0003C.37 (annotated)



CDX-0003C.38 (annotated)

Dr. Lebby, however, clearly explained that the combination of *Hikita* with *Beach624* did not change the sequence of *Hikita*'s process shown in Figures 8A-8F, except when the self-aligned gate process is incorporated in *Hikita*. Instead, the combination explains how the gate contact is formed in Figure 8F and how the ohmic contacts are formed in Figure 8E, which *Hikita* does not describe in detail. Tr. (Lebby) 907:17-910:24; 912:21-913:3. Dr. Lebby further explained that, to incorporate the self-aligned process to form *Hikita*'s gate structure, a POSITA would have implemented *Beach624*'s self-alignment process at step Figure 8A of *Hikita*, such that the self-aligned gate structure is formed before the ohmic contacts. Tr. (Lebby) 910:15-24. Indeed, *Hikita* describes etching the doped GaN layer **before** depositing a dielectric layer. Tr. (Lebby) 910:3-14; Tr. (Schubert) 996:13-20; RX-0041, ¶ [0061] ("The source electrode 409, the drain electrode 410 and the gate electrode 411 may be formed before formation of the SiN film 408"); Figs. 8C, 8D. That ordering is preserved in Dr. Lebby's combination, and Dr. Schubert acknowledged that *Hikita* disclosed depositing the dielectric layer **after depositing the gate metal**. Tr. (Schubert) 1029:14-1030:7.

5. EPC Fails to Show Secondary Considerations

As with the '294 Patent, EPC as the patent owner bears the burden of demonstrating secondary considerations may render a claim nonobvious. *Supra* § II.B.6. No secondary considerations support a finding of nonobviousness.

a. Alleged Nexus

For "secondary considerations" to be relevant, there must be a nexus between the claim elements and the alleged secondary considerations. *See Fox Factory*, 944 F.3d at 1373. For nexus to exist, the alleged secondary consideration must be limited to the features of the claimed invention and not due to an unclaimed feature of the device or some other consideration and the patentee bears the burden that a nexus exists. *Id.* EPC has not, cannot, connect its alleged secondary

considerations to specific elements of claim 1 of the ’508 patent. Dr. Schubert claims that the alleged novel feature of the ’508 patent is the self-aligned gate structure. Tr. (Schubert) 1011:21-1012:2. But, as shown above, this type of structure was not new. And, EPC has failed to show any connection between this allegedly new self-aligned gate structure and secondary considerations.

b. Alleged Failure of Others and Long Felt Need

EPC argues that there was a long-felt but unrealized need for the invention disclosed in the ’508 patent (CDX-0003C.53), as well as a failure of others to meet that need. But Dr. Schubert’s *general* descriptions about the ’508 patent’s self-aligned gate structure over silicon MOSFETs fail to satisfy EPC’s burden to show evidence of secondary considerations of nonobviousness. *See generally* Tr. (Schubert) 1013:4-1015:16. As described above, this self-aligned gate structure was well known in the art at the time of the ’508 patent, and therefore, EPC has failed to show that such a problem existed in the art. At best, EPC merely identifies generic benefits of GaN transistors over silicon MOSFETs.

c. Alleged Praise

EPC also describes so called “industrial praise by others” and lists several awards given to EPC. CDX-0003C.53. But again, Dr. Schubert’s generic list of awards fails to show how this alleged industrial praise relates to the claimed invention. Dr. Schubert described one award that was specifically given to EPC “for the commercialization of gallium nitride power devices.” Tr. (Schubert) 1014:19-25; *see also* CDX-0003C.53. But again, this generalized description of “gallium nitride power devices” is not linked to the alleged novelty of the ’508 patent, specifically the self-aligned gate structure. Therefore, EPC has failed to meet its burden of proving any secondary considerations of non-obviousness related to the features of the ’508 patent. At best, EPC again merely identifies generic benefits of GaN transistors over silicon MOSFETs.

IV. CONCLUSION: THE ASSERTED PATENTS ARE INVALID AND THERE IS NO VIOLATION

For all the reasons above, the ’294 and ’508 patents are invalid in view of prior art. EPC cannot establish a violation of Section 337 or that it is entitled to any relief it seeks. Respondents respectfully request the CALJ enter a finding of no violation.

Date: March 15, 2024

Respectfully submitted,

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Attachments

TITLE	ATTACHMENT NAME	SIZE	PAGE COUNT	DATE CREATED
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