UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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PETITIONER (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
PETITIONER AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

_____

Case IPR2023-01384
U.S. Patent No. 10,312,335

_____

PATENT OWNER'S SUR-REPLY

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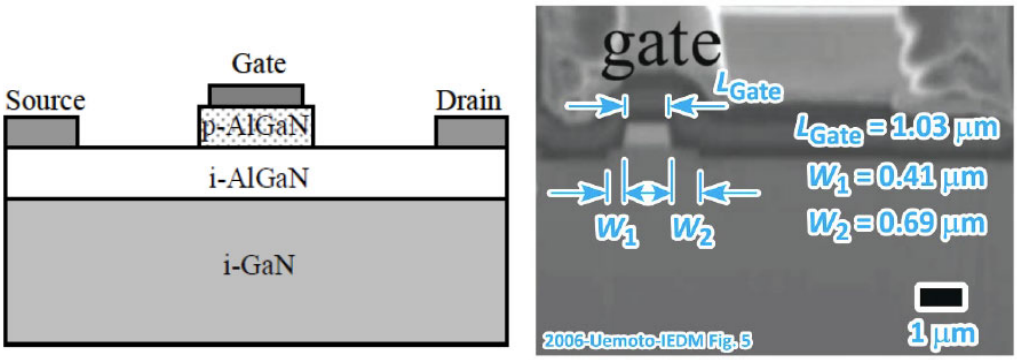
I. Introduction

All of the grounds of the Petition rely ***solely*** on the drawings of Saxler and Yoshida to disclose "substantially equal" ledges. Paper 19 ("Reply"), 14 (§VI heading). But as discussed in the Patent Owner's Response (Paper 17, 31-35 ("POR")), *Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc.*, holds that drawings cannot be relied on to disclose precise or relative proportions. 222 F.3d 951, 956 (Fed. Cir. 2000). Petitioner cites *Ex Parte Bjorn*, No. 2018-001567, 2019 WL 6173305 (P.T.A.B. Oct. 16, 2019), for an alleged exception to the general rule of *Hockerson*. Paper 8, 2. To the contrary, *Ex Parte Bjorn* supports Patent Owner's position by agreeing with the general rule of *Hockerson* and finding it applied to "substantially equal." 2019 WL 6173305, at *17.

Petitioner misdirectly cites to another portion of *Ex Parte Bjorn* that dealt with a different scope of claim limitation allowing for an open-ended range – "***less than or substantially equal***." Paper 8, 2 (emphasis in original) (citing 2019 WL 6173305, at *10). That portion of *Ex Parte Bjorn* is not applicable to the claims at issue here.

Importantly, unlike *Ex Parte Bjorn,* the prior art in this case admits that the drawings cannot be relied on for shapes and dimensions. POR, 35-36. Petitioner even admits this. *Id.*, 36-37. Uemoto illustrates the point. *Id.*, 33.



EX1020, Fig. 1 & Fig.5 (annotated)

Petitioner further tacitly concedes the lack of disclosure by now offering a ***new*** rationale for modifying Saxler and Yoshida under obviousness. Reply, 18-19. Introduction of these new theories is foreclosed by statute, precedent, and Board guidelines. *See* 35 U.S.C. § 312(a)(3) (requiring petitions to identify "with particularity the grounds on which the challenge to each claim is based"). Moreover, Petitioner fails to provide an articulated reason for the modification.

Grounds 3 and 6 are an attempt at hindsight recreation of the claims while ignoring the teachings of the Saxler and Yoshida. POR, 35-37.

Contrary to Petitioner's argument, a POSITA would not centrally align the gate-electrode of Saxler, because it runs counter to Saxler's source-side-alignment teaching. *Id.*, 37-39. For Yoshida, Petitioner's proposed method of forming ledges after the gate structure is already formed would only introduce unnecessary steps and cost to produce structure that has no function and only frustrate Yoshida's purpose, e.g., etching away pGaN *except* where the gate contact is to be loaded. *Id.*

68-72.

Petitioner's application of Beach would cut off or not form the tapered sidewalls of Saxler. *Id.*, 48-49. Again, Petitioner shifts its position by now relying on "Saxler's etching techniques," which is inconsistent with and unsupported by the Petition and thus should not be considered. Consolidated Trial Practice Guide, 84 Fed. Reg. 64,280, 73 (November 2019) ("TPG"). Combining Saxler with Shenoy's theoretical etching model would etch the GaN material, thereby failing to meet the claim limitations. POR, 50-56.

Additional overarching deficiencies for Grounds 1-3 are that, as Petitioner now admits, Saxler does not ***disclose*** the specific structure or enhancement-mode transistor as it relies on throughout the Petition, and it now shifts its position to ***obviousness***. Reply, 5. Similarly for Ground 4, Petitioner now admits Yoshida does not disclose horizontally extending sidewalls, and again shifts its position from being "necessarily" in the Petition (at 67-68) to obviousness in the Reply (at 24-25). For Grounds 5 and 6, Petitioner again newly proposes an "alternative" modification in the Reply (at 25-26). None of these shifts should be considered. TPG, 73.

II. Statement of facts

The Board need not accept the purported material facts as admitted; indeed, it is discretionary. 37 C.F.R. §42.23. Patent Owner does not admit the individual elements were known or obvious in combination, because Petitioner never made that

part of its statement of facts. Moreover, Petitioner's arguments regarding its statement of facts underscores the hindsight nature of its arguments. Petitioner also improperly attempts to bring in other sections of the Petition into the Statement of Facts. Reply, 2-3.

III. Neither Saxler nor Yoshida discloses "substantially equal ledges" (All Grounds)

Petitioner's reliance solely on the drawings of Saxler and Yoshida for "substantially equal ledges" is legal error. POR, 2-3, 29-35, 59-60. Petitioner misinterprets applicable legal precedent to avoid the very case law that it relies on in its Petition. Reply, 18-19. The correct application of the case law to the specification and claims at hand demonstrates the figures of Yoshida and Saxler cannot legally be relied on to disclose "substantially equal ledges." POR, 31-32. Petitioner's only argument in its Petition was that Saxler and Yoshida disclosed "substantially equal ledges" based on the drawings; now, recognizing the weakness of its arguments, Petitioner pivots and argues the figures ***render obvious*** this limitation. *Compare* POR, 2-3, 29-35, 59-60 *with* Reply, 18-19. This new argument was not in the Petition and should not be considered. TPG, 73.

A. *Ex Parte Bjorn* supports patent pwner's position

Petitioner misreads – or at least overstates the holding of – *Ex Parte Bjorn*. Reply, 16. In *Ex Parte Bjorn*, the Board declined to apply the general rule of *Hockerson* for the claim limitation "less than or substantially equal" as it related to

one prior art reference, but, applied the general rule of *Hockerson* as it related to another prior art reference. 2019 WL 6173305, at *10-11. For the first reference, the Board held that the figures showed that "the outer surfaces of the abutment . . . are less than or substantially equal to the ***maximum*** diameter of [the] threads." *Id.*, *12 (emphasis in original). The Board relied on the open-ended range of the claim limitation (i.e., "less than"), thus did not apply the holding of *Hockerson*.

But further in the opinion, when the heart of the issue related to the "substantially equal" limitation, the Board applied the general rule of *Hockerson*. *Id.*, *17. There, the Board found that the prior art could not meet the "less than" limitation. *Id.* Thus, the Board was faced with deciding whether the prior art reference disclosed the remaining part of the claim (i.e., "substantially equal"). Relying on *Hockerson*, the Board held that the prior art drawings could not have disclosed "substantially equal" because, as the Board noted earlier in its opinion, "patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." *Id.*, *10, 17 (quoting *Hockerson*, 222 F.3d at 956). Thus, the Board held that a drawing not disclosed as being to scale or having any particular dimensions cannot be relied on for "such precise or relative proportions" of "substantially equal." *Id*. (citing *Hockerson*, 222 F.3d at 956).

Indeed, in the cases Petitioner relies on for exceptions to *Hockerson*, the

technology of the patent is analyzed to determine to what extent the patent drawings actually represent the actual device. POR, 35; *Ex parte Bjorn*, at *11 (opting not to apply *Hockerson* to claim 1 by reasoning that a screw of the patent in question must have certain dimensions to be screwed into a fixture). Petitioner still fails to perform such analysis. This may be because any such analysis would go against Petitioner in that the exact structural relationship – for example a screw to be threaded into a fixture – is not present in the gate structure of Saxler and Yoshida.

Petitioner alleges that the POR does not address *Seattle Box*[1] or the MPEP.[2] Reply, 15. However, neither is especially relevant nor contrary to the holding in *Hockerson* or *Ex parte Bjorn* that a drawing not disclosed as being to scale or having any particular dimensions cannot be relied on for "such precise or relative proportions" of "substantially equal." *Seattle Box* is not relevant to an interpretation of drawings and merely finds that "substantially equal" is not indefinite. 731 F.2d at 826. Similarly, MPEP §2173.05(b)(III)(D)[3] does not address prior art drawings. Rather, since Petitioner is relying on verbiage in disparate contexts, §2173.05(b)(III)(D) explicitly states that the term "substantially" used "to describe a ***particular*** characteristic of the claimed invention" where "***particular*** sizes" is how

[1] *Seattle Box Co. v. Indus. Crating & Packing, Inc.*, 731 F.2d 818 (Fed. Cir. 1984).

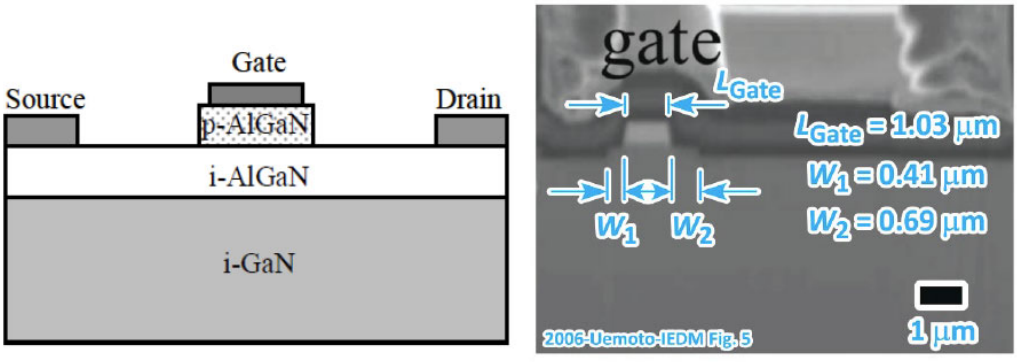
[2] MPEP §2173.05(b)(III)(D)

[3] Petitioner's citation to MPEP §2173.05(b)(II)(D) appears to be incorrect.

Petitioner characterizes the conditions of the *Hockerson* holding. Paper 8, 1. Thus, neither *Seattle Box* nor the MPEP supports Petitioner's position, but rather finds that the term "substantially" is definite and "describe[s] a ***particular*** characteristic" similar to *Hockerson*. MPEP §2173.05(b)(III)(D)*; Seattle Box*, 731 F.2d at 826.

B. Transistor schematics are known to be inaccurate

Petitioner does not refute that the prior art says that the drawings are schematics that do not accurately reflect an actual transistor. POR, 35-37, 60. Saxler explicitly declares that the "shapes [of the drawings] are not intended to illustrate the precise shape of a region of a device." *Id.*, 35-37. Petitioner also explicitly applies the same "principle" that the drawings do not represent an actual transistor to address the drawings of Yoshida. Pet., 90-91. Uemoto demonstrates that drawings are inaccurate and that a POSITA would not understand them to accurately portray a device, or to teach ledges of "substantially equal widths," as shown below. *Id.*, 90-91; POR, 3, 30-31.



EX1020, Fig. 1 & Fig. 5 (annotated)

C. Petitioner's belated obviousness rationale to address "substantially equal ledges" should be disregarded (Grounds 1-6)

Petitioner initially devotes a single sentence for each ground in the Petition relying solely on the drawings of Saxler and Yoshida to ***disclose*** "a pair of horizontal ledges having substantially equal widths." POR, 29. In the Reply, Petitioner concedes that "substantially equal ledges" are not disclosed by stating that the feature would have been "obvious." Reply, 18-19. Petitioner attempts to replace its disclosure argument with an obviousness rationale to modify Saxler and Yoshida – an argument absent in its Petition. *Id.*, 18-19.

A petitioner cannot argue in a reply that it would have been obvious to modify the prior art where the petition argued only that the prior art disclosed a particular claim limitation. *Yita LLC v. MacNeil IP LLC*, 69 F.4th 1356, 1365-67 (Fed. Cir. 2023); *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369-70 (Fed. Cir. 2016). An argument that a POSA would have modified the prior art is a "meaningfully distinct contention" from arguments limited to what the prior art reference teaches. *Yita*, at 1367.

Furthermore, because the arguments are new and not supported by Dr. Shealy's declaration, Petitioner falls back on conclusory attorney argument, in alleging that "a POSITA would have seen Figure 1A shows a centered gate with ledges of substantially equal width and found such a gate obvious." Reply, 18 (citing patent drawings in Pet., 51, 83). Petitioner provides even less reasoning in alleging

that Yoshida renders obvious the feature, again relying solely on the drawings. Reply, 19. Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference. *In re Stepan Co.*, 868 F.3d 1342, 1345-46 (Fed. Cir. 2017).

IV. Neither Saxler nor Yoshida discloses "self-aligned ledges" (All Grounds)

Petitioner maintains its argument that "self-aligned ledges" are a product-by-process limitation (Reply, 19-21), which Patent Owner disagrees with (POR, 38-44).

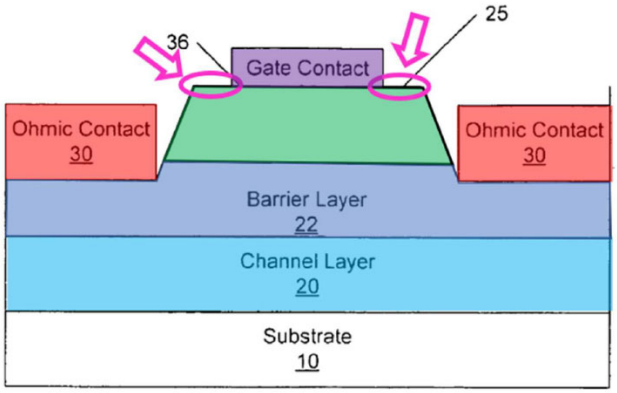
Even if the Board construes the term as product-by-process, the structure implied by the process steps needs to be considered when assessing the patentability of product-by-process claims over the prior art. *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1369 (Fed. Cir. 2009) ("In determining validity of a product-by-process claim, the focus is on the product and not the process of making it.").

Petitioner fails to show the "product" of the prior art is the same as the claimed "self-aligned ledges", as discussed in §III. Indeed, Petitioner is of the mindset that a product-by-process limitation "lend[s] no patentable weight." EX1003 ¶135.

V. Petitioner abandons its position that Saxler discloses a non-recessed, recessed embodiment and that Saxler discloses an enhancement mode transistor (Ground 1)

Grounds 1 is based on a hypothetical non-recessed recessed embodiment. Pet., 25-26. The Petition declared that the non-recessed recessed embodiment was disclosed by Saxler in arguing that "Saxler's gate contact may be recessed or non-

recessed (i.e., flat) . . . Where the gate recess is not utilized, Saxler would result in the following structure." *Id*. (internal citation omitted). Petitioner specifically relies on the figure below that is not found in Saxler, but refers to it to as "Saxler's non-recessed embodiment." Pet., 28.



Saxler, Fig. 1A (modified).

Pet., 26

In his deposition, Dr. Shealy clarifies that "Saxler's non-recessed embodiment" was based on ¶[0052] of Saxler and his opinion is that he "mix and match" and "take all the embodiments and bring in which ones you want, depending on what you're trying to accomplish." EX2004, 39:3-5, 40:1-8, 41:24-42:1. In the Reply, Petitioner concedes that "Dr. Shealy's testimony accurately reflects obviousness law" in his interpretation of ¶[0052] of Saxler. Reply, 5.

By citing "obviousness law", Petitioner contradicts its earlier position that Saxler ***discloses*** Saxler's non-recessed embodiment, instead now relying on *modifying* the disclosure. *Id*. Thus, this is not a scenario where a POSITA is

selecting a disclosed embodiment, but instead one where a POSITA would be creating a new embodiment based upon the disclosure. And because Petitioner now admits Saxler must be modified, a motivation to modify with an expectation of success is required. *Id*.; *In re O'Farrell*, 853 F.2d 894, 904 (Fed. Cir. 1988). But Petitioner fails to provide that analysis.

Petitioner also concedes that Saxler does not disclose "a normally off enhancement-mode GaN transistor" by requiring modification to make an enhancement-mode device. Reply, 5.[4]

VI. The Petition failed to provide motivation to arrive at "Saxler's non-recessed embodiment," and now belated introduces numerous new theories of obviousness (Ground 1)

The Petition fails to provide any support for Petitioner's new position that a POSITA would ***modify*** Saxler's recessed embodiment by removing its recess. Having to pivot to "obviousness law," Petitioner attempts to cure this deficiency by 1) introducing a new theory of obviousness under *KSR*[5], and 2) citing passages of the Petition (and Dr. Shealy's testimony) that were ***not*** relied on in Ground 1.

A petitioner cannot argue in a reply that it would have been obvious to modify

[4] *See also* POR, 22-25; EX1003 ¶103 ("[W]ith the recess, Saxler's device is not enhancement-mode (always off)" with reference to the recessed embodiments); Reply, 8 n.2 (relying on a modification of separating the ohmic contacts from the cap layer to turn the non-recessed embodiments (Fig. 1B) into enhancement-mode).

[5] *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007).

the prior art where the petition argued only that the prior art disclosed a particular claim limitation. *Yita*, 69 F.4th at 1365-67; TPG, 73. Arguing that a POSITA would modify the prior art is a "meaningfully distinct contention" from arguments limited to what the prior art reference teaches. *Yita*, at 1367.

The Petition states that "a POSITA would have understood Saxler's transistors to be enhancement-mode GaN transistors at least because of their gate structure." Pet., 35-36. Thus, Ground 1 relies only on Saxler ***disclosing*** enhancement-mode transistors and does not articulate any reasoning for the modification now proposed under §103.

Petitioner alleges that Dr. Shealy's deposition statement adheres to *KSR* — that ¶[0052] allows you to "mix and match" and "bring in which [embodiments] you want, depending on what you're trying to accomplish,". Reply, 4-5. First, *KSR* does not allow a POSITA to simply "mix and match" embodiments to "accomplish" an invalidity analysis and Petitioner fails to provide adequate motivation, because it lacks any articulated reasoning for removing a recess from a recessed gate. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1074 (Fed. Cir. 2015). Second, the "mix and match" argument is not disclosed by the Petition, and is a belated obviousness rationale. TPG, 73.

Petitioner further argues that ¶[0052] "expressly acknowledges Saxler's recess is optional in every figure" and "***Saxler itself*** tells a POSITA to remove Figure

1A's recess." Reply, 4 (emphasis in original). Paragraph ¶[0052] of Saxler states the possibility of "other embodiments . . . may include or not include a gate recess" without illustrating or further describing those "other embodiments." Dr. Schubert points out that Petitioner's proposed modification based on the generic statement of ¶[0052] would allow practically any modification without requiring any motivation to combine or expectation of success. EX2005 ¶¶99-102. Petitioner's interpretation would thus eviscerate any requirement to identify a motivation to combine for a POSITA and allow all hindsight depending on what "[he's] trying to accomplish." EX2005 ¶99-100. Petitioner's rationale is clearly hindsight. POR, 21-22.

The hindsight continues in "mix[ing] and match[ing]" parameters to arrive at an enhancement-mode device. Reply, 4-5. Saxler only discloses depletion-mode transistors, and any such modification would require optimizing numerous parameters (including the shape of the cap layer) to change its principle of operation without any direction or expectation of success. POR, 46; *In re O'Farrell*, 853 F.2d at 904.

Petitioner points to the Petition and the Shealy declaration for an alleged motivation. Reply, 4; Pet., 33; EX1003 ¶[103]. However, the cited page of the Petition does not address Ground 1, only the section of "Ground 2: Motivation to Combine." Pet., 29. Indeed, this section discusses modifying Saxler based on the enhancement-mode transistor of Yoshida, addressing only Ground 2 (Saxler in view

of Yoshida), and the cited ¶[103] was similarly only cited in Ground 2.

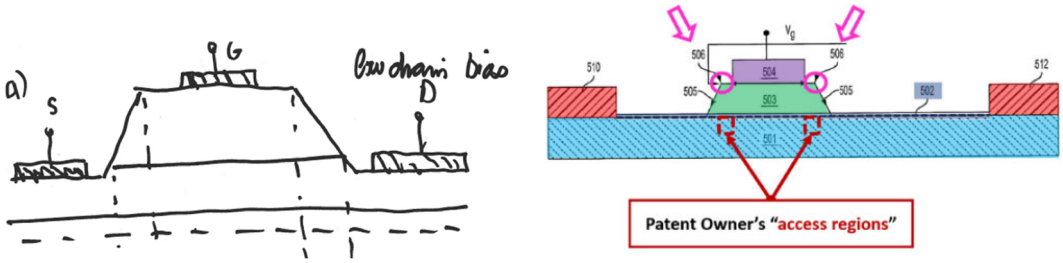
Petitioner further argues motivation for the first time in that removing the recess of Saxler's Figure 1A removes steps to form a recess in its gate. Reply, 4, 6. However, that motivation is not found in the Petition nor supported by expert testimony and should not be considered. TPG, 73. Additionally, Dr. Schubert specifically explained that Petitioner's reliance on Smith in the Petition is merely "circular logic" that starts with a recessed embodiment of Saxler and attempts to find disclosure in Smith to arrive at a non-recessed embodiment, while completely ignoring the non-recessed embodiments taught by Saxler (or Smith). EX2005 ¶¶107-112.

Indeed, Petitioner fails to provide any motivation and expectation of success. And with good reason: it makes no sense to have a non-recessed, recessed embodiment. EX2005 ¶¶104-112. The Petition is riddled with hindsight bias in selecting a recessed gate structure and then removing the recess even though the reference itself describes a distinct non-recessed gate structure. *Id.*

VII. The proposed modification to Saxler does not result in a functional enhancement-mode transistor (Grounds 1-3)

As discussed in §V, Petitioner admits that none of the embodiments of Saxler (neither FIG. 1A nor FIG. 1B) are enhancement-mode without modification. POR, 22-23; Reply, 8 n.2. Patent Owner addresses the proposed modification regarding the length between the ohmic contacts. POR, 23-29, 45-46. Petitioner newly argues

that "the patent has the same 'access regions' as modified Figure 1A (shown below), and it purports to operate in enhancement mode." Reply, 8-9.



Reply, 9-10

Petitioner cannot reasonably make the statement that the depletion-mode gate structure of Saxler is the "same" as that in the '335 patent. Initially, Petitioner misunderstands "access regions," which refers to the lengths of the ***2DEG between the gate and the source and drain***, respectively, and not ***just the region underneath the cap layer***. POR, 23. Petitioner's proposed transistor has cap layer 24 extending (substantially) the entire width of the access regions, while typical enhancement-mode transistors (including in the '335 patent) do not. Reply, 8-10 (reproduced above); POR, 23-29.

Dr. Schubert explains that depletion-mode transistors and enhancement-mode transistors operate differently. POR, 27-28 (citing EX2005). A depletion-mode transistor is normally-on and only needs to "pinch off" the 2DEG at one point to turn the transistor off, such that the width of the gate material underneath the gate electrode, as compared to the width of the gate electrode, does not matter. *Id.* Thus,

the gate material can extend (substantially) the entire length between the ohmic contacts and still function in depletion-mode. *Id*. Alternatively, enhancement-mode transistors deplete the 2DEG underneath the gate material to be normally off. *Id*. When a positive voltage is applied to the gate electrode, the 2DEG underneath the gate electrode is replenished. *Id*. If the gate material is too much wider than the gate electrode, the entire 2DEG cannot be replenished and the device would not turn on. *Id*.

Petitioner's proposed transistor based on FIG. 1A of Saxler would require excessive voltage to be applied to turn the transistor ON based on the relative size of the cap layer. POR, 27-29 (citing EX2005). ***Petitioner's*** ITC expert, Dr. Lebby, agreed and opined that a similar gate arrangement would "not be an ideal device" if implemented as an enhancement-mode device, due to the excessive voltage demand resulting in "lots of leakage." POR, 28-29; EX2005 ¶123. Thus, there is no motivation to make the modification resulting in a leakier transistor.

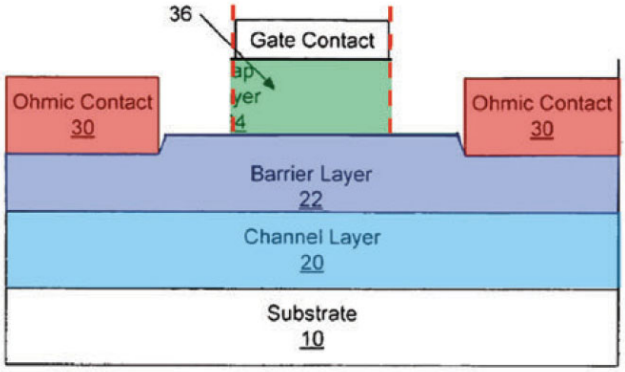
Accordingly, a POSITA would not be motivated to produce an enhancement-mode device as suggested by Petitioner at least because of the required excessive voltage requirements to operate in enhancement-mode. POR, 27-29; *In re Ratti*, 270 F.2d 810, 813 (C.C.P.A. 1959). That is, a POSITA would not be motivated to remove the gate recess of the depletion-mode transistor in FIG. 1A of Saxler in view of itself or Yoshida to arrive at an enhancement-mode device, because the resulting

transistor "would not be an ideal device" and have "lots of leakage." POR, 28-29; EX2005 ¶123.

VIII. Petitioner proposes a new combination of Saxler and Beach unsupported by the Petition (Grounds 4 and 6)

The Petition states "[a] POSITA would have found it obvious ***to make the stacked gate structure consisting of a cap layer and gate contact of the Saxler-Yoshida GaN HEMT device using the methods of Beach and Shenoy***." Pet., 59 (emphasis added). And, "[a] POSITA would have ***found it obvious to use Beach's approach to create Saxler-Yoshida's gate structure, which would have improved alignment between layers***. It would have been obvious to look to ***Beach for its simple methods of making stacked gate structures***." Pet., 62 (emphasis added, internal citations omitted).

Dr. Schubert shows that all the "self-aligned" approaches cited by Petitioner (Smith, Beach, Beach-II) are for self-aligning ***sidewalls***, and would result in cutting off, or not forming, the horizontally extending "sloped" side surfaces that Petitioner relies on from Fig. 1A of Saxler. POR, 48-49; EX2005 ¶¶148-153.



POR, 49

Petitioner now proposes a new "combination us[ing] Saxler's etching technique to create sloped sidewalls when using Beach's one-mask approach." Reply, 23. This is inconsistent with and is unsupported by the Petition. The combination of the Petition is "to make the stacked gate structure of Saxler's non-recessed embodiments using Beach's and Shenoy's methods" and fails to reference "Saxler's etching technique" and how it would be modified based on Beach/Shenoy. Thus, this new combination from the Reply should not be considered for unpatentability. *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1329-1331 (Fed. Cir. 2019) (rejecting a new theory of unpatentability where petitioner argued a new combination of features from the same references for the first time in its reply); TPG, 73.

Moreover, even if the combination were to be considered, the Reply fails to provide a step-by-step analysis of how the three disparate etching steps would be combined, why a POSITA would have combined them, and whether a POSITA

would have had a reasonable expectation of success. Instead, Petitioner again retreats to vague reasoning such as "no more than simple substitution" and "known methods that would be predictably implemented" without providing specific process sequences for the proposed combination. POR, 57. This is insufficient as a matter of law. *KSR,* 550 U.S. at 418 ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

IX. Petitioner relies on irrelevant and conclusory statements regarding Shenoy (Grounds 3 and 6)

As discussed above, Petitioner reverse engineers schematics of Saxler and Yoshida. Based on that strawman, Petitioner newly argues that Dr. Shealy's mention of "liquid metal etches" (EX2004, 99:14-17) – that Petitioner refers to as "many wet etches"– "would 'work fine.'" Reply, 24. But reliance on these "wet etches" would be inappropriate because they are not cited in any Ground nor sufficiently tied to Shenoy. POR, 53. As such, this new argument should not be considered. TPG, 73.

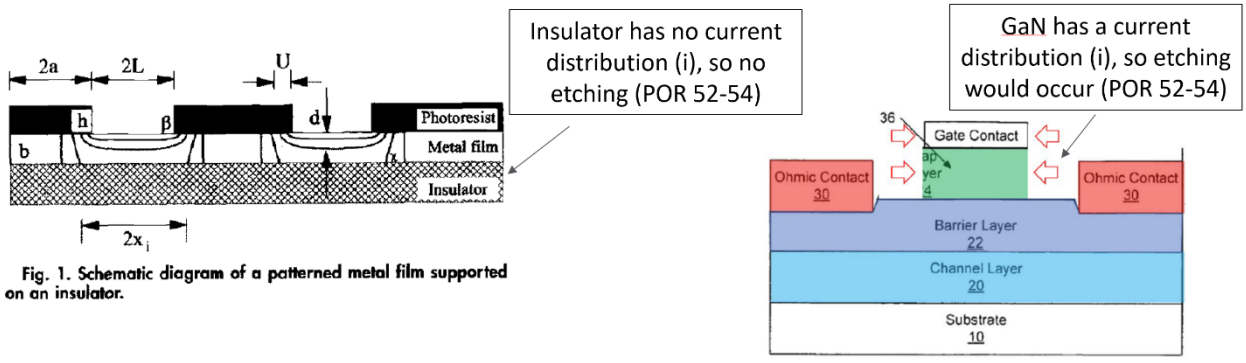
But Dr. Shealy distinguishes these other etching techniques from Shenoy. EX2004, 97:19-21 ("[T]hese solutions [are] ***unlike the technique used in Shenoy***. . . ." (emphasis added)). As such, the new argument fails.

Moreover, the new argument suffers from similar deficiencies as the Petition. It relies on hindsight in Dr. Shealy's statement that the wet etches "work fine"

(Reply, 24), which is purely conclusory and cannot satisfy the reasonable expectation of success requirement.

Indeed, Dr. Shealy's opinion that the approach would "etch the gate metal, not the p-type GaN layer" provides no supporting evidence. Reply, 24. Petitioner is specifically referring to a depleted "holes" theory of Dr. Shealy that directly contradicts the proposed modification. POR, 50-54; EX2004, 98:25-99:13.

In contrast, Dr. Schubert actually addresses the principles of the mathematical model of Shenoy, and its reliance on an underlying insulator that is not present in the proposed modification. POR, 50-54. Dr. Schubert explains that the equation of Shenoy's mathematical model based on "Faraday's law" and "Laplace's equation" applies to both metals and semiconductors, in etching both the gate contact and the underlying GaN, because neither is an insulator. *Id*.



Petitioner newly argues that p-GaN material etches more slowly than the gate metal according to Shenoy (Reply, 24), which should not be considered. TPG, 73. This characterization of Dr. Shealy's testimony is wrong, because the modification

based on Shenoy was to ***preserve*** the ledges (Dr. Shealy: "they don't touch the gallium nitride" with reference to the many wet etches), which Patent Owner establishes is not how Shenoy would work. Pet., 60-63; EX2004, 99:14-19; POR, 50-56. Petitioner fails to provide how the relative etching rate is relevant to its application of Shenoy.

Petitioner newly argues that "Saxler repeatedly describes passivation techniques." Reply, 24. First, Petitioner fails to make this argument in its Petition, and it should not be considered. TPG, 73. Second, Petitioner fails to provide any explanation for how or why a POSITA would incorporate the alleged "passivation techniques" into the relevant layer, when in the process it would have occurred, and whether there would have been a reasonable expectation of success, given the alleged "passivation techniques" of Shenoy would affect the plurality of disparate etching steps of Saxler, Yoshida, and Beach.

X. Petitioner concedes that Yoshida does not disclose horizontally extending sidewalls, and the Petition does not support an obviousness rationale (Ground 4)

As admitted by Petitioner, Yoshida discloses vertical sidewalls and not horizontally extending sidewalls. Pet., 70 (alleging "a simple substitution of Yoshida's vertical sidewalls with Saxler's sloped sidewalls"). Furthermore, Petitioner never refutes that the feature is not inherent due to the possibility of vertical or undercut sidewalls. POR, 61-62; Reply, 18 ("this does not mean that

vertical sidewall would ***not*** have been obvious" in view of Saxler), 24-25.

Rather, Petitioner newly relies on obviousness. Reply, 24-25. This position is inconsistent with the Petition and still does not proffer a legally sufficient obviousness rationale.

The Petition succinctly presents its inherency-based argument:

> [U]nder Patent Owner's construction of the slope terms ('p-type gate material having side surfaces extending horizontally such that the bottom of the material is wider than the top of the material'), a[A] POSITA would know ***any constructed embodiment would <u>necessarily</u> extend at least slightly on the bottom due to manufacturing tolerances***.

Pet., 67-68 (emphasis added).

A petitioner cannot switch theories in a reply. *Yita*, 69 F.4th at 1365-67; TPG, 73. The Petition solely argued that the prior art ***disclosed*** a particular claim limitation; now, for the first time, Petitioner argues that it would have been ***obvious to modify*** the prior art.

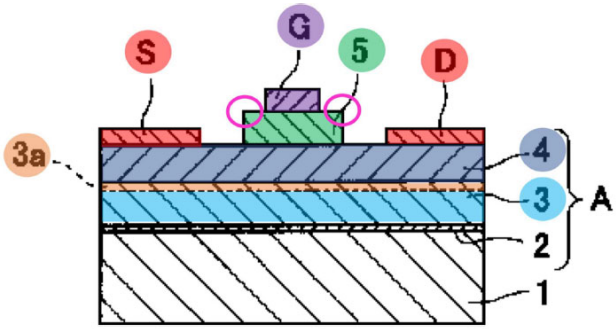
Indeed, in relying on the element being "necessarily" met or "when implemented", the Petition fails to provide any motivation to modifying the vertical sidewalls of Yoshida in Ground 4. But, Petitioner agrees that vertical or undercut walls are a possibility, and therefore no inherency. Pet., 70; POR, 61-62; Reply, 18; EX2004, 46:3-5, 47:6-10; EX2005 ¶¶287-294. Petitioner fails to provide any motivation for modifying Yoshida's vertical sidewalls. Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or

motivation to modify the teachings of that reference. *In re Stepan Co.*, 868 F.3d at 1345-46.

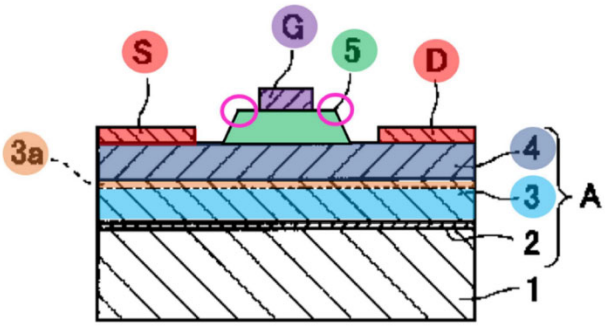
XI. Petitioner introduces new obviousness rationales to modify Yoshida with Saxler's sloped sidewalls (Grounds 5 and 6)

Petitioner newly relies on an "alternative" obviousness rationale in "using Saxler's etch within the p-GaN's existing footprint creates sloped sides and maintains the same (or less) width at the bottom of the p-GaN." Reply, 25-26 (internal citations omitted).

The Petition fails to argue that a POSITA could maintain the p-GaN's existing footprint, rather, clearly relies on ***adding*** the sloped walls of Saxler to ***widen*** the p-type GaN material 5 of Yoshida. Pet., 68-69, 78-82.

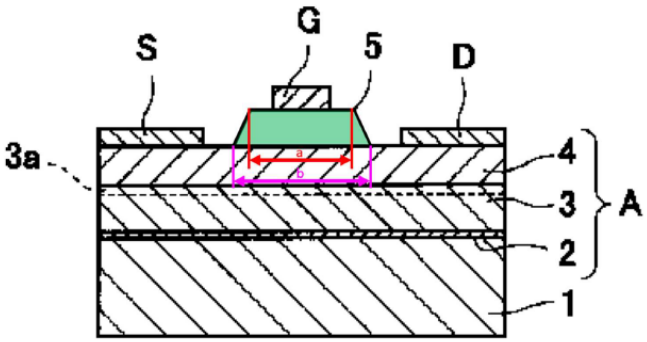


Yoshida, Fig. 1.



Yoshida, Fig. 1 (modified).

This is especially evident in Petitioner's reliance on dimensions of the widened p-type GaN material 5 in the modified transistor. Pet., 80-81. Petitioner specifically touts that the modification would increase the footprint of the p-type GaN material 5 by "more than 10%." *Id.*

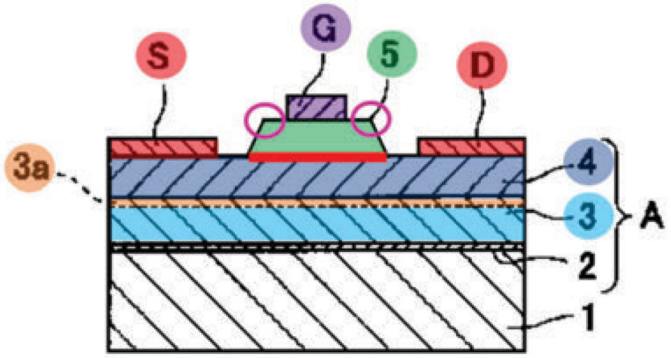


Yoshida, Fig. 1 (modified).

For this reason alone, Petitioner's "alternative" theory should be rejected.

Regardless, the argument suffers from the same fatal deficiencies as the obviousness rationale of the Petition. Patent Owner establishes that the transistor of Yoshida is assembled with the p-type GaN layer 5 "etch[ed] away . . . except for where the gate electrode was to be loaded" in order to position the pn junction of a p-type GaN layer 5 "immediately under" the gate electrode G for "voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels." POR, 63-66.

Thus, it is immaterial whether Petitioner proposes adding the sloped walls to the p-GaN 5 of Yoshida (as in the Petition) or reducing the size of the gate electrode G while maintaining the same footprint of the p-GaN 5 (as in the Reply), because both modifications would widen the p-GaN 5 ***relative to*** the gate electrode G such that the pn junction would not be "immediately under" the gate electrode G, reducing the desired "voltage control" of Yoshida. *Id.*



As discussed in §VII, the structure and function of the depletion-mode cap layer of Saxler is substantially divergent from the enhancement-mode p-type GaN layer 5 of Yoshida.

XII. Petitioner still fails to provide any motivation for forming the "ledges" in Yoshida-Saxler after the gate is formed (Ground 6)

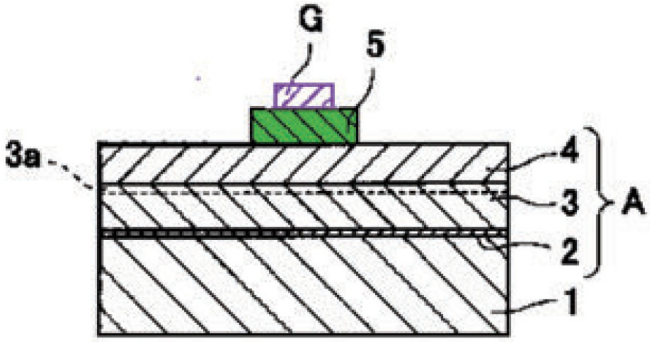
Petitioner continues to rely on reverse engineering FIG. 1 of Yoshida. Reply 26-27. In place of motivation, Petitioner relies on a statement that "the combination would form the claimed ledges." Reply, 27.

However, initially, Petitioner agrees that the schematic of FIG. 1 does not represent a transistor as manufactured, in applying the "principle" of ¶[0042] in Saxler. POR, 35-37; Pet., 76.

Furthermore, Petitioner does not refute that the ledges of FIG. 1 are a byproduct of Yoshida's approach of etching the p-type GaN layer 5 before loading the gate contact G, that Petitioner proposes modifying away from. POR, 68-69; Reply, 26-27. Petitioner does not refute that the p-type GaN layer 5 would be etched

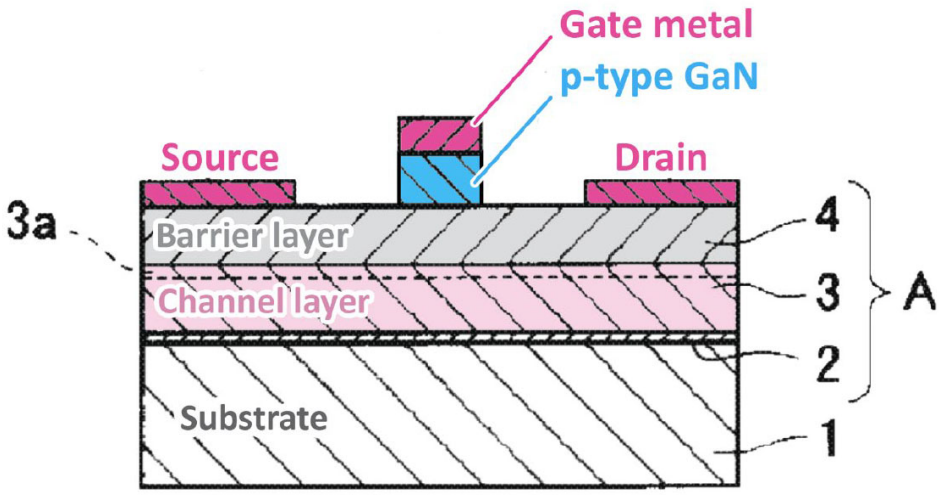
slightly wider in this "gate-last" approach (before the gate electrode is loaded) in order to receive the gate electrode without overhang. POR, 68-69. This is supported by the references that Petitioner relies on showing ledges. *Id*.

Yoshida specifically discloses that its transistor is formed by a process where the p-type GaN layer 5 is layered and "etch[ed] away . . . except where the gate electrode was to be loaded" such that the pn junction of the p-type GaN layer 5 is "immediately under" the gate electrode G when loaded for "voltage control with a small amount of carrier injection." POR, 11-14, 68-69.



EX1007, Fig. 1 (annotated)

But Petitioner still does not provide a valid reason to add an unnecessary second etching step to form ledges in Yoshida after the gate metal is already loaded on the p-type GaN and initially etched to form the gate. POR, 70-72.



Yoshida after first etching step of Beach

The ledges 1) would have no function because the gate metal would already be loaded and etched simultaneously to form the gate, 2) would only frustrate Yoshida's purposes by being detrimental to voltage control by reducing the width of the gate metal relative to the pn junction, and 3) would undesirably add manufacturing cost and steps as explicitly discouraged by Petitioner. POR, 71-72 (citing motivations from the Petition including "eliminating masking and etching steps," "reduc[ing] steps and costs" and predictably creating the "stacked gate structure more efficiently").

Thus, a POSITA would not perform an additional etching step to form the "ledges" in Yoshida or Yoshida-Saxler after the gate metal is loaded on the p-type GaN and etched to form the gate. *Id.*

XIII. Conclusion

For the foregoing reasons, Petitioner's challenge is deficient, and no claim should be held unpatentable.

Dated: October 22, 2024 Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing **PATENT OWNER'S SUR-REPLY** complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 5,475 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

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CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S SUR-REPLY** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

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