Patent Owner's Demonstrative

Innoscience (Zhuhai) Technology Company, Ltd., and Petitioner America, Inc. ("Petitioner")

v.

Efficient Power Conversion Corporation ("Patent Owner")

Case Nos. IPR2023-01382 & IPR2023-01384
U.S. Patent Nos. 9,748,347 & 10,312,335

Hearing scheduled January 7, 2024 at 9:00 AM

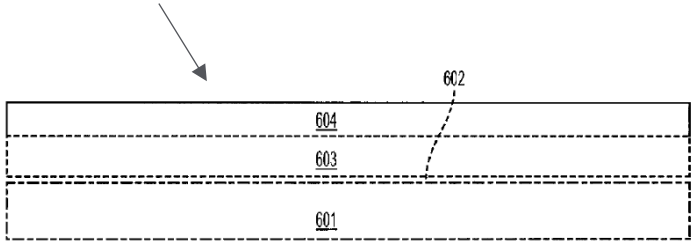
Overview of Patents

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

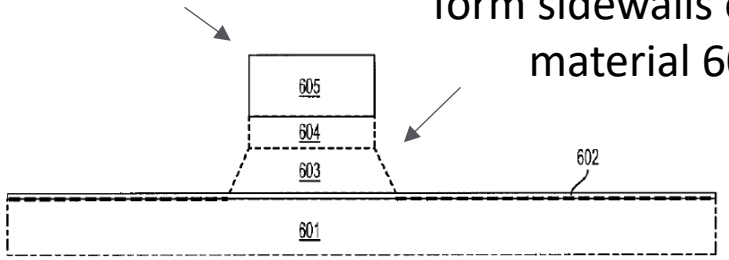
Overview of the ’347 Patent

The ’347 patent describes and claims a method for forming an enhancement-mode GaN (Gallium Nitride) MISFET (Metal Insulator Semiconductor Field Effect Transistor) with self-aligned ledges and laterally extending sidewalls.

Gate metal 604 and GaN material 603 layered

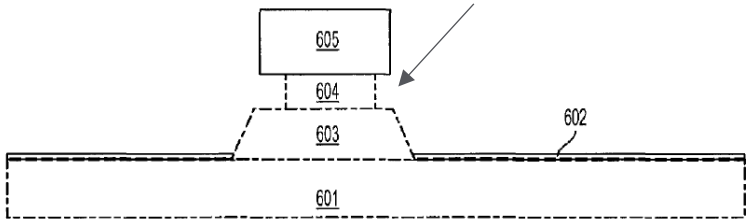


Photoresist 605 deposited



Gate metal 604 and GaN material 603 etched to form sidewalls on GaN material 603

Gate metal 604 etched to form self-aligned ledges on GaN material 603



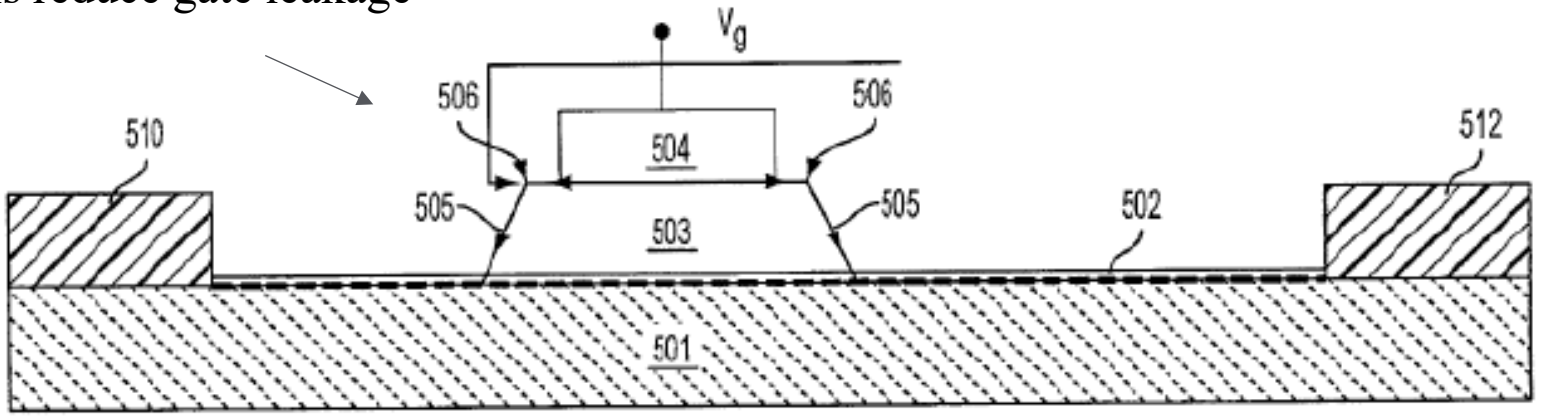
’347: Paper 17 at 4-10

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Overview of the ’335 Patent

Similarly, the ’335 patent describes and claims an enhancement-mode GaN MISFET having substantially equal or self-aligned ledges and laterally extending sidewalls.

elongated surface length defined by ledges and sidewalls reduce gate leakage



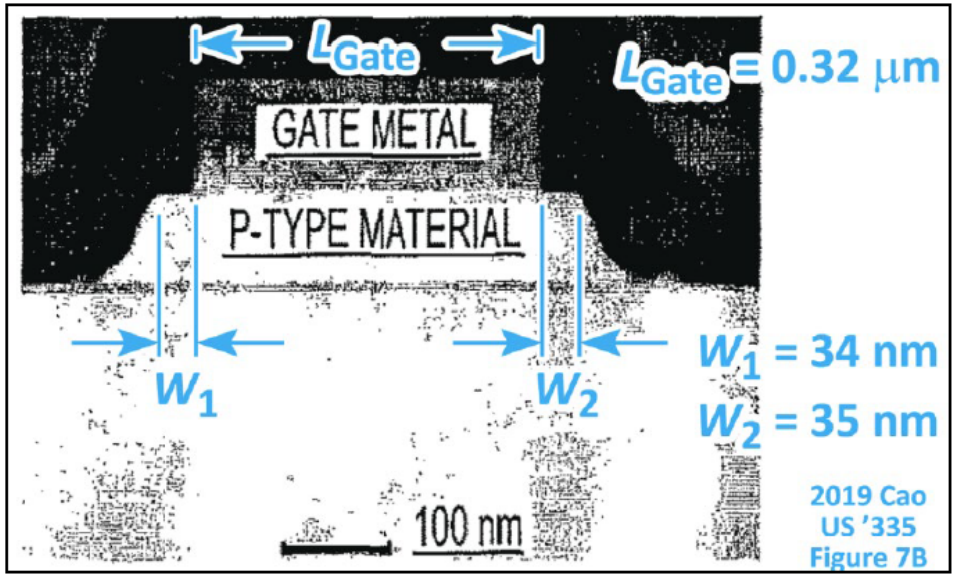
’335: Paper 7 at 4-5; Paper 17 at 4-7

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Overview of the ’335 Patent

Similarly, the ’335 patent describes and claims an enhancement-mode GaN MISFET having substantially equal or self-aligned ledges and laterally extending sidewalls.

elongated surface length defined by ledges and sidewalls reduces gate leakage



’335: Paper 7 at 4-5; Paper 17 at 4-7

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claims

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Independent Claim 1 of the ’347 Patent

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

[1d] depositing a p-type gate material on the barrier layer;

[1e] depositing a gate metal on the p-type gate material;

[1f] forming a photoresist over the gate metal;

[1g] etching the gate metal and the p-type gate material,

[1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

[1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

First Etching Step

Second Etching Step

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Independent Claim 1 of the ’335 Patent

[1p] An enhancement-mode GaN transistor, comprising:

[1a] a GaN layer;

[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[1c] a source contact and a drain contact formed on the barrier layer;

Side Surfaces

[1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and

[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

Horizontal Ledges

[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

Independent Claim 5 of the ’335 Patent

[5p] An enhancement-mode GaN transistor, comprising:

[5a] a GaN layer;

[5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[5c] a source contact and a drain contact disposed on the barrier layer;

[5d] a p-type gate material formed above the barrier layer and between the source and drain contacts; and

[5e] a gate metal disposed on the p-type gate material,

[5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

[5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

Self-Aligned Ledges

Side Surfaces

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claim Construction

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claim Construction for the ’347 and ’335 Patent

Claim Term	Petitioner’s Proposal	Patent Owner’s Proposal
forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer	forming side surfaces of the p-type gate material such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces that contact the barrier layer	“forming side surfaces of the p-type gate semiconductor material such that the bottom of the material, which contacts the barrier layer, is wider than the top of the material

’347: Paper 1 at 19-22
’335: Paper 1 at 19-23

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claim Construction for the ’347 Patent

Claim Term	Petitioner’s Proposal	Patent Owner’s Proposal
etching the gate metal and the p-type gate material	using the photoresist to etch the gate metal and the p-type gate material	etching the gate metal and etching the p-type gate material

’347: Paper 1 at 22-23

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Claim Construction for the ’347 Patent

Claim Term	Petitioner’s Proposal	Patent Owner’s Proposal
etching the gate metal to form a pair of ledges	after the etching of the gate metal and the p-type gate material, etching the gate metal to form a pair of ledges	performing a process during which gate metal is removed and two ledges are created

’347: Paper 1 at 23

Claim Construction for the ’335 Patent

Claim Term	Petitioner’s Proposal	Patent Owner’s Proposal
“self-aligned” ledges	“no patentable weight”	Ledges of “substantially equal widths” produced by self-aligned process

‘335: Paper 1 at 23-24; Paper 17 at 29-30

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Summary of Grounds

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds for the ’347 Patent

	Ground	Prior Art	Basis	Claims
Saxler-Based	1	Saxler, Beach, Shenoy	§ 103	1-3
	2	Saxler, Yoshida, Beach, Shenoy	§ 103	1-3
	3	Saxler and Ahn	§ 103	1-3
Yoshida-Based	4	Yoshida, Saxler, Beach, Shenoy	§ 103	1-3
	5	Yoshida and Ahn	§ 103	1-3

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds for the ’335 Patent

	Ground	Prior Art	Basis	Claims
Saxler-Based	1	Saxler in view of knowledge of a POSITA	§ 103	1-7
	2	Saxler, Yoshida	§ 103	1-7
	3	Saxler, Yoshida, Beach, Shenoy	§ 103	2, 5-7
Yoshida-Based	4	Yoshida in view of knowledge of a POSITA	§ 103	1-7
	5	Yoshida, Saxler	§ 103	1-7
	6	Yoshida, Saxler, Beach, Shenoy	§ 103	2, 5-7

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Cited Prior Art

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-4 for ’347 & Grounds 1-3, 5, & 6 for ’335
Saxler | Prior Art Overview

Petitioner admits D-Mode (not E-Mode)

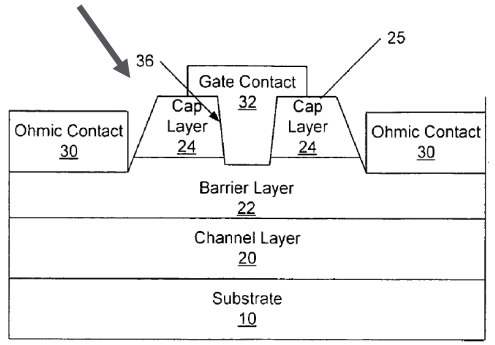


FIG. 1A – Recessed Embodiment

Petitioner admits D-Mode (not E-Mode)

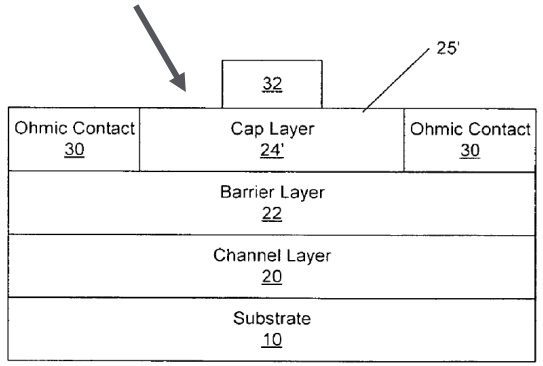
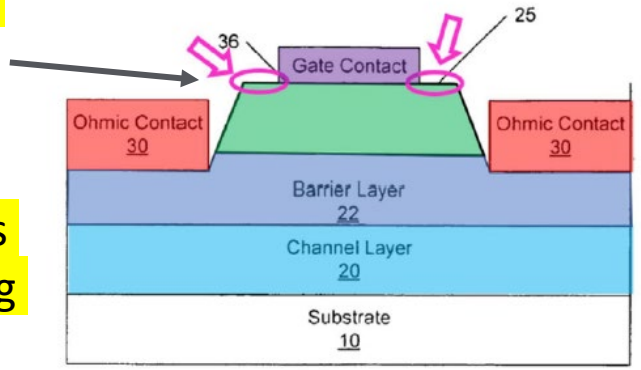


FIG. 1B – Non-Recessed Embodiment

Petitioner admits gate structure as relied on is not disclosed by Saxler

Petitioner “mix and match” and “take all the embodiments and bring in which ones you want, depending on what you’re trying to accomplish”



Saxler, Fig. 1A (modified).

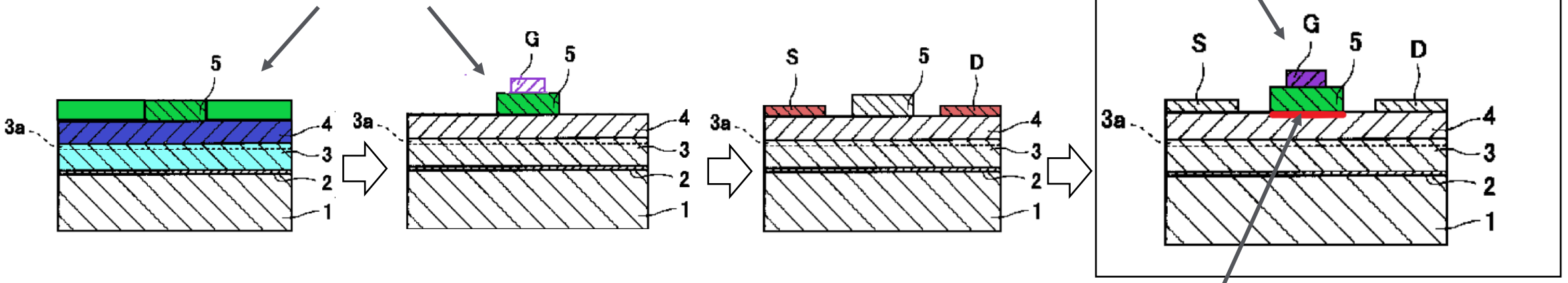
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 11-12; Paper 21 at 3-5, 9
’335: Paper 17 at 9-10; Paper 21 at 9-11, 14-15

Grounds 2, 4, and 5 for ’347 & Grounds 2-6 for ’335
Yoshida | Prior Art Overview

Gate electrode G deposited onto already etched p-type GaN layer 5 ¶23 (i.e., a “gate-last” process)

p-type GaN layer 5 “etch[ed] away . . . except for where the gate electrode was to be loaded” ¶22



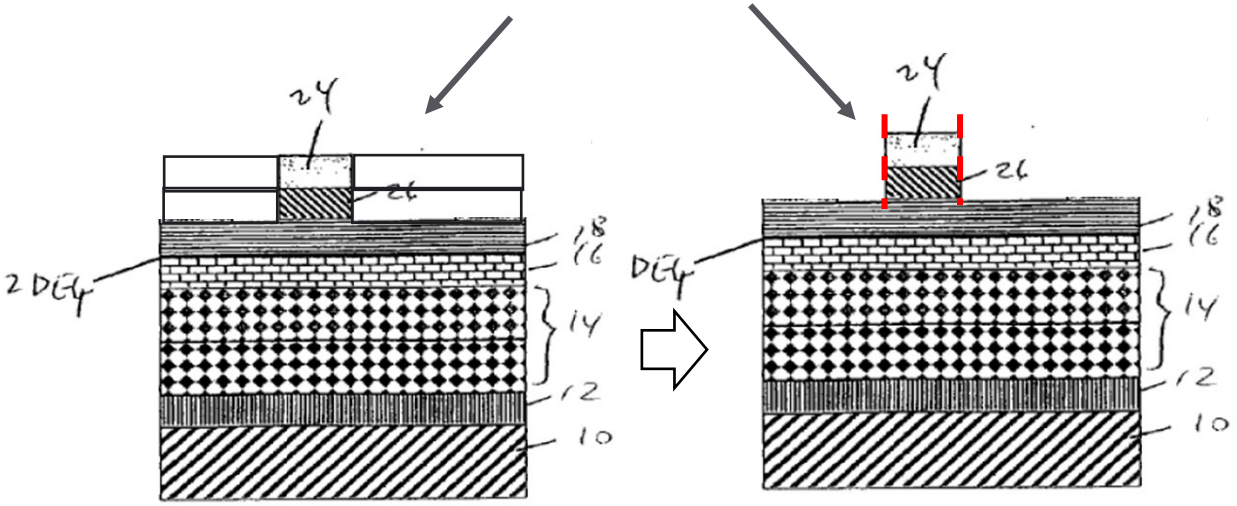
pn junction of a p-type GaN layer 5 “immediately under” the gate electrode G for “voltage control with a small amount of carrier injection” ¶17

Ledges of p-type GaN layer 5 formed for later deposition of gate electrode G (not refuted by Petitioner)

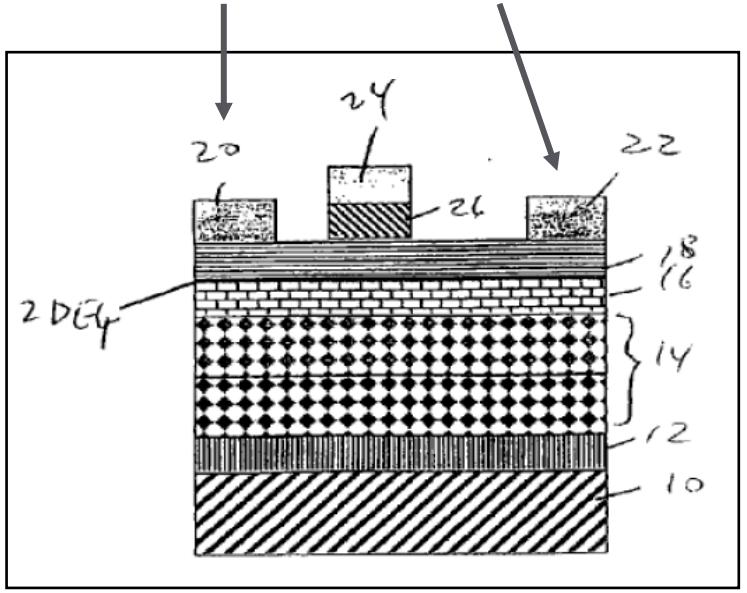
’347: Paper 17 at 13-15, 57-59; Paper 21 at 23
’335: Paper 17 at 10-14, 69-70; Paper 21 at 25-26

Grounds 1, 2, and 4 for ’347 & Grounds 3 and 6 for ’335
Beach | Prior Art Overview

Gate arrangement 24 and gate barrier 26 is patterned and etched to form a self-aligned gate arrangement. Fig 2F, ¶40.



Gate arrangement is fabricated before the ohmic contacts 20, 22 are formed on the device (i.e., a “gate-first” process). Fig 2F, ¶40



Beach forms self-aligned ***sidewalls***

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 16, 38-39; Paper 21 at 14
’335: Paper 17 at 14-15, 68; Paper 21 at 17

Grounds 1, 2, and 4 for ’347 & Grounds 3 and 6 for ’335
Shenoy | Prior Art Overview

Shenoy is purely mathematical model

Shenoy produces an undercut (U) based on underlying insulator that has no current distribution (i)

Model Development

The parameters that characterize the shape evolution during through-mask EMM are (Fig. 1): (*i*) aspect ratio, h/L, (*ii*) spacing to opening ratio, a/L, (*iii*) metal film thickness ratio, b/L, and (*iv*) mask wall angle, β. The aspect ratio, spacing to opening ratio, and the mask wall angle influence the current distribution at the electrode. On the other hand, the metal film thickness ratio determines the extent to which EMM must proceed before the underlying insulator is exposed. The influence of these parameters on the undercut, U, and the etch factor are of interest. The etch factor is defined as the ratio of the maximum etched depth to the undercut, (d/U). Once the insulator is exposed, metal dissolution continues in the lateral direction leading to a change in metal wall angle, χ. Fine line through-mask EMM of metal films on insulator requires minimized undercut (hence increased etch factor), and straight walls. In this investigation, the influence of the mask wall angle, β, on the etch factor has been evaluated.

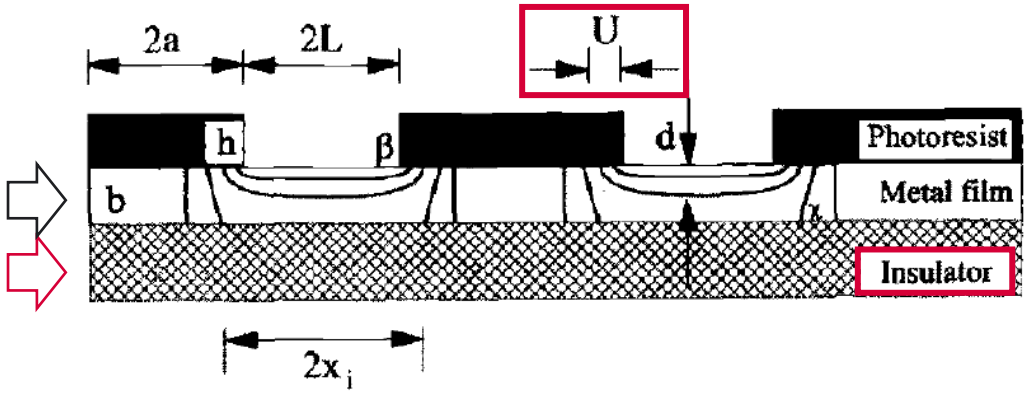


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

The current distribution at the anode has been combined with Faraday’s law to determine the evolution of the metal surface. The rate, r, at which the anodic surface recedes is

$$r = \frac{M\theta}{nF\rho} i \qquad [5]$$

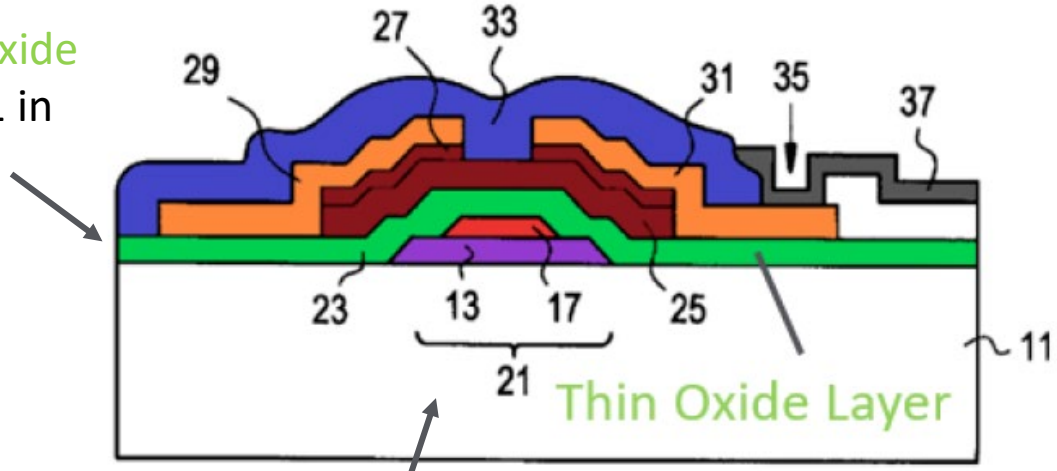
where M is the molecular weight of the metal, n is the metal dissolution valence, ρ is the density of the metal film, F is Faraday’s constant, and θ is the current efficiency of metal dissolution which is assumed to be constant at 100%.

’347: Paper 17 at 17, 40-44; Paper 21 at 16-17

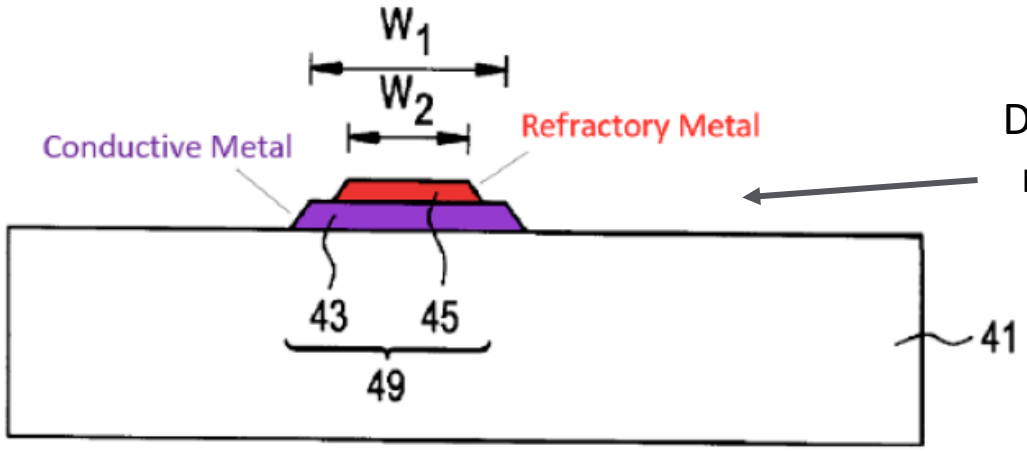
’335: Paper 17 at 15-16, 50-56; Paper 21 at 20-21

Grounds 3 and 5 for ’347
Ahn | Prior Art Overview

Thin film transistor characterized by insulating layer 23 (“gate oxide layer”) thinly separating semiconductive layer 25 from gate 21 in vertical arrangement



Deterioration of the thin gate oxide layer 23 may cause an electrical connection between the semiconductive layer 25 and the gate 21 causing short circuit



Double-step gate structure formed by additional etching to reduce deterioration of overlying thin gate oxide layer 23

Ahn has unrelated structure, function, and fabrication

’347: Paper 17 at 17-21, 53-55

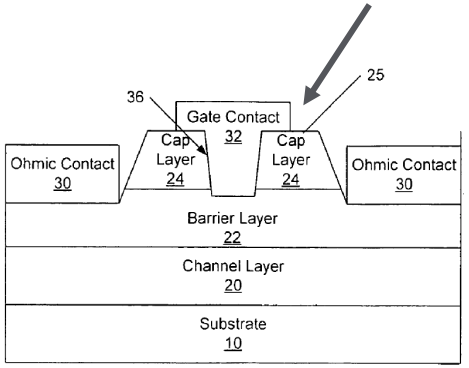
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

General Concepts

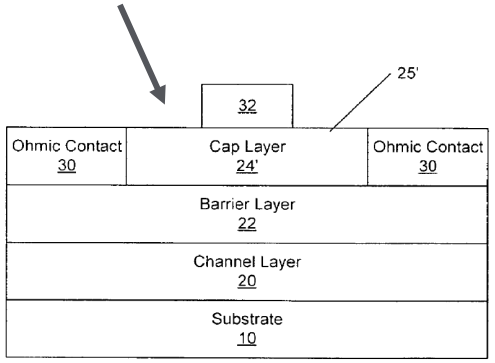
Overview
Enhancement-Mode v. Depletion-Mode Transistors

Depletion-Mode (e.g., Saxler)
Normally On
"Pinch" off 2DEG <u>just under gate</u> to turn off

Because of "pinching" function, <u>p-GaN can extend the entire or substantially the entire length between the ohmic contacts and still function in depletion-mode</u>.



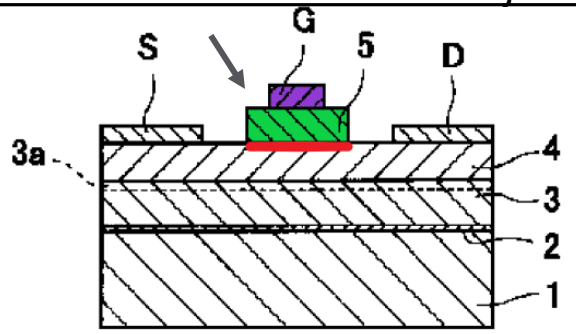
Saxler - FIG. 1A



Saxler - FIG. 1B

Enhancement-Mode (e.g., Yoshida)
Normally Off
Replenish <u>entire</u> length of 2DEG under cap layer to turn on

p-type GaN layer 5 "<u>etch[ed] away . . . except for where the gate electrode was to be loaded</u>" to form pn junction "immediately under" the gate electrode G for "<u>voltage control with a small amount of carrier injection</u>"



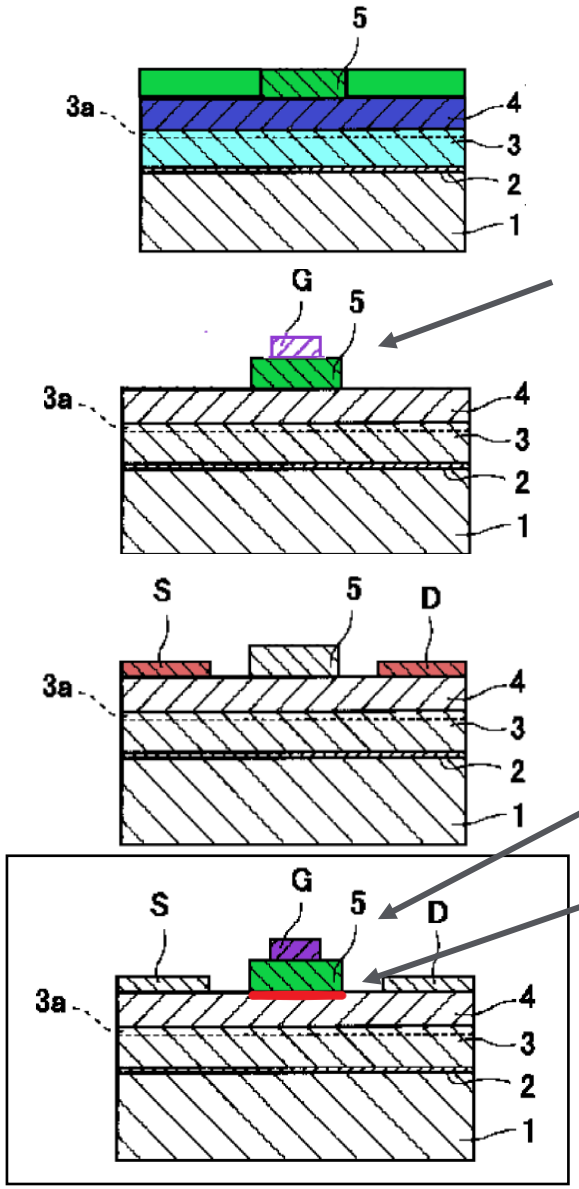
Yoshida - FIG. 1

Dr. Schubert: E-Modes are designed to minimize length of 2DEG that needs to be replenished to turn transistor ON (voltage control)

'347: Paper 17 at 30-31; Paper 21 at 10-11
'335: Paper 17 at 27-28; Paper 21 at 15-16

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Overview
"Gate-Last" v. "Gate-First" Fabrication



"Gate-Last" Fabrication
(e.g., Yoshida)

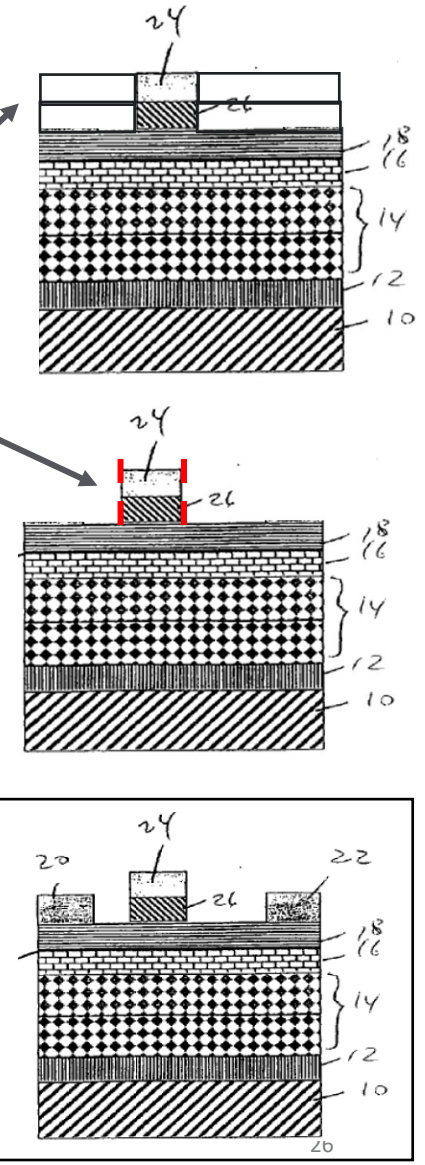
p-GaN 5 etched wider to receive later deposited Gate Contact

Gate Contact is then deposited on p-GaN 5 after p-GaN 5 is etched

pn junction of a p-type GaN layer 5 "immediately under" the gate electrode G for "voltage control with a small amount of carrier injection"

"Gate-First" Fabrication
(e.g., Beach)

Gate arrangement 24 and gate barrier 26 etched together to form self-aligned sidewalls



'347: Paper 17 at 13-16, 57-62
'335: Paper 17 at 10-15, 68-72

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Substance of Grounds

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-6 of ’335 | Independent Claim 1

[1p] An enhancement-mode GaN transistor, comprising:
[1a] a GaN layer;
[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
[1c] a source contact and a drain contact formed on the barrier layer;
[1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,
[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

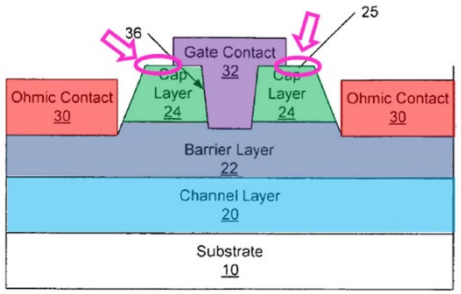
Horizontal Ledges

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

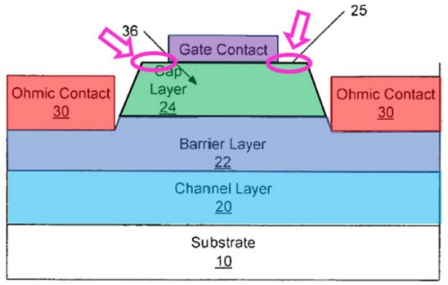
Grounds 1-6 of ’335
The Petition relies solely on drawings for “substantially equal widths”

The Petition relies solely on transistor schematics without providing any “articulated reasoning” of forming ledges of “substantially equal widths”

Under Ground 1, *Saxler* depicts its **gate contact** is narrower than its **cap layer**, thereby exposing **horizontal ledges** with substantially equal widths that extend past the respective sidewalls of the **gate** and toward the **source** and **drain** as shown in Figure 1A below. *Saxler*, Fig. 1A; Shealy, [132]-[133]. In some embodiments, *Saxler*’s gate recess is not present or does not separate the **cap layer** into distinct portions. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; Shealy, [133]; §VIII.B.5 (Grounds 1-2, [1d]). A POSITA would have understood *Saxler*’s **gate contact** in non-recessed embodiments (or embodiments where the recess did not extend through the **cap layer**) would similarly be narrower than the **cap layer** to expose the **horizontal ledges**. Shealy, [133]. *Saxler* thereby discloses or at least renders [1f] obvious (Ground 1).*Id.*

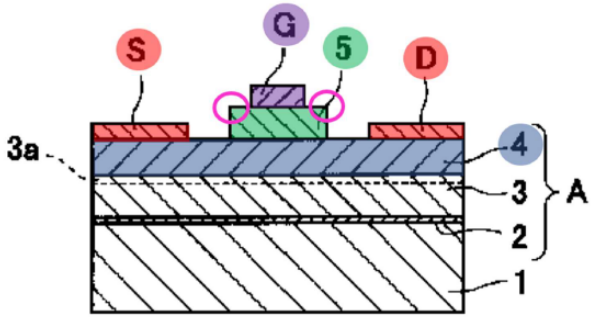


Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

Yoshida’s **gate electrode** is narrower than **layer 5**, thereby exposing **horizontal ledges** that extend past the respective sidewalls of the **gate electrode** and toward the **source** and **drain**. *Yoshida*, [0022]-[0023], Fig. 1; Shealy, [214]. These ledges are symmetric on either side of the gate metal (i.e., having substantially equal widths). *Yoshida*, Fig. 1; Shealy, [214]. *Yoshida* thus discloses this element (Ground 4).



’335: Paper 1 at 49, 83; Paper 17 at 2-3, 29, 59-60; Paper 21 at 1, 4

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-6 of ’335
Case law establishes that drawings cannot be relied on to disclose precise or relative proportions, including “substantially equal”

Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc., holds that drawings cannot be relied on to disclose precise or relative proportions

fins are drawn to scale. HHI's argument thus hinges on an inference drawn from certain figures about the quantitative relationship between the respective widths of the groove and fins. Under our precedent, however, it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue. *See In re Wright*, 569 F.2d 1124, 1127, 193 USPQ 332, 335 (CCPA 1977) (“Absent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value.”); *In re Olson*, 41 C.C.P.A. 871, 212 F.2d 590, 592, 101 USPQ 401, 402 (CCPA 1954); *cf. Manual of Patent Examining Procedure* 2125 (1998). Thus,

Hockerson-Halberstadt, 222 F.3d 951, 956 (Fed. Cir. 2000)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’335: Paper 17 at 2-3, 31-32; Paper 21 at 1

Grounds 1-6 of ’335
Case law establishes that drawings cannot be relied on to disclose precise or relative proportions, including “substantially equal”

The Board applied *Hockerson* to “substantially equal” in *Ex Parte Bjorn*, No. 2018-001567, 2019 WL 6173305 at *17 (P.T.A.B. Oct. 16, 2019)

The issue is whether Lazzara's abutment portion, which is larger in diameter than the maximum diameter of the bone fixture screw threads in Figure 9, can be considered “substantially equal to the maximum thread diameter of the male screw section of the bone fixture” as recited in claim 8.

The Specification therefore discloses the abutment diameter D1 as being up to 20% less than the maximum thread diameter D2 but no greater than that diameter D2, namely “1 to 1 on the high end.” Because claim 8 recites “substantially equal” rather than “equal,” we agree with the Examiner that Lazzara's abutment exterior surface may have a diameter that is larger than the maximum thread diameter and meet the claim limitation. However, even if we determine what percentage or ratio of an oversized abutment diameter is permitted within the scope of the claim, the drawings cannot be relied on to disclose such precise or relative proportions. *See Hockerson-Halberstadt*, 222 F.3d at 956. The Specification indicates that “substantially equal” requires abutment diameter D1 to be very nearly equal to maximum thread diameter D2. We cannot make that determination from Figure 9 of Lazzara, which illustrates the abutment diameter as larger than the maximum thread diameter, but Figure 9 is not disclosed as being to scale or having any particular dimensions. Thus, we do not sustain the rejection of claim 8 or claim 10, which depends from claim 8.

Petitioner’s own case law states that you cannot rely on drawings for “substantially equal” dimensions

Ex Parte Bjorn, No. 2018-001567, 2019 WL 6173305 at *17.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’335: Paper 17 at 3, 32; Paper 21 at 1, 4-5; Paper 10 at 1-2

Grounds 1-6 of ’335
The Petitioner continues to rely on irrelevant holdings in the same case law

The Petitioner is misdirected for repeatedly citing passages in *Ex Parte Bjorne* where the Board is explicitly not applying *Hockerson* in relying on the drawings to address an open-ended range

We agree that "patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." *Hockerson-Halberstadt, Inc. v. Avia Group. Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000). "[A]rguments based on measurements of a drawing are of little value" if there is no written description in the specification of quantitative values or no indication that the drawings are to scale. *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977); *Go Med. Indus. Pty, Ltd. v. Inmed Corp.*, 471 F.3d 1264, 1271 (Fed. Cir. 2006). However, "a drawing is available as a reference for all that it teaches a person of ordinary skill in the art." *In re Meng*, 492 F.2d 843, 847 (CCPA 1974; *see also In re Aslanian*, 590 F.2d 911, 914 (CCPA 1979) (same). Furthermore, things shown clearly in patent drawings are not to be disregarded. *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972). Therefore, "a drawing in a utility patent can be cited against the claims of a utility patent application even though the feature shown in the drawing was unintended or unexplained in the specification of the reference patent." *Aslanian*, 590 F.2d at 914; *see also In re Seid*, 161 F.2d 229, 231 (CCPA 1947) ("an accidental disclosure, if clearly made in a drawing, is available as a reference.").

In this case, claim 1 merely requires the abutment to have an exterior surface diameter that is "less than or substantially equal to the maximum thread diameter of the male screw section of the bone fixture." No particular dimensions or proportions are claimed. We agree with the Examiner that the drawings of Shepard clearly disclose to a skilled artisan that abutment 82 has exterior surfaces with a diameter that is "less than or substantially equal to the maximum thread diameter of the male screw section of the bone fixture" as claimed. Shepard's Figures 15, 19, 22, and 29 are reproduced below.

Ex Parte Bjorn, No. 2018-001567, 2019 WL 6173305 at *10

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’335: Paper 17 at 3, 32; Paper 21 at 1, 4-5

Grounds 1-6 of ’335
Transistor schematics are known by POSITA to not be accurate, and Petitioner specifically relies on this “principle”

Even in instances where *Hockerson* is not applied, the Board considers the prior art and the accuracy of the drawings. The prior art, Petitioner, and Dr. Shealy repeatedly discredit the drawings.

Petitioner relies on this “principle” of schematics not representing a transistor “when built in a practical device” to address Yoshida

Saxler ¶42

etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the present invention.

2, 5). Although *Yoshida* draws substantially vertical sidewalls of p-type **layer 5**, a POSITA would have known a sidewall drawn vertically would have a slight slope when built in a practical device. *Id.*

A POSITA would have been familiar with this principle. Shealy, [204] (citing *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5). For example, *Saxler* notes that, in practice, “an etched region illustrated as a rectangle will, typically, have ***tapered***, rounded or curved features.” *Saxler*, [0042]; Shealy, [204]. As another example, a 2006 IEEE

’335: Paper 1 at 75-76; Paper 17 at 35-37; Paper 21 at 5-7

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-6 of ’335
Transistor schematics are known by POSITA to not be accurate, and Petitioner specifically relies on this “principle”

Dr. Shealy further repeatedly discredits the transistor schematics as being inaccurate, but somehow relies on precise dimensions of schematic ledges (and sidewalls) for invalidity purposes

Dr. Shealy: Yes. You'll note that the vertical scale of these diagrams is exaggerated, so you could see details of the epitaxial layer.

Dr. Shealy: 1B is a strange cartoon.

Dr. Shealy: You could fabricate something that is intended to -- you know, this can be like a, I don't know, some sort of a crude design.

But there's no way to place Ohmic contacts and butt them up against that cap layer with no gap in between, as shown.

Yoshida’s drawings are also not accurate in vertical scale

Dr. Shealy: . But that's -- Figure 1 doesn't appear like what's described in 23, because the SiO2 isn't shown there. And it obviously was removed to get to that figure.

’335: Paper 17 at 36-37, 60

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-6 of ’335
Transistor schematics are known by POSITA to not be accurate, and Petitioner specifically relies on this “principle”

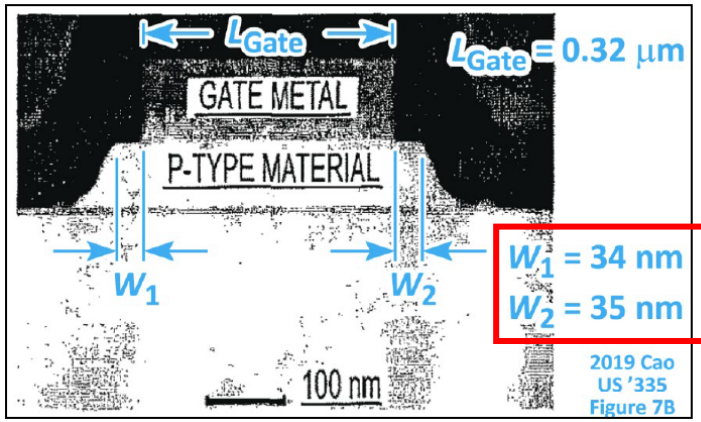


FIG. 6 of the ‘335 Patent
(TEM Image)

Substantially equal ledges formed by the self-aligned technique of the patent

Uemoto – as Petitioner relied on to illustrate previously mentioned “principle” of schematics not representing a transistor “when built in a practical device”

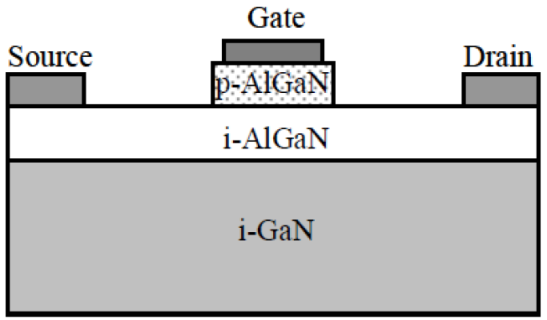


Fig. 1 - Schematic

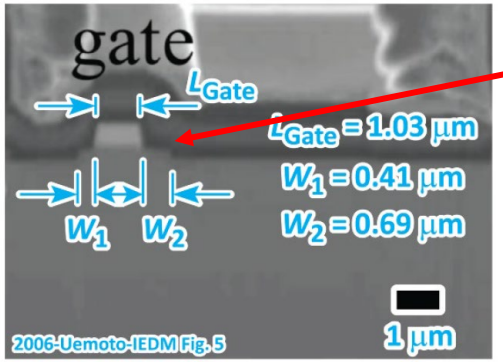


Fig. 5 – SEM Image

Dr. Shealy: `I would not call those "substantially equal ledges," no.`

’335: Paper 17 at 30-31, 33; Paper 21 at 7

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-6 of ’335
The Petition improperly attempts to introduce motivation for “substantially equal widths” in the Reply

In the Reply, Petitioner improperly attempts to introduce a motivation

- In the Reply, Petitioner attempts to rely on the conclusory statement of “a POSITA would have seen Figure 1A [of Saxler] shows a centered gate with ledges of substantially equal width and found such a gate obvious.”
  - The Petition relies on disclosure is completely devoid of a motivation to modify, which cannot be entered in a Reply
  - Even considering this argument from the Reply, Figure 1A by itself is not a sufficient motivation to modify with an expectation of success
  - Furthermore, Saxler ¶42 contradicts this argument by explicitly disclosing “the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device” (which Petitioner explicitly relies on to address Yoshida for another feature)
- In the Reply, Petitioner provides even less reasoning for obviousness in view of Yoshida

’335: Paper 17 at 35-37; Paper 19 at 18; Paper 21 at 4, 7-9

Grounds 1-6 of ’335 | Independent Claim 5

[5p] An enhancement-mode GaN transistor, comprising:
[5a] a GaN layer;
[5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
[5c] a source contact and a drain contact disposed on the barrier layer;
[5d] a p-type gate material formed above the barrier layer and between the source and drain contacts; and
[5e] a gate metal disposed on the p-type gate material,
[5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and
[5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

Self-Aligned Ledges

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-6 of ’335
Petitioner fails to provide sufficient basis for “self-aligned ledges”

Patent Owner establishes that “self-aligned ledges” [5f] are not product-by-process.

However, even if [5f] was construed as “product-by-process”, Petitioner fails to provide any additional analysis (with respect to [1f]), thus fails to show the “product” of the prior art is the same as the claimed “self-aligned ledges” as required by law. *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1369 (Fed. Cir. 2009) (“In determining validity of a product-by-process claim, the focus is on the product and not the process of making it.”).

Dr. Shealy

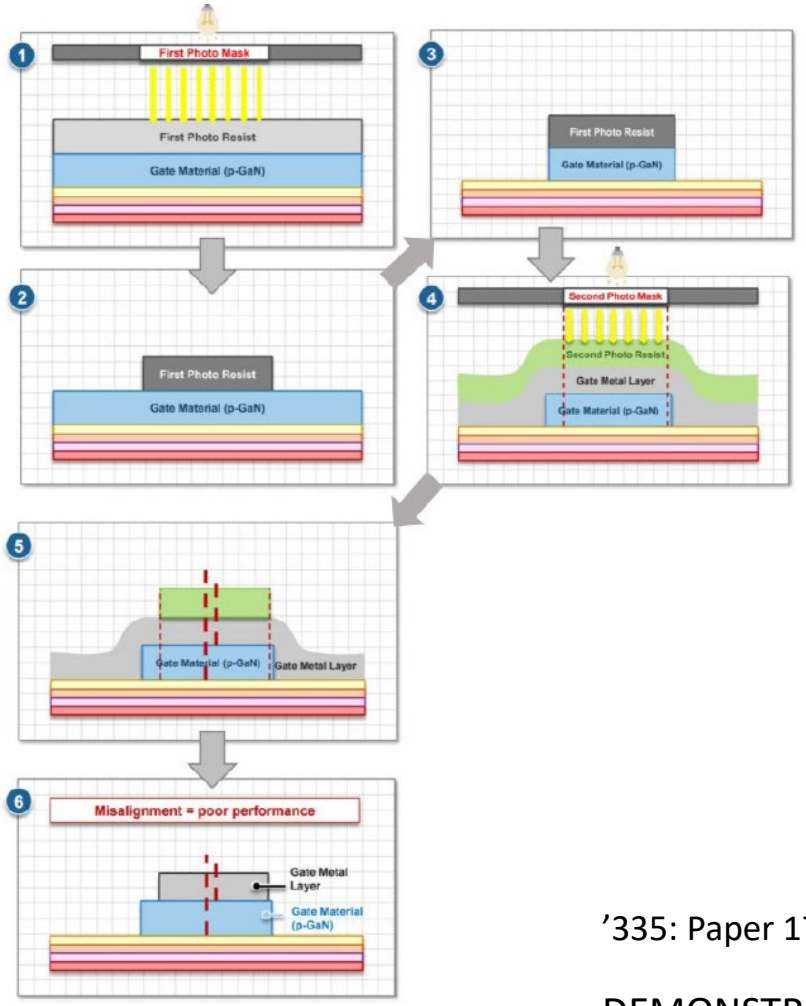
[135] Claim 2 is for a transistor, but the term “self-aligned” refers to ***how*** the transistor’s ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that claim 2 is thus drawn a product-by-process claim for “self-aligned” ledges, which lends no patentable weight. §IX.B (Claim Construction). So for reasons I explained above for Limitation [1f], claim 2 is obvious over *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2). §X.B.7 (Grounds 1-2, Limitation [1f]).

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

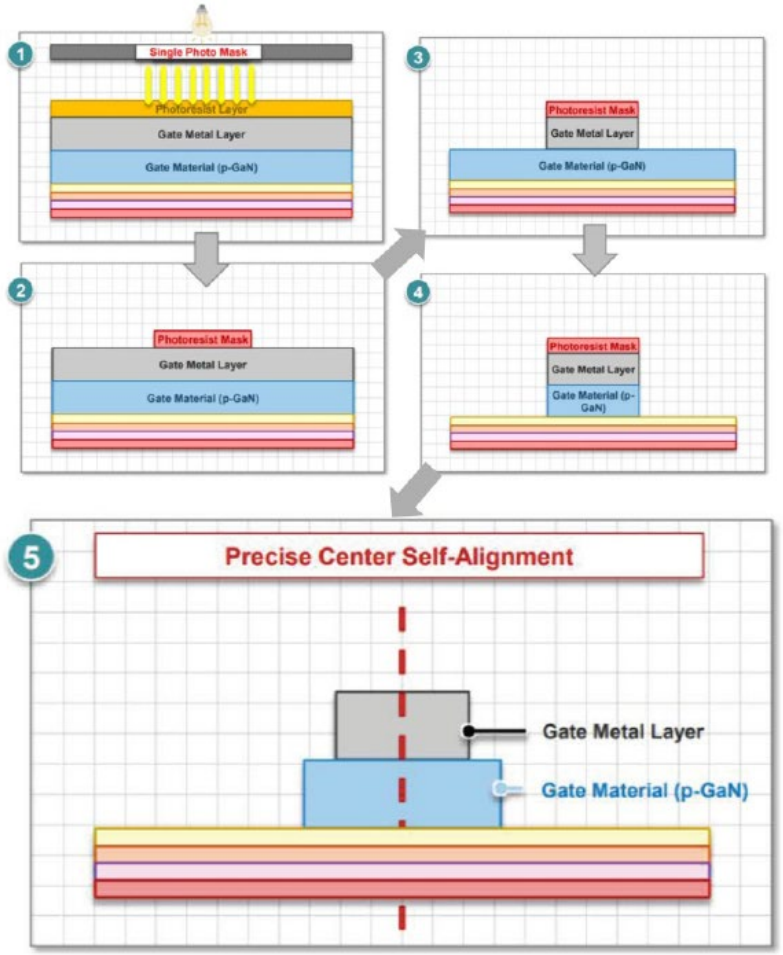
’335: Paper 17 at 38-44; Paper 21 at 9

Grounds 1-6 of ’335
Petitioner fails to provide sufficient basis for “self-aligned ledges”

Two-Mask Approach



One-Mask (“Self-Aligned”) Approach



’335: Paper 17 at 38-44

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 4 of ’335 | Independent Claim 1

[1p] An enhancement-mode GaN transistor, comprising:
[1a] a GaN layer;
[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
[1c] a source contact and a drain contact formed on the barrier layer;
[1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,
[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

Side Surfaces

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 4 of ’335 | Independent Claim 5

[5p] An enhancement-mode GaN transistor, comprising:
[5a] a GaN layer;
[5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
[5c] a source contact and a drain contact disposed on the barrier layer;
[5d] a p-type gate material formed above the barrier layer and between the source and drain contacts; and
[5e] a gate metal disposed on the p-type gate material,
[5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and
[5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

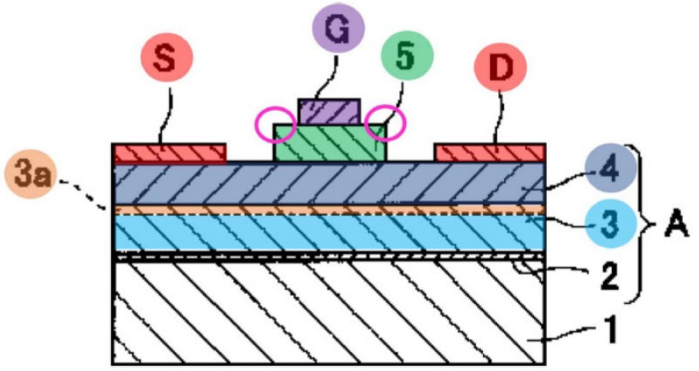
Side Surfaces

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 4 of ’335
Petitioner abandons its basis of the Petition and attempts to introduce a new “obviousness” position in the Reply

The Petition relies on inherency under § 102 for [1d], without providing any motivation to modify

“Under Patent Owner's construction of the slope terms (‘p-type gate material having side surfaces extending horizontally such that the bottom of the material is wider than the top of the material’), a POSITA would know ***any*** **constructed embodiment would *necessarily* extend at least slightly on the bottom due to manufacturing tolerances**.”



Yoshida, Fig. 1.

However, Dr. Shealy and Dr. Schubert agree that vertical or undercut walls are a possibility

Indeed, in the Reply, Petitioner specifically takes the position that “this does not mean a vertical sidewall would not have been obvious”

- In the Reply, Petitioner concedes “inappropriate[]” argument addressing anticipation, thus abandons the basis of the Petition.
- Petitioner attempts to improperly replace its prior § 102 position with a new “obviousness” position, which should not be considered.
- Even considering the new obviousness argument, Petitioner still fails to provide a motivation to modify Yoshida by replacing the vertical sidewalls with laterally extending sidewalls.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

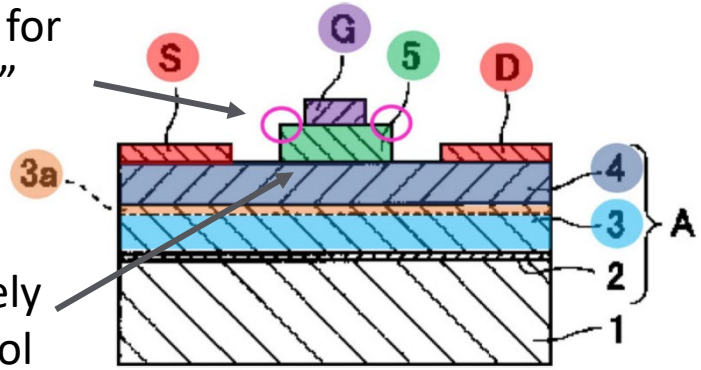
’335: Paper 1 at 67-68; Paper 17 at 61-62; Paper 19 at 18, 21-25, 25; Paper 21 at 21-23

Ground 4 of ’347 & Grounds 5 & 6 of ’335
A POSITA would not modify Yoshida with the tapered walls of Saxler

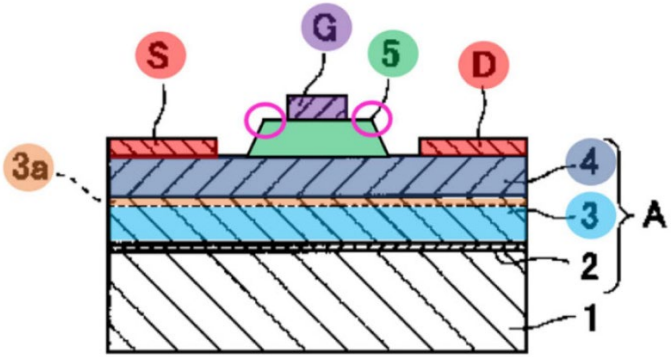
Widening the p-type GaN layer 5 would reduce desired “voltage control.” Cap layer structure of Saxler’s D-Mode transistor functions differently than E-Mode and is irrelevant.

p-type GaN layer 5 “etch[ed] away . . . except for where the gate electrode was to be loaded”

pn junction of a p-type GaN layer 5 “immediately under” the gate electrode G for “voltage control with a small amount of carrier injection”

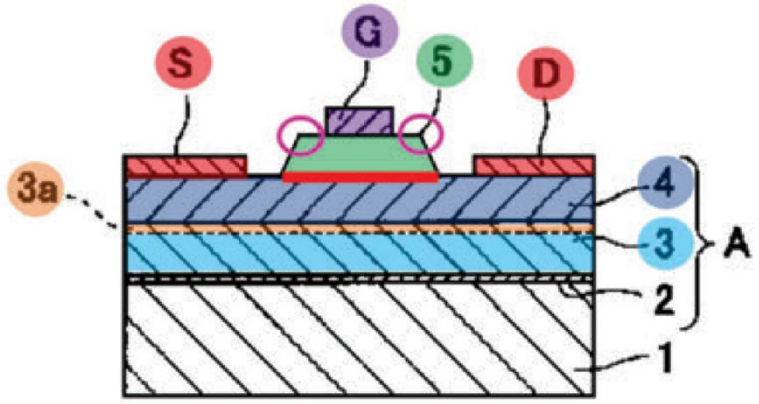


Yoshida, Fig. 1.



Yoshida, Fig. 1 (modified).

- In the Reply, Petitioner attempts to shift to “alternative” obviousness rational, which should not be considered.
- Even if considered, it would have same deficiencies of widening pn junction relative to GaN layer 5 by “more than 10%” reducing “voltage control” in that that pn junction is not “immediately under” the gate electrode G



’347: Paper 19 at 26; Paper 21 at 20-22
’335: Paper 17 at 63-66; Paper 19 at 25-26; Paper 21 at 23-25

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1 and 3 for ’347 | Independent Claim 1

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

[1d] depositing a p-type gate material on the barrier layer;

[1e] depositing a gate metal on the p-type gate material;

[1f] forming a photoresist over the gate metal;

First Etching Step

[1g] etching the gate metal and the p-type gate material,

[1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

[1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 1 for ’335 | Independent Claim 1

[1p] An enhancement-mode GaN transistor, comprising:
[1a] a GaN layer;
[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;
[1c] a source contact and a drain contact formed on the barrier layer;
[1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,
[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

Horizontal Ledges

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 1 for ’335 | Independent Claim 5

[5p] An enhancement-mode GaN transistor, comprising:

[5a] a GaN layer;

[5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[5c] a source contact and a drain contact disposed on the barrier layer;

[5d] a p-type gate material formed above the barrier layer and between the source and drain contacts; and

[5e] a gate metal disposed on the p-type gate material,

Self-Aligned Ledges

[5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

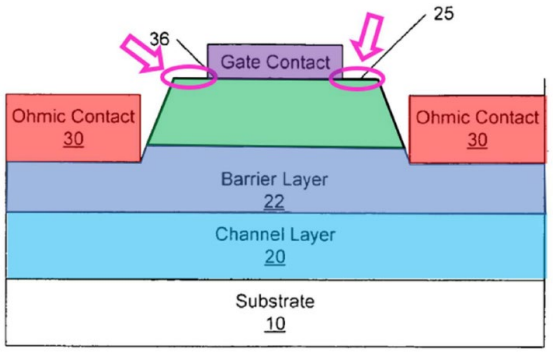
[5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1 and 3 for ’347 & Ground 1 for ’335
Petitioner relies on disclosure for 1) “Saxler’s Non-Recessed Embodiment” and 2) E-Mode

The Petition relies on disclosure 1) of “Saxler’s Non-Recessed Embodment” and 2) that Saxler’s transistors (including Figs. 1A, 1B) are enhancement-mode transistors

Saxler’s gate contact may be recessed or non-recessed (i.e., flat). *Saxler*, [0052], [0066]. Where the gate recess is not utilized, *Saxler* would result in the following structure. Shealy, [081].



Saxler, Fig. 1A (modified).

“Saxler’s non-recessed embodiment”

embodiments, the recess in *Saxler*’s cap layer 24 is optional, and where not employed the cap is a continuous material. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; Shealy, [121].

preamble. Shealy, [099]-[100]. *Saxler* discloses a GaN high-mobility transistor that includes a p-type doped GaN cap layer below the gate and above an AlGaN barrier layer. *Saxler*, [0007]-[0010], [0013], [0046], [0059]-[0064] Figs. 1A, 1B; Shealy, [099]. This constitutes a normally off enhancement-mode GaN transistor. Shealy, [099]. *Saxler* discloses methods for making this transistor. Saxler, [0053]-[0066], Figs. 1A-1B.

A POSITA would have understood that *Saxler*’s transistors were enhancement-mode GaN transistors at least because of their gate structure. Shealy,

The Petitions rely on a disclosure

’347: Paper 1 at 25, 31, 34-36, 45 (quoted)
’335: Paper 1 at 24-26; 35 (nearly identical)

Grounds 1 and 3 for ’347 & Ground 1 for ’335
“Saxler’s Non-Recessed Embodiment” not actually disclosed by Saxler, thus Petitioner abandons its basis of Petitions

Petitioner abandons its position in the Petition that 1) Saxler discloses the transistor relied on in the Petition; and 2) Saxler discloses an enhancement-mode transistor

In his deposition, Dr. Shealy clarifies that “Saxler’s non-recessed embodiment” was based on ¶52 of Saxler and his opinion is that he “mix and match” and “take all the embodiments and bring in which ones you want, depending on what you’re trying to accomplish.”

Petitioner agrees “Saxler’s non-recessed embodiment” and E-mode not disclosed

Dr. Shealy’s testimony accurately reflects obviousness law. His statement a POSITA “could take all the embodiments” accords with the principle that prior art must be considered for “everything it teaches.” *EXP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985). His statement a POSITA would “bring in which [embodiments] you want, *depending on what you’re trying to accomplish*,” acknowledges one may combine the teachings of the prior art with reason to do so. *KSR*, 550 U.S. at 401-402; *Boston Sci.*, 554 F.3d at 991. Dr. Shealy provided a reason to remove Figure 1A’s recess: to accomplish the benefits of enhancement mode. Shealy, [103]. The benefits of enhancement mode were well known, and Dr. Shealy’s analysis adheres to *KSR*.

’347: Paper 17 at 26-27; Paper 19 at 6 (quoted); Paper 21 at 3-5, 7
’335: Paper 17 at 21; Paper 19 at 5 (nearly identical); Paper 21 at 9-11

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1 and 3 of ’347 & Ground 1 of ’335
Petition provides no motivation to modify Saxler to produce “Saxler’s Non-Recessed Embodiment”

In the Reply, Petitioner failed to provide a motivation to modify to produce “Saxler’s Non-Recessed Embodiment”

In the Reply:

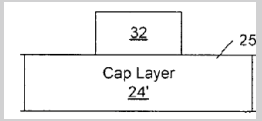
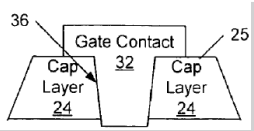
1) Petitioner cites unrelated grounds in alleging a motivation to produce E-Mode
   - The Petition relies on Saxler’s gate structures already being E-Mode (Why would POSITA modify Saxler to produce E-Mode when Saxler’s transistors are supposedly already E-Mode?)
   - Saxler does not mention E-Mode
   - KSR rationale not a basis in the Petition for this feature
   - Petitioner cites to unrelated grounds, which cannot be basis for obviousness

Saxler in view of Yoshida (Not Saxler alone)
’347: Paper 1 at 55-56; EX1003 ¶¶146-148
’335: Paper 1 at 33; EX1003 ¶103

2) Petitioner introduces a new motivation of to “simplif[y] Saxler’s Figure 1A”
   - Not supported by Petition, so should not be considered
   - No motivation, just “circular logic”
   - Saxler already discloses a non-recessed embodiment in FIG. 1B, and Petitioner still provides no motivation to modify recessed embodiment of FIG. 1A

’347: Paper 1 at 35-36; Paper 19 at 5-7; Paper 21 at 5-9
’335: Paper 1 at 35; Paper 19 at 5-6; Paper 21 at 11-14

Grounds 1 and 3 of ’347 & Ground 1 of ’335
The Recessed Embodiment is thicker and more highly doped, with a thicker doped region

Saxler Feature(s)	Non-Recessed Embodiment	Recessed Embodiment
Shape of cap layer and gate contact		
Thickness of cap layer	“from about 2 Å to about 20 Å”	“from about 5 to about 5000 Å”
Level of doping of cap layer	“should be sufficiently high so as to reduce leakage current… and be the dominant ‘surface’ state but not so high as to [] introduce traps or leakage paths by becoming a conductive layer”	“a high level of p-type dopants may be provided such that the cap layer 34’ may be provided as a conductive layer”
Dopant concentration of cap layer	“from about 10^{18} to about 10^{21} cm^{-3}”	“more heavily doped than 10^{21} cm^{-3}”
Thickness of doped region	“into the cap layer from about 2.5 Å to about 50 Å”	“into the cap layer from about 20 Å to about 5000 Å”

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 24-26
’335: Paper 17 at 18-21

Grounds 1 and 3 of ’347 & Ground 1 of ’335
Saxler distinguishes the Recessed and Non-Recessed Embodiments

Petitioner cites ¶¶13, 71 of Saxler for an alleged disclosure of the same concentration range, but ¶¶13, 71 just distinguishes the recessed embodiment and the non-recessed embodiment

Recessed

[0013] In other embodiments, the doped region is a region doped with p-type dopants. In particular embodiments of the present invention without a gate recess, the doped region extends into the cap layer from about 2.5 Å to about 50 Å. In particular embodiments of the present invention with a gate recess, the doped region extends into the cap layer from about 30 Å to about 5000 Å. The doped region may provide a dopant concentration of from about 10^{16} to about 10^{22} cm^{-3}. The p-type dopants may be Mg, Be, Zn, Ca or C. In particular embodiments of the present invention, the doped region may be one or more delta-doped regions at or near the surface of the cap layer and may, for example, have a dopant concentration of from about 10^{11} to about 10^{15} cm^{-2}.

Non-Recessed

Recessed

Non-Recessed

Recessed

[0071] In other embodiments, the doped region **40** is a region doped with p-type dopants. In particular embodiments of the present invention without a gate recess, the doped region **40** extends into the cap layer **34** from about 2.5 Å to about 100 Å. In particular embodiments of the present invention with a gate recess, the doped region **40** extends into the cap layer **34'** from about 30 Å to about 5000 Å. With p-type dopants, the doped region **40** may provide a dopant concentration of from about 10^{16} to about 10^{22} cm^{-3}. The p-type dopants may be Mg, Be, Zn, Ca and/or C. In particular embodiments of the present invention, the doped region may be one or more delta-doped regions at or near the surface of the cap layer and may, for example, have a dopant concentration of from about 10^{11} to about 10^{15} cm^{-2}. P-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents. The level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant “surface” state but not so high as to provide introduce traps or leakage paths by becoming a conductive layer. However, in particular embodiments of the present invention have a recessed gate as illustrated, for example, in **FIG. 2B**, if an insulating region, such as a SiN layer or gap, is provided between the cap layer **34'** and the gate contact **32**, a high level of p-type dopants may be provided such that the cap layer **34'** may be provided as a conductive layer.

’347: Paper 17 at 24-26; Paper 19 at 4
’335: Paper 17 at 18-21; Paper 19 at 4

Grounds 1 and 3 of ’347 & Grounds 1 of ’335
Saxler ¶52

Dr. Shealy misinterprets ¶52 to read:

- He can “mix and match” and “take all the embodiments and bring in which ones you want, depending on what you’re trying to accomplish”

Petitioner misinterprets ¶52 to read:

- “expressly acknowledges Saxler’s recess is optional in every figure”
- “***Saxler itself*** tells a POSITA to remove Figure 1A’s recess”

- Petitioner already admits that relied on transistor structure not disclosed (contradiction)
- Motivation still required for “obviousness law”, and none provided

[0052] Exemplary devices according to some embodiments of the present invention are schematically illustrated in **FIGS. 1A through 6**. Thus, while embodiments of the present invention are described herein with reference to a recessed gate structure or a non-recessed gate structure, other embodiments of the present invention may include or not include a gate recess. Accordingly, embodiments of the present invention should not be construed as limited to the particular exemplary embodiments described herein but may include any suitable structure having a cap layer and/or passivation layer as described herein.

- No illustration or further disclosure of these vague “other embodiments”
- No mention of “mix and match” embodiments
- No motivation or expectation of success

’347: Paper 17 at 27-28; Paper 19 at 5; Paper 21 at 3-5, 7-8
’335: Paper 17 at 21-22; Paper 19 at 4; Paper 21 at 9-13

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-3 of ’347 & Grounds 1-3 of ’335
Saxler’s Transistors are not E-Mode

Again, the Petition relies on Saxler’s disclosed gate structures being E-Mode.

preamble. Shealy, [099]-[100]. *Saxler* discloses a GaN high-mobility transistor that includes a p-type doped GaN cap layer below the gate and above an AlGaN barrier layer. *Saxler*, [0007]-[0010], [0013], [0046], [0059]-[0064] Figs. 1A, 1B; Shealy, [099]. This constitutes a normally off enhancement-mode GaN transistor. Shealy, [099]. *Saxler* discloses methods for making this transistor. Saxler, [0053]-[0066], Figs. 1A-1B.

A POSITA would have understood that *Saxler*’s transistors were enhancement-mode GaN transistors at least because of their gate structure. Shealy,

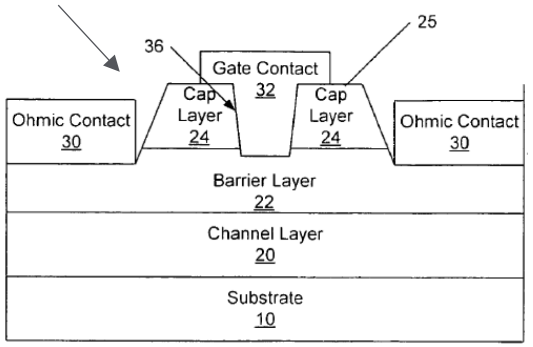
’347: Paper 1 at 36 (quoted)
’335: Paper 1 at 35 (nearly identical)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-3 of ’347 & Grounds 1-3 of ’335
Saxler’s Transistors are not E-Mode

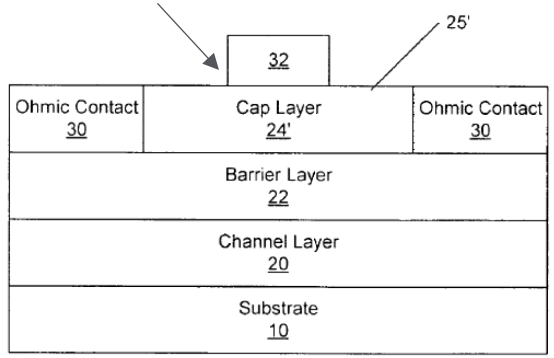
However, Saxler only discloses D-Mode transistors.

Petitioner: Not E-Mode



Saxler FIG. 1A

Petitioner: Not E-Mode



Saxler FIG. 1B

Petitioner: Not E-Mode

[0072] Furthermore, in certain embodiments of the present invention, the doped region **40** may be doped with p-type dopants so as to provide a p-n junction between the doped region and the cap layer **34** and the gate contact **32** is provided directly on the doped region **40** so as to provide a Junction HEMT (JHEMT). In such a case, the dope region **40** would not extend to the ohmic contacts **30**, which may be isolated from the doped region by an insulating region, Such as a SiN layer or gap.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

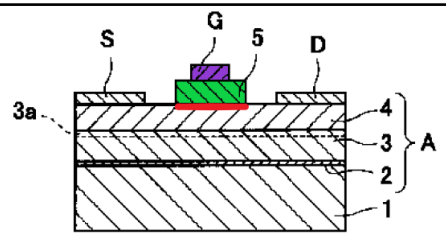
’347: Paper 17 at 28, 32; Paper 21 at 9
’335: Paper 17 at 22-24; Paper 21 at 14-15

Grounds 1-3 of ’347 & Grounds 1-3 of ’335
A POSITA would not retrofit Saxler’s D-Mode Transistor to produce E-Mode

A POSA would not be motivated to modify Saxler’s D-Mode transistor to produce an E-Mode transistor, at least because of the size of the cap layer

Enhancement-Mode	Depletion-Mode
Normally Off	Normally On
Replenish entire length of 2DEG under cap layer to turn on	“Pinch” off 2DEG just under gate to turn off

E-Mode - Yoshida

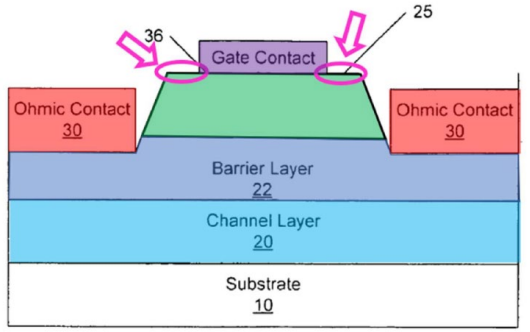


pn junction of GaN layer 5 “immediately under” gate electrode G for “voltage control with a small amount of carrier injection”

formed in gate-last approach by “etch[ing] away the p-type GaN layer except for where the gate electrode was to be loaded”

Petitioner’s own ITC Expert: a wide cap layer would require high voltage to turn on, producing “not… an ideal device” with “lots of leakage.”

Petitioner’s Modification based on a D-Mode Transistor



Saxler, Fig. 1A (modified).

Dr. Schubert: a POSA would not produce an E-mode device in this manner because of excess voltage requirements and might not even turn on.

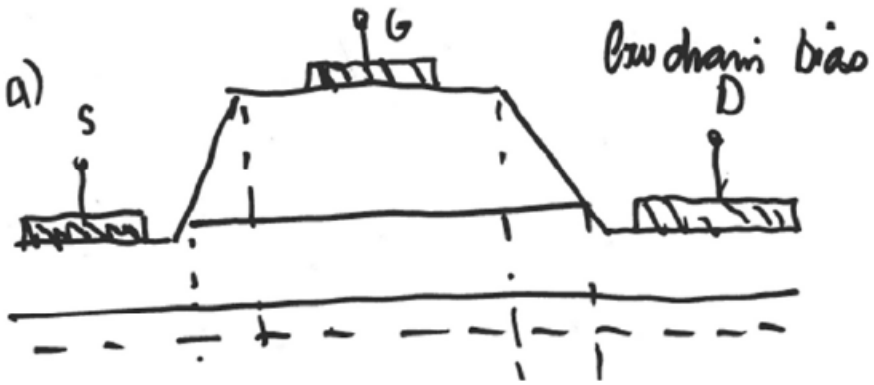
’347: Paper 17 at 30-32; Paper 21 at 9-11
’335: Paper 17 at 27-28; Paper 21 at 14-17

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

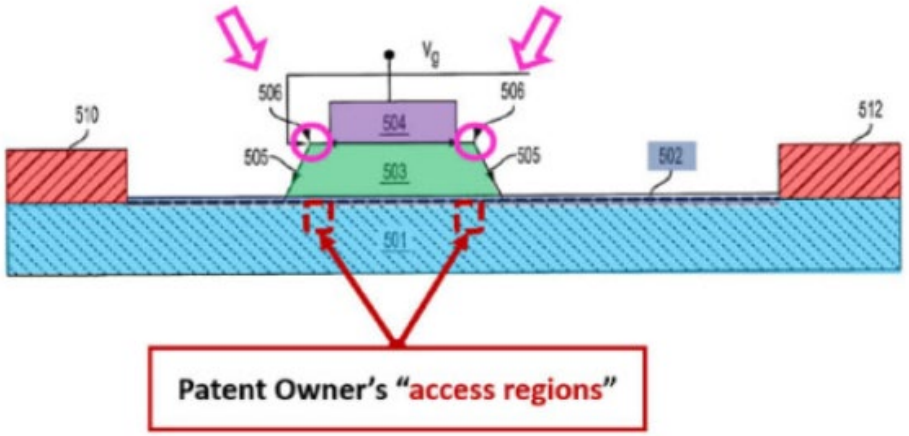
Grounds 1-3 of ’347 & Grounds 1-3 of ’335
Petitioner’s proposed transistor not “the same” as the transistor of patent

Petitioner improperly attempts to introduce a new argument that “the patent has the same ‘access regions’ as modified Figure 1A.”

Modified Fig. 1A (Shealy Depo)



Petitioner’s Annotation of FIG. 5 of Patent



- Pure attorney argument
- Petitioner misunderstands “access regions”
  - Access region refers to entire lengths of ***2DEG between the gate and the source and drain***, respectively, and not ***just the region underneath the cap layer***
- Access regions are <u>not</u> the “same”

’347: Paper 19 at 9-10; Paper 21 at 9-10
’335: Paper 19 at 9; Paper 21 at 14-15

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-5 of ’347 | Independent Claim 1

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

[1d] depositing a p-type gate material on the barrier layer;

[1e] depositing a gate metal on the p-type gate material;

[1f] forming a photoresist over the gate metal;

[1g] etching the gate metal and the p-type gate material,

[1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

[1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

First Etching Step

Second Etching Step

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-3 of ’347 & Grounds 3 & 6 of ‘335
Saxler’s Method is not “flexible” and Petitioner relies on substantial hindsight by piecing together disparate references

Petitioner mischaracterizes Saxler as “flexible” in an attempt to completely reengineer Saxler’s method of fabrication by piecing together disparate references with substantial hindsight bias.

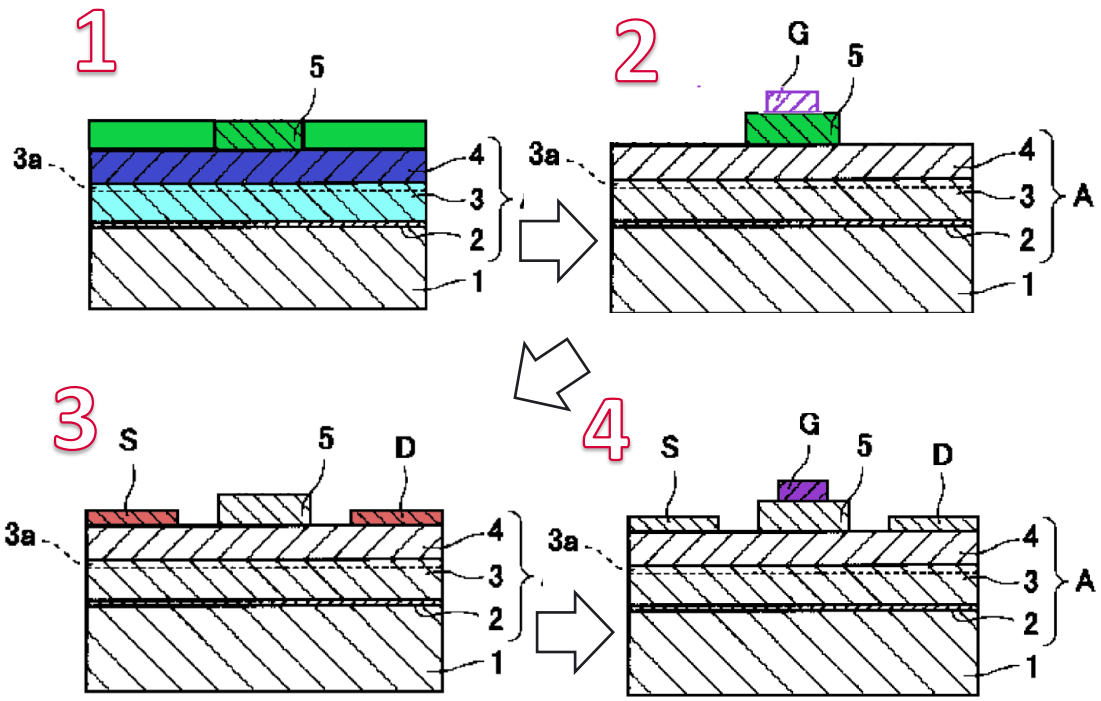
- Splitting steps or combining steps does not provide authority to completely reengineer Saxler’s method
- Petitioner improperly uses the present claims as a roadmap and attempts to “mix and match” disparate references “to accomplish” the claimed subject matter
- Petitioner improperly reengineers Saxler’s processes based on alleged “simple substitutions” which is fraught with hindsight bias
- Petitioner fails to even provide a specific process sequence
  - Apparently by strategy so they could improperly shift positions and combinations as they did in their Replies

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 2-3, 46-48; Paper 21 at 14-15
’335: Paper 17 at 57-59

Grounds 4 and 5 of ’347
Yoshida’s method is not “flexible” and Petitioner relies on substantial hindsight by piecing together disparate references

In falsely stating the Yoshida’s method is flexible and citing KSR, Petitioner takes complete freedom to “mix and match” components from divergent references to try to piece together the claimed steps through hindsight



Dr. Shealy establishes order of Yoshida

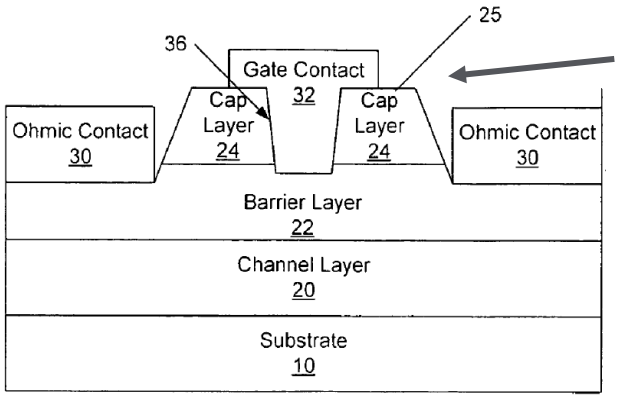
Specifically, *Yoshida* discloses: (i) depositing a p-type GaN layer 5 onto AlGaN layer 4 (*Yoshida*, [0021]); (ii) dry etching the “p-type layer except where the gate electrode was to be loaded” (*Yoshida*, [0022]); (iii) depositing an SiO_2 film over the entire surface (*id.*); (iv) patterning with a photoresist, and masking where the gate electrode was to be loaded (*id.*); (v) depositing source and drain electrodes (*id.*); (vi) “etching away the masking and opening the SiO2 film (*Yoshida*, [0023]); (vii) masking the source and drain electrodes; and (viii) depositing Au to form the gate electrode (*id.*).

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 55-56; Paper 21 at 19-20

Grounds 1-5 of ’347 & Grounds 3 and 6 of ’335
Petitioner improperly attempts to reverse engineer schematic drawings

Petitioner does not provide any reason/disclosure for a centrally aligned gate electrode. Saxler only discloses that electrode may be positioned “offset… closer to source contact.”

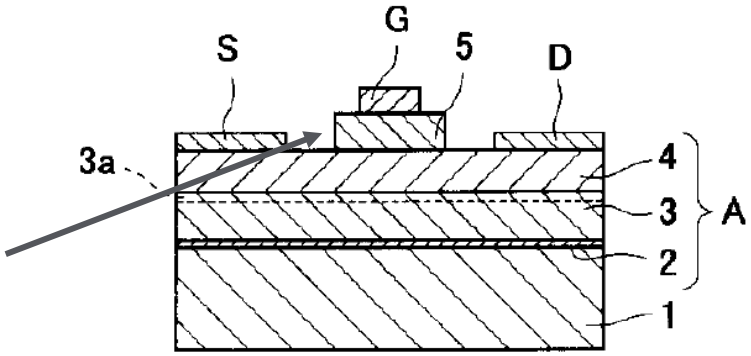


Saxler FIG. 1A

etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the present invention.

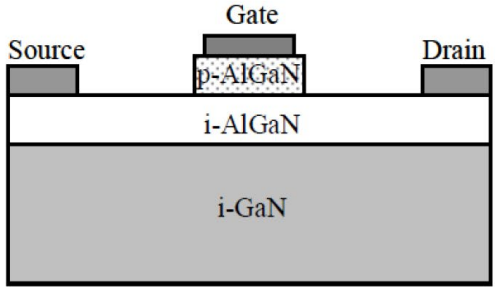
Saxler ¶42

Dr. Shealy: not an actual device

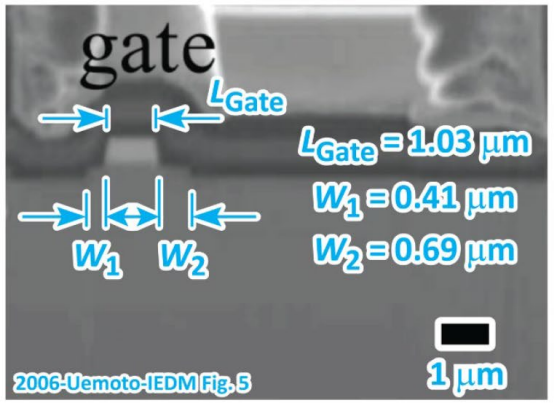


Yoshida Fig. 1

Saxler only discloses gate contact to be “offset… closer to the source contact than the drain contact”



Uemoto Fig. 1



Uemoto Fig. 5

Non-centrally aligned gate electrode

’347: Paper 17 at 34-37
’335: Paper 17 at 35-38

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1-3 of ’347 & Ground 3 of ’335
Saxler’s “Precise Positioning” as relied on by Petitioner

In Reply, Petitioner argued “Saxler’s need for precision is self-evident… because Saxler incorporates Smith for its fabrication methods, which addresses gate misalignment. Imprecise gate positioning would obviously lead to manufacturing defects, so a POSITA would have been motivated to improve gate alignment and positioning.”

“aligned to the source-side sidewall 27 of the gate electrode 26”

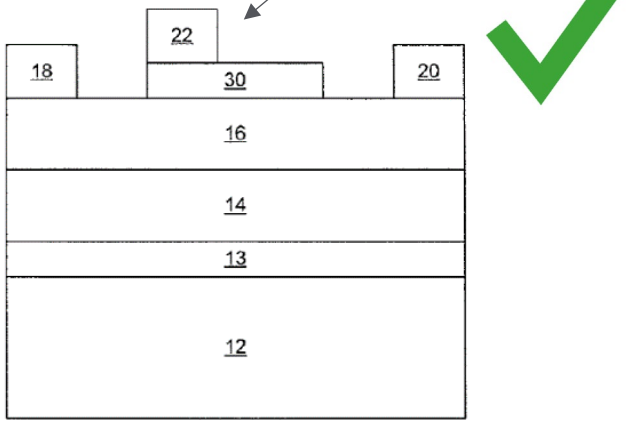


Figure 4C

“substantially aligned”

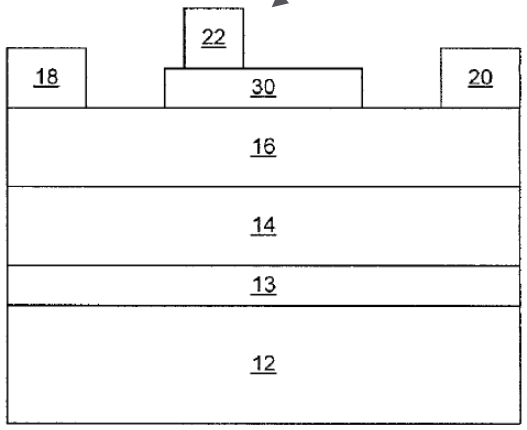
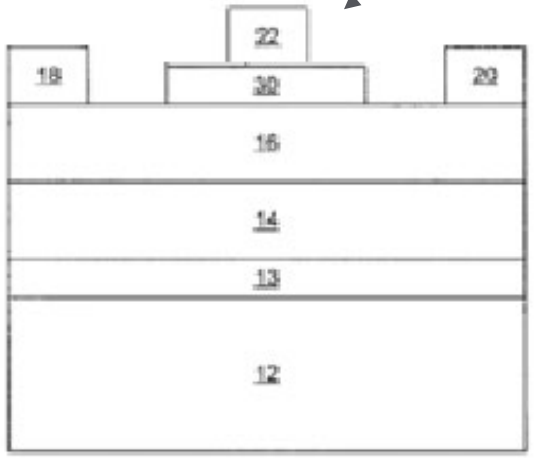


Figure 5B

“severe misalignment may be detrimental to the device”



Petitioner: “would obviously lead to manufacturing defects”

Reproduced from Smith (as incorporated into Saxler and relied on by Petitioner)

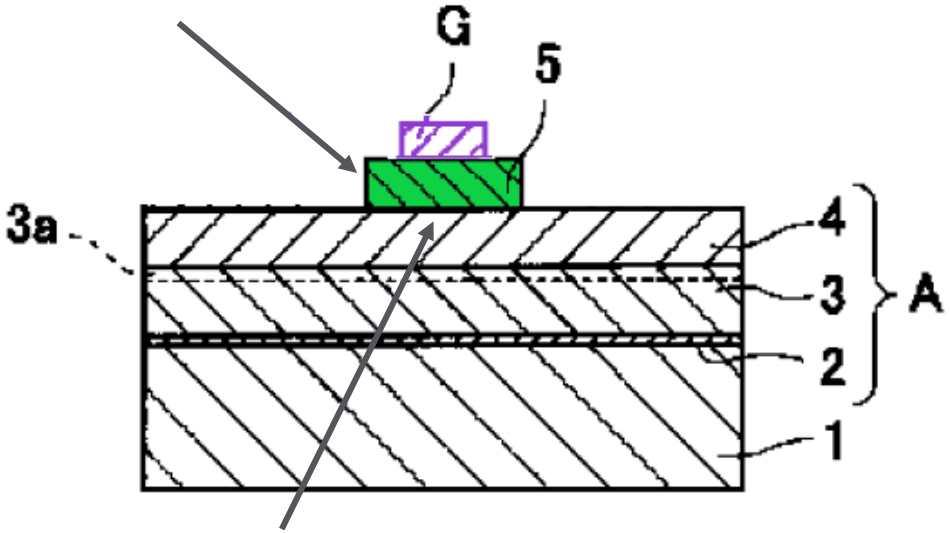
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 19 at 1, 16; Paper 21 at 12-13
’335: Paper 17 at 37-38

Grounds 4 and 5 for ’347 & Ground 6 for ’335
Ledges illustrated in FIG. 1 of Yoshida are by-product of “gate-last” fabrication

Petitioner does not refute that ledges illustrated in FIG. 1 are for later receiving the electrode without overhang and have no function after the gate electrode is loaded

dry etching to etch away the p-type GaN layer “except where the gate electrode was to be loaded”



to form pn junction of the p-type GaN layer 5 “immediately under” the gate electrode G for “voltage control with a small amount of carrier injection”

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

This is consistent with the references that Petitioner cites to show a pair of ledges, where the ledges are common when the base is patterned before the electrode metal is deposited. EX2005 ¶268; EX1011 Fig. 1, ¶[0006] (“processed with two different photomasks”); EX1018 at Fig. 1, Page 1 (“Transistors were then fabricated with… source-drain contacts… Ni/Au contacts were then deposited over the selective area grown *p*-GaN regions.”); EX1017, Figs. 5-6; ¶[0056] (“Referring to FIG. 5, the p-type Al_z GaN cap layer 11 is etched to define a gate region where the p-type Al_zGaN cap 11 is located. Referring to FIG. 6, a gate 17 with a schottky contact… are formed on the Ga-face to form an assembly.”); EX1007 Fig. 1A, 1B, ¶¶[0061]-[0065].

Not refuted by Petitioner

’347: Paper 17 at 57-59 (quoted); Paper 21 at 2, 23
’335: Paper 17 at 69-70 (almost identical); Paper 21 at 25-26

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Petitioner relies on Beach for First Etching Step

Beach

First Etching Step

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

[1d] depositing a p-type gate material on the barrier layer;

[1e] depositing a gate metal on the p-type gate material;

[1f] forming a photoresist over the gate metal;

[1g] etching the gate metal and the p-type gate material,

[1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

[1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

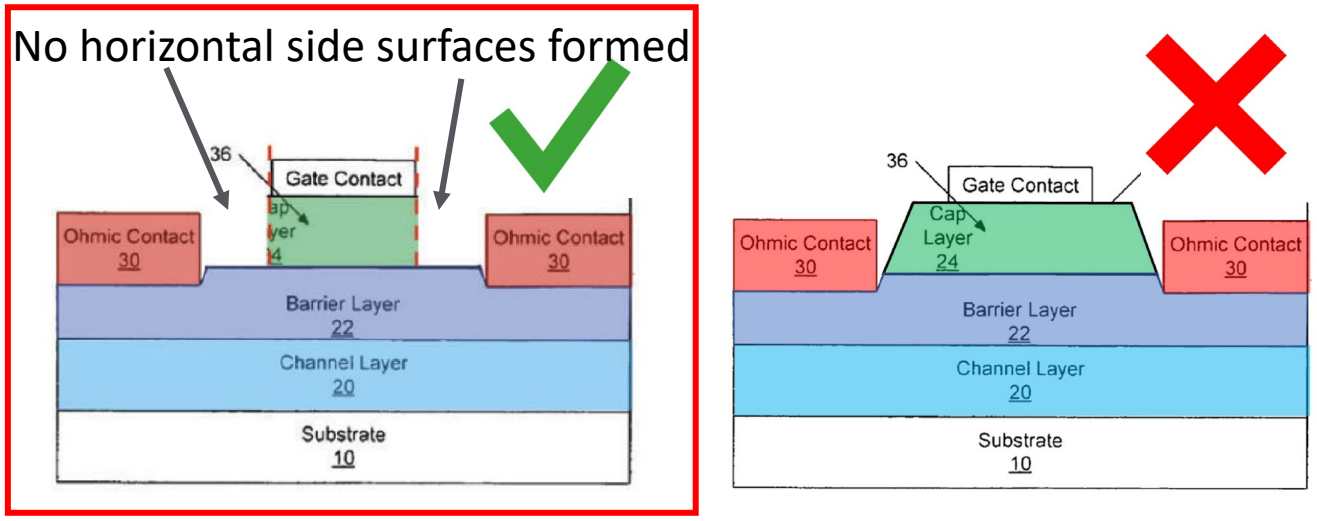
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Beach’s self-alignment would cut off or not form sloped wall

The Petition specifically states:

- “[a] POSITA would have found it obvious ***to make the stacked gate structure of Saxler’s non-recessed embodiments using Beach’s and Shenoy’s methods***.”
- “[i]t would have been obvious ***to create Saxler’s gate structure with Beach’s approach for improved alignment between layers***. It would have been obvious to look to ***Beach for its simple methods of making stacked gate structures***.”

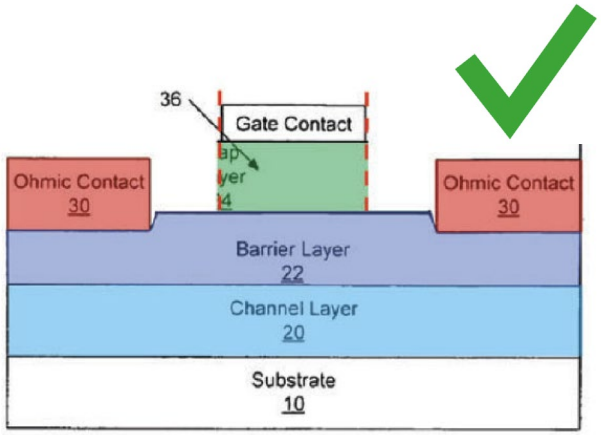
Dr. Schubert establishes that “self-aligned” approaches of Beach (Beach-II and Smith) are for self-aligning ***sidewalls***, and would result in cutting off, or not forming, the horizontally extending “sloped” side surfaces that Petitioner relies on from Fig. 1A of Saxler.



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

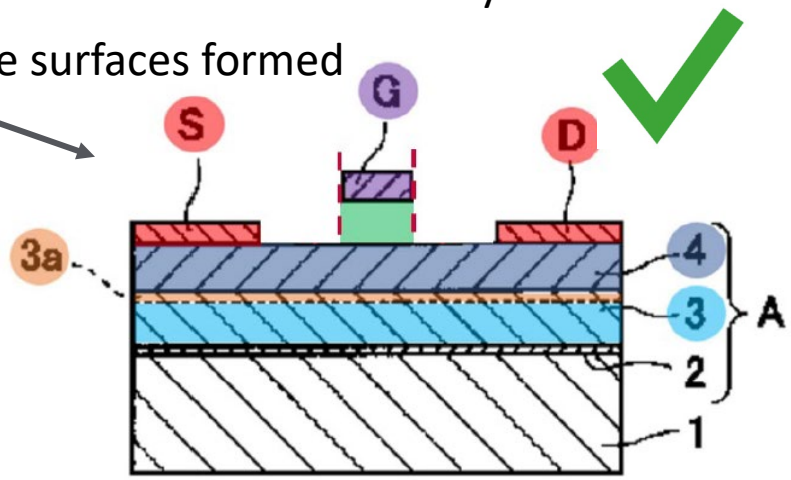
’347: Paper 1 at 31, 34 (quoted); Paper 17 at 38-39; Paper 21 at 13-15
‘335: Paper 1 at 59, 62 (nearly identical); Paper 17 at 48-49; Paper 21 at 17-19

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Beach’s self-alignment would cut off or not form sloped wall

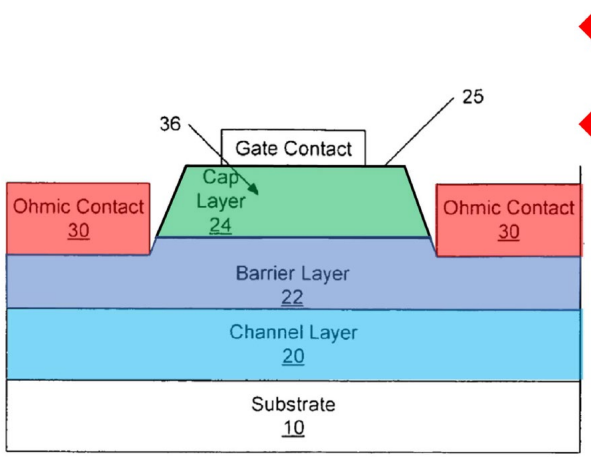


Saxler etched by Beach

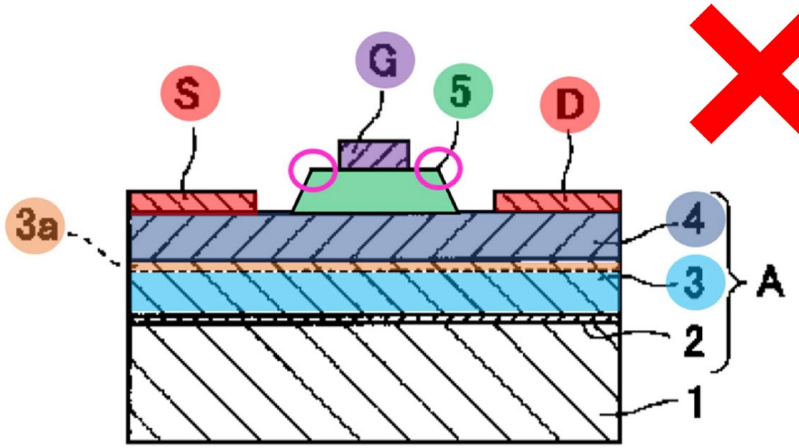
No horizontal side surfaces formed



Yoshida etched by Beach



Petitioner’s Structure in view of Saxler



Petitioner’s Structure in view of Yoshida

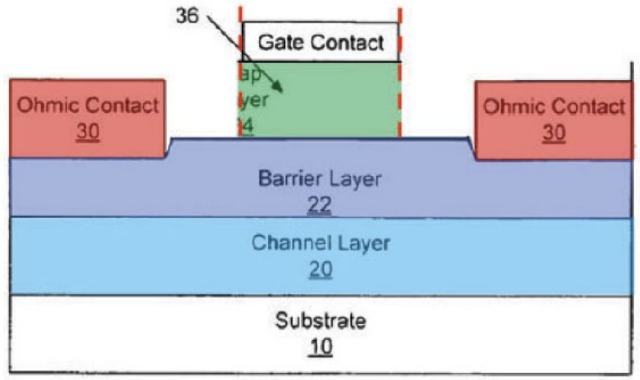
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 1 at 31, 34 (quoted); Paper 17 at 38-39; Paper 21 at 13-15
‘335: Paper 1 at 59, 62 (nearly identical); Paper 17 at 48-49; Paper 21 at 17-19

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Beach’s self-alignment would cut off or not form sloped wall

Recognizing the Petition’s weakness, Petitioner in the Reply proposed a new “combination us[ing] Saxler’s etching technique to create sloped sidewalls when using Beach’s one-mask approach”

- The new argument should not be considered because the combination of the Petition was “to make the stacked gate structure of Saxler’s nonrecessed embodiments using Beach’s and Shenoy’s methods”
- The Petition 1) fails to reference “Saxler’s etching technique” with respect to the modified method and 2) does not provide any suggestion on how “Saxler’s etching technique” would be modified based on Beach and Shenoy
- Petitioner intentionally shifting positions



’347: Paper 19 at 13-14; Paper 21 at 13-15
‘335: Paper 19 at 23; Paper 21 at 17-19

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Petitioner relies on Shenoy for Second Etching Step

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

[1d] depositing a p-type gate material on the barrier layer;

[1e] depositing a gate metal on the p-type gate material;

[1f] forming a photoresist over the gate metal;

[1g] etching the gate metal and the p-type gate material,

Shenoy

[1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

Second Etching Step

[1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Shenoy is purely mathematical and based on underlying insulator

Shenoy is a mathematical model under very controlled conditions (with underlying insulator), a POSA would not look to Shenoy to modify Saxler/Yoshida as modified by Beach.

Model Development

The parameters that characterize the shape evolution during through-mask EMM are (Fig. 1): (*i*) aspect ratio, h/L, (*ii*) spacing to opening ratio, a/L, (*iii*) metal film thickness ratio, b/L, and (*iv*) mask wall angle, β. The aspect ratio, spacing to opening ratio, and the mask wall angle influence the current distribution at the electrode. On the other hand, the metal film thickness ratio determines the extent to which EMM must proceed before the underlying insulator is exposed. The influence of these parameters on the undercut, U, and the etch factor are of interest. The etch factor is defined as the ratio of the maximum etched depth to the undercut, (d/U). Once the insulator is exposed, metal dissolution continues in the lateral direction leading to a change in metal wall angle, χ. Fine line through-mask EMM of metal films on insulator requires minimized undercut (hence increased etch factor), and straight walls. In this investigation, the influence of the mask wall angle, β, on the etch factor has been evaluated.

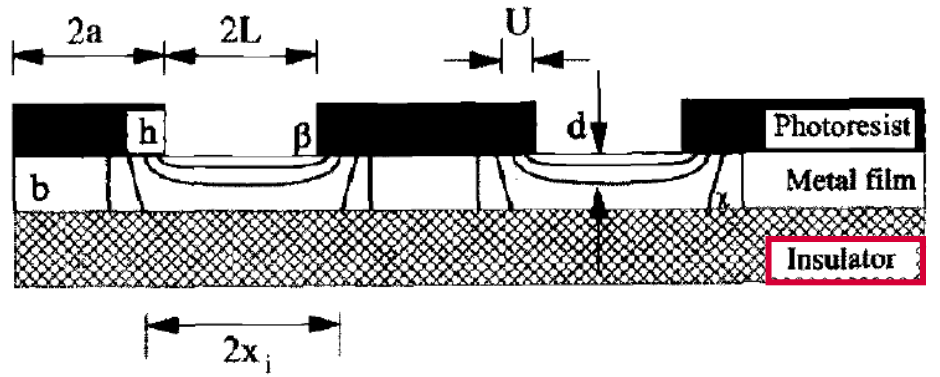


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

’347: Paper 17 at 40-41
’335: Paper 17 at 50-51

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Shenoy is purely mathematical and would etch GaN cap layer

The current distribution at the anode has been combined with Faraday's law to determine the evolution of the metal surface. The rate, r, at which the anodic surface recedes is

$$r = \frac{M\theta}{nF\rho} i \qquad [5]$$

where M is the molecular weight of the metal, n is the metal dissolution valence, ρ is the density of the metal film, F is Faraday's constant, and θ is the current efficiency of metal dissolution which is assumed to be constant at 100%.

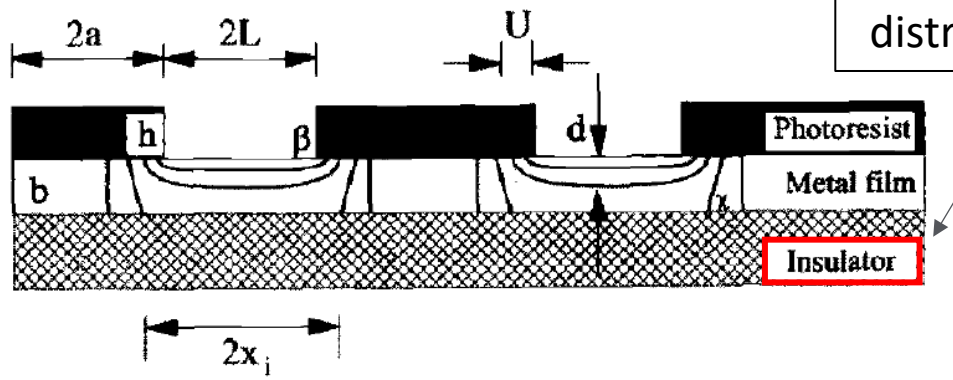
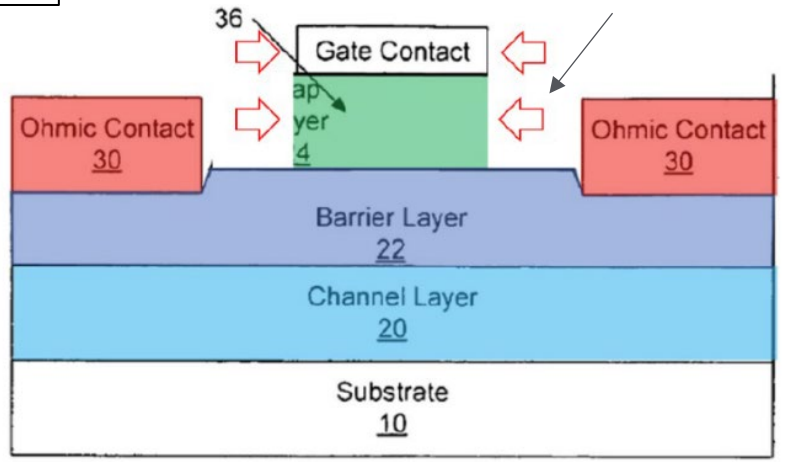


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

Insulator has no current distribution (i), so no etching

GaN has a current distribution (i), so etching would occur

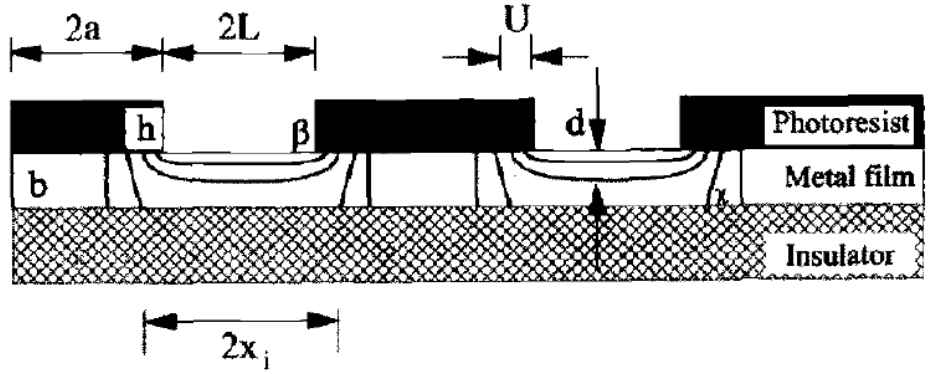


’347: Paper 17 at 42-43
’335: Paper 17 at 52-54

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Shenoy is purely mathematical and would etch GaN cap layer

- Even considering Dr. Shealy’s “holes” theory (EX2004, 98:25-99:13), the surface of the GaN material (red arrows) underlying the Gate Contact would not have been etched by Beach.
- Thus, underlying surface would still have “holes” and not behave as an insulator => Underlying surface of the GaN would be etched by Shenoy and not form the claimed ledges.



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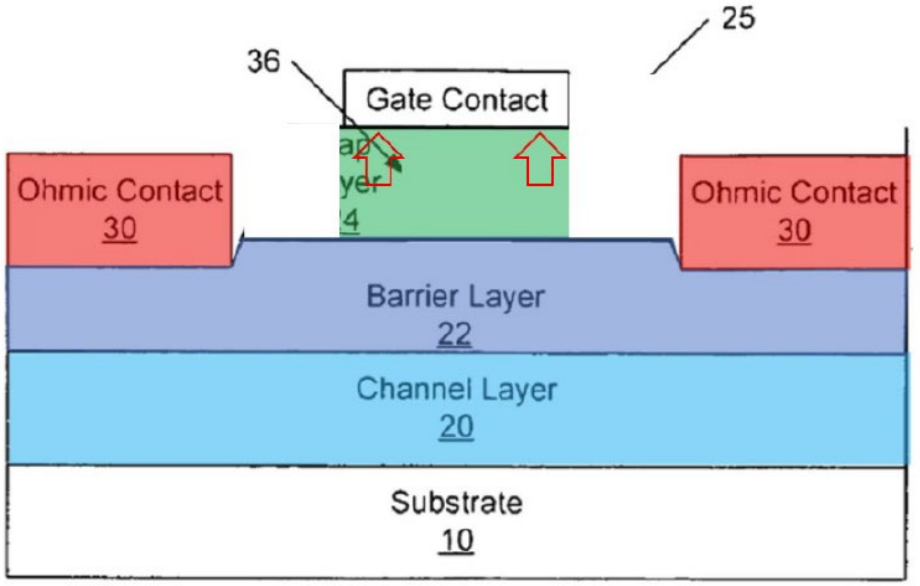

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 43-46; Paper 21 at 16
’335: Paper 17 at 54-56; Paper 21 at 20

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
In the Reply, Petitioner diverts from Shenoy and introduces new conclusory statements

In the Reply, Petitioner introduces arguments on “many wet etches”.

- “Many wet etches” or “liquid metal etches” not relevant to any ground because they are “unlike” Shenoy

Petitioner also relies on general conclusory statements that Shenoy would not etch GaN, which is inconsistent with the record

- Dr. Schubert establishes that Shenoy etching is based on current distribution not “tough[ness] of material”
- Petitioner’s modification based on Shenoy not etching GaN, and not differential rates

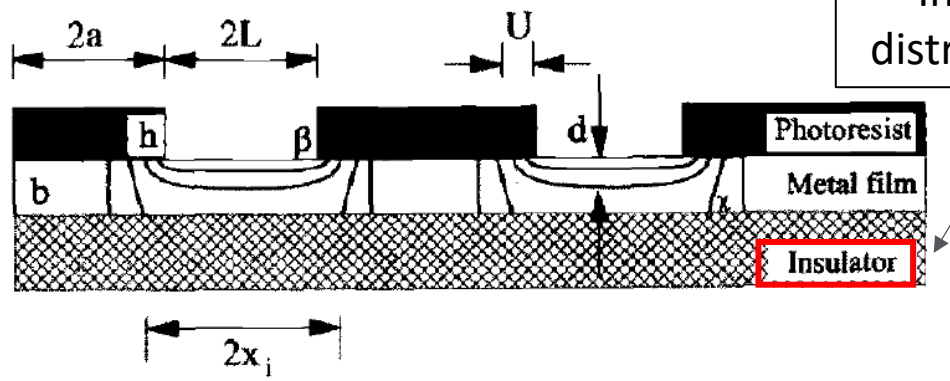

Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

Insulator has no current distribution (i), so no etching

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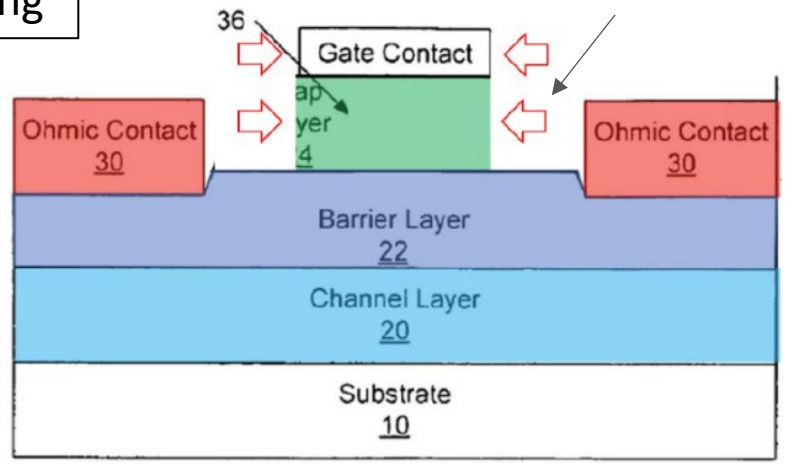
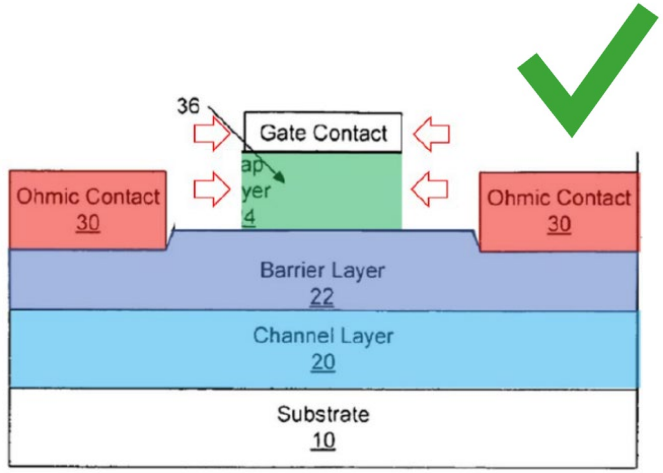


DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

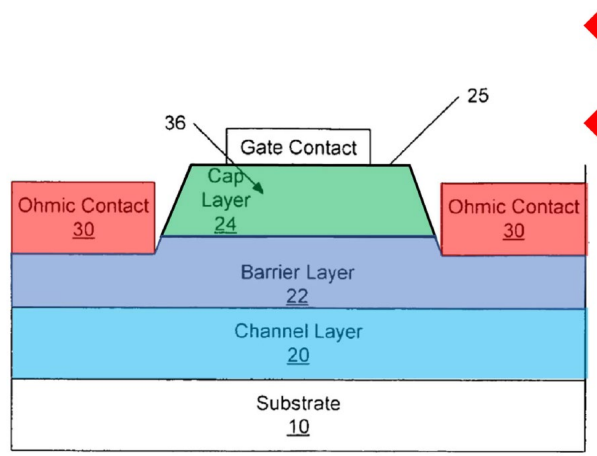
’347: Paper 17 at 41-42; Paper 21 at 15-18
’335: Paper 17 at 54-57; Paper 21 at 19-21

Grounds 1, 2, and 4 of ’347 & Grounds 3 and 6 of ’335
Shenoy is purely mathematical and would etch GaN cap layer

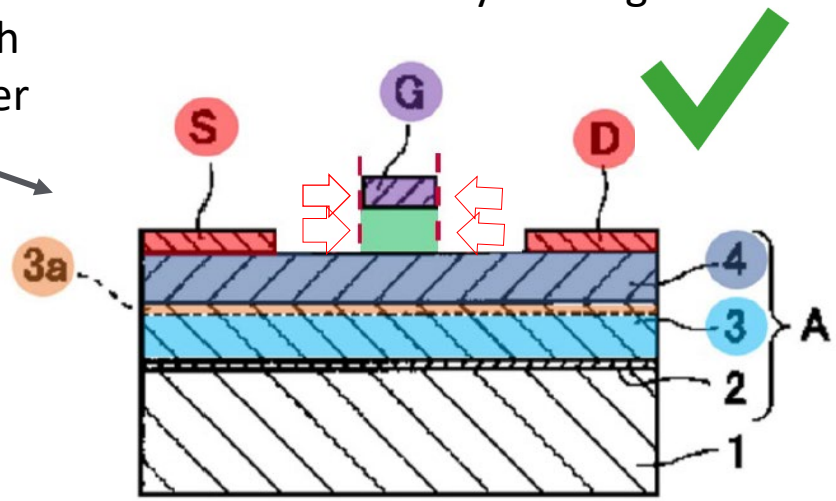
Shenoy would etch both gate metal and GaN layer



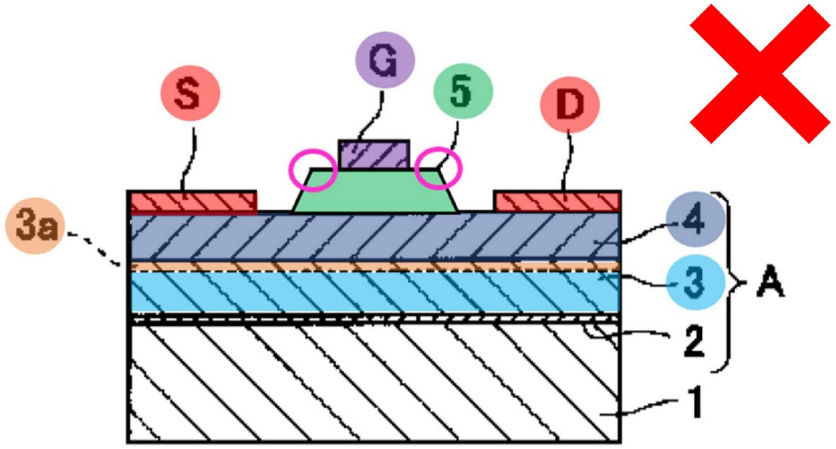
Saxler with Shenoy etching



Petitioner’s Structure in view of Saxler



Yoshida with Shenoy etching



Petitioner’s Structure in view of Yoshida

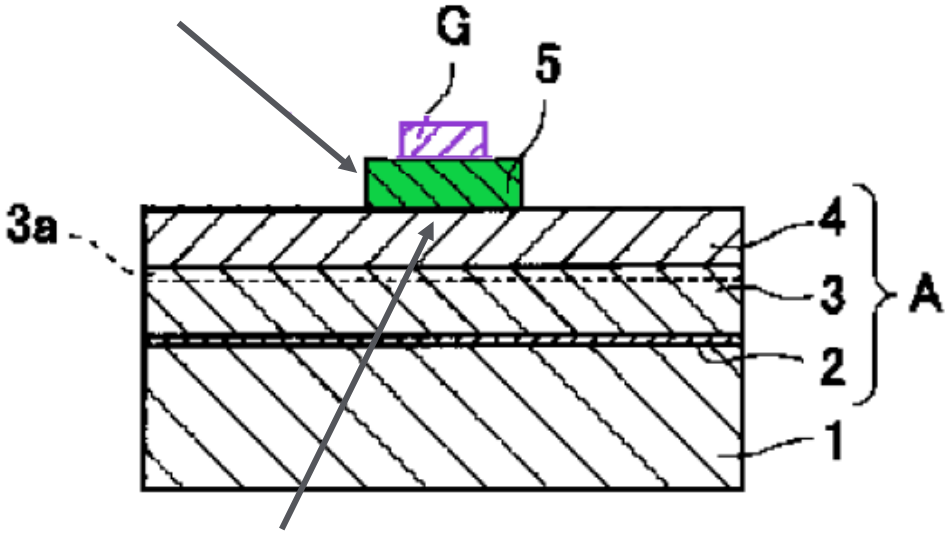
’347: Paper 17 at 42-43
’335: Paper 17 at 52-54

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 4 and 5 for ’347 & Ground 6 for ’335
Ledges illustrated in FIG. 1 of Yoshida are by-product of “gate-last” fabrication

Petitioner does not refute that ledges illustrated in FIG. 1 are for later receiving the electrode without overhang and have no function after the gate electrode is loaded

dry etching to etch away the p-type GaN layer “except where the gate electrode was to be loaded”



to form pn junction of the p-type GaN layer 5 “immediately under” the gate electrode G for “voltage control with a small amount of carrier injection”

This is consistent with the references that Petitioner cites to show a pair of ledges, where the ledges are common when the base is patterned before the electrode metal is deposited. EX2005 ¶268; EX1011 Fig. 1, ¶[0006] (“processed with two different photomasks”); EX1018 at Fig. 1, Page 1 (“Transistors were then fabricated with… source-drain contacts… Ni/Au contacts were then deposited over the selective area grown *p*-GaN regions.”); EX1017, Figs. 5-6; ¶[0056] (“Referring to FIG. 5, the p-type Al_z GaN cap layer 11 is etched to define a gate region where the p-type Al_zGaN cap 11 is located. Referring to FIG. 6, a gate 17 with a schottky contact… are formed on the Ga-face to form an assembly.”); EX1007 Fig. 1A, 1B, ¶¶[0061]-[0065].

Not refuted by Petitioner

’347: Paper 17 at 57-59 (quoted); Paper 21 at 2, 23
’335: Paper 17 at 69-70 (almost identical); Paper 21 at 25-26

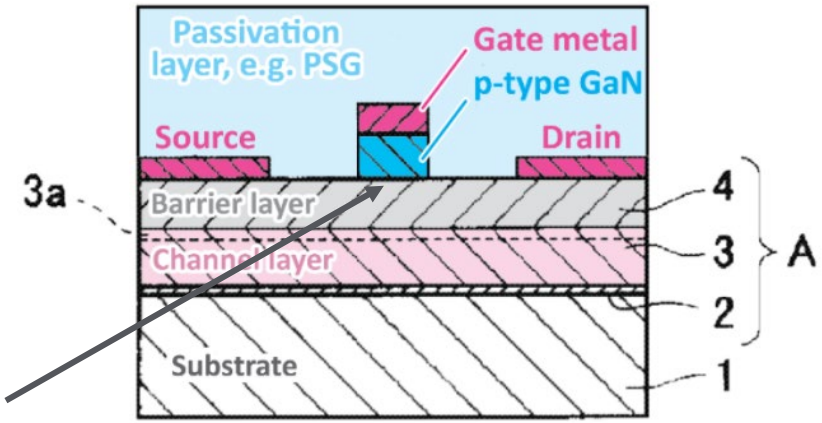
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 4 and 5 for ’347 & Ground 6 for ’335
No Motivation to form Ledges in modified method of fabricating Yoshida

In purely relying on the schematic of FIG. 1 (produced from “gate-last” technique), Petitioner does not provide any “articulated reasoning” for etching ledges after gate metal is layered in proposed method

Additional etching would:

1) form ledges that would have no function because gate electrode is already loaded;
2) would only frustrate Yoshida’s purpose by being detrimental to voltage control by widening PN junction relative to gate metal; and
3) add unnecessary cost of additional etching after gate is already formed (as Petitioner states is undesirable)



After first etching step (e.g. Beach), PN junction of GaN layer 5 would be “immediately under” gate electrode G for “voltage control with a small amount of carrier injection” as required by Yoshida

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 59-61, 67, 69; Paper 21 at 23-25
’335: Paper 17 at 70-72; Paper 21 at 25-27

Ground 4 of ’347
Petitioner attempts to improperly add a new motivation for Ground 4

Petitioner again attempts to introduce a new motivation in the Reply in alleging that it would have been obvious to form ledges to reduce gate leakage

It would have been obvious to modify *Yoshida*’s transistor with the sloped sidewalls of *Saxler*’s capping layer to reduce gate leakage. Shealy, [197]. The combination calls for nothing more than the simple substitution of *Saxler*’s sidewalls to predictably make an enhancement-mode GaN HEMT. *Id.* And a POSITA would have recognized *Saxler*’s sidewalls would have reliably reduced *Yoshida*’s gate leakage, making the combination obvious. *Id.*

Paper 1 at 73-74

A POSITA would have additionally recognized that *Saxler*’s sloped sidewalls would have beneficially reduced *Yoshida*’s leakage losses and found the combination obvious. Shealy, [201]. It was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage. *Id.* (citing *Xu*, 1; *Kanda*, [0013], [0027], [0144], [0157], Fig. 12A).

Paper 1 at 75

Motivation in Petition was to add Saxler’s tapered sidewalls for longer leakage path to reduce gate leakage (not ledges).

Petitioner does not refute that the ledges in prior art are for loading the gate metal in a “gate-last” approach.

’347: Paper 17 at 57-60; Paper 19 at 25; Paper 21 at 22-23

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 3 and 5 of ’347
Petitioner relies on Ahn for the First and Second Etching Steps

Ahn

First Etching Step

Second Etching Step

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

[1d] depositing a p-type gate material on the barrier layer;

[1e] depositing a gate metal on the p-type gate material;

[1f] forming a photoresist over the gate metal;

[1g] etching the gate metal and the p-type gate material,

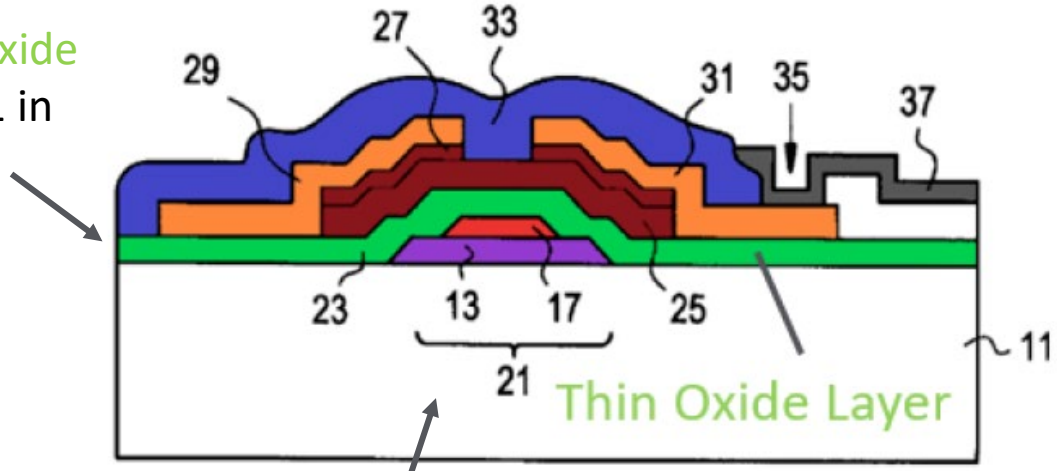
[1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

[1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

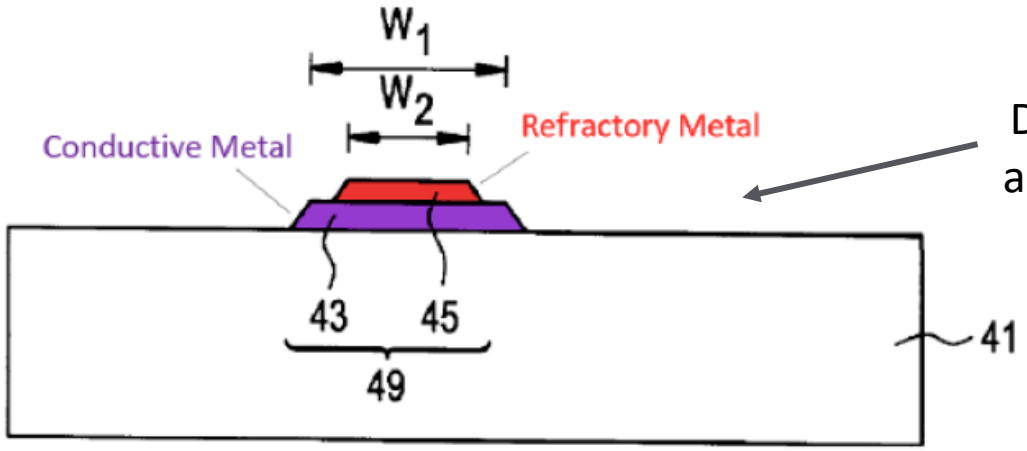
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Grounds 3 and 5 of ’347
Ahn is directed to an unrelated thin film transistor

Thin film transistor characterized by insulating layer 23 (“gate oxide layer”) thinly separating semiconductive layer 25 from gate 21 in vertical arrangement



Deterioration of the thin gate oxide layer 23 may cause an electrical connection between the semiconductive layer 25 and the gate 21 causing short circuit. 1:34-38.



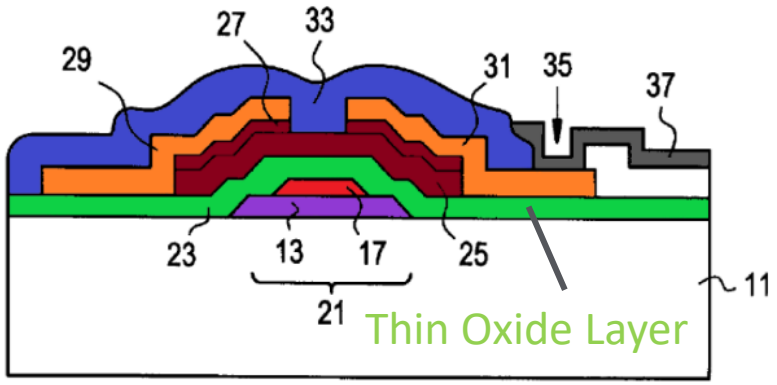
Double-step gate structure (with tapered walls) formed by additional etching to reduce deterioration of overlying thin gate oxide layer 23

Ahn has unrelated structure, function, and fabrication

’347: Paper 17 at 17-21, 53-55

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 3 of ’347
A POSA would not look to the method/resultant structure of Ahn to modify Saxler



Thin-Film Transistor of Ahn

Ahn performs additional etching to form double step gate structure to prevent deterioration of thin gate oxide layer 23 that may cause an electrical connection between the semiconductive layer 25 and the gate 21 causing short circuit.

1) Petitioner lacks basis for its relied-on transistor structure (not disclosed and no motivation to modify provided in Petition)

2) Saxler does not disclose central gate structure contrary to Ahn

“aligned to the source-side sidewall 27 of the gate electrode 26” [0041]

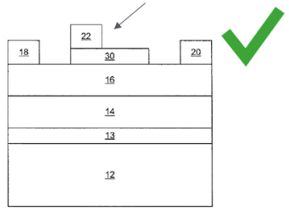


Figure 4C

“substantially aligned” [0041]

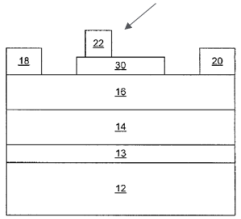
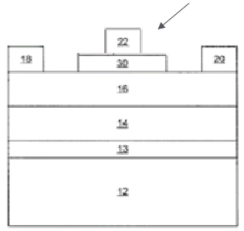


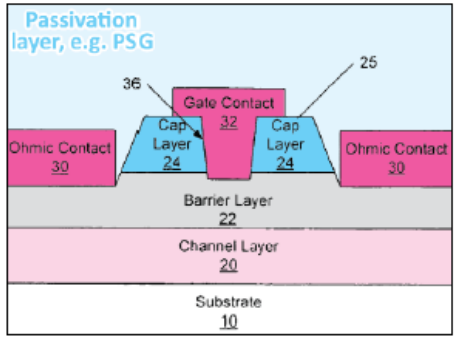
Figure 5B

“severe misalignment may be detrimental to the device” [0041]



Innoscience: “would obviously lead to manufacturing defects” (Reply 1, 16)

3) Saxler’s passivation layer is much thicker than in thin film transistor and not vertically separating ohmic contacts, thus no concern for deterioration

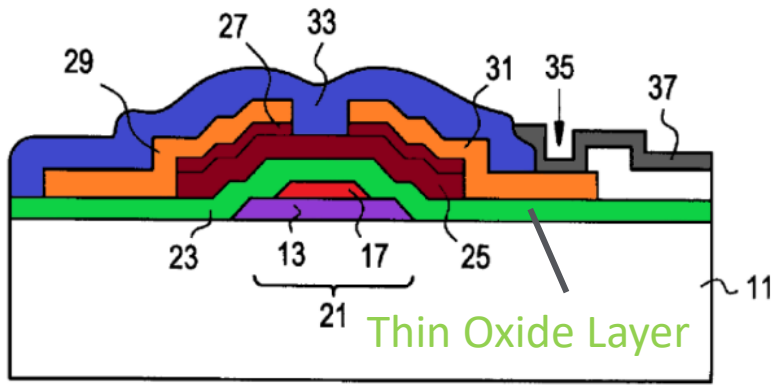


DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 34-37, 52-55; Paper 21 at 18-19

Ground 5 of ’347
A POSA would not look to the method/resultant structure of Ahn to modify Yoshida

Petitioner’s vague motivation of “improve[] performance and prevent[] deterioration” in view of Ahn has no applicability to Yoshida.



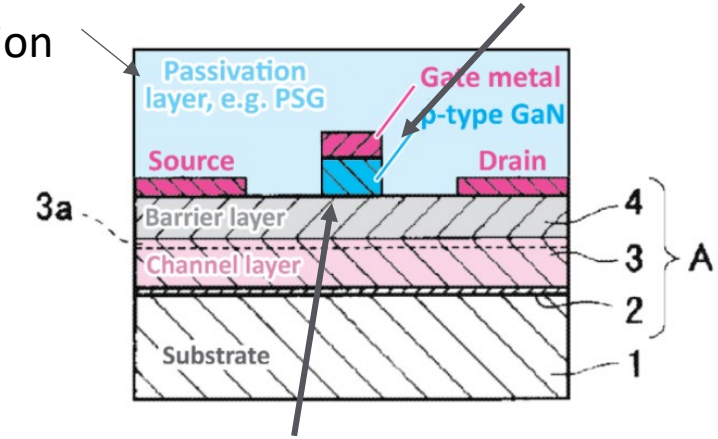
Thin-Film Transistor of Ahn

Ahn performs additional etching to form double step gate structure to prevent deterioration of thin gate oxide layer 23 that may cause an electrical connection between the semiconductive layer 25 and the gate 21 causing short circuit.

2) Passivation layer much thicker than thin film transistor and not vertically separating conductive layer, thus no concern for deterioration

3) Second etching step a) adds steps and manufacturing cost and b) increases voltage demand, by etching ledges

Yoshida



1) After first etching step (e.g., Beach), PN junction of GaN layer 5 is “immediately under” gate electrode G for “voltage control with a small amount of carrier injection” as required by Yoshida

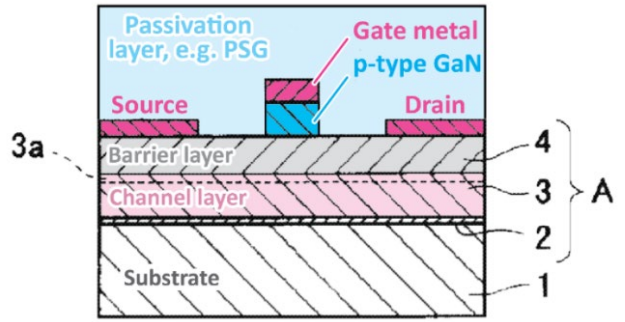
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

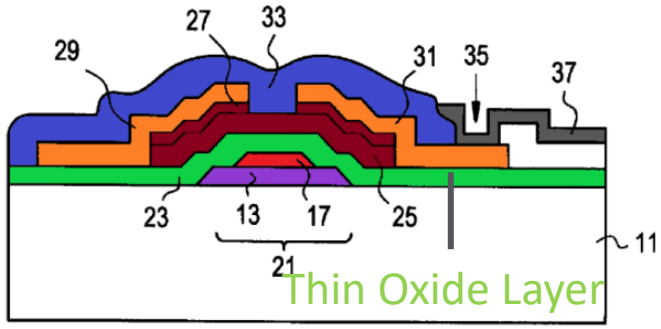
’347: Paper 1 at 95; Paper 17 at 59-61, 66-69; Paper 21 at 23-27

Ground 5 of ’347
A POSA would not look to the method/resultant structure of Ahn to modify Yoshida

In the Reply, Petitioner again improperly attempts to introduce a new motivation in a conclusory statement of “form[ing] the same gate structure as Yoshida more efficiently and with sloped side walls on the gate layers”

- Petitioner still does not address the substantial structural and functional divergences from Yoshida and Ahn
- Petitioner relies on conclusory statements such as it “would work” and same field of endeavor, <u>without providing any motivation</u> for modifying Yoshida with Ahn’s gate structure
- Adding unecessary etching steps to produces ledges would necessarily <u>not</u> be “more efficient[]” and would be undesirable
- Patent Owner establishes why a POSA would not form sloped side walls on Yoshida, and Petitioner fails to provide any evidence otherwise





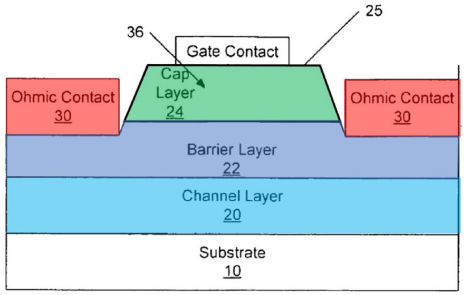
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 17 at 63-69; Paper 19 at 26-28; Paper 21 at 20-22, 25-27

Grounds 3 & 5 of ’347
Petitioner’s conclusory statement of Differential Etching Rates

Petitioner makes a conclusory statement that Ahn’s differential etching rates would also be applicable to Saxler/Yoshida to create the specific structure that they are relying on

- Ahn specifically discloses that the etching is successful in forming the double step structure “**because of the etching material and metals used for the first and second metal layers of the gate**”
  - where the first metal layer 43 is a conductive metal (Al, Cu, or Au), the second metal layer 45 is a refractory metal (Mo, Ta, or Co), and the etching material is a mixture of phosphoric acid H3 PO4, acetic acid CH3 COOH and nitric acid HNO3
- “**the etching material and metals** used for the **first and second metal layers** of the gate” of Ahn has no relation to the method and metal/GaN gate structure of Yoshida
- Petitioner’s conclusory statement provides no support for the complex interactions of any known etching material with each of the specific p-type doped semiconductor of the gate material and the specific metals of the gate contact of Yoshida and Saxler



’347: Paper 1 at 98-99; Paper 17 at 69-70

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ground 5 of ’347
Petitioner’s Inconsistency on Yoshida further highlights hindsight

Petitioner takes contradictory positions in stating that Yoshida’s gate structure is “symmetric” in Ground 4 of ’335 but attempts to modify Yoshida’s gate structure “to improve alignment and symmetry” in Ground 5 of ’347

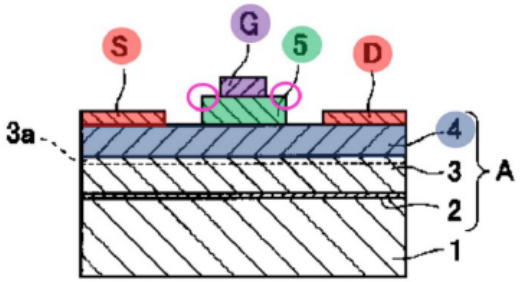
Petitioner’s Invalidity Position for U.S. Pat. 9,748,347

Furthermore, Petitioner attempts to rely on the motivation of modifying Yoshida in order “to improve alignment and precision” (Pet. 98) and “to improve alignment and symmetry between layers” (Pet. 99).

- No need to “improve… symmetry” when gate structure is already “symmetric”
- Perfect illustration of hindsight that Petitioner relies on throughout Petitions

Petitioner’s Invalidity Position for U.S. Pat. 10,312,335

Petitioner alleges that “Yoshida’s gate electrode is narrower than layer 5, thereby exposing horizontal ledges that extend past the respective sidewalls of the gate electrode and toward the source and drain. Yoshida, [0022]-[0023], Fig. 1; Shealy, [214]. **These ledges are symmetric on either side of the gate metal** (i.e., having substantially equal widths). Yoshida, Fig. 1; Shealy, [214]. Yoshida thus discloses this element (Ground 4).” EX2007 83.



EX2007 83 (annotating EX1006, Fig. 1)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

’347: Paper 1 at 98-99; Paper 17 at 65-66; Paper 21 at 27-28
’335: Paper 1 at 83