

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,  
AND  
INNOSCIENCE AMERICA, INC.  
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,  
Patent Owner.

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IPR2023-01384  
Patent 10,312,335 B2

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Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and  
KIMBERLY McGRAW, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

JUDGMENT  
Final Written Decision  
Determining All Challenged Claims Unpatentable  
*35 U.S.C. § 318(a)*

## I. INTRODUCTION

### A. *Background and Summary*

Innoscence (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc., (collectively “Petitioner”) filed a Petition for an *inter partes* review (Paper 1 (“Pet.”)) challenging claims 1–7 of U.S. Patent No. 10,312,335 B2 (Ex. 1001 (“the ’335 patent”)). Efficient Power Conversion Corporation (“Patent Owner”) filed a Preliminary Response. Paper 7. After receiving authorization from the Board, Petitioner filed a Preliminary Reply to the Preliminary Response (Paper 8) and Patent Owner filed a Preliminary Sur-reply (Paper 10).

On March 26, 2024, we instituted an *inter partes* review of all of the challenged claims based on all of the grounds identified in the Petition. Paper 11 (“Inst. Dec.” or “Institution Decision”). Patent Owner filed a Response to the Petition (Paper 17, “PO Resp.”), Petitioner filed a Reply (Paper 19, “Reply”), and Patent Owner filed a Sur-reply (Paper 21, “Sur-reply”). We held an oral hearing for this proceeding on January 7, 2025, and a transcript of the hearing has been entered into the record. Paper 30 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). Based on the record before us, we conclude that Petitioner has shown by a preponderance of the evidence that claims 1–7 of the ’335 patent are unpatentable.

### B. *Real Parties-in-Interest*

Petitioner identifies Innoscience (Zhuhai) Technology Company, Ltd., Innoscience America, Inc., and Innoscience (Shuzou) Technology Company, Ltd. as real parties-in-interest. Pet. 98. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1–2.

C. *Related Matters*

The parties identify two matters involving the '335 patent: *Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd*, 2:23-cv-04026-AB-AS (C.D. Cal. May 24, 2023) and *Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same*, Inv. No. 337-TA-1366 (USITC May 26, 2023). Pet. 99; Paper 5, 2.

D. *The '335 Patent (Ex. 1001)*

The '335 patent, titled “Gate with Self-aligned Ledge for Enhancement Mode GaN Transistors,” issued June 4, 2019, and is directed to “[a]n enhancement-mode GaN transistor with reduced gate leakage current between a gate contact and a [two-dimensional electron gas (2DEG)] region and a method for manufacturing the same.” Ex. 1001, codes (45), (54), (57), 1:47–48.

The '335 patent explains that “GaN semiconductor devices are increasingly desirable because of their ability to switch at high frequency, to carry large current, and to support high voltages.” Ex. 1001, 1:30–32. Devices developed for high power/high frequency applications are based on structures that exhibit high electron mobility and are referred to as, *inter alia*, high electron mobility transistors (HEMT). Ex. 1001, 1:32–39. GaN HEMT devices typically include a nitride semiconductor with at least two nitride layers. Ex. 1001, 1:42–43. Different materials (e.g., AlGaN and GaN) on the semiconductor cause adjacent layers to have different band gaps and also cause polarization, which contributes to a conductive 2DEG region near the junction of the two layers, and allows charge to flow through the device. Ex. 1001, 1:43–53.

The '335 patent further explains that:

Because the 2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices. If the 2DEG region is depleted (i.e., removed ) below the gate at zero applied gate bias, the device can be an enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide and because they are easier to control with simple, low cost drive circuits. An enhancement mode device requires a positive bias applied at the gate in order to conduct current.

Ex. 1001, 1:54–63.

Figure 2 of the '335 patent, reproduced below, depicts a prior art enhancement-mode GaN transistor.

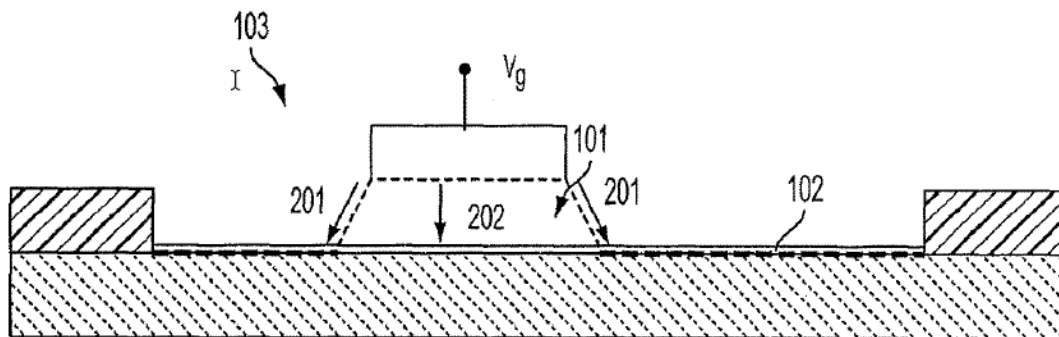


FIG. 2  
PRIOR ART

Figure 2 depicts a conventional enhancement-mode GaN transistor having gate 103 comprising p-type material 101, and a 2DEG region 102 under gate 103, with two gate leakage current paths 201 and 202. Ex. 1001, 1:64–2:8. According to the '335 patent, the gate leakage current is predominantly along gate edge path 201. Ex. 1001, 2:20–26.

The '335 patent depicts an embodiment of the claimed invention in Figure 5, reproduced below.

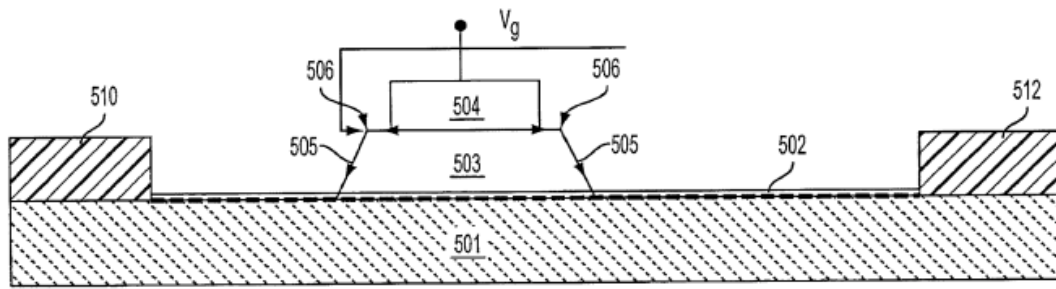


FIG. 5

Figure 5 shows a schematic diagram of a transistor device including GaN base layer 501, barrier layer 502, source metal 510, drain metal 512, p-type gate material 503, gate metal 504, and horizontal ledges 506 on each side of gate metal 504. Ex. 1001, 3:37–59. The '335 patent states that ledges 506 “have equal or substantially equal widths, i.e., the respective ledges are symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material, which is due to the self-aligned manufacturing process.” Ex. 1001, 3:59–64.

Figure 5 also includes arrows showing gate current path 505 that travels horizontally along the ledges 506 and then follows the diagonal path along the edge of p-type gate material 503. Ex. 1001, 4:6–11. According to the '335 patent, this structure results in reduced gate leakage current compared to conventional gates without ledges. Ex. 1001, 4:12–13, 4:47–51, Fig. 8.

The '335 patent also describes an exemplary manufacturing process for forming a gate with self-aligned ledges and depicts the steps in Figures 6A–6C, reproduced below. Ex. 1001, 4:14–35, Figs. 6A–6C.

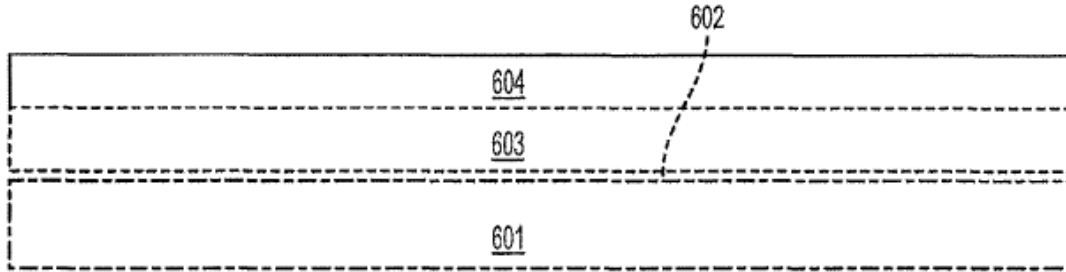


FIG. 6A

Figure 6A shows forming AlGaN barrier layer 602 on GaN base layer 601, forming a layer of p-type gate material 603 on barrier layer 602, and depositing gate metal 604 on p-type gate material 603. Ex. 1001, 4:14–22.

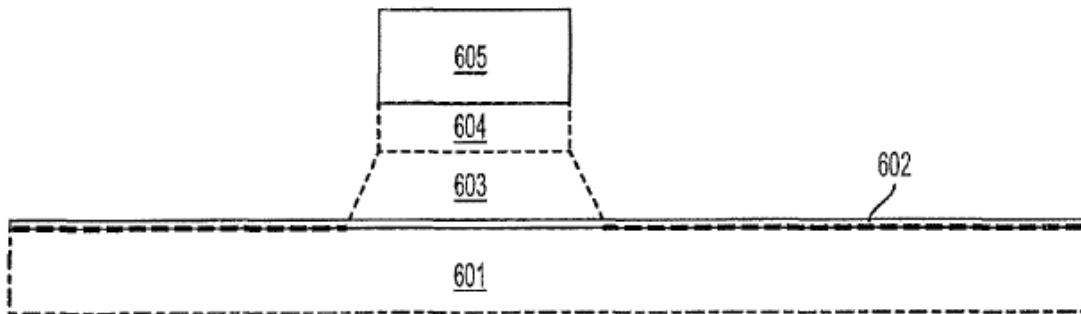


FIG. 6B

Figure 6B shows photoresist layer 605 deposited on gate metal 604, and the resulting structure after gate metal 604 and p-type gate material 603 are etched. Ex. 1001, 4:23–26.

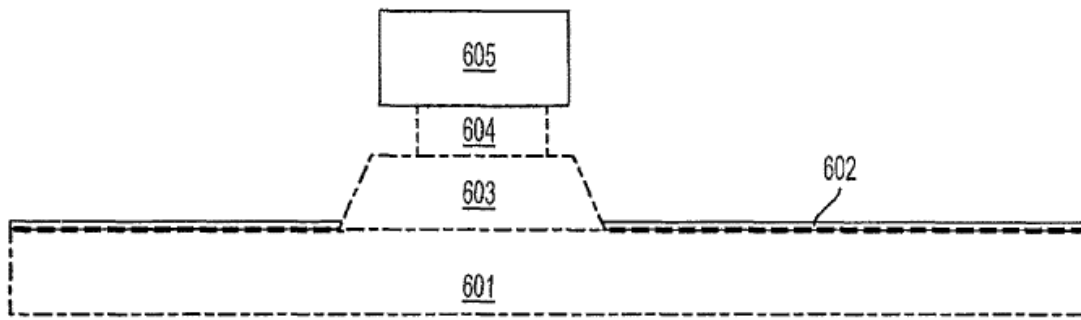


FIG. 6C

Figure 6C shows the resulting structure after gate metal 604 is etched isotropically such that gate metal 604 has a width less than the planar upper surface of p-type gate material 603. Ex. 1001, 4:26–29. According to the '335 patent, “[t]his second etching step results in the formation of the ledges 506 of the p-type gate material 603.” Ex. 1001, 4:29–31. Photoresist 605 is then removed, resulting in the gate with self-aligned ledges shown in Figure 5. Ex. 1001, 4:32–34.

The '335 patent states that the self-aligned process illustrated in Figures 6A–6C is “vastly superior to forming gate ledges using separate masks” due to the possibility of misalignment between the gate metal and p-type gate material when using a two-mask process. Ex. 1001, 4:52–63.

#### *E. Illustrative Claims*

Of the challenged claims, claims 1 and 5 are independent claims, and are reproduced below.

Claim 1:

[1p] An enhancement-mode GaN transistor, comprising:

[1a] a GaN layer;

[1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[1c] a source contact and a drain contact formed on the barrier layer;

[1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and

[1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

[1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

Ex. 1001, 5:5–25 (labels added to correspond with Petitioner’s designation of claim limitations (Pet. Claim Appendix)).

Claim 5:

[5p] An enhancement-mode GaN transistor, comprising:

[5a] a GaN layer;

[5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[5c] a source contact and a drain contact disposed on the barrier layer;

[5d] a p-type gate material formed above the barrier layer and between the source and drain contacts;

[5e] and a gate metal disposed on the p-type gate material,



[5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

[5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

Ex. 1001, 6:6–23 (minor formatting and labels added to correspond with Petitioner’s designation of claim limitations (Pet. Claim Appendix)).

### *F. Unpatentability Challenges*

Petitioner presents the following challenges in the Petition:

<b>Claims Challenged</b>	<b>35 U.S.C. §<sup>1</sup></b>	<b>Reference(s)/Basis</b>
1–7	103	Saxler <sup>2</sup>
1–7	103	Saxler, Yoshida <sup>3</sup>
2, 5–7	103	Saxler, Yoshida, Beach, <sup>4</sup> Shenoy <sup>5</sup>
1–7	103	Yoshida
1–7	103	Yoshida, Saxler
2, 5–7	103	Yoshida, Saxler, Beach, Shenoy

<sup>1</sup> The relevant sections of the Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. Because the ’335 patent has an effective filing date prior to the effective date of the applicable AIA amendments, the pre-AIA version of § 103 applies.

<sup>2</sup> US 2006/0108606 A1, published May 25, 2006 (Ex. 1007).

<sup>3</sup> JP H11-261053, published Sept. 24, 1999 (Ex. 1005 (original language); Ex. 1006 (certified English translation)).

<sup>4</sup> US 2007/0007547 A1, published Jan. 11, 2007 (Ex. 1008).

<sup>5</sup> R.V. Shenoy, et. al, *Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining*, J. ELECTROCHEM. SOC., Vol. 143, No. 2, 544, Feb. 1996 (Ex. 1009).

Petitioner relies on the declaration of James Richard Shealy, Ph.D. (Ex. 1003). Patent Owner deposed Dr. Shealy and filed a transcript of the deposition as Exhibit 2004 in this proceeding.

Patent Owner relies on the declaration of E. Fred Schubert, Ph.D. Ex. 2005.

## II. ANALYSIS

### A. *Applicable Law*

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (2012) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art;

(3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.<sup>6</sup> *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). “This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *KSR*, 550 U.S. at 418–19.

On the other hand, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). However, a petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, a petitioner must articulate a reason why a person of ordinary skill in the art would have combined or modified the prior art references. *In re NuVasive, Inc.*, 842 F.3d 1376, 1382 (Fed. Cir. 2016); *see also Metalcraft of Mayville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1366 (Fed. Cir. 2017) (“In determining whether there would have been a motivation to combine prior art references to arrive at the claimed invention, it is insufficient to simply conclude the combination would have been obvious without identifying any reason why a person of skill in the art would

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<sup>6</sup> The parties have not asserted or otherwise directed our attention to any objective evidence of non-obviousness.

have made the combination.”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”) (citing *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014)).

We analyze the challenges presented in the Petition in accordance with the above-stated principles.

*B. Level of Ordinary Skill in the Art*

Petitioner asserts that a person of ordinary skill in the art would have had “at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field, and at least two years of experience in semiconductor device design and/or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies.” Pet. 18 (citing Ex. 1003 ¶¶ 52–53). Petitioner also contends that “[a]dditional education could substitute for professional experience and vice versa.” Pet. 18.

Patent Owner contends that a person of ordinary skill in the art would have had “at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN,” and that “[r]elevant graduate education could substitute for the professional work experience.” PO Resp. 8–9 (citing Ex. 2005 ¶ 20).

Patent Owner further contends that the difference between Petitioner’s and Patent Owner’s proposals regarding a person of ordinary skill in the art

“would not affect the outcome of this proceeding or change [Dr. Schubert’s] opinion in any material manner.” PO Resp. 9 (citing Ex. 2005 ¶ 20).

Petitioner agrees that “the differences [on the level of ordinary skill] do not impact the analysis.” Reply 1.

In light of the record before us, we determine that we do not need to reach a specific finding regarding the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown”) (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

### C. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b). Under *Phillips*, claim terms are afforded “their ordinary and customary meaning.” *Phillips*, 415 F.3d at 1312. “[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

In the Petition, Petitioner argues that the Board should construe two claim terms: (1) “side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer,” recited in claims 1 and 5 (the “side surfaces” limitation), and (2) “self-aligned,” recited in claims 2 and 5. Pet. 18–24.

1. “side surfaces”

Petitioner contends that we should construe the “side surfaces” limitation to mean “side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer.” Pet. 19.

In the Institution Decision, we declined to adopt Petitioner’s proposed construction of the “side surfaces” limitation and determined that it was not necessary to further construe this term because “[t]he parties do not dispute that the language ‘side surfaces extending horizontally’ encompasses a gate material with sloped side surfaces as depicted in Figure 5 of the ’335 patent.” Inst. Dec. 11–16 (citing *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”)). We invited the parties to address this limitation further during the course of this trial, but neither party provided additional evidence or argument regarding the “side surfaces” limitation. Inst. Dec. 16; *see generally* PO Resp.; Reply; Sur-reply. Accordingly, we maintain our determination from the Institution Decision that we do not need to construe the “side surfaces” limitation. Inst. Dec. 15–16.

2. “self-aligned”

Claims 2 and 5 recite horizontal ledges that are “self-aligned.” Ex. 1001, 5:26–28 (claim 2), 6:18–19 (claim 5). According to Petitioner, “[i]n the ’335 patent, a ‘self-aligned’ ledge refers to a process for making the claimed gate structure and does not describe the structure itself.” Pet. 23

(citing Ex. 1001, 3:49–53 (referring to “ledges 506 that are created by a self-aligned process”), 3:65–4:39 (referring to a “self-aligned manufacturing process”)). As a result, Petitioner argues that claims 2 and 5 recite product-by-process steps in a device claim, which lend no patentable weight. Pet. 24 (quoting and citing *In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985) (“If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.”); citing *United Therapeutics Corp. v. Liquidia Techs., Inc.*, 74 F.4th 1360, 1373 (Fed. Cir. 2023) (“As these claims are product claims, they are anticipated by a disclosure of the same product irrespective of the processes by which they are made.”)). Although not presented in its section titled “Claim Construction” (PO Resp. 7–8), Patent Owner disagrees that “self-aligned ledges” constitutes a product-by-process limitation. PO Resp. 38–44; Sur-reply 9.

The law on product-by-process claims is well-established. “In determining validity of a product-by-process claim, the focus is on the product and not the process of making it.” *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1369 (Fed. Cir. 2009). “That is because of the already described, long-standing rule that an old product is not patentable even if it is made by a new process. As a result, a product-by-process claim can be anticipated by a prior art product that does not adhere to the claim’s process limitation.” *Id.* at 1370 (internal footnote omitted). The Federal Circuit has noted an exception to this general rule, stating that “[a]s we recognized in *Amgen*, if the process by which a product is made imparts ‘structural and functional differences’ distinguishing the claimed product from the prior art, then those differences ‘are relevant as evidence of no anticipation’ although they ‘are not explicitly part of the claim.’” *Greenliant*

*Sys., Inc. v. Xicor LLC*, 692 F.3d 1261, 1268 (Fed. Cir. 2012). Accordingly, we consider whether there are structural or functional differences between a product made by a self-aligned process and a product made using a different process.

Patent Owner contends that “the structural features imparted by the self-aligned process allows ledges to be created that are ‘substantially symmetric’ with respect to the gate metal disposed on the p-type material.” PO Resp. 38–39 (quoting Ex. 1001, 3:65–4:3). Patent Owner explains that the self-aligned process described in the ’335 patent uses a single photo mask to pattern and etch the gate metal and underlying gate material such that they are automatically aligned with one another. PO Resp. 39–40 (citing Ex. 1001, 4:14–34).

Patent Owner contends that “the ‘335 patent does **not** indicate that at least one other method can produce transistors that are ‘substantially symmetric’ within the meaning of the ‘335 patent.” PO Resp. 39 (quoting Ex. 1001, 3:65–4:3); *see also* PO Resp. 42–43 (arguing that a gate structure with ledges having substantially equal widths is “**not achievable**” without using a single photo-mask process). According to Patent Owner, the process for forming gate ledges using separate masks cannot produce ledges that are “substantially symmetric” because of “the misalignment that naturally results from a two-mask process.” PO Resp. 39 (citing Ex. 2005 ¶ 50); *see also* PO Resp. 40 (Patent Owner contending that “naturally there is some alignment error when using two photo masks,” and that a “second alignment generally results in misalignment”). Patent Owner and Dr. Schubert provide “graphical representations” to “illustrate the differences between a self-aligning process/self-aligned structure versus a two photo-mask process,



which cannot result in ledges having ‘substantially equal widths’ because of inevitable misalignment.” PO Resp. 41–43 (citing Ex. 2005 ¶ 50).

Petitioner argues that “the patent states that a two-mask process may result in ‘the possibility of misalignment,’” which means “the two-mask process may also result in alignment.” Reply 20 (quoting Ex. 1001, 4:52–63 (emphasis omitted)). Petitioner argues that Dr. Shealy provided unrebutted testimony that supports its position (Reply 21 (quoting Ex. 2004, 54:3–7)), and that Dr. Schubert’s testimony contradicting the patent should be given no weight. Reply 20–21 (citing Ex. 2004, 57:3–7; Ex. 2005 ¶¶ 48–52). Petitioner also argues that claim differentiation shows other methods besides the self-aligned method can create symmetrical ledges because claim 2 recited “self-aligned” ledges whereas claim 1 recites “substantially equal” ledges without requiring a self-aligned process. Reply 20 (citing *Phillips*, 415 F.3d at 1314–15).

We find Petitioner’s arguments to be persuasive.

The ’335 patent discusses two processes for forming gate ledges, a self-aligned process and a process using separate masks (i.e., a two-mask process). Ex. 1001, 4:14–39, 4:54–60. Consistent with Patent Owner’s argument, the ’335 patent states that the self-aligned process creates ledges that “are symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material.” Ex. 1001, 3:59–4:3; PO Resp. 38–39 (“[T]he structural features imparted by the self-aligned process allows ledges to be created that are ‘substantially symmetric’ with respect to the gate metal disposed on the p-type material.”). As for the two-mask process, the ’335 patent states that “[o]ne significant disadvantage of this two mask process is the possibility of misalignment between the gate metal and the p-type gate material.” Ex. 1001, 4:60–63.

On its face, this language indicates only that misalignment between the gate metal and p-type material is possible when using a two-mask process. It does not indicate that a two-mask process will “naturally result” in misalignment, as Patent Owner suggests. PO Resp. 39. Accordingly, we agree with Petitioner that this language suggests only that “the two-mask process may also result in alignment.” Reply 20. This is consistent with testimony Dr. Shealy provided during his deposition regarding centering a gate contact without the use of a self-aligned process:

Q. Do you expect the gate contact of Figure~1A [of Saxler] to be centered, as depicted?

A. There are -- without self-alignment, it’s certainly possible to use lithographic techniques to place that in the center, yes.

Ex. 2004, 57:3–7.

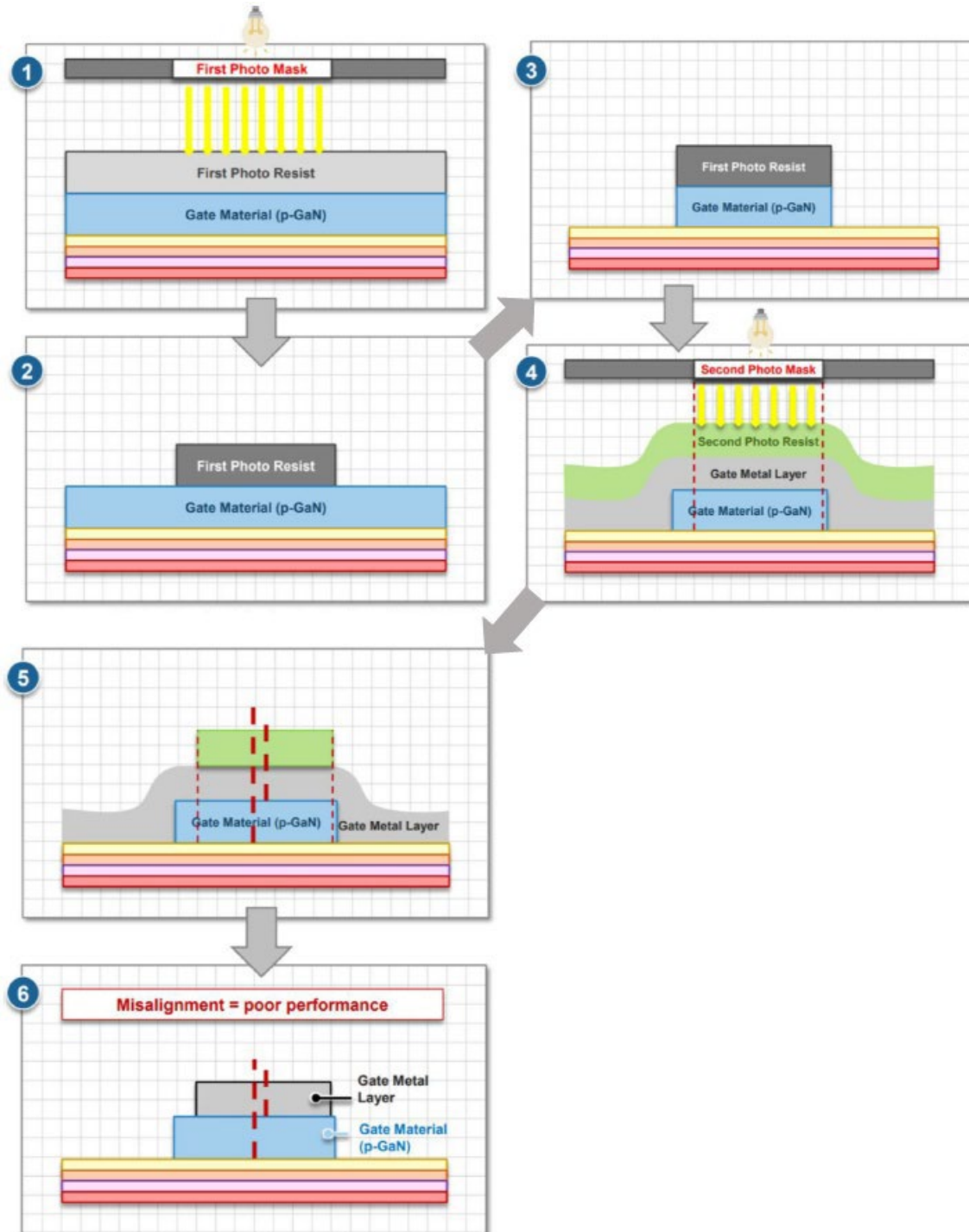
This evidence, particularly the language in the ’335 patent itself, undermines Patent Owner’s argument that “[t]he process for forming gate ledges using separate masks instead of the self-aligned process disclosed in the ’335 patent *cannot* produce ledges that are ‘substantially symmetric.’” PO Resp. 39 (emphasis added); *see also* PO Resp. 42–43 (arguing that a gate structure with ledges having substantially equal widths is “**not achievable**” without using a single photo-mask process). We have considered the evidence presented by Patent Owner and Dr. Schubert in support of Patent Owner’s arguments. PO Resp. 38–43; Ex. 2005 ¶¶ 49–51. We, however, are unable to discern sufficient evidence supporting a conclusion that using separate masks cannot produce ledges that are substantially symmetric, particularly when the ’335 patent suggests otherwise. See Ex. 1001, 4:60–63 (referring only to the “possibility of misalignment”). Even if, as Patent Owner and Dr. Schubert contend, misalignment “naturally” occurs when using a two-mask process, that does not foreclose the possibility that the

IPR2023-01384

Patent 10,312,335 B2

process can result in alignment. Moreover, we note that in some instances Patent Owner and Dr. Schubert refer to separate masks as “generally result[ing] in misalignment,” which, similar to the language in the ’335 patent, is not absolute. PO Resp. 40; Ex. 2005 ¶ 50.

Petitioner and Dr. Schubert direct us to the graphical representation below to illustrate misalignment due to a two-mask process.



This figure shows “an example form of misalignment . . . due to the double photo-mask process.” PO Resp. 41–42. Although we agree that the image shows the center of the gate metal and the center of the gate semiconductor material being out of alignment, neither Patent Owner nor Dr. Schubert

explains or demonstrates sufficiently why this misalignment is “inevitable” when using a two-mask process. PO Resp. 41; Ex. 2005 ¶ 50.

Additional evidence in the record supports a finding that other methods besides the self-aligned process can create symmetric ledges. The Specification of the ’335 patent equates ledges that are “symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material,” the purported structural feature imparted by the self-aligned process, with ledges that have substantially equal widths. Ex. 1001, 3:59–64. As Petitioner points out, claim 1 requires ledges having substantially equal widths, but does not require that the ledges are self-aligned. Ex. 1001, 5:5–24. Claim 2, which depends from claim 1, requires that the horizontal ledges of claim 1 are self-aligned. Ex. 1001, 5:26–28. The presence of “self-aligned” in claim 2 but not claim 1 suggests that there are other ways to achieve ledges having substantially equal widths (i.e., that are symmetrical) other than using the self-aligned process recited in claim 2. *Phillips*, 415 F.3d. at 1314–15 (“[T]he presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim.”).

Patent Owner also asserts that the self-aligned process provides the benefit of achieving the “minimal critical dimension (CD)” for the gate contact, meaning the gate semiconductor material only needs to be as wide as the desired width of the gate metal. PO Resp. 40–41. Patent Owner explains that without using the self-aligned process, “the gate semiconductor material (or other layers) below the gate metal had to be wider than the gate metal to accommodate for expected misalignment that occurs when more than one photo mask is used.” PO Resp. 40.

To the extent Patent Owner is asserting that minimal CD is a structural feature unique to the self-aligned process, we note that the '335 patent refers to minimal CD when discussing the two-mask process. Ex. 1001, 4:54–60. As Petitioner points out, the '335 patent states that a two mask process involves “etch[ing] the gate metal to a minimum CD.” Ex. 1001, 4:57–58; Reply 20; *see also* Tr. 14:14–15 (counsel for Petitioner stating that “[y]ou can make that same minimum critical dimension in the two-mask process”). During the oral hearing, counsel for Petitioner indicated that the '335 patent, when discussing minimum CD in the context of the self-aligned process (Ex. 1001, 3:65–67) and in the context of the two-mask process (Ex. 1001, 4:54–60), is “talking about the same thing, even though they are referring to it in two different ways.” Tr. 13:22–14:5. Patent Owner did not dispute this assertion. Nor does Patent Owner dispute Petitioner’s assertion that the '335 patent fails to provide an example of a “minimum CD” or explain how to determine whether a gate has achieved a minimum. Reply 20 n.5. And as to Patent Owner’s assertion that without using the self-aligned process “the gate semiconductor materials (or other layers) below the gate metal had to be wider than the gate metal,” we note that for both the self-aligned method and two-mask method, the p-type gate material is wider than the gate metal. *See* Ex. 1001, Fig. 6C; PO Resp. 40; Ex. 2005 ¶¶ 50–51; *see also* Tr. 13:14–21 (counsel for Petitioner explaining that for both the self-aligned method and two-mask method, the p-type material has a wider critical dimension than the gate material above it).

Thus, although using the self-aligned process may impart structural features to a transistor, the evidence suggests those same structural features may be imparted using other processes. In other words, the evidence of record demonstrates that it is possible to make a transistor having a p-type

gate with a minimum CD and symmetric ledges using a process other than a self-aligned process. We recognize the '335 patent explains a self-aligned process may provide an advantage over other processes, i.e., by reducing or eliminating the “possibility of misalignment.” Ex. 1001, 4:60–63. But it is not clear how that purported advantage of the process translates into a new, structurally different product. Rather, the language in the Specification addresses making an old product using a new, more advantageous process.

Accordingly, we find that “self-aligned” is a product-by-process limitation in claims 2 and 5, and does not fall within the exception to the rule for product-by-process claims.

#### *D. Overview of Asserted Prior Art*

##### *1. Saxler (Ex. 1007)*

Saxler discloses Group III-nitride high electron mobility transistors and methods for forming those transistors. Ex. 1007 ¶¶ 1, 7. In particular, Saxler is directed to HEMTs that include “a non-uniform aluminum concentration AlGaN based cap layer having a high aluminum concentration adjacent a surface of the cap layer that is remote from the barrier layer on which the cap layer is provided.” Ex. 1007, code (57). Saxler explains that having such a cap layer “may improve robustness of the device during processing and/or device operation” over conventional devices. Ex. 1007 ¶ 47. Saxler also explains that HEMTs “may offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies.” Ex. 1007 ¶ 4.

Saxler discloses several embodiments of its claimed invention, including the transistors depicted in Figures 1A and 1B, reproduced below.

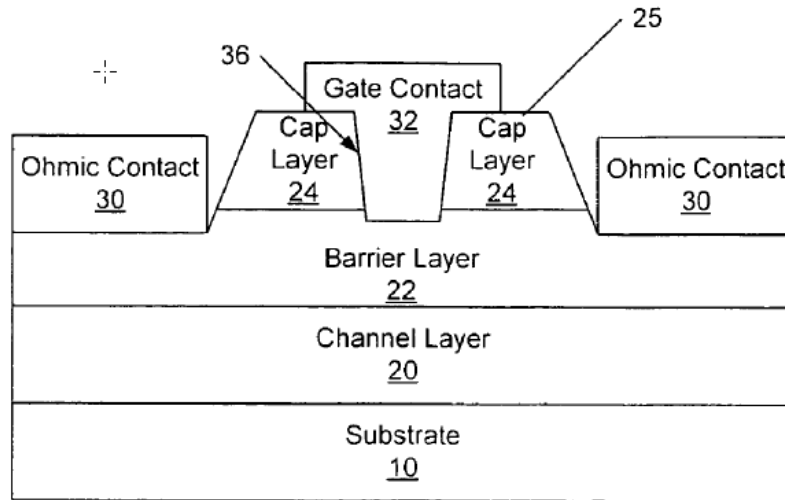


Figure 1A

Figure 1A of Saxler shows a cross-sectional schematic drawing illustrating a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24, and gate contact 32. Ex. 1007 ¶¶ 31, 57, 61, 66. In this embodiment, gate contact 32 occupies recess 36 in cap layer 24. Ex. 1007 ¶¶ 61, 66.

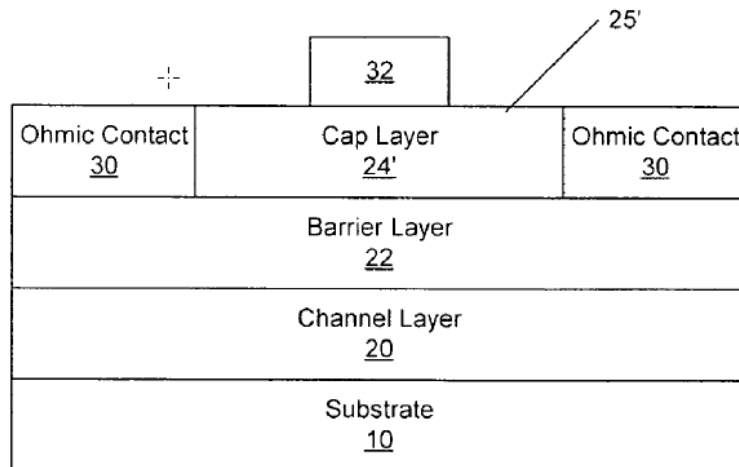


Figure 1B



Figure 1B of Saxler shows a cross-sectional schematic drawing illustrating a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24', and gate contact 32. Ex. 1007 ¶¶ 31, 57, 61, 66. In this embodiment, cap layer 24' does not have a recess, such that gate 32 is on cap layer 24'. Ex. 1007 ¶¶ 61, 66.

Saxler describes the features of its various embodiments, including those with a gate recess and those without a gate recess. *E.g.*, Ex. 1007 ¶¶ 66 (describing suitable gate materials), 70 (describing suitable n-type dopants), 71 (describing suitable p-type dopants). Saxler also discloses methods for making transistors according to the embodiments described in the specification. Ex. 1007 ¶¶ 6, 68.

## 2. Yoshida (Ex. 1006)

Yoshida discloses GaN-based HEMT structures that can operate under the application of high voltages and at higher speeds. Ex. 1006 ¶¶ 1, 8. Yoshida depicts the basic structure of its described invention in Figure 1, reproduced below.

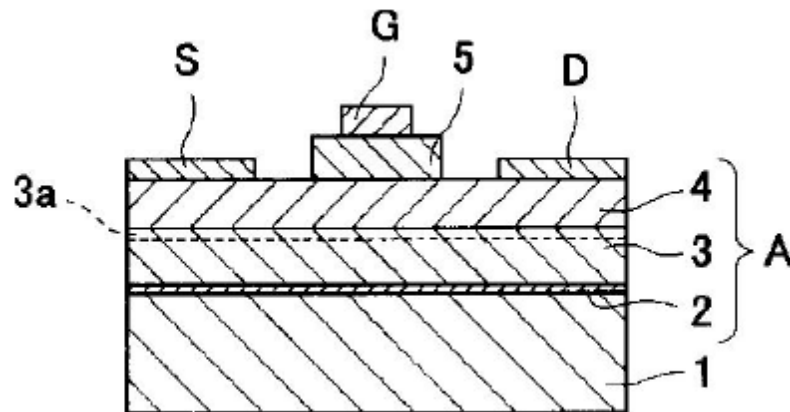


Figure 1 of Yoshida shows a cross-sectional view of a transistor having a stacked structure comprising buffer layer 2, i-type semiconductor layer 3,

and n-type semiconductor layer 4 formed on semi-insulating substrate 1.

Ex. 1006 ¶ 10. Figure 1 also shows gate electrode G on p-type semiconductor layer 5, as well as source electrode S and drain electrode D, all formed on n-type semiconductor layer 4. Ex. 1006 ¶ 10.

Yoshida discloses methods for fabricating the structure shown in Figure 1, including deposition and etching conditions. Ex. 1006 ¶¶ 19–23.

*E. Claims 1–7 – Alleged Obviousness in view of Yoshida and Saxler*

Petitioner contends claims 1–7 of the '335 patent are unpatentable as obvious over Yoshida in view of Saxler. Pet. 68–88; Reply 14–19, 25–26. Patent Owner argues that Petitioner fails to demonstrate sufficiently that Yoshida and Saxler disclose or suggest all of the limitations in claims 1–7, or that a person of ordinary skill in the art would have modified Yoshida in view of Saxler. PO Resp. 62–67; Sur-reply 4–9, 23–25.

*1. Analysis*

*a) Claim 1*

*i. [Ip]*

Petitioner contends Yoshida discloses an “enhancement-mode GaN transistor,” as recited in the preamble of claim 1. Pet. 71–72. According to Petitioner “Yoshida discloses a GaN high-mobility transistor that includes a p-type GaN layer below the gate, which ‘enables voltage control with a small amount of carrier injection,’ constituting a normally-off enhancement-mode GaN transistor.” Pet. 71–72<sup>7</sup> (quoting Ex. 1006 ¶ 17; citing Ex. 1006

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<sup>7</sup> Petitioner italicizes the names of references, but we have omitted such emphasis for purposes of this Decision.

¶ 15, Fig. 1). Patent Owner agrees that Yoshida discloses an enhancement mode device. PO Resp. 2 (“Yoshida . . . is an enhancement mode device.”).

*ii. [1a]–[1c]*

Limitation [1a] recites “a GaN layer” (Ex. 1001, 5:6), limitation [1b] recites “a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer” (Ex. 1001, 5:7–9), and limitation [1c] recites “a source contact and a drain contact formed on the barrier layer” (Ex. 1001, 5:10–11). Petitioner contends Yoshida discloses each of these limitations and directs us to Figure 1 of Yoshida, reproduced below. Pet. 72–74.

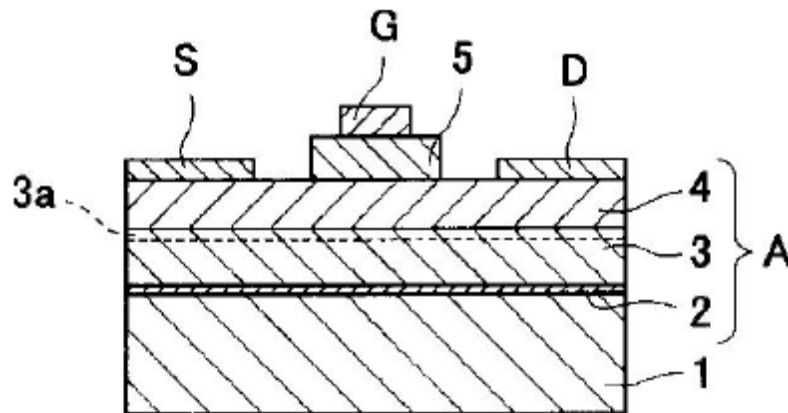


Figure 1 of Yoshida shows a cross-sectional view of a transistor having a stacked structure. Ex. 1006 ¶ 10. Petitioner argues that Yoshida teaches layer 3 is a GaN layer, layer 4 is a barrier layer that can be an AlGaIn layer, and that a 2DEG is formed at the interface of layer 3 and layer 4. Pet. 72–73 (citing Ex. 1006 ¶¶ 10, 12, 13, 16, Abstract, Fig. 1; Ex. 1003 ¶¶ 192–197). Petitioner also contends that Yoshida discloses source and drain electrodes,

identified as S and D in Figure 1, respectively, formed on barrier layer 4.

Pet. 74 (citing Ex. 1006 ¶¶ 14, 22, Abstract, Fig. 1; Ex. 1003 ¶¶ 198–199).

Patent Owner does not dispute Petitioner’s arguments and evidence that Yoshida discloses limitations [1a]–[1c]. Based on the undisputed evidence presented in the Petition, Petitioner has demonstrated persuasively that Yoshida discloses the subject matter recited in limitations [1a]–[1c].

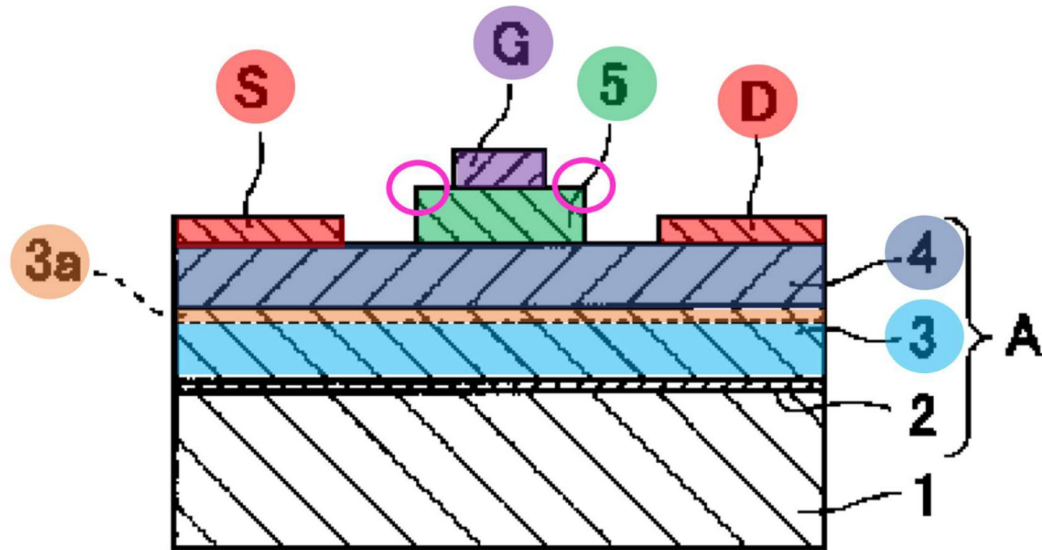
Ex. 1006 ¶¶ 10, 12–14, 16, 22, Abstract, Fig. 1.

*iii. [1d] (the “side surfaces” limitation)*

Limitation [1d] recites “a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer.” Ex. 1001, 5:12–15.

Petitioner argues that Yoshida teaches layer 5 in Figure 1 is formed above (AlGaIn) barrier layer 4 and may comprise p-type GaN. Pet. 75 (citing Ex. 1006 ¶¶ 09, 15, 18). Petitioner also argues that, similar to Yoshida’s layer 5, Saxler’s cap layer is a p-type gate material and resides above an AlGaIn barrier layer. Pet. 78 (citing Ex. 1007 ¶¶ 13, 69, 71, 73). Referring to Figure 1A of Saxler, Petitioner further argues that Saxler’s cap layer has side surfaces extending horizontally towards the source and drain contacts, and that it would have been obvious to combine the sloped sidewalls of Saxler’s cap layer with Yoshida’s layer 5. Pet. 78–79.

Petitioner contends that implementing Saxler’s sloped sidewalls in Yoshida’s GaN layer 5 would result in the structure depicted in modified Figure 1 of Yoshida, reproduced below. Pet. 68–69.



Modified Figure 1 of Yoshida shows a cross-sectional view of a transistor having GaN layer 3 (highlighted in light blue) and n-type semiconductor layer 4 (highlighted in dark blue) formed over barrier layer 2 and substrate 1, with 2DEG 3a (highlighted in orange) formed at the interface of layers 3 and 4. Pet. 68–69, 73–74. Figure 1 also depicts source contact S and drain contact D (both highlighted in red) and a stacked gate structure above semiconductor layer 4 consisting of gate metal G (highlighted in purple) overlaying GaN layer 5 (highlighted in green), modified to show sloped sidewalls. Pet. 68–69. The stacked gate structure includes a pair of horizontal ledges (highlighted in pink) on either side of gate metal G. Pet. 69.

Petitioner contends that modifying Yoshida to include Saxler’s sloped sidewalls “calls for nothing more than . . . simple substitution . . . to predictably make an enhancement-mode GaN HEMT,” and that a person of ordinary skill in the art would have made the proposed modification to reduce gate leakage. Pet. 69–70 (citing Ex. 1003 ¶¶ 185–189). In particular, Petitioner contends that (1) sloped sidewalls were conventional, (2) the angle of Saxler’s sloped sidewall is typical for mesa structures, (3) Saxler

discloses conventional etching techniques for forming its sloped sidewalls, and (4) “[i]t was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage.” Pet. 70–71 (citing Ex. 1003 ¶¶ 185–189; Ex. 1014,<sup>8</sup> 1; Ex. 1019<sup>9</sup> ¶¶ 13, 27, 144, 157, Fig. 12A).

Patent Owner does not dispute that the combined teachings of Yoshida and Saxler disclose or suggest the “side surfaces” limitation recited in [1d]. See PO Resp. 62–67. Nor does Patent Owner dispute Petitioner’s arguments and evidence demonstrating that (1) sloped sidewalls were conventional, (2) the angle of Saxler’s sloped sidewall is typical for mesa structures, (3) Saxler discloses conventional etching techniques for forming its sloped sidewalls, and (4) “[i]t was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage.” See PO Resp. 62–67; Pet. 70–71; Ex. 1003 ¶¶ 185–189; Ex. 1014, 1; Ex. 1019 ¶¶ 13, 27, 144, 157, Fig. 12A.

Instead, Patent Owner argues that a person of ordinary skill in the art would not have modified Yoshida with the sloped sidewalls of Saxler because Yoshida teaches away from adding the sloped sidewalls of Saxler’s cap layer to Yoshida’s layer 5. PO Resp. 64. Patent Owner’s teaching away argument is based on its assertions that Yoshida is formed “by a specific process where the p-type GaN layer 5 is ‘etch[ed] away . . . except for where the gate electrode was to be loaded,’” and that Yoshida’s transistor is “assembled to position the pn junction of a p-type GaN layer 5 ‘immediately

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<sup>8</sup> Xu et al., *The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure*, IEEE ELECTRON DEVICE LETTERS, Vol. 28, No. 11, 942 (Nov. 2007).

<sup>9</sup> Kanda et al., US 2005/0087763 A1, published Apr. 28, 2005.

under’ the gate electrode G.” PO Resp. 64 (quoting Ex. 1006 ¶¶ 17, 22; alterations by Patent Owner). Patent Owner contends Yoshida’s specific assembly process provides for

voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility.

PO Resp. 64 (quoting Ex. 1006 ¶ 17; citing Ex. 2005 ¶ 432).

Patent Owner argues that Yoshida teaches away from adding Saxler’s sloped sidewalls to Yoshida’s layer 5 “because doing so would intentionally widen the pn junction relative to the gate electrode G creating misalignment, thus reducing ‘voltage control’ by increasing the required amount of carrier injection and reducing high-speed electron mobility.” PO Resp. 64–65.

Patent Owner further asserts that the sloped sidewalls would provide excessive surface area that cannot receive the gate electrode G, which is “contrary to the intentional shape” of Yoshida’s layer 5. PO Resp. 65; *see also* PO Resp. 66 (arguing that Yoshida “limits the width of its p-type GaN layer”).

It is well settled that “[a] reference does not teach away . . . if it merely expresses a general preference for an alternative invention but does not ‘criticize, discredit or otherwise discourage’ investigation into the invention claimed.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)). Furthermore, “teaching that a composition may be optimal or standard does not criticize, discredit, or otherwise discourage

investigation into other compositions.” *Galderama Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 739 (Fed. Cir. 2013).

Here there is no express teaching away from applying Saxler’s sloped sidewalls in Yoshida’s transistor. Rather, Patent Owner infers Yoshida teaches away from the proposed modification because Yoshida describes a benefit (i.e., voltage control) resulting from the structure achieved by following the assembly process disclosed in Yoshida. PO Resp. 63–65. However, even assuming that implementing Petitioner’s proposed modification to Yoshida would impact the resulting structure in the way Patent Owner argues, namely by widening the pn junction relative to gate electrode G, and would have the alleged effect of “reducing voltage control,” Patent Owner does not direct us to any evidence in Yoshida, nor do we discern any, that indicates this result is “serious enough to dissuade” the proposed modification to Yoshida to include sloped sidewalls. *Galderama*, 737 F.3d at 739; *see also Winner Int’l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000) (“The fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another.”). Accordingly, we find that Yoshida does not teach away from adding Saxler’s sloped sidewalls.<sup>10</sup>

Patent Owner also disputes Petitioner’s contention that “[t]he combination calls for nothing more than the simple substitution of Saxler’s sidewalls to predictably make an enhancement-mode GaN HEMT.”

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<sup>10</sup> In view of this finding, we decline to address Petitioner’s alternative argument that “[e]ven if *Yoshida* teaches away from widening the pn-junction . . . , the proposed combination does not require widening it” (Reply 25) and Patent Owner’s counter arguments (Sur-reply 23–24).



PO Resp. 63–64 (quoting Pet. 69). According to Patent Owner, the embodiment from Saxler that Petitioner relies upon is not an enhancement-mode transistor and does not provide any guidance on making an enhancement mode GaN HEMT. PO Resp. 65. Additionally, Patent Owner argues that “[t]he cap layer of Saxler extends substantially the entire width between the source and the drain (EX1007, Fig. 1A) while Yoshida intends to limit the width of its p-type GaN layer (EX1006 ¶[0022]).” PO Resp. 65.

Contrary to Patent Owner’s assertion, however, Petitioner does not seek to substitute Saxler’s entire cap layer for Yoshida’s. Instead, Petitioner’s proposed modification is directed to modifying the sidewalls of Yoshida’s cap layer to include the sloped sidewalls of Saxler’s cap layer. Pet. 79–80. Thus, Patent Owner’s argument based on differences between how far the cap layers of Saxler and Yoshida extend between source and drain is misplaced.

Additionally, it is undisputed that Yoshida discloses a process for making an enhancement mode device. Pet. 71–72; Ex. 1006 ¶¶ 15, 17, Fig. 1; PO Resp. 2 (“Yoshida . . . is an enhancement mode device.”), 66 (referring to the “enhancement-mode transistor of Yoshida”). Patent Owner also does not dispute Petitioner’s arguments and evidence demonstrating that sloped sidewalls were conventional and that Saxler discloses conventional techniques for forming its sloped sidewalls. Pet. 70–71. Moreover, we do not discern evidence on this record demonstrating that Saxler’s etching technique would only be applicable to a non-enhancement mode device or that a person of ordinary skill in the art would not have been able to apply Saxler’s etching technique to Yoshida’s process. Indeed, Dr. Shealy testified that a person of ordinary skill in the art “would be familiar with both” enhancement and non-enhancement mode devices. Ex. 2004, 65:3–

11. And Dr. Schubert testified that “[d]epletion-mode FETs are easier to fabricate.” Ex. 2005 ¶ 35. The evidence of record thus supports Petitioner’s assertion that “[t]he combination calls for nothing more than the simple substitution of Saxler’s sidewalls to predictably make an enhancement-mode GaN HEMT.” Pet. 69.

In view of the foregoing, including the undisputed evidence presented in the Petition, we find Petitioner has demonstrated persuasively that Yoshida and Saxler disclose or suggest the subject matter recited in limitation [1d], and that a person of ordinary skill in the art would have had reason to modify Yoshida to include Saxler’s sloped sidewalls with a reasonable expectation of success. Pet. 68–71, 75, 78–79; Ex. 1003 ¶¶ 185–189; 1006 ¶¶ 9, 15, 18; Ex. 1007 ¶ 13, 69, 71, 73; Ex. 1014, 1; Ex. 1019 ¶¶ 13, 27, 144, 157, Fig. 12A.

*iv. Limitation [1e]*

Limitation [1e] recites “a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material.” Ex. 1001, 5:16–18. Petitioner contends that Yoshida’s gate electrode is a metal formed on p-type layer 5 with sidewalls that extend vertically towards p-type layer 5. Pet. 81–82 (citing Ex. 1006 ¶¶ 6, 9–10, 16, 22–23, Fig. 1; Abstract).

Patent Owner does not dispute Petitioner’s arguments and evidence that Yoshida discloses limitation [1e]. Based on the undisputed evidence presented in the Petition, Petitioner has demonstrated persuasively that Yoshida discloses the subject matter recited in limitation [1e]. Ex. 1006 ¶¶ 6, 9–10, 16, 22–23, Fig. 1; Abstract.

v. *Limitation [1f]*

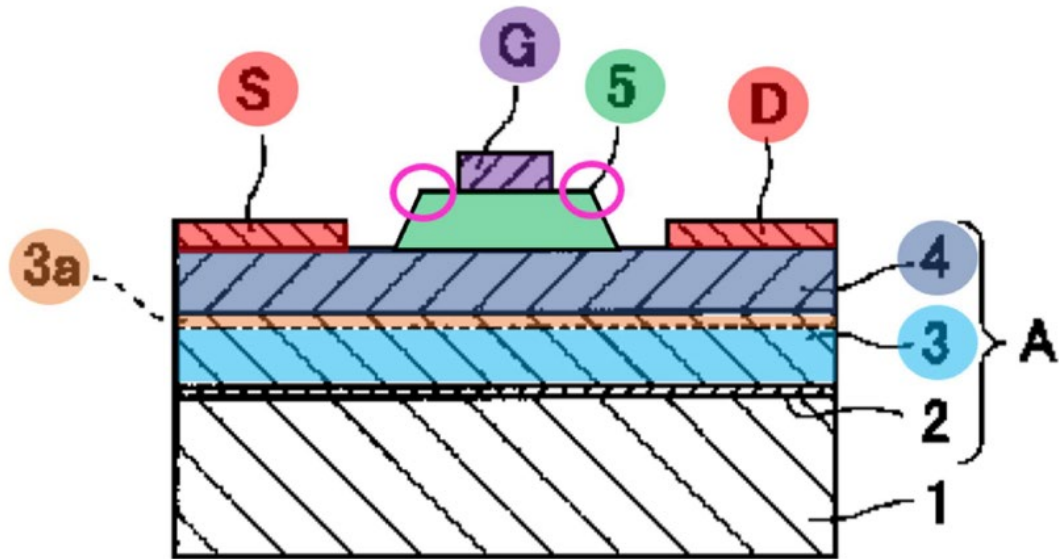
Limitation [1f] requires

the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

Ex. 1001, 5:19–25. Petitioner contends, and Patent Owner does not dispute, that Yoshida’s gate electrode is narrower than layer 5, such that Yoshida discloses horizontal ledges that extend past the sidewalls of the gate metal and toward Yoshida’s source and drain. Pet. 83 (citing Ex. 1006 ¶¶ 22–23, Fig. 1; Ex. 1003 ¶ 201). According to Petitioner, Yoshida’s ledges “are symmetric on either side of the gate metal (i.e., having substantially equal widths).” Pet. 83. Petitioner asserts that the combination of Yoshida and Saxler renders obvious the subject matter recited in [1f], and directs us again to the structure depicted in modified Figure 1 of Yoshida, reproduced below. Pet. 83–84.<sup>11</sup>

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<sup>11</sup> Patent Owner contends that Petitioner presents a new argument in the reply that the figures in Yoshida and Saxler render obvious “substantially equal ledges.” Sur-reply 4. We disagree, as Petitioner expressly states that “[t]he combination of *Yoshida* and *Saxler* also renders obvious [1f].” Pet. 83.



Modified Figure 1 of Yoshida shows a cross-sectional view of a transistor having, *inter alia*, a stacked gate structure consisting of gate metal G (highlighted in purple) overlaying GaN layer 5 (highlighted in green), modified to show sloped sidewalls. Pet. 68–69, 84. Petitioner has included a pair of pink circles to highlight the allegedly symmetric horizontal ledges on either side of gate metal G. Pet. 84; Ex. 1003 ¶ 215.

Patent Owner argues that Petitioner improperly relies on patent drawings in asserting that Yoshida Figure 1 discloses substantially symmetric ledges because the Federal Circuit has held that “patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” PO Resp. 31 (quoting *Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000)).

In the Institution Decision, we determined that the claim term “substantially equal” in the ’335 patent does not require a precise proportion or particular size because “substantially” is a common approximation or term of degree in patent claims. Inst. Dec. 37–38. Therefore, *Hockerson*

does not apply because Petitioner is not relying on a drawing in Yoshida for precise proportions. Inst. Dec. 37–38. Patent Owner does not directly dispute that “substantially” is a term of degree or an approximation. *See generally* PO Resp; Sur-reply, 6–7 (arguing only that “substantially” is definite and “describe[s] a **particular** characteristic”).

In the Institution Decision, we also noted that claim 7 requires self-aligned edges that are “symmetrical” with respect to the gate material, and invited the parties to address whether the holding in *Hockerson* applies to that claim term. Inst. Dec. 38 n.11. Petitioner asserts that the general rule of *Hockerson* does not apply to claim 7’s symmetric ledges, but Patent Owner did not address the applicability of *Hockerson*’s rule to claim 7. Reply 17; *see generally* PO Resp.; Sur-reply. Patent Owner has thus forfeited any argument that the rule in *Hockerson* applies to claim 7, including any argument that the claim term “symmetrical” requires a precise proportion or particular size. *See* Paper 12, 9 (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.”). This favors Petitioner’s argument that the rule in *Hockerson* does not apply to the claims in the ’335 patent in general because the ’335 patent explicitly equates “substantially equal widths” with “symmetric.” Ex. 1001, 3:59–63.

We turn next to the Board’s decision in *Ex parte Bjorn*, No. 2018-001567, 2019 WL 6173305 (PTAB Oct. 16, 2019) and the parties’ arguments as to how this case applies to the term “substantially equal” ledges recited in claim 1. In *Bjorn*, the Board addressed an Examiner’s rejection of several claims based on various prior art references. In one instance, the Board did not apply the holding of *Hockerson* and relied on patent drawings to sustain the examiner’s rejection. *Id.* at \*10–11. In another instance, the Board did apply the general rule of *Hockerson* and

refused to rely on drawings alone to sustain the rejection. *Id.* at \*17. Not surprisingly, both parties argue that *Bjorn* supports their own positions. PO Resp. 32; Reply 17; Sur-reply 1, 4–7.

The technology at issue in *Bjorn* involved bone implants. Claim 1 of the application involved in *Bjorn* recited an abutment that includes “an exterior surface diameter . . . that is less than or substantially equal to the maximum thread diameter of the male screw section of the bone fixture.” *Bjorn*, 2019 WL 6173305 at \*1. The examiner rejected claim 1 based on drawings in a prior art patent application, but the appellant argued that the reference did not disclose the drawings as being to scale, and, therefore, the drawings could not be used to teach an abutment that includes “an exterior surface diameter . . . that is less than or substantially equal to the maximum thread diameter of the male screw section of the bone fixture.” *Id.* at \*10. The Board determined that the general rule of *Hockerson* did not apply because “[n]o particular dimensions or proportions are claimed” and “the drawings of [the prior art patent application] clearly disclose to a skilled artisan that abutment 82 has exterior surfaces with a diameter that is ‘less than or substantially equal to the maximum thread diameter of the male screw section of the bone fixture’ as claimed.” *Id.* In reaching its decision to sustain the examiner’s rejection, the Board determined several figures clearly showed abutments having an exterior surface with a diameter that was substantially equal to external threads. *Id.* at \*11 (relying on surfaces that appear “even/flush” in the figures).

Claim 8 of the application involved in *Bjorn* also recited an abutment that includes an exterior surface with a maximum length that “is less than or substantially equal to the maximum thread diameter of the male screw section.” *Id.* at \*17. In addressing the examiner’s rejection of claim 8 based

on a different reference than the one discussed above with regard to claim 1, the Board stated that “[t]he issue is whether [the reference’s] abutment portion, which is larger in diameter than the maximum diameter of the bone fixture screw threads in Figure 9, can be considered ‘substantially equal to the maximum thread diameter of the male screw section of the bone fixture’ as recited in claim 8.” *Id.* at \*17. The Board explained that “even if we determine what percentage or ratio of an oversized abutment diameter is permitted within the scope of the claim, the drawings cannot be relied on to disclose such precise or relative proportions.” *Id.* (citing *Hockerson*, 222 F.3d at 956). The Board therefore determined that the general rule in *Hockerson* did apply and the Board did not sustain the examiner’s rejection.

Patent Owner argues that we should not follow the Board’s analysis with regard to claim 1 in *Bjorn*, where it did not apply the general rule *Hockerson*, because there the Board was addressing the limitation of “less than or substantially equal.” PO Resp. 32; Sur-reply 4–5. Instead, Patent Owner argues that we should follow the Board’s analysis with regard to claim 8, where it did apply the general rule of *Hockerson*, because the “heart of the issue related to the ‘substantially equal’ limitation.” Sur-reply 5. Patent Owner’s argument, however, is unavailing, as both claim 1 and claim 8 in *Bjorn* recited “less than or substantially equal,” and the Board addressed the “substantially equal” language in its analysis of both claims. *Bjorn*, 2019 WL 6173305 at \*10–11, 17.

In *Bjorn*, the Board’s determination of whether or not to apply the rule in *Hockerson* did not depend on any difference in claim language, but rather a difference in what the drawings disclosed to a person of ordinary skill in the art. Indeed, after agreeing with the general rule set forth in *Hockerson*, the Board stated that

“a drawing is available as a reference for all that it teaches a person of ordinary skill in the art.” *In re Meng*, 492 F.2d 843, 847 (CCPA 1974[]); *see also In re Aslanian*, 590 F.2d 911, 914 (CCPA 1979) (same). Furthermore, things shown clearly in patent drawings are not to be disregarded. *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972). Therefore, “a drawing in a utility patent can be cited against the claims of a utility patent application even though the feature shown in the drawing was unintended or unexplained in the specification of the reference patent.” *Aslanian*, 590 F.2d at 914; *see also In re Seid*, 161 F.2d 229, 231 (CCPA 1947) (“an accidental disclosure, if clearly made in a drawing, is available as a reference.”).

*Bjorn*, 2019 WL 6173305 at \*10. Consistent with this, the Board relied on drawings (and did not apply the rule in *Hockerson*) when the drawings “clearly disclosed” the claim limitation at issue. When the drawings did not (e.g., the drawings clearly showed a larger size), the Board did not rely on drawings.

Here, as in *Bjorn*, the claims do not expressly recite particular dimensions or proportions. Further, Patent Owner concedes that the drawing shows a gate that is centrally aligned. PO Resp. 3 (stating that “Uemoto, like Saxler and Yoshida, represents the transistor with schematics illustrating a gate with a centrally aligned electrode contact”); *see also* Tr. 87:18–20 (counsel for Patent Owner characterizing Figure 1 of Yoshida as “centrally aligned”). Because the drawing in Yoshida “is available as a reference for all that it teaches a person of ordinary skill in the art,” which in this case is a centrally-aligned gate contact, we decline to disregard what is shown in Yoshida’s drawing. *Meng*, 492 F.2d at 847; *Aslanian*, 590 F.2d at 914; *Mraz*, 455 F.2d at 1072.

For all of the foregoing reasons, we determine that Petitioner did not improperly rely on the drawing in Yoshida to disclose “substantially equal



ledges,” as the general rule in *Hockerson* does not apply in view of the specific facts and circumstances in the present case.

Patent Owner contends that even when a patent drawing appears on its face to disclose equal width ledges, the drawing “does not disclose ‘a pair of ledges having substantially equal widths’ within the meaning of the ’335 patent.” PO Resp. 31. According to Patent Owner, “the ‘substantially equal width’ ledges described in the ’335 patent are **nanometer** widths and could not be depicted in patent drawings without an exploded view of the gate, annotated with dimensions.” PO Resp. 29. By way of example, Patent Owner asserts that a drawing in Uemoto shows ledges that are substantially equal in width, but “[i]n reality,” the ledges of Uemoto “differ substantially” based on measurements made from a scanning electron microscope image of Uemoto’s fabricated transistor. PO Resp. 30–31 (arguing that in Uemoto’s actual device, one of the ledges is 68% larger than the other based on Patent Owner’s annotated version of Uemoto Figure 5).

As Petitioner points out, however, the claims of the ’335 patent do not recite any dimensions or assign a numerical value to the term “substantially equal widths,” and Patent Owner does not present any argument that the claims should be construed to include any such dimensions or values. Reply 14; *see* PO Resp. 7–8. We also note that the ’335 patent does not contain any annotated figures showing measurements of the ledges of an actual transistor or comparing the widths of each ledge. *See* Ex. 1001, Figures 1–8. Patent Owner presents an annotated version of Figure 7B from the ’335 patent, but the measurements and annotations appear to have been created in connection with this proceeding. *Compare* Ex. 1001, Fig. 7B *with* PO Resp. 30 (showing Patent Owner’s annotated Figure 7B). Thus, we discern no evidence in the ’335 patent itself supporting Patent Owner’s assertion that

“the ‘substantially equal width’ ledges described in the ‘335 patent . . . could not be depicted in patent drawings.” PO Resp. 29. Additionally, we agree with Petitioner that “[t]he fact that [Uemoto] happens to draw a centered gate and build an offset gate does not mean the ‘335 patent’s ‘substantially equal’ requirement should be limited to any particular dimension.” Reply 15. Nor does it mean that every patent drawing that “appears on its face” to disclose equal width ledges “does not disclose ‘a pair of ledges having substantially equal widths’ within the meaning of the ‘335 patent.” PO Resp. 31.

Instead, the relevant inquiry here is what a person of ordinary skill in the art would have understood from Yoshida’s drawing. *Meng*, 492 F.2d at 847; *Aslanian*, 590 F.2d at 914; *Mraz*, 455 F.2d at 1072. It is undisputed that, on its face, Yoshida’s figure shows a gate contact that is centrally aligned, creating symmetric ledges. *See* PO Resp. 3; Tr. 87:18–20; Ex. 1003 ¶ 214.

Patent Owner contends that Dr. Shealy “discredited the accuracy of transistor schematics” and “specifically stated that the schematic of Fig. 1 of Yoshida cannot be relied on for its accuracy.” PO Resp. 60 (citing Ex. 2004, 53:13, 53:16–25, 56:24–57:1, 60:17–18, 82:16–19).<sup>12</sup> According to Patent Owner, “Yoshida itself demonstrates that patent drawings are not drawn to scale, and cannot be relied upon for dimensions” because “[l]ayers 3 and 4 of Yoshida are shown in the schematic of Fig. 1 as having the same

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<sup>12</sup> In its Sur-reply, Patent Owner states that “Petitioner also explicitly applies the same ‘principle’ that the drawings do not represent an actual transistor to address the drawings of Yoshida. Pet., 90-91.” Sur-reply 7. We, however, do not discern any such explicit discussion regarding whether the drawings of Yoshida represent an actual transistor on Pages 90–91 of the Petition.

thickness, while Yoshida explicitly discloses that layer 3 is 10 times thicker than layer 4.” PO Resp. 60 (citing Ex. 1006 ¶¶ 20–21).

We have reviewed the deposition testimony of Dr. Shealy that Patent Owner cites to support its arguments. In all but one instance, Dr. Shealy was discussing Saxler’s figures, not Yoshida’s. Ex. 2004, 53:13, 53:16–25, 56:24–57:1, 60:17–18. In that regard, to the extent Dr. Shealy’s testimony could even be construed as “discrediting the accuracy of transistor schematics,” we discern nothing in that testimony to suggest the testimony would apply beyond Saxler’s figures.<sup>13</sup> We do note, however, that one aspect of Saxler’s figure that Dr. Shealy did not “discredit” is his expectation that the gate contact would be centered, as depicted. Ex. 2005, 57:3–7.

With regard to Yoshida, Dr. Shealy did testify that “Figure 1 doesn’t appear like what’s described in [paragraph] 23, because the SiO<sub>2</sub> isn’t shown there. And it obviously was removed to get to that figure.” Ex. 2004, 82:16–19. We, however, do not consider this testimony to be a “specific[] state[ment] that the schematic of Fig. 1 of Yoshida cannot be relied on for its accuracy.” PO Resp. 60.<sup>14</sup> Instead, this testimony, when considered in

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<sup>13</sup> Saxler states that its illustrations are “idealized embodiments of the present invention,” and that “variations from the shapes of the illustrations as a result . . . of manufacturing techniques and/or tolerances, are to be expected.” Ex. 1007 ¶ 42. Saxler continues to state that the embodiments of the present invention “should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes.” Ex. 1007 ¶ 42. We consider such language to convey to a person of ordinary skill in the art that Saxler’s teachings include, but are not limited to, the particular shapes shown in the figures. Patent Owner has not directed us to similar language in Yoshida.

<sup>14</sup> Notably, in some instances, Patent Owner itself relies on Figure 1 of Yoshida to support its own arguments. PO Resp. 11–14, 28, 59 (“Petitioner ignores the vertical sidewalls shown in Fig. 1 of Yoshida.”), 62, 66; *see also*

connection with the language in paragraph 23 of Yoshida, indicates only that Figure 1 does not depict the SiO<sub>2</sub> masking film used to fabricate the transistor shown in Figure 1 of Yoshida. Similarly, in view of the discussion in paragraphs 20 and 21, a person of ordinary skill in the art would have understood that the thicknesses shown for layers 3 and 4 in Figure 1 may not be to scale. Ex. 1006 ¶¶ 20–21. Patent Owner, however, directs us to no evidence in Yoshida, nor do we discern any, that would suggest to a person of ordinary skill in the art that the symmetry shown in Figure 1 is inaccurate or unintentional. To the contrary, in a portion of the Patent Owner Response addressing modifying Yoshida to use a “self-aligned” technique, which according to the ’335 patent provides symmetry, Patent Owner states that “this ‘self-aligned’ technique would achieve what Yoshida intends.”

PO Resp. 71 (also referring to “[t]he direct alignment of the gate electrode G with the pn junction” that is formed under the p-type GaN layer 5).

For all of the foregoing reasons, including the evidence that Yoshida’s Figure 1 shows a centrally aligned gate, we find Petitioner has demonstrated sufficiently that Yoshida and Saxler disclose or suggest the subject matter recited in limitation [1f].

*vi. Conclusion for claim 1*

Based on the present record, Petitioner has shown by a preponderance of evidence that Yoshida and Saxler disclose or suggest all of the limitations in claim 1 and that a person of ordinary skill in the art would have had a reason to combine the teachings of Yoshida and Saxler with a reasonable expectation of success. Accordingly, we determine Petitioner has

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Tr. 70:24–25 (counsel for Patent Owner arguing that “we’re not completely discrediting the drawings . . . , the drawings still have features”).

demonstrated sufficiently that claim 1 is unpatentable as obvious in view of Yoshida and Saxler.

*b) Claim 2*

Claim 2 depends from claim 1 and requires that “the pair of horizontal ledges of the p-type gate material are self-aligned.” Ex. 1001, 5:26–28.

Petitioner contends that “self-aligned” is a product-by-process limitation, and lends no patentable weight to the claim. For the reasons discussed above in Section II.C.2, we agree.

“In determining validity of a product-by-process claim, the focus is on the product and not the process of making it.” *Amgen*, 580 F.3d at 1369. As Patent Owner acknowledges, “the structural features imparted by the self-aligned process allows ledges to be created that are “substantially symmetric” with respect to the gate metal disposed on the p-type material.” PO Resp. 38–39. For the reasons discussed above in Section II.E.1.a.v, we determine Petitioner has demonstrated persuasively that Yoshida and Saxler disclose or suggest ledges that are symmetric with respect to the gate metal disposed on the p-type material.

For these reasons, we determine Petitioner has demonstrated by a preponderance of evidence that claim 2 is unpatentable as obvious in view of Yoshida and Saxler.

*c) Claims 3 and 4*

Claim 3 depends from claim 1 and requires the “barrier layer comprises aluminum gallium nitride (AlGa<sub>0.5</sub>N).” Ex. 1001, 5:29–31. Claim 4 also depends from claim 1 and requires “the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width.” Ex. 1001, 6:1–5.

Petitioner assert that Yoshida discloses its layer 4 comprises AlGaIn, as required by claim 3, and that Yoshida alone and/or in view of Saxler discloses a gate electrode narrower than layer 5, as required by claim 4. Pet. 84–85 (citing Ex. 1006 ¶¶ 10, 13, 21–23, Fig. 1, Abstract; Ex. 1003 ¶¶ 218–219).

Patent Owner does not separately dispute Petitioner’s arguments and evidence that Yoshida and/or Saxler disclose or suggest the limitations in claims 3 and 4. Based on the undisputed evidence presented in the Petition, Petitioner has demonstrated persuasively that Yoshida and/or Saxler disclose or suggest the subject matter recited in claims 3 and 4. Ex. 1006 ¶¶ 10, 13, 21–23, Fig. 1, Abstract.

*d) Claim 5*

Independent claim 5 recites limitations similar to those in claim 1, but states that that the p-type gate material comprises a pair of self-aligned ledges instead of ledges having substantially equal widths. Ex. 1001, 6:6–23. Petitioner again contends that “self-aligned” is a product-by-process limitation, and lends no patentable weight to the claim. Pet. 86. Relying on the arguments it presented for claim 1, Petitioner asserts that the subject matter of claim 5 would have been obvious in view of the combined teachings of Yoshida and Saxler. Pet. 85–87.

Patent Owner likewise relies on the arguments it presented for claim 1 and claim 2, and does not present any arguments unique to, or specifically directed to, claim 5. Accordingly, for the same reasons discussed above with regard to claims 1 and 2, we find Petitioner has demonstrated persuasively that Yoshida and/or Saxler disclose or suggest the subject matter recited in claim 5.

*e) Claim 6*

Claim 6 depends from claim 5, and requires the barrier layer comprises AlGa<sub>N</sub>. Ex. 1001, 6:24–26. Petitioner assert that Yoshida discloses its layer 4 comprises AlGa<sub>N</sub>, as required by claim 6. Pet. 87.

Patent Owner does not separately dispute Petitioner’s arguments and evidence that Yoshida discloses the additional limitation in claim 6. Based on the undisputed evidence presented in the Petition, Petitioner has demonstrated persuasively that Yoshida and/or Saxler disclose or suggest the subject matter recited in claim 6. Ex. 1006 ¶¶ 10, 13, 21, Fig. 1, Abstract.

*f) Claim 7*

Claim 7 depends from claim 5 and recites that “the pair of self-aligned ledges are symmetric with respect to the gate metal.” Ex. 1001, 6:28–30. Petitioner argues that, as explained for limitation [1f], Yoshida as modified by Saxler includes p-type gate material that has symmetric ledges on either side of the gate material. Pet. 87–88.

Patent Owner does not separately address claim 7. Accordingly, for the same reasons discussed above with regard to claim 1 and claim 2, we find Petitioner has demonstrated persuasively that Yoshida and Saxler disclose or suggest the subject matter recited in claim 7.

*2. Conclusion*

For all of the foregoing reasons, we determine Petitioner has demonstrated by a preponderance of evidence that claims 1–7 are unpatentable as obvious in view of the combined disclosures of Yoshida and Saxler.

*F. Remaining Unpatentability Challenges*

Having determined that Petitioner establishes by a preponderance of the evidence that claims 1–7 are unpatentable as obvious in view of Yoshida

and Saxler, we do not address Petitioner’s additional grounds challenging claims 1–7. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (nonprecedential) (“We agree that the Board need not address [alternative grounds] that are not necessary to the resolution of the proceeding.”).

### III. CONCLUSION

After reviewing the complete record developed during the course of the trial, we conclude that Petitioner has satisfied its burden of demonstrating, by a preponderance of the evidence, that claims 1–7 of the ’335 patent are unpatentable.<sup>15</sup>

In summary:

<b>Claim(s)</b>	<b>35 U.S.C. §</b>	<b>Reference(s)/ Basis</b>	<b>Claim(s) Shown Unpatentable</b>	<b>Claim(s) Not Shown Unpatentable</b>
1–7	103	Yoshida, Saxler	1–7	
1–7	103	Saxler <sup>16</sup>		

<sup>15</sup> Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. §§ 42.8(a)(3), (b)(2).

<sup>16</sup> As explained above, we do not reach this ground in view of our determination that the challenged claims are unpatentable as obvious in view of Yoshida and Saxler.



<b>Claim(s)</b>	<b>35 U.S.C. §</b>	<b>Reference(s)/ Basis</b>	<b>Claim(s) Shown Unpatentable</b>	<b>Claim(s) Not Shown Unpatentable</b>
1–7	103	Saxler, Yoshida <sup>17</sup>		
2, 5–7	103	Saxler, Yoshida, Beach, Shenoy <sup>18</sup>		
1–7	103	Yoshida <sup>19</sup>		
2, 5–7	103	Yoshida, Saxler, Beach, Shenoy <sup>20</sup>		

#### IV. ORDER

For the reasons given, it is:

ORDERED that, Petitioner established by a preponderance of evidence that claims 1–7 of the '335 patent are unpatentable; and

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<sup>17</sup> As explained above, we do not reach this ground in view of our determination that the challenged claims are unpatentable as obvious in view of Yoshida and Saxler.

<sup>18</sup> As explained above, we do not reach this ground in view of our determination that the challenged claims are unpatentable as obvious in view of Yoshida and Saxler.

<sup>19</sup> As explained above, we do not reach this ground in view of our determination that the challenged claims are unpatentable as obvious in view of Yoshida and Saxler.

<sup>20</sup> As explained above, we do not reach this ground in view of our determination that the challenged claims are unpatentable as obvious in view of Yoshida and Saxler.

IPR2023-01384

Patent 10,312,335 B2

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2023-01384  
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