UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01384
U.S. Patent No. 10,312,335

PATENT OWNER'S PRELIMINARY RESPONSE

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I. INTRODUCTION

In accordance with 37 C.F.R. § 42.107, Patent Owner Efficient Power Conversion Corporation ("EPC" or "Patent Owner") submits this preliminary response to the Petition (the "Petition" or "Pet.") filed by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. ("Petitioner") for *Inter Partes* Review of claims 1-7 of U.S. Patent No. 10,312,335 (the "'335 patent"). Patent Owner respectfully requests that the Board deny the Petition for at least the reasons set forth below.

The '335 Patent relates to an enhancement mode GaN MISFET with self-aligned ledges comprised of p-type gate material. As explained below, these ledges, in conjunction with side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, provide the advantageous effect of reducing gate leakage current during operation.

As demonstrated below, none of the prior art references cited in the Petition teach or disclose these ledges and horizontally extending side surfaces to form an enhancement mode device. Indeed, it is this combination of features that provide the benefits described in the '335 Patent and innovate over preexisting designs at the time of the invention.

Accordingly, for the reasons explained below, Petitioner has not established that there is a reasonable likelihood that at least one of the challenged claims of the '335 patent is unpatentable, and the Petition should be denied.

II. BACKGROUND

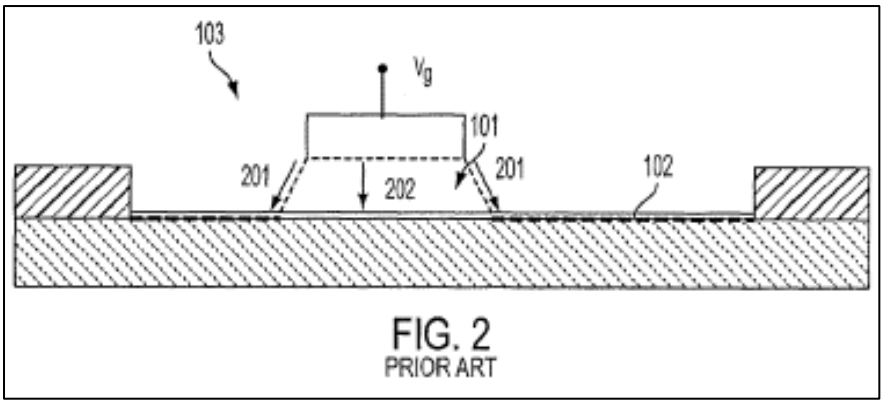
A. The '335 Patent

The '335 Patent issued on June 4, 2019 from an application filed on July 20, 2017. The '335 Patent arose from an application that was a divisional application from the application that became U.S. Patent No. 9,748,347. Therefore, the '335 Patent claims priority to a United States Provisional Applications filed on August 1, 2013, as well as claims priority through U.S. Patent No. 8,890,168 to a United States provisional patent application filed on April 8, 2009, which also led to the U.S. Pat. No. 8,404,508 ("the '508 Patent").

The '335 Patent describes and claims an enhancement mode GaN (Gallium Nitride) MISFET (Metal Insulator Semiconductor Field Effect Transistor) with a self-aligned ledge. GaN transistor devices may be categorized into two different categories: (1) depletion-mode FETs and (2) enhancement-mode FETs. *See* '335 Patent at 1:54-63. *See id*. Depletion-mode FETs maintain an "ON" state at zero gate-source voltage (normally ON), while enhancement mode FETs maintain an "OFF" state at zero gate source voltage (normally OFF). *See id.* Depletion-mode FETs deplete the 2DEG located near the junction of two layers having different

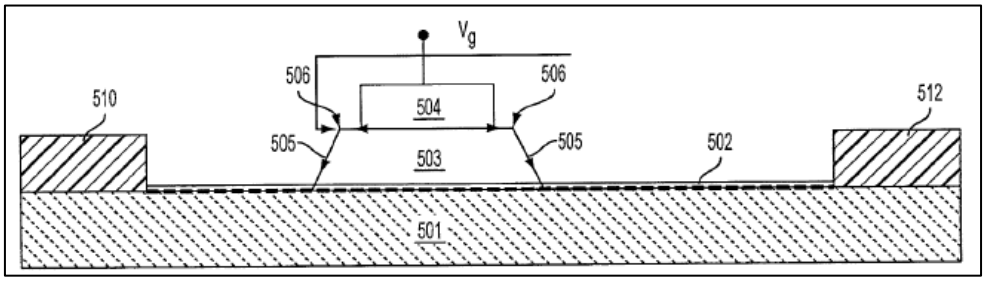
band gaps. *See id.* In the depletion-mode FETs, an electron channel that exists at zero gate voltage is depleted by applying a negative gate voltage, thereby turning the FET OFF. *See id.* Conversely, enhancement-mode FETs have no electron channel at zero gate voltage, but an electron channel can be induced by applying a positive gate voltage, thereby turning the FET ON. *See id.*

The '335 patent explains that a gate leakage current in GaN high electron mobility transistors occurs between the gate contact above gate material 101 and the 2DEG region 102 below and adjacent to the gate material along gate leakage current paths 201 (along the sidewalls of gate material 101) and 202 (through the bulk of gate material 101). *See id.* at FIG. 2 (reproduced below); 2:5-8. It was further identified that the gate leakage current of the prior art structure occurs predominantly along gate leakage current path 201, e.g., along the edge of the gate material. *See id.* at FIGs. 3A, 3B, and 4 (demonstrating that an increased number of gate p-type semiconductor sidewall edges increases the gate leakage current).



'335 Patent at Fig. 2

GaN FETs are known for their ability to carry greater current and withstand higher voltages than their silicon counterparts. In particular, the '335 Patent, as shown below, innovatively teaches a gate structure with an elongated surface length that reduces the gate leakage from the device. Due to the enhanced surface length of the elongated ledges and sidewalls of the device, there is a lower gate leakage during operation. The gate leakage current can be reduced by lengthening the gate leakage current path at the edges of the gate p-type semiconductor material by including a pair of ledges that extend horizontally towards the source and drain contacts, as shown in Fig. 5 (reproduced below). The '335 Patent describes the ledges as self-aligned. *See id*. at 2:46-48.



'335 Patent at FIG. 5.

In FIG. 5 above, the gate p-type semiconductor material 503 is positioned below the gate metal 504 and above barrier layer 502. In some embodiments, the barrier layer is formed of AlGaN. *See id*. at 3:46-48. Gate p-type semiconductor material 503 includes ledges 506 on each side of gate metal 504. The sidewalls of gate metal 504 define a width of the gate metal which is narrower than the width of

the narrowest portion of gate p-type material 503. The width of gate metal 504 being narrower than gate p-type material 503 effectively forms a pair of horizontal ledges 506 at the top of gate p-type material 503. The sidewalls, or edges, of the gate p-type material, which track reference number 505, extend respectively towards the source and drain material. In this embodiment, the narrowest portion of gate material 503 is at the top of the gate p-type material, from where the sidewalls of the gate p-type material descend towards the barrier layer, and the width of the gate p-type material increases.

B. Grounds of challenge

The petitioner challenges the patentability of the claims of the '335 patent on six grounds:

Ground 1: Claims 1-7 are challenged as being obvious over *Saxler* in view of the knowledge of a POSA.

Ground 2: Claims 1-7 are challenged as being obvious over *Saxler* in view of *Yoshida*.

Ground 3: Claims 2 and 5-7 are challenged as being obvious over *Saxler* in view of *Yoshida, Beach,* and *Shenoy*.

Ground 4: Claims 1-7 are challenged as being obvious over *Yoshida* in view of the knowledge of a POSA.

Ground 5: Claims 1-7 are challenged as being obvious over *Yoshida* in view of *Saxler*.

Ground 6: Claims 2 and 5-7 are challenged as being obvious over *Yoshida* in view of *Saxler*, *Beach*, and *Shenoy*.

III. CLAIM CONSTRUCTION

Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Without waiving its right to submit proposed claim constructions in a Patent Owner Response, Patent Owner submits that the Board need not engage in any pre-institution claim construction. However, Patent Owner notes the following errors in Petitioner's proposed claim constructions.

A. Petitioner Improperly Imports Limitations from the Specification to Construe the "Side Surface" Limitation

Petitioner incorrectly contends that the limitation, "side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer," in claims 1 and 5 of the '335 Patent, should be construed such that the bottom of the p-type gate material must be "more than 10% wider than the top of the material, leading to sloped side surfaces." Petition at p. 19.

The intrinsic evidence fails to mandate the additional restrictions Petitioner's proposed construction would seek to import into the claims. First, the only

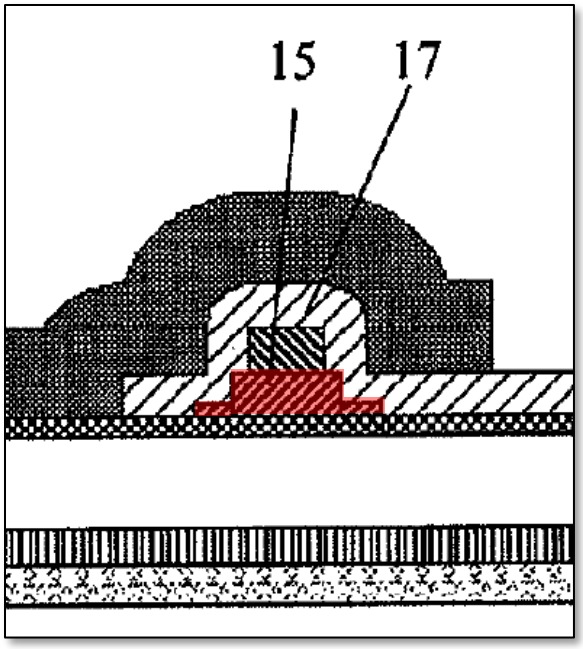
intrinsic support for Petitioner's proposed construction that the bottom of the p-type gate material must be "more than 10% wider than the top of the material" comes from one embodiment (the fourth) described in the specification. *See* '508 Patent at 5:23-28.[1] The claims at issue do not recite any numerical degree of horizontal extension for the claimed side surfaces or threshold values for the p-type gate material width compared to the top. And no such values are ***required*** by any intrinsic evidence. Simply put, there is no intrinsic evidence ***defining*** the horizontal extension of the side surfaces to have a minimum threshold value or unequivocally disavowing from the scope of the claims p-type gate materials where the side surfaces extend horizontally towards the source and drain contacts but where the bottom of those materials is less than 10% wider than the top. *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015) ("The standards for finding lexicography and disavowal are exacting.") (quotations omitted). Accordingly, Petitioner's proposed additional restriction that the bottom of the p-type gate material must be "more than 10% wider than the top of the material" improperly seeks to import a limitation from the specification into the

[1] The '508 Patent is incorporated by reference and the '335 Patent claims priority to the '508 Patent.

claim and should therefore be rejected. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005).

Second, there is no intrinsic support for Petitioner's proposed additional restriction that the claimed side surfaces must be "sloped." A sloped side surface is only one example of the type of side surface structure subsumed within the plain meaning of "side surfaces extending horizontally to the source and drain contacts." For example, side surfaces can be stepped towards the source and drain contacts, not sloped.

Limiting the claimed side surfaces to those that are "sloped" would read out embodiments from the '508 patent, which the '335 Patent incorporates by reference. As depicted below, Figure 12 of the '508 patent depicts a p-type gate material (15, annotated in red) where the bottom is wider than the top but where the side surfaces are stepped, not sloped.



'508 Patent, Fig. 12 (annotated)

Accordingly, Petitioner's proposal to limit the scope of the claims only to "sloped" side surfaces must be rejected.

Third, there is no intrinsic support for Petitioner's additional restriction that the sloped portion of the claimed "side surfaces" must contact the barrier layer. As discussed above, the claimed "side surfaces" need not be sloped but can alternatively be stepped towards the source and drain contacts. In such a configuration—even if the stepped side surface overall could be considered sloped—the portion of the side surface that contacts the barrier layer can be entirely vertical (i.e., have no slope), as shown in Figure 12 of the '508 patent above. Accordingly, Petitioner's proposal to limit the nature of the claimed barrier

layer contact only to the portion of the side surface that is "sloped" must be rejected.

B. Petitioner Improperly Construes "Self-Aligned" as a Product-by-Process Limitation

Petitioner incorrectly contends that the claimed "self-aligned ledges" term is a product-by-process limitation. Its strategy in doing so is clear—seeking to ease their burden on invalidity by ignoring the self-alignment process entirely, relying on the general rule that the validity of a product-by-process claim focuses "on the product and not the process of making it." *Greenliant Sys., Inc. v. Xicor LLC*, 692 F.3d 1261, 1268 (Fed. Cir. 2012). Petitioner, must however, consider self-alignment in the prior art because self-alignment, as used in claims 2 and 5 of the '335 patent, connotes a specific structure to the claimed GaN transistor and imparts structural and functional differences onto the claimed GaN transistor.

While the '335 Patent does identify a process for self-alignment, whether the term refers to a product made by a process does not end the inquiry into whether the "self-aligned ledges" term is a "product-by-process" limitation. A "product-by-process" claim is one in which the product is defined, at least in part, in terms of the method or process by which it is made. *Bonito Boats, Inc. v. Thunder Craft Boats, Inc.*, 489 U.S. 141, 158 n. *2 (1989) (citing D. Chisum, Patents § 8.05, p. 8–67 (1988)). The mere reference to a process in a product claim, however, does not render that claim a "product-by-process" claim. Instead, "if the process limitation

connotes specific structure and may be considered a structural limitation," then the so-called process limitation is considered structural. *In re Nordt*, 881 F.3d at 1374. This is because "words of limitation that can connote with equal force a structural characteristic of the product or a process of manufacture are commonly and by default interpreted in their structural sense, unless the patentee has demonstrated otherwise." *Id.* at 1375. Moreover, even if a particular limitation, on its face, is a product-by-process limitation, that process limitation is not made irrelevant "if the process by which [the claimed] product is made imparts 'structural and functional differences' distinguishing the claimed product from the prior art." *Greenliant*, 692 F.3d at 1268 (recognizing this as the "exception to th[e] general rule that the process by which the product is made is irrelevant" to an invalidity analysis) (citing *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1370 (Fed. Cir. 2009)). In assessing whether a process imparts structural or functional differences to the claimed product such that the process is entitled to patentable weight, the specification, the prosecution history, and any extrinsic evidence may be considered. *See Amgen*, 580 F.3d at 1365-67; *Purdue Pharma L.P. v. Epic Pharma, LLC*, 811 F.3d 1345, 1353-54 (Fed. Cir. 2016).

The term "self-aligned" ledges is not a product-by-process limitation because while the term may refer to a process, "intrinsic evidence demonstrates that the term connotes specific structure" onto the claimed GaN transistors. *Pacira*

Pharms. Inc. v. eVenus Pharms. Labs., Inc., Nos. 22-00718 & 21-19829, 2023 WL 3841559, at *9 (D.N.J. June 6, 2023). *Pacira* is instructive in confirming that the term "self-aligned" connotes specific structure onto the claimed GaN transistors and therefore is not a product-by-process limitation. In *Pacira*, the parties disputed whether the term "prepared by a commercial process" as it related to the preparation of bupivacaine, a numbing agent, encapsulated in multivescular liposomes (MVLs) to facilitate drug delivery into the body was a product-by-process limitation. 2023 WL 3841559, at *1, *9. The court found that the term connoted specific structure based on disclosure in the specification that, due to the claimed commercial process, the resulting drug product exhibited increased stability, contained less lipid degradation products, and exhibited increased encapsulation. *Id.* at *9. The court also agreed with the patentee's expert, who opined that the "prepared by a commercial process" term "informs a POSA about the structural properties of the claimed composition." *Id.* at *10 (internal quotations omitted). In short, both the intrinsic and extrinsic evidence in *Pacira* confirmed that the claimed process imparted structural characteristics onto the claimed composition, resulting in a better product compared to products not prepared by such commercial processes.

Like in *Pacira*, the specification here discloses the structural characteristics imparted by the process on the claimed product. The specification explains that

the "primary benefit" of self-alignment is that it "enable[s] the creation of a p-type gate with a minimum critical dimension ("CD")" and allows ledges to be created "that are symmetric to the gate metal disposed on the p-type gate material." '335 Patent at 3:65–4:3.

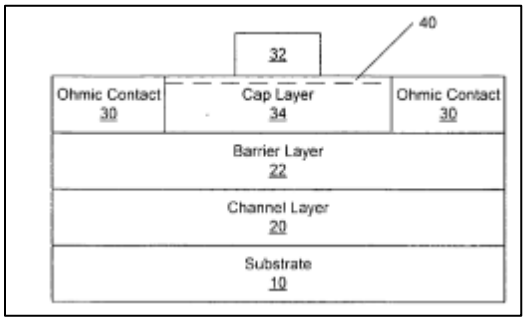
Nothing in the intrinsic evidence suggests that the "patentee has demonstrated" that the term "self-aligned" should be interpreted as a mere "process of manufacture." *In re Nordt*, 881 F.3d at 1374. Thus, although the term "self-aligned" refers to a process, because it also refers to a "structural characteristic" of the claimed product and a POSA would understand the process as imparting structural characteristics onto the claimed GaN transistor, the term must be "interpreted in [its] structural sense." *Id.* at 1374-1375 (finding the term "injection molded" is not product-by-process limitation because, although the application refers to the term as a process of manufacture, the term connotes structure to claimed knee braces). Self-alignment is a feature that differentiates the claimed transistor from prior art as none of the prior art before the Examiner disclosed self-aligned ledges of a p-type GaN gate material in a GaN transistor that also utilized elongated side surfaces. Moreover, the lack of any such prior art resulted in the issuance of claim 2 of the '335 patent, which depends from claim 1 and adds as its only additional limitation that the ledges are self-aligned, which confirms the

patentability of the feature over the prior art. Accordingly, the term "self-aligned ledges" is not a product-by-process limitation.

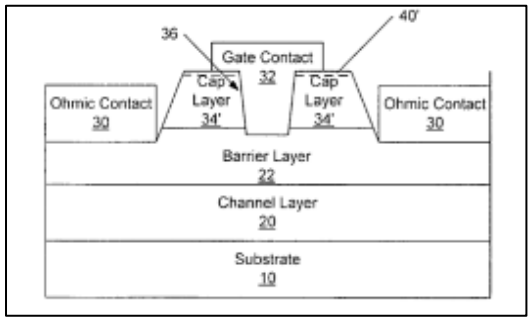
IV. OVERVIEW OF THE REFERENCES RELIED UPON BY PETITIONER

A. Saxler

Saxler describes a HEMT that includes a gallium nitride channel layer, also known as a buffer layer, and an aluminum gallium nitride barrier layer. *See Saxler* at ¶¶ [0058]-[0059]. *Saxler* further includes cap layer 34, 34', which is described as moving the top (outer) surface of the device physically away from the channel layer, which may reduce electrical effects of the surface. *See id.* at ¶ [0061], [0069]. The cap layer 34, 34' is shown as two distinct embodiments—one with a recessed gate structure (right) and one with a non-recessed gate structure (left). As can be seen, *Saxler* shows the recessed gate structure as two distinct regions on either side of the gate with slanted sidewalls and shows the non-recessed gate structure as a rectangle. *Saxler* does not describe any benefits of either gate structure or that its figures are representative of an intended device.



***Saxler* at FIG. 2A.**



***Saxler* at FIG. 2B.**

As can be seen from Figures 2A and 2B, *Saxler* describes a HEMT transistor having substrate 10 formed of a silicon carbide (SiC) substrate. *See id*. at ¶ [0053]. The channel layer 20 is positioned above substrate 10 and can be a gallium nitride (GaN) layer. *See id*. at ¶ [0053]. Adjacent and above the GaN channel layer is barrier layer 22, which can be preferably AlN, AlInN, AlGaN, or AlInGaN. *Id*. at ¶ [0059]. As known in the art at the time, the interaction between the barrier layer 22 and channel layer 20 induces carrier concentration at the interface. *Id*. As seen in the above Figures, the source and drain ohmic contacts 30 are located on opposite sides of the gate structure and graphically depicted as above the barrier layer.

Saxler describes its gate structure as including gate contact 32, made of nickel (Ni), platinum (Pt), nickel silicide ($NiSi_x$), copper (Cu), palladium (Pd), chromium (Cr), tungsten (W), and/or tungsten silicon nitride (WSiN). *See id*. at ¶ [0066]. The gate structure further includes cap layer 34, 34', which, in a particular embodiment, can be magnesium (Mg) doped GaN and/or a Mg-doped AlGaN. *Id*. at ¶ [0069]. In describing the cap layer, the alleged focus of *Saxler* is on doping the cap layer with p-type, n-type, or deep-level dopants. *Saxler* states:

> In further embodiments of the present invention, the outer surface of the cap layer of a nitride-based HEMT is doped with p-type, n-type or deep-level dopants such that the cap layer has a higher concentration of dopants at a surface of the cap layer that is remote from the barrier layer than at other regions of the cap layer. The cap layer may be a GaN based cap layer. The dopants at the outer surface of the device may

> segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations. The dopant may have different characteristics when at a dislocation than when in the bulk crystal. For example a shallow dopant in the bulk crystal may have characteristics of a deep level when at a dislocation.

Id. at ¶ [0049].

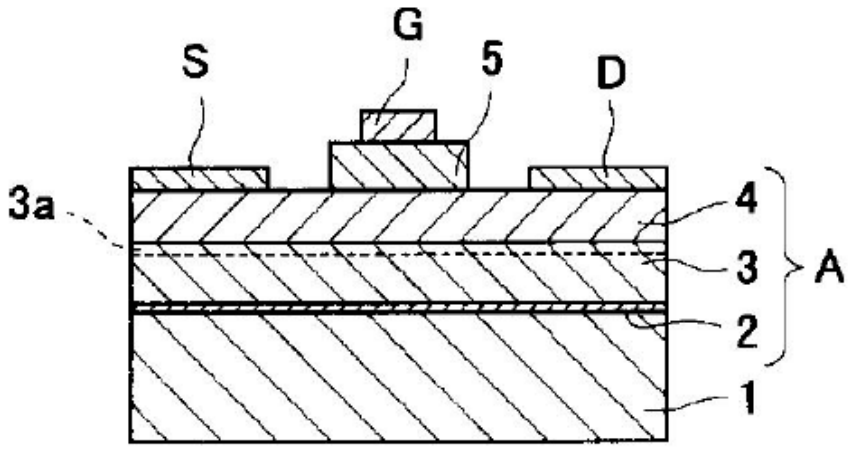
The above-referenced paragraph, among others, explains the purpose of doping the cap layer in *Saxler*: "The dopants at the outer surface of the device may segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations." *See id*. A person skilled in the art would have recognized that this purpose is unrelated and distinct from creating an enhancement mode transistor. Indeed, from the disclosure of *Saxler,* it is clear that *Saxler* does not claim to make an enhancement-mode transistor. Instead, *Saxler* purportedly advances the art to show that the intended interaction of the dopants is to segregate to dislocations to "reduce gate leakage along the dislocations."

Saxler does not explicitly disclose a process to fabricate its gate structure beyond a general description of a potassium hydroxide (KOH) etching step that makes regions for source and drain contacts. Rather, *Saxler* describes that the cap layer may be provided by conventional epitaxial growth techniques and that the gate contact may be added using "conventional fabrication techniques. *Id*. at ¶¶ [0063], [0066]. *Saxler* describes the general knowledge in the field of "gate-last" processes in which the source and drain contacts are formed first followed by the

gate contact. *See e.g., Saxler* ¶¶ [0064]-[0066]. Because *Saxler* teaches the use of multiple photo masks, it does not disclose a self-aligned (single photo mask) process for gate formation. *Saxler* does not disclose or suggest how to etch its cap layer or intended structural designs or configurations for its cap layer. *Only with respect to forming the ohmic contacts 30*, *Saxler* describes a "patterned mask and etch process may be used to expose the underlying barrier layer." *Id*. at ¶ [0064]. *Saxler*, however, does not disclose whether a dry or wet etching or patterning process is used to form the cap layer.

B. Yoshida

Yoshida discloses an enhancement mode GaN HEMT, with a P-GaN layer under the gate contact.



***Yoshida* Fig. 1**

The enhancement mode GaN HEMT of *Yoshida* is comprised of a semi-insulating substrate (1), a buffer (GaN) layer (2), an i-type semiconductor (GaN)

layer (3), an n-type semiconductor (InGaN) layer (4), and a p-type GaN layer (5). *Yoshida* at p. 7. As shown in *Yoshida*'s FIG. 1 above, the p-type GaN layer has vertical sidewalls.

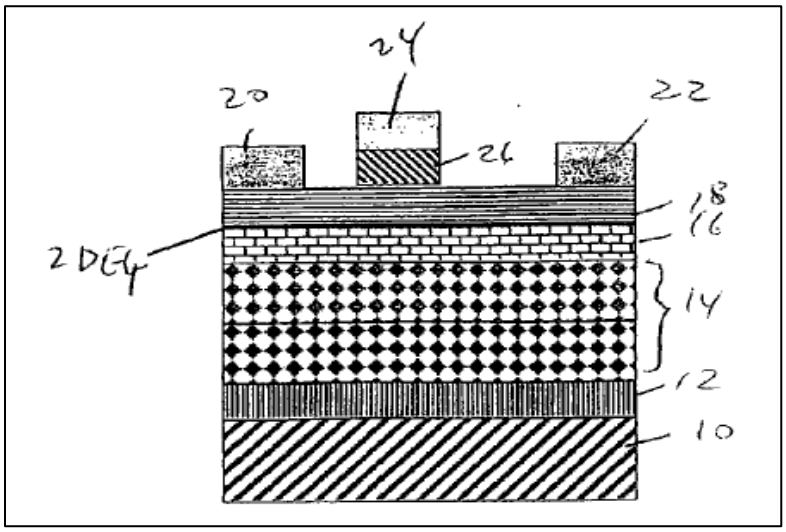
The enhancement mode GaN HEMT of *Yoshida* is made by a process in which the gate structure is formed *after* forming the source and drain contacts (e.g., a "gate-last" process). Specifically, *Yoshida* discloses the following process:

1. grow layers 2-5 over the substrate 1;
2. etch away the p-GaN layer 5 except where the gate electrode is to be loaded;
3. deposit a dielectric layer (SiO_2) to cover the entire surface, including the p-GaN layer 5;
4. apply photo resist/mask, open areas in the dielectric layer for the source S and drain D electrodes;
5. deposit Al in the openings to form the source S and drain D electrodes on the AlGaN barrier layer;
6. remove the mask and open the SiO2 film over the gate p-GaN material 5, leaving the source S and drain D electrodes masked.
7. deposit Au in the opening to form the gate electrode G and form the gate contact above the p-GaN layer to produce an enhancement mode GaN transistor.

Yoshida at ¶¶ [0019]-[0023].

C. Beach

Beach describes an alleged III-Nitride enhancement-mode semiconductor device, including a gate barrier layer under the gate. *Beach* at Abs., Title. *Beach* describes a transistor (image below) including substrate 10, bonding layer 12, first III-N buffer body 14, first III-N semiconductor body 16, second III-N semiconductor body 18, first and second power electrodes 20, 22, gate barrier 26, and gate arrangement 24. *See id*. at ¶¶ [0031]-[0032]. In a preferred embodiment, gate barrier 26 is an AlInGaN alloy, which can be, for example, AlGaN. *Id*. at ¶ [0032]. In preferred embodiments, first III-N semiconductor body 16 is AlGaN and second III-N semiconductor body 18 is GaN. *Id*. *Beach* describes the equivalent of a 2DEG region formed at the heterojunction of first III-N semiconductor body 16 and second III-N semiconductor body 18, as identified in the below figure.



***Beach* at FIG. 1.**

Beach further describes the formation of its gate structure. The gate structure of gate arrangement 24 and gate barrier 26 are patterned and etched using a single photo mask and result in a self-aligned gate arrangement. *Id*. at ¶ [0040]. *Beach* describes fabricating the gate structure *before* the ohmic contacts 20, 22 are formed on the device. *See, e.g.*, *id*.

D. Shenoy

Shenoy is an article exploring the theoretical shape evolution that occurs in through-mask electrochemical micromachining (EMM) through mathematical modeling. *Shenoy* at Abstract. *Shenoy* is not directed to the formation of GaN based semiconductors and/or HEMTs. *Shenoy* further does not disclose or suggest methods of manufacturing an enhancement-mode GaN transistor. *Shenoy* further does not address self-aligned structures.

Instead, *Shenoy* theoretically explores how deviations in photoresist mask wall angle affect the directionality of the subsequent etching process. Further, because *Shenoy* is based on a mathematical model, its disclosure relies upon theoretical assumptions that would not necessarily be applicable in practice, or true with respect to enhancement-mode GaN transistors and their applicable materials. *See, e.g.*, *id*. at 544-45. Particularly, *Shenoy* describes the shape of an ideal evolving EEM etching cavity but does not explicitly or implicitly instruct a POSA how to etch a GaN-based layer, any particular desired patterning designs, or

methods or desires to achieve particular sidewall designs. Instead, *Shenoy* is entirely ambivalent to any desired design. Further, *Shenoy* does not disclose or suggest that its etching methods or theoretical mathematical results would be applicable to GaN based materials.

V. THE BOARD SHOULD DENY INSTITUTION OF GROUND 1 (SAXLER ALONE)

In Ground 1, Petitioner asserts that *Saxler* alone renders obvious claims 1-7 of the '335 Patent. Petition, pp. 24-25. As explained below, Petitioner misinterprets and misrepresents the teachings of *Saxler*.

A. *Saxler* does not Teach or Disclose an Operational Enhancement-Mode Transistor

Saxler describes two different embodiments of its cap layer, a bifurcated recessed cap layer where the gate contact intersects and divides the cap layer (FIG. 1A), and an alternative non-recessed gate contact positioned higher than the cap layer (FIG. 1B), as shown below.

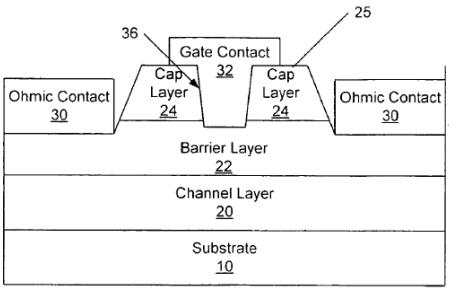


Figure 1A

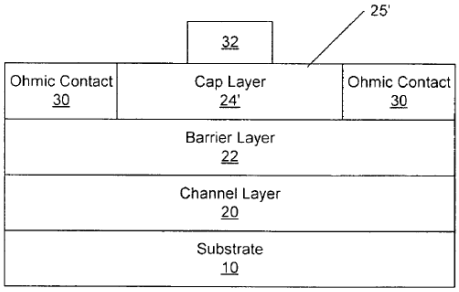
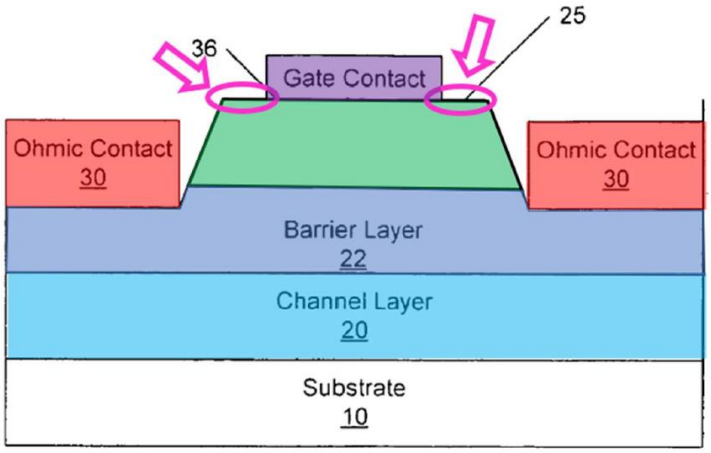


Figure 1B

Although the specification does not describe with any specificity the configuration of the cap layer and its sidewalls, in the bifurcated recessed embodiment, the cap layer is generally depicted in the figures as having slanted sidewalls. In the non-recessed cap layer embodiment, however, the cap layer is depicted exclusively as a rectangular layer between the source and drain contacts. *Saxler* does not describe that these two embodiments can be combined or how to manufacture an alleged combined embodiment.

Petitioner acknowledges that both independent claims 1 and 5 of the '335 Patent recite "[a]n enhancement-mode GaN transistor…" Petition at pp. 1, 8. Petitioner further acknowledges that *Saxler* does not actually disclose an enhancement-mode device. *See id.* at p. 33 (requiring modification to "turn *Saxler*'s device into an enhancement mode device…") Because *Saxler* does not disclose an enhancement-mode device, Petitioner proposes the below structure as a purported enhancement-mode device. That structure, represented by a hypothetical diagram below, has been designed solely based on hindsight by the Petitioner and does not appear anywhere in *Saxler*. Further, this hypothetical device would not function as an enhancement-mode device. Instead, if attempting to function as an enhancement-mode device, it would be non-operational due to its inability to induce a 2DEG between the ohmic contacts.



Saxler, Fig. 1A (modified).

Petition at p. 26.

The "p-type cap layer" (green, above) in the device created and proposed by Petitioner, and not described in *Saxler*, reaches all the way from source to drain, including the so-called access regions between the source and gate, and between gate and drain. *See above*. Indeed, even assuming that *Saxler* disclosed such a device (and it does not), the lower endpoint of the sloped side coincides with the edge of the ohmic contact (30) (indicating the two are aligned). An enhancement-mode device operates by depleting the 2DEG below the gate contact for a certain portion of the distance between the source and drain. In Petitioner's hypothetical embodiment, the depletion of both access regions (between the gate contact and each of the ohmic contacts) will result in the complete absence of the 2DEG all the way from source to drain. When applying a voltage, the gate contact could only induce a 2DEG substantially under the gate, that is, in the middle. Thus, to the

extent that the transistor is intended to operate as an enhancement-mode transistor, the transistor would always lack a 2DEG in the access regions (between source and gate and between gate and drain). Furthermore, the 2DEG could not be induced in the access regions. Without a 2DEG, such a transistor will not work properly and could not be switched to its ON state, thereby rendering the hypothetical device non-functional as an enhancement-mode device, as recited in independent claims 1 and 5 of the '335 Patent.

B. *Saxler* does not Teach or Disclose a P-Type Gate Material Having Side Surfaces Extending Horizontally Towards the Source Contact and Drain Contact, Respectively, and Contacting the Barrier Layer

Saxler describes two distinct embodiments of a recessed and non-recessed gate contacts, and only based on impermissible hindsight would a POSA be motivated to modify the two distinct embodiments identified by Petitioner. *Saxler* describes either a recessed gate with a bifurcated cap layer having sloped sidewalls, due to forming the gate recess, or a rectangular cap layer without sloped sidewalls *See id*.

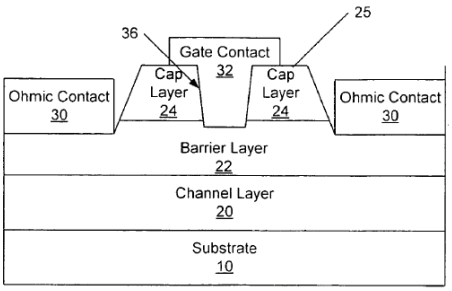


Figure 1A

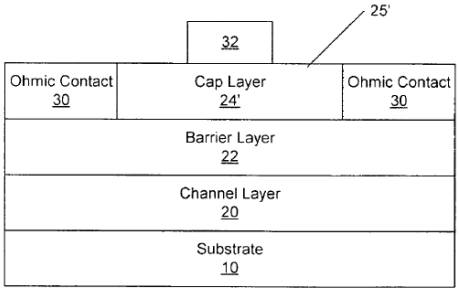


Figure 1B

There is no motivation for a POSA to modify *Saxler* to achieve a singular p-type gate material with sidewalls extending towards both the source and drain contacts, in the manner suggested by Petitioner in its hypothetical device. Therefore, neither *Saxler*'s bifurcated embodiment nor its unibody embodiment can teach or suggest "a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer," as recited in independent claims 1 and 5 of the '335 Patent.

Although sloped sidewalls may exist in the prior art, sloped sidewalls *together* with top surface ledges were not known as of the priority date of the '335 Patent. Indeed, Petitioner has not cited to any evidence teaching benefits to elongated surface ledges prior to the priority date of the '335 Patent for enhancement mode gallium nitride transistors including a p-type gallium-nitride based gate semiconductor material.

Furthermore, as discussed above, the KOH etching process described in *Saxler* does not necessarily apply to the formation of its cap layer. In addition, as *Saxler* does not teach or describe a benefit of sloped walls, a POSA seeking to use a non-recessed gate contact would not understand *Saxler* as teaching a unibody gate material with sloped sidewalls, as shown in Petitioner's hypothetical diagram. *Saxler* chose to depict its non-recessed embodiment without sloped sidewalls, and

therefore a POSA may have understood that forming the opening for the recessed gate – if anything – also formed the sloped sidewalls on the gate structure. Petitioner's hypothetical modifications to *Saxler*, combining a non-recessed gate with ledges and sloping sidewalls, are therefore nothing more than hindsight.

C. *Saxler* does not Teach or Disclose a Pair of Horizontal Ledges that Have Substantially Equal Widths from the Sidewalls of the Gate Metal to the Side Surfaces of the P-Type Gate Material or are Self-Aligned

Saxler does not teach or disclose a "pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively," as recited in independent claim 1 or "a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively," as recited in independent claim 5. Although the illustrative representation of Petitioner's hypothetical diagram shows the sidewalls as largely equidistant, in practice, a POSA would recognize that some unintended misalignment almost always occurs in the practice of forming these structures and the structure described in *Saxler* would not have self-aligned or even substantially equal sidewalls. *Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) ("Under our precedent, however, it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue."); *see also In re Wright*, 569 F.2d 1124, 1127

(CCPA 1977). This is due to unavoidable unintentional misalignment, for example, overlay deviations, when using multiple photo masks, as taught in *Saxler*. *Saxler* describes the general knowledge in the field of "gate-last" processes in which the source and drain contacts are formed first followed by the gate contact. *See e.g.*, *Saxler* ¶¶ [0064]-[0066]. Such processes will always lead to some unavoidable or accidental misalignment, and thus to unequal length ledges, to the extent ledges are included.

Petitioner identifies no prior art teaching or disclosure elongating the external length of the surface of the gate semiconductor material or any methods, means, or desires for having substantially equal length ledges. Indeed, there is no evidence in the record that p-type gate materials having ledges on the top surface and side surfaces extending towards the gate and source contacts were known prior to the '335 Patent. Petitioner relies solely on its hypothetical diagram as evidence for ledges of substantially equal length, and that diagram is based solely on hindsight. Moreover, that hypothetical diagram does not demonstrate the ledges are substantially equal, as that conclusion is based entirely on the way the diagram is drawn, rather than any concrete evidence. Indeed, the use of multiple photo masks in *Saxler* teaches the opposite – that the purported ledges *will not* be substantially equal in length and certainly not self-aligned.

Saxler does not actually describe, teach, or suggest ledges having substantially equal length. Instead, *Saxler* describes a process including etching the p-type material to form regions for the ohmic contacts and then subsequently depositing the gate contact metal above the etched p-type material *See Saxler* at ¶¶ [0064]-[0066]. This type of process results in misalignments in the positioning of the gate contact such that any resulting ledges would not have substantially equal widths. Moreover, *Saxler* does not disclose or suggest a motivation to achieve substantially equal width ledges on the p-type gate material. Indeed, this is not surprising given that *Saxler*, as described above, is focused on doping the cap layer instead of the structural design of the gate structure. Therefore, based on the teachings of *Saxler*, a POSA would not have been motivated to achieve the claimed gate structure, as recited in independent claims 1 and 5 of the '335 Patent.

VI. THE BOARD SHOULD DENY INSTITUTION OF GROUND 2 (SAXLER IN VIEW OF YOSHIDA)

In Ground 2, Petitioner asserts that *Saxler* in view of *Yoshida* renders obvious claims 1-7 of the '335 Patent. Petition, pp. 29. As explained above, Petitioner misinterprets and misrepresents the teachings of *Saxler*. Furthermore, as explained below, *Yoshida* does not rectify the deficiencies of *Saxler*.

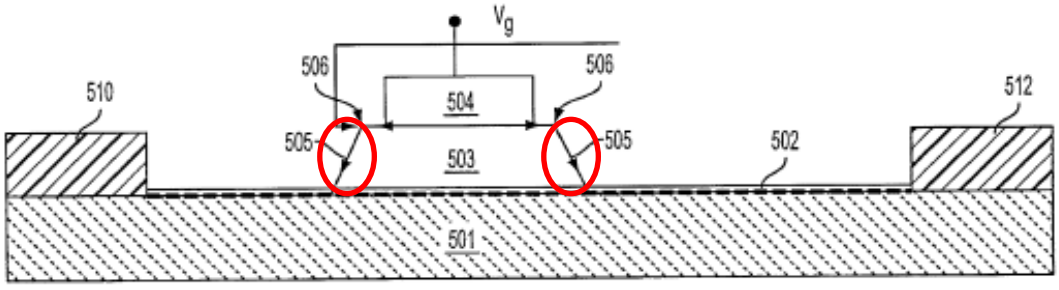
A. Neither *Saxler* nor *Yoshida* Teach or Disclose Side Surfaces that Extend Horizontally Toward the Source and Drain Contact

For at least the reasons in Section V.B, *Saxler* does not teach or disclose a p-type gate material "having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer," as recited in independent claims 1 or 5. *Yoshida* does not remedy that deficiency.

As shown in annotated FIG. 5 of the '335 Patent below, the p-type gate material's side surfaces (circled in red), as recited in independent claims 1 and 5, are such that the bottom of the p-type gate material is wider at the bottom than at the top. The '335 Patent notes:

> As indicated by the arrows (denoted by reference numbers **505**) shown on ledges **506** and the side surfaces of the p-type gate material **503**, when a positive voltage V_g is applied to the gate metal **504**, the gate current path **505** first travels horizontally along the upper edge of the p-type gate material **503** and, once it reaches the ledges **506**, the current path **505** follows the diagonal path along the edge of the p-type gate material **503**. This structure results in reduced gate leakage current as discussed below with respect to FIG. 8.

'335 Patent at 4:3-12 (emphasis added).

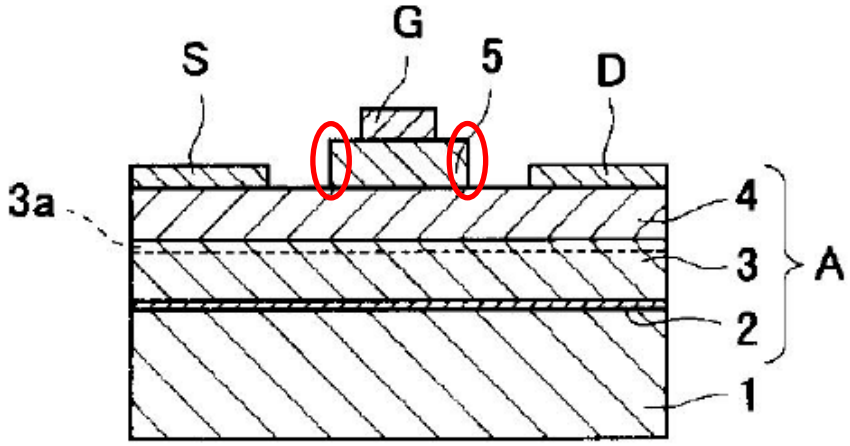


'335 Patent, Fig. 5 (annotated)

That interpretation is further supported by the disclosure of the '508 Patent, which is incorporated by reference and to which the '335 Patent claims priority. The '508 Patent identifies a number of embodiments in which the side surfaces extend horizontally, including FIG. 10 (showing sloped side surfaces) and FIG. 12 (showing stepped side surfaces). '508 Patent at FIGs. 10, 12; 5:52-60; 6:15-23. In those embodiments, the side surfaces of the p-type gate material are such that the bottom of the material is wider than the top of the material, a fact that Petitioner concedes, as well.[2] Petition at pp. 19-21.

Yoshida does not teach or disclose the side surfaces, as claimed in the '335 Patent. As shown in FIG. 1 of *Yoshida* below, the p-type GaN layer (5) does not have side surfaces that extend horizontally towards the source and drain contact, respectively, as required by independent claims 1 and 5, because the p-type GaN layer (5) of *Yoshida* is rectangular, such that its side surfaces (circled in red below) do not extend horizontally.

[2] Petitioner, however, improperly imports a limitation from a single embodiment into the claim, arbitrarily requiring that the bottom be 10% wider than the top of the p-type gate material.



***Yoshida* Fig. 1 (annotated)**

As shown, the side surfaces of the p-type GaN of *Yoshida* are vertical - they do not extend horizontally. Therefore, they cannot teach or disclose side surfaces that extend horizontally towards the source and drain contact, as recited in independent claims 1 and 5.

B. Neither *Saxler* nor *Yoshida* Teach or Disclose a Pair of Horizontal Ledges that Have Substantially Equal Widths from the Sidewalls of the Gate Metal to the Side Surfaces of the P-Type Gate Material or are Self-Aligned

Further, as explained in Section V.C, *Saxler* does not teach or disclose that the p-type gate material has ledges that are self-aligned or even ledges that have substantially equal widths from the sidewalls, as recited in independent claims 1 and 5. *Yoshida* does not remedy that deficiency.

As noted above, Petitioner relies solely and improperly upon the appearance of *Saxler*'s purported ledges in its FIG. 1A as evidence that the ledges have

substantially equal widths, as required by independent claim 1, or self-aligned ledges, as required by independent claim 5. But the Federal Circuit makes it clear that the appearance of drawings may not form the basis of such a quantitative determination. *Hockerson-Halberstadt, Inc.*, 222 F.3d at 956.

Yoshida does not disclose or teach that limitation of claims 1 and 5 for the same reasons, as its FIG. 1 provides only the appearance of substantially equal widths and provides no disclosure related to self-alignment of its gate structure. *Yoshida* is focused on the "use of a pn junction structure between the gate electrode and the channel layer, forming a two-dimensional electron gas layer with excellent electron trapping effect at the junction interface between i-type and n-type semiconductor layers," rather than concerned with the alignment of the gate and the p-type GaN layer. *Yoshida* at ¶ [0025]. Indeed, as explained above, *Yoshida* discloses that the gate is deposited *after* removal of the photoresist mask. *Id.* at ¶ [0023]. Such a process means that there is no evidence that the gate metal is self-aligned with respect to the side surfaces of the p-type gate material or even that any effort is taken to ensure that the gate is formed such that ledges of substantially equal width are formed. Absent that evidence, *Yoshida* simply discloses the previously known prior art and is therefore incapable of teaching a p-type gate material has ledges that are self-aligned or even ledges that have

substantially equal widths from the sidewalls, as recited in independent claims 1 and 5.

C. There is No Motivation to Combine *Saxler* with *Yoshida*

Saxler, as explained above, is directed to a device that is inoperable in enhancement mode. By contrast, *Yoshida* is directed to an enhancement mode device. Petitioner provides no motivation as to why a POSA would choose to incorporate features from a device that cannot operate in enhancement mode (*Saxler*) into a preexisting, operable enhancement mode device (*Yoshida*). As explained above, enhancement mode devices are structurally and functionally different from depletion mode devices. A POSA would therefore find no motivation to combine features from one with the other, as what is favorable to enhancement mode operation could be detrimental to depletion mode, and vice versa.

Petitioner also provides no motivation as to why a POSA would incorporate elements from the depletion mode, recessed gate transistor of *Saxler* into the enhancement mode, non-recessed gate transistor of *Yoshida*, as those devices are, again, substantially different. A POSA would not select features from *Saxler*'s recessed gate device to incorporate into *Yoshida*'s non-recessed gate device, absent impermissible hindsight.

VII. THE BOARD SHOULD DENY INSTITUTION OF GROUND 3 (SAXLER IN IEW OF YOSHIDA, BEACH, AND SHENOY)

In Ground 3, Petitioner asserts that *Saxler* in view of *Yoshida, Beach,* and *Shenoy* renders obvious claims 2 and 5-7 of the '335 Patent. Petition, p. 57. As explained above, Petitioner misinterprets and misrepresents the teachings of *Saxler*. Furthermore, as explained below, none of *Yoshida*, *Beach*, nor *Shenoy* rectify the deficiencies of *Saxler*.

A. A POSA would not have Found it Obvious to Combine *Saxler, Beach,* and *Shenoy*

None of *Saxler*, *Beach*, and *Shenoy* teach or disclose a "pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively," as recited in independent claim 1 or "a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively," as recited in independent claim 5, at least because it is not obvious to combine those references, absent impermissible hindsight. Initially, as explained in Section VI above, *Yoshida* does not remedy the deficiencies of *Saxler*.

Beach similarly cannot be applied to *Saxler*'s deficiencies because *Beach* discloses a "gate-first" fabrication process, which is incompatible with *Saxler*, which discloses a "gate-last" fabrication process. *Saxler* describes fabricating the gate structure *after* its cap layer is already fabricated. *See Saxler* at ¶¶ [0064]-

[0066]. Therefore, a POSA would not have found it obvious to pattern *Saxler*'s gate contact *and* cap layer using a self-aligned process as *Saxler* has already described patterning the cap layer, and therefore, could not rely upon a self-aligned process after the patterning has already been completed. Moreover, *Saxler* describes patterning and depositing the ohmic metals prior to the gate contact ("gate-last process"). *See Saxler* ¶¶ [0064]-[0066]. A POSA would also have not sought to incorporate *Beach*'s self-aligned "gate-first" process into *Saxler*.

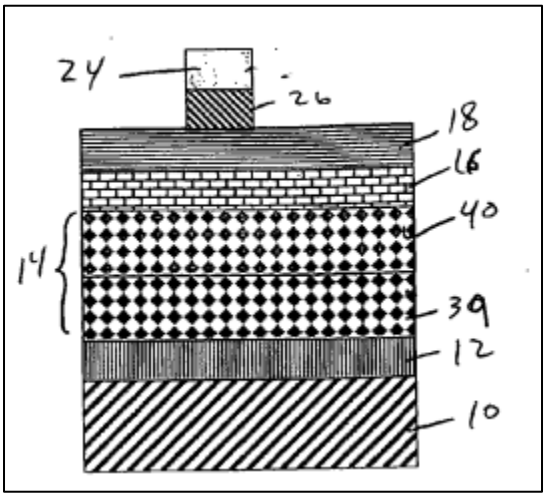
Second, a POSA would not have sought to incorporate *Beach*'s self-aligned "gate-first" process into *Saxler* because of the different structures between *Saxler* and *Beach*. As shown below, a POSA would have known that *Beach* describes a substantially different layer sequence and device structure, and the teachings would not have been adapted into *Saxler*. *Beach* describes the specific use of N-polar (nitrogen polar) orientation, which is different from *Saxler*. *Beach* at ¶¶ [0033], [0065]. Due to the N-polar orientation of *Beach*, a POSA would not have used *Beach* as guidance to modify the teachings of *Saxler*. Further, because the devices described in each reference are substantially different, the teachings of *Beach* would not have been incorporated by a POSA into the structure and method of manufacture described in *Saxler*.

Although self-aligned structures, in general, were largely known as of the priority date of the '335 Patent, this fact would not have suggested combining the

teachings of *Saxler* and *Beach*. *Saxler* describes a transistor having either a recessed or non-recessed gate structure. *See, e.g.*, *Saxler* at FIGs. 2A, 2B. *Saxler* further describes etching regions for gate and source contact deposition prior to depositing the gate contact. *See id*. at ¶¶ [0064]-[0066]. It would not have been obvious to a POSA to modify *Saxler* to incorporate Beach's self-aligned process, because the different structure and methods of manufacture involved could not be effectively combined.

As discussed above, *Saxler* describes a patterning step of the cap layer prior to deposition of the gate contact. *Beach* teaches the opposite – forming the gate contact first. While *Saxler* requires such patterning to deposit the ohmic metals, *Beach* does not address this issue prior to forming the structure (as shown below in Figure 2F of *Beach* illustrating a gate structure formed without source and drain contacts). That is, the *Saxler* process is a gate-last process, whereas the *Beach* is a gate-first process. A POSA would have only sought to modify *Saxler* to incorporate a self-aligned process if relying upon hindsight based on the teachings of the '335 Patent. The processes and structures are substantially different, and there is no justification for a POSA to have sought to incorporate the self-aligned process of *Beach* into *Saxler*. Indeed, a POSA would not look at a structure in the abstract but rather in the context of a manufacturing process. Moreover, a POSA

would restrict himself / herself to structures that can actually be made. In that context, *Beach* cannot be combined with *Saxler* to arrive at the claimed invention.



***Beach* at FIG. 2F**

There are significant differences in the process of *Saxler* and *Beach* which would lead a POSA to not view the self-aligned process taught by *Beach* as applicable to the gate design disclosed by *Saxler* or to Petitioner's hypothetical gate design based on *Saxler*. Specifically, *Beach* does not include the illustrated ledges of *Saxler* in either of its disclosed embodiments. Petitioner attempts to overcome this deficiency by asserting *Shenoy*'s isotropic etching technique would have been an obvious substitution, but Petitioner does not identify any motivation based on any of *Saxler*, *Beach*, or *Shenoy* to apply *Shenoy*'s technique after a self-aligned process. Further, Petitioner does not address how a POSA would have proceeded to manufacture the ledges depicted in *Saxler* using the process described in *Shenoy* after a self-aligned etching process has already occurred, and in particular whether this would require an additional photo mask. Based on *Saxler*

and *Beach*, a POSA would not have realized that ledges could be achieved through a self-aligned process.

Additionally, as explained above, a POSA would not have considered the teachings of *Shenoy* applicable to *Saxler* or the subject matter of the '335 Patent. Petitioner asserts a POSA would have found it obvious to use *Shenoy*'s isotropic etching technique, but does not address the differences in structures or teachings of the references. Even if a POSA would have considered *Shenoy*, *Shenoy* does not address subsequent etching of a previously etched device or provide guidance to a POSA to deposit a new photo mask on an etched material to perform the isotropic etching. A POSA therefore would not have found it obvious to combine *Shenoy* with *Saxler* and *Beach* as proposed by Petitioner.

B. *Shenoy* is Non-Analogous Art and May Not be Combined with *Saxler*, *Yoshida*, or *Beach*

Shenoy involves electrochemical etching – etching with an applied voltage, an applied electric field, and an electrical current flowing. However, because *Saxler* does not describe the conductivity of its materials, a POSA would not have considered *Shenoy* to modify the teachings of *Saxler*, because *Shenoy* describes electrochemical etching, a highly specialized etching method with little relevance to the process described in either the '335 Patent or *Saxler*. Indeed, electrochemical etching can only be used in conjunction with conductive materials,

and therefore would not have been considered based upon the KOH etching described in *Saxler*.

Although *Shenoy* generally describes an isotropic etching process, a POSA would not have considered the materials used and the structure etched in *Shenoy* to be related to either *Saxler* or *Beach*. First, *Shenoy* does not address self-alignment or how to etch a material below a hard mask. Instead, *Shenoy* solely addresses the verticality of the photoresist during etching and its effect on the resulting EEM etching process. And second, *Shenoy* does not address materials relevant to *Saxler* or the '335 Patent and therefore any etching process would have been significantly different from the etching process proposed by *Saxler* and not considered as a substitution. Indeed, a POSA would have recognized that an unduly significant amount of experimentation would be required to attempt *Shenoy*'s etching process in *Saxler* (with no expectation of success) and for this reason a POSA would not have sought to apply the EEM process of *Shenoy* to *Saxler*. Therefore, although *Shenoy* describes isotropic etching, its technology and the application are substantially different from *Saxler* and would not have been considered by a POSA.

VIII. THE BOARD SHOULD DENY INSTITUTION OF GROUND 4 (YOSHIDA ALONE)

In Ground 4, Petitioner asserts that *Yoshida* alone renders obvious claims 1-7 of the '335 Patent. Petition, pp. 67. As explained below, Petitioner misinterprets and misrepresents the teachings of *Yoshida*.

As explained above in Section VI, *Yoshida* does not teach or disclose at least two limitations from independent claims 1 and 5: (1) a p-type gate material "having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer;" and (2) p-type gate material has ledges that are self-aligned or even ledges that have substantially equal widths from the sidewalls.

Beyond a vague reference to "manufacturing tolerances" (Petition at pp. 67-68), Petitioner provides no evidence that a POSA would understand the vertical side surfaces of the p-GaN layer (5) of *Yoshida* to have a wider bottom surface than top surface. Indeed, there is no evidence that *Yoshida* contemplated such a design for its p-GaN layer. As such, *Yoshida* does not render obvious independent claims 1 or 5 of the '335 Patent.

IX. THE BOARD SHOULD DENY INSTITUTION OF GROUND 5 (YOSHIDA IN VIEW OF SAXLER)

In Ground 5, Petitioner asserts that *Yoshida* in view of *Saxler* renders obvious claims 1-7 of the '335 Patent. Petition, p. 69. As explained above,

Petitioner misinterprets and misrepresents the teachings of *Yoshida*. Furthermore, as explained below, *Saxler* does not rectify the deficiencies of *Yoshida*.

As explained above in Sections V and VI, neither *Saxler* nor *Yoshida* teach or disclose: (1) a p-type gate material "having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer;" or (2) p-type gate material has ledges that are self-aligned or even ledges that have substantially equal widths from the sidewalls, as recited in independent claims 1 and 5.

Relying solely on hindsight, Petitioner attempts to shoehorn the recessed gate embodiment of *Saxler* (FIG. 1A), which is *not* an enhancement-mode device, into the enhancement-mode device of *Yoshida* (FIG. 1). Petition at pp. 69-70. Such a combination is not merited. Petitioner does not establish why a POSA would choose to incorporate features from a device that cannot operate in enhancement mode (*Saxler*) into a preexisting, operable enhancement mode device (*Yoshida*). As explained above, enhancement mode devices are structurally and functionally different from depletion mode devices. A POSA would therefore find no motivation to combine features from one with the other, as what is favorable to enhancement mode operation could be detrimental to depletion mode, and vice versa.

Petitioner also does not establish why a POSA would incorporate elements from the depletion mode, recessed gate transistor of *Saxler* into the enhancement mode, non-recessed gate transistor of *Yoshida*, as those devices are, again, substantially different. A POSA would not select features from *Saxler*'s recessed gate device to incorporate into *Yoshida*'s non-recessed gate device, absent impermissible hindsight. As such, claims 1-7 of the '335 Patent are not rendered obvious by *Yoshida* in view of *Saxler*.

X. THE BOARD SHOULD DENY INSTITUTION OF GROUND 6 (YOSHIDA IN VIEW OF SAXLER, BEACH, AND SHENOY)

In Ground 6, Petitioner asserts that *Yoshida* in view of *Saxler*, *Beach*, and *Shenoy* renders obvious claims 2 and 5-7 of the '335 Patent. Petition, p. 88. As explained above, Petitioner misinterprets and misrepresents the teachings of *Yoshida*. Furthermore, as explained below, none of *Saxler*, *Beach*, nor *Shenoy* rectify the deficiencies of *Yoshida*.

As explained above in Sections V and VI, neither *Saxler* nor *Yoshida* teach or disclose: (1) a p-type gate material "having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer;" or (2) p-type gate material has ledges that are self-aligned or even ledges that have substantially equal widths from the sidewalls, as recited in independent claims 1 and 5. Moreover, as explained in Section VI, there is no motivation to combine *Yoshida* with *Saxler* because *Saxler* does not disclose an

operational enhancement mode device and requires the specious combination of a recessed gate device with a non-recessed gate device.

Furthermore, as explained in Section VII, *Beach* discloses a "gate-first" process, which cannot be combined with *Saxler*'s "gate-last" process. *Yoshida* similarly describes such a "gate-last" process, in which "Au was deposited in the opening portions [of the source and drain electrodes]" and then "gate electrode D were loaded above the p-type GaN layer 5 to fabricate the HEMT shown in FIG. 1." *Yoshida* at ¶ [0023]. Therefore, for the same reasons as *Saxler*, *Yoshida* cannot be combined with *Beach*.

Finally, as explained in Section VII.B, *Shenoy* discloses electrochemical etching, a process that is non-analogous art to those used to fabricate the device of the '335 Patent. As such, a POSA would not choose to combine its teachings with any of *Saxler*, *Yoshida*, or *Beach*.

For at least those reasons, *Yoshida* in view of *Saxler*, *Beach*, and *Shenoy* do not render obvious claims 2 and 5-7 of the '335 Patent.

XI. RESERVATION OF RIGHTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if IPR is instituted. Similarly, Patent Owner does not concede any underlying contentions in the

Petition and reserves the right to rebut any such contention later. Further, Patent Owner is not limited to the arguments presented in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented herein.

XII. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and no *inter partes* review should be instituted.

Dated: December 28, 2023

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER's PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 8,878 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

Dated: December 28, 2023

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CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

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