

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BMW OF NORTH AMERICA, LLC,
Petitioner,

v.

FORAS TECHNOLOGIES LTD.,
Patent Owner.

IPR2024-01347
Patent 7,624,302 B2

Before WILLIAM V. SAINDON, THOMAS L. GIANNETTI, and
RUSSELL E. CASS, *Administrative Patent Judges*.

GIANNETTI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

BMW of North America, LLC (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review (“IPR”) of claims 1–27 (the “challenged claims”) of U.S. Patent No. 7,624,302 B2 (Ex. 1001, “the ’302 patent”).

Foras Technologies Limited (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”). Patent Owner’s Preliminary Response does not address the merits of Petitioner’s challenge to patentability. Instead, Patent Owner contends that the Board should exercise its discretion to deny institution of *inter partes* review under 35 U.S.C. § 325(d) because the Petition is based on prior art and arguments that were already presented to the USPTO and expressly considered during prosecution. *See* Prelim. Resp. 1–8.

We have authority to determine whether to institute review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). An *inter partes* review may not be instituted unless it is determined that “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

For the reasons provided below, we determine, based on the record before us, there is a reasonable likelihood Petitioner would prevail in showing at least one of the challenged claims is unpatentable. Furthermore, we deny Patent Owner’s request that we exercise our discretion to deny institution in this proceeding under 35 U.S.C. § 325(d). We therefore institute *inter partes* review on all claims and all grounds. *See SAS Inst. Inc.*

v. Iancu, 584 U.S. 357 (2018); 37 C.F.R. § 42.108(a) (“When instituting . . . review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”).

B. Related Matters

Patent Owner identifies the following current district court proceedings involving the ’302 patent: *Bayersiche Motoren Werke AG, et al. v. Foras Technologies Ltd.*, No. 1:24-cv-00363 (E.D. Va.); *Foras Technologies Limited. v. Nissan Motor Company, Ltd., et al.*, No. 1:23-cv-00640 (W.D. Tex.). Paper 4, 2.

Petitioner identifies the following additional district court proceedings involving the ’302 patent: *Foras Technologies Ltd. v. Toyota Motor North America, Inc.*, No. 2:23-cv-00321 (E.D. Tex.); *Foras Technologies Limited v. Toyota Motor North America, Inc. et al.*, No. 2:23-cv-00150 (E.D. Tex.). Pet. 79.

The parties also identify the following USPTO proceeding involving the ’302 patent: *Ex Parte* Reexamination Control No. 90/019,243, filed by Unified Patents (USPTO). Pet. 79; Paper 4, 2.

C. The ’302 Patent (Ex. 1001)

The ’302 patent discloses a method comprising detecting loss of lockstep (LOL) for a processor in a multi-processor system, determining that the processor for which the LOL is detected is assigned the role of boot processor, and switching the role of boot processor to a spare processor without shutting down the system’s operating system. Ex. 1001, code (57).

The ’302 patent describes that “[t]he traditional response to detected LOL has been to crash the system to ensure that the detected error is not

propagated through the system.” Ex. 1001, 3:13–16. According to the ’302 patent, “crashing the system each time LOL is detected is not an attractive proposition,” especially for large systems having many processors. *Id.* at 3:19–25. As a solution, the ’302 patent describes techniques for recovering from LOL detected for a boot processor in a multi-processor system, in which a spare processor is utilized for such recovery by assuming the role of boot processor. *Id.* at 4:60–5:5.

The ’302 patent describes a multi-processor system storing information (a “device tree”) that “identifies the processor in the system that is the boot processor and identifies the processor that is the spare for the boot processor.” Ex. 1001, 5:40–44. The ’302 patent also describes that the system’s firmware can access such information, and “upon detecting LOL for the boot processor, determines the spare processor from the device tree and assigns the spare processor the role of boot processor.” *Id.* at 5:44–48. According to the ’302 patent, “[t]he firmware then attempts to recover lockstep for the processor for which LOL was detected,” and “[i]f the recovery of lockstep is successful, the processor for which lockstep was recovered (i.e., the former boot processor) may be assigned the role of spare for the current boot processor.” *Id.* at 5:48–53. In this way, the ’302 patent explains, “the multi-processor system may recover from LOL detected for the boot processor without requiring a crash of the system (at least for certain types of ‘recoverable’ LOLs).” *Id.* at 5:53–56.

According to the ’302 patent, the spare processor for the boot processor may be a “hot” spare processor, which “is held in reserve, idling until such time as it assumes the role of boot processor responsive to detected LOL for the boot processor.” Ex. 1001, 5:57–63. Alternatively, the spare processor may be an “active” processor that is not held in reserve, but

“is made available to the OS for executing instructions during normal system operation,” and “[u]pon LOL being detected for the boot processor, [it] is dynamically transformed into a hot spare (i.e., it is idled) such that it can assume the role of the boot processor.” *Id.* at 5:63–6:2.

According to the ’302 patent, its embodiments “enable the role of boot processor to be dynamically switched, during system runtime, to a spare processor responsive to a detected LOL for the boot processor, thus enabling recovery from the LOL without requiring that the system be crashed or re-booted.” Ex. 1001, 18:65–19:3.

D. Illustrative Claims

Claims 1–27 (all claims) are challenged. Claims 1, 13, 21, and 26 are independent. Claims 1 and 26 are illustrative of the claimed subject matter and are reproduced below.¹

[1 preamble] A method comprising:

[1a] detecting loss of lockstep (LOL) for a processor in a multi-processor system;

[1b] determining that the processor for which said LOL is detected is assigned a role of boot processor;

[1c] changing a system identifier, used by the system’s operating system to recognize the boot processor, of said boot processor for which said LOL is detected, to a different value, which causes the system’s operating system to not recognize the processor for which said LOL is detected as the boot processor; and

[1d] changing a system identifier of the spare processor to that of the boot processor, thereby switching the role of boot processor to a spare processor without shutting down the system’s operating system.

¹ Paragraph labeling provided by Petitioner has been added in brackets. *See* Pet. i–ii, vi.

[26 preamble] A system comprising:

[26a] system firmware means for detecting loss of lockstep (LOL) for a processor in a multi-processor system;

[26b] system firmware means for determining whether the processor for which said LOL is detected is assigned the role of boot processor; and

[26c] system firmware means for switching the role of boot processor to a spare processor without shutting down the system's operating system if determined that the processor for which said LOL is detected is assigned the role of boot processor.

Ex. 1001, 19:6–20, 21:5–22:5, p. 18 (Certificate of Correction).²

E. Prior Art and Other Evidence

The Petition relies on the following references:

Name	Reference	Date	Exhibit No.
Fox	US 2005/0172164 A1	Filed Jan. 21, 2004	1005
Safford	US 2004/0006722 A1	Jan. 8, 2004	1006
Arai	US 2006/0036889 A1	Filed Aug. 16, 2004	1007
Landry	US 5,408,647	Apr. 18, 1995	1011
Bigbee	US 2003/0126498 A1	July 3, 2003	1012

In addition, Petitioner submits the Declaration of Dr. Michael C. Brogioli in support of its Petition. Ex. 1002 (“Brogioli Decl.”).

² Unless otherwise specified, page citations to exhibits use the page numbers assigned by the parties and not the original page numbers.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–27 are unpatentable based on the following grounds (Pet. 1–2):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–25	103(a) ³	Fox, Safford, Arai
1–25	103(a)	Fox, Safford, Landry, Arai
26, 27	103(a)	Fox, Safford, Arai, Bigbee
26, 27	103(a)	Fox, Safford, Landry, Arai, Bigbee

G. Overview of the Prior Art

1. Fox (Ex. 1005)

Fox is titled “Autonomous Fail-Over to Hot-Spare Processor Using SMI.” Ex. 1005, code (54). Fox is directed to “a method and system for dynamically activating a spare processor when processor failure is detected in a multi-processor data processing system.” *Id.* ¶ 2. Fox describes a method and system for dynamically replacing a failing processor using Systems Management Interrupt (SMI) functionality provided within basic input output system (BIOS) of the IA-32 architecture.⁴ *Id.* ¶ 15. At least one processor of the multiprocessor system (MP) is initially provided as a reserve (or hot-spare) processor that remains in an idle, off, or low-power mode. *Id.* While in that mode, the OS is prevented from initially utilizing the hot-spare processor. *Id.* When a processor failure is detected, SMI code

³ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the ’302 patent asserts a filing date prior to the effective date of the applicable AIA amendment, we refer to the pre-AIA version of § 103.

⁴ IA (Intel Architecture)-32 refers to an architecture used by Intel in its Pentium and certain other microprocessors. *Barron’s Dictionary of Computer and Internet Terms* 244 (12th ed. 2017). Ex. 3001.

running on a good processor instructs the OS to hold off allocating processes to the failing processor. *Id.* Contemporaneously, the SMI (and OS) activates and completes an initialization of the hot-spare processor to prepare it to begin receiving the held-off processes. *Id.* Control is then returned to the OS, which updates the “active” processor list and allocates the threads that were running on the failing processor to the hot-spare processor. *Id.*

2. Safford (Ex. 1006)

Safford is titled “Method and Apparatus for Recovery from Loss of Lock Step.” Ex. 1006, code (54). Safford describes a computer system using lock-stepped processor cores that operate in a master/checker pair to improve reliability of processing assets. *Id.* ¶ 15. Each of the processors in the pair processes the same code sequences. *Id.* When a logic circuit compares the resulting outputs of the processors, any difference in the processor outputs indicates the existence of an error, prompting the logic circuit to initiate a sequence of steps to halt operation of the two processors. *Id.*

Figure 3 of Safford is reproduced below.

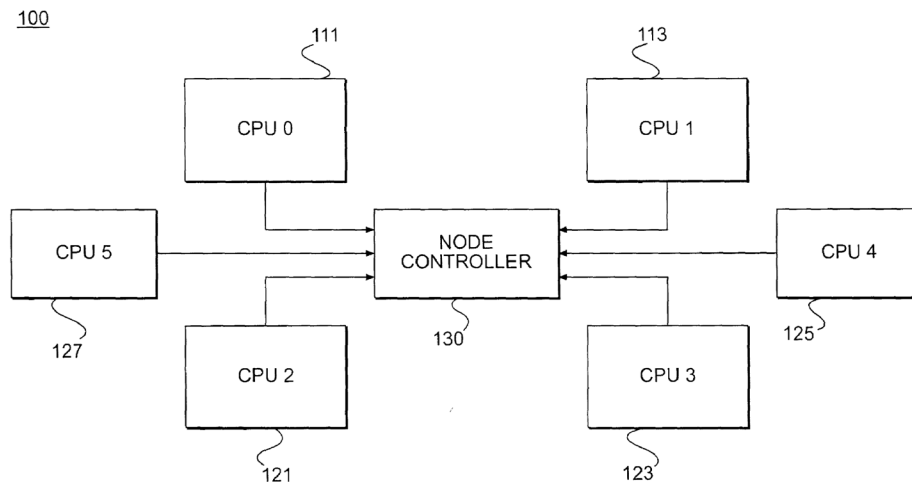


FIG. 3

Figure 3 depicts computer system 100 with processors 111, 113, 121, 123, 125, and 127 that operate as pairs when in lock step (i.e., processors 111 and 113 are a first pair; processors 121 and 123 are a second pair; and processors 125 and 127 are a third pair). Ex. 1006 ¶ 18. The processor pairs are coupled to a lockstep logic, connected to node controller 130. *Id.*

According to Safford, “[t]he processor 125 may be designated as a ‘hot standby,’ and is sitting idle in lock step mode with the processor 127.” *Id.* ¶ 20. “Should one of the processors 111, 113, 121, and 123 suffer an error, the hot standby processors 125, 127 may be used to speed recovery from the resulting loss of lock step.” *Id.*

3. *Arai (Ex. 1007)*

Arai is titled “High Availability Multi-Processor System.” Ex. 1007, code (54). *Arai* describes “a method and system for reserving a processor in a multiprocessor system for availability of replacement in response to detection of an error in a non-reserved processor.” *Id.* ¶ 2. According to *Arai*, “[w]hen a central processor in a multiprocessor system encounters an error, it is very desirable to not lose the work being done on that processor and to move that work to another processor that is still operating in the system.” *Id.* ¶ 5.

In *Arai*, during system initialization, one or more logical processors may be reserved in an inactive state. Ex. 1007, code (57). In the event an error is detected on a logical or physical processor, the execution context of the processor experiencing the error is transferred to one or more of the reserved logical processors. *Id.* Thereafter, the active processor is designated as inactive and replaced by the inactive processor to which the execution context has been transferred. *Id.*; *see also id.* ¶ 19.

Figure 4b of Arai is reproduced below.

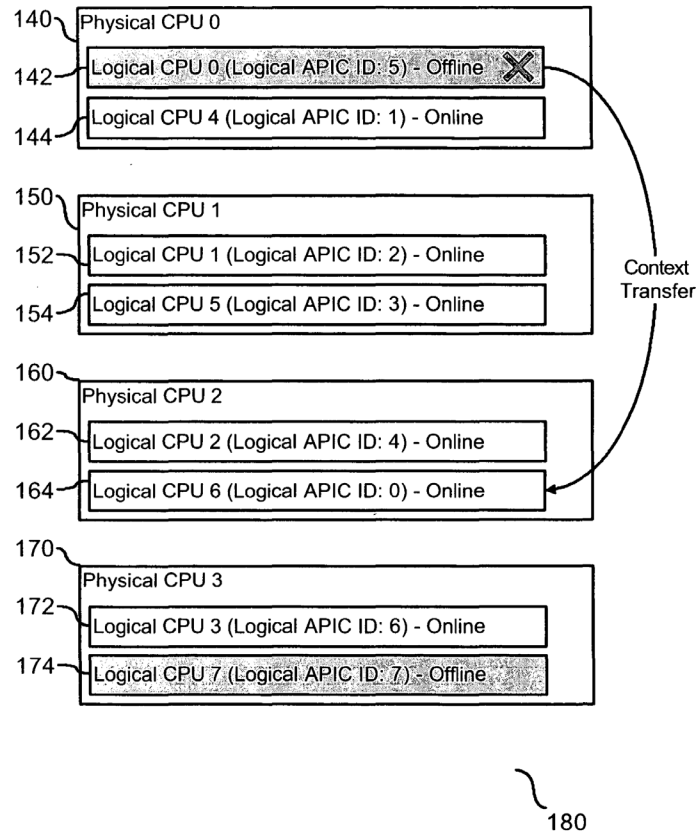


FIG. 4b

Figure 4b depicts the identification and status of each processor following occurrence of an error in a logical processor. Ex. 1007 ¶ 16. Following detection of an error with logical CPU₀ (142), logical CPU₀ is placed in an idle state and assigned the identification number of logical CPU₆ (164). *Id.* ¶ 23. At the same time, logical CPU₆ (164) is placed in an active state and assigned the identification number of CPU₀ (142). *Id.* In this way, in response to an error in an active processor, the execution context of the active processor may be transferred to an identified inactive processor, followed by activation of the processor that has received the execution context. *Id.* ¶ 25.

4. Landry (Ex. 1011)

Landry is titled “Automatic Logical CPU Assignment of Physical CPUs.” Ex. 1011, code (54). Landry relates to “startup logic for assigning logical central processing unit (CPU) designations among multiple CPUs.” *Id.* at 1:7–10.

Landry discloses a multiprocessor computer system that includes fault tolerant power up logic for finding a functioning CPU to operate as logical CPU0. Ex. 1011, 2:9–11. When the system is powered up, all of the CPUs except the CPU in physical slot 0 (CPU P0) are initially placed in a SLEEP mode. *Id.* at 2:15–18. The microprocessor in physical location 0 performs its power on self-test (POST) routine and tests its associated cache memory system. *Id.* at 2:18–20. If the CPU functions properly, the CPU is designated as CPU L0, and the microprocessor retains this designation until the system is power cycled. *Id.* at 2:20–23. The CPU designated as CPU L0 then awakens the remaining CPUs and boots up the rest of the computer system. *Id.* at 2:23–25.

If CPU P0 is not functioning properly, it is designated as inoperative. Ex. 1011, 2:26–27. The system then awakens CPU P1 and repeats the process of testing the CPU. If CPU P1 is operational, then it is designated as CPU L0, and it boots the remainder of the system. *Id.* at 2:27–31. On the other hand, if CPU P1 also fails, it is also given an inoperative designation. The computer system then turns on CPU P2, and repeats the process. *Id.* at 2:31–32. The process repeats until an operational microprocessor is found to perform the CPU L0 functions. *Id.* at 2:33–35. Consequently, if at least one of the microprocessors in the system is functioning, the computer system boots and operates. *Id.* at 2:35–37. Thus, the multiprocessor system is not

crippled by the failure of a single processor, enhancing the dependability of the computer system. *Id.* at 2:37–40.

5. *Bigbee (Ex. 1012)*

Bigbee is titled “Method and Apparatus for Functional Redundancy Check Mode Recovery.” Ex. 1012, code (54). Bigbee describes data processing systems where “two or more physical processing elements or ‘cores’ are associated with and function as a single logical processor.” *Id.* ¶ 2. Bigbee describes that “[t]he processor cores are operated in a functional redundancy check (FRC) mode in which identical instructions are provided to each core and concurrently executed on identical data so that any error occurring within a single core will produce an inconsistent result as compared to the remaining cores associated with a given processor.” *Id.* Specialized FRC logic performs this comparison and generates a signal such as an interrupt or exception once an inconsistent result has been detected. *Id.*

II. REQUEST FOR DENIAL OF INSTITUTION UNDER 35 U.S.C. § 325(d)

A. *Background*

As noted, Patent Owner argues that the Board should exercise its discretion to deny institution under 35 U.S.C. § 325(d).⁵ Prelim. Resp. 1–8. Patent Owner asserts that “the Petition is based on art and arguments that are the same and/or substantially similar to the art and arguments considered by

⁵ “[T]he Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d).

the USPTO during prosecution.” *Id.* at 1. Petitioner asserts that “[t]his Petition presents new prior art, grounds, and arguments not previously considered by the Office.” Pet. 74; *see also id.* at 75–77.

In evaluating arguments under § 325(d), we use a two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential). We must also consider the non-exclusive factors set forth in *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential in relevant part), which “provide useful insight into how to apply the framework” under § 325(d). *Advanced Bionics*, Paper 6 at 9. Those non-exclusive factors include:

- (a) the similarities and material differences between the asserted art and the prior art involved during examination;
- (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
- (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
- (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
- (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and

(f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson, Paper 8 at 17–18. “If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office, then factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office.”

Advanced Bionics, Paper 6 at 10.

For the reasons given below, we are not persuaded to exercise our discretion to deny the Petition based on § 325(d). Our discussion begins with the prosecution history of the ’302 patent and then proceeds with an analysis using the *Advanced Bionics* framework.

B. Prosecution History

The application for the ’302 patent (Serial No. 10/972,588) was filed on October 25, 2004. Ex. 1004, 275.

In a non-final Office Action mailed on September 12, 2007, the Examiner rejected all pending claims (application claims 1–30). Ex. 1004, 238–263. In addition to a double patenting rejection, the Examiner rejected application claims 1–4, 7, 9–23, and 29 under 35 U.S.C. § 102(e) as anticipated by Safford (U.S. Patent No. 7,085,959, Ex. 2002)⁶ and application claims 5, 6, 8, 24–28, and 30 under 35 U.S.C. § 103(a) as obvious over Safford and Marshall (U.S. Patent No. 5,915,082, Ex. 1022).

⁶ The Safford reference cited in the Petition (Ex. 1006) is identified as a prior publication of the Safford patent (Ex. 2002) cited during prosecution of the ’302 patent. Ex. 2002, code (65); *see also* Prelim. Resp. 1 n.1. Consistent with the parties’ usage, we refer to both the Safford patent and its published application as “Safford.”

Ex. 1004, 242–251 (rejections under § 102), 251–261 (rejections under § 103).

The applicants responded on December 12, 2007. Ex. 1004, 244–322. The response to the § 102 rejection over Safford argued that Safford is distinguishable from the then-pending claims reciting a “boot processor”: “Safford does not discuss boot processors, the system determining whether a processor is a boot processor, or switching the role of [the] boot processor from one processor to another.” *Id.* at 232. Responding to the § 103 rejection over Safford and Marshall, quoting 35 U.S.C. § 103(c),⁷ the applicants argued that “Safford is not a valid prior art reference that may be used in a rejection under 35 U.S.C. § 103(a).” Ex. 1004, 235.

In the next Office Action, on March 10, 2008, the Examiner allowed application claims 24–28 and rejected the remaining claims. Ex. 1004, 203. The Examiner repeated the § 102 rejection of application claims 1–4, 7, 9–23, and 29 over Safford. *Id.* at 204–209. The Examiner withdrew the § 103 rejection over Safford and Marshall and rejected application claims 1–23 and 29–30 over Quach (U.S. Patent 6,625,749) and Fox (U.S. Patent 7,251,749).⁸ *Id.* at 209–216.

⁷ Pre-AIA 35 U.S.C. § 103(c) provides: “Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title [35 U.S.C. § 102], shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person.”

⁸ The Fox reference cited in the Petition (Ex. 1005) is identified as a prior publication of the Fox patent (U.S. Patent 7,251,746, Ex. 2001) cited during prosecution of the ’302 patent. Ex. 2001, code (65); *see also* Prelim. Resp. 1

The Examiner did not address the applicants' argument based on § 103(c).

The applicants responded on June 5, 2008. Ex. 1004, 195–199. In response to the § 102 rejection over Safford, the applicants repeated their previous arguments that “Safford does not discuss a boot processor” and “Safford does not teach or suggest switching the role of [the] boot processor.” *Id.* at 197. In response to the § 103 rejection over Quach and Fox, the applicants admitted that their prior argument that Safford was not available as prior art “was not correct.” Ex. 1004, 197. Further, referring to the previous Office Action, the applicants again emphasized the boot processor recitation, asserting that “[n]othing in that discussion provides support for a combination of Quach and Fox teaching or suggesting boot processors or switching the role of boot processors.” *Id.* at 198.

The applicants' attorney conducted a telephonic interview with the Examiner on September 5, 2008. Ex. 1004, 164. The Examiner's Interview Summary indicates that Safford, Fox, and Quach were discussed and that agreement was reached. *Id.* The Examiner's summary does not provide any details about the arguments presented at the interview, only a brief description of the “general nature of what was agreed to.” *Id.*

On September 5, 2008, the applicants submitted an Amendment in Response to Phone Interview on 09/05/2008. Ex. 1004, 176–183. The amendment canceled certain claims (application claims 13–15) and amended others. The amendments further define the steps for “switching” the role of the boot processor for which an LOL is detected. For example, to

n.1. Consistent with the parties' usage, we refer to both the Fox patent and its published application as “Fox.”

application claim 1 (which issued as patent claim 1), the amendment added the following:

changing a system identifier, used by the system's operating system to recognize the boot processor, of said boot processor for which said LOL is detected, to a different value, which causes the system's operating system to not recognize the processor for which LOL is detected as the boot processor, and

changing the system identifier of the spare processor to that of the boot processor

Ex. 1004, 177. Similar amendments were made to another independent claim under rejection. *Id.* at 179 (amending application claim 16, which issued as claim 13). The remarks accompanying the amendment briefly address the § 102 rejection over Safford, pointing to the amendment, but do not discuss the merits of the Safford rejection or address the § 103 rejection over Quach and Fox. *Id.* at 182.

On September 23, 2008, the Examiner allowed the pending claims without further comment. Ex. 1004, 163 (Notice of Allowability). After several Requests for Continued Examination (RCEs) were filed citing additional prior art, the '302 patent issued on November 24, 2009. Ex. 1001, code (45).

C. Advanced Bionics Analysis

Part one of the *Advanced Bionics* framework asks whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office. *Advanced Bionics*, Paper 6 at 8. We disagree with Patent Owner that “the Petition is based on art and arguments that are the same and/or

substantially similar to the art and arguments considered by the USPTO during prosecution.” Prelim. Resp. 1.

Petitioner’s challenges to claims 1–25 of the ’302 patent are based on the combination of Fox, Safford, and Arai, or the combination of Fox, Safford, Landry, and Arai. *See* Pet. 1–2. It is undisputed that while the Examiner considered and discussed Fox and Safford during prosecution of the ’302 patent (*see id.* at 75; Prelim. Resp. 1 & n.1), Arai, Landry, and their combination with Fox or Safford, were not cited and therefore not considered by the Examiner.

Safford was first cited in a September 12, 2007 non-final Office Action that rejected all pending claims as anticipated under 35 U.S.C. § 102. Ex. 1004, 242–251. The applicants responded that “Safford does not discuss boot processors, the system determining whether a processor is a boot processor, or switching the role of [the] boot processor from one processor to another.” *Id.* at 232. In the next Office Action, the Examiner repeated the § 102 rejection over Safford. *Id.* at 204–209. The applicants again argued: “Safford does not discuss a boot processor” and “Safford does not teach or suggest switching the role of [the] boot processor.” *Id.* at 197.

As to Fox, when cited by the Examiner in a § 103 rejection with Quach on March 10, 2008, the applicants responded with an argument similar to that presented for Safford. Ex. 1004, 197–198. Referring to the March 10 Office Action, the applicants argued that “[n]othing in that discussion provides support for a combination of Quach and Fox teaching or suggesting boot processors or switching the role of boot processors.” *Id.* at 198. The prosecution record shows no further substantive arguments directed to Fox during the prosecution. *See* discussion of the prosecution history in Section II.B, *supra*.

Petitioner's grounds in this proceeding rely on additional prior art references and combinations of references that were not before the Examiner. Specifically, Petitioner challenges claims 1–25 based on two grounds not before the Examiner: (1) Fox, Safford, and Arai, and (2) Fox, Safford, Landry, and Arai. Pet. 1–2. Petitioner relies on the additional references Arai and Landry for teachings that the applicants asserted were missing from Safford and Fox during prosecution. For example, Petitioner relies on Arai for its teaching of switching processors: “Arai discloses replacing an active processor with an error with a reserved inactive processor.” *Id.* at 27 (citing Ex. 1007 ¶¶ 2, 8, 9, 19–24). Further, “Arai discloses switching the identification numbers of the active processor in error and the reserved inactive processor.” *Id.* at 28 (citing Ex. 1007 ¶¶ 22, 23, 25). In addition, Petitioner asserts that Landry teaches switching out a faulty boot processor: “Landry's fault-tolerant boot process dynamically designates a functional CPU as logical CPU0 that performs the unique functions of a boot processor.” *Id.* at 31. Further, “[a person of ordinary skill] would have understood the benefits of implementing Landry's boot processor selection in Fox.” *Id.*

In addition to not having the references themselves, the Examiner did not have the benefit of Dr. Brogioli's testimony regarding the combined teachings of these references. *See, e.g.*, Ex. 1002 ¶¶ 81–145 (testifying regarding obviousness of claim 1 over the combined teachings of Fox, Safford, and Arai, and over the combined teachings of Fox, Safford, Landry, and Arai).

Patent Owner asserts that “prior art considered by the Examiner already included similar disclosures to those of Arai regarding storing

configuration information in memory,” pointing to U.S. Patent No. 6,438,687 (“Klein”). Prelim. Resp. 5. We disagree.

Klein is titled “Method and Apparatus for Improved Storage of Computer System Configuration Information.” Ex. 2003, code (54). Klein was cited during prosecution of the ’302 patent in an IDS (Information Disclosure Statement), along with 30 other references. Ex. 1004, 145–146.

Patent Owner contends that Petitioner’s grounds “rely on Arai in a very limited role.” Prelim. Resp. 5. We disagree. As discussed *supra*, Petitioner relies on Arai for several teachings, most notably for its teaching of switching processors. Specifically, Petitioner asserts that “Arai discloses transfer[ring] of the execution context from the active processor that is experiencing the error to at least one of the inactive processors that has been designated to replace the active processor.” Pet. 29 (citing Ex. 1007 ¶¶ 22, 25) (alteration in original) (internal quotation marks eliminated). As noted *supra*, during prosecution the applicants argued that both Safford and Fox lack this teaching.

Furthermore, Arai and Klein are not cumulative; there are significant differences between them. Petitioner relies on Arai to teach details of “replacing an active processor [detected] with an error with a reserved inactive processor [in a multiprocessor system].” Pet. 27 (citing Ex. 1007, Abstract, ¶¶ 2, 8–9, 19–24); *see also id.* at 10, 18–20. In contrast, Klein describes switching memories. Klein describes a configuration ROM of a ROM module that has a backup copy of the system configuration parameters stored in a configuration CMOS RAM. Ex. 2003, code (57). Klein discloses that “[i]f the configuration CMOS RAM fails to provide valid configuration data, the contents of the configuration ROM are used to configure the computer system.” *Id.* For the reasons given, we find Arai’s

processor-switching implementation technique differs materially from Klein's *memory-switching* technique.

It is undisputed that Landry was not considered by the Examiner during prosecution. Yet, Patent Owner does not address Landry in its *Becton, Dickinson* analysis. See Prelim. Resp. 3–6. We find on this record that Landry is not substantially the same as the art relied upon during prosecution of the '302 patent, such as Fox or Safford. As is discussed *supra*, Petitioner asserts that Landry teaches switching out a faulty boot processor: “Landry’s fault-tolerant boot process dynamically designates a functional CPU as logical CPU0 that performs the unique functions of a boot processor.” See Pet. 31. Petitioner relies on Landry’s teaching of a “fault-tolerant process dynamically designat[ing] a functional CPU as logical CPU0 that performs the unique functions of a boot processor.” *Id.* Petitioner asserts that a person of ordinary skill in the art would have understood that implementing Landry’s process in Fox would have been beneficial because, *inter alia*, “logical CPU0 was a known and conventional identification of the boot processor” and “using the logical CPU0 as the identification for the boot processor allows for transparent replacement of the physical processor experiencing a failure with another processor without interrupting the operating system.” *Id.* at 31–32.

Patent Owner does not demonstrate that Landry is cumulative of Fox or Safford by showing a teaching similar to Landry’s designating a functional CPU as logical CPU0 that performs the functions of a boot processor in Fox or Safford. In fact, the applicants argued against such a disclosure in Fox and Safford during prosecution. Accordingly, we find for the reasons given that Landry is not cumulative of those references.

Patent Owner's assertion that each of Petitioner's challenges "presents essentially the same argument" considered during prosecution is likewise deficient. Prelim. Resp. 3–4. We note that with respect to the overlap between arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art, some overlap in arguments will likely always occur because the same claims are being analyzed. Here, we have an additional factor. During prosecution, to overcome a § 102 rejection over Safford and a § 103 rejection over Fox and Quach, Patent Owner amended the claims to add further details relating to changing the system identifiers of the boot processor and the spare processor in the switching operation. Ex. 1004, 176–181. In the remarks accompanying the amendment, the applicants did not address the § 103 rejection over Fox and Quach or present substantive arguments in opposition to the § 102 rejection over Safford. *Id.* at 182–183. An Examiner's Interview Summary indicates that a telephonic interview with the applicants' attorney took place before the amendment was filed, but presents no details on what arguments were presented by the applicants. Ex. 1004, 164. The Examiner allowed the claims shortly thereafter without further discussion. *Id.* at 160–163. As a consequence, the prosecution history does not reflect what arguments were presented by the applicants and considered by the Examiner in allowing the amended claims that appear in the patent.

As can be seen in the discussion above and the analysis of Petitioner's grounds below, Arai and Landry are significant to Petitioner's challenges. Because the Office did not previously consider all of the prior art references or combinations of references relied on in the Petition, including Arai and Landry, and because Arai and Landry are not the same or substantially the same as the art that was previously considered, we determine the Office did

not previously consider the same or substantially the same prior art as is relied on in the Petition. Further, we find that there is not a substantial overlap, if any, between the arguments made during examination and the manner in which Petitioner relies on the prior art, including Arai and Landry, as discussed above. Therefore, part one of the *Advanced Bionics* framework is not met, and we need not proceed to part two of the *Advanced Bionics* framework. *See Advanced Bionics*, IPR2019-01469, Paper 6 at 8.

D. Conclusion

There is new, noncumulative prior art asserted in the Petition, e.g., Arai and Landry. Patent Owner's arguments during prosecution were directed to other references and combinations.

For at least these reasons, we determine not to exercise our discretion under § 325(d) to deny the Petition on this basis.

III. ANALYSIS OF THE CHALLENGED CLAIMS

A. Claim Construction

In an *inter partes* review proceeding, the Board applies the same claim construction standard as is applied in federal courts in a civil action under 35 U.S.C. § 282(b), which is generally referred to as the *Phillips* standard. *See* 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Under the *Phillips* standard, “words of a claim ‘are generally given their ordinary and customary meaning.’” *Phillips*, 415 F.3d at 1312.

We construe only those claim terms and phrases necessary to our decision. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the

controversy.” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

1. *Means-Plus-Function Terms*

Challenged claim 26 recites elements using the word “means.” See Ex. 1001, 21:6–22:5. The use of the word “means” in a claim element creates a rebuttable presumption that 35 U.S.C. § 112 ¶ 6 applies.⁹ See *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (en banc in relevant part). Construing a means-plus-function claim term is a two-step process. We must first identify the claimed function. Then, we must determine what structure, if any, disclosed in the specification corresponds to the claimed function. *Id.* at 1351 (citation omitted). The parties do not dispute that 35 U.S.C. § 112 ¶ 6 applies to those “means” elements recited in claim 26. See Pet. 6–8; see generally Prelim. Resp.

a. “system firmware means for detecting loss of lockstep (LOL) for a processor in a multi-processor system” (Claim limitation [26a])

Petitioner contends that the function is “detecting loss of lockstep (LOL) for a processor in a multiprocessor system.” Pet. 7. Petitioner contends the corresponding structure is “firmware including a Processor Abstraction Layer (PAL), System Abstraction Layer (SAL), and Extended Firmware Interface (EFI), or equivalents thereof.” *Id.* (citations omitted).

Patent Owner does not dispute Petitioner’s position or discuss claim construction in its Preliminary Response.

⁹ Section 4(c) of the AIA re-designated 35 U.S.C. § 112, sixth paragraph, as 35 U.S.C. § 112(f). Because the application from which the ’302 patent issued was filed before the effective date of the relevant amendment, we refer to the pre-AIA version of § 112.

We are not aware of any controversy between the parties over this claim term's meaning that would affect this Decision. Therefore, we determine that at this stage, we do not need to expressly construe this claim term to resolve a controversy.

b. “system firmware means for determining whether the processor for which said LOL is detected is assigned the role of boot processor” (Claim limitation [26b])

Petitioner contends that the function is “determining whether the processor for which said LOL is detected is assigned the role of boot processor.” Pet. 7. Petitioner contends the corresponding structure is “firmware including a Processor Abstraction Layer (PAL), System Abstraction Layer (SAL), Extended Firmware Interface (EFI), and a device tree, or equivalents thereof.” *Id.* (citations omitted).

Patent Owner does not dispute Petitioner's position or discuss claim construction in its Preliminary Response.

We are not aware of any controversy between the parties over this claim term's meaning that would affect this Decision. Therefore, we determine that at this stage, we do not need to expressly construe this claim term to resolve a controversy.

c. “system firmware means for switching the role of boot processor to a spare processor without shutting down the system's operating system if determined that the processor for which said LOL is detected is assigned the role of boot processor” (Claim limitation [26c])

Petitioner contends the function is “switching the role of boot processor to a spare processor without shutting down the system's operating system if determined that the processor for which said LOL is detected is assigned the role of boot processor.” Pet. 7–8. Petitioner contends the

corresponding structure is “firmware including a Processor Abstraction Layer (PAL), System Abstraction Layer (SAL), and Extended Firmware Interface (EFI), or equivalents thereof.” *Id.* (citations omitted).

Patent Owner does not dispute Petitioner’s position or discuss claim construction in its Preliminary Response.

We are not aware of any controversy between the parties over this claim term’s meaning that would affect this Decision. Therefore, we determine that at this stage, we do not need to expressly construe this claim term to resolve a controversy.

2. Other Terms

Petitioner offers the following additional construction:

a. “*detecting loss of lockstep (LOL)*”/“*detect loss of lockstep (LOL)*”
(Claims 1, 13, 21, 26)

Petitioner argues that these terms “should be construed to include both mismatch errors and errors that may eventually result in mismatch errors constituting a ‘precursor to lockstep mismatch’—including at least one of (1) detecting a lockstep mismatch error; and (2) detecting an error that may eventually cause a lockstep mismatch error.” Pet. 6. Petitioner asserts that “[t]he specification provides detecting these two types of errors as examples of detection of LOL.” *Id.* (citing Ex. 1001, 2:40–3:6, 7:25–36; Brogioli Decl. ¶¶ 34–36). Petitioner further asserts that this construction “is consistent with the undisputed construction in the IPR challenging U.S. Patent No. 7,502,958.” *Id.* (citing *BMW of N. Am., LLC v. Foras Techs. Ltd.*, IPR2023-01373, Paper 18 at 2 (PTAB July 12, 2024)).

Patent Owner does not dispute Petitioner’s position or discuss claim construction in the Preliminary Response.

We are not aware of any controversy between the parties over the meaning of these claim terms that would affect this Decision. Therefore, we determine that at this stage, we do not need to expressly construe these claim terms to resolve a controversy.

3. Summary and Conclusion

For the reasons given, we determine that at this stage, we do not need expressly to construe any claim term for this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs.*, 200 F.3d at 803)).

H. The Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill at the time of the alleged invention “would have at least a bachelor’s degree in computer science, computer engineering, or equivalent, and at least two years of prior work experience with computer architecture design, including fault-tolerant computer architecture design,” and “[a]dditional education could substitute for professional experience and vice versa.” Pet. 4 (citing Brogioli Decl. ¶¶ 28–30). At this stage, Patent Owner does not respond to this contention.

For the purpose of institution, we adopt Petitioner’s definition of a person of ordinary skill in the art because it is consistent with the level of skill reflected by the ’302 patent specification and the asserted prior art.

I. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) if in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).¹⁰

J. Obviousness of Claims 1–25 Based on Fox, Safford, Landry, and Arai

Petitioner contends that claims 1–25 would have been obvious over Fox, Safford, and Arai (Pet. 9–30, 36–66), and alternatively, over Fox, Safford, Landry, and Arai (*id.* at 30–66).¹¹ Petitioner presents supporting testimony by Dr. Brogioli. Brogioli Decl. ¶¶ 81–239. At this stage, Patent Owner does not address the merits of Petitioner’s challenges.

1. Motivation to Combine Fox, Safford, and Arai and Fox, Safford, Landry, and Arai

Petitioner asserts that a person of ordinary skill “would have found it obvious to combine Fox’s multiprocessor system with Safford’s lockstep processor and error detection logics and Arai’s processor-switching

¹⁰ Patent Owner does not present evidence related to secondary considerations.

¹¹ For claims 2–25, Petitioner combines its analysis of the two grounds. *See* Pet. 30–66.

implementation details.” Pet. 11–15. Dr. Brogioli testifies that “[a person of ordinary skill] would have been motivated to implement the processors in Fox as lockstep processors to improve reliability and availability of Fox’s server system for critical processes, for which higher reliability and availability of the system are desired.” Brogioli Decl. ¶ 87. He further testifies that “[a person of ordinary skill] also would have been motivated to implement in Fox the error detection logics that detect loss of lockstep together with the lockstep processors as taught by Safford to implement lockstep functions and further improve availability of the system.” *Id.* He asserts that “[a person of ordinary skill] would have understood how to implement Fox’s processors as lockstep processors with error detection logics and expect success. [A person of ordinary skill] would only have applied well-known configurations and ordinary hardware and software configuration skills.” *Id.* ¶ 88. Dr. Brogioli provides additional reasons motivating the combination. *Id.* ¶¶ 89–96.

Petitioner contends that “Arai discloses switching the role of a failing processor with a spare processor.” Pet. 10. Dr. Brogioli testifies that “[a person of ordinary skill] would have been motivated to incorporate Arai’s teaching of transferring processor context from the failing processor to the spare processor not to interrupt the operating system and its running applications as desired by Fox.” Brogioli Decl. ¶ 105. He reasons that “[a person of ordinary skill in the art] would have understood that incorporating Arai’s processor-switching implementation details into Fox-Safford would provide the benefit of switching the role of the failing processor to the spare processor without affecting the operating system and running applications, which is expressly taught as desirable by both Fox and Arai and well known in the art.” *Id.* ¶ 106.

Petitioner asserts that a person of ordinary skill also would have been motivated to further combine these references with Landry. Pet. 31–33. Dr. Brogioli testifies that “Landry discloses a fault-tolerant boot process that dynamically designates a functional CPU as logical CPU0 that performs the unique functions of a boot processor.” Brogioli Decl. ¶ 132. He testifies further that “[a person of ordinary skill] would have understood Landry’s process would have been a suitable option for selecting a boot processor in Fox’s system consistent with the initialization protocol of the IA-32 multiprocessor system.” *Id.* ¶ 132. He asserts that “[a person of ordinary skill] would have understood the benefits of implementing Landry’s boot processor selection process in Fox.” *Id.* ¶ 133. Among other reasons, “[a person of ordinary skill] would have further understood that using the logical CPU0 as the identification for the boot processor allows for transparent replacement of the physical processor experiencing a failure with another processor without interrupting the operating system.” *Id.*

At this stage, Patent Owner does not respond to these arguments by Petitioner or refute the testimony by Dr. Brogioli. On this record, we find that Petitioner has sufficiently demonstrated a motivation to combine Fox and Safford with Arai and to further combine these references with Landry with a reasonable expectation of success.

2. Independent Claim 1

Petitioner presents an element-by-element analysis of claim 1 supported by the testimony of Dr. Brogioli. Pet. 22–30, 33–36; Brogioli Decl. ¶¶ 109–128, 136–145. For the reasons given by Petitioner, we determine that Petitioner demonstrates a reasonable likelihood of prevailing on its challenges to this claim.

[Preamble]: “A method comprising:”

Petitioner relies on Fox as disclosing the preamble of claim 1. Pet. 22, 33.¹²

[1a]: “detecting loss of lockstep (LOL) for a processor in a multi-processor system;”

Petitioner relies on Fox and Safford to meet this limitation. Pet. 22–25, 33. Petitioner explains that “Fox does not expressly disclose that its processors are lockstep processors or detecting loss of lockstep (LOL). Safford does.” *Id.* at 22 (citing Brogioli Decl. ¶¶ 111–112).

[1b]: “determining that the processor for which said LOL is detected is assigned a role of boot processor;”

In its first ground, Petitioner relies on Fox and Safford to meet this limitation. Pet. 25. In its second ground, Petitioner relies on Fox, Safford, and Landry. *Id.* at 33–35. Petitioner asserts that “Fox-Safford-Landry renders obvious determining that the processor for which said LOL is detected is assigned a role of boot processor.” *Id.* at 34 (citing Brogioli, Decl. ¶¶ 140–141). Dr. Brogioli testifies that “Fox combined with Safford and Landry, would have determined that the processor for which said LOL is detected is logical CPU0, which is the processor assigned a role of boot processor.” Brogioli Decl. ¶ 143.

[1c]: “changing a system identifier, used by the system’s operating system to recognize the boot processor, of said boot processor for which said LOL is detected, to a different value, which causes the system’s operating system

¹² We do not express an opinion on whether the preamble recitations of the challenged claims are limiting. We find that Petitioner establishes a reasonable likelihood that the cited art discloses the preambles.

to not recognize the processor for which said LOL is detected as the boot processor; and”

Petitioner contends that “[i]n Fox-Safford-Arai, a [person of ordinary skill] would have understood that [such] identification switching would have switched the logical APIC ID (‘system identifier’) of the lockstep processor pair of the boot processor detected to have LOL with that of the spare processor pair.” Pet. 27–28 (citing Ex. 1006 ¶ 21). Dr. Brogioli testifies further that “[a person of ordinary skill] would have understood that such switching would have ‘cause[d] the system’s operating system to not recognize the processor for which said LOL is detected as the boot processor.” Brogioli Decl. ¶ 122 (second alteration in original). He continues, “[t]his is because the unique logical identification of the boot processor having LOL as it was known to the BIOS and operating system has been assigned to that of the spare processor.” *Id.*

[Id]: “changing a system identifier of the spare processor to that of the boot processor, thereby switching the role of boot processor to a spare processor without shutting down the system’s operating system.”

Petitioner asserts in its first ground that “[a person of ordinary skill] would have understood that in Fox-Safford, in response to determining that the LOL is detected in the boot processor, implementing Arai’s identification switching and context transfer would have reassigned the processor logical identification and responsibilities of the failing boot processor pair to the spare processor pair without interrupting the operating system (‘switching the role of boot processor to a spare processor without shutting down the system’s operating system’).” Pet. 29–30 (citing Ex. 1005 ¶¶ 8, 10, 13; Ex. 1007 ¶ 6). Dr. Brogioli testifies that “a [person of ordinary

skill] would have understood that incorporating Arai’s processor-switching implementation detail would improve availability and reliability of the multiprocessor system in Fox as modified by Safford.” Brogioli Decl.

¶ 128. He further testifies that “[a person of ordinary skill] would have expected success in such modification because it merely involves using known techniques to improve a similar device in the same way taught in the prior art.” *Id.*

Petitioner’s second ground relies on Fox, Safford, Landry, and Arai, and refers to the above analysis for this limitation in Petitioner’s first ground and the above discussion of claim limitation [1b]. Pet. 36.

3. Independent Claims 13 and 21

Petitioner has provided element-by-element analyses for these claims supported by testimony from Dr. Brogioli. *See* Pet. 36–51; Brogioli Decl. ¶¶ 147–190. Petitioner’s analysis of these claims in relation to Fox, Safford, Arai, and Landry is similar to its analysis of claim 1. For example, claim limitation [13e] recites: “changing a system identifier of the spare processor to that of the boot processor, thereby switching the role of boot processor to said spare processor.” Pet. 43. Petitioner’s analysis of this limitation asserts that this limitation “is similar to [1d],” and relies on its prior analyses of Fox-Safford-Arai and Fox-Safford-Landry-Arai in connection with [1d]. *Id.*; *see also* Section II.D.2.[1d], *supra*.

Similarly, claim limitation [21e] recites: “wherein if determined that said first processor module is assigned the role of system boot processor, said system firmware is further operable to cause said operating system to recognize another processor module as system boot processor without shutting down said operating system.” Pet. 51. Petitioner’s analysis of this

limitation relies on Fox-Safford-Arai and Fox-Safford-Landry-Arai and refers back to its analysis of claims 1 and 13. *Id.* at 51–52.

For the reasons given by Petitioner, we determine that Petitioner has demonstrated a reasonable likelihood of proving that these claims would have been obvious.

4. Dependent Claims 2–12, 14–20, and 22–25

Claims 2–12 depend from claim 1. Claims 14–20 depend from claim 13. Claims 22–25 depend from claim 21. Petitioner provides a separate analysis for each of these dependent claims. Pet. 53–66. Patent Owner’s Preliminary Response does not address these claims.

For the reasons given for independent claims 1, 13, and 21 and additionally for the dependent claims, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 2–12, 14–20, and 22–25, based on Fox, Safford, and Arai and on Fox, Safford, Landry, and Arai.

5. Conclusion on Claims 1–25

In sum, after considering the reasons presented above and in the Petition, which were not addressed in Patent Owner’s Preliminary Response, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1–25 based on Fox, Safford, and Arai, and on those references further combined with Landry.

K. Remaining Challenges to Patentability

Petitioner presents additional challenges to claims 26 and 27. Pet. 67–74. As set forth above, after considering the evidence and arguments presented in the Petition, we determine that there is a reasonable likelihood

that Petitioner would prevail with respect to at least two challenges to the '302 patent claims, i.e., those challenges to claims 1–25 based on the combination of Fox, Safford, and Arai and the combination of Fox, Safford, Landry, and Arai. We, therefore, do not address the other challenges at this stage and institute trial as to all challenged claims on all grounds stated in the Petition. *See SAS Inst. Inc.*, 584 U.S. at 365; 37 C.F.R. § 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”).

II. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated a reasonable likelihood that Petitioner would prevail in showing at least one of the challenged claims of the '302 patent is unpatentable.

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–27 of the '302 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '302 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

IPR2024-01347
Patent 7,624,302 B2

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