

Compensation Pixel Circuit to Improve Image Quality for Mobile AMOLED Displays

Chih-Lung Lin¹, Member, IEEE, Po-Chun Lai¹, Li-Wei Shih, Chia-Che Hung, Po-Cheng Lai¹,
Tsu-Yuan Lin, Kuang-Hsiang Liu, and Tsang-Hong Wang

Abstract—This paper proposes a new pixel circuit using low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) for use in mobile active matrix organic light-emitting diode (AMOLED) displays. The purpose of a pixel circuit is to supply stable and uniform currents to current-driving devices of OLEDs. The proposed pixel circuit uses overlapping compensation times to extend the period of precise sensing of V_{TH} variations of LTPS TFTs. Moreover, the proposed circuit prevents a current from flowing into an OLED when the OLED is not operated in the emission stage to avoid image flicker. An 1.3-in panel that uses the proposed pixel circuit is fabricated. Measurement results verify that the increased T_{COMP} of 33.3 μ s results in higher contrast ratio and lower required data voltages than those at T_{COMP} values of 4.3 and 2.2 μ s. Red, green, and blue images displayed by the fabricated panel with a T_{COMP} of 33.3 μ s with a 255 gray level are all much more uniform than with T_{COMPS} of 4.3 and 2.2 μ s. White images with a T_{COMP} of 33.3 μ s for 16 and 8 gray levels on the fabricated panel confirm that the serious line and spot defects in the images with T_{COMP} values of 4.3 and 2.2 μ s are effectively eliminated. Therefore, the proposed pixel circuit is suitable for use in mobile AMOLED displays.

Index Terms—Active matrix organic light-emitting diode (AMOLED), low-temperature polycrystalline silicon (LTPS), pixel circuit, thin-film transistor (TFT).

I. INTRODUCTION

ACTIVE matrix organic light-emitting diode (AMOLED) displays are expected to become the next generation of commercial displays and have been rapidly developed by the electronics industry in recent years [1]–[4]. AMOLED displays have the advantages of a high contrast ratio, a wide viewing angle, a short response time, a high brightness, and a wide color gamut [5]–[7]. The self-emissive characteristics of OLED devices ensure that AMOLED displays have higher

contrast ratio and a black image of higher quality than active matrix liquid crystal displays (AMLCDs) [8]–[13]. In mobile applications such as smartphones, the high quality of a black image is critical because any light leakage is easily observed on mobile devices in the case of dark environment. Theoretically, a panel can easily display a pure black image when all OLEDs in the panel are turned off. However, in real display operations, each OLED is driven by a pixel circuit because an OLED is a current-driven device [14]. Thus, each data voltage, which will be applied to the pixel circuit and determine the magnitude of driving current, corresponding to each gray level should be defined. After the definition, each data voltage for each gray level is fixed. Therefore, the driving TFT generates a driving current according to its gate-to-source voltage (V_{GS}) and threshold voltage (V_{TH}). The backplanes of mobile AMOLED displays adopt low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) owing to their high mobility and small layout area [15]–[17]. However, LTPS TFTs inevitably suffer from threshold voltage (V_{TH}) variations that are caused by fluctuations of the laser beam in the excimer laser annealing (ELA) process. As the TFT V_{TH} varies, I_{OLED} also changes, indicating that the OLED emits light with the defined data voltage that corresponds to the zero gray level. When the OLED luminance from single-color (red, green, or blue) sub-pixels is non-uniform, serious image color distortion may occur. The compensation mechanism senses the V_{TH} variation of the driving TFT and stores the sensed voltage in a storage capacitor. If the stored voltage is identical to the real V_{TH} of the driving TFT, then the pixel circuit can provide a precise driving current, such as a zero driving current at the zero gray level and produce uniform displayed images. Thus, many compensating methods have been proposed to solve this problem of non-uniformity [18]–[24]. The voltage programming method is now widely used in AMOLED displays because of a shorter compensating period than that of the current programming method, real-time compensation, and the lack of any need for an additional external circuit [16]. However, as the required resolution and frame rate of displays increase, the scan time of one row (T_{SCAN}) becomes shorter. Pixel circuits in one row can only acquire voltages from data lines within the T_{SCAN} . In the voltage programming method, most pixel circuits must use data lines to provide reference or data voltages for pixels while they compensate for V_{TH} variations of TFTs, making compensation time (T_{COMP}) shorter than or equal to T_{SCAN} [16], [25]–[27]. Therefore, a short T_{SCAN} may cause the T_{COMP} to be too short for the voltage programming method, resulting

Manuscript received February 24, 2018; revised June 5, 2018 and August 24, 2018; accepted November 4, 2018. This work was supported in part by the Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan, Taiwan, in part by the Ministry of Science and Technology of Taiwan under Project MOST 107-2221-E-006-188-MY3 and Project MOST 106-2622-E-006-011-CC2, and in part by AU Optronics Corporation. This paper was approved by Associate Editor David Stoppa. (Corresponding author: Chih-Lung Lin.)

C.-L. Lin is with the Department of Electrical Engineering, National Cheng Kung University, Tainan 701-01, Taiwan, and also with the and the Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan 701-01, Taiwan (e-mail: cllin@ee.ncku.edu.tw).

P.-C. Lai, L.-W. Shih, C.-C. Hung, T.-Y. Lin, K.-H. Liu, and T.-H. Wang are with the AU Optronics Corporation, Hsinchu 30078, Taiwan.

P.-C. Lai is with the Department of Electrical Engineering, National Cheng Kung University, Tainan 701-01, Taiwan.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2018.2881922

TABLE I
COMPARISON BETWEEN PROPOSED AND PREVIOUS
DEVELOPED PIXEL CIRCUITS

Reference	Number of lines	Flicker prevention	T_{COMP} extension	Small reset current	Large reset V_{GS} of driving TFT	Fixed power voltage
[14] 4T2C	3	×	×	×	×	○
[28] 6T1C	3	×	○	×	○	○
[29] 3T2C	2	×	○	×	○	×
[30] 4T2C	2	×	○	×	○	×
[31] 6T2C	6	○	○	×	○	○
[32] 5T2C	4	○	○	×	○	○
This work 6T2C	4	○	○	○	○	○

in the failure of compensation for non-uniform brightness of a display image. If the stored voltage cannot exactly equal the real V_{TH} of the driving TFT, the compensation performance is an important issue. To enhance the uniformity of a high-resolution and high-frame-rate display, T_{COMP} should not be limited by T_{SCAN} . Several pixel circuits have been developed to extend T_{COMP} [28]–[32]. However, none of the pixel circuits in [28]–[30] ensures that no current flows through the OLEDs when a black image is required, and this defect is unacceptable for mobile display applications. Although the pixel circuits in [31] and [32] can produce high-quality black images, their resetting methods generate huge resetting currents, increasing the power consumption. The pixel circuit in [31] needs four control signal and two reference lines, reducing applicability to high-resolution displays. The pixel circuit in [32] suffers from a heavy loading on the data line, so a data line may not transmit data signals to pixels in a column correctly in a real display. The control signals of pixel circuit in [32] are complicated, increasing the difficulty of acquiring suitable gate drivers. Also, higher reset V_{GS} of the driving TFT favors the sensing of TFT V_{TH} variations.

This paper proposes a new pixel circuit to compensate for V_{TH} variations of LTPS TFTs without using data lines, so the T_{COMP} is not limited by the T_{SCAN} . This prolonging T_{COMP} in each row guarantees an accurate detection of V_{TH} variations in LTPS TFTs. Preventing any current from flowing through OLEDs can further suppress image flicker in mobile displays. Table I shows the comparison of the proposed circuit with [14] and [28]–[32]. The control signal and reference lines are both counted in the number of lines. An 1.3-in panel based on the proposed pixel circuit is fabricated. Experimental results demonstrate that extending T_{COMP} indeed improved the contrast ratio of the display and reduced the required data voltages. Uniform red, green, and blue images are displayed on the panel to confirm the compensation capability of proposed pixel circuit. The proposed method also eliminates the serious line and spot defects in images at low light-intensity levels, as can be seen from Table V.

II. OPERATION OF PROPOSED PIXEL CIRCUIT

Fig. 1(a) shows the structure of the proposed pixel circuit, and Fig. 1(b) displays the timing diagram of the control signals. The proposed pixel circuit is composed of one driving TFT, five switching TFTs, and two capacitors. The operation of the proposed pixel circuit can be divided into four stages, which are described in detail, as shown in Fig. 2.

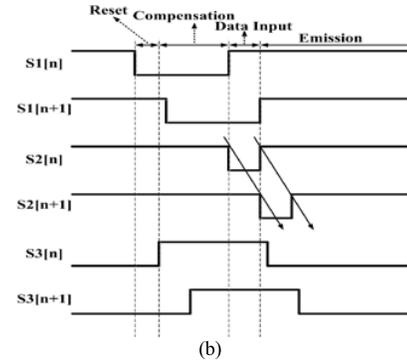
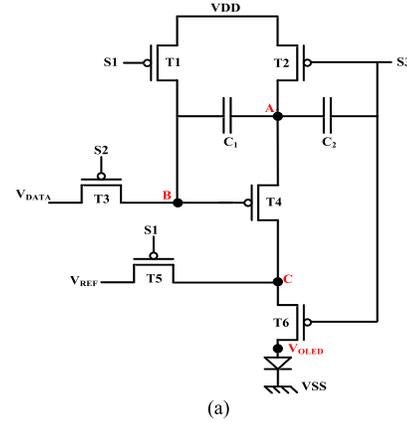


Fig. 1. (a) Proposed pixel circuit schematic and its (b) timing diagram of control signals.

- 1) *Reset Stage*: In this stage, as shown in Fig. 2(a), $S2$ is at a high voltage to turn off $T3$. $S1$ and $S3$ are low to turn on $T1$, $T2$, $T5$, and $T6$. The purpose of this stage is to reset the voltages of the gate and source nodes of the driving TFT. The V_{DD} is applied to gate and source nodes of the driving TFT through $T1$ and $T2$ simultaneously, so the source-to-gate voltage of the driving TFT (V_{SG_T4}) is 0 V. V_{SG_T4} is smaller than $|V_{TH_T4}|$ so the driving TFT is cut off to avoid the generation of a current to the OLED. In addition, V_{REF} is applied to the anode of the OLED through $T5$ and $T6$. The voltage across the OLED is $V_{REF} - V_{SS}$ (1.8 V), which is smaller than the V_{TH_OLED} of 1.85 V. Therefore, the OLED is completely turned off in the reset stage to prevent flicker.
- 2) *Compensation Stage*: $S3$ goes high to turn off $T2$ and $T6$. $S1$ remains low to apply V_{DD} and V_{REF} to nodes B and C, respectively. Since $C2$ is connected to $S3$ which changes from V_{GL} to V_{GH} , by the charge conservation, the voltage of node A (V_A) is boosted as follows:

$$V_A = V_{DD} + (V_{GH} - V_{GL}) \times \frac{C2}{C1 + C2}. \quad (1)$$

V_{SG_T4} is larger than $|V_{TH_T4}|$ so the driving TFT starts to generate a current. Meanwhile, node A discharges until the driving TFT is cut off. Finally, node A will be discharged to $V_{DD} + |V_{TH_T4}|$. Fig. 2(b) shows the operating conditions of all TFTs, the OLED, and the

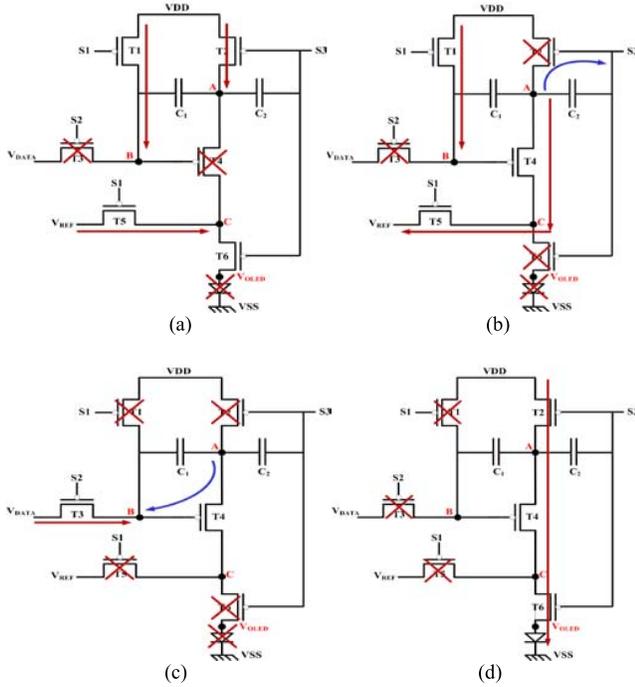


Fig. 2. Schematic of circuit operation in (a) reset, (b) compensation, (c) data input, and (d) emission stages.

major current paths. Blue arrow indicates the voltage boosting of node A when S3 goes high. In this stage, S2 remains high to turn off T3, so the proposed compensating scheme does not need any voltage from data lines. Therefore, T_{COMP} is not limited by T_{SCAN} and T_{COMPS} of multiple rows can be overlapped. Overlapping the T_{COMPS} in multiple rows increases the total T_{COMP} for sensing V_{TH_T4} , increasing the precision of sensing. Hence, pixel circuits generate uniform driving currents when the V_{TH} variations of driving TFTs are well compensated for. In addition, T6 is turned off and T5 is turned on, so all currents that are generated by the driving TFT will flow into the reference line rather than the OLED. Thus, the OLED remains in a completely dark state in this stage.

- 3) *Data Input Stage*: During this stage, as shown in Fig. 2(c), S1 goes high to turn off T1 and T5. S2 goes low to turn on T3 so the data voltage (V_{DATA}) is applied to node B. By charge conservation, V_A is boosted as shown in the following equation and blue arrow in Fig. 2(c):

$$V_A = V_{DD} + |V_{TH_T4}| + (V_{DATA} - V_{DD}) \frac{C1}{C1 + C2}. \quad (2)$$

Thus, V_{SG_T4} is stored in C1, as shown in the following equation:

$$\begin{aligned} V_{SG_T4} &= V_{DD} + |V_{TH_T4}| \\ &+ (V_{DATA} - V_{DD}) \frac{C1}{C1 + C2} - V_{DATA} \\ &= (V_{DD} - V_{DATA}) \frac{C2}{C1 + C2} + |V_{TH_T4}|. \end{aligned} \quad (3)$$

S3 remains high to keep the OLED in the dark state.

- 4) *Emission Stage*: According to Fig. 2(d), S1 and S2 are high to turn off T1, T3, and T5. S3 goes low to turn on T2 and T6 and the OLEDs in all pixels of a row start emission. The driving current (I_{OLED}) can be calculated as shown in the following equation:

$$\begin{aligned} I_{OLED} &= \frac{1}{2} k (V_{SG_T4} - |V_{TH_T4}|)^2 \\ &= \frac{1}{2} k \left[(V_{DD} - V_{DATA}) \frac{C2}{C1 + C2} \right. \\ &\quad \left. + |V_{TH_T4}| - |V_{TH_T4}| \right]^2 \\ &= \frac{1}{2} k \left[(V_{DD} - V_{DATA}) \frac{C2}{C1 + C2} \right]^2 \end{aligned} \quad (4)$$

where k is $\mu \cdot C_{OX} \cdot W_{T4}/L_{T4}$. In (4), V_{TH_T4} is eliminated so the variations of V_{TH} of the driving TFTs will not influence the uniformity of the display image. Since the driving voltage is stored by C1 and the voltage on node A, which is connected to C1, is supplied by V_{DD} , the changes of the driving currents that are caused by small voltage fluctuations on S3 signal line are so small that they can be ignored. Since the V_{DD} of the proposed pixel circuit is fixed, the panel can adopt the mesh layout to minimize the V_{DD} IR drop. Furthermore, the OLEDs are all completely turned off from stage 1 to stage 3 so the quality of the black image can be ensured. Therefore, the proposed pixel circuit can generate uniform driving currents and prevent mobile AMOLED displays from exhibiting flicker.

III. RESULTS AND DISCUSSION

To confirm that the proposed pixel circuit provides uniform OLED luminance and a high-quality black image, HSPICE simulations are conducted and an 1.3-in panel is fabricated. The target display specifications in this paper are a 5.8-in panel size, full high-definition (FHD) resolution, and a 120-Hz frame rate. Although the newest mobile devices have QHD or even higher resolution, most currently used mobile devices still use FHD resolution. Mobile devices with a frame rate of 120 Hz are being developed but are not yet widely commercialized. Therefore, in this paper, the proposed pixel circuit with the widely used FHD and a frame rate of 120 Hz, which is reasonable for future mobile device applications, is simulated. Fig. 3 shows the current-to-voltage ($I-V$) characteristics of fabricated LTPS TFTs with an aspect ratio of $3 \mu\text{m}/3 \mu\text{m}$ in three different glasses, supporting the simulations in this paper. In this paper, the proposed, conventional 2T1C [17], and conventional four-transistor-two-capacitor (4T2C) [14] compensating pixel circuits are compared. Table II shows the parameters of TFTs, capacitors, scan signals, and power levels, indicating that the three pixel circuits are compared fairly. Fig. 4(a) shows the simulated driving currents of a conventional 2T1C pixel circuit with different data voltages. Obviously, as the V_{TH} of the driving TFT varies by 0.5 V, the driving currents considerably change, causing apparent non-uniformity of the display image. A huge driving current is generated as the V_{TH} of the driving TFT varies by +0.5 V with a data voltage of 1.2 V, resulting in unwanted brightness

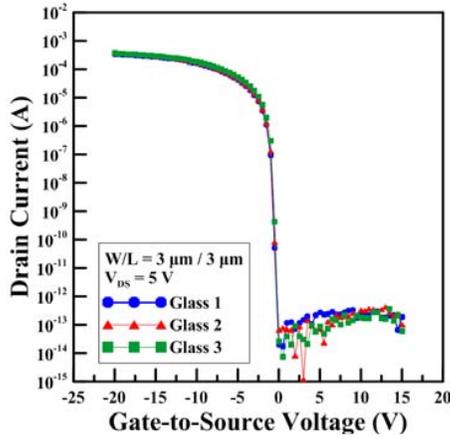
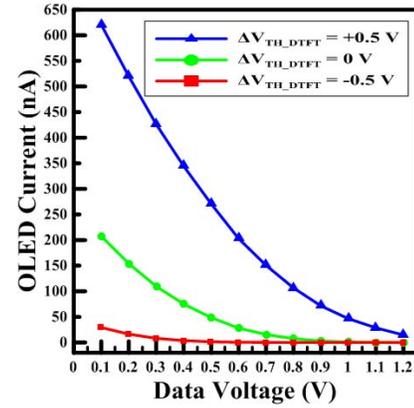


Fig. 3. Measured I - V characteristics of fabricated LTPS TFTs in three different glasses.

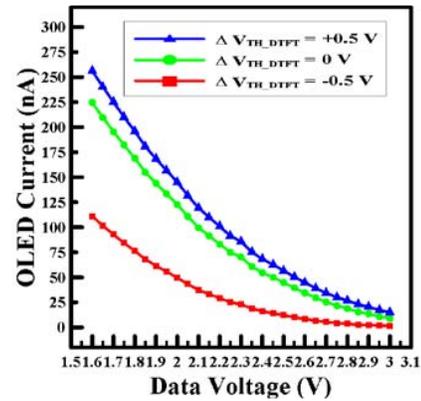
TABLE II
PARAMETERS OF THREE PIXEL CIRCUITS

Parameter	Value	Parameter	Value
C_{OLED} (pF)	0.2	$V_{TH_{OLED}}$ (V)	1.85
V_{DD} (V)	3	$S1 \sim S2 \sim S3$ (V)	-5 ~ 5
Proposed Pixel Circuit			
$(W/L)_{T1, T3, T6}$ (μm)	2.5/3	$(W/L)_{T2}$ (μm)	7/3
$(W/L)_{T4}$ (μm)	3/32	$(W/L)_{T5}$ (μm)	3/3
$C1 \sim C2$ (pF)	0.39	V_{REF} (V)	0
V_{SS} (V)	-1.8		
Conventional 2T1C Pixel Circuit			
$(W/L)_{T_{Switch}}$ (μm)	2.5/3	$(W/L)_{T_{Driving}}$ (μm)	3/32
C_S (pF)	0.78	V_{SS} (V)	-1.8
Conventional 4T2C Compensating Pixel Circuit			
$(W/L)_{MN1, MN4}$ (μm)	2.5/3	$(W/L)_{MN2}$ (μm)	3/32
$(W/L)_{MN3}$ (μm)	3/3	$C1 \sim C2$ (pF)	0.39
V_{SS} (V)	-1.8		

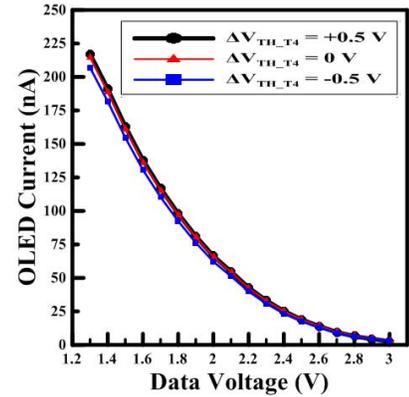
in a black image. Fig. 4(b) shows the simulated driving currents versus the data voltages of the conventional 4T2C compensating pixel circuit with 0.5 V variations in V_{TH} . For a given initial driving current, the driving currents of driving TFTs in a 4T2C pixel with V_{TH} variations of 0.5 V are much closer to the initial current than those in a 2T1C pixel circuit, revealing that a pixel circuit with a V_{TH} compensation mechanism exhibits more uniform driving currents. Although the conventional 4T2C compensating pixel circuit seems to be capable of dealing with the V_{TH} variations of driving TFTs, its compensating performance should be further evaluated in terms of specific frame rate and resolution of the display, which directly determine the T_{SCAN} , owing to the use of a data line in the compensation phase. To confirm that the proposed pixel circuit also compensates for the V_{TH} variations of the driving TFTs, Fig. 4(c) shows the simulated driving currents of the proposed pixel circuit with different data voltages. The driving currents are almost unaffected by variations of V_{TH} in the driving TFT, and no large driving current is generated at low gray levels. Based on the simulation results in Fig. 4(a)–(c), the conventional 2T1C pixel circuit cannot generate high-quality images if no other compensating



(a)



(b)



(c)

Fig. 4. Driving currents of OLEDs in (a) conventional 2T1C [17], (b) conventional compensating 4T2C [14], and (c) proposed pixel circuits.

mechanism is used. The compensating efficiencies of the conventional 4T2C and proposed pixel circuits require further evaluation. To confirm that the extended T_{COMP} efficiently enhances the compensating capability of a pixel circuit, T_{COMP} is set to 33.3, 8.6, 4.3, and 2.2 μs in the simulations. T_{SCAN} is 8.6 and 4.3 μs at the specification of FHD resolution with frame rate of 60 and 120 Hz, respectively. Many compensating pixel circuits can only compensate for V_{TH} variations of TFTs with a shorter T_{COMP} than T_{SCAN} , so T_{COMP} is set to 2.2 μs

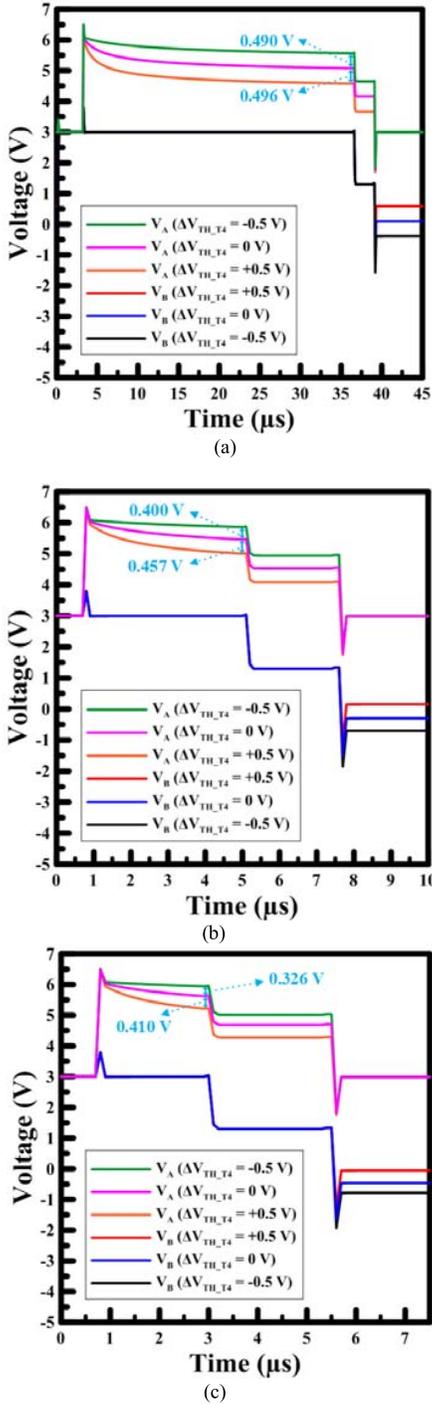


Fig. 5. Simulated transient waveforms of V_A and V_B of the proposed pixel circuit with different V_{TH_T4} variations when T_{COMP} is (a) 33.3, (b) 4.3, and (c) 2.2 μs .

under this condition. Fig. 5(a) shows the simulated transient waveforms of node A of the proposed pixel circuit using a T_{COMP} of 33.3 μs with V_{TH} variations of $+0.5$ and -0.5 V in the driving TFT. At the end of the compensation stage, the proposed circuit senses the variations of $+0.496$ and -0.490 V, which are very close to the actual variations

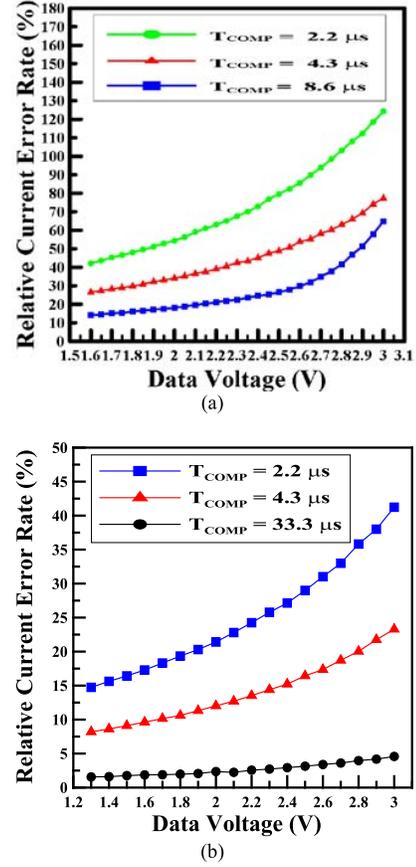


Fig. 6. Simulated relative current error rates of (a) conventional compensating 4T2C [14] and (b) proposed pixel circuits with different T_{COMP} .

of $+0.5$ and -0.5 V, respectively. When T_{COMP} is set to 4.3 μs , the pixel circuit senses the variations of $+0.457$ and -0.400 V rather than the actual values of $+0.5$ and -0.5 V, as shown in Fig. 5(b). In Fig. 5(c) with the shortest T_{COMP} of 2.2 μs , the pixel circuit senses variations of $+0.410$ and -0.326 V, which differ markedly from the actual values of $+0.5$ and -0.5 V. Therefore, using an overlapping compensating period to extend T_{COMP} causes the proposed pixel circuit to sense variations of V_{TH} of the driving TFTs more precisely, increasing the uniformity of the display image. To evaluate the compensating performance of the conventional 4T2C and proposed pixel circuits with different gray levels, the relative current error rates with various V_{DATA} values and different values of T_{COMP} are simulated, as shown in Fig. 6. To compare fairly the proposed pixel circuit with the conventional 4T2C pixel circuit, the ranges of V_{DATA} in Fig. 6 that are used to generate the same initial driving currents equal those in Fig. 4. For a conventional 4T2C pixel circuit, T_{COMP} must be shorter than the T_{SCAN} . Thus, the T_{COMP} of 2.2 μs is close to that for FHD resolution and a frame rate of 120 Hz. T_{COMP} values of 8.6 and 4.3 μs are utilized to simulate ideal cases of FHD resolution with 60 and 120 Hz, respectively. As shown in Fig. 6(a), the relative current error rates range from 14.12% to 64.85%, 26.58% to 77.29%, and 42.16% to 124.23% for T_{COMP} values of 8.6, 4.3, and 2.2 μs , respectively, confirming

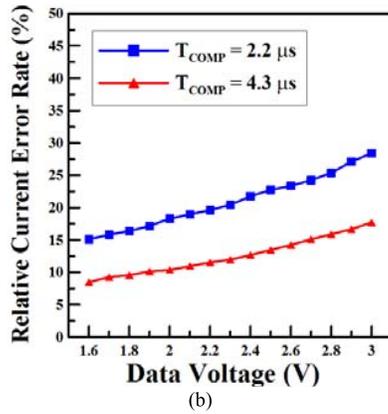
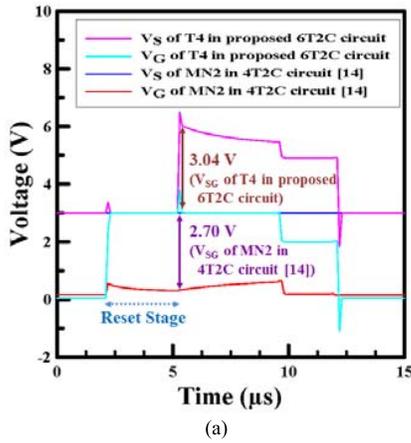


Fig. 7. (a) Simulated transient waveforms of source and gate nodes of driving TFTs in the proposed 6T2C and conventional 4T2C pixel circuits. (b) Simulated relative current error rates of conventional 4T2C pixel circuit with lower V_{SS} of -2.6 V with different T_{COMP} [14].

that the conventional 4T2C circuit with the longer T_{COMP} of $8.6 \mu s$ indeed compensates more effectively for TFT V_{TH} variations. The T_{COMP} of the proposed pixel circuit can be extended to $33.3 \mu s$ owing to its overlapping compensation. As shown in Fig. 6(b), the relative current error rates with a T_{COMP} of $33.3 \mu s$ are all lower than 5%, revealing much better uniformity of the driving currents than the conventional 4T2C pixel circuit. Fig. 6(b) displays the simulation of the proposed pixel circuit with a T_{COMP} of 4.3 or 2.2 μs . The relative current error rates range from 8.20% to 23.30% and 14.74% to 41.23%, which are all lower than the 26.58% to 77.29% and 42.16% to 124.23% of the conventional 4T2C pixel circuit, respectively. The simulated results verify that the proposed resetting method yields more effective compensation than the conventional 4T2C pixel circuit under the same T_{COMP} . The compensation performance of a pixel circuit is determined by not only the compensation time but also the reset method. When V_{GS} of driving TFT is reset to be larger, the compensation performance will be better. As shown in Fig. 7(a), the proposed pixel circuit resets V_{GS} of the driving TFT to 3.04 V, which is larger than 2.70 V in the 4T2C pixel circuit. Therefore, the proposed pixel circuit has lower relative current error rates than the 4T2C pixel circuit at the

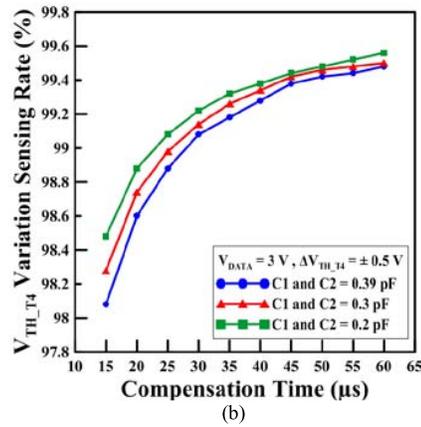
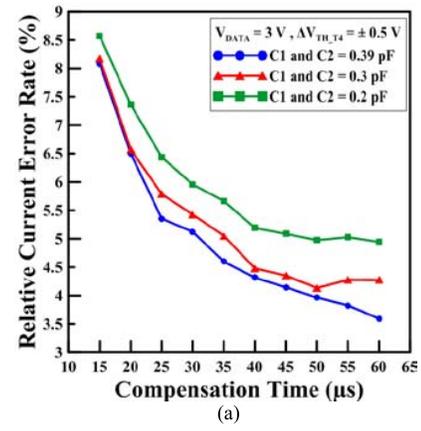


Fig. 8. Simulated (a) relative current error rates and (b) sensing rates of TFT V_{TH} variation of proposed pixel circuit with different capacitances of capacitors and compensation times.

same compensation time. Fig. 7(b) shows the relative current error rates of the conventional 4T2C pixel circuit when V_{SS} is changed from -1.8 to -2.6 V. Figs. 6(b) and 7(b) confirm that the conventional 4T2C pixel circuit with a low reset voltage has nearly the same compensation capability as the proposed 6T2C pixel circuit with the same compensation time. Also, when most of the variations of TFT V_{TH} have been sensed and stored, increasing the compensation time only slightly improves the compensation performance because each source node of the driving TFT in each pixel is discharged very slowly. When the capacitors have high capacitance, the pixel circuit needs a longer compensation time to sense the V_{TH} variations of TFTs because more charges are stored in the capacitors. However, reducing the capacitances of the capacitors also increases the relative current error rates because other side effects, such as charge sharing between nodes A and C during the data input stage, charge injection, and clock feed-through, dominate the current errors. In particular, when the $C1$ and $C2$ are smaller, the side effects are more obvious, so the current error is higher when $C1$ and $C2$ are lower. Considering these issues, whether the compensation time should be increased or decreased when the capacitances of the capacitors vary has no definite answer. As shown in Fig. 8(a), when $C1$ and $C2$ are both reduced from 0.39 to

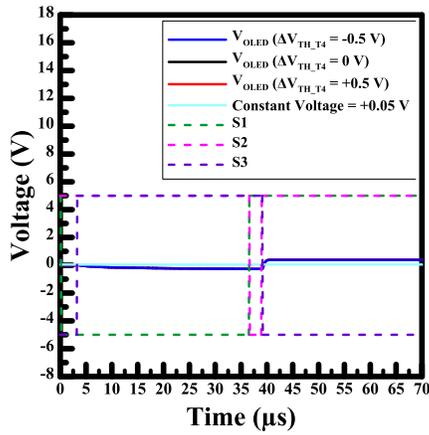


Fig. 9. Simulated voltages on anode of OLED when V_{TH} variations of driving TFT are -0.5 , 0 , and $+0.5$ V.

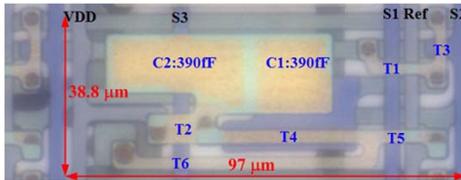
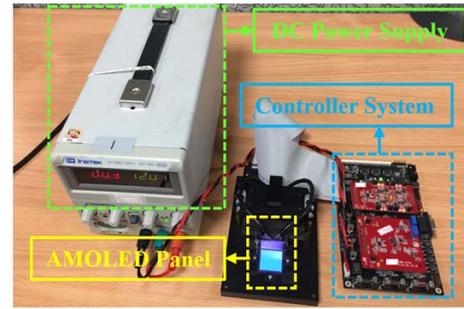
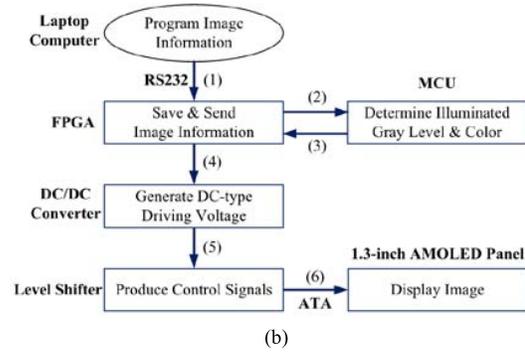


Fig. 10. Optical photograph of fabricated pixel circuit.

0.3 and 0.2 pF, the pixel circuit needs a compensation time more than 35 and 45 μs , respectively, to maintain the relative current error rates of the proposed pixel circuit below 5% . Fig. 8(a) shows that the current error rate stop decreasing at around 5% with $C1$ and $C2$ at 0.3 pF and at around 4.3% with $C1$ and $C2$ at 0.2 pF, confirming that the compensation time can be increased to improve the compensating performance of pixel circuits to a limited extent. However, as shown in Fig. 8(b), the pixel circuit did sense the V_{TH} variations of TFTs faster during the compensation period when it had lower capacitances. Fortunately, the compensation time of the proposed pixel circuit is adjustable, so it must be further evaluated by simulation and experimentally for use in real products. Fig. 9 shows the anode voltages of the OLED in each stage of operation with variations of $+0.5$ and -0.5 V in the driving TFT. Since V_{TH_OLED} is 1.85 V and V_{SS} is -1.8 V, the OLED will be turned off when the anode voltage is lower than $V_{SS} + V_{TH_OLED}$, which equals 0.05 V. As shown in Fig. 9, the anode voltage of OLED exceeds 0.05 V only in the emission stage, demonstrating that the OLED only emits in the emission stage. Modulating the V_{DATA} to the lowest gray level to generate a black image causes no current to flow into the OLED so the OLED is also turned off in the emission stage. Since the OLED does not emit throughout the frame, the black image has high quality. To verify the feasibility of the proposed pixel circuit, an 1.3 -in AMOLED panel that is based on the LTPS TFT process is fabricated. Fig. 10 shows a photograph of the proposed pixel circuit with a pixel area of 97 $\mu\text{m} \times 38.8$ μm in the fabricated panel, in which the positions of the SCAN lines, the V_{DD} line, the TFTs, and the capacitors are indicated. In real products, the layouts of $T1$ and $T3$ in the proposed pixel circuit, which



(a)



(b)

Fig. 11. (a) Photograph of display system. (b) Block diagram of measurement platform system.

are connected to the floating point of node B, have a dual gate structure to minimize the movement of the charges in $T1$ and $T3$ to $C1$ and the leakage currents that flow through $T1$ and $T3$. However, the switching TFTs of $T1$ and $T3$ in the proposed circuit are presented as one TFT in Fig. 1(a). Since this paper is not concerned with analyzing the issue of leakage currents, the pixel layout of the fabricated testing panel did not adopt a dual gate structure. For real product applications, a dual gate structure must be used. Fig. 11(a) shows the overall configuration of the measurement platform system, which composes the fabricated 1.3 -inch AMOLED panel, a specialized controller system for driving the panel, and a dc power supply. The resolution, active area, and color depth of the panel are $240 \times \text{RGB} \times 240$, 23.28 mm (H) $\times 23.28$ mm (V), and 16.7 M, respectively. The controller system involves a micro-controller unit (MCU C8051F130, 8-bit processor with an operating frequency of 100 MHz), a field-programmable gate array (FPGA Spartan-6), power supply circuits, and level shifter circuits. Fig. 11(b) presents a block diagram of the measurement platform system. First, a computer inputs information about the desired image, including gate control signals and various gray level signals, into FPGA via the RS232 serial interface. The MCU subsequently commands FPGA to deliver the control signals and the determined gray signal to the level shifter. The power supply circuit generates stable and precise dc sources to drive the OLED ($V_{DD} = 3$ V and $V_{SS} = -1.8$ V). The level shifter circuit converts the gate control signals and gray signals to those with appropriate voltage levels as shown in Table II before transmitting them to the panel. Finally, the data voltages, the timing control signals, and the dc voltage sources are sent to the panel and enable

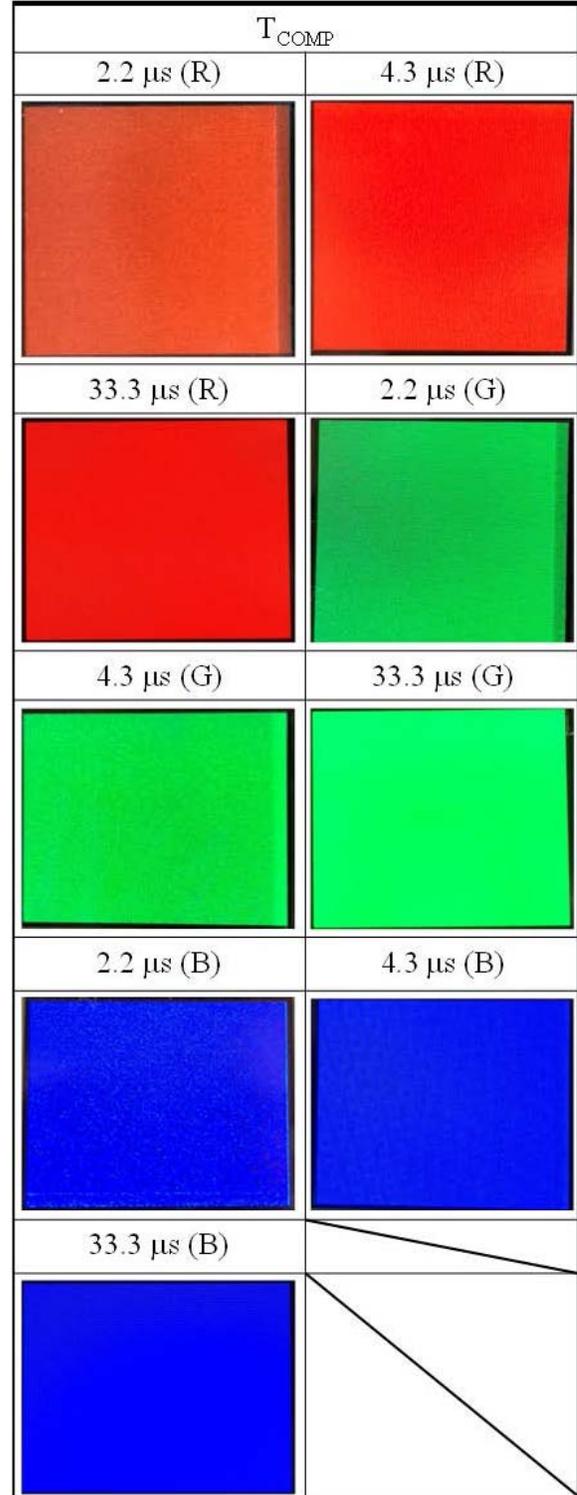
TABLE III
MEASURED LUMINANCE AND CONTRAST RATIO OF FABRICATED PANEL

Compensation time = 33.3 μ s				
Contrast ratio: 700400				
Gray Level	Luminance (nit)	V _{DATA} (R)	V _{DATA} (G)	V _{DATA} (B)
0	0.0005	5 V	5 V	5 V
8	0.180	4.4998 V	3.8360 V	3.7622 V
16	0.799	3.9660 V	3.7170 V	3.5589 V
64	16.81	3.3599 V	3.2485 V	2.8643 V
128	77.45	2.9479 V	2.8240 V	2.2368 V
255	350.2	2.3094 V	2.1571 V	1.0730 V
Compensation time = 4.3 μ s				
Contrast ratio: 145875				
Gray Level	Luminance (nit)	V _{DATA} (R)	V _{DATA} (G)	V _{DATA} (B)
0	0.0024	7 V	7 V	7 V
8	0.174	5.8464 V	4.9192 V	4.8468 V
16	0.790	5.2439 V	4.8850 V	4.6204 V
64	17.15	4.6106 V	4.4455 V	3.8323 V
128	78.69	4.1900 V	3.9959 V	3.0715 V
255	350.1	3.5677 V	3.3431 V	1.6633 V
Compensation time = 2.2 μ s				
Contrast ratio: 134846				
Gray Level	Luminance (nit)	V _{DATA} (R)	V _{DATA} (G)	V _{DATA} (B)
0	0.0026	7 V	7 V	7 V
8	0.172	6.2480 V	5.4163 V	4.8468 V
16	0.780	5.7551 V	5.3553 V	4.6204 V
64	16.73	4.9314 V	4.7376 V	3.8323 V
128	77.43	4.3628 V	4.1498 V	3.0715 V
255	350.6	3.5897 V	3.3419 V	1.6633 V

the pixel array to produce relative driving currents through the Advanced Technology Attachment (ATA) interface. Table III shows the measured luminance of the fabricated panel with T_{COMP} values of 33.3, 4.3, and 2.2 μ s. Table III presents various data voltage settings for red, green, and blue pixels and various gray levels. From the measured results, the highest luminance is set close to 350 nits under all three conditions, and the lowest luminance values at T_{COMP} values of 33.3, 4.3, and 2.2 μ s are 0.0005, 0.0024, and 0.0026 nits, respectively. For a given gray level, a shorter T_{COMP} results in higher data voltages, indicating that an insufficient T_{COMP} increases the power consumption in real panels. The maximum V_{DATA} of 7 V is only used to demonstrate the highest contrast ratios when the panel is operated with short compensation times of 4.3 and 2.2 μ s. A maximum V_{DATA} of 5 V and the compensation time of 33.3 μ s are adopted in this paper. For real product applications, leakage currents must be considered, so the high voltage of the scan signals will be increased. When the pixel circuit compensates for V_{TH} variation of driving TFT better, the variation of I_{OLED} between each pixel is smaller. Therefore, a panel can display a darker image of 0 gray level with better V_{TH} compensation. Calculation yield contrast ratios of the panel of 700400, 145875, and 134846 at T_{COMP} values of 33.3, 4.3, and 2.2 μ s, respectively, confirming the improvement in the contrast ratio by overlapping compensation. Notably, the contrast ratios of the fabricated panel are not limited by the measured values shown in Table II which are obtained only for comparison. The contrast ratios can be further increased by using more widely separated V_{DD} and V_{SS} than the current value of 4.8 V ($V_{DD} = 3$ V and $V_{SS} = -1.8$ V).

In addition to the measured luminance and contrast ratio, displayed images on the fabricated panel are compared. Table IV shows photographs of the fabricated panel which

TABLE IV
PHOTOGRAPH OF FABRICATED PANEL WITH DIFFERENT T_{COMPS} AT 255 GRAY LEVEL



displays red, green, and blue images with T_{COMP} values of 33.3, 4.3, and 2.2 μ s, respectively, at a gray level of 255. All parameters in the displayed images are the same as those in

TABLE V
PHOTOGRAPH OF FABRICATED PANEL WITH DIFFERENT T_{comps} AT 16 AND 8 GRAY LEVELS

T_{COMP}		
16 Gray level		
2.2 μs	4.3 μs	33.3 μs
8 Gray level		
2.2 μs	4.3 μs	33.3 μs

the simulations. Thus, the displayed images actually support the results from simulations. The image of each color with T_{COMP} of 33.3 μs is highly uniform owing to the sufficient compensation by the proposed pixel circuit. When the T_{COMP} is reduced to 4.3 or 2.2 μs , the uniformity of the displayed image of each color decreases; this effect is especially obvious at a T_{COMP} value of 2.2 μs . Since the human eye is highly sensitive to the images with low gray level, white images with T_{COMP} values of 33.3, 4.3, and 2.2 μs for 16 and 8 gray levels are provided, as shown in Table V. Serious line and spot defects are observed in the images with T_{COMP} values of 4.3 and 2.2 μs , whereas almost no line or spot defect is observed in the images with a T_{COMP} of 33.3 μs . The reddish color distortion of images at low gray levels is caused by the instability of the data driver IC, which is only for testing panels. As shown in Table III, the difference of V_{DATA} between gray level 0 and 8 for the red sub-pixel is much smaller than that for green and blue sub-pixels. Therefore, when the voltage supplied by data driver IC is unstable, the same voltage variation causes a greater red color shift than green and blue color shifts, resulting in the image with gray level of 8 to become reddish-gray rather than completely gray. Use of an appropriate data driver IC and mature bonding technology prevents the color distortion in real products. According to the experimental results in Tables III–V, the proposed pixel circuit indeed causes the display to exhibit high-quality images. To further evaluate the feasibility of the proposed pixel circuit for use in high-resolution commercial smartphones, two additional pixel layouts using dual gate TFTs of T1 and T3 are used and the post-layout simulations are carried out. Fig. 12 shows the first pixel layout of the proposed circuit

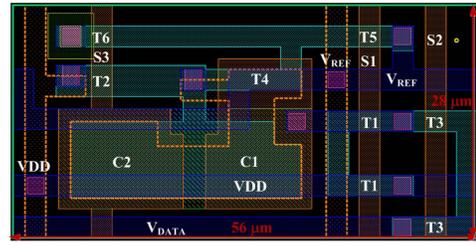


Fig. 12. Layout of the proposed pixel circuit with 454 ppi.

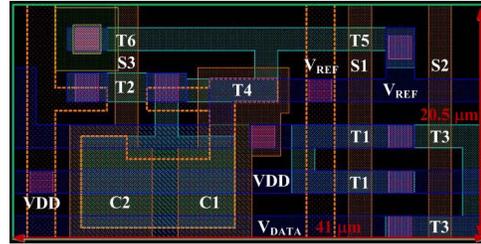


Fig. 13. Layout of the proposed pixel circuit with 620 ppi.

TABLE VI
PARAMETERS OF PROPOSED PIXEL CIRCUIT WITH 454 ppi

Parameter	Value	Parameter	Value
(W/L) _{T1, T3} (μm)	2.5/(2.5+2.5)	Cpa_vdd-S3 (fF)	0.2438
(W/L) _{T5, T6} (μm)	2.5/2.5	Cpa_vdd-A (fF)	5.1338
(W/L) _{T2} (μm)	3.75/2.5	Cpa_vdd-B (fF)	0.2438
(W/L) _{T4} (μm)	2.5/10	Cpa_vref-S3 (fF)	1.5113
C1 (fF)	120	Cpa_vref-A (fF)	4.2254
C2 (fF)	120	Cpa_vref-B (fF)	0.4875
Cpa_vdata-S3 (fF)	0.4063		

TABLE VII
PARAMETERS OF PROPOSED PIXEL CIRCUIT WITH 620 ppi

Parameter	Value	Parameter	Value
(W/L) _{T1, T3} (μm)	2/(2+2)	Cpa_vdata-B (fF)	0.52
(W/L) _{T5, T6} (μm)	2/2	Cpa_vdd-S3 (fF)	0.13
(W/L) _{T2} (μm)	2.5/2	Cpa_vdd-A (fF)	1.998
(W/L) _{T4} (μm)	2/8	Cpa_vdd-B (fF)	0.195
C1 (fF)	46	Cpa_vref-S3 (fF)	0.53
C2 (fF)	46	Cpa_vref-A (fF)	2.3175
Cpa_vdata-S3 (fF)	0.5363	Cpa_vref-B (fF)	0.26
Cpa_vdata-A (fF)	0.999		

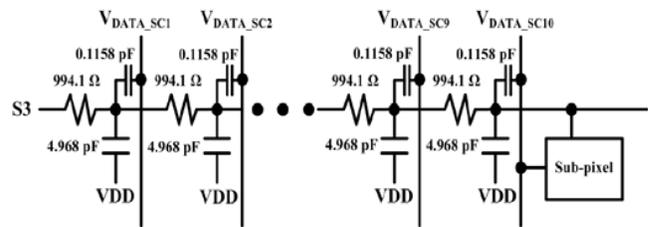
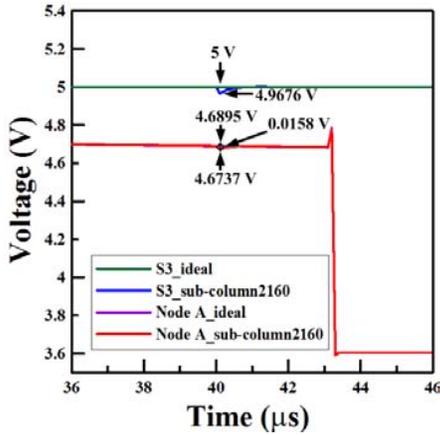
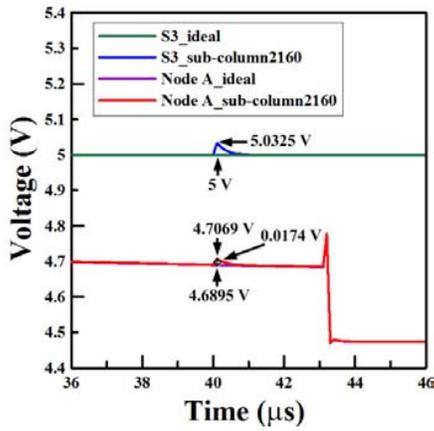


Fig. 14. Schematic of simulated condition of proposed pixel circuit with 620 ppi.

with 454 ppi, which is close to the 458 ppi of the iPhone X, and its corresponding parameters are shown in Table VI. Fig. 13 shows the second pixel layout of the proposed circuit



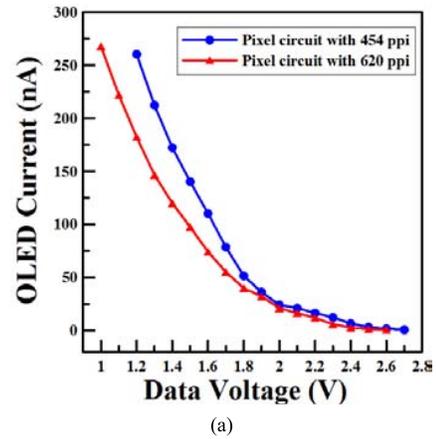
(a)



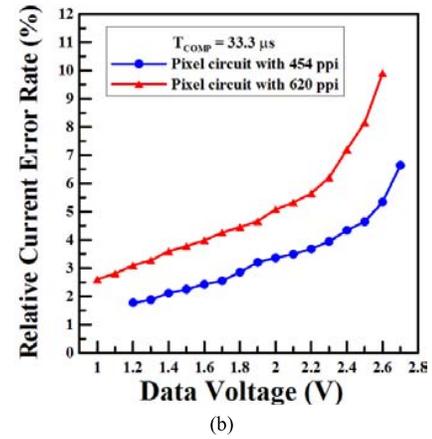
(b)

Fig. 15. Simulated transient waveforms of node A in the proposed pixel circuit and S3 control signal when V_{DATA} changes from (a) 2.6 to 1 V and (b) 1 to 2.6 V.

with 620 ppi, which is higher than 570 ppi of Galaxy S9, and its corresponding parameters are shown in Table VII. In the reset and emission stages, T_2 is turned on and V_{DD} stabilizes the voltage of node A. During the compensation and data input stages, T_2 is turned off and the node A is floating so its voltage may be distorted if the voltage on S3 varies. However, in the layout of the proposed pixel circuit with 620 ppi, C_1 and C_2 , which are 46 fF and 46 fF, are much larger than the parasitic capacitance between S3 and the data line in a sub-pixel, which is 0.5363 fF. Although thousands of data lines cross an S3 signal line, thousands of C_1 and C_2 in thousands of pixel circuits maintain the voltage on S3 during the compensation and data input stages. Thus, the voltage on S3 changes very slightly through the parasitic capacitance between S3 and the data lines. Furthermore, before the next change in the data voltage, the S3 is again quickly charged or discharged back to 5 V. Therefore, the voltage variation of node A is very small and so can be ignored. To verify this point, simulations were carried out with FHD resolution. Fig. 14 displays the simulated condition of the proposed pixel circuit, based on the pixel layout with 620 ppi. An S3 signal line is divided into 10 sections, and its corresponding resistance and capacitance



(a)



(b)

Fig. 16. (a) Transfer curves and (b) relative current error rates of proposed pixel circuit with 454 ppi and 620 ppi.

in each section are shown in Fig. 14. The voltage on all data lines changes from 2.6 to 1 V or from 1 to 2.6 V to simulate the worst case in which S3 exhibits possible voltage variation as a result of the parasitic capacitance between S3 and the data lines. The 2.6 and 1 V are the largest and smallest data voltages of the proposed pixel circuit with 620 ppi, corresponding to smallest and largest current levels, respectively, that are used in this paper. Fig. 15(a) and (b) shows the simulated voltages of node A, S3, and data signals of two sub-pixels, of which one is in the ideal condition without parasitic capacitance and the other sub-pixel is in the condition that is shown in Fig. 14. When the data voltage changes from 2.6 to 1 V as shown in Fig. 15(a), the largest voltage variation of node A is 0.0158 V. When the data voltage changes from 1 to 2.6 V as shown in Fig. 15(b), the largest voltage variation of node A is 0.0174 V. Also, these voltage variations decrease rapidly when S3 is charged or discharged back to 5 V. At the end of the compensation stage, the parasitic capacitance between S3 and the data lines in these two worst cases causes almost no variation of the voltage of node A. Therefore, the voltage variation of node A is confirmed to be very small to be ignored. Fig. 16(a) shows the transfer curves of the proposed pixel circuit with 454 and 620 ppi, indicating that the pixel circuits in this paper are compared based on an approximate driving

current range. Fig. 16(b) shows the relative current error rates of the proposed pixel circuit with 454 and 620 ppi, which range from 1.77% to 6.64% and 2.60% to 9.90%, respectively. The simulation results confirm that the proposed pixel circuit exhibits effective compensation when all parasitic capacitances and real values of $C1$ and $C2$ are considered.

IV. CONCLUSION

This paper presents a new pixel circuit that is based on the LTPS TFT backplane and overlapping compensation scheme. The circuit overlaps the compensation times of multiple rows to extend the sensing period for the precise extraction of variations of V_{TH} variations of the LTPS driving TFTs. The proposed pixel circuit turns off the OLEDs to avoid lighting of the display when the pixel circuits are not in emission stage, ensuring no flicker on the display. Three pixel circuits are compared by simulations, confirming that the proposed pixel circuit improves the uniformity of driving currents than those in the conventional 2T1C and 4T2C pixel circuits. A real 1.3-in panel is fabricated. The fabricated panel exhibits highly uniform red, green, and blue images. No line or spot defect is observed in the images with gray levels of 16 and 8 on the panel with the extended T_{COMP} of 33.3 μ s. Moreover, two additional pixel layouts with 454 and 620 ppi are provided. Post-layout simulations confirm that the proposed pixel circuit presents effective compensation for high-resolution commercial smartphones. Therefore, the proposed pixel circuit is suitable for use in mobile AMOLED displays.

REFERENCES

- [1] D. W. Kim, H. Oh, B. D. Youn, and D. Kwon, "Bivariate lifetime model for organic light-emitting diodes," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2325–2334, Mar. 2017.
- [2] C. Wang, Z. Hu, X. He, C. Liao, and S. Zhang, "One gate diode-connected dual-gate a-IGZO TFT driven pixel circuit for active matrix organic light-emitting diode displays," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3800–3803, Sep. 2016.
- [3] J. Genoe *et al.*, "Integrated line driver for digital pulse-width modulation driven AMOLED displays on flex," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 282–290, Jan. 2015.
- [4] H. Jung, Y. Kim, Y. Kim, C. Chen, and J. Kanicki, "A-IGZO TFT based pixel circuits for AM-OLED displays," in *SID Tech. Dig.*, 2012, pp. 1097–1100.
- [5] C. C. Wu *et al.*, "Integration of organic LEDs and amorphous Si TFTs onto flexible and lightweight metal foil substrates," *IEEE Electron Device Lett.*, vol. 18, no. 12, pp. 609–612, Dec. 1997.
- [6] X. Xu, R. A. Sporea, and X. Guo, "Source-gated transistors for power- and area-efficient AMOLED pixel circuits," *J. Display Technol.*, vol. 10, no. 11, pp. 928–933, Nov. 2014.
- [7] K.-Y. Lee and P. C.-P. Chao, "A new AMOLED pixel circuit with pulsed drive and reverse bias to alleviate OLED degradation," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1123–1130, Apr. 2012.
- [8] C.-L. Lin, P.-C. Lai, P.-C. Lai, P.-S. Chen, and W.-L. Wu, "Pixel circuit with parallel driving scheme for compensating luminance variation based on a-IGZO TFT for AMOLED displays," *J. Display Technol.*, vol. 12, no. 12, pp. 1681–1687, Dec. 2016.
- [9] C.-L. Lin *et al.*, "Optical pixel sensor of hydrogenated amorphous silicon thin-film transistor free of variations in ambient illumination," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2777–2785, Nov. 2016.
- [10] S.-H. Lee *et al.*, "Pixel architecture for low-power liquid crystal display comprising oxide and ferroelectric memory thin film transistors," *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 585–587, Jun. 2015.
- [11] Y.-K. Lo, K.-H. Wu, K.-J. Pai, and H.-J. Chiu, "Design and implementation of RGB LED drivers for LCD backlight modules," *IEEE Trans. Ind. Electron.*, vol. 56, no. 12, pp. 4862–4871, Dec. 2009.
- [12] J. H. Baek *et al.*, "A current-mode display driver IC using sample-and-hold scheme for QVGA full-color AMOLED displays," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2974–2982, Dec. 2006.
- [13] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, "Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1477–1486, Sep. 2004.
- [14] R. M. A. Dawson *et al.*, "The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays," in *IEDM Tech. Dig.*, Dec. 1998, pp. 875–878.
- [15] C.-L. Fan, Y.-C. Chen, C.-C. Yang, Y.-K. Tsai, and B.-R. Huang, "Novel LTPS-TFT pixel circuit with OLED luminance compensation for 3D AMOLED displays," *J. Display Technol.*, vol. 12, no. 5, pp. 425–428, May 2016.
- [16] C.-L. Lin, C.-C. Hung, P.-S. Chen, P.-C. Lai, and M.-H. Cheng, "New voltage-programmed AMOLED pixel circuit to compensate for nonuniform electrical characteristics of LTPS TFTs and voltage drop in power line," *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2454–2458, Jun. 2014.
- [17] C.-L. Lin, C.-C. Hung, W.-Y. Chang, M.-H. Cheng, P.-Y. Kuo, and Y.-C. Chen, "Voltage driving scheme using three TFTs and one capacitor for active-matrix organic light-emitting diode pixel circuits," *J. Display Technol.*, vol. 8, no. 10, pp. 602–608, Oct. 2012.
- [18] J.-S. Bang *et al.*, "A hybrid AMOLED driver IC for real-time TFT nonuniformity compensation," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 966–978, Apr. 2016.
- [19] W. Liu, G. Yao, C. Jiang, Q. Cui, and X. Guo, "A new voltage driving scheme to suppress non-idealities of polycrystalline thin-film transistors for AMOLED displays," *J. Display Technol.*, vol. 10, no. 12, pp. 991–994, Dec. 2014.
- [20] C.-L. Lin, W.-Y. Chang, and C.-C. Hung, "Compensating pixel circuit driving AMOLED display with a-IGZO TFTs," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1166–1168, Sep. 2013.
- [21] C.-L. Lin, K.-W. Chou, C.-C. Hung, and C.-D. Tu, "Lifetime amelioration for an AMOLED pixel circuit by using a novel AC driving scheme," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2652–2659, Aug. 2011.
- [22] A. Nathan, G. R. Chaji, and S. J. Ashtiani, "Driving schemes for a-Si and LTPS AMOLED displays," *J. Display Technol.*, vol. 1, no. 2, pp. 267–277, Dec. 2005.
- [23] J.-H. Lee, W. Nam, B.-K. Kim, H.-S. Choi, Y.-M. Ha, and M.-K. Han, "A new poly-Si TFT current-mirror pixel for active matrix organic light emitting diode," *IEEE Electron Device Lett.*, vol. 27, no. 10, pp. 830–833, Oct. 2006.
- [24] C.-L. Lin, P.-S. Chen, M.-H. Cheng, Y.-T. Liu, and F.-H. Chen, "A three-transistor pixel circuit to compensate for threshold voltage variations of LTPS TFTs for AMOLED displays," *J. Display Technol.*, vol. 11, no. 2, pp. 146–148, Feb. 2015.
- [25] J. P. Lee, H. S. Jeon, D. S. Moon, and B. S. Bae, "Threshold voltage and IR drop compensation of an AMOLED pixel circuit without a V_{DD} Line," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 72–74, Jan. 2014.
- [26] C.-H. Ho, C. Lu, and K. Roy, "An enhanced voltage programming pixel circuit for compensating GB-induced variations in poly-Si TFTs for AMOLED displays," *J. Display Technol.*, vol. 10, no. 5, pp. 345–351, May 2014.
- [27] W.-J. Wu, L. Zhou, M. Xu, L.-R. Zhang, R.-H. Yao, and J.-B. Peng, "An AC driving pixel circuit compensating for TFTs threshold-voltage shift and OLED degradation for AMOLED," *J. Display Technol.*, vol. 9, no. 7, pp. 572–576, Jul. 2013.
- [28] Y. Kim, J. Kanicki, and H. Lee, "An a-InGaZnO TFT pixel circuit compensating threshold voltage and mobility variations in AMOLEDs," *J. Display Technol.*, vol. 10, no. 5, pp. 402–406, May 2014.
- [29] G. R. Chaji and A. Nathan, "Low-power low-cost voltage-programmed a-Si:H AMOLED display for portable devices," *J. Display Technol.*, vol. 4, no. 2, pp. 233–237, Jun. 2008.
- [30] G. R. Chaji and A. Nathan, "Parallel addressing scheme for voltage-programmed active-matrix OLED displays," *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp. 1095–1100, May 2007.
- [31] B. Y. Chung *et al.*, "Driving method for a 2D-3D switchable AMOLED display using progressive or simultaneous emission," in *SID Tech. Dig.*, 2011, pp. 268–271.
- [32] N.-H. Keum, K. Oh, S.-K. Hong, and O.-K. Kwon, "A pixel structure using block emission driving method for high image quality in active matrix organic light-emitting diode displays," *J. Display Technol.*, vol. 12, no. 11, pp. 1250–1256, Nov. 2016.



Chih-Lung Lin (M'07) received the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1993 and 1999, respectively.

He is currently a Professor with the Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan. His current research interests include pixel circuits design for active matrix organic light-emitting diode, gate driver circuit design for AMLCD, and flexible display circuit.



Po-Cheng Lai received the B.S. degree in electrical engineering from Feng Chia University, Taichung, Taiwan, in 2014, and the M.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering with National Cheng Kung University, Tainan, Taiwan.

His current research interests include the pixel circuit design for active matrix organic light-emitting diode and gate driver circuit design for AMLCD.



Po-Chun Lai received the M.S. and Ph.D. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2013 and 2018, respectively.

He is currently with the AU Optronics Corporation, Hsinchu, Taiwan, working on the active matrix organic light-emitting diode (AMOLED) panel design. His current research interests include pixel circuit, gate driver circuit, and system design for AMOLED displays and AMLCDs.



Tsu-Yuan Lin received the M.S. degree in optoelectronic engineering from Dong Hwa University, Hualien, Taiwan, in 2010.

He was responsible for array and cell design. He is currently a Principal Engineer with the Department of AMOLED, AU Optronics Corporation, Hsinchu, Taiwan.



Li-Wei Shih received the M.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2000, where he is currently pursuing the Ph.D. degree in electrical engineering.

He is currently a Director with the Department of AMOLED, AU Optronics Corporation, Hsinchu, Taiwan.



Kuang-Hsiang Liu received the M.S. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2003.

He is currently a Senior Manager and a Principal Researcher with the Department of AMOLED, AU Optronics Corporation, Hsinchu.



Chia-Che Hung received the M.S. and Ph.D. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2010 and 2013, respectively.

He is currently with the AU Optronics Corporation, Hsinchu, Taiwan, working on the design of blue phase liquid crystal displays. His current research interests include pixel circuits and display system designs for active matrix organic light-emitting diodes.



Tsang-Hong Wang received the M.S. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2004.

He is currently a Senior Manager and a Principal Researcher with the Department of AMOLED, AU Optronics Corporation, Hsinchu.