

Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Operation for Ultra High Density Storage Devices

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Abstract

We propose Pipe-shaped Bit Cost Scalable (P-BiCS) flash memory which consists of pipe-shaped NAND strings folded like a U-shape instead of the straight-shape. P-BiCS flash technology achieves a highly reliable memory film of which the program and erase (P/E) operation is managed by Fowler-Nordheim (FN) tunneling, that is originated by the strong curvature effect of its small pipe radius, a low resistance source line by the layered metal wirings and a tightly controlled diffusion profile for the select-gate (SG) transistor due to low thermal budget. The effective 1-bit cell area of 0.00082 um^2 and its functionality are successfully demonstrated using the 32 Gbit test chip with the 3-dimensionally 16 stacked layers and the Multi-Level-Cell (MLC) operation by 60nm P-BiCS flash technology.

Introduction

Bit Cost Scalable (BiCS) technology has been developed as one of the promising candidates for the future ultra high density storage devices [1-5]. The punch and plug process forms a NAND string of vertical FETs with SONOS-type memories, which are sandwiched in between the lower and the upper select-gates (LSG/USG) [1]. Three critical issues to be resolved are as follows; (1) SiN-based tunnel film is implemented to minimize the damage by diluted-HF treatment for the "gate-first" process [2]; however the P/E window, the immunity to read disturb and the data retention are insufficient to operate it as a Multi-Level-Cell (MLC). (2) The high-resistance source line is hardly clamped on its initial voltage due to the large total current from a huge number of NAND strings during a read operation. (3) The LSG transistor is placed upon the heavily doped source diffusion and suffered from many thermal process steps for the memory-film formation; therefore the diffusion profile is not controllable.

In this paper, we propose P-BiCS flash memory to overcome the above issues and fabricate the 32 Gbit test chip; as a result, we demonstrate the feasibility of the P-BiCS flash technology for the future Tbit storage devices.

Proposal of P-BiCS flash memory

Figure 1 shows the schematic of P-BiCS flash memory. Two adjacent NAND strings are connected at the bottoms by so-called pipe-connection (PC) which is gated by the bottom electrode. One of the terminals for the U-shaped pipe is connected to the bit line (BL), and the other is bound by the source line (SL). The SL consists of the meshed wiring of the third level metal and accessed by the first and the second level metal like a conventional planar technology, therefore the resistance of the SL is sufficiently low. The both of the SG transistors are placed bellow the SL and the BL. The control-gate (CG) is isolated by the slits and faces to each other as a couple of combs pattern. The memory films consist of a block film, a charge trap film and the oxide-based film as a tunnel film. The implementation of the oxide-based tunnel-film is because the sequential processing from the

deposition of the tunnel film to the body silicon is applicable by the fabrication process for the P-BiCS NAND strings which is as shown below in detail.

Fabrication of P-BiCS NAND strings

The fabrication process of the P-BiCS NAND strings is described in Fig.2. Due to the sacrificial film process and the topological reason of the U-shaped pipe, the deposition of the memory films are sequentially followed by the deposition of the body silicon film deposition, therefore the surface of the tunnel film is not suffered by any pre-treatment. Figure 4 shows the cross-sectional SEM images for the 16 layered P-BiCS NAND strings fabricated by repeating the process steps for 8 layers. The diffusions of the SG transistors are formed after the fabrication of the P-BiCS NAND strings. The carrier concentration at the SG diffusion is measured by Scanning Spreading Resistance Microscopy (SSRM) [6] in Fig.3. The SG-diffusion profile of the P-BiCS is shallower and steeper because of the low thermal budget and no spreading and/or no auto-doping from the heavily doped source diffusion are indicated. Finally, the steps of 16 floors and the contact via to access to the CG are fabricated.

MLC operation with highly reliable memory films

Figures 5 and 6 show the P/E characteristics of the straight-shaped BiCS and that of the P-BiCS. The both of the P/E window and speed are dramatically improved by the P-BiCS memory films. Data retention is also compared between the both of the BiCS flashes in Fig.7. The data retention of P-BiCS shows almost no degradation after 10 years. Read disturb is measured as a function of read voltages in Fig. 8. The threshold voltage shift of P-BiCS is less than 0.3 V after 100k cycles of read operation with the read voltage of 7.5 V. The diameter dependence of the P/E window is measured on the test structure of cylindrical capacitors in Fig. 9. The P/E window is enlarged by the smaller hole, because the electric field strength of the tunnel film is enhanced by the curvature effect. Finally, the data retention of the MLC operation is examined. The data of the multi level show almost the constant threshold voltage during 10 years in Fig. 10. The data retention and the immunity to read disturb are considered to be sufficient for the MLC operation.

32 Gbit test chip using 60nm P-BiCS flash technology

The photograph in Fig. 11 shows the 32 Gbit test chip of the P-BiCS flash memory. The specification for the test chip is listed in Table I. 0.00082 um^2 of effective 1-bit cell area and its functionality are successfully demonstrated with 3-dimensionally 16 stacked layers and the MLC operation, which is enabled by the P-BiCS flash technology. We conclude that the P-BiCS flash memory is one of the most promising candidates for the future Tbit storage devices.

References

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- [3] H. Aochi et al., Ext. Abs. SSDM, pp820-821, 2008.
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 [6] L. Zhang et al, IEEE Electron Device Letter, Vol.29, Issue 7 pp.799-801, 2008.

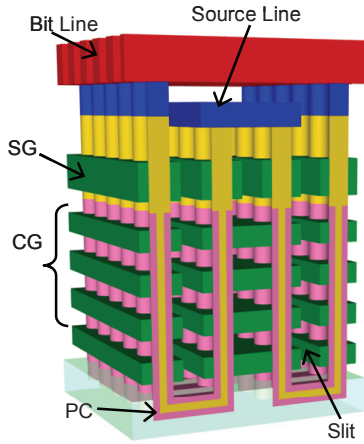


Fig. 1 Schematic of P-BiCS flash memory.

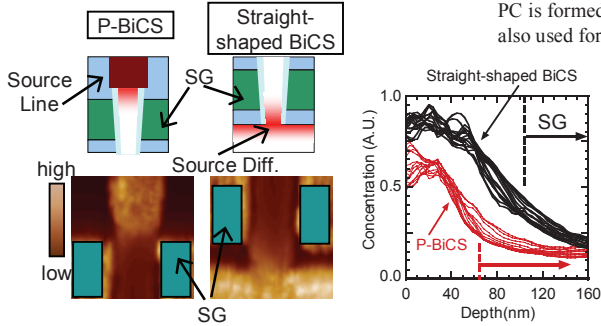


Fig. 3 Comparison of SG active-doping concentration between P-BiCS and straight-shaped BiCS. The doping profile of P-BiCS is steeper and shallower. The surface concentration of straight-shaped BiCS is high because of the diffusion from heavily doped source line.

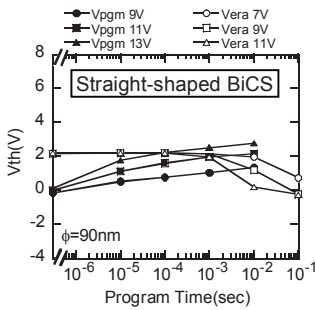


Fig. 5 P/E characteristics of straight-shaped BiCS with SONOS memory film.

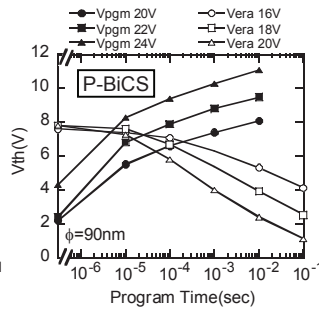


Fig. 6 P/E characteristics of P-BiCS with SONOS memory film.

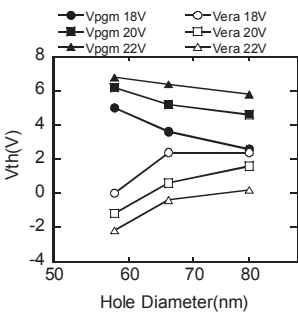


Fig. 9 Hole diameter dependence of P/E characteristics. The P/E window is enhanced by smaller hole.

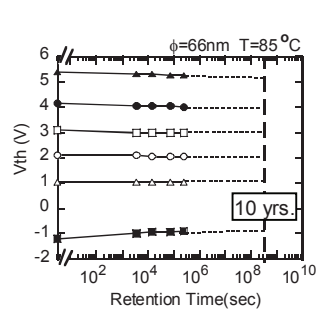


Fig. 10 Data retention for MLC operation.

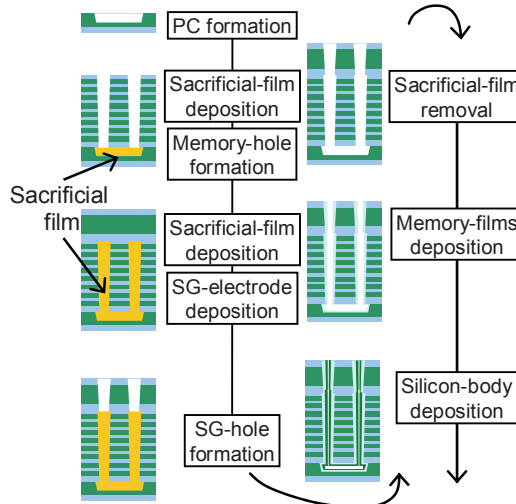


Fig. 2 Fabrication process of P-BiCS flash memory. PC is formed on the first-level gate-conductor which is also used for the support devices.

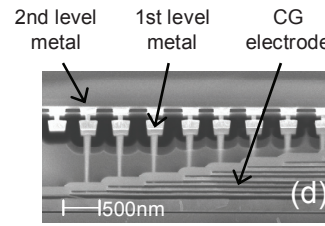


Fig. 4 Cross-sectional SEM image of 60nm P-BiCS flash memory and equivalent circuit. (a) Source line, bit line and select-gate (b) Memory hole after the removal of sacrificial film. (c) Pipe-connection. (d) Contact via for access to control-gate electrode.

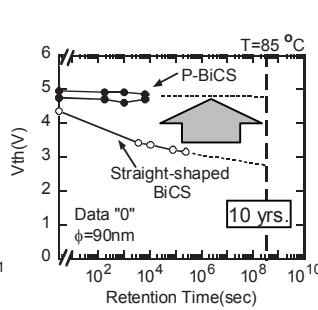


Fig. 7 Data retention of P-BiCS (solid circle) and straight-shaped BiCS (opened circle).

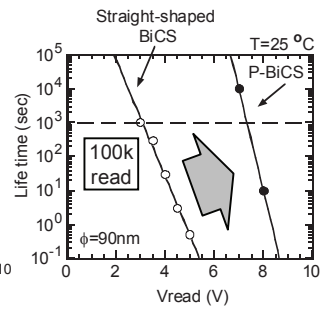


Fig. 8 Read disturb of P-BiCS (solid circle) and straight-shaped BiCS (opened circle).

TABLE I SPECIFICATION

Process	60 nm CMOS
Unit cell size	0.00082 μm^2
Memory films	O/N/O
Memory hole	66 nm
Control Gate stack	16 layer
String length	32 NAND
BEOL	3-metal (Al/Cu/W)

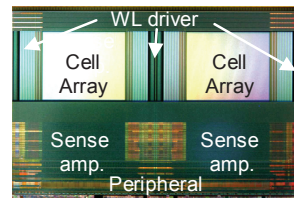


Fig. 11 Photograph of 32Gb P-BiCS flash memory.