Claim 27 is rejected under 35 U.S.C. 103 as being unpatentable over Dickinson et al. (US 7,251,386) in view of Kim et al. (US 2010/0288341) in view of Okamoto et al. (US 2010/0308428) in view of Iwai et al. (US 2009/0230498) in view of Ertel et al. (US 2013/0084044).

Regarding claim 27, Dickinson teaches the single-chip device of claim 1, however Dickinson does not teach:

- further comprising a light guide to said MSPD configured to bend the optical input from an initial propagation direction to a propagation direction transverse to said layers, and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip (output electrodes contained within 115).

Ertel teaches in Fig. 1A:

- further comprising a light guide to said MSPD configured to bend the optical input from an initial propagation direction to a propagation direction transverse to said layers (¶ 0042), and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip (I/O electrodes contained within 115).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made (for Pre-AIA) or before the effective filing date of the claimed invention (for the AIA FITF practice) to have used:

- further comprising a light guide to said MSPD configured to bend the optical input from an initial propagation direction to a propagation direction transverse to said layers, and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip,

in the invention of Dickinson et al. as taught by Benjamin, for the purpose of allowing for electrical and optical means of input and output of information with a flexible light coupling mechanism.

Claim 31 is rejected under 35 U.S.C. 103 as being unpatentable over Dickinson et al. (US 7,251,386) in view of Kim et al. (US 2010/0288341) in view of Okamoto et al. (US 2010/0308428) in view of Iwai et al. (US 2009/0230498) in view of Raj et al. (US 2013/0230272).

Regarding claim 31, Dickinson teaches the single-chip device of claim 1, however they do not teach:

- further comprising one or more additional active electronic circuits that are formed on or in the said single substrate and comprise one or more transimpedance amplifiers (TIAs) and one or more application specific integrated circuits (ASICs).

Raj teaches the use of ASICS (¶ 0054) and TIAs (¶ 0039) in optical electrical communication (¶ 0028) arrangements.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made (for Pre-AIA) or before the effective filing date of the claimed invention (for the AIA FITF practice) to have used:

- further comprising one or more additional active electronic circuits that are formed on or in the said single substrate and comprise one or more transimpedance amplifiers (TIAs) and one or more application specific integrated circuits (ASICs),

in the invention of Dickinson as taught by Raj, for the purpose of utilizing components which aid in the transfer of information switching between the optical signal domain and the electrical signal domain in a high frequency setting.

Claims 37 and 38 are rejected under 35 U.S.C. 103 as being unpatentable over Dickinson et al. (US 7,251,386) in view of Kim et al. (US 2010/0288341) in view of Okamoto et al. (US 2010/0308428) in view of Iwai et al. (US 2009/0230498) in view of Choi et al. (US 2010/0059789).

Regarding claims 37 and 38, Dickinson teaches the single-chip device of claim 1, however they do not teach:

- further including a deliberately textured surface at a side of one of said first and second layers facing away from the intermediate layer,

(and for claim 38) further including a layer of micro-nano structures formed at of one of said first and second facing, at a surface thereof facing away from the intermediate layer.

Choi teaches in many of the Figures including Fig. 9 which has one of the semiconductor layers (300) having a textured surface (220) that is formed away from the active region / intermediate layer (400), and further it is noted that the devices are on a nano scale and any features present will be of the nano size, Kim teaches this in paragraph 0043, wherein the device region is 426 or 325 nanometers, therefore a feature smaller than the device layer itself will be smaller than the noted dimensions of Kim).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made (for Pre-AIA) or before the effective filing date of the claimed invention (for the AIA FITF practice) to have used:

- further including a deliberately textured surface at a side of one of said first and second layers facing away from the intermediate layer,

(and for claim 38) further including a layer of micro-nano structures formed at of one of said first and second facing, at a surface thereof facing away from the intermediate layer,

in the invention of Dickinson et al. as taught by Choi, for the purpose of increasing light conversion efficiency.

Claim 40 is rejected under 35 U.S.C. 103 as being unpatentable over Dickinson et al. (US 7,251,386) in view of Kim et al. (US 2010/0288341) in view of Okamoto et al. (US 2010/0308428) in view of Iwai et al. (US 2009/0230498) in view of Sahura et al. (US 6,392,282).

Regarding claim 40, Dickinson teaches the single-chip device of claim 1, however they do not teach:

- further including an isolation trench between the MSPD and the active electronic circuit.

Sahura teaches in Fig. 3A wherein the locos shallow trenches are formed between avalanche photodiode and the circuit active region.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made (for Pre-AIA) or before the effective filing date of the claimed invention (for the AIA FITF practice) to have used:

- further including an isolation trench between the MSPD and the active electronic circuit,

in the invention of Dickinson et al. as taught by Sahura, for the purpose of preventing crosstalk between device intended to function separately.

Claim 42 is rejected under 35 U.S.C. 103 as being unpatentable over Dickinson et al. (US 7,251,386) in view of Kim et al. (US 2010/0288341) in view of Okamoto et al. (US 2010/0308428) in view of Iwai et al. (US 2009/0230498) in view of Tian et al. (US 2008/0080854).

Regarding claim 42, Dickinson et al. teaches the single-chip device of claim 1, however they do not teach:

- wherein the optical input and the electrical output are each modulated at a frequency of at least 30 Gigabits per second.

Tian teaches a device with optical signal frequency operating speeds as claimed in paragraph 0022.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made (for Pre-AIA) or before the effective filing date of the claimed invention (for the AIA FITF practice) to have used:

- wherein the optical input and the electrical output are each modulated at a frequency of at least 30 Gigabits per second,

in the invention of Dickinson as taught by Tian, for the purpose of improving data transfer rates in the device.

Claim 43 is rejected under 35 U.S.C. 103 as being unpatentable over Dickinson et al. (US 7,251,386) in view of Kim et al. (US 2010/0288341) in view of Okamoto et al. (US 2010/0308428) in view of Iwai et al. (US 2009/0230498) in view of Nakaji et al. (US 2009/0321868).

Regarding claim 43, Dickinson et al. teaches the single-chip device of claim 1, however they do not teach:

- wherein the quantum efficiency of the MSPD that is at least 1.5 times greater than that of an otherwise same photodetector that does not include said holes.

Nikaji teaches in Fig. 5 and 6, a pin photodiode device with optical efficiencies reaching as high 80 plus percent. Further the holes added by Kim would only improve the efficiency above the 80 percent shown by Nikaji.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made (for Pre-AIA) or before the effective filing date of the claimed invention (for the AIA FITF practice) to have used:

- wherein the quantum efficiency of the MSPD that is at least 1.5 times greater than that of an otherwise same photodetector that does not include said holes,

in the invention of Dickinson et al. as taught by Nikaji, for the purpose of improving the sensitivity of the detector.

Claim 44 is rejected under 35 U.S.C. 103 as being unpatentable over Dickinson et al. (US 7,251,386) in view of Kim et al. (US 2010/0288341) in view of Okamoto et al. (US 2010/0308428) in view of Iwai et al. (US 2009/0230498) in view of Firth et al. (US 2013/0114629).

Regarding claim 44, Dickinson et al. teaches the single-chip device of claim 1, however they do not teach:

- further including a hermetic seal integral with the device.

Firth teaches in paragraph 0057 where it is discussed that the optical and electrical package is hermetically sealed.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made (for Pre-AIA) or before the effective filing date of the claimed invention (for the AIA FITF practice) to have used:

- further including a hermetic seal integral with the device,

in the invention of Dickinson et al. as taught by Firth, for the purpose of preventing mechanical damage or environmental corrosion.

Allowable Subject Matter

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. While the prior art teaches using overlying layers over the device layers, the prior art does not teach the overlying layer has holes that match with the holes of the device, and therefore does not teach, "in which said overlying layer is present as a superstrate at one side of said first, intermediate, and second layers, and contains said holes".

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach, "in which at least some of said holes differ from each other in at least one of (i) distance by which the holes extend in said directions, (ii) shape of the holes, and (iii) spacing of the holes from each other".

Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach, "in which the holes are in the intermediate layer and wherein one of said first and second layers conformally covers inside walls of the holes as well as spaces between the holes".

Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach, "in which the MSPD further includes ohmic contacts to said first and second layers, at least one of said ohmic contact being through a via in said substrate".

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the

form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-40 and 42-44 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-28 of U.S. Patent No. 9,525,084 and claims 1-30 of U.S. Patent No. 9,530,905. Although the claims at issue are not identical, they are not patentably distinct from each other because the claims share each limitation contained therein.

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571)272-8797. The examiner can normally be reached on M-F, 9 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571)272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eduardo A. Rodela/, Primary Examiner, Art Unit 2893

Notice of References Cited	Application/Control No. 15/797,821	Applicant(s)/Patent Under Reexamination WANG ET AL.	
	Examiner Eduardo A. Rodela	Art Unit 2893	Page 1 of 2

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	15797821
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First Named Inventor	Shih-Yuan WANG et al.
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Examiner Name	
Attorney Docket Number	5176/88184-CIP

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15797821
	Filing Date	2017-10-30
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	5176/88184-CIP

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	First Named Inventor	Shih-Yuan WANG et al.
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	Attorney Docket Number	5176/88184-CIP

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	First Named Inventor	Shih-Yuan WANG et al.
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	Examiner Name	
	Attorney Docket Number	5176/88184-CIP

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Examiner Signature	/EDUARDO A RODELA/	Date Considered	07/18/2018

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	225	(optical same electrical same communication same circuit$1) and ((optical or light) with fiber with (curve or bend))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/07/1 10:22
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L6	112	(US-20160126381-$ or US-20060082318-$ or US-20110291103-$ or US-20110165707-$ or US-20120021525-$ or US-20100288341-$ or US-20060220000-$ or US-20080179503-$ or US-20080050081-$ or US-20050053319-$ or US-20060289960-$ or US-20020175339-$ or US-20140286367-$ or US-20120153260-$ or US-20110267612-$ or US-20080095663-$ or US-20090225804-$ or US-20090203158-$ or US-20080107388-$ or US-20030218143-$ or US-20030127608-$ or US-20030123827-$ or US-20090278125-$ or US-20120044489-$ or US-20090183774-$ or US-20090141489-$).did. or (US-20070014505-$ or US-20020101895-$ or US-20030016895-$ or US-20130056623-$ or US-20080303033-$ or US-20120292676-$ or US-20100221866-$ or US-20100193768-$ or US-20090267049-$ or US-20080248608-$ or US-20050184354-$ or US-20100284432-$ or US-20070013991-$ or US-20180102442-$ or US-20160307939-$ or US-20150144797-$ or US-20130089888-$ or US-20100308428-$ or US-20090230498-$ or US-20090152664-$ or US-20140341506-$ or US-20050063634-$ or US-20050117853-$ or US-20040149998-$ or US-20130084044-$).did. or (US-7239001-$ or US-8319241-$ or US-6687423-$ or US-6295130-$ or US-5329136-$ or US-9419156-$ or US-9312448-$ or US-9099623-$ or US-8796716-$ or US-8785955-$ or US-8754445-$ or US-8604511-$ or US-8160404-$ or US-7683310-$ or US-6879014-$ or US-6316286-$ or US-6043517-$ or US-7973377-$ or US-7579668-$ or US-6858912-$ or US-5942789-$ or US-3914137-$ or US-8372726-$ or US-6359283-$ or US-5451767-$ or US-8436370-$).did. or (US-7079307-$ or US-9082922-$ or US-4894526-$ or US-4873555-$ or US-7067853-$ or US-5698858-$ or US-6549684-$ or US-4961198-$ or US-4952791-$ or US-4754132-$ or US-6667528-$ or US-8357960-$ or US-7183127-$ or US-7986022-$ or US-7919347-$ or US-6943409-$ or US-8670637-$ or US-8461541-$ or US-7489014-$ or US-7560784-$ or US-6538299-$ or US-6451702-$ or US-6404031-$ or US-5818066-$ or US-4814847-$ or US-6027956-$ or US-5757057-$).did. or (US-5625636-$ or US-9214787-$ or US-6711200-$ or US-9042418-$ or US-7915604-$ or US-7994521-$ or US-8462827-$ or US-7251386-$).did.	US-PGPUB; USPAT	OR	OFF	2018/07/1 12:42
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L8	662	(optical same electrical same communication same circuit$1) and (hermet$2 or hermit$2 or hermitically or hermetically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/07/1 12:44
L9	799	(optical same electrical same communication same circuit$1) and (hermet$2 or hermit$2 or hermitically or hermetically)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 12:44
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L25	3	(quantum adj efficiency) same (pin adj photodiode) same (percent or "%")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 17:16
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L27	56	((quantum adj efficiency) same (percent or "%")) and (pin with photodiode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 17:16
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L30	18	(@pd<="20130522" or @rlpd<="20130522" or @ad<="20130522" or @rlad<="20130522") and l29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 17:26
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L37	4	W&WSens.as. and wang.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 17:55
S1	5	(micro near (cavity or structure or aperture$1 or hole$1)) with absorption with ((light or photo or radiation or wavelength) near (sensitive or sensing or sensor or pick-up or detect$ion or transduc$1 or conversion or converting))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:31
S2	15	("20020163643" | "20030020926" | "5022745" | "5291502" | "5329136" | "5629951" | "5646729" | "6295130" | "6665076" | "6687423" | "7095776").PN. OR ("7239001").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/09/1 09:32
S3	36214	H01L31/00,02,0216,02161,02164,02165,0232,02327,0236,02363,02366,,035281,06,09,10,101,102,11.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/09/1 09:40
S4	653	(micro near (cavity or structure or aperture$1 or hole$1)) with absorption	US-PGPUB;	OR	ON	2016/09/1

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			09:40
S5	7	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S4 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:41
S6	128707	apd or (avalanche near photo near diode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:44
S7	40550	micro adj (cavity or structure or aperture$1 or hole$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:44
S8	100	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S6 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:44
S9	6	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S6 and S7 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:44
S10	10	398/115.ccls. and apd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 10:25
S11	10	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 10:25
S12	8	"945003".ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 10:37
S13	58821	(photon or photo or light) near (detect$3 or absorb$3 or sens$3 or sensitive or transduc$3 or convers$3 or convert$3) with (diode or P-I-N)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:38
S14	12532630	holes or cavities or apertures	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:39
S15	1469	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and ("SiGe" or (silicon near germanium)) and S13 and S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:40
S16	575288	communicat$3 with (optical or light)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2016/09/2 08:42

			EPO; JPO; DERWENT; IBM_TDB			
S17	63533	broad near band	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:42
S18	70	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and ("SiGe" or (silicon near germanium)) and S13 and S14 and S16 and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:42
S19	6	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and (("SiGe" or (silicon near germanium)) same S13 same S14) and S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:44
S20	25	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and (("SiGe" or (silicon near germanium)) same S13 same S14)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:45
S21	181	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and ("SiGe" or (silicon near germanium)) and (S13 same S14)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:45
S22	78	rodela.xp. and optical	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:55
S23	7675	optical near confinement	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:59
S24	6400	photonic near band near gap	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:59
S25	263	S23 and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:59
S26	263	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and S25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:00
S27	168254	("SiGe" or (silicon near germanium))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:02
S28	263	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and S25 and S23 and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:02

S29	18	("4959694" | "5942789").PN. OR ("6043517").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/09/2 09:14
S30	60737	(photon or photo or light) near (detect$3 or absorb$3 or sens$3 or sensitive or transduc$3 or convers$3 or convert$3) with (apd or (avalanche near photo) or diode or P-I-N)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:32
S31	34	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and (S24 same S30)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:33
S32	164	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and S24 and S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:35
S33	25	(892821|943898).ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 10:10
S34	60828	(photon$2 or photo or light) near (detect$3 or absorb$3 or sens$3 or sensitive or transduc$3 or convers$3 or convert$3) with (apd or (avalanche near photo) or diode or P-I-N)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 10:21
S35	11803	photonic with (cavit$3 or hole or aperture$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 10:21
S36	349	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and S34 and S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 10:21
S37	7	(8436370|5451767).pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 10:39
S38	21	(8604511|20030127608|20030016895).pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 10:42
S39	3	(8604511|20030127608|20030016895).pn.	US-PGPUB; USPAT	OR	ON	2016/09/2 10:42
S40	57778	pin with diode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/0 17:03
S41	2259363	(photo or light) with (detect$3 or sens$3 or sensitive or conversion or convert$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/0 17:04
S42	7137	S40 same S41	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/10/0 17:06

			DERWENT; IBM_TDB			
S43	5289	S40 with S41	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/0 17:06
S44	406	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S43 and photonic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/0 17:07
S45	150	("7397101" | "7795064" | "7893346" | "20050092925" | "20050184354" | "20080248608" | "20120292676" | "20140001528" | "6027956" | "6177289" | "7397101" | "7495306" | "5457327" | "20070190434" | "4571559" | "5625636" | "7601597" | "20070092192" | "7674563" | "20090188557" | "20100193768" | "5757057" | "8436370" | "20080265449" | "7501597" | "8129710" | "20080047604" | "5451767" | "7115971" | "7898052" | "20100126548" | "7115971" | "20081012582" | "20100029067" | "20100221866" | "4637129" | "7972934" | "8129710" | "20050184354" | "20060218740" | "20070092192" | "20080218740" | "20090267049" | "20100197068" | "20100313941" | "20120193676" | "20130207222" | "457327A" | "5886374" | "6667528" | "7893348" | "20090188557" | "20160225631" | "4716449" | "7674563" | "7772615" | "20050092925" | "20100193766" | "20100197068" | "4637129" | "20080265449" | "20100126548" | "20150041965" | "7795064" | "8114695").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/0 08:51
S46	11	("5451767" | "5504365" | "5698858" | "6331911" | "6483094" | "6794628" | "7067853" | "7079307" | "7196390" | "7842957").PN. OR ("8436370").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/0 09:36
S47	16	("4873555" | "4894526" | "5567955" | "5892222" | "6028323" | "6563627" | "6768827" | "6819476").PN. OR ("7079307").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/0 09:38
S48	21	("4546244" | "4716449" | "4754132" | "4952791" | "4961198" | "5020153").PN. OR ("5451767").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/0 10:22
S49	29	("4815087" | "4815090" | "4820655" | "4829535").PN. OR ("4961198").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/0 10:25
S50	45	("4814847" | "4829013" | "5600130" | "5818066" | "5973260" | "6107643" | "6177289" | "6388301" | "6404031" | "6429463" | "6451702" | "6486522").PN. OR ("6667528").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/0 10:31
S51	11	("20050255581" | "20070158661" | "20070210349" | "20080105296" | "4814847" | "5266814" | "6667528" | "7015139" | "7132677" | "7183127").PN. OR ("8357960").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/0 10:40
S52	26	("4916087" | "5294562" | "6177289" | "6218262" | "6261623" | "6287974" | "6451702" | "6538299" | "6667528" | "6707075" | "6828626").PN. OR ("6943409").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/0 11:02
S53	2	"8357960".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/10/0 09:29
S54	1	"5528056".pn.	USPAT	OR	OFF	2016/10/0 16:30
S55	0	(wang near shih near yuan).in. and (W&W near sens).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/10/1 11:21
S58	1	"9112103".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/1 12:32
S59	2	"20050118795"	US-PGPUB; USPAT; USOCR	OR	OFF	2016/10/1 12:48
S60	1	"20100288341"	USPAT	OR	OFF	2018/07/1 08:38
S61	2	"20100288341"	US-PGPUB; USPAT	OR	OFF	2018/07/1 08:39
S62	4	("2010/0288341").URPN.	USPAT	OR	OFF	2018/07/1 08:58
S63	6	("20040135155" | "20070013991" | "20100284432" | "20100288341" | "6643439" | "6711200").PN. OR ("9214787").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/1 09:03
S64	114	("5229320" | "5482890" | "5663592" | "6028693" | "6151347" | "6366598").PN. OR ("6711200").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/1 09:06
S65	47	("20020041749" | "20020048422" | "5784400" | "5999308" | "6130969" | "6175671" | "6381389" | "6468823" | "6532326").PN. OR ("6643439").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/1 10:21

S66	3	"20100288341" or "7251386".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/1 11:24
S67	26809	(amplify or amplification) with (light or optical) with signal	US-PGPUB; USPAT; USOCR	OR	OFF	2018/07/1 14:36
S68	100	(US-20160126381-$ or US-20060082318-$ or US-20110291103-$ or US-20110165707-$ or US-20120021525-$ or US-20100288341-$ or US-20060220000-$ or US-20080179503-$ or US-20080050081-$ or US-20050053319-$ or US-20060289960-$ or US-20020175339-$ or US-20140286367-$ or US-20120153260-$ or US-20110267612-$ or US-20080095663-$ or US-20090225804-$ or US-20090203158-$ or US-20080107388-$ or US-20030218143-$ or US-20030127608-$ or US-20030123827-$ or US-20090278125-$ or US-20120044489-$ or US-20090183774-$ or US-20090141489-$).did. or (US-20070014505-$ or US-20020101895-$ or US-20030016895-$ or US-20130056623-$ or US-20080303033-$ or US-20120292676-$ or US-20100221866-$ or US-20100193768-$ or US-20090267049-$ or US-20080248608-$ or US-20050184354-$ or US-20100284432-$ or US-20070013991-$).did. or (US-7239001-$ or US-8319241-$ or US-6687423-$ or US-6295130-$ or US-5329136-$ or US-9419156-$ or US-9312448-$ or US-9099623-$ or US-8796716-$ or US-8785955-$ or US-8754445-$ or US-8604511-$ or US-8160404-$ or US-7683310-$ or US-6879014-$ or US-6316286-$ or US-6043517-$ or US-7973377-$ or US-7579668-$ or US-6858912-$ or US-5942789-$ or US-3914137-$ or US-8372726-$ or US-6359283-$ or US-5451767-$ or US-8436370-$).did. or (US-7079307-$ or US-9082922-$ or US-4894526-$ or US-4873555-$ or US-7067853-$ or US-5698858-$ or US-6549684-$ or US-4961198-$ or US-4952791-$ or US-4754132-$ or US-6667528-$ or US-8357960-$ or US-7183127-$ or US-7986022-$ or US-7919347-$ or US-6943409-$ or US-8670637-$ or US-8461541-$ or US-7489014-$ or US-7560784-$ or US-6538299-$ or US-6451702-$ or US-6404031-$ or US-5818066-$ or US-4814847-$ or US-6027956-$ or US-5757057-$).did. or (US-5625636-$ or US-9214787-$ or US-6711200-$ or US-9042418-$ or US-7915604-$ or US-7994521-$ or US-8462827-$ or US-7251386-$).did.	US-PGPUB; USPAT	OR	OFF	2018/07/1 14:36
S69	6	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S67 and S68	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 14:36
S70	43887	H01L31/00,02,0216,02161,02164,02165,0232,02327,0236,02363,02366,,035281,06,09,10,101,102,11.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/07/1 14:43
S71	188	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S67 and S70	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 14:43
S72	106	(US-20160126381-$ or US-20060082318-$ or US-20110291103-$ or US-20110165707-$ or US-20120021525-$ or US-20100288341-$ or US-20060220000-$ or US-20080179503-$ or US-20080050081-$ or US-20050053319-$ or US-20060289960-$ or US-20020175339-$ or US-20140286367-$ or US-20120153260-$ or US-20110267612-$ or US-20080095663-$ or US-20090225804-$ or US-20090203158-$ or US-20080107388-$ or US-20030218143-$ or US-20030127608-$ or US-20030123827-$ or US-20090278125-$ or US-20120044489-$ or US-20090183774-$ or US-20090141489-$).did. or (US-20070014505-$ or US-20020101895-$ or US-20030016895-$ or US-20130056623-$ or US-20080303033-$ or US-20120292676-$ or US-20100221866-$ or US-20100193768-$ or US-20090267049-$ or US-20080248608-$ or US-20050184354-$ or US-20100284432-$ or US-20070013991-$ or US-20180102442-$ or US-20160307939-$ or US-20150144797-$ or US-20130089888-$ or US-20100308428-$ or US-20090230498-$).did. or (US-7239001-$ or US-8319241-$ or US-6687423-$ or US-6295130-$ or US-5329136-$ or US-9419156-$ or US-9312448-$ or US-9099623-$ or US-8796716-$ or US-8785955-$ or US-8754445-$ or US-8604511-$ or US-8160404-$ or US-7683310-$ or US-6879014-$ or US-6316286-$ or US-6043517-$ or US-7973377-$ or US-7579668-$ or US-6858912-$ or US-5942789-$ or US-3914137-$ or US-8372726-$ or US-6359283-$ or US-5451767-$ or US-8436370-$).did. or (US-7079307-$ or US-9082922-$ or US-4894526-$ or US-4873555-$ or US-7067853-$ or US-5698858-$ or US-6549684-$ or US-4961198-$ or US-4952791-$ or US-4754132-$ or US-6667528-$ or US-8357960-$ or US-7183127-$ or US-7986022-$ or US-7919347-$ or US-6943409-$ or US-8670637-$ or US-8461541-$ or US-7489014-$ or US-7560784-$ or US-6538299-$ or US-6451702-$ or US-6404031-$ or US-5818066-$ or US-4814847-$ or US-6027956-$ or US-5757057-$).did. or (US-5625636-$ or US-9214787-$ or US-6711200-$ or US-9042418-$ or US-7915604-$ or US-7994521-$ or US-8462827-$ or US-7251386-$).did.	US-PGPUB; USPAT	OR	OFF	2018/07/1 17:25
S73	92	S72 and (silicon or germanium or sige)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/07/1 17:25
S74	106	(US-20160126381-$ or US-20060082318-$ or US-20110291103-$ or US-20110165707-$ or US-20120021525-$ or US-20100288341-$ or US-20060220000-$ or US-20080179503-$ or US-20080050081-$ or US-20050053319-$ or US-20060289960-$ or US-20020175339-$ or US-20140286367-$ or US-20120153260-$ or US-20110267612-$ or US-20080095663-$ or US-20090225804-$ or US-20090203158-$ or US-20080107388-$ or US-20030218143-$ or US-20030127608-$ or US-20030123827-$ or US-20090278125-$ or US-20120044489-$ or US-20090183774-$ or US-20090141489-$).did. or (US-20070014505-$ or US-20020101895-$ or US-20030016895-$ or US-20130056623-$ or US-20080303033-$ or US-20120292676-$ or US-20100221866-$ or US-20100193768-$ or US-20090267049-$ or US-20080248608-$ or US-20050184354-$ or US-20100284432-$ or US-20070013991-$ or US-20180102442-$ or US-20160307939-$ or US-20150144797-$ or US-20130089888-$ or US-20100308428-$ or US-20090230498-$).did. or (US-7239001-$ or US-8319241-$ or US-6687423-$ or US-6295130-$ or US-5329136-$ or US-9419156-$ or US-9312448-$ or US-9099623-$ or US-8796716-$ or US-8785955-$ or US-8754445-$ or US-8604511-$ or US-8160404-$ or US-7683310-$ or US-6879014-$ or US-6316286-$ or US-6043517-$ or US-7973377-$ or US-7579668-$ or US-6858912-$ or US-5942789-$ or US-3914137-$ or US-	US-PGPUB; USPAT	OR	OFF	2018/07/1 16:24

		8372726-$ or US-6359283-$ or US-5451767-$ or US-8436370-$).did. or (US-7079307-$ or US-9082922-$ or US-4894526-$ or US-4873555-$ or US-7067853-$ or US-5698858-$ or US-6549684-$ or US-4961198-$ or US-4952791-$ or US-4754132-$ or US-6667528-$ or US-8357960-$ or US-7183127-$ or US-7986022-$ or US-7919347-$ or US-6943409-$ or US-8670637-$ or US-8461541-$ or US-7489014-$ or US-7560784-$ or US-6538299-$ or US-6451702-$ or US-6404031-$ or US-5818066-$ or US-4814847-$ or US-6027956-$ or US-5757057-$).did. or (US-5625636-$ or US-9214787-$ or US-6711200-$ or US-9042418-$ or US-7915604-$ or US-7994521-$ or US-8462827-$ or US-7251386-$).did.				
S75	20	avalanche and S74	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 16:25
S76	1	"7251386".pn.	USPAT	OR	OFF	2018/07/1 08:59
S77	325	(optical same electrical same communication same circuit$1) and ((optical or light) with (band adj pass))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2018/07/1 09:03
S78	317	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S77	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/1 09:04

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S56	0	H01L31/00,02,0216,02161,02164,02165,0232,02327,0236,02363,02366,035281,06,09,10,101,102,11.cpc. and ((integrated)(detector)(processor)(data)(communication)(photodetector)(microstructure)(enhanced)(photoabsorption)(single)(semiconductor)(chip)(photon near absorbing)(region)(optical near source near signal)(output)(electrical near signal)(I-region)(p-region)(n-region)(plural)(number)(holes)).clm.	US-PGPUB; USPAT	AND	ON	2016/10/13 11:06
S57	0	(wang near shih near yuan).in. and (W&W near sens).as.	US-PGPUB; USPAT	AND	ON	2016/10/13 11:20

7/18/2018 5:56:08 PM
C:\Users\erodela\Documents\EASTold\EAST\Workspaces\15797821.wsp

Dkt. 5176/88184-CIP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG et al. Application No.: 15/797,821

Filed: October 30, 2017 Confirmation No.: 1009

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

This correspondence is being transmitted by facsimile transmission and/or EFS-Web to the U.S. Patent and Trademark Office.

/Maria Antonakis/ April 25, 2018
Maria Antonakis Date

30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO OFFICE ACTION MAILED 04/13/2018

The Office Action mailed April 13, 2018 requires an election of one of two groups of claims and a possible election of species.

In response and without traverse:

Applicants elect Group I (claims 1-40 and 42-80); and

Further elect Species II (claims 1-40 and 42-44, which recite, *inter alia*, an "active electronic circuit on or in said single substrate.")

Applicants submit that dependent claims 41 should also be included in the elected claims.

Applicants further submit that claim 77 (when re-written to incorporate its parent claim 45) also should be included in the elected claims because it recites "one of more active electronic circuits formed on or in said substrate."

If a petition for an extension of time is required to make this response timely, this paper should be taken as such petition. The Patent Office is hereby authorized to charge any fees that are required in connection with this response, and to credit any overpayment, to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

/IVAN KAVRUKOV/

Ivan Kavrukov, Reg. 25, 161
Attorney for Applicant
COOPER & DUNHAM LLP
30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

Electronic Acknowledgement Receipt

EFS ID:	32442602
Application Number:	15797821
International Application Number:	
Confirmation Number:	1009
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/MARIA ANTONAKIS
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176/88184-CIP
Receipt Date:	25-APR-2018
Filing Date:	30-OCT-2017
Time Stamp:	15:15:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	ResponseToRestriction_88184-CIP.pdf	94606 20627888c17bf63c7299bf9c3f1fc0a2112ef6b3	no	2

Warnings:

Information:	
Total Files Size (in bytes):	94606

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Notice of References Cited	Application/Control No. 15/797,821	Applicant(s)/Patent Under Reexamination WANG ET AL.	
	Examiner Eduardo A. Rodela	Art Unit 2893	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2012/0279553 A1	11-2012	Shigeta; Hiroaki	H01L31/035281	136/246
*	B	US-2009/0008735 A1	01-2009	Ogino; Masaya	H01L27/14601	257/436
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/797,821	10/30/2017	Shih-Yuan WANG	5176/88184-CIP	1009

23432 7590 04/13/2018

COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
04/13/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 15/797,821	Applicant(s) WANG ET AL.	
	Examiner Eduardo A. Rodela	Art Unit 2893	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/30/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-112* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-112* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communications received October 30, 2017. Claims 1-112 are under consideration.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

REQUIREMENT FOR UNITY OF INVENTION

As provided in 37 CFR 1.475(a), a national stage application shall relate to one invention only or to a group of inventions so linked as to form a single general inventive concept ("requirement of unity of invention"). Where a group of inventions is claimed in a national stage application, the requirement of unity of invention shall be fulfilled only when there is a technical relationship among those inventions involving one or more of the same or corresponding special technical features. The expression "special technical features" shall mean those technical features that define a contribution which each of the claimed inventions, considered as a whole, makes over the prior art.

The determination whether a group of inventions is so linked as to form a single general inventive concept shall be made without regard to whether the inventions are claimed in separate claims or as alternatives within a single claim. See 37 CFR 1.475(e).

WHEN CLAIMS ARE DIRECTED TO MULTIPLE CATEGORIES OF INVENTIONS

As provided in 37 CFR 1.475(b), a national stage application containing claims to different categories of invention will be considered to have unity of invention if the claims are drawn only to one of the following combinations of categories:

(1) A product and a process specially adapted for the manufacture of said product; or

(2) A product and process of use of said product; or

(3) A product, a process specially adapted for the manufacture of the said product, and a use of the said product; or

(4) A process and an apparatus or means specifically designed for carrying out the said process; or

(5) A product, a process specially adapted for the manufacture of the said product, and an apparatus or means specifically designed for carrying out the said process.

Otherwise, unity of invention might not be present. See 37 CFR 1.475(c).

Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in reply to this action, to elect a single invention to which the claims must be restricted.

- Group I, independent claims 1 and 45 with dependent claims 2-40 and 42-80, drawn to an apparatus of a light sensing device for conversion to electrical signal.

- Group II, claims 81-112, drawn to a method of making an apparatus of a light sensing device for conversion to electrical signal.

Both groups (claims 1, 45 and claim 17) share a common technical feature of:

1) a microstructure-enhanced photodetector with continuous layers of the first doped layer, the second doped layer and the less doped intermediate layer,

2) holes formed in the above mentioned layers extending transverse to the layers,

3) a region of optical input,

4) a region of electrical output,

5) (for claim 1, not claim 45) the active electronic circuit that processes the optical device's electrical output.

This common technical feature is known in the prior art. Shigeta et al. (US 2012/0279553) in Fig. 1(a, b) and 2(a), the shared common technical feature of:

1) a microstructure-enhanced photodetector ("the photonic crystal has a periodic structure made of the medium of the photoelectric conversion layer (first medium) and a second medium whose dielectric constant (refractive index) is different from that of the first medium, and light with a specific wavelength enters the photonic crystal and is resonated therein. The resonated light goes back and forth inside the medium of the photoelectric conversion layer and is absorbed by the medium of the photoelectric conversion layer, so that the light is converted

photoelectrically", ¶ 0033) with continuous layers of the first doped layer (21, p-type semiconductor, ¶ 0113), the second doped layer (22, n-type semiconductor, ¶ 0113) and the less doped intermediate layer (20, intrinsic semiconductor, ¶ 0113),

2) holes formed in the above mentioned layers extending transverse to the layers (30, "nanorod", ¶ 0109 discusses the regions 30 being filled with air or silicon dioxide),

3) a region of optical input (as discussed in ¶ 0033, 0037, the region of a stack of semiconductor films 20, 21 and 22 with apertures 30 are configured to convert light into electrical signal),

4) a region of electrical output (converted visible energy "converted into electrons", ¶ 00373, further discussion of circuit to output the converted electricity in ¶ 0280).

Claim 1 exclusively recites the feature(s) of:

5) "at least one of said layers, or an overlying covering layer that may be present, has holes intentionally formed therein" (this limitation sets for the limitation where neither of the "first layer", the "intermediate layer" and "the second layer" have holes formed therein, but the holes are formed in "an overlying covering layer"),

6) each of the layers comprises silicon, germanium or an alloy thereof,

7) the active electronic circuit on or in said single substrate … that amplifies and processes said electrical output.

Claim 81 exclusively recites the feature(s) of:

8) holes are only formed in one possible outcome, "at least one of the layers has holes intentionally formed therein".

So to recap, Claims 1, 45 and 81 share the common technical feature of a memory device with aspects 1) through 4). Claim 1 solely includes aspects 4) through 6). Claim 81 solely includes only the hole arrangement outcome in aspect 8). Unity of invention is present *a priori*, as aspects 1) through 4) are common to both claims. However, because aspects 1) through 4) are known in the art, there is a lack of unity of invention *a posteriori*, since aspects 1) through 4) are not Applicant's contribution over the prior art. Therefore, a lack of unity exists between the claims of Groups I and II.

This application contains claims directed to more than one species of the generic invention. These species are deemed to lack unity of invention because they are not so linked as to form a single general inventive concept under PCT Rule 13.1.

The species are as follows:

Species I, directed to a first embodiment a photodetector with only a bottom layer, an intermediate layer and a top layer, wherein holes are formed in at least one of said layers, for the purpose of converting light into an electrical output signal.

Species II, directed to a second embodiment a photodetector on or in a single substrate with a bottom layer, an intermediate layer and a top layer, wherein holes are formed in at least one of said layers or the holes are formed only in a, overlying covering layer, for the purpose of converting light into an electrical output signal, where the output signal is amplified and processed by an active electronic circuit that is on or in the said single substrate.

Applicant is required, in reply to this action, to elect a single species to which the claims shall be restricted if no generic claim is finally held to be allowable. The reply must also identify the claims readable on the elected species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered non-responsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise require all the limitations of an allowed generic claim. Currently none of the claims appear to be generic to all species.

The groups of inventions listed above do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Species I and II lack unity of invention because the groups do not share the same or corresponding technical feature.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention or species may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention or species.

Should applicant traverse on the ground that the inventions have unity of invention (37 CFR 1.475(a)), applicant must provide reasons in support thereof. Applicant may submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. Where such evidence or admission is provided by applicant, if the examiner finds one of the inventions unpatentable over the prior art,

the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an

allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571)272-8797. The examiner can normally be reached on M-F, 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571)272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eduardo A. Rodela/

Primary Examiner, Art Unit 2893

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/797,821	10/30/2017	Shih-Yuan WANG	5176/88184-CIP

CONFIRMATION NO. 1009

PUBLICATION NOTICE

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

OC000000098745648

Title:MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Publication No.US-2018-0102442-A1
Publication Date:04/12/2018

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/797,821

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	112 minus 20 =	* 92	x 40 =	3680	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			600			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	5010		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/797,821	10/30/2017		5080	5176/88184-CIP	112	3

CONFIRMATION NO. 1009
UPDATED FILING RECEIPT

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

OC000000098487814

Date Mailed: 01/04/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;
M. Saif Islam, Davis, CA;

Applicant(s)

W&WSens, Devices Inc., Los Altos, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 15/309,922 11/09/2016 PAT 9818893
which is a 371 of PCT/US2015/061120 11/17/2015
which claims benefit of 62/081,538 11/18/2014
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/199,607 07/31/2015

and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/232,716 09/25/2015
and said 15/309,922 11/09/2016
is a CON of 14/943,898 11/17/2015 PAT 9530905
which claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/232,716 09/25/2015
and said 15/309,922 11/09/2016
is a CON of 14/945,003 11/18/2015 PAT 9525084
which claims benefit of 62/081,538 11/18/2014
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/009,311 06/08/2014
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/232,716 09/25/2015
This application 15/797,821
is a CIP of PCT/US2016/067977 12/21/2016
which claims benefit of 62/415,339 10/31/2016
and claims benefit of 62/270,577 12/21/2015
This application 15/797,821

is a CIP of 14/947,718 11/20/2015
which is a CON of PCT/US2014/039208 05/22/2014
which claims benefit of 61/826,446 05/22/2013
and claims benefit of 61/834,873 06/13/2013
and claims benefit of 61/843,021 07/04/2013
and claims benefit of 61/905,109 11/15/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 11/27/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/797,821**

Projected Publication Date: 04/12/2018

Non-Publication Request: No

Early Publication Request: No

** **SMALL ENTITY** **

Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Electronic Acknowledgement Receipt

EFS ID:	31395919
Application Number:	15797821
International Application Number:	
Confirmation Number:	1009
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Vishal Parikh
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176/88184-CIP
Receipt Date:	03-JAN-2018
Filing Date:	30-OCT-2017
Time Stamp:	16:04:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$670
RAM confirmation Number	010418INTEFSW00002562033125
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	Reponse_NMP_88184_CIP.pdf	86207 7ed024f7f8935b521a45019eb8cbe85f12b26bd1	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32393 80ecdd02f229de7af36100dd2ad8168bab83c8ef	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	118600		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	15797821
Filing Date:	30-Oct-2017
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Vishal Parikh
Attorney Docket Number:	5176/88184-CIP

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
UTILITY APPL SIZE FEE PER 50 SHEETS >100	2081	3	200	600
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	2051	1	70	70
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**670**

Docket No. 5176/88184-CIP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG et al.

Serial No.: 15/797,821 Examiner: N/A

Filed: October 30, 2017 Art Unit: N/A

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Conf. No.: 1009

This correspondence is being transmitted by facsimile transmission and/or EFS-Web to the U.S. Patent and Trademark Office.

January 3, 2018

/Vishal J. Parikh/
Vishal J. Parikh Date

30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

By EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Ladies and Gentlemen:

COMMUNICATION IN RESPONSE TO NOTICE TO FILE MISSING PARTS OF A NONPROVISIONAL APPLICATION

This Communication is submitted in response to the November 28, 2017 Notice to File Missing Parts of Nonprovisional Application (hereinafter "the Notice"), issued by the U.S. Patent and Trademark Office in connection with the above-identified application. A response to the Notice is due January 28, 2017. Accordingly, this Response to the Notice is being timely filed.

The Notice states that a surcharge as set forth in 37 CFR 1.16(f) is due for late submission of the Declaration. The fee for a surcharge under 37 CFR 1.16(f) is $70.00 for a small entity. Further, the Notice states that a fee of $600.00 is required for 143 electronically equivalent pages

in excess of 100 application size. Authorization is hereby given to charge the $70.00 surcharge fee and the $600.00 excess page fee to Deposit Account No. 03-3125.

No additional fees are believed to be required in connection with this filing. Nevertheless, the Office is hereby authorized to charge any fees, or credit any overpayments, associated with this filing to Deposit Account No. 03-3125.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No.: 25,161
Attorney for Applicants
COOPER & DUNHAM LLP
30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

Electronic Acknowledgement Receipt

EFS ID:	31073554
Application Number:	15797821
International Application Number:	
Confirmation Number:	1009
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Maria Antonakis
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176/88184-CIP
Receipt Date:	29-NOV-2017
Filing Date:	30-OCT-2017
Time Stamp:	12:46:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	IDS_TransmittalLetter.pdf	285480 ab8881885dc1495414753eebcd5e0924945bb5de	no	2

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	88184-CIP_IDS_1.pdf	811263 6175e1120db617c01bb81bb9b6886b1dae553155	no	13
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Information Disclosure Statement (IDS) Form (SB08)	88184-CIP_IDS_2.pdf	565002 7288ac2ff0ea95b150273c22db990200d7106972	no	7
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Information Disclosure Statement (IDS) Form (SB08)	88184-CIP_IDS_3.pdf	407469 a203543295df1422ecdbffad2743e8c6a8090a8b	no	5
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Non Patent Literature	56-6-Fan_etal_ApplSurfScience_2013_264_761-766.pdf	1376665 5aa59eb5b6b83c83893823befd6e50adf637a662	no	6
Warnings:					
Information:					
6	Non Patent Literature	57-7-Wu_etal_JApplPhys_2010_108_051101.pdf	5687614 daf17aff9c63a9660d56767198390bb347b2f362	no	21
Warnings:					
Information:					
7	Non Patent Literature	58-8-Singh_etal_IntlJEngSciandEmTech_2011_1-16.pdf	3368230 89c045dc05421d9f5c0124e49443bd343f65660f	no	16
Warnings:					
Information:					

8	Non Patent Literature	59-9-Montalenti_etal_PhysRev_2010_014101.pdf	1797384 11746cbd3bb0f47d9d87ad735e85664bf751d729	no	7
Warnings:					
Information:					
9	Non Patent Literature	60-10-Collot_etal_JVacSciTechnol_1991.pdf	971324 b40274797bd8f71e157a5af936e51b32f626af6a	no	7
Warnings:					
Information:					
10	Non Patent Literature	61-11-Ingham_OFC_2017.pdf	557035 6e00af9b05870d5fc2865ef5028ca4b3b4147c62	no	3
Warnings:					
Information:					
11	Non Patent Literature	62-12-Sun_etal_JLightwaveTech_2017.pdf	2539513 38bfab1d7b9b47aa0f04b5bb8cad5475d55c8c5d	no	8
Warnings:					
Information:					
12	Non Patent Literature	63-13-Tekin_IEEEJSelTopicsQuantumElect_2011.pdf	4857490 deaa6f03588be0edc590b488f908ec7e312eaaeb	no	17
Warnings:					
Information:					
13	Non Patent Literature	64-14-Orcutt_OFC_2016.pdf	1004661 80b6af1aef73570006ccf074b9aec03191309166	no	3
Warnings:					
Information:					
14	Non Patent Literature	65-15-Eshaghi_etal_Optik_2014_125_1478-1481.pdf	843947 e83a6288baebc51506cbac78e4434b4ba3424e11	no	4
Warnings:					
Information:					

15	Non Patent Literature	66-16-Uddin_etal_OptExpress_2013_12497.pdf	1638258 6b0669d36587a8522600f794941c76852ac647a3	no	12
Warnings:					
Information:					
16	Non Patent Literature	67-17-Jacob_etal_JOptAmA_2001.pdf	2549905 af47669fa6184aa1727b39c52702765ec983d754	no	12
Warnings:					
Information:					
17	Non Patent Literature	68-18-Zhou_etal_OptExpress_2008_16_17282.pdf	1354239 c77aa82255bdace0095d11180e03172772823ac0	no	6
Warnings:					
Information:					
18	Non Patent Literature	69-19-Poulton_etal_IEEEspectrum_2016.pdf	1531317 64146ec7f9f31ef18efb9906f08d89bcf76c1ada	no	6
Warnings:					
Information:					
19	Non Patent Literature	70-20-Rasshoper_etal_AdvRadioSci_2011_9_49-60.pdf	2630506 ef4c449c826f4569da1578f97ebc140f5db468e5	no	12
Warnings:					
Information:					
20	Non Patent Literature	71-21-Youn_etal_IEEEJQuanElec_2012.pdf	1989469 f2f787d7f48ba9984cc6f6dd79baee0d77bfc1dc	no	8
Warnings:					
Information:					
21	Non Patent Literature	72-22-Swoboda_etal_IEEE_IntlSolStatecircConf.pdf	1115459 b263de6dbc4e8316fe1e04031ac348854ab262c1	no	8
Warnings:					
Information:					

22	Non Patent Literature	73-23-Tavernier_34thEuropeanSolStateCircConf_2008.pdf	959830 77264de1c74e2d747e01cca8af118406a79bb14a	no	4
Warnings:					
Information:					
23	Non Patent Literature	74-24-CMOSManufacturingProcess.pdf	2959996 e8cf61f26a0b6289b00a1679f75c27cd4cef5d1c	no	28
Warnings:					
Information:					
24	Non Patent Literature	75-25-Williams_MaterSciEng_1998_8-15.pdf	1547335 fee972ab6cff13767262858459a85e335361611f	no	8
Warnings:					
Information:					
25	Non Patent Literature	76-26-gibbons_etal_ProcIEEE_1968.pdf	6441996 0d2d8d1a8406a1898481cb9741ecc211cfe5438a	no	26
Warnings:					
Information:					
26	Non Patent Literature	77-27-Assefa_etal_OFC-NFOECTechDigest_2013.pdf	680373 292fb9b72d0a0135db6f26d9343cafa3a9a286c6	no	3
Warnings:					
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27	Non Patent Literature	78-28-Taubenblatt_JLightwaveTech_2012_30_448.pdf	2640770 f42caec86a1b8eebe6e15af3d7ff89083b81880b	no	11
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28	Non Patent Literature	79-29-Chen_etal_IEEEJSolidStateCirc_2005_40_1388.pdf	1817289 a1465a06578153588c47e4dd2cca6e741bae41ba	no	9
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29	Non Patent Literature	80-30-Kuchta_etal_IEEEPhotonicsConf_2012.pdf	558905 00da048d3abd00422d280aa224c9975c7c1af93d	no	2
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30	Non Patent Literature	82-32-Ghosh_etal_IEEE-NEWCAS_Conf_2005.pdf	1101883 532fab52f548fb644f61095d1e05a0cbbf727732	no	4
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31	Non Patent Literature	84-34-Knochenhauer_etal_ElectrLett_2011.pdf	423443 2c6fb124c5432e16b8cbbcc72132c18346f68210	no	2
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32	Non Patent Literature	85-35-Nishihara_etal_ElectrLett_2008.pdf	474248 e87fdc61ca3d072d12ec4e2718e1f6c42d44b703	no	2
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33	Non Patent Literature	86-36-Racanelli_etal_IEEECustIntegrCircConf_2003.pdf	365087 1ffa6b8b638c46dee3fa67965264f06d869b4988	no	4
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34	Non Patent Literature	87-37-GeneralPropertiesofSilicon_PVEducation.pdf	210032 6c0d955527e8301f4e78e33aa1ae7c554265bac2	no	2
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35	Non Patent Literature	88-38-Wegrecka_etal_Opto-ElectrRev_2004_95-104.pdf	2103063 fa0872566cc9d77be3b6227f8357deb35dd101b8	no	10
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36	Non Patent Literature	89-39-Xie_etal_JMicroelectrMechSys_2002_11_93.pdf	2099471 f03f7ef54d13b8b9ef83291b8237f05c02549fc4	no	9
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37	Non Patent Literature	90-40-Huang_etal_IEEEJSolStateCirc_2011_46_1158.pdf	2616887 b66a2ba587264b57c168c5bffddffac7c39a1f67	no	12
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38	Non Patent Literature	91-41-IEEEJSolStateCirc_2009_44_2856.pdf	3005413 bda325893b48de338a46984082e25f052bcc49ce	no	12
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39	Non Patent Literature	92-42-Kao_etal_IEEETransCircSyst_2010_2844.pdf	3701911 5c34f02aa6238b1e7d10512193e079d49aa299ca	no	14
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40	Non Patent Literature	93-43-Hartman_etal_JLightwaveTech_1985.pdf	2113184 9b60888ba5cfedc63f9dc9637ca84ff001723bfa	no	10
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41	Non Patent Literature	94-44-Radovanovic_etal_IEEEJSolStateCirc_2005_40_1706.pdf	3164690 72f657b48ff13474c41cf7a8967f5b08a104b7f5	no	12
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42	Non Patent Literature	95-45-Csutak_etal_JLightwaveTech_2002_20_1724.pdf	1112638 7e167aebb7effd9e5efd06ce876fb488f06506a9	no	6
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43	Non Patent Literature	96-46-Yin_etal_OptExpress_2004_12_2710.pdf	1185784 e86d16d8a5c3261f729a64bc253ae55e1f80ad24	no	6
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44	Non Patent Literature	97-47-Michel_etal_NaturePhotonics_2010.pdf	2028057 a9a69548ff4eaee1919d887008848adda8c3f611	no	8
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45	Non Patent Literature	98-48-AnalogDevicesIncDataSheet.pdf	916032 cab606f6e97620b6501f3a4e6e3d4117bfa79a00	no	11
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46	Non Patent Literature	99-49-Yashiki_etal_OFC_2015.pdf	745394 73861607c8aec72d97f4ed34674c311d486ff66a	no	3
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47	Non Patent Literature	100-50-Pyo_etal_AdvOptMater_2016_4_1190-1195.pdf	1401162 f4a5ed99806ee085e1d61345d9f0ca5f33c3397b	no	6
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48	Non Patent Literature	101-1-Berenschot_etal_JMicromechMicroeng_2013.pdf	2226289 ea55fed22d9b60cffb16ad09f75153a95b047e57	no	11
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49	Non Patent Literature	102-2-Sato_Basic2AnisotropicWet-etching_of_Silicon.pdf	7004927 3c58d13c9002bf51dbc632f8a5f8e8572280d6e6	no	53
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50	Non Patent Literature	103-3-Sato_etal_SensorsActuators_1999.pdf	1612081 9a5bb9fcdceb0cb098e0fe9e1659baecb0f7b6ce	no	7
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51	Non Patent Literature	104-4-Bassous_IEEETransElecDev_10_1978.pdf	3949362 c784c302d67417792fd2fa62fc97c10da0fa45da	no	8
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52	Non Patent Literature	105-5-Zubel_PrcSPIEVol_10175.pdf	1849291 2f2e919fbb884276778c3d1734a5122f7cfb00b8	no	10
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53	Non Patent Literature	106-6-HSIAO_etal_OPTICSEXPRESS_2009_17_24250.pdf	2253329 58e33464dfaf87220e716920adfaa823a0dec544	no	11
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54	Non Patent Literature	107-7-Rola_MicrosystTech_2017_1463-1473.pdf	3020836 576f830427f49943010dc43e82dcbced4e703f19	no	11
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55	Non Patent Literature	108-8-Rola_etal_JMicroelectromechSyst_2013_1373.pdf	3137503 4ff317509e2bd6402968fe21b6149512ff673e06	no	10
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58	Non Patent Literature	111-11-Judy_SmartMaterStruct_2001_1115-1134.pdf	5096084 f5bfc927edbd6f190b80578f28194bc9945e5c5e	no	21
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59	Non Patent Literature	112-12-Smith_etal_Proc_1995_609-612.pdf	885200 c857c50a25ab9e3ed5d5388c2f2dce345ab2d74c	no	4
Warnings:					
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60	Non Patent Literature	113-13-Gao_etal_.pdf	2553985 760c055a366fde9afe927bb62161f640597be0f9	no	8
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Examiner Name	
Attorney Docket Number	5176/88184-CIP

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	1	BERENSCHOT et al. "Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon" J. Micromech. Microeng. 2013, 23,055024 (10pp).	☐
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Application of: Shih-Yuan WANG et al.

Application No.: 15/797,821 Confirmation No.: 1009

Filed: October 30, 2017

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

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INFORMATION DISCLOSURE STATEMENT

Applicants hereby provide the Examiner with updated information regarding applications/patents with related subject matter:

1. Ser. No. 14/892,821 filed November 20, 2015, now patent 9,496,435;
2. Ser. No. 14/943,898 filed November 17, 2015, now patent 9,530,905;
3. Ser. No. 14/945,003 filed November 18, 2015, now patent 9,525,084;
4. Ser. No. 14/947,718 filed November 20, 2015;
5. Ser. No. 15/309,922 filed November 9, 2016, now patent 9,818,893;
6. Ser. No. 15/797,821 filed October 30, 2017;
7. Ser. No. 13/821,963 filed October 22, 2013, now patent 9,559,231 B2;

8. PCT/US14/39208 filed May 22, 2014;

9. PCT/US15/061120 filed November 17, 2015;

10. PCT/US16/67977 filed December 21, 2016; and

11. PCT/US11/51091 filed September 9, 2011.

Applicants direct the Examiner's attention to the claims of the above-identified patents and applications for consideration regarding any double-patenting issues, and request the Examiner to consider the references cited in the prosecution of said patents/applications.

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Respectfully submitted,

By: /ivan kavrukov /

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Attorney for Applicant
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Application Number:	15797821
International Application Number:	
Confirmation Number:	1009
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/MARIA ANTONAKIS
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	5	WO2016081476	WO		2016-05-26	Wang, S.		☐
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15797821
	Filing Date	2017-10-30
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	
	Attorney Docket Number	5176/88184-CIP

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/797,821

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	112 minus 20 =	* 92	x 40 =	3680	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			600			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	5010		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/797,821	10/30/2017	Shih-Yuan WANG	5176/88184-CIP

CONFIRMATION NO. 1009

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

FORMALITIES LETTER

OC000000095709281

Date Mailed: 11/28/2017

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **600** for **143** electronically equivalent pages in excess of **100** application size fee.
- $ **70** surcharge.
- $(**0**) previous unapplied payment amount.
- $ **670** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

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Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tnguyen/

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/797,821	10/30/2017		4410	5176/88184-CIP	112	3

CONFIRMATION NO. 1009

FILING RECEIPT

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

OC000000093709280

Date Mailed: 11/28/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;
M. Saif Islam, Davis, CA;

Applicant(s)

W&WSens, Devices Inc., Los Altos, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 15/309,922 11/09/2016 PAT 9818893
which is a 371 of PCT/US2015/061120 11/17/2015
which claims benefit of 62/081,538 11/18/2014
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/139,511 03/27/2015
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and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/199,607 07/31/2015

and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/232,716 09/25/2015
and said 15/309,922 11/09/2016
is a CON of 14/943,898 11/17/2015 PAT 9530905
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and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/232,716 09/25/2015
This application 15/797,821
is a CIP of PCT/US2016/067977 12/21/2016
which claims benefit of 62/415,339 10/31/2016
and claims benefit of 62/270,577 12/21/2015
This application 15/797,821

is a CIP of 14/947,718 11/20/2015
which is a CON of PCT/US2014/039208 05/22/2014
which claims benefit of 61/826,446 05/22/2013
and claims benefit of 61/834,873 06/13/2013
and claims benefit of 61/843,021 07/04/2013
and claims benefit of 61/905,109 11/15/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/797,821**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

** **SMALL ENTITY** **

Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed

from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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Electronic Patent Application Fee Transmittal

Application Number:	15797821
Filing Date:	
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Vishal Parikh
Attorney Docket Number:	5176/88184-CIP

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
PROCESSING FEE, EXCEPT PROV. APPLS.	2830	1	70	70
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**70**

Docket No. 5176/88184-CIP

IN THE UNITED STATES RECEIVING OFFICE

Application of: Shih-Yuan WANG et al.

Serial No.: 15/797,821 Examiner: N/A

Filed: October 30, 2017 Art Unit: N/A

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Conf. No.: 1009

This correspondence is being transmitted by facsimile transmission and/or EFS-Web to the U.S. Patent and Trademark Office.

November 14, 2017

/Vishal J. Parikh/
Vishal J. Parikh Date

30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

By EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Ladies and Gentlemen:

CORRECTION OF INVENTORSHIP

This paper is submitted pursuant to 37 C.F.R. §1.48 to correct the inventorship of the above-identified non-provisional application. In accordance with 37 C.F.R. §1.48(a), a revised application data sheet and the processing fee set forth in 37 C.F.R. §1.17(i) is submitted herewith.

REMARKS

This Correction of Inventorship is submitted pursuant to 37 C.F.R. §1.48(a) to correct the inventorship of the above-identified non-provisional application. The inventor M. Saif ISLAM was inadvertently omitted as an inventor in the above-identified application. In accordance with 37 C.F.R. §1.48(a), a revised application data sheet and the processing fee set forth in 37 C.F.R. §1.17(i) is submitted herewith. The revised application data sheet merely adds information for inventor M. Saif ISLAM. The Office is respectfully requested to correct the inventorship of the above-identified application as presented in the new application data sheet. Further, Applicants hereby submit the declaration for all inventors.

The fee set forth in 37 C.F.R. 1.17(i)(1) is $70 for a small entity. The Office is hereby authorized to charge this amount to our Deposit Account No. 03-3125. No additional fees are believed to be required in connection with this Response. Nevertheless, the Office is hereby authorized to charge any fees, or credit any overpayments, associated with this filing to Deposit Account No. 03-3125.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No.: 25,161
Attorney for Applicants
COOPER & DUNHAM LLP
30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 15/797821

filed on October 30, 2017.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: M. Saif Islam Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	30945754
Application Number:	15797821
International Application Number:	
Confirmation Number:	1009
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Vishal Parikh
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176/88184-CIP
Receipt Date:	14-NOV-2017
Filing Date:	
Time Stamp:	14:54:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$70
RAM confirmation Number	111517INTEFSW00001432033125
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request under Rule 48 correcting inventorship	Correction_Inventorship_88184_CIP_uspto.pdf	71973 90f636eb4e6ee4e0198a3fae515009d680af5523	no	2
Warnings:					
Information:					
2	Application Data Sheet	88184_CIP_ADS_CORRECTED_FINAL.pdf	568263 196d988a564c0c6481b3c63f29bc67b9af7b27ce	no	16
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
3	Oath or Declaration filed	Islam_M_Saif_Declaration_88184_CIP_signed_uspto.pdf	1465529 5197e099a1dca83cf56e5e4745618cd2222faffb	no	2
Warnings:					
Information:					
4	Oath or Declaration filed	Yuan_Ping_Decs.pdf	552821 fa6071bd49c1e64748b6d653e67cac93dcfe03c8	no	4
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30573 f1976fd06f98912277d84d19ea0240c09085c6d0	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2689159		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Yuan		WANG	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Palo Alto	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	766 Encina Grande Dr.		
Address 2			
City	Palo Alto	State/Province	
Postal Code	94306	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Ping		WANG	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Los Altos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	38 3rd Street, Suite #307		
Address 2			
City	Los Altos	State/Province	
Postal Code	94022	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	M. Saif		ISLAM	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

City	Davis	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	3038 Mallorca Ln.		
Address 2			
City	Davis	State/Province	CA
Postal Code	95618	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23432		
Email Address	pdockeling@cooperdunham.com	Add Email	Remove Email

Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
Attorney Docket Number	5176/88184-CIP	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	131	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23432		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Continuation in part of	15309922	2016-11-09
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15309922	a 371 of international	PCT/US2015/061120	2015-11-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62081538	2014-11-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62090879	2014-12-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62100025	2015-01-05

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62111582	2015-02-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62153443	2015-04-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62154675	2015-04-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62174498	2015-06-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62175855	2015-06-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62182602	2015-06-21

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62188876	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62199607	2015-07-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62205717	2015-08-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62213556	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62232716	2015-09-25
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15309922	Continuation of	14943898	2015-11-17	9530905	2016-12-27

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	620181538	2014-11-18

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62090879	2014-12-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62100025	2015-01-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62111582	2015-02-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62153443	2015-04-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62154675	2015-04-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62174498	2015-06-11

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62175855	2015-06-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62182602	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62188876	2015-07-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62199607	2015-07-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62205717	2015-08-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62213556	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62232716	2015-09-25

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15309922	Continuation of	14945003	2015-11-17	9525084	2016-12-20

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62081538	2014-11-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62090879	2014-12-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62100025	2015-01-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62111582	2015-02-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62153443	2015-04-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62154675	2015-04-29

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62174498	2015-06-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62175855	2015-06-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62182602	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62188876	2015-07-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62199607	2015-07-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62205717	2015-08-15

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62213556	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62232716	2015-09-25
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Continuation in part of	PCT/US2016/67977	2016-12-21
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2016/67977	Claims benefit of provisional	62415339	2016-10-31
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2016/67977	Claims benefit of provisional	62270577	2016-12-21
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Continuation in part of	14947718	2015-11-20
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14947718	Continuation of	PCT/US2014/039208	2014-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2014/039208	Claims benefit of provisional	61826446	2013-05-05

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2014/039208	Claims benefit of provisional	61834873	2013-06-13
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2014/039208	Claims benefit of provisional	61843021	2013-07-04
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2014/039208	Claims benefit of provisional	61905109	2013-11-15

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	

If the Applicant is an Organization check here. ☒

Organization Name	W&WSens, Devices Inc.

Mailing Address Information For Applicant:

Address 1	W&WSens, Devices Inc.		
Address 2	4546 El Camino Real, Suite 215		
City	Los Altos	**State/Province**	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Ivan S. Kavrukov/			Date (YYYY-MM-DD)	2017-11-14 ~~2017-10-30~~
First Name	Ivan	Last Name	Kavrukov	Registration Number	25,161

Additional Signature may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	15/797821
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 15/797821 filed on October 30, 2017

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Shih-Ping WANG Date (Optional) :

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 15/797821 filed on October 30, 2017

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: Shih-Yuan WANG Date (Optional) :

Signature: Shih-Yuan Wang

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	30802988
Application Number:	15797821
International Application Number:	
Confirmation Number:	1009
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Vishal Parikh
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176/88184-CIP
Receipt Date:	30-OCT-2017
Filing Date:	
Time Stamp:	17:01:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$4410
RAM confirmation Number	103117INTEFSW00004649033125
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	88184_CIP_ADS.pdf	1825179 377d05c004249c4cd9e4e0c67ce773a457fc76f9	no	16
Warnings:					
Information:					
2	Transmittal of New Application	aia0015_Transmittal_88184.pdf	276859 807a8583dcd8509c3d81b8271d43a19512cec760	no	2
Warnings:					
Information:					
3	Drawings-only black and white line drawings	Drawings_USPTO.pdf	3229240 d63edd07404480bb2fdce55eadd5964e9800998c	no	131
Warnings:					
Information:					
4		Application_USPTO.pdf	856617 46d75d5d7206bd3c6d5f69b3f567473e05524e61	yes	195

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	178
Claims	179	194
Abstract	195	195

Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	36953 a10ba1d93ce70a39f58e5bac96741bf2cf1a1f50	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	6224848

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Yuan		WANG	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Palo Alto	CA	US

Mailing Address of Inventor:

Address 1	766 Encina Grande Dr.
Address 2	
City	Palo Alto
State/Province	
Postal Code	94306
Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Ping		WANG	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Los Altos	CA	US

Mailing Address of Inventor:

Address 1	38 3rd Street, Suite #307
Address 2	
City	Los Altos
State/Province	
Postal Code	94022
Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23432		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
Attorney Docket Number	5176/88184-CIP	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	131	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23432		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation in part of	15309922	2016-11-09
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15309922	a 371 of international	PCT/US2015/061120	2015-11-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62081538	2014-11-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62090879	2014-12-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62100025	2015-01-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62111582	2015-02-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62153443	2015-04-27

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62154675	2015-04-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62174498	2015-06-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62175855	2015-06-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62182602	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62188876	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62199607	2015-07-31

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62205717	2015-08-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62213556	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2015/061120	Claims benefit of provisional	62232716	2015-09-25
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15309922	Continuation of	14943898	2015-11-17	9530905	2016-12-27

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	620181538	2014-11-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62090879	2014-12-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62100025	2015-01-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62111582	2015-02-03

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62153443	2015-04-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62154675	2015-04-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62174498	2015-06-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62175855	2015-06-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62182602	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62188876	2015-07-06

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62199607	2015-07-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62205717	2015-08-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62213556	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14943898	Claims benefit of provisional	62232716	2015-09-25
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15309922	Continuation of	14945003	2015-11-17	9525084	2016-12-20

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62081538	2014-11-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62090879	2014-12-11

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62100025	2015-01-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62111582	2015-02-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62153443	2015-04-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62154675	2015-04-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62174498	2015-06-11

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62175855	2015-06-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62182602	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62188876	2015-07-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62199607	2015-07-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62205717	2015-08-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62213556	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14945003	Claims benefit of provisional	62232716	2015-09-25

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation in part of	PCT/US2016/67977	2016-12-21
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2016/67977	Claims benefit of provisional	62415339	2016-10-31
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2016/67977	Claims benefit of provisional	62270577	2016-12-21
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation in part of	14947718	2015-11-20
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14947718	Continuation of	PCT/US2014/039208	2014-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2014/039208	Claims benefit of provisional	61826446	2013-05-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2014/039208	Claims benefit of provisional	61834873	2013-06-13
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2014/039208	Claims benefit of provisional	61843021	2013-07-04
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US2014/039208	Claims benefit of provisional	61905109	2013-11-15

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	W&WSens, Devices Inc.		
Mailing Address Information For Applicant:			
Address 1	W&WSens, Devices Inc.		
Address 2	4546 El Camino Real, Suite 215		
City	Los Altos	**State/Province**	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Ivan S. Kavrukov/			Date (YYYY-MM-DD)	2017-10-30
First Name	Ivan	Last Name	Kavrukov	Registration Number	25,161

Additional Signature may be generated within this form by selecting the Add button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5176/88184-CIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	5176/88184-CIP
First Named Inventor	Shih-Yuan WANG et al.
Title	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. ☑ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification** [*Total Pages* 195] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. ☑ **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 131]
6. **Inventor's Oath or Declaration** [*Total Pages* ____] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☐ Newly executed (original or copy)
   b. ☐ A copy from a prior application (37 CFR 1.63(d))
7. ☑ **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   ☐ Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

ACCOMPANYING APPLICATION PAPERS

10. ☐ **Assignment Papers** (cover sheet & document(s))
    Name of Assignee _____
11. ☐ **37 CFR 3.73(c) Statement** (*when there is an assignee*) ☐ **Power of Attorney**
12. ☐ **English Translation Document** (*if applicable*)
13. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
14. ☐ **Preliminary Amendment**
15. ☐ **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. ☐ **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. ☐ **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. ☐ **Other:** _____

*Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 23432 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Ivan S. Kavrukov/	Date	October 30, 2017
Name (Print/Type)	Ivan S. Kavrukov	Registration No. (Attorney/Agent)	25,161

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

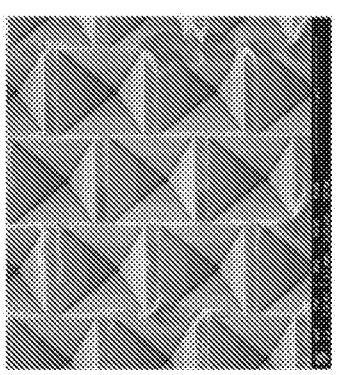


FIG. 1G

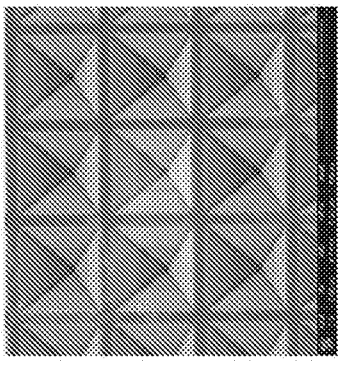


FIG. 1H

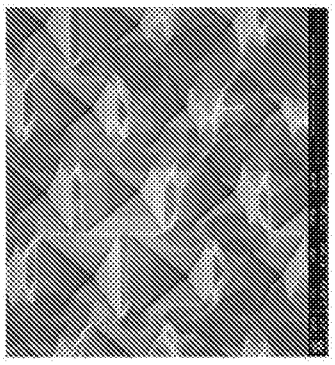


FIG. 1E

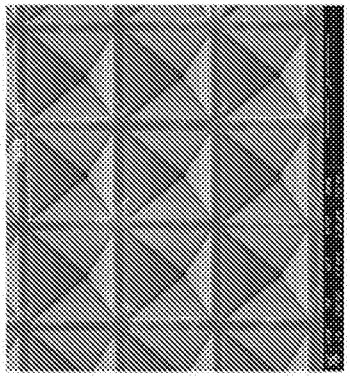


FIG. 1F

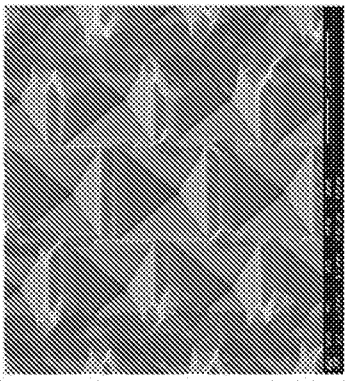


FIG. 1C

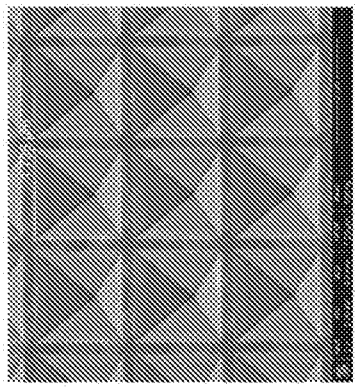


FIG. 1D

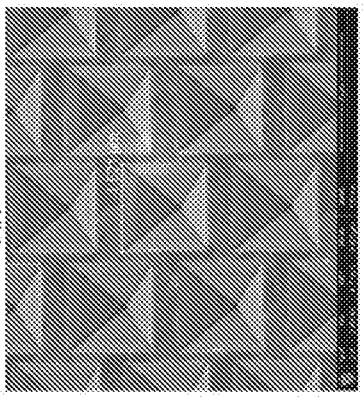


FIG. 1A

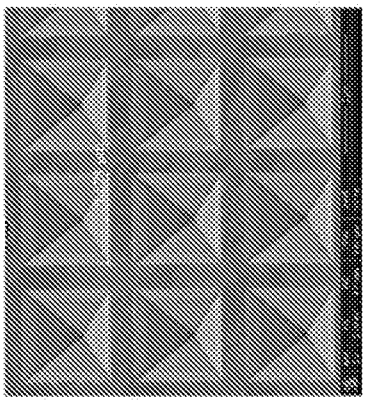


FIG. 1B

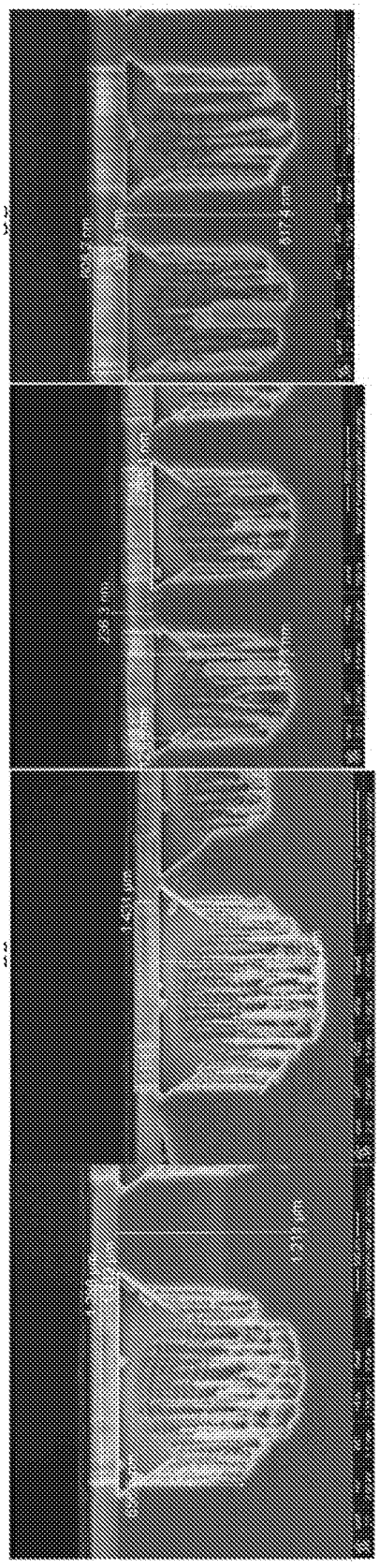


FIG. 2A FIG. 2B FIG. 2C FIG. 2D

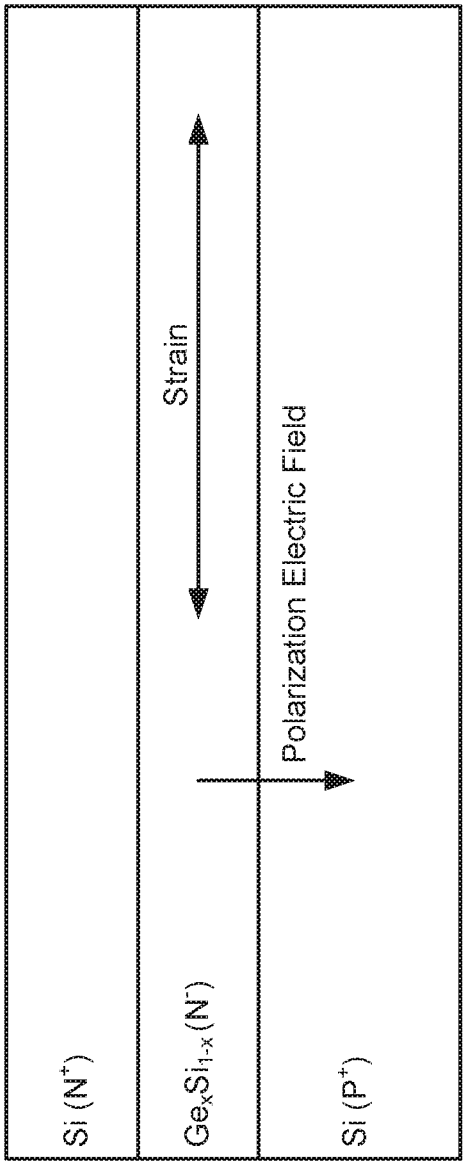


FIG. 3

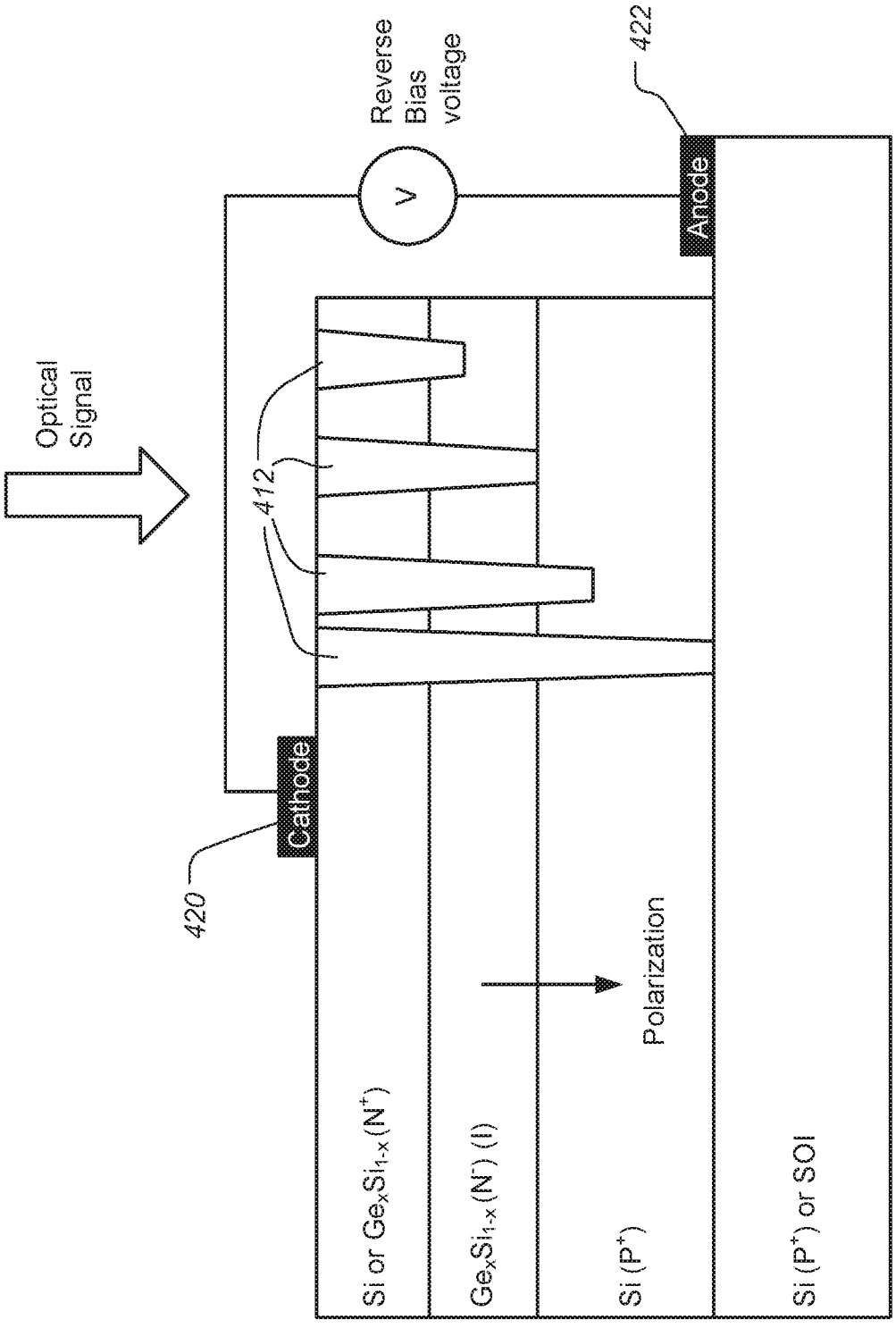

Reverse
Bias
voltage
V
422
Anode
Optical
Signal
412
Cathode
420
Si or Ge_xSi_{1-x} (N^+)
Ge_xSi_{1-x} (N^-) (I)
Si (P^+)
Si (P^+) or SOI
Polarization

FIG. 4

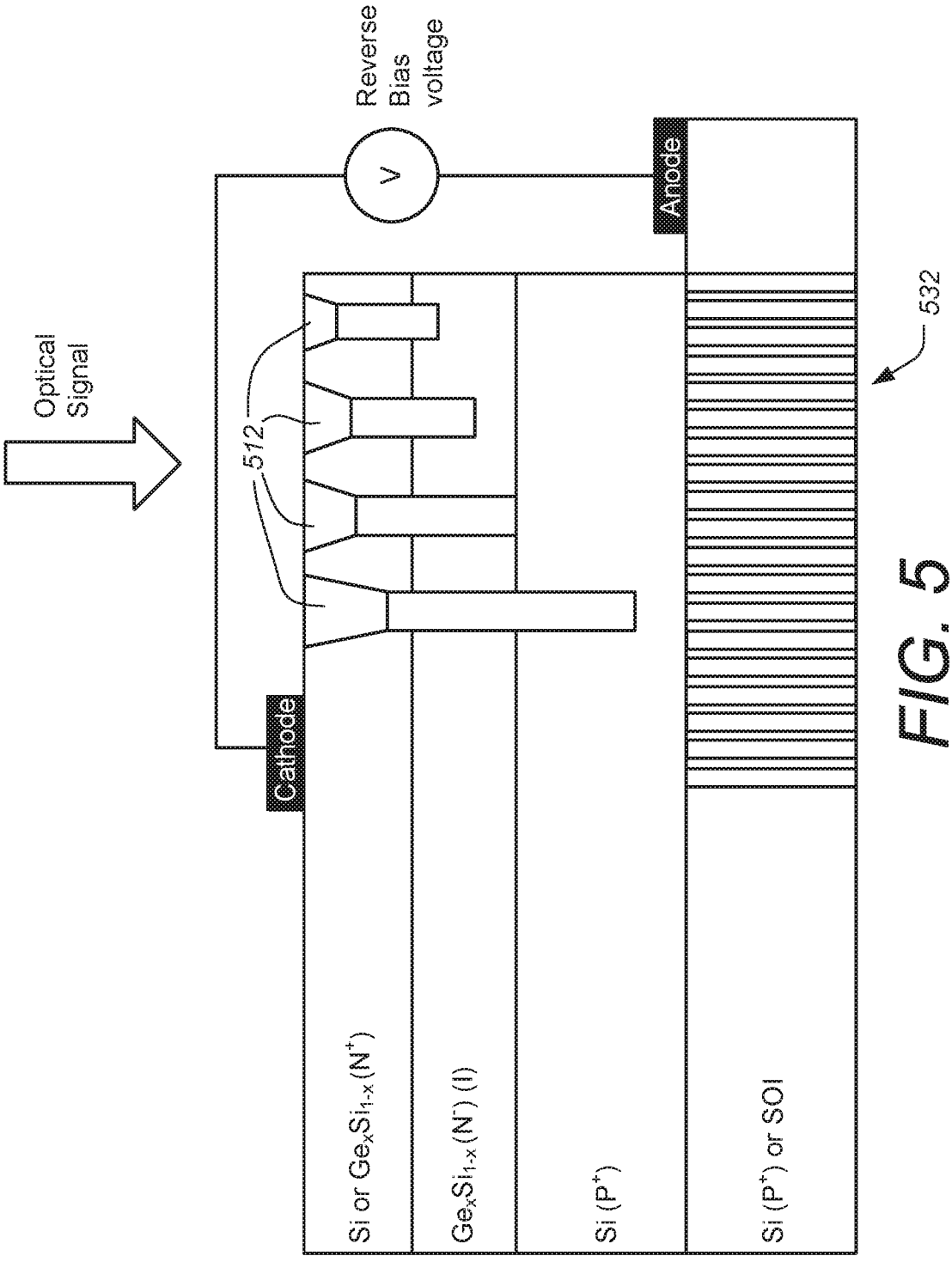

Reverse
Bias
voltage
V
Anode
Optical
Signal
512
532
Cathode
Si or $Ge_xSi_{1-x}(N^+)$
$Ge_xSi_{1-x}(N^-)$ (I)
Si (P^+)
Si (P^+) or SOI

FIG. 5



FIG. 6A

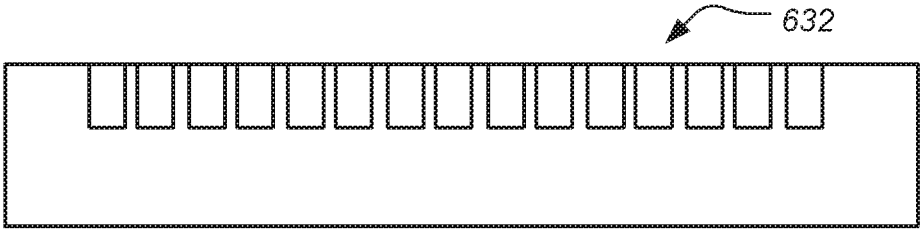


FIG. 6B

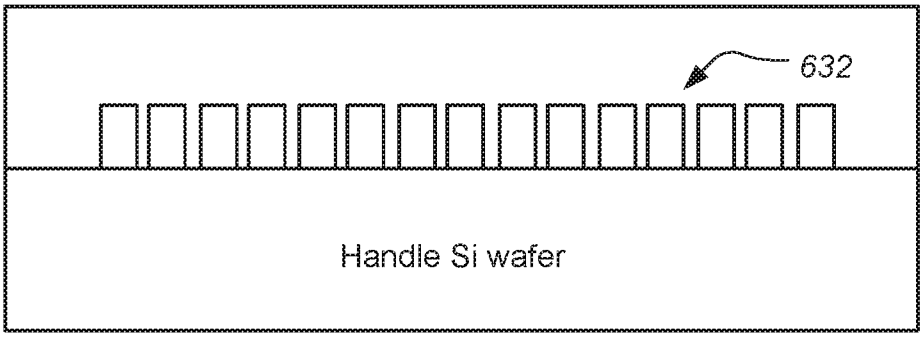


FIG. 6C

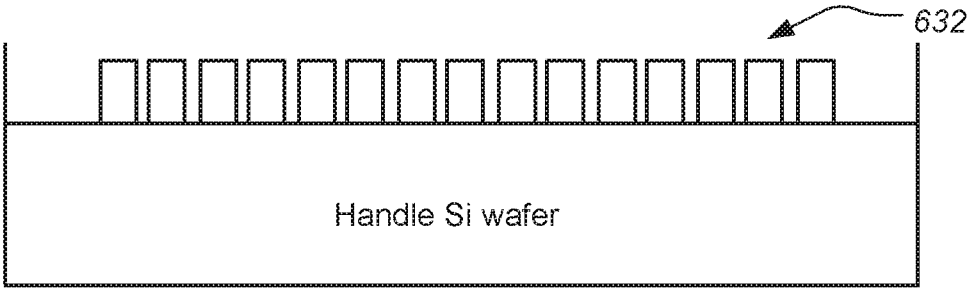


FIG. 6D

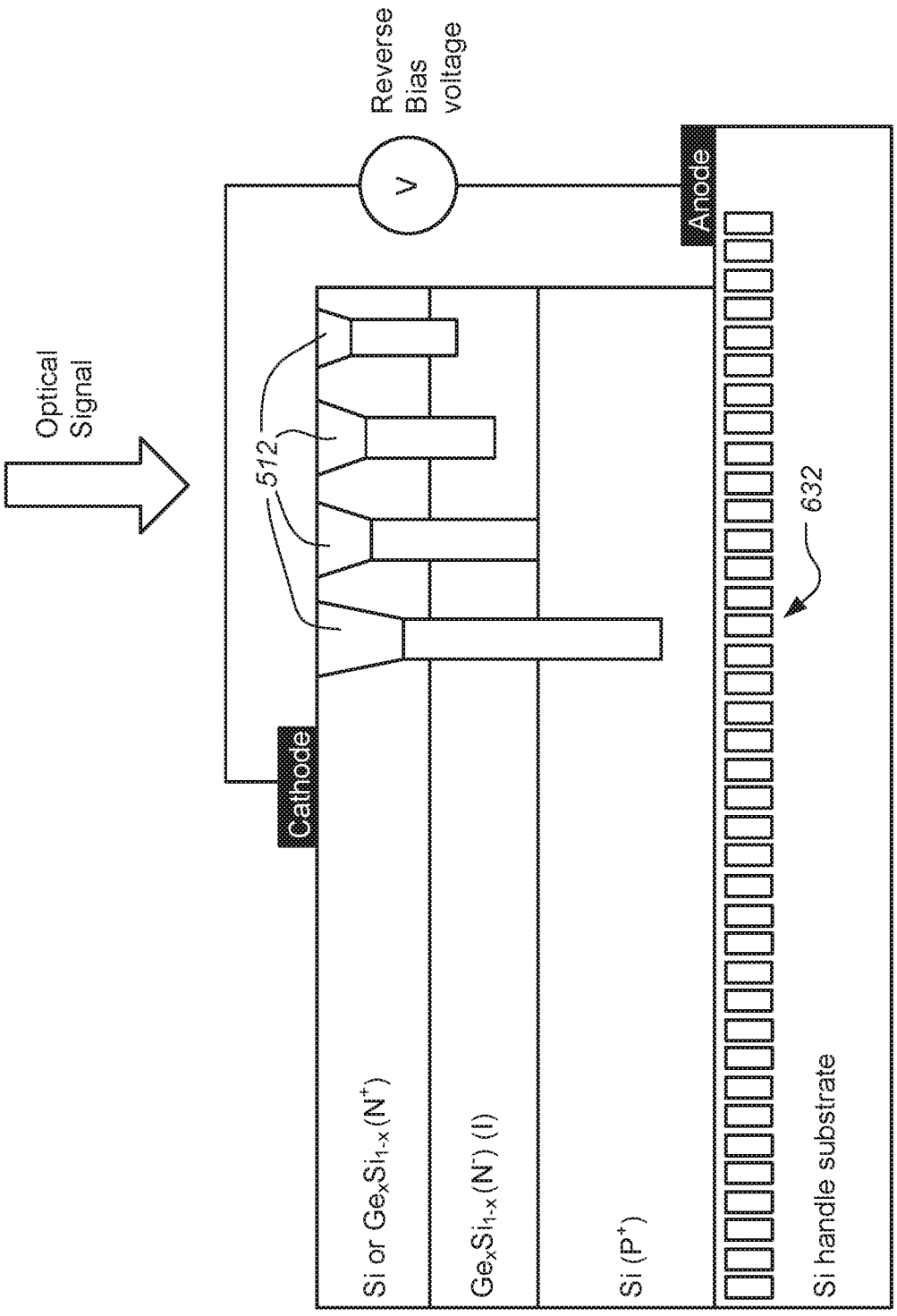

Reverse
Bias
voltage
V
Anode
Optical
Signal
512
632
Cathode
Si or $Ge_xSi_{1-x}(N^+)$
$Ge_xSi_{1-x}(N^-)$ (I)
Si (P^+)
Si handle substrate

FIG. 6E

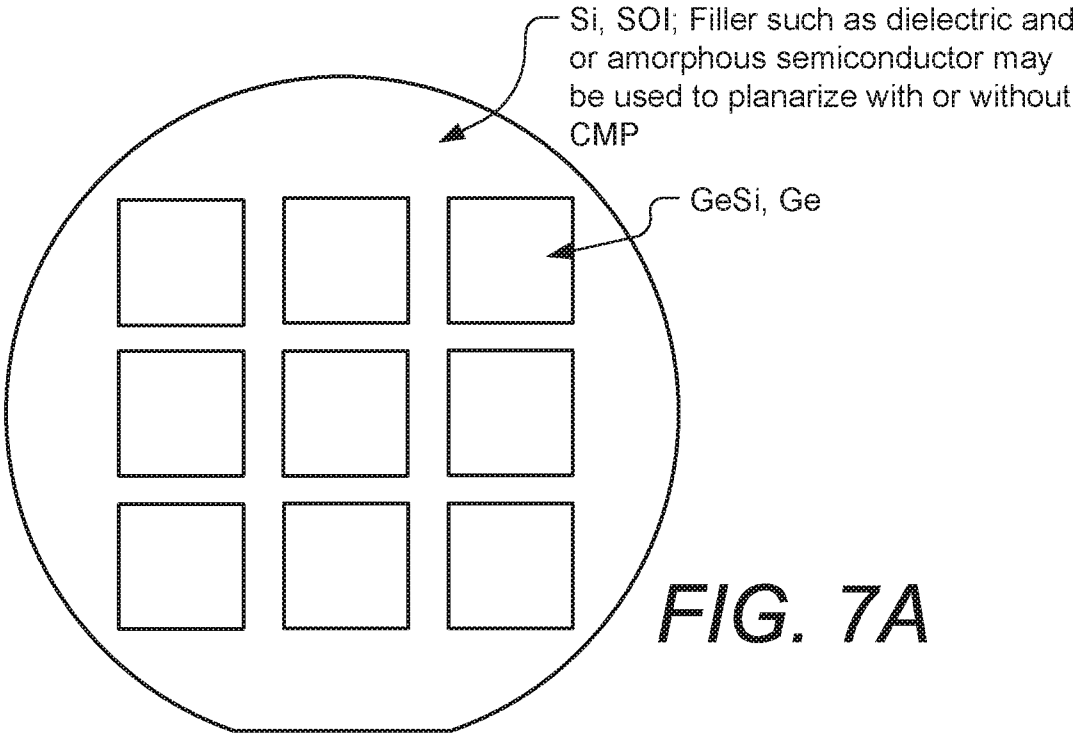

Si, SOI; Filler such as dielectric and or amorphous semiconductor may be used to planarize with or without CMP
GeSi, Ge

FIG. 7A

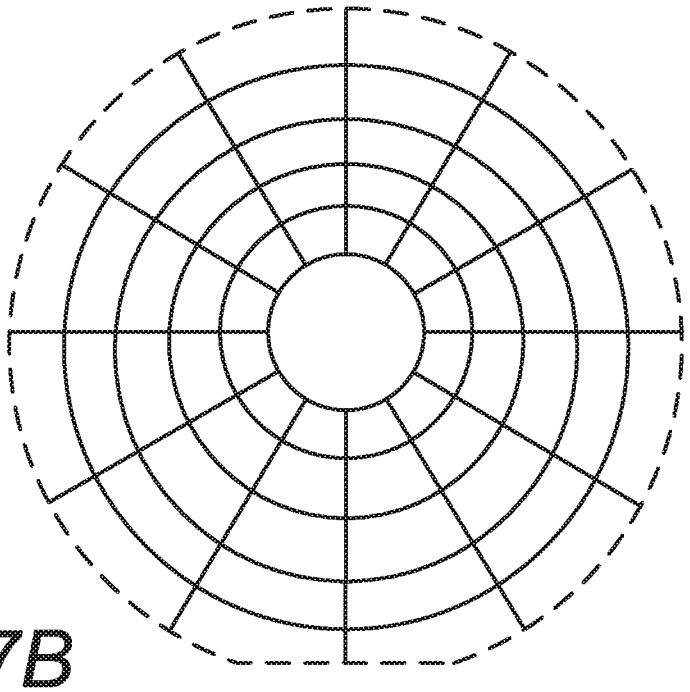


FIG. 7B

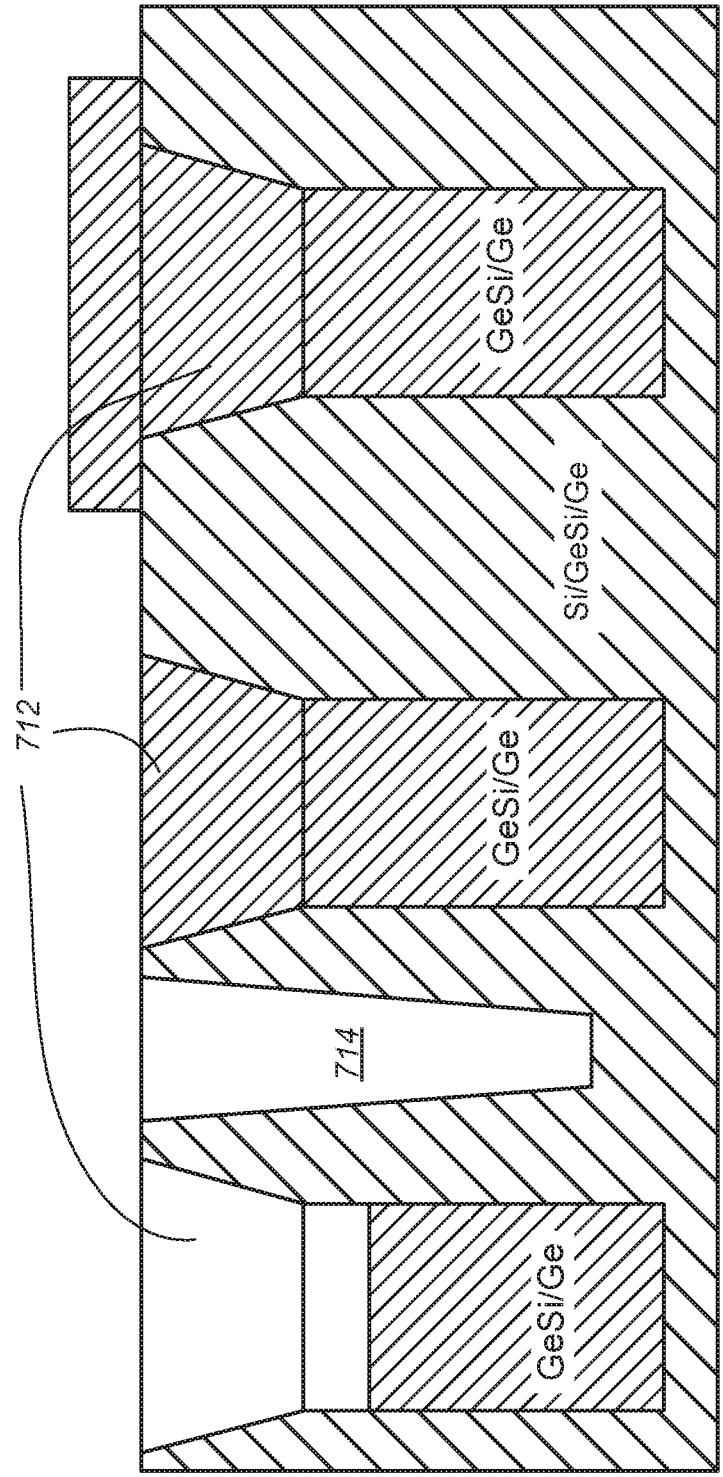


FIG. 7C

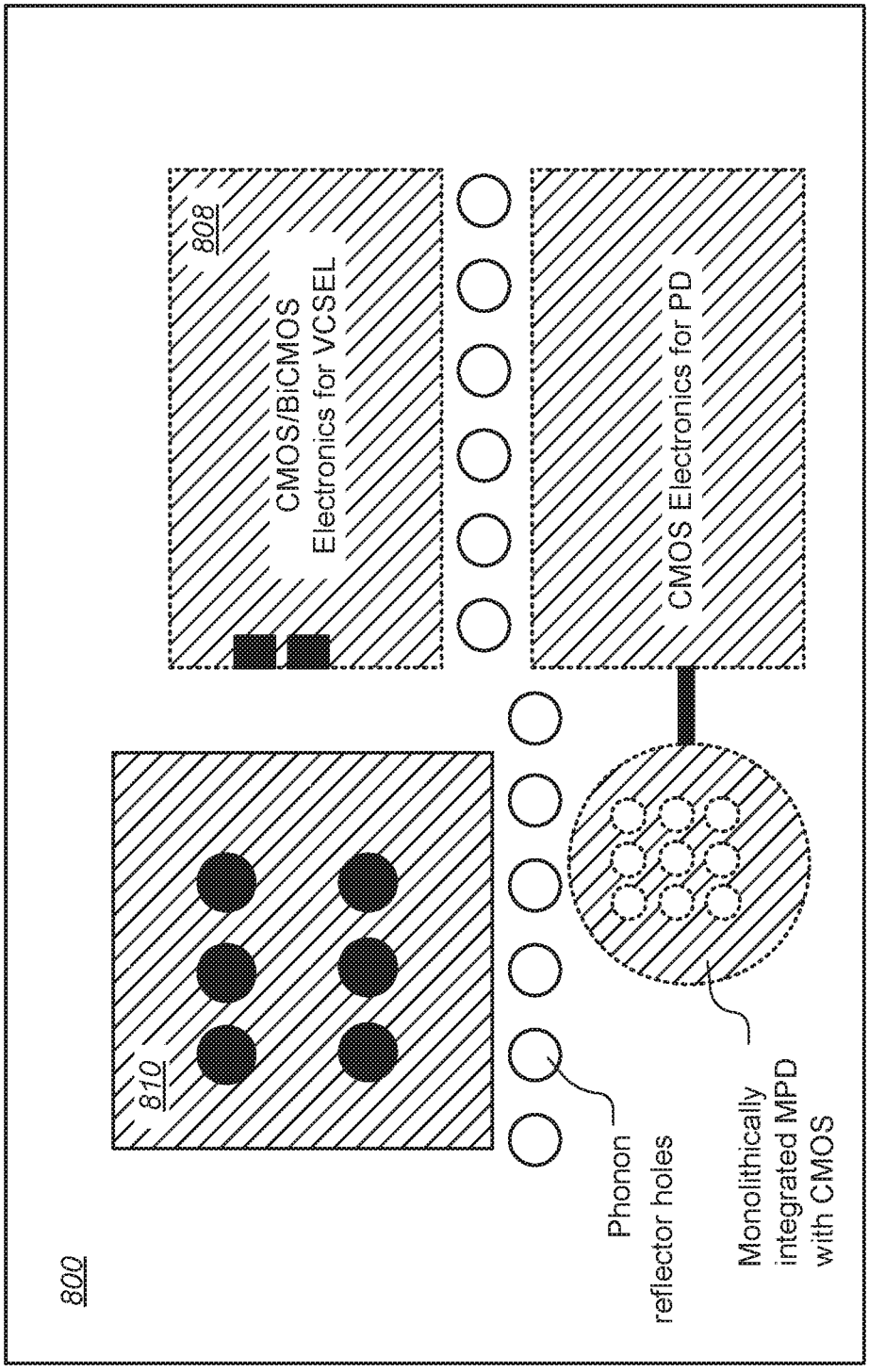

800
808
CMOS/BiCMOS
Electronics for VCSEL
CMOS Electronics for PD
810
Phonon
reflector holes
Monolithically
integrated MPD
with CMOS

FIG. 8

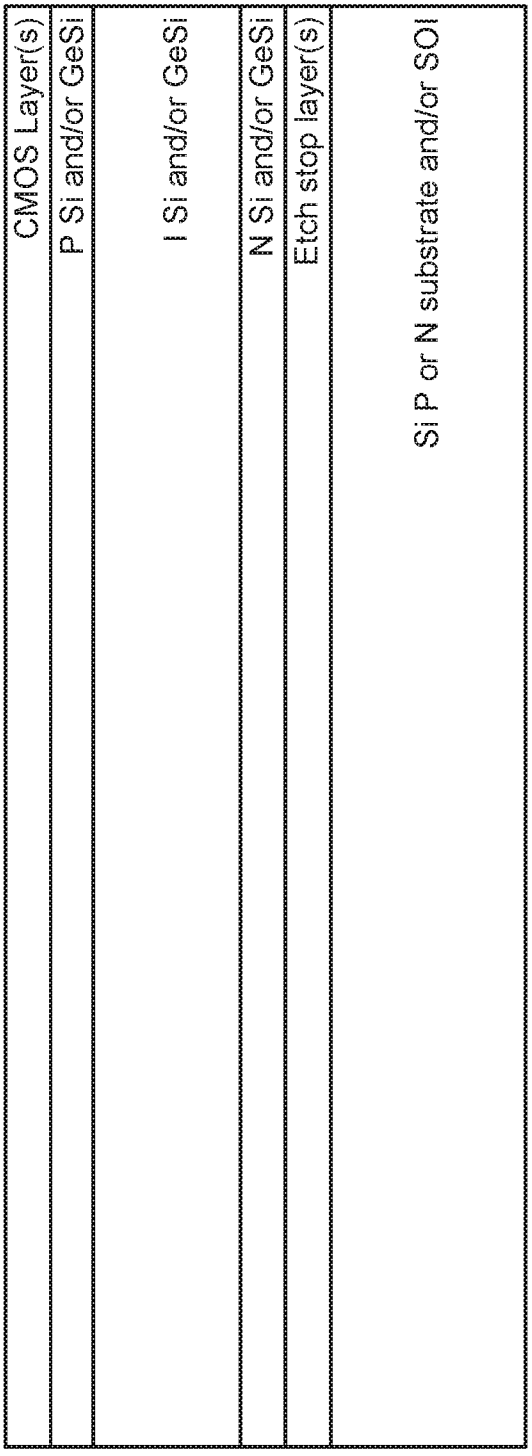

CMOS Layer(s)
P Si and/or GeSi
I Si and/or GeSi
N Si and/or GeSi
Etch stop layer(s)
Si P or N substrate and/or SOI

FIG. 9A

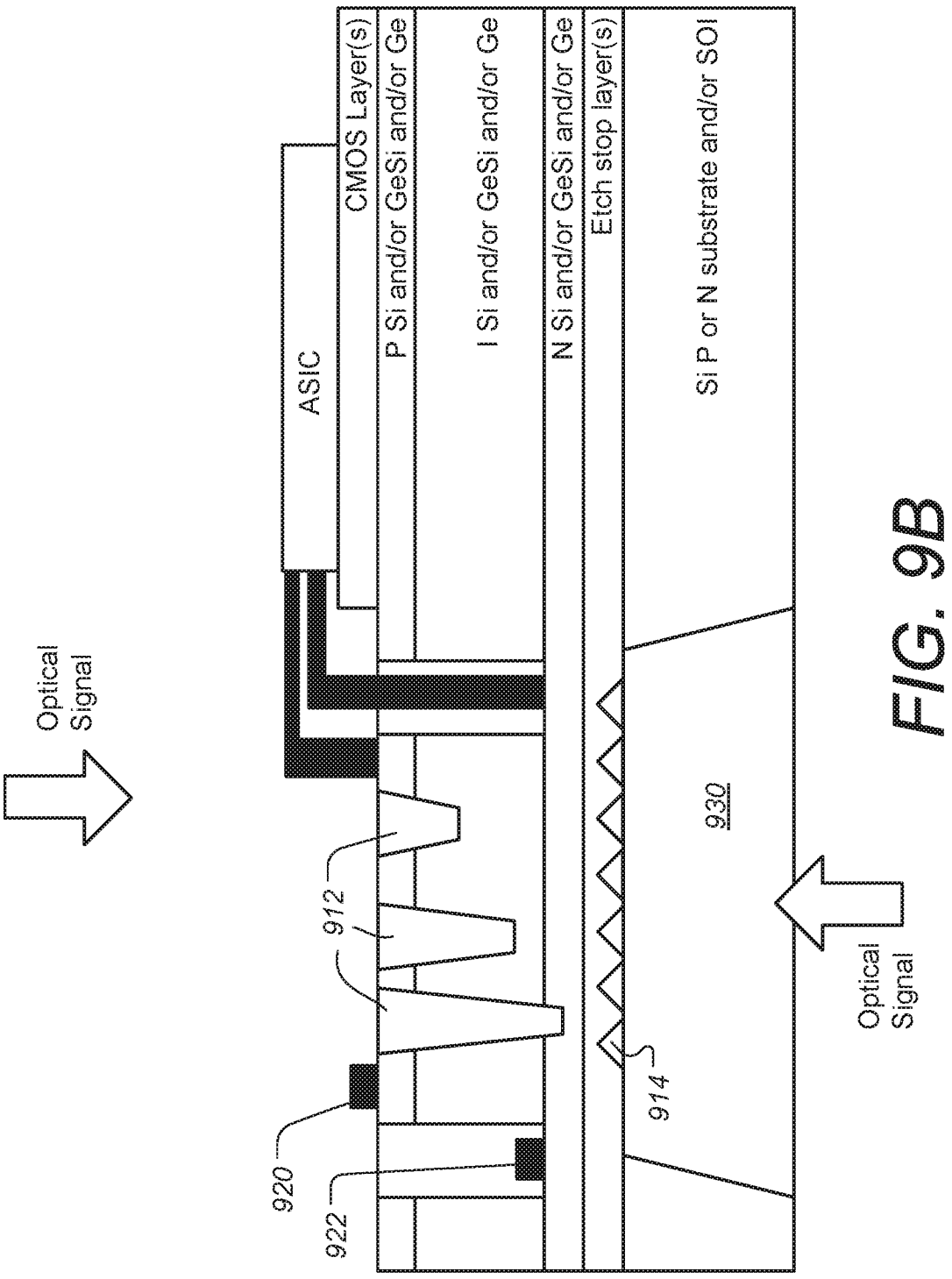

Optical Signal
ASIC
CMOS Layer(s)
P Si and/or GeSi and/or Ge
I Si and/or GeSi and/or Ge
N Si and/or GeSi and/or Ge
Etch stop layer(s)
Si P or N substrate and/or SOI
912
920
922
914
930
Optical Signal

FIG. 9B

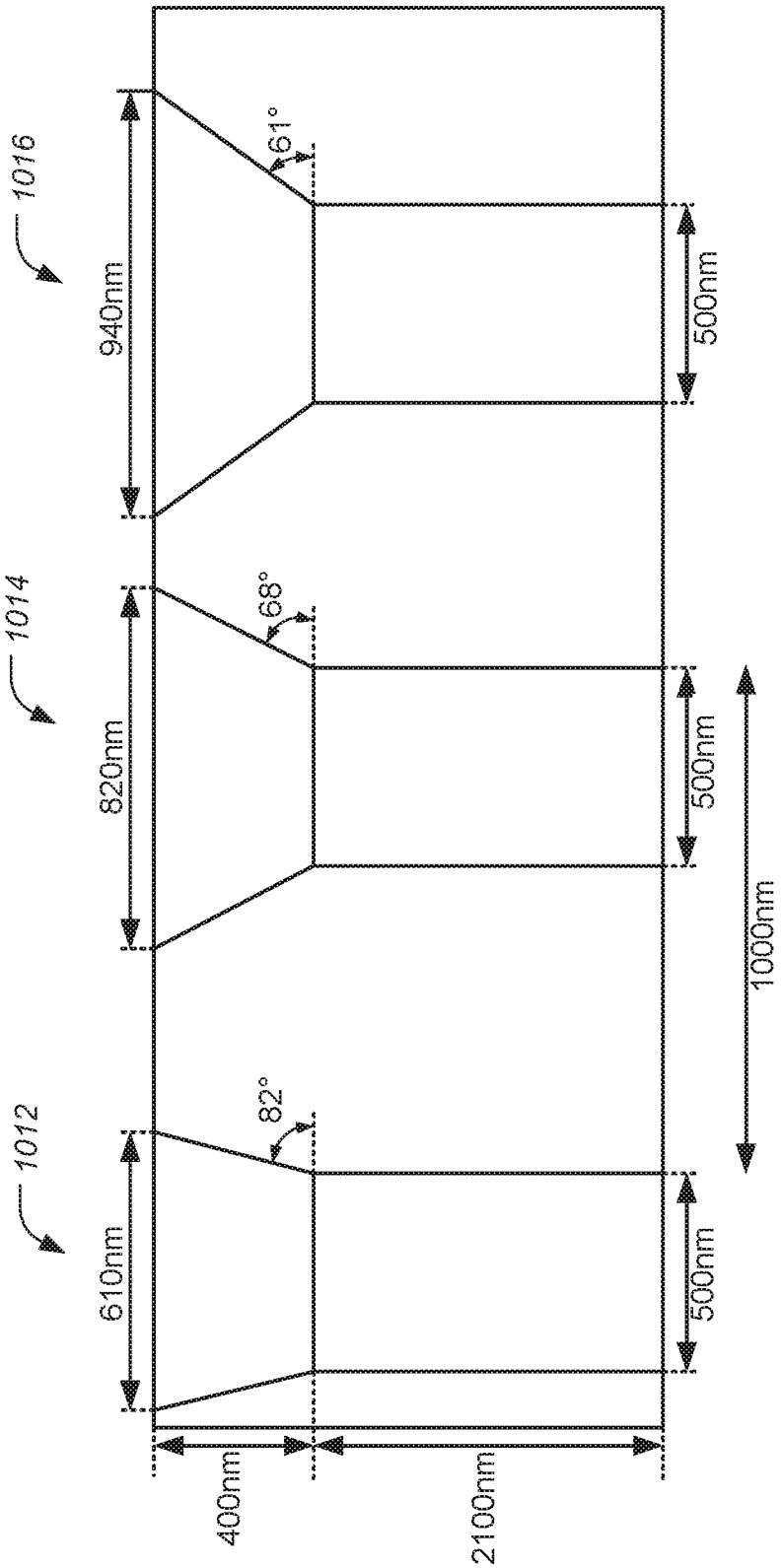

1016
940nm
61°
500nm
1014
820nm
68°
500nm
1000nm
1012
610nm
82°
500nm
400nm
2100nm

FIG. 10

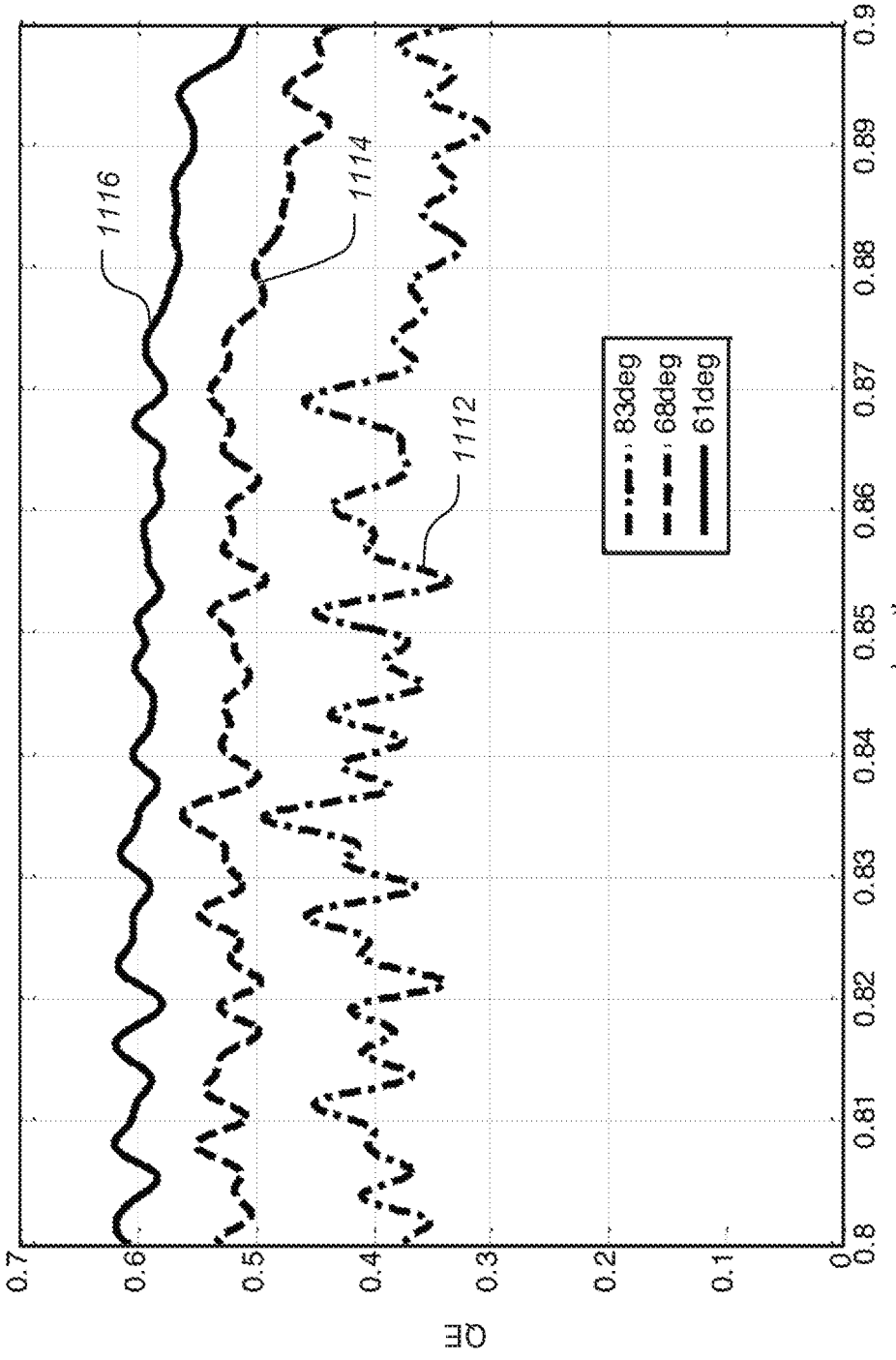

1116
1114
1112
83deg
68deg
61deg
QE
wavelength, um
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9

FIG. 11

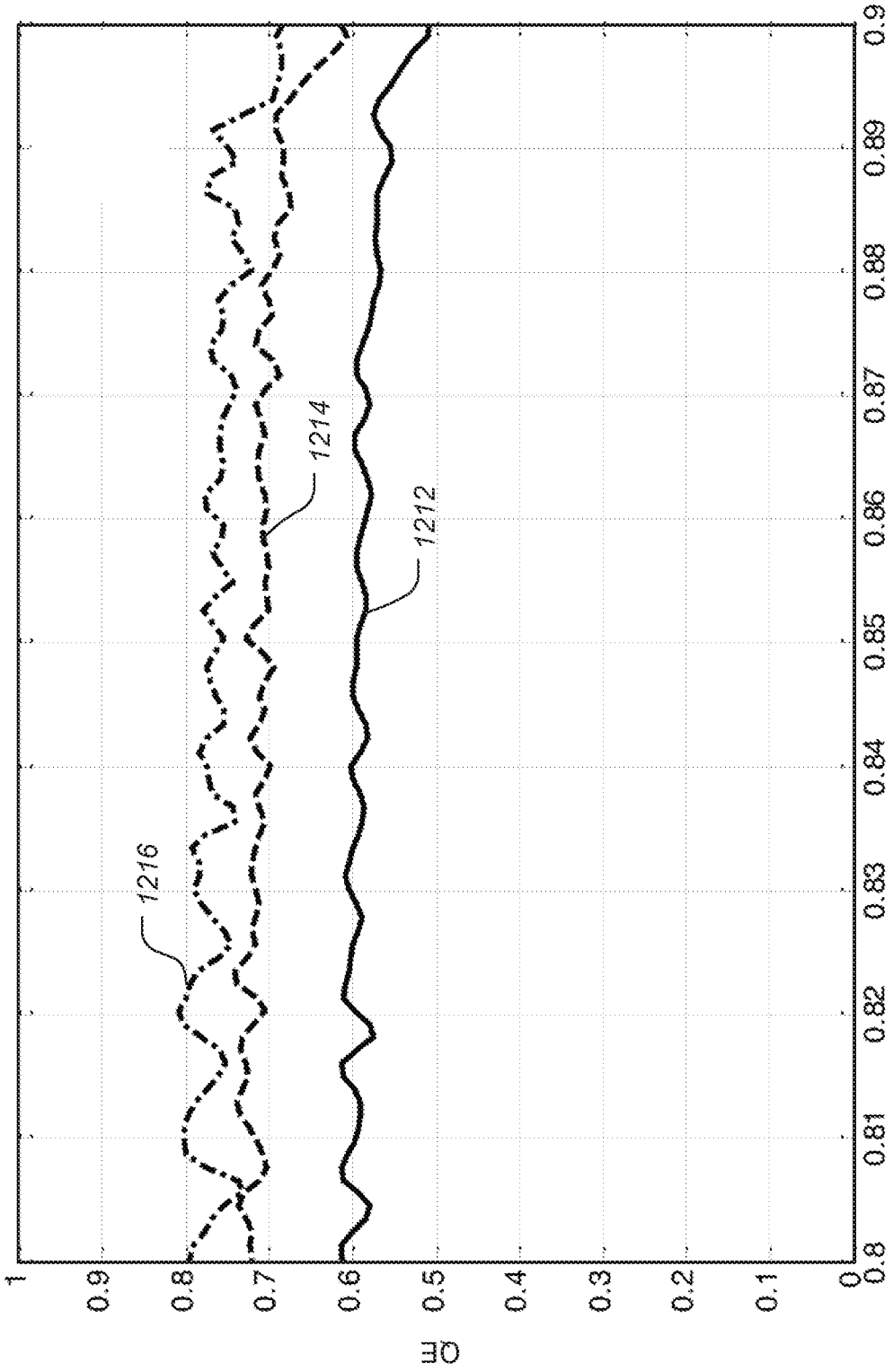

EQE
wavelength, um
1216
1214
1212
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9

FIG. 12A

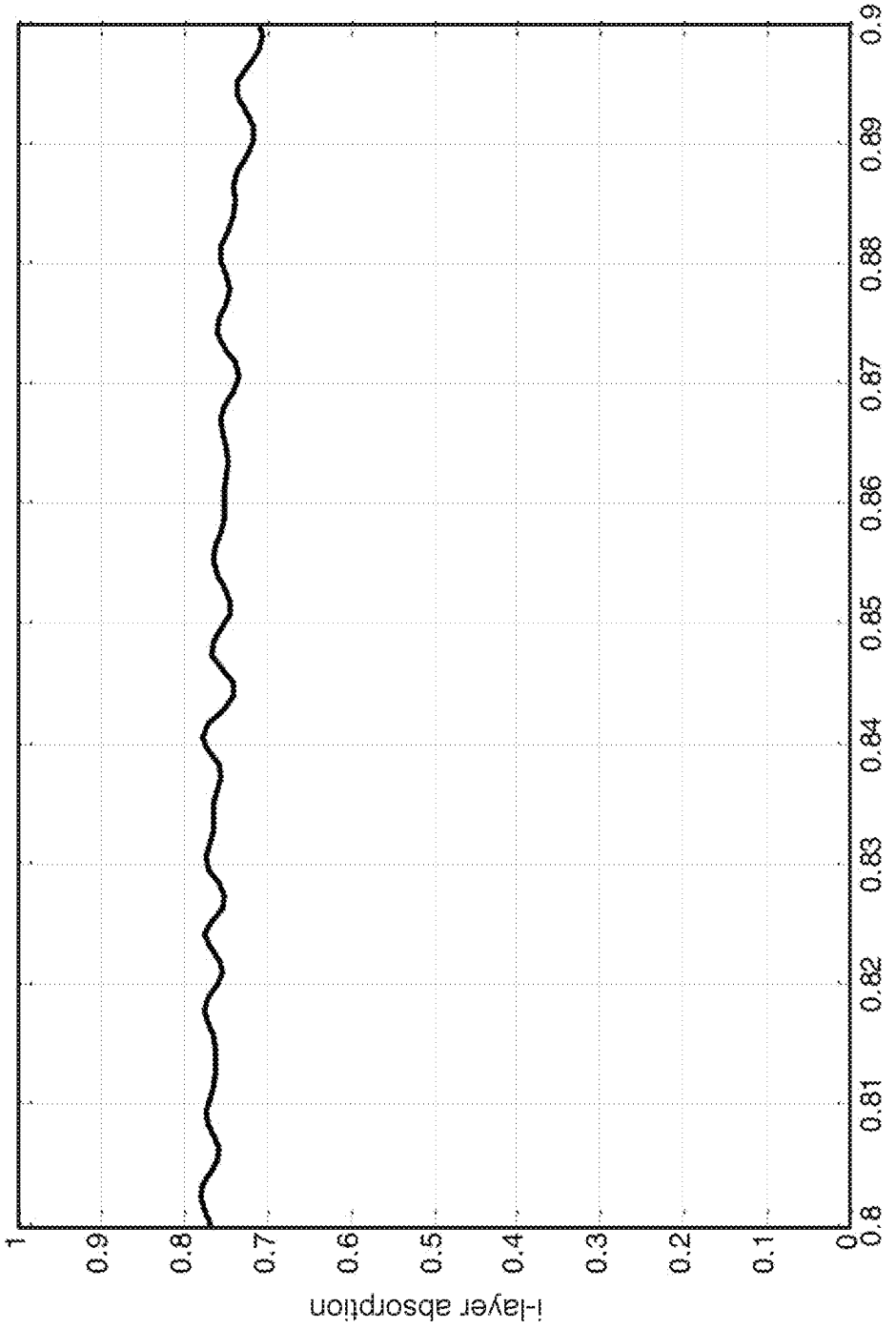

i-layer absorption
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9
wavelength, um

FIG. 12B

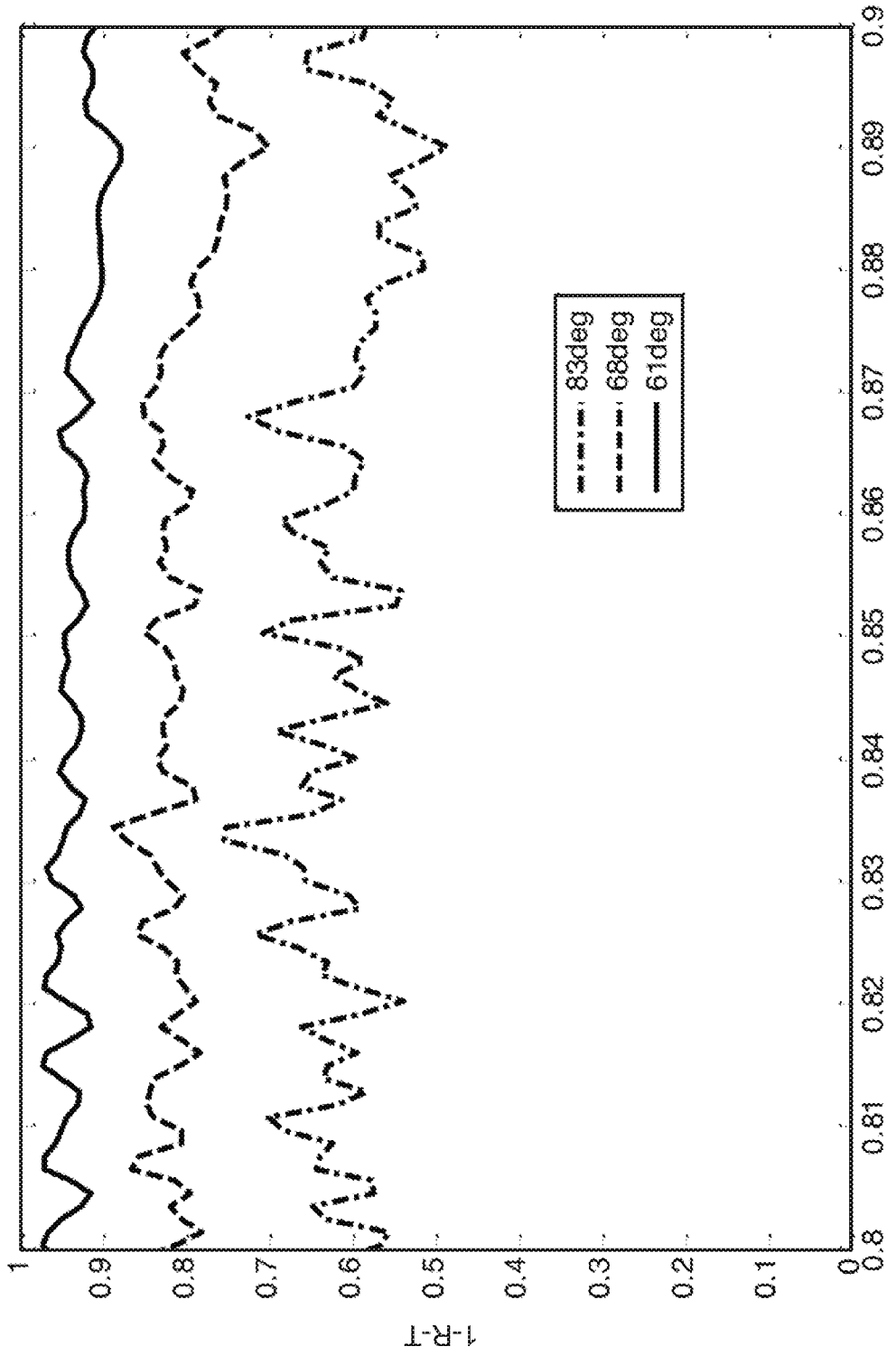

1-R-T
wavelength, um
83deg
68deg
61deg
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9

FIG. 13

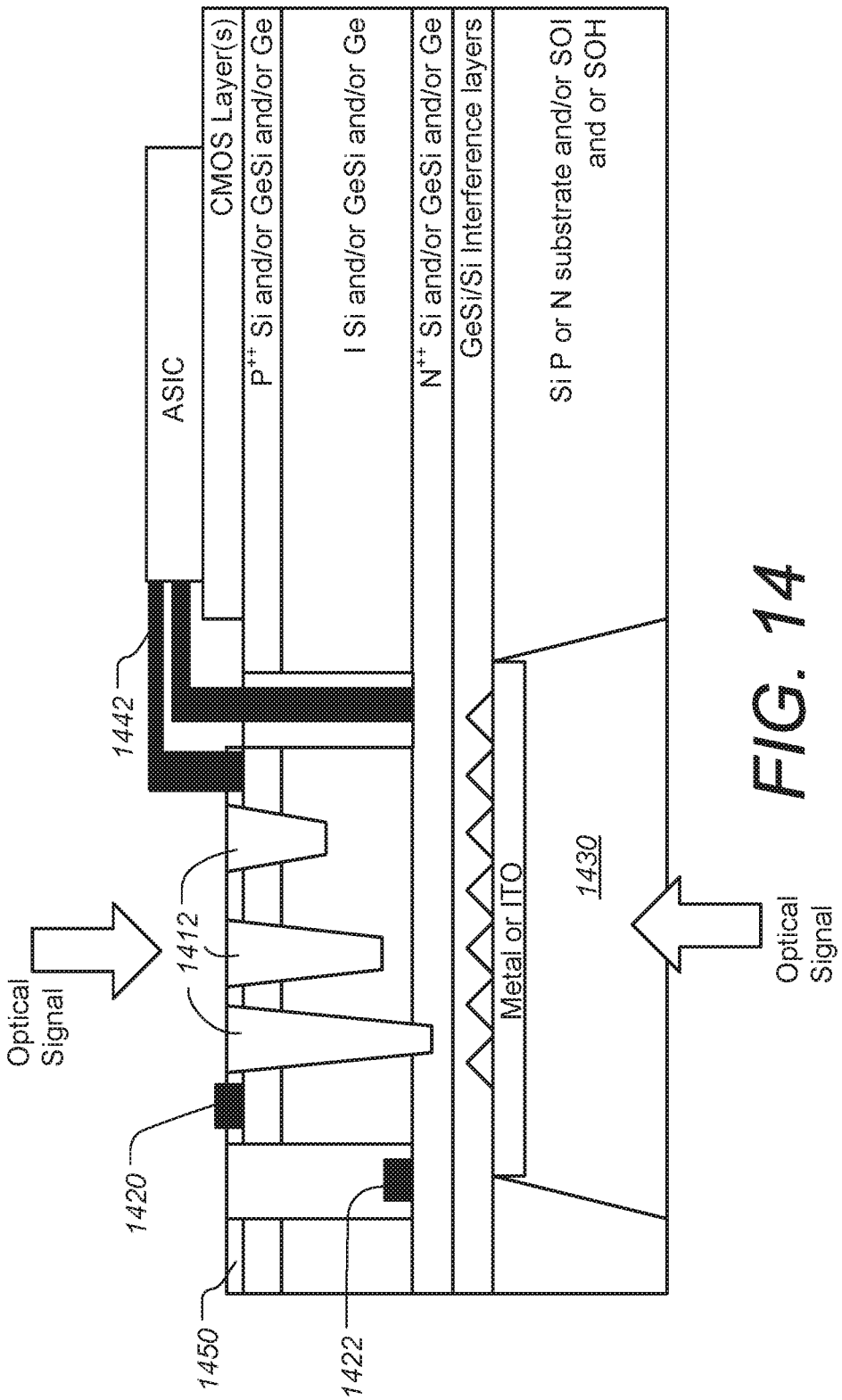

ASIC
CMOS Layer(s)
P++ Si and/or GeSi and/or Ge
I Si and/or GeSi and/or Ge
N++ Si and/or GeSi and/or Ge
GeSi/Si Interference layers
Si P or N substrate and/or SOI and or SOH
Metal or ITO
1430
Optical Signal
Optical Signal
1442
1412
1420
1450
1422

FIG. 14

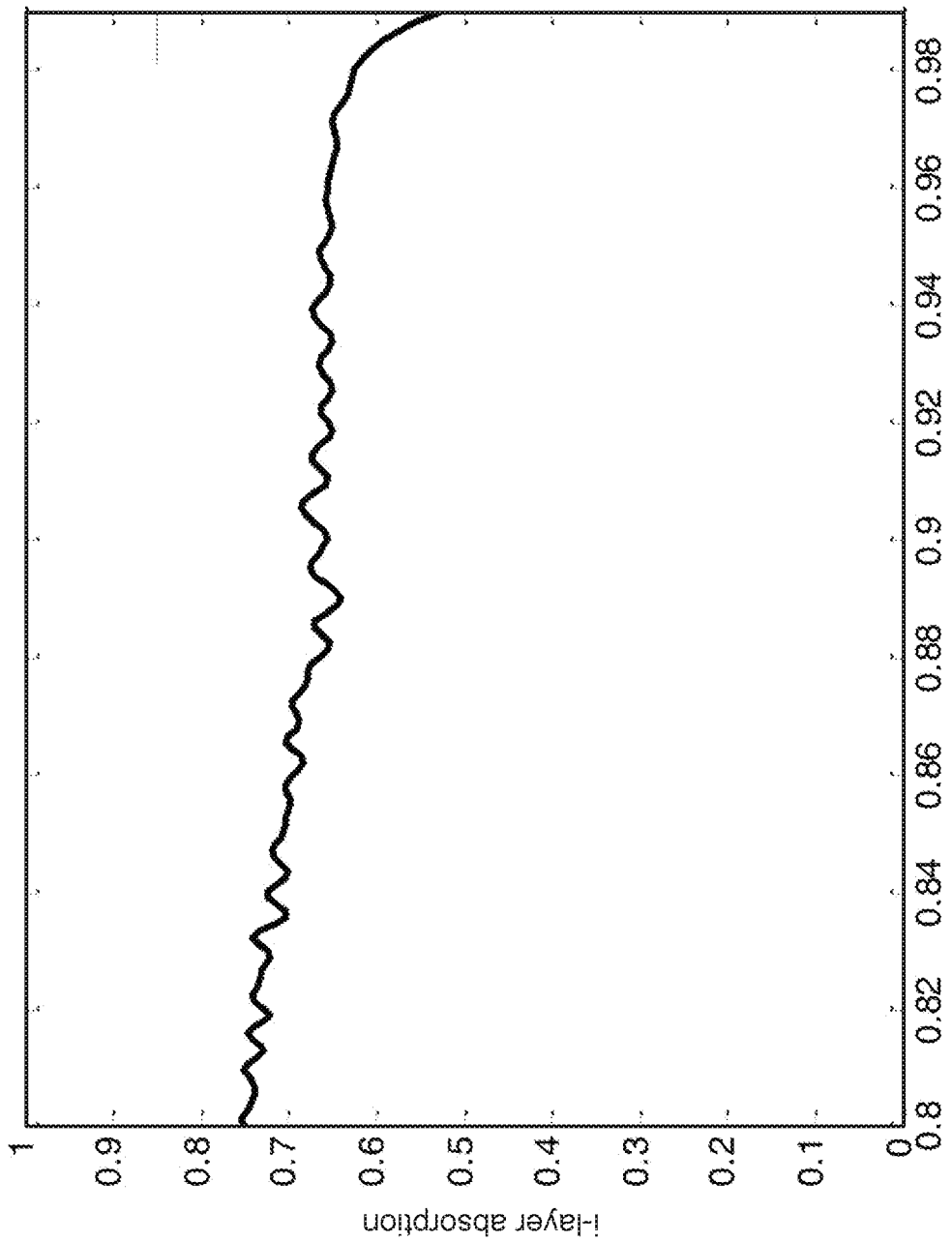

i-layer absorption
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.82
0.84
0.86
0.88
0.9
0.92
0.94
0.96
0.98
wavelength, um

FIG. 15

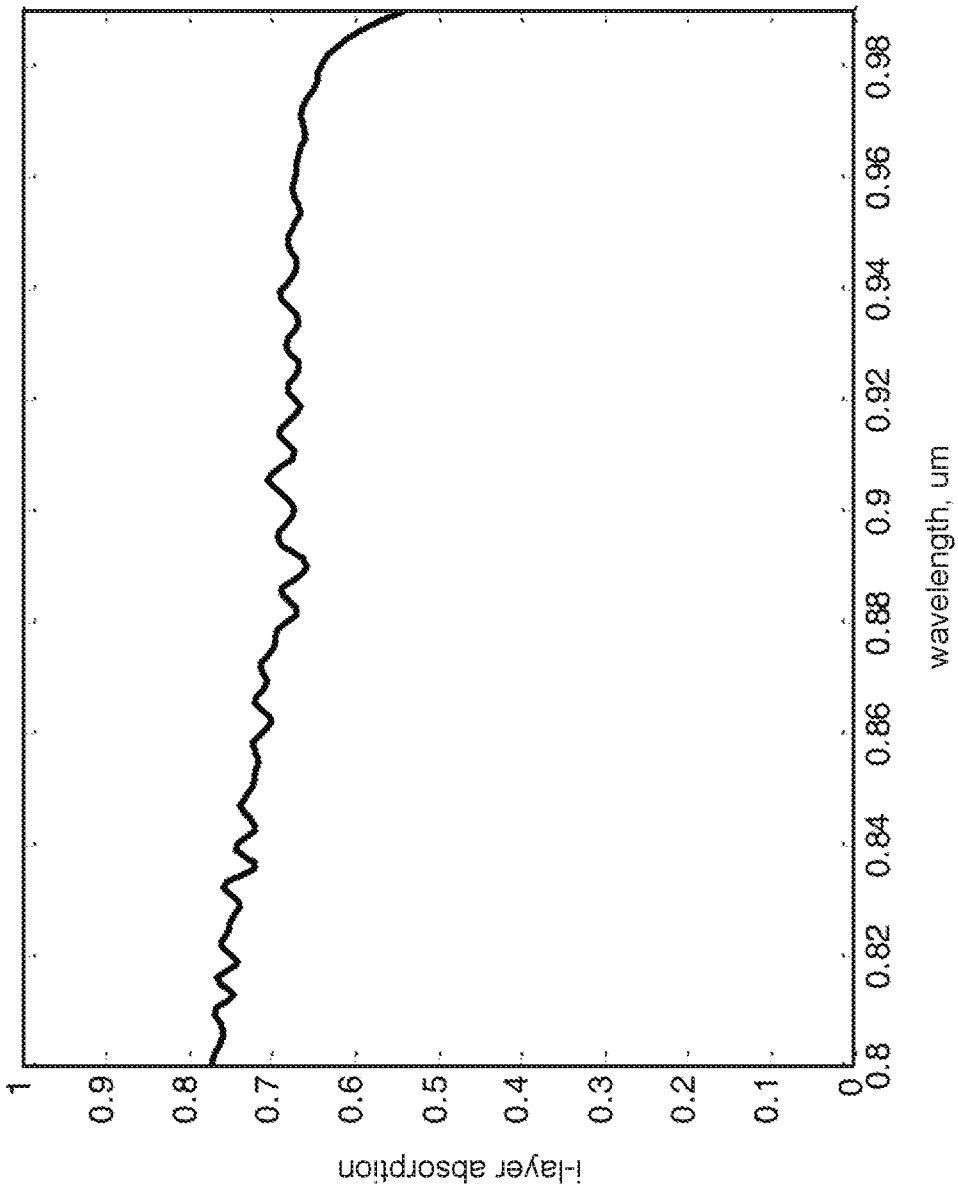

i-layer absorption
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.82
0.84
0.86
0.88
0.9
0.92
0.94
0.96
0.98
wavelength, um

FIG. 16

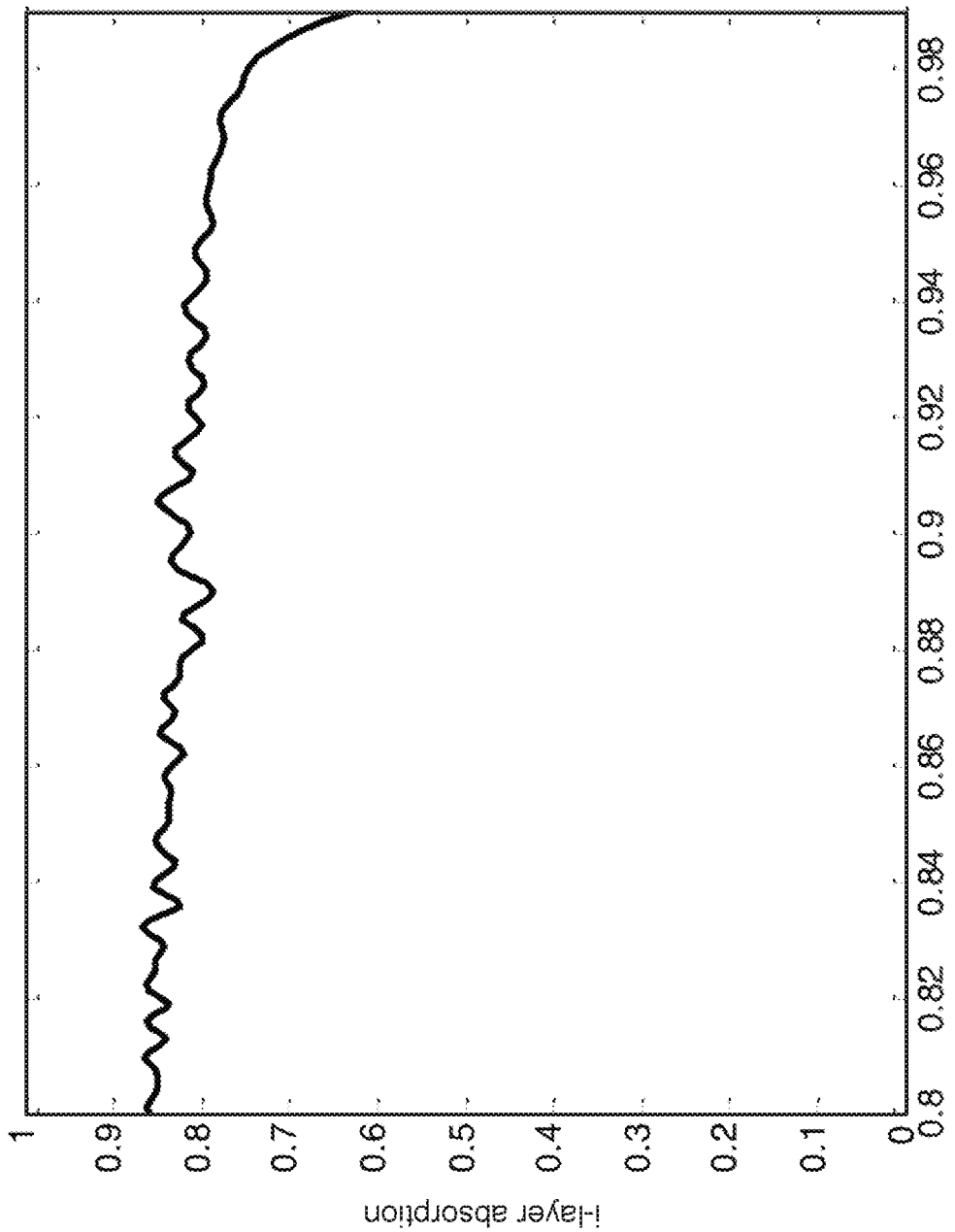

i-layer absorption
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.82
0.84
0.86
0.88
0.9
0.92
0.94
0.96
0.98
wavelength, um

FIG. 17

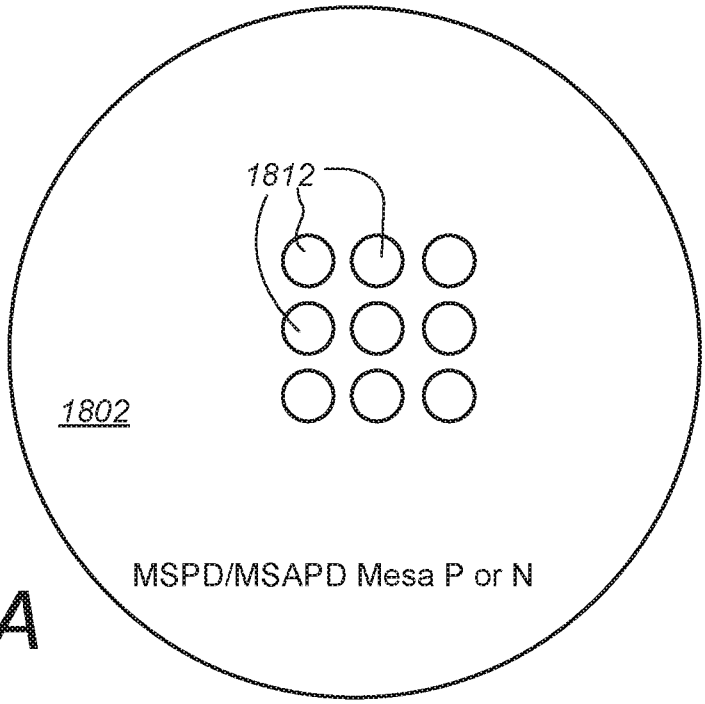


FIG. 18A

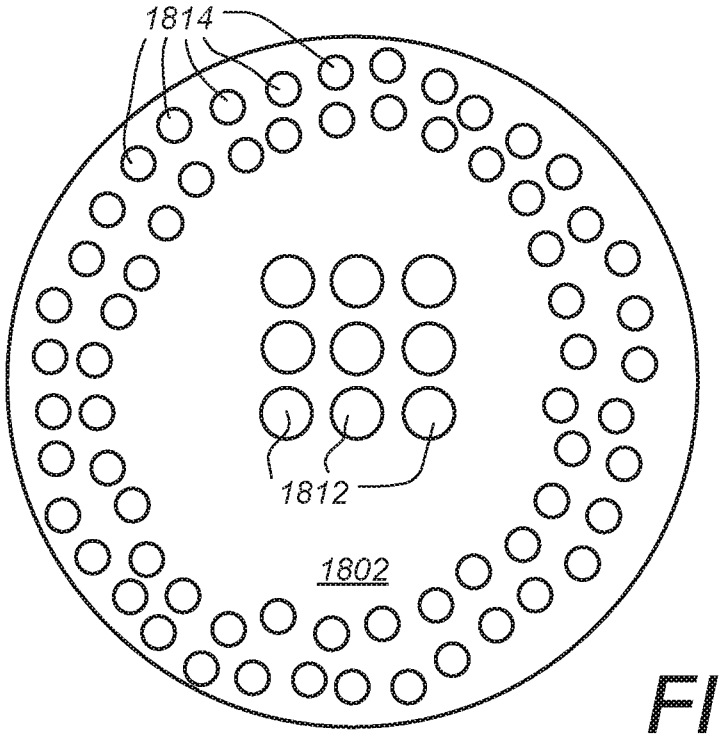


FIG. 18B

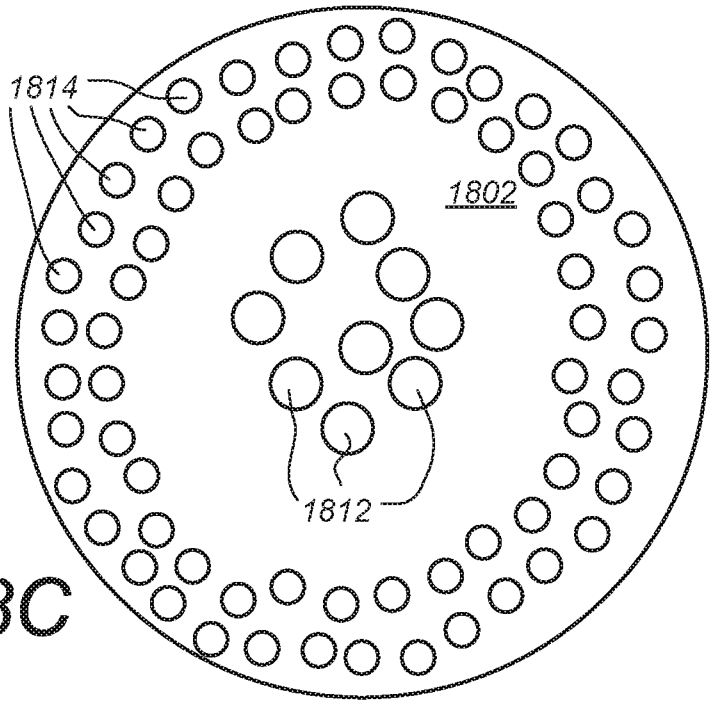


FIG. 18C

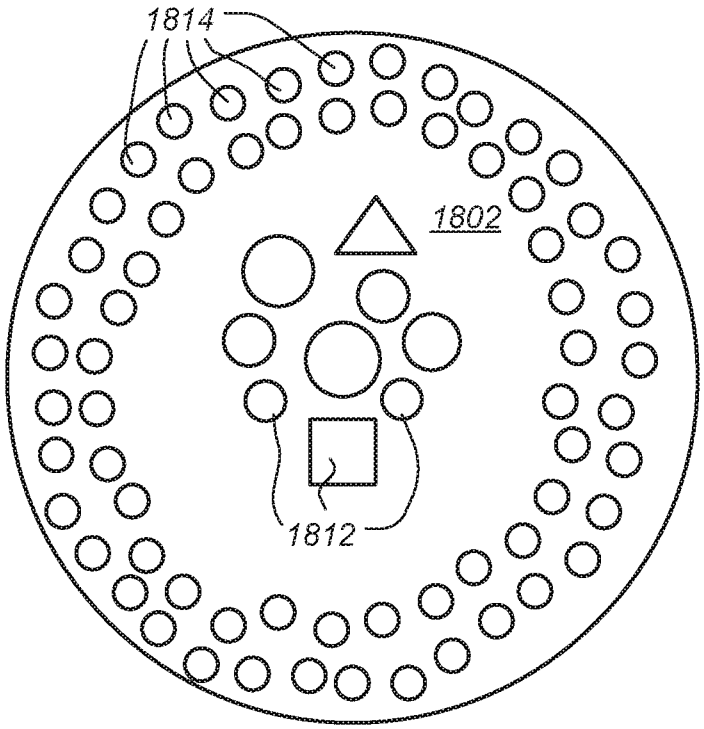


FIG. 18D

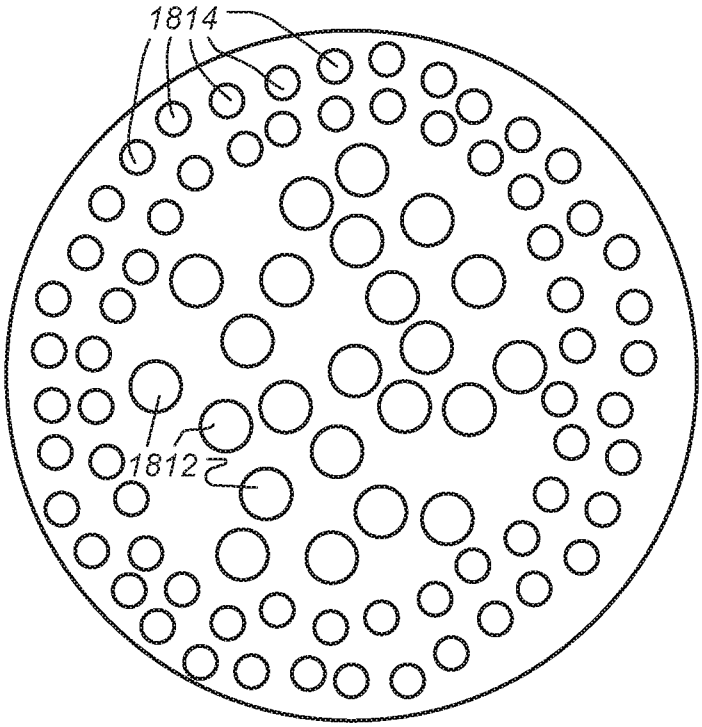


FIG. 18E

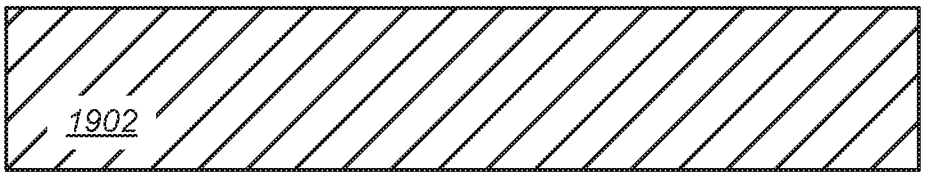


FIG. 19A

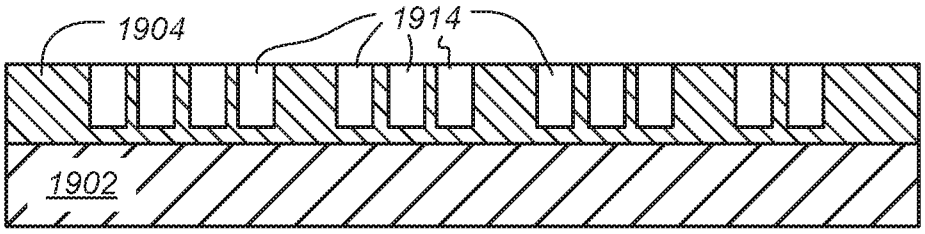


FIG. 19B

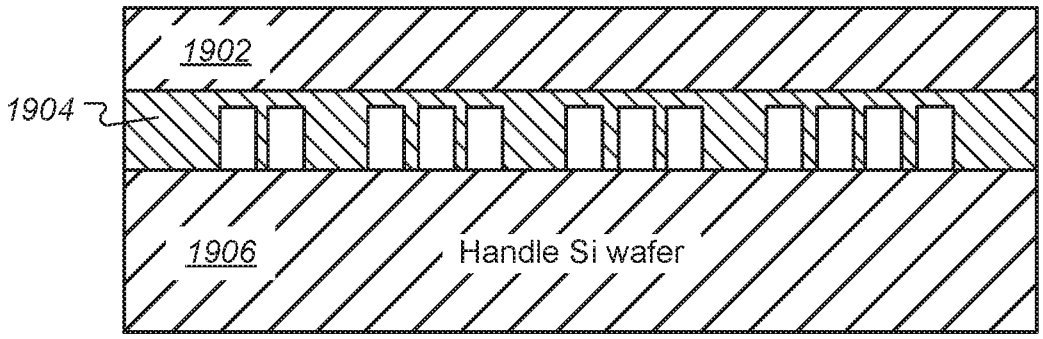


FIG. 19C

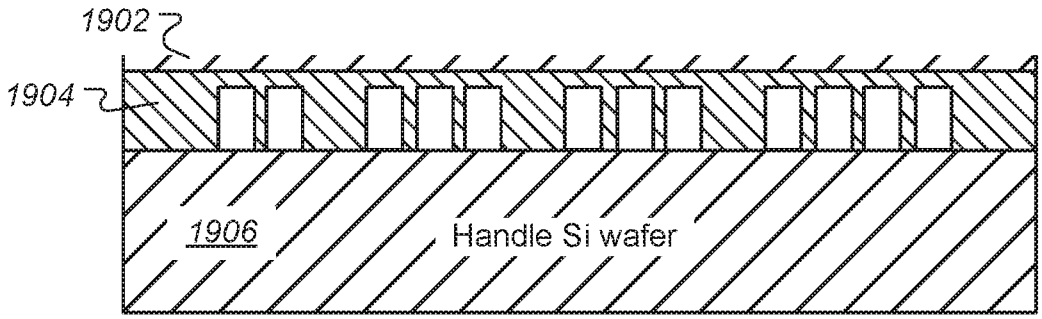


FIG. 19D

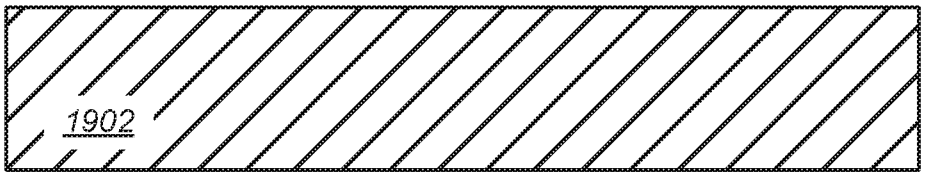


FIG. 19E

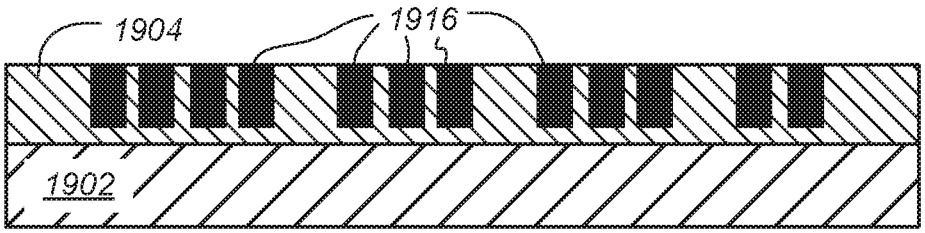


FIG. 19F

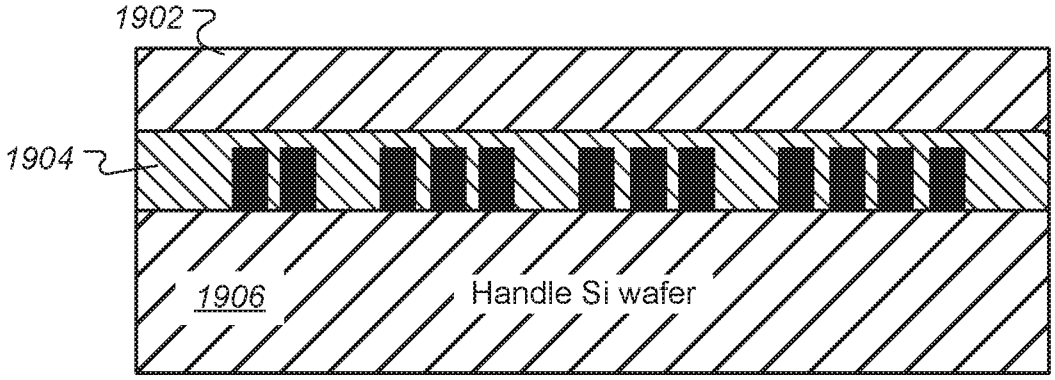


FIG. 19G

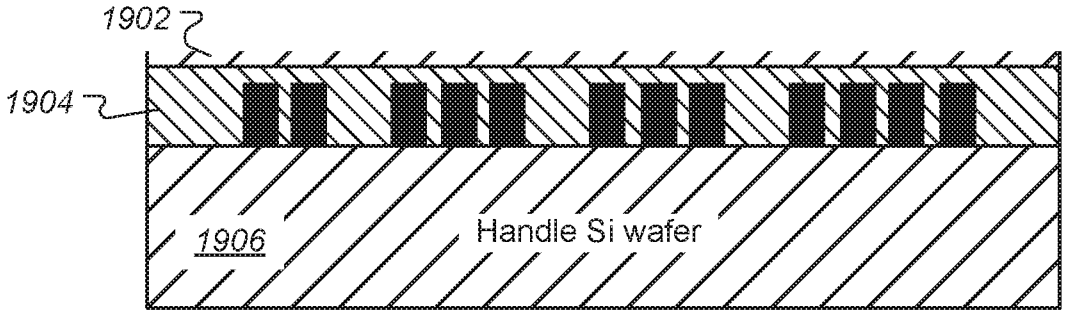


FIG. 19H

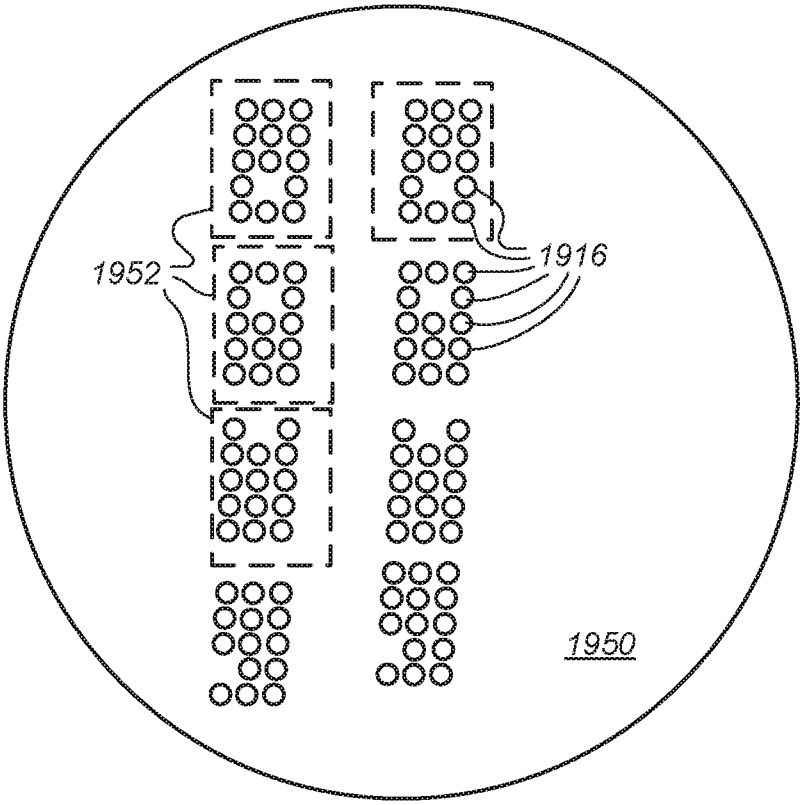


FIG. 19I

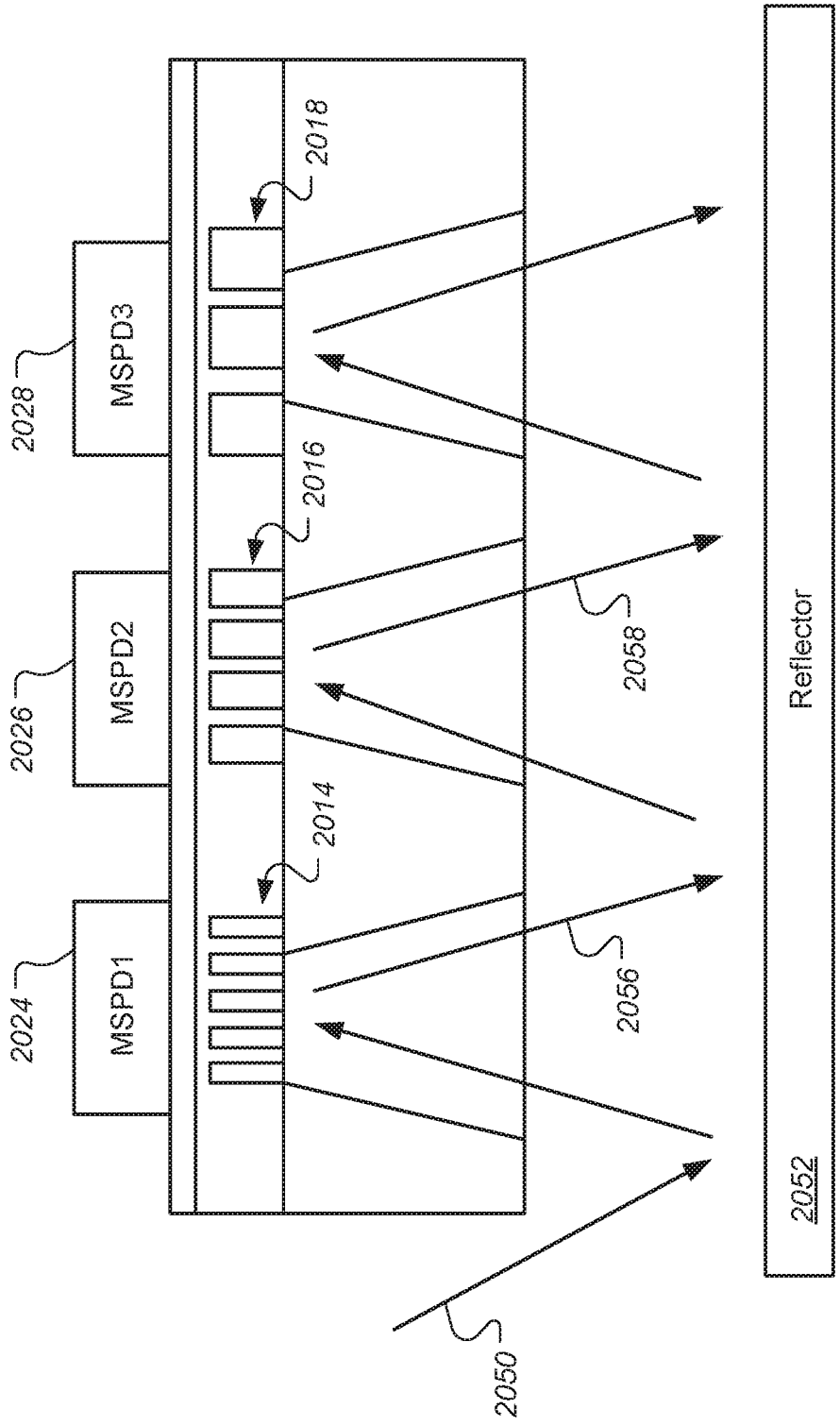

MSPD3
MSPD2
MSPD1
2028
2026
2024
2018
2016
2014
2058
2056
2050
Reflector
2052

FIG. 20

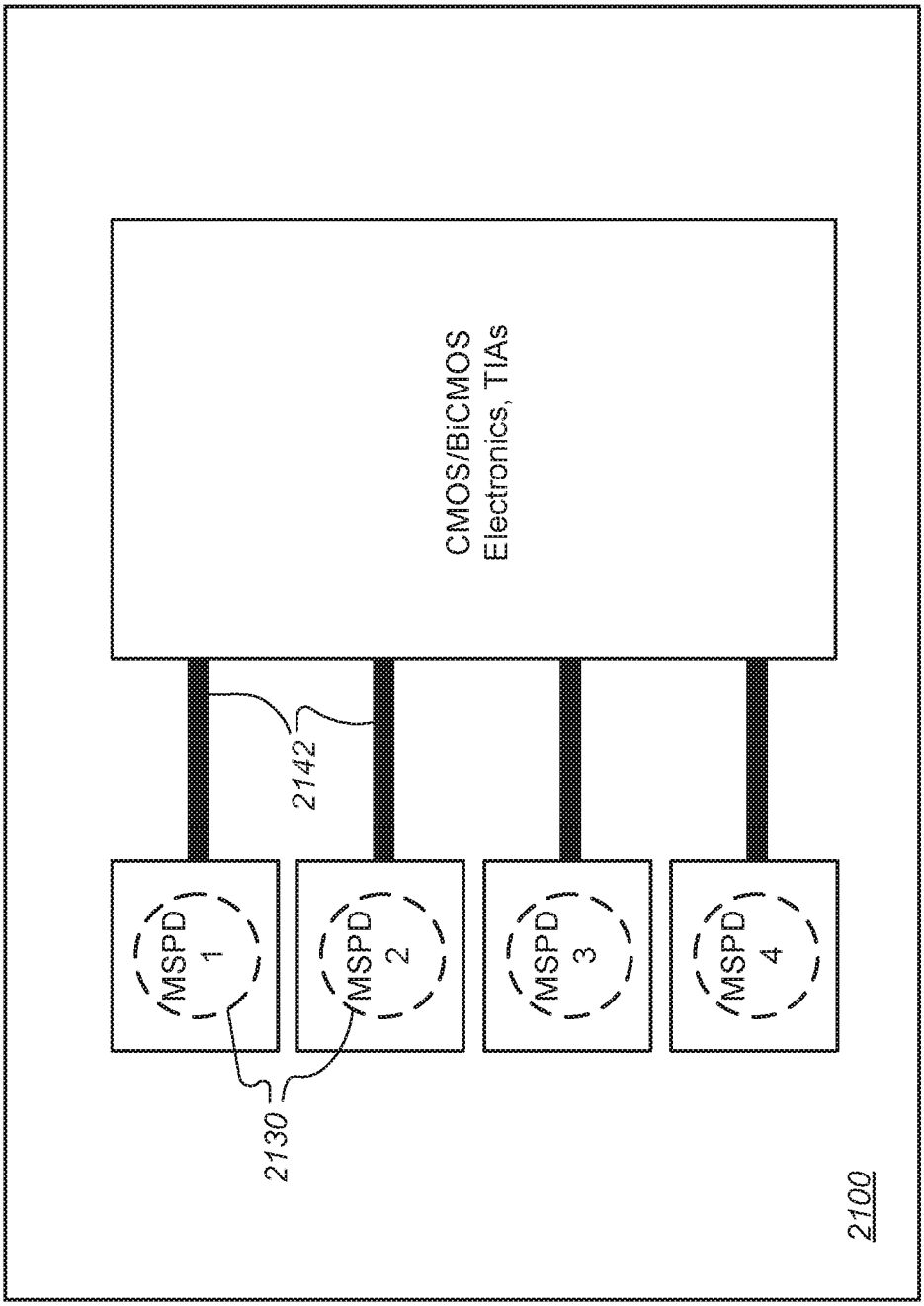

CMOS/BiCMOS
Electronics, TIAs
2142
MSPD 1
MSPD 2
MSPD 3
MSPD 4
2130
2100

FIG. 21

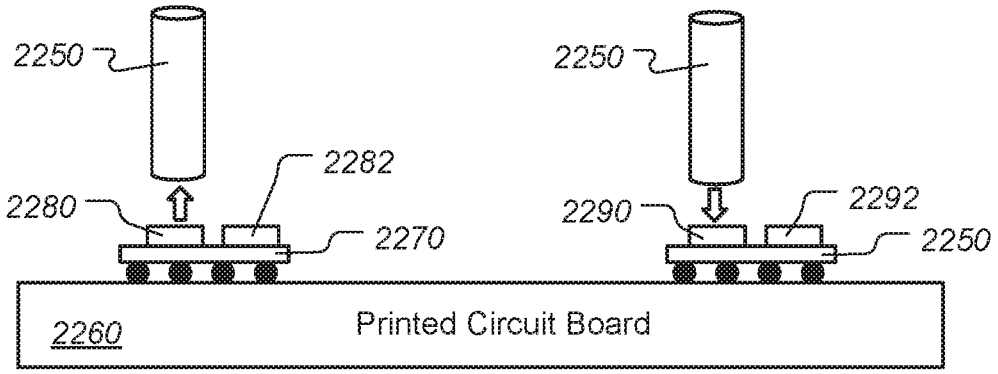


FIG. 22A
(prior art)

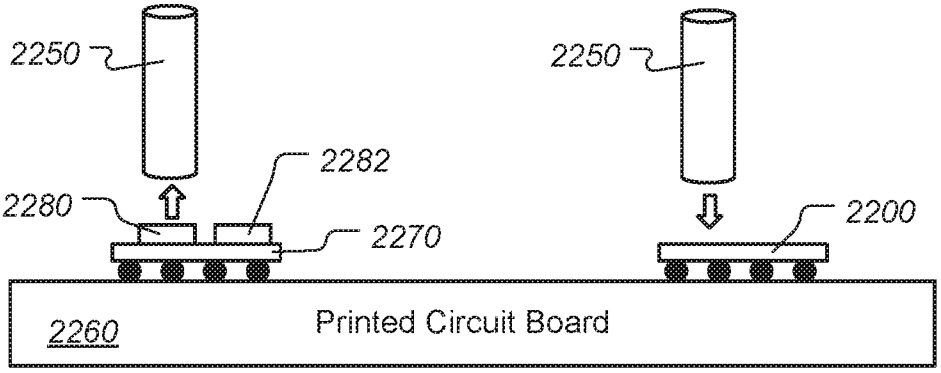


FIG. 22B

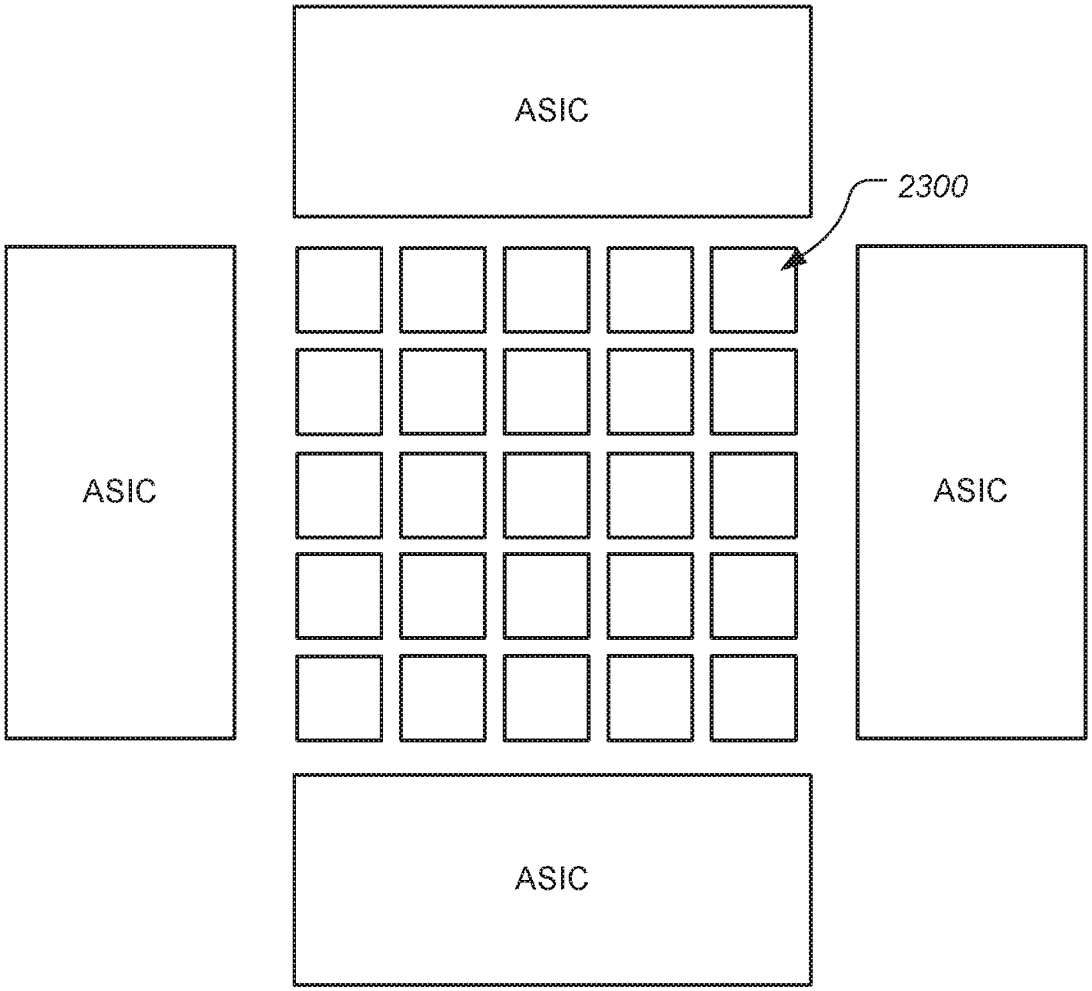


FIG. 23

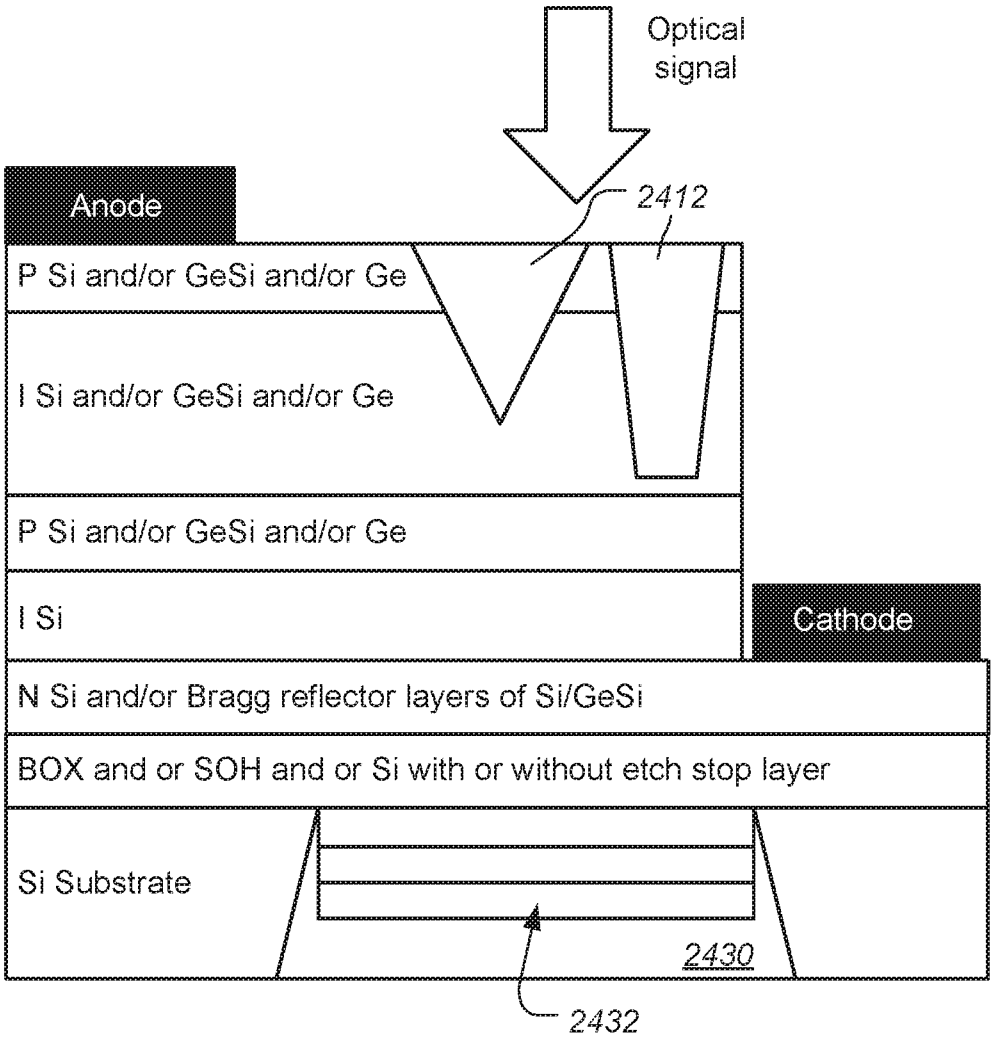

Optical signal
2412
Anode
P Si and/or GeSi and/or Ge
I Si and/or GeSi and/or Ge
P Si and/or GeSi and/or Ge
I Si
Cathode
N Si and/or Bragg reflector layers of Si/GeSi
BOX and or SOH and or Si with or without etch stop layer
Si Substrate
2430
2432

FIG. 24

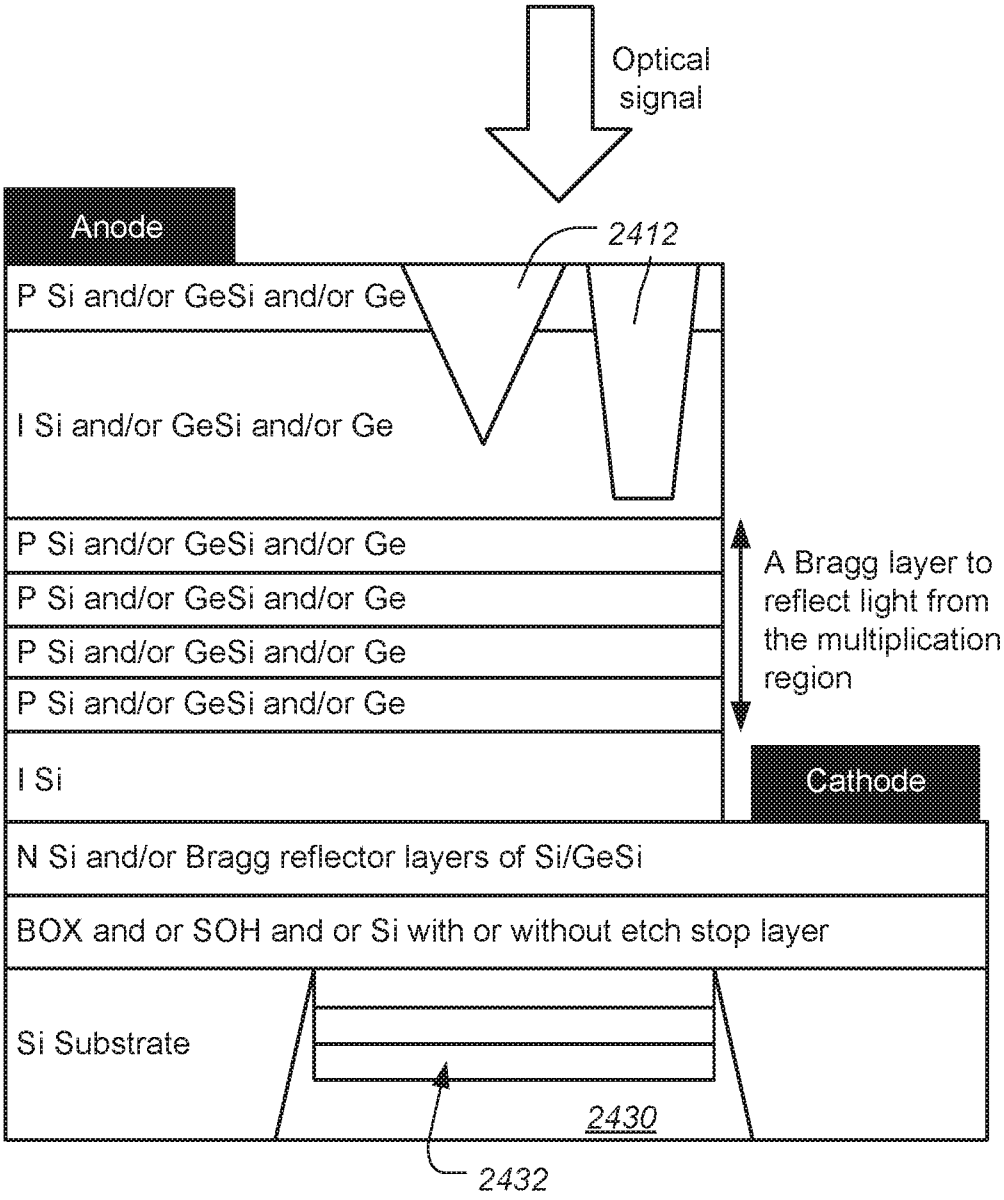

Optical signal
Anode
2412
P Si and/or GeSi and/or Ge
I Si and/or GeSi and/or Ge
P Si and/or GeSi and/or Ge
P Si and/or GeSi and/or Ge
P Si and/or GeSi and/or Ge
P Si and/or GeSi and/or Ge
A Bragg layer to reflect light from the multiplication region
I Si
Cathode
N Si and/or Bragg reflector layers of Si/GeSi
BOX and or SOH and or Si with or without etch stop layer
Si Substrate
2430
2432

FIG. 25

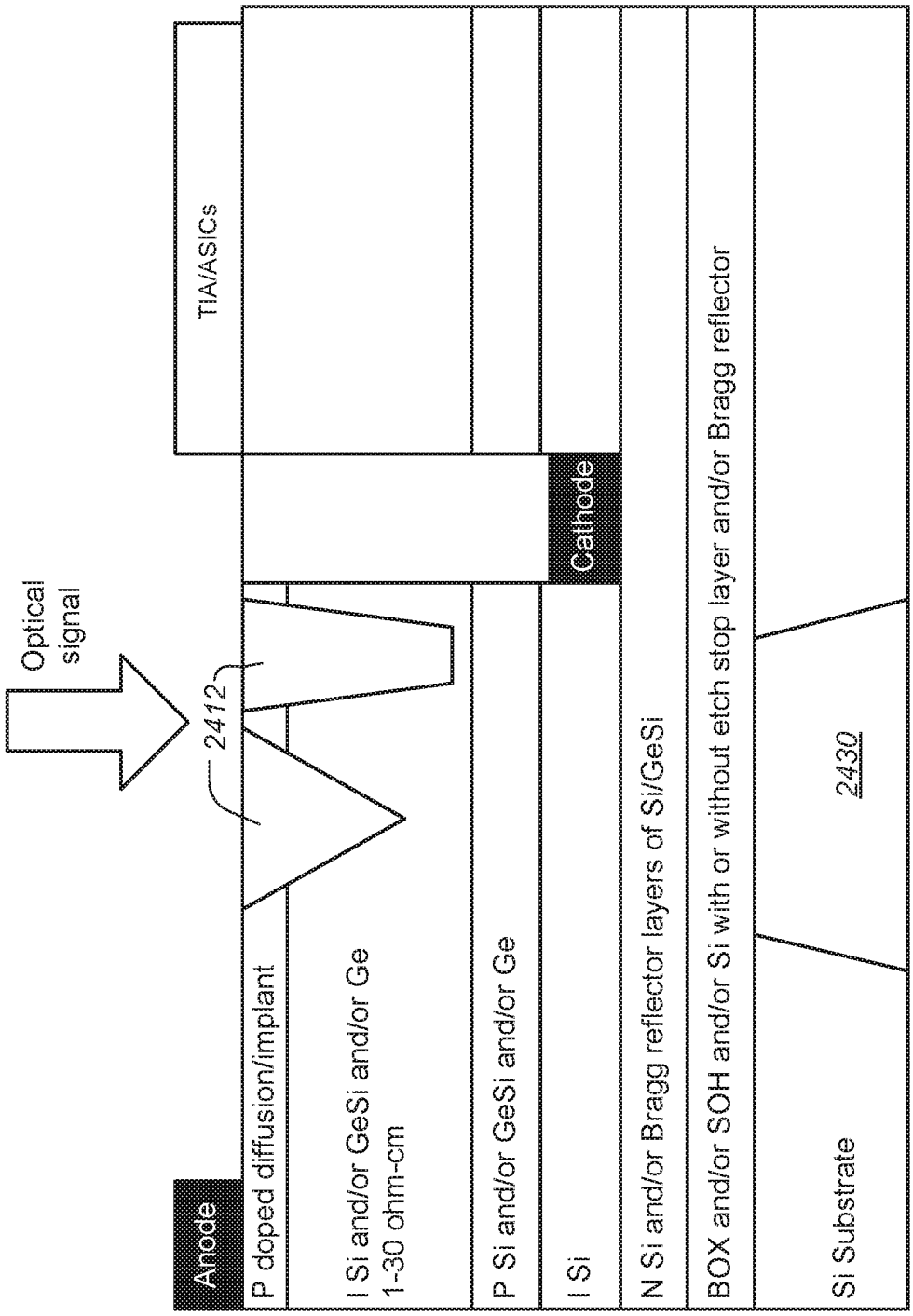

TIA/ASICs
Optical signal
2412
Anode
P doped diffusion/implant
I Si and/or GeSi and/or Ge
1-30 ohm-cm
P Si and/or GeSi and/or Ge
I Si
Cathode
N Si and/or Bragg reflector layers of Si/GeSi
BOX and/or SOH and/or Si with or without etch stop layer and/or Bragg reflector
Si Substrate
2430

FIG. 26

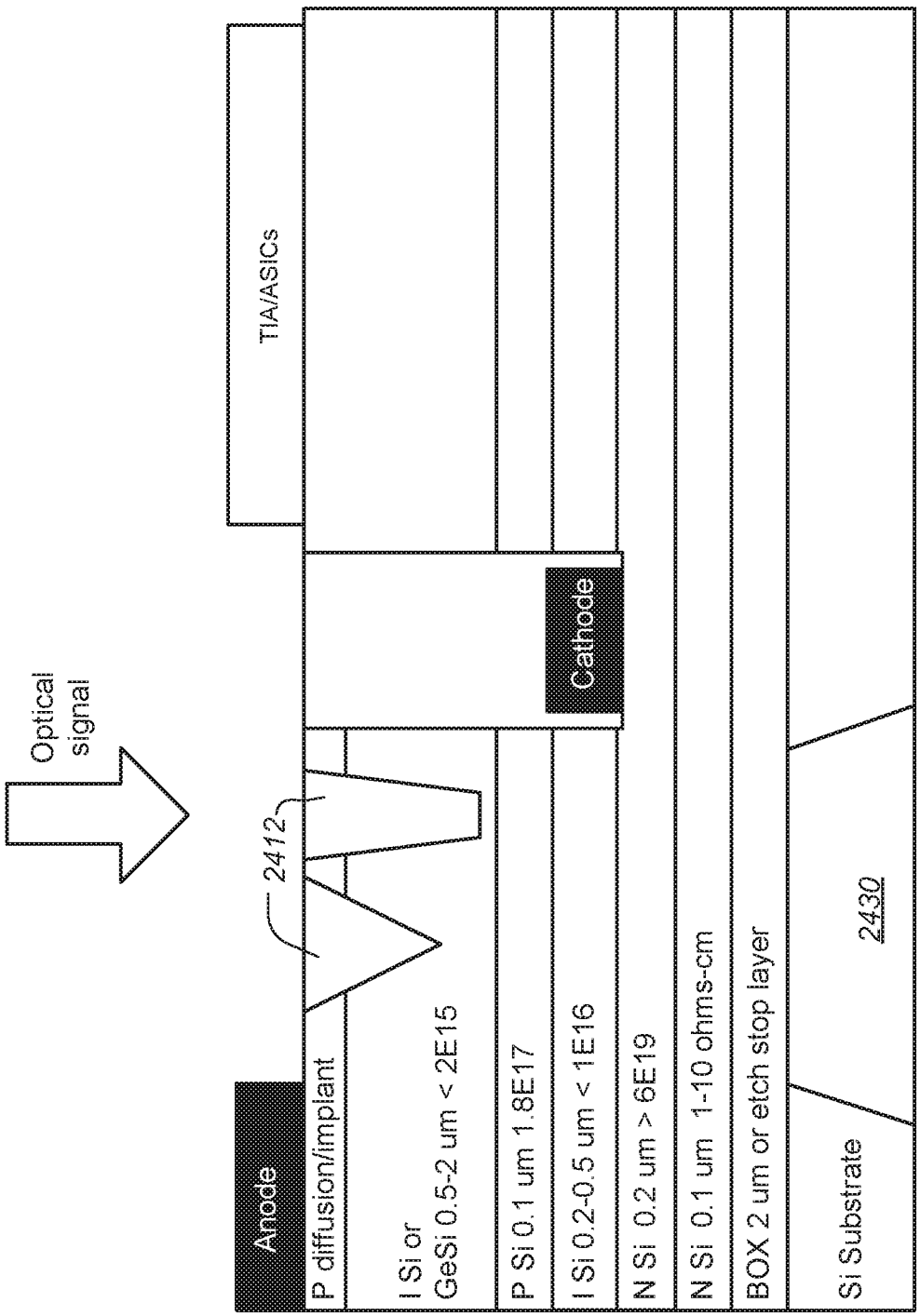

Optical signal
TIA/ASICs
Anode
Cathode
2412
2430
P diffusion/implant
I Si or GeSi 0.5-2 um < 2E15
P Si 0.1 um 1.8E17
I Si 0.2-0.5 um < 1E16
N Si 0.2 um > 6E19
N Si 0.1 um 1-10 ohms-cm
BOX 2 um or etch stop layer
Si Substrate

FIG. 27

d/p:700/1000nm	Responsivity (A/W) @980 nm	Responsivity (A/W) @990 nm
KOH-only	0.156	0.138
KOH+DRIE	0.142	0.116
61° tapered	0.144	0.130
68° tapered	0.122	0.111
83° tapered	0.112	0.096
90° straight	0.092	0.079
2 μm Si-theory	0.015	0.012

FIG. 28

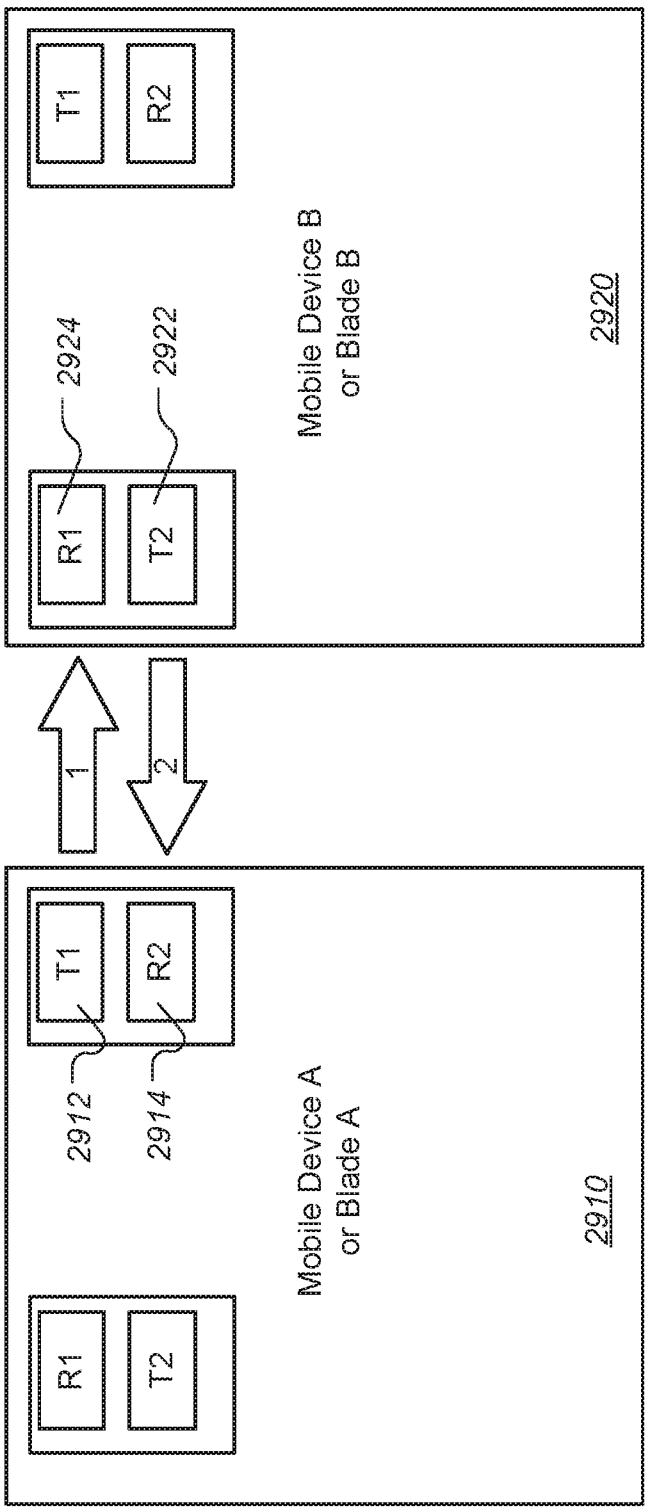

T1
R2
2924
2922
R1
T2
Mobile Device B
or Blade B
2920
1
2
T1
R2
2912
2914
R1
T2
Mobile Device A
or Blade A
2910

FIG. 29

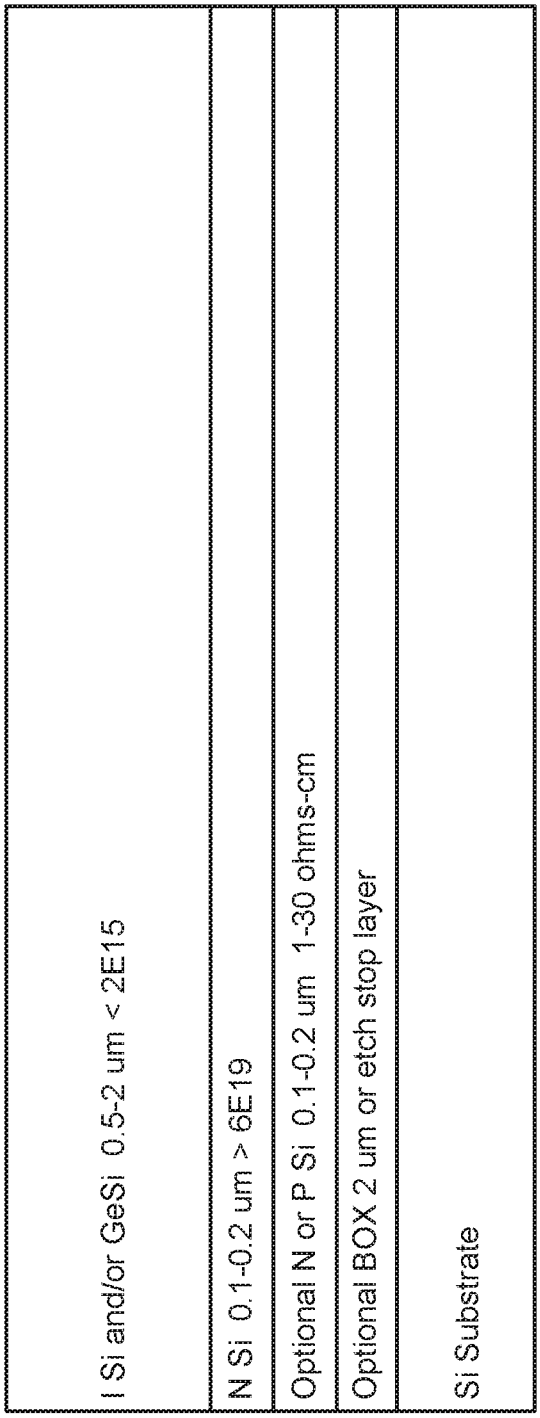

I Si and/or GeSi 0.5-2 um < 2E15
N Si 0.1-0.2 um > 6E19
Optional N or P Si 0.1-0.2 um 1-30 ohms-cm
Optional BOX 2 um or etch stop layer
Si Substrate

FIG. 30

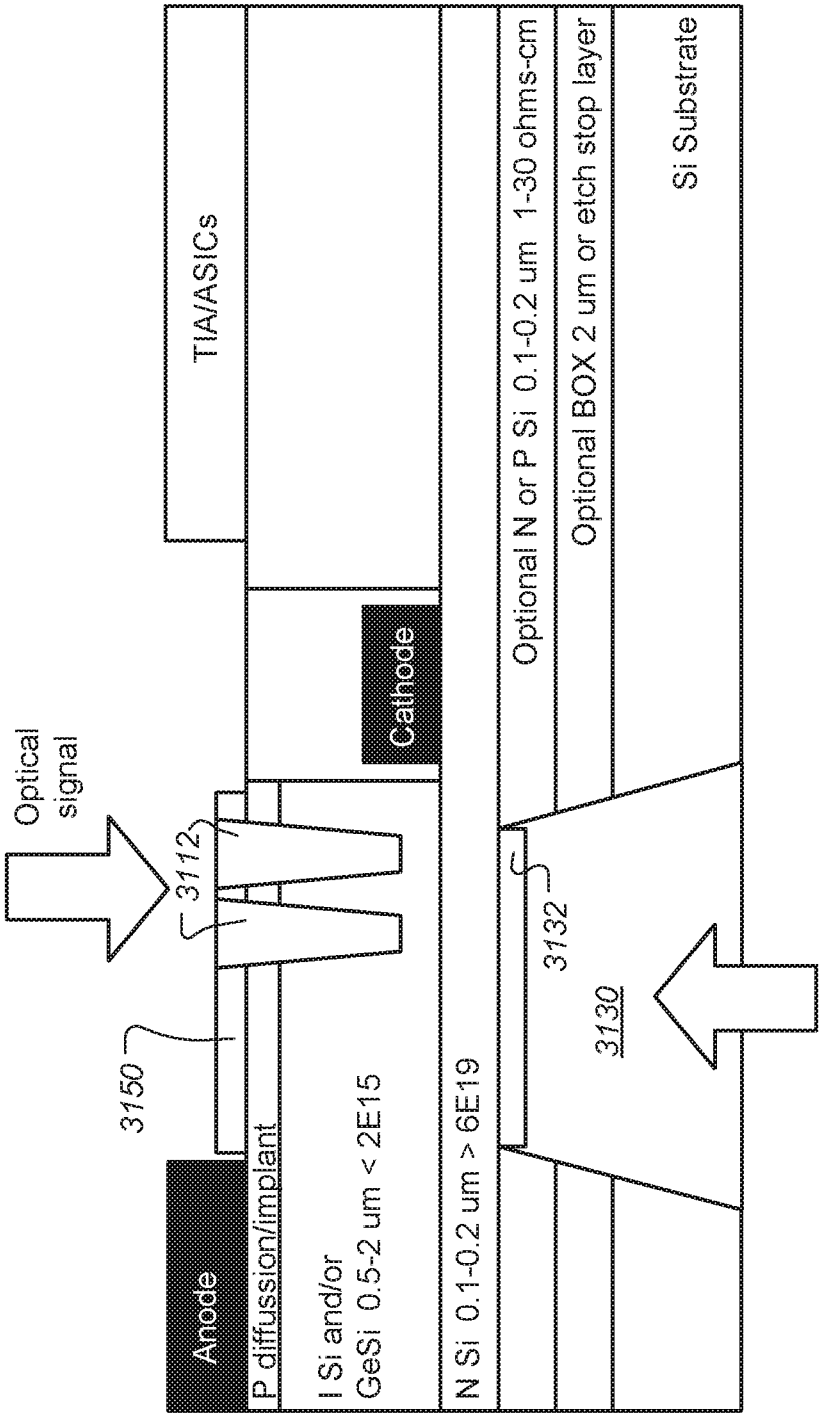

Optical signal
3112
3150
Anode
P diffussion/implant
I Si and/or
GeSi 0.5-2 um < 2E15
Cathode
N Si 0.1-0.2 um > 6E19
Optional N or P Si 0.1-0.2 um 1-30 ohms-cm
Optional BOX 2 um or etch stop layer
Si Substrate
3132
3130
TIA/ASICs

FIG. 31

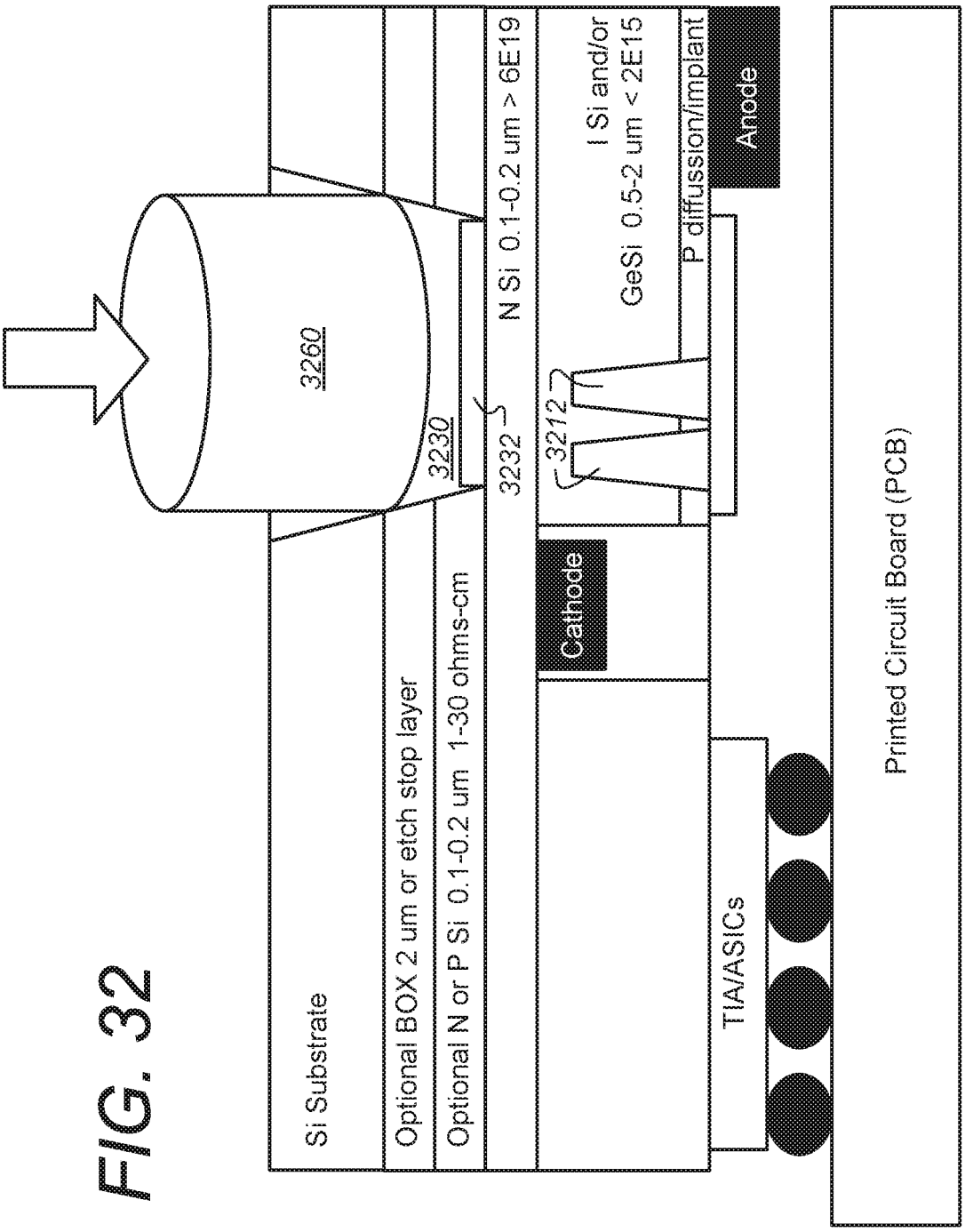

3260
3230
3232
3212
Si Substrate
Optional BOX 2 um or etch stop layer
Optional N or P Si 0.1-0.2 um 1-30 ohms-cm
N Si 0.1-0.2 um > 6E19
I Si and/or
GeSi 0.5-2 um < 2E15
P diffussion/implant
Anode
Cathode
TIA/ASICs
Printed Circuit Board (PCB)

FIG. 32

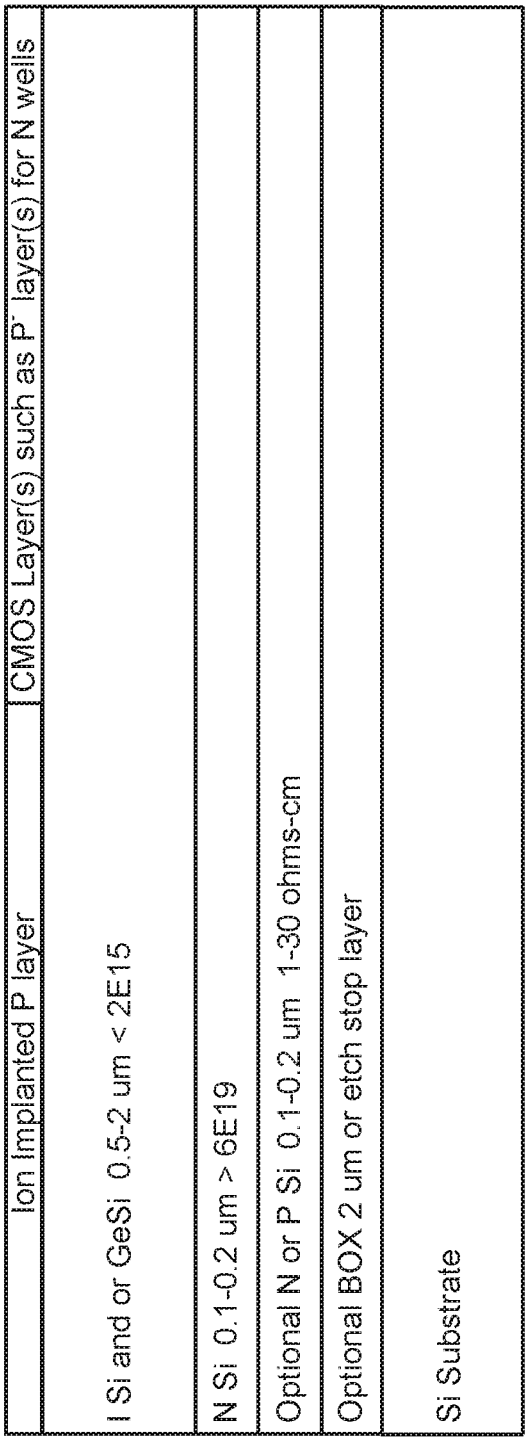

Ion Implanted P layer
CMOS Layer(s) such as P+ layer(s) for N wells
I Si and or GeSi 0.5-2 um < 2E15
N Si 0.1-0.2 um > 6E19
Optional N or P Si 0.1-0.2 um 1-30 ohms-cm
Optional BOX 2 um or etch stop layer
Si Substrate

FIG. 33

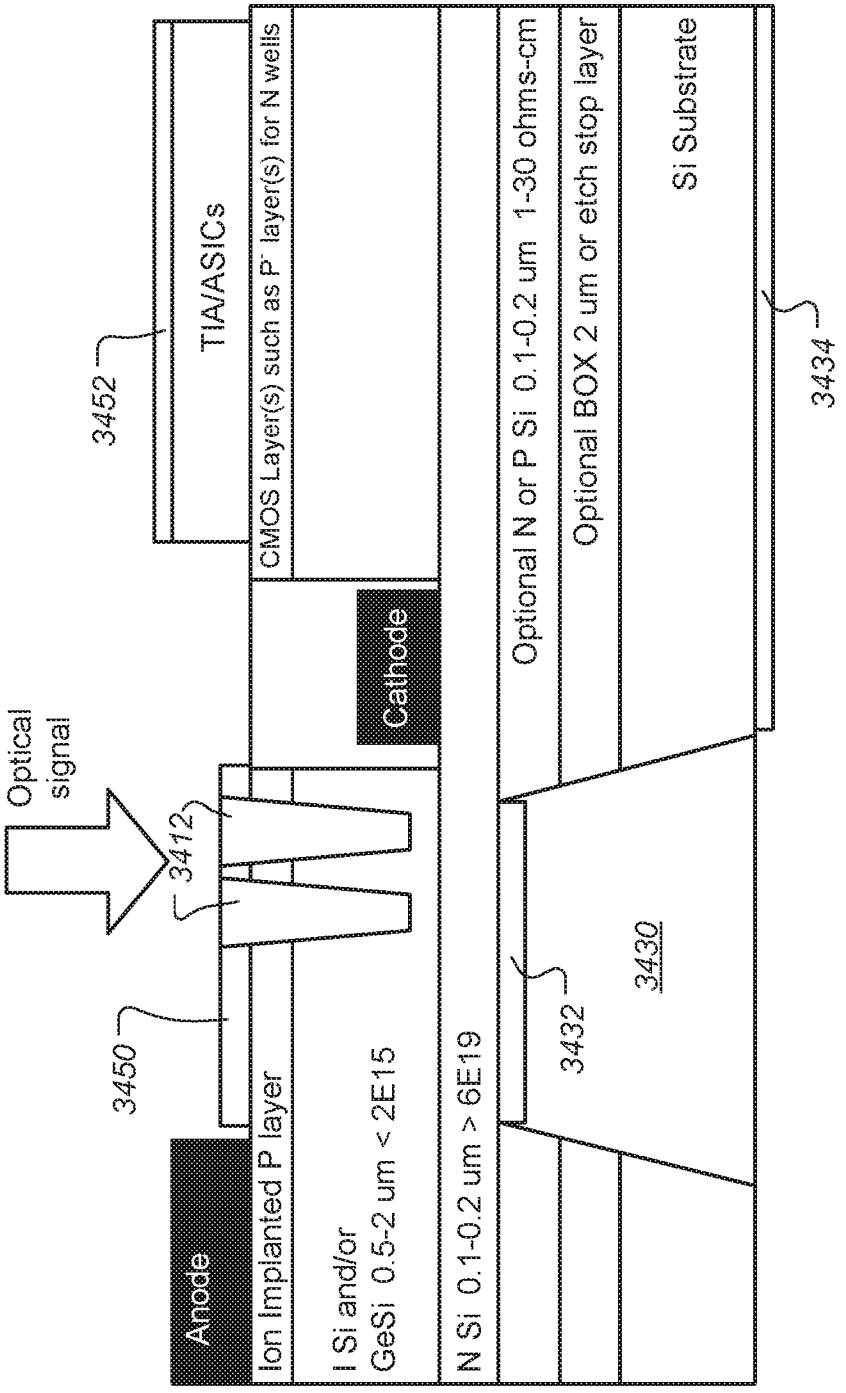

Optical signal
3412
3450
3452
3434
3430
3432
Anode
Ion Implanted P layer
I Si and/or GeSi 0.5-2 um < 2E15
N Si 0.1-0.2 um > 6E19
Cathode
CMOS Layer(s) such as P- layer(s) for N wells
TIA/ASICs
Optional N or P Si 0.1-0.2 um 1-30 ohms-cm
Optional BOX 2 um or etch stop layer
Si Substrate

FIG. 34

CMOS/BiCMOS Layer(s)
I Si and or GeSi 0.5-2 um < 2E15
P Si and or GeSi 0.1 um 1.8E17
I Si 0.5 um < 1E16
N Si 0.1-0.2 um > 6E19
Optional N or P Si 0.1-0.2 um 1-30 ohms-cm
Optional BOX 2 um or etch stop layer
Si Substrate

FIG. 35

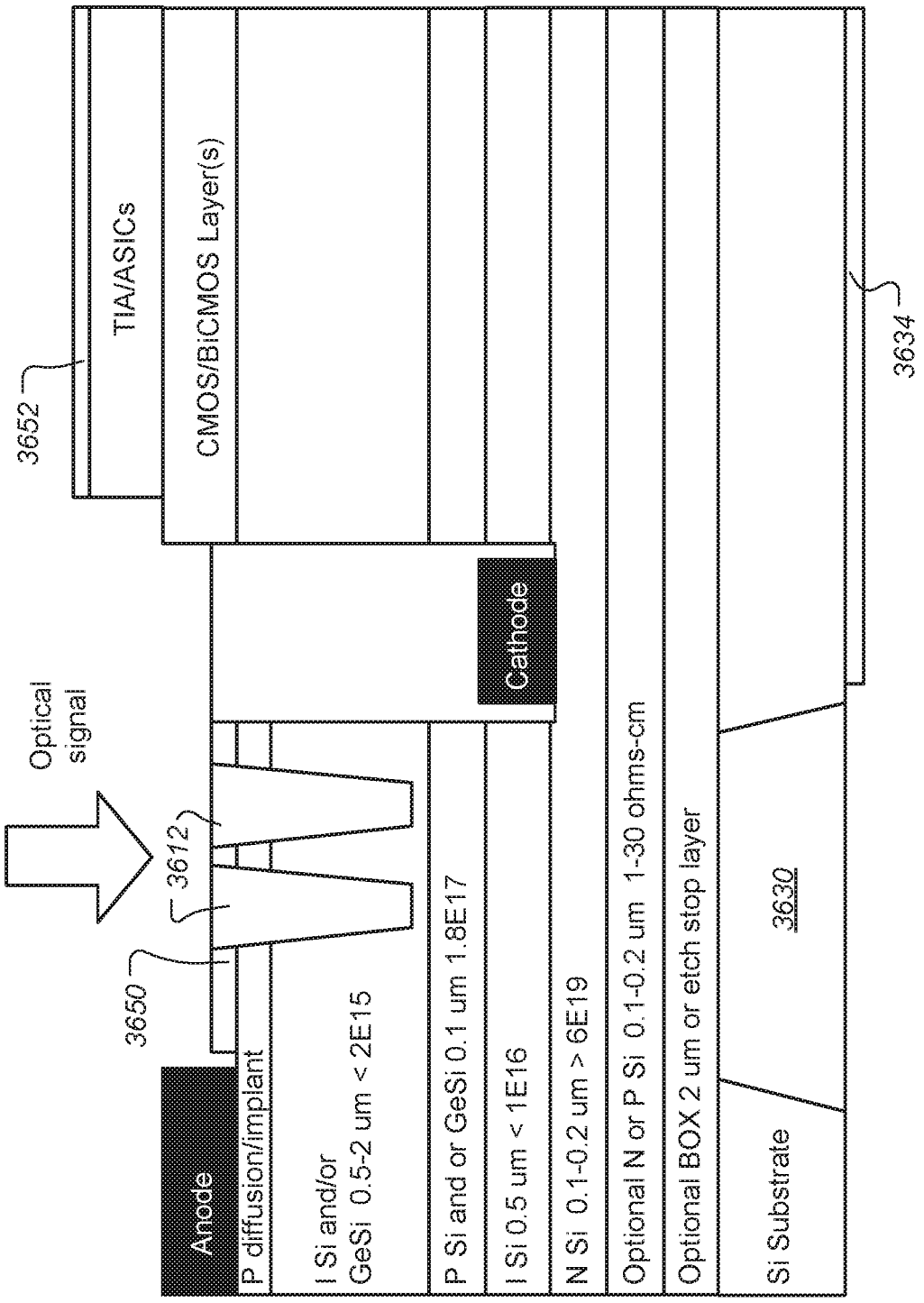

3652
TIA/ASICs
CMOS/BiCMOS Layer(s)
3634
Optical signal
3612
3650
Anode
P diffusion/implant
I Si and/or GeSi 0.5-2 um < 2E15
P Si and or GeSi 0.1 um 1.8E17
I Si 0.5 um < 1E16
Cathode
N Si 0.1-0.2 um > 6E19
Optional N or P Si 0.1-0.2 um 1-30 ohms-cm
Optional BOX 2 um or etch stop layer
Si Substrate
3630

FIG. 36

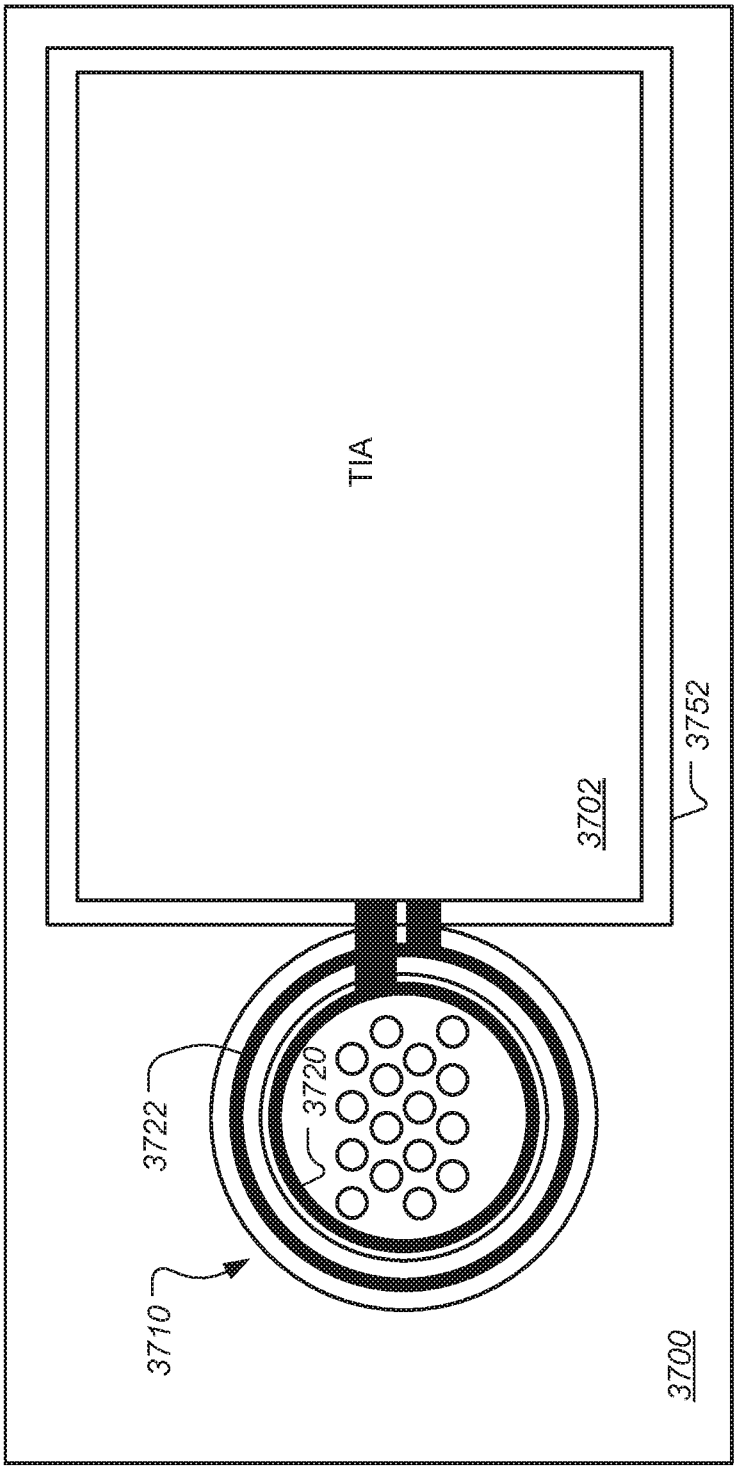


FIG. 37

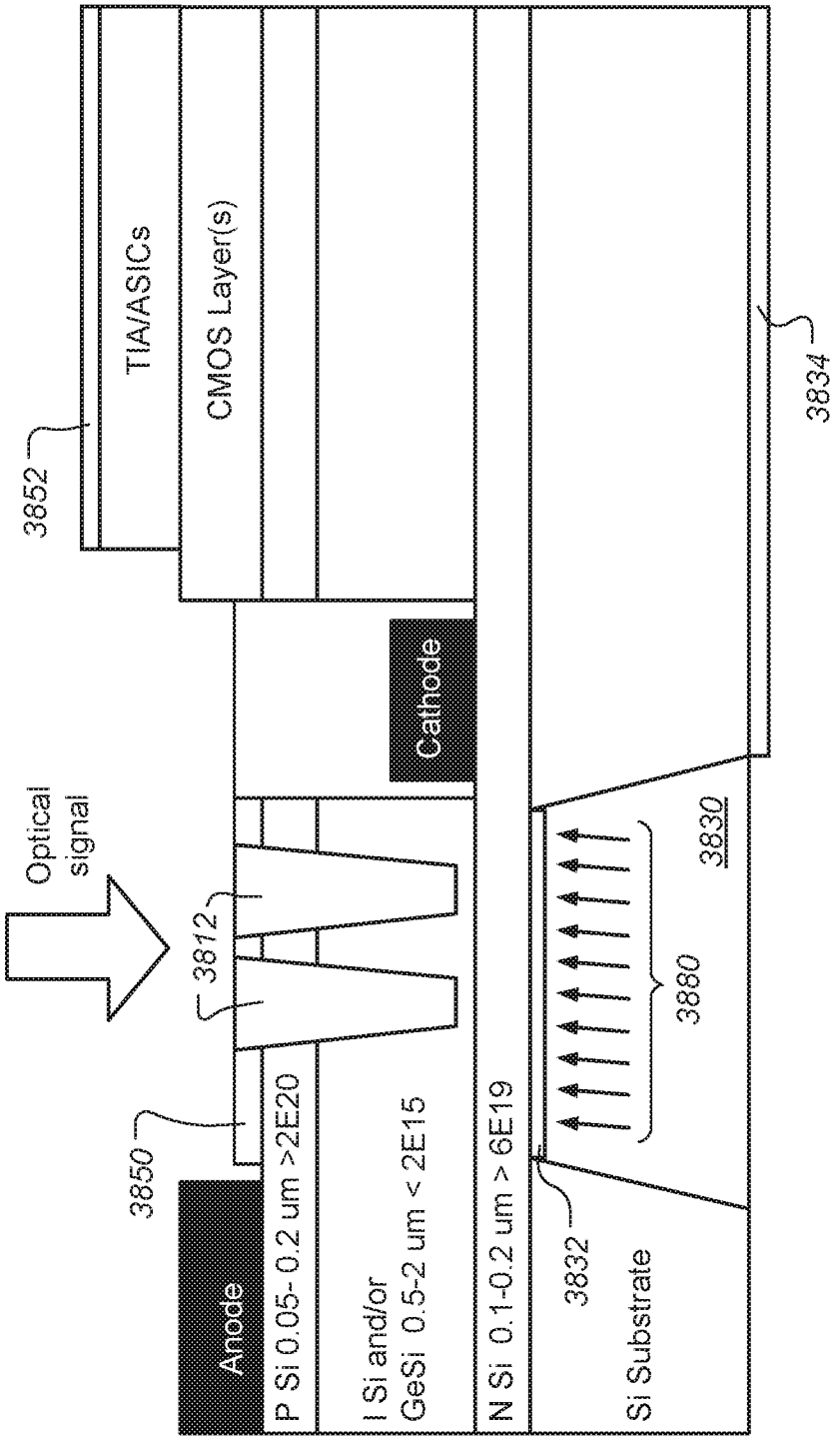

TIA/ASICs
CMOS Layer(s)
3852
3834
Optical signal
3812
Cathode
3850
Anode
P Si 0.05- 0.2 um >2E20
I Si and/or
GeSi 0.5-2 um < 2E15
N Si 0.1-0.2 um > 6E19
3880
3830
3832
Si Substrate

FIG. 38

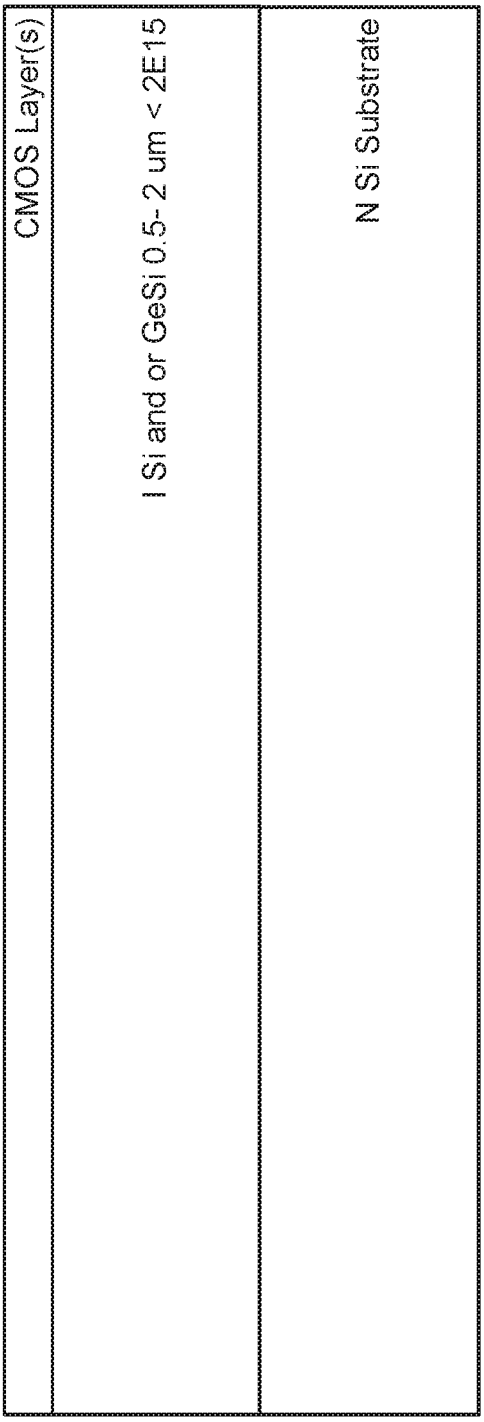


FIG. 39

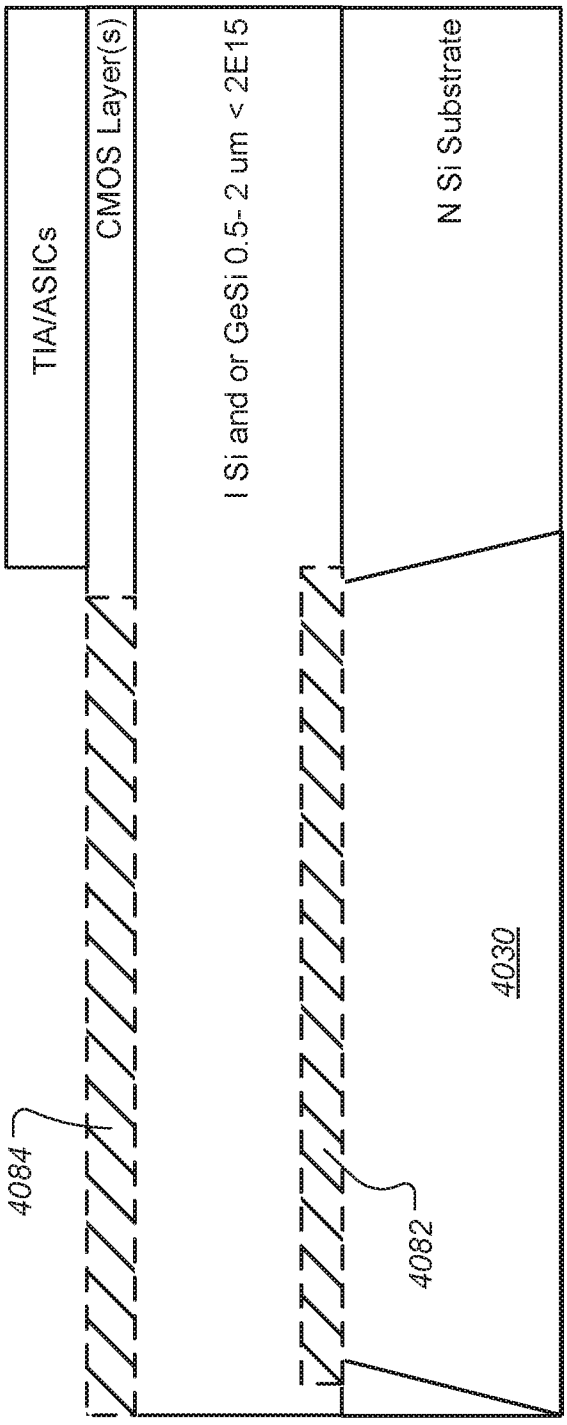

TIA/ASICs
CMOS Layer(s)
I Si and or GeSi 0.5- 2 um < 2E15
N Si Substrate
4084
4082
4030

FIG. 40

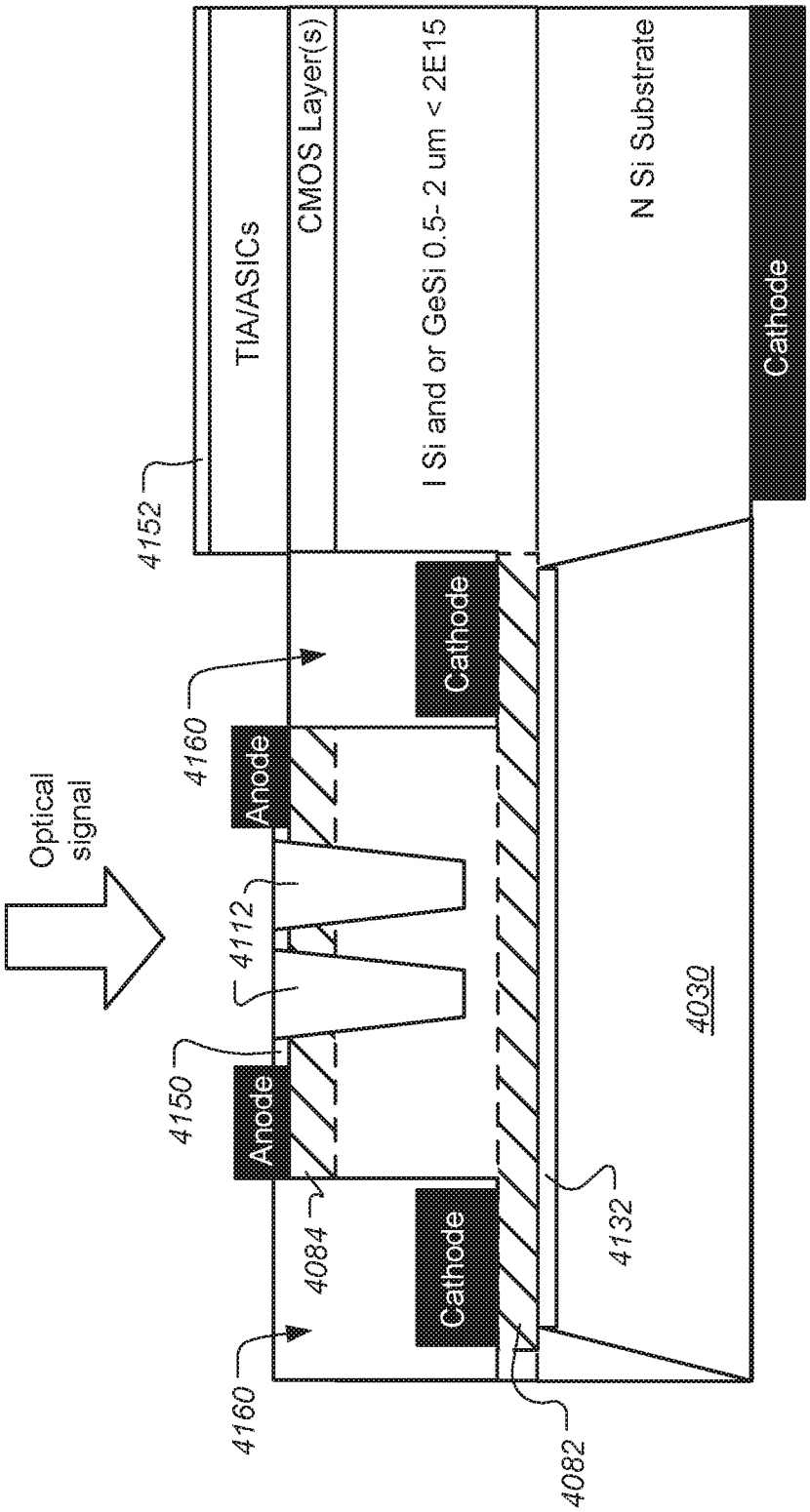

TIA/ASICs
CMOS Layer(s)
I Si and or GeSi 0.5- 2 um < 2E15
N Si Substrate
Cathode
4152
4160
Anode
Cathode
Optical signal
4112
4150
Anode
4084
Cathode
4132
4030
4160
4082

FIG. 41

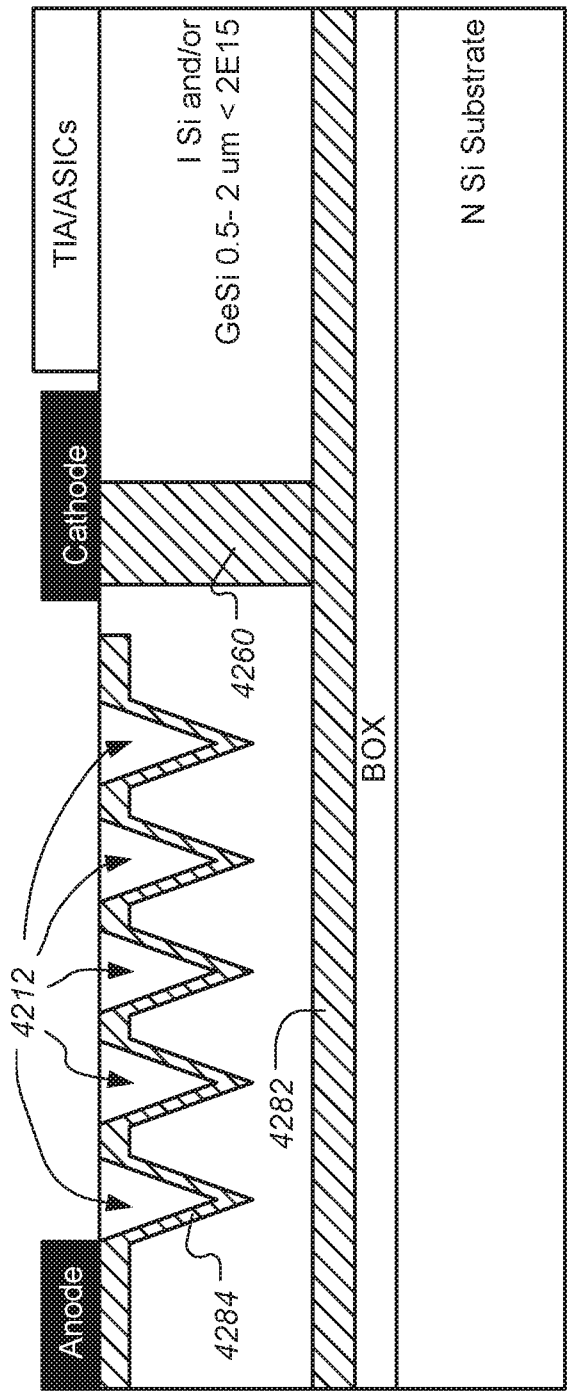

TIA/ASICs
I Si and/or
GeSi 0.5- 2 um < 2E15
N Si Substrate
Cathode
Anode
BOX
4260
4212
4282
4284

FIG. 42

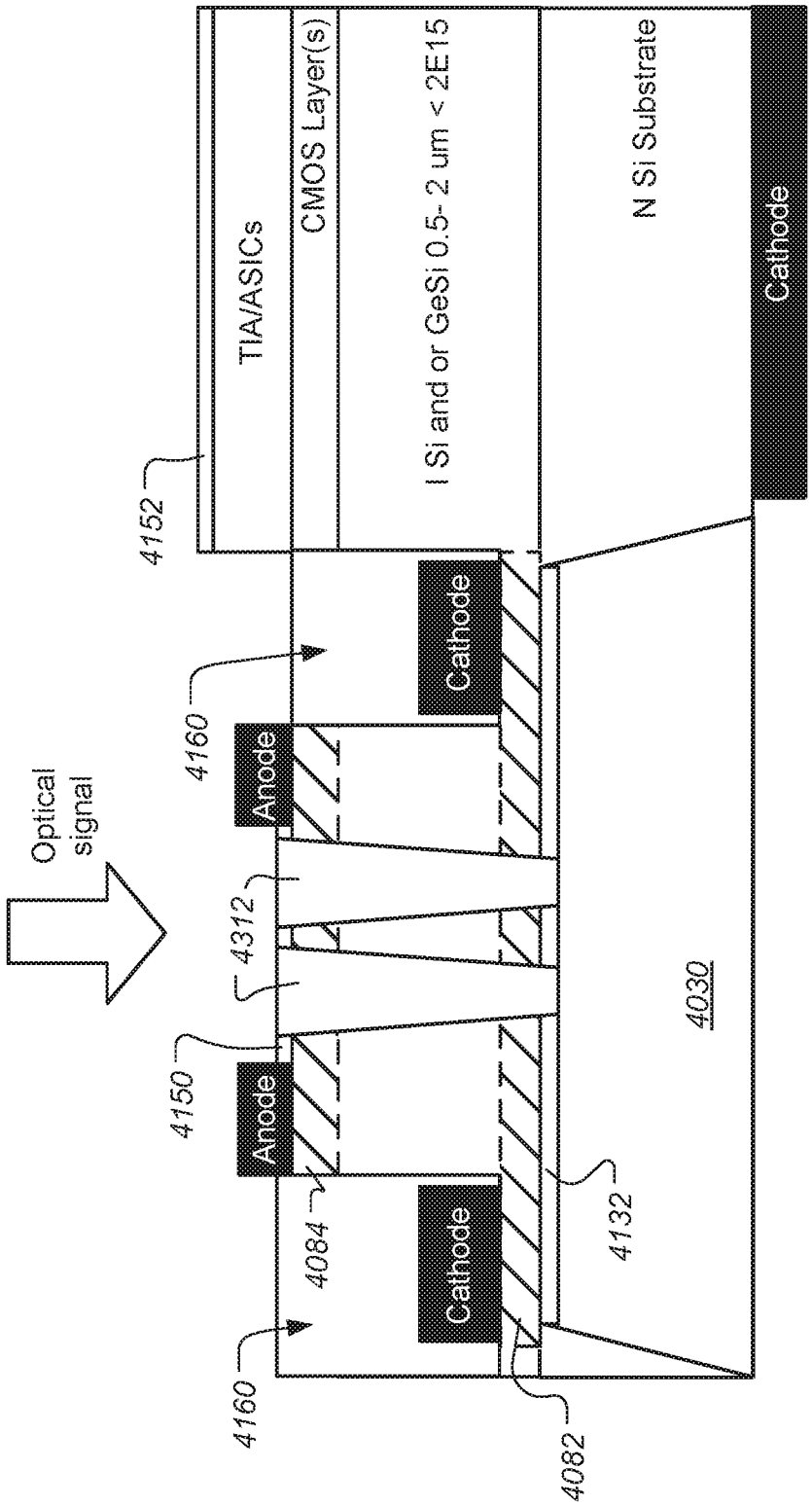

TIA/ASICs
CMOS Layer(s)
I Si and or GeSi 0.5- 2 um < 2E15
N Si Substrate
Cathode
4152
4160
Anode
Cathode
Optical signal
4312
4150
Anode
4084
Cathode
4132
4030
4160
4082

FIG. 43

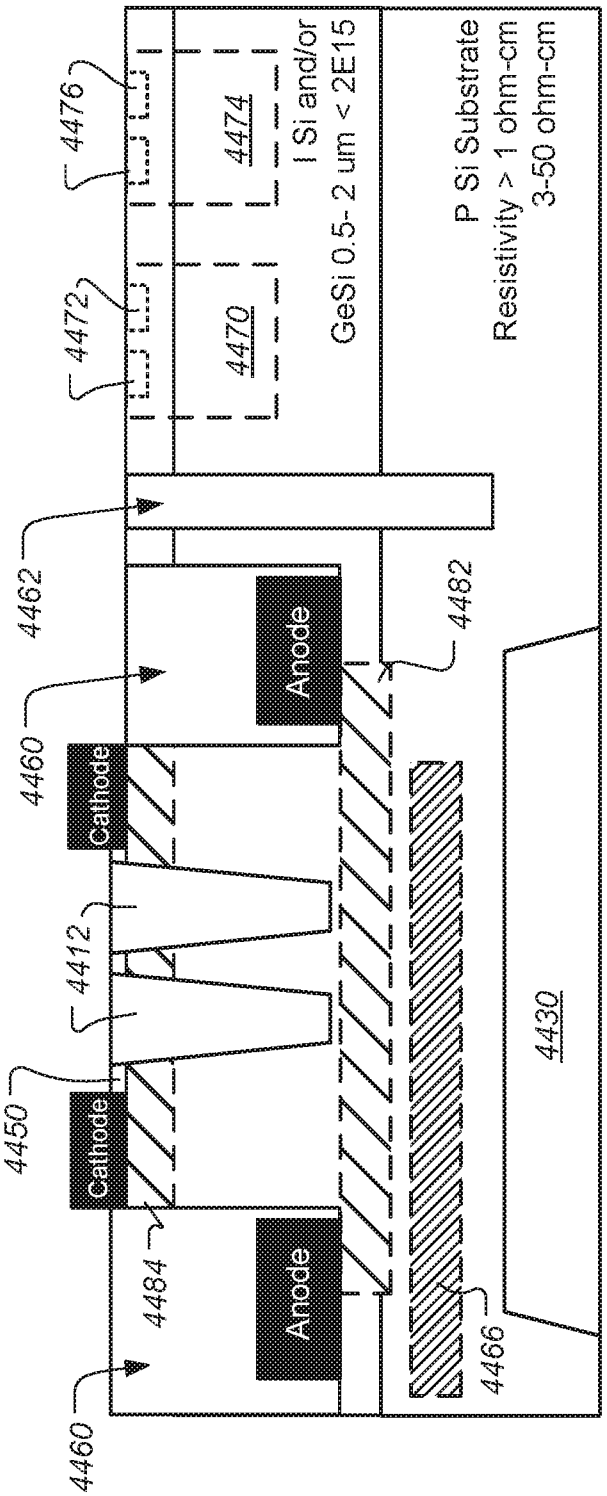

4476
4474
I Si and/or
GeSi 0.5- 2 um < 2E15
4472
4470
P Si Substrate
Resistivity > 1 ohm-cm
3-50 ohm-cm
4462
4482
Anode
4460
Cathode
4412
4450
Cathode
4484
Anode
4430
4466
4460

FIG. 44A

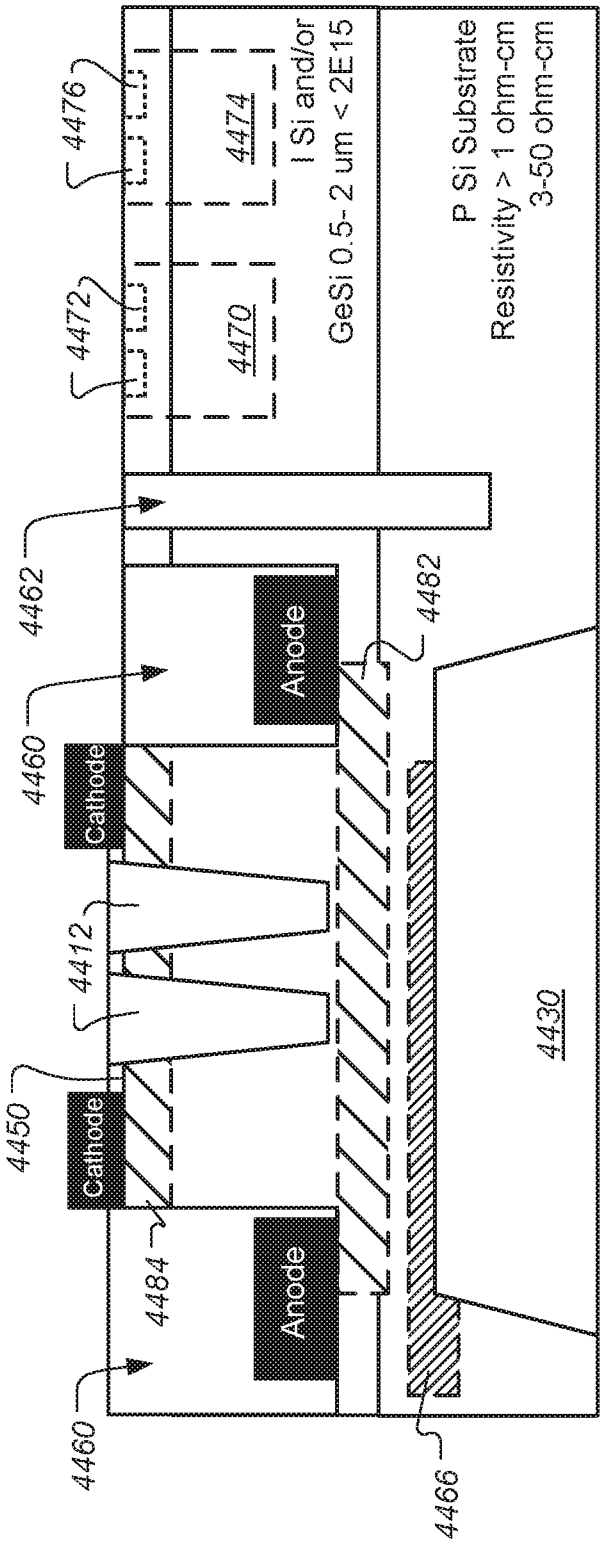

4476
4474
I Si and/or
GeSi 0.5- 2 um < 2E15
4472
4470
P Si Substrate
Resistivity > 1 ohm-cm
3-50 ohm-cm
4462
4482
Anode
4460
Cathode
4412
4430
4450
Cathode
4484
Anode
4460
4466

FIG. 44B

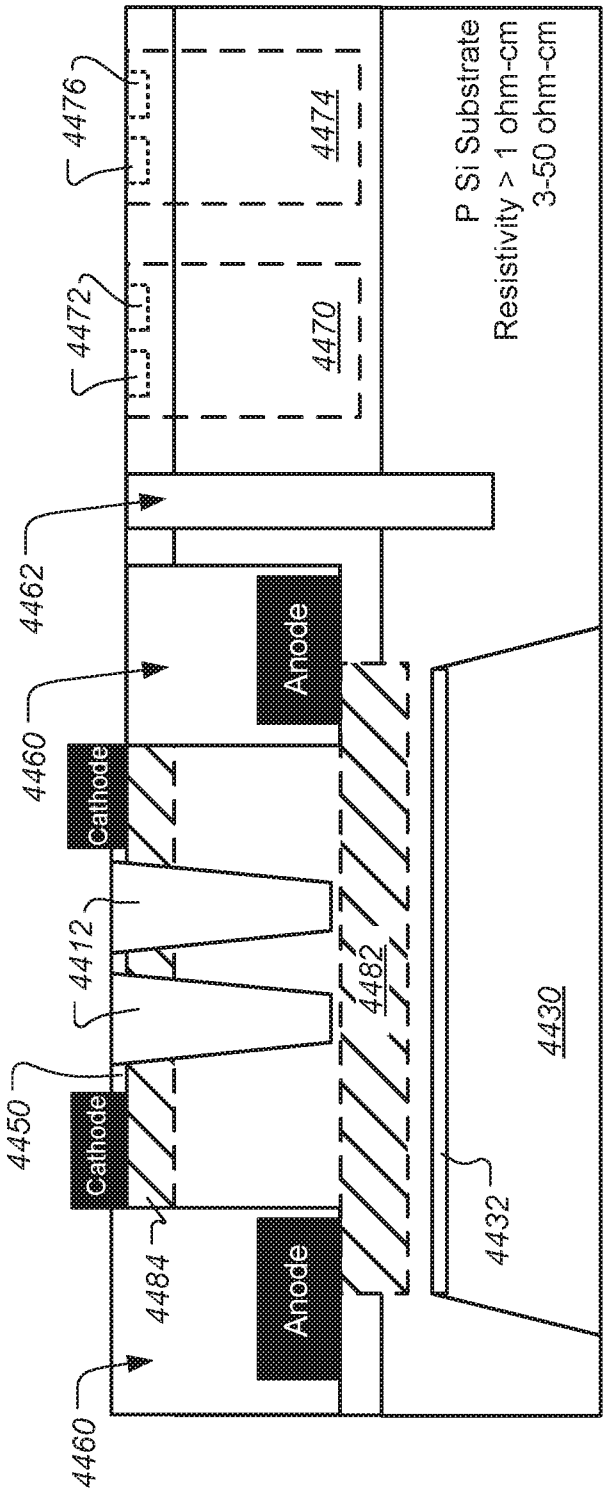

4476
4474
4472
4470
P Si Substrate
Resistivity > 1 ohm-cm
3-50 ohm-cm
4462
4460
Anode
Cathode
4412
4482
4450
Cathode
4430
4484
Anode
4432
4460

FIG. 44C

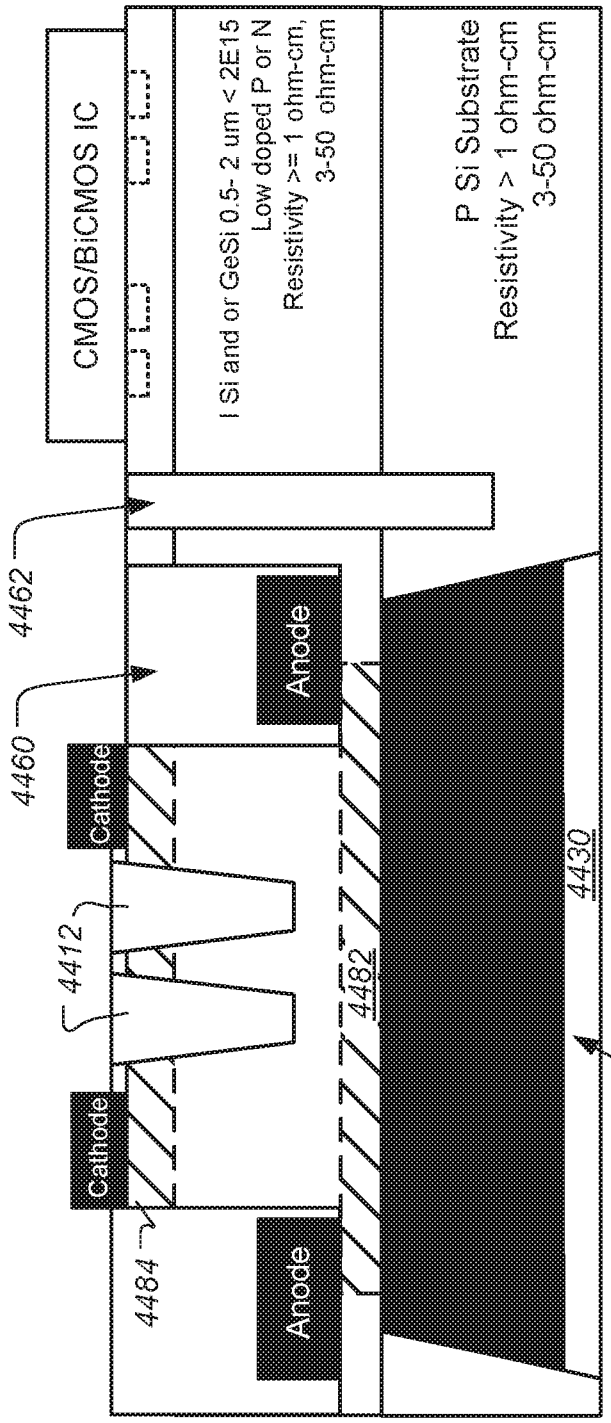

CMOS/BiCMOS IC
I Si and or GeSi 0.5- 2 um < 2E15
Low doped P or N
Resistivity >= 1 ohm-cm,
3-50 ohm-cm
P Si Substrate
Resistivity > 1 ohm-cm
3-50 ohm-cm
4462
4460
Anode
Cathode
4412
4482
4430
Cathode
4484
Anode
4532

FIG. 45

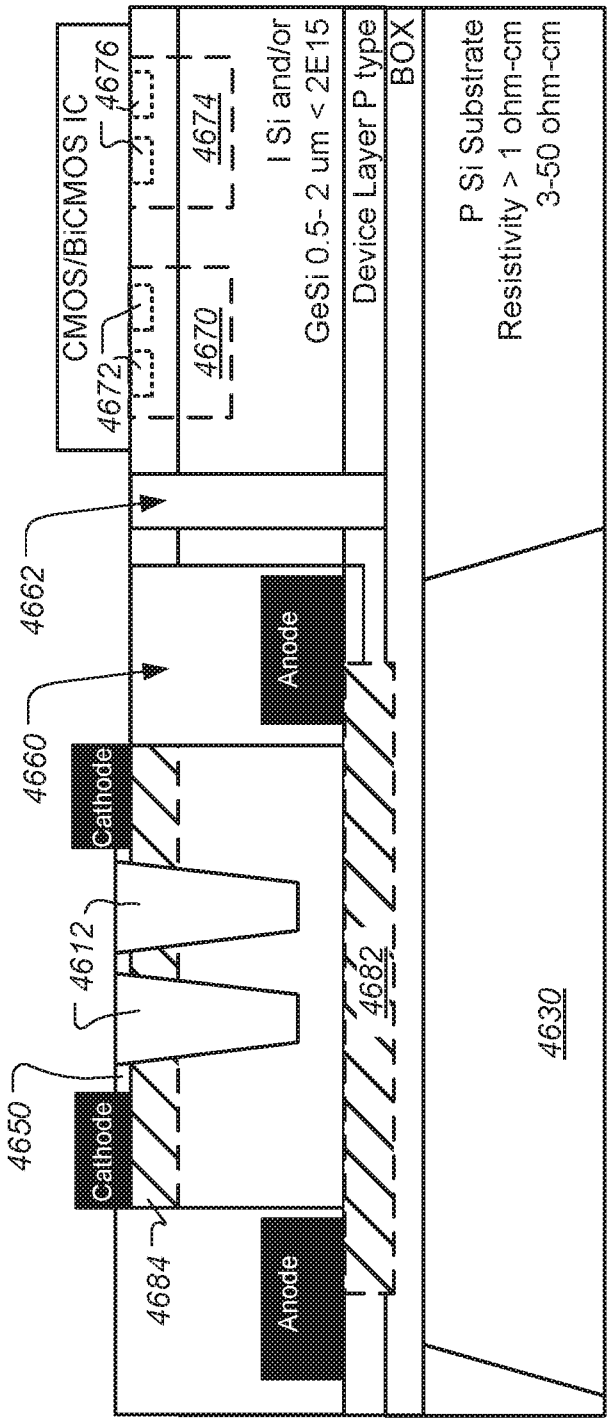

CMOS/BiCMOS IC
4676
4674
4672
4670
I Si and/or
GeSi 0.5- 2 um < 2E15
Device Layer P type
BOX
P Si Substrate
Resistivity > 1 ohm-cm
3-50 ohm-cm
4662
4660
4612
4650
4684
Anode
Cathode
Cathode
Anode
4682
4630

FIG. 46

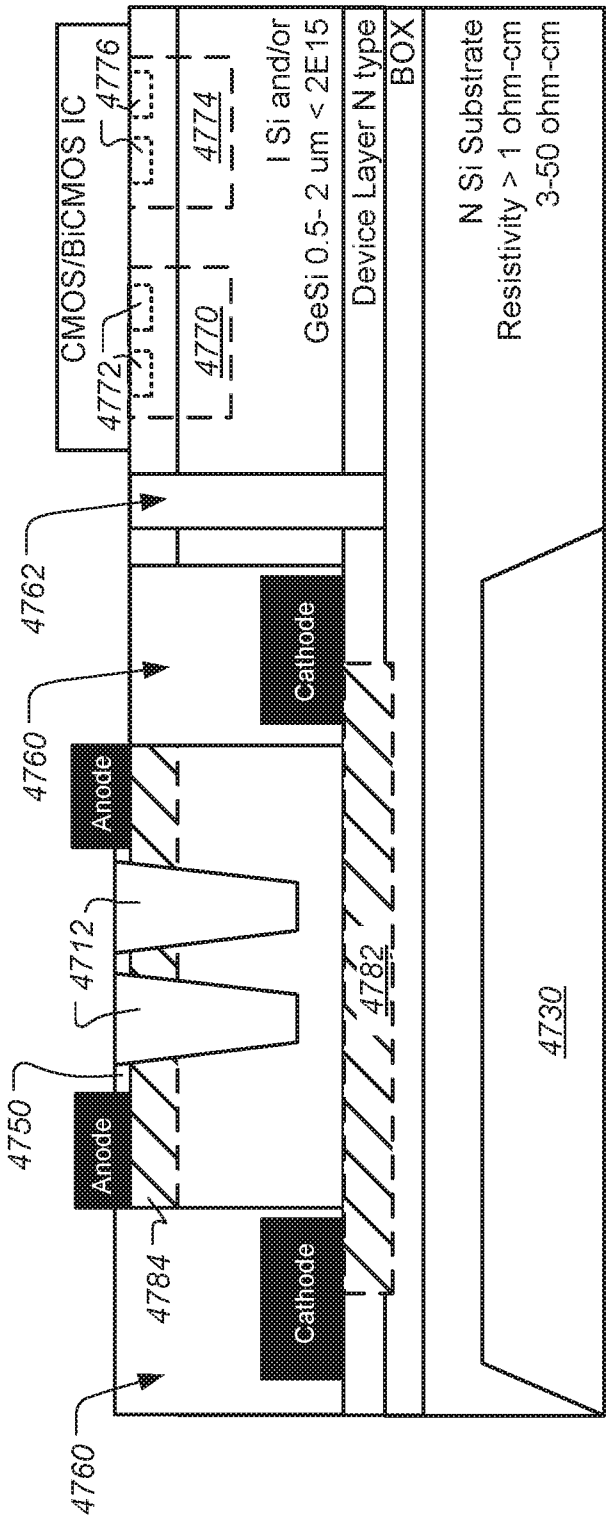

CMOS/BiCMOS IC
4776
4774
I Si and/or
GeSi 0.5- 2 um < 2E15
4770
4772
Device Layer N type
BOX
N Si Substrate
Resistivity > 1 ohm-cm
3-50 ohm-cm
4762
4760
Anode
Cathode
4712
4782
4730
4750
Anode
Cathode
4784
4760

FIG. 47

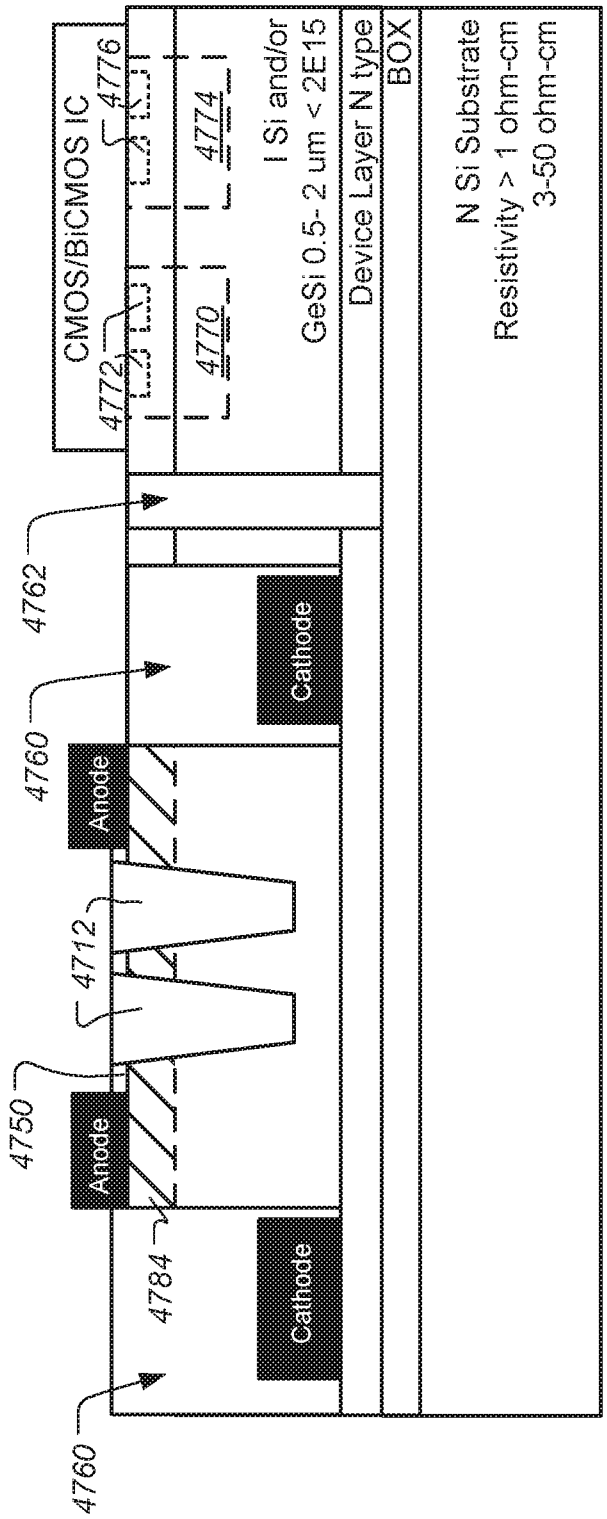

CMOS/BiCMOS IC
4776
4774
4772
4770
I Si and/or
GeSi 0.5- 2 um < 2E15
Device Layer N type
BOX
N Si Substrate
Resistivity > 1 ohm-cm
3-50 ohm-cm
4762
4760
Anode
Cathode
4712
4750
Anode
Cathode
4784
4760

FIG. 48

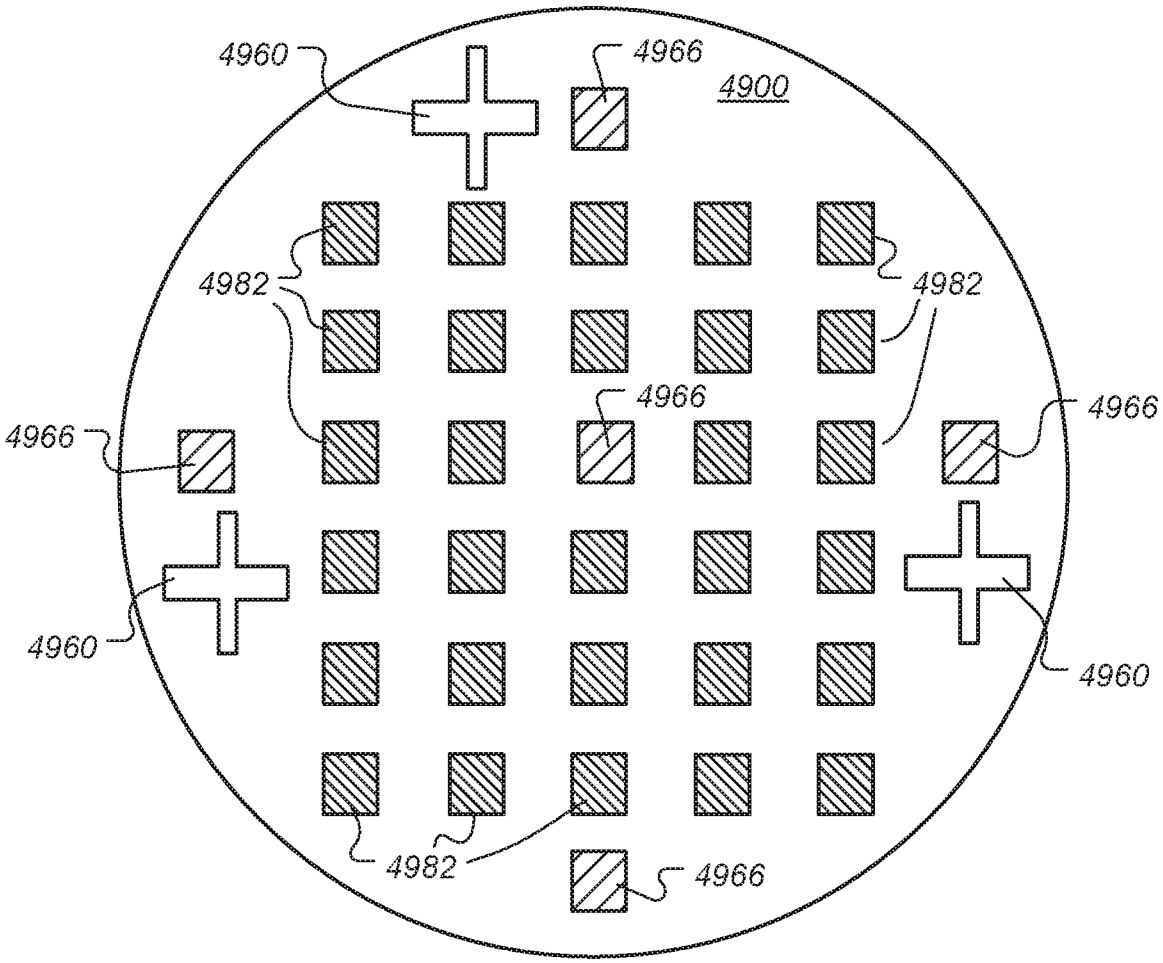


FIG. 49

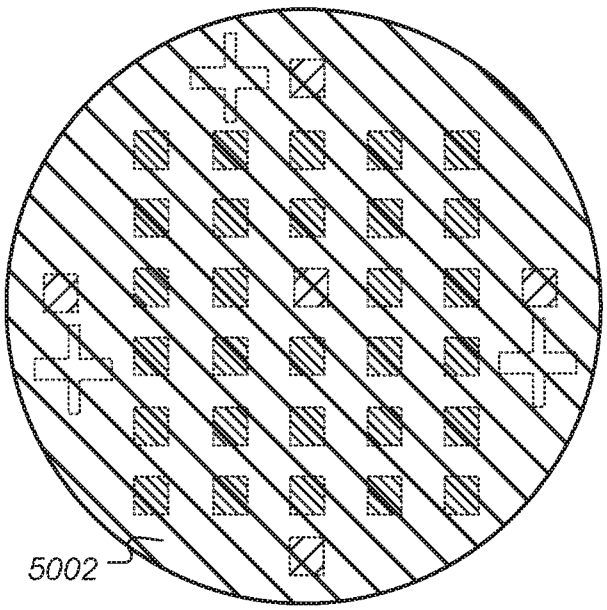


FIG. 50A

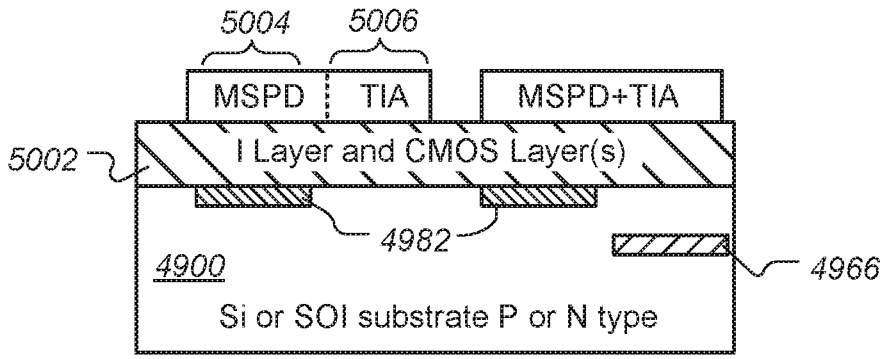


FIG. 50B

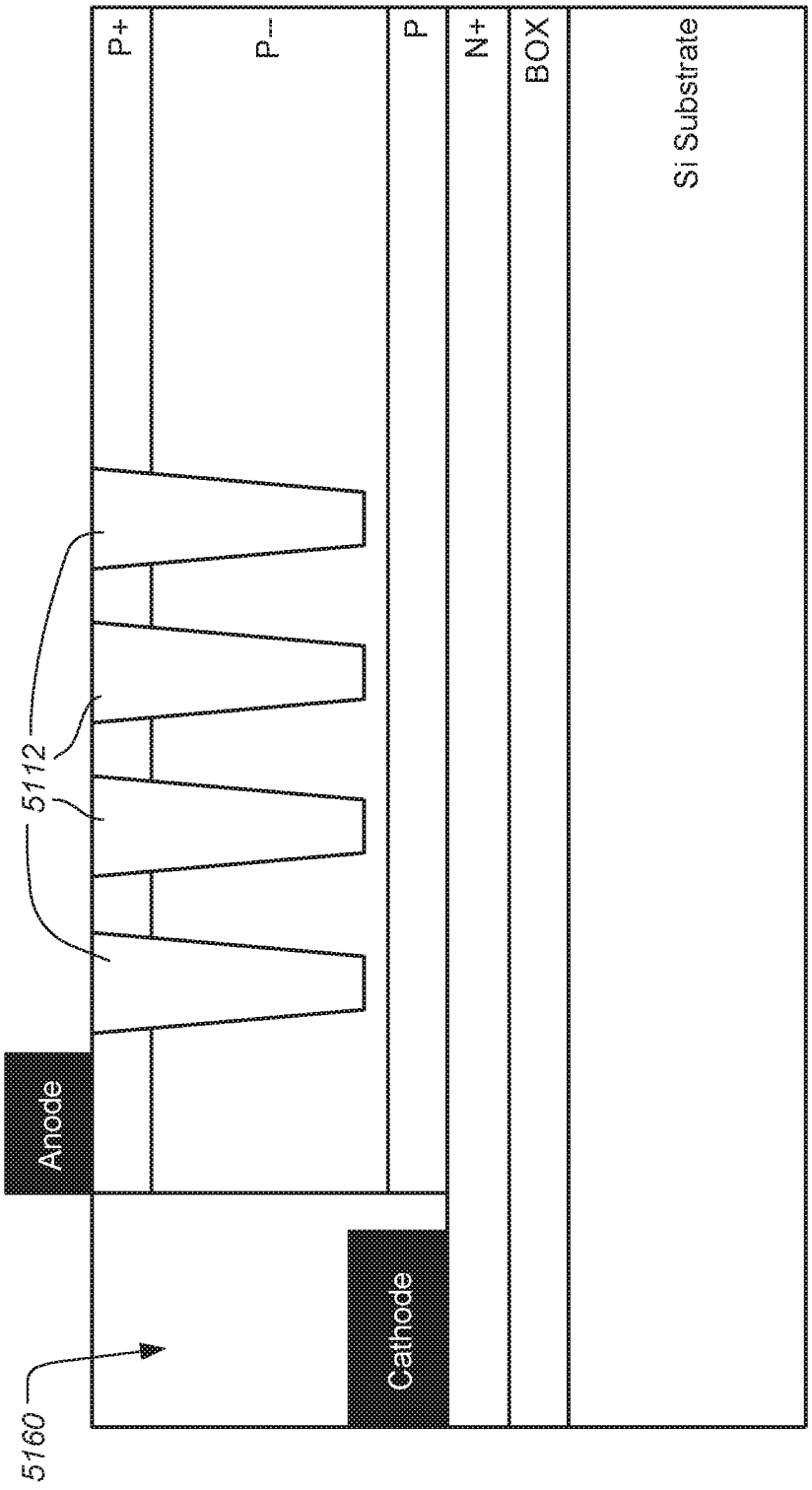


FIG. 51

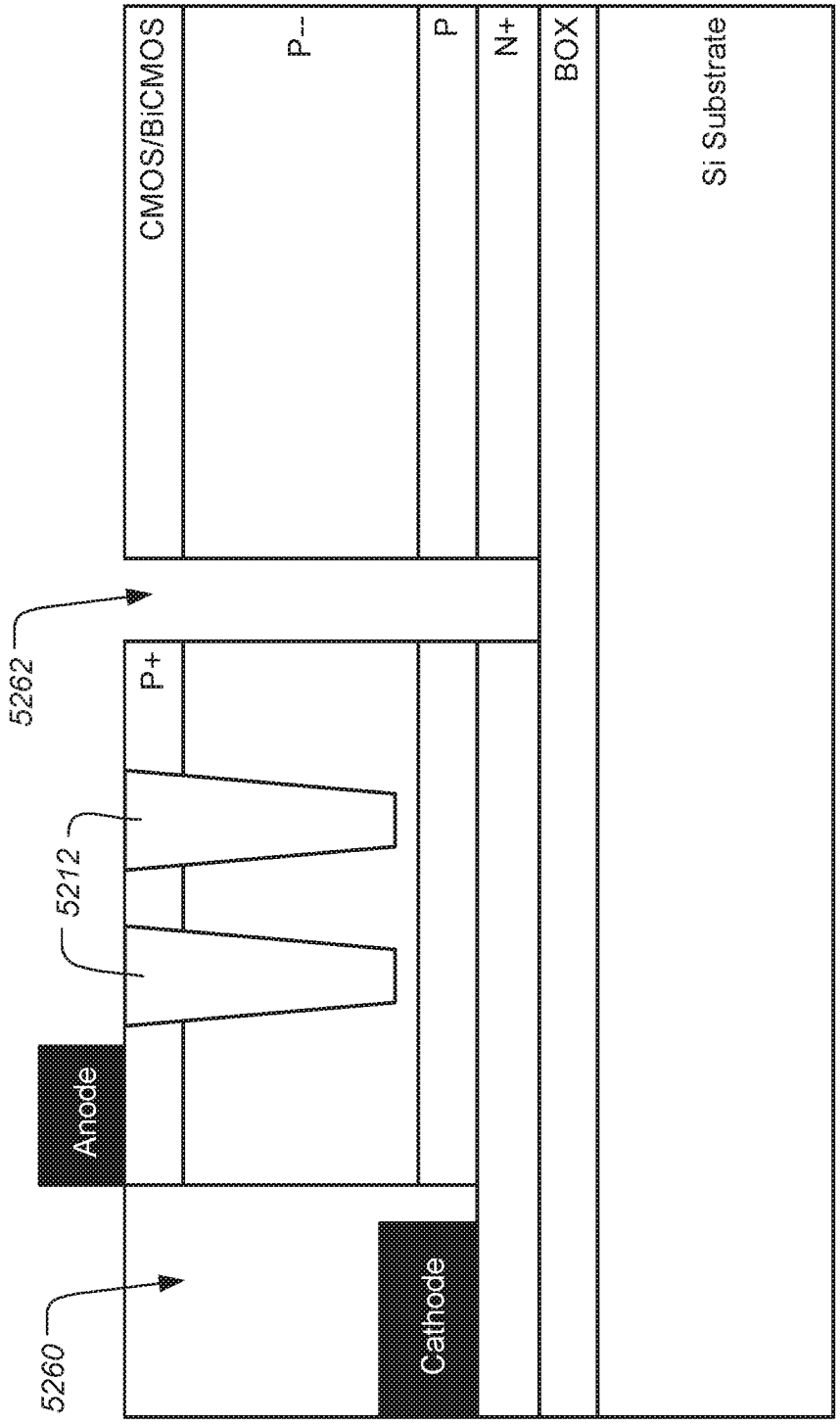

CMOS/BiCMOS
P--
P
N+
BOX
Si Substrate
P+
5262
5212
Anode
Cathode
5260

FIG. 52

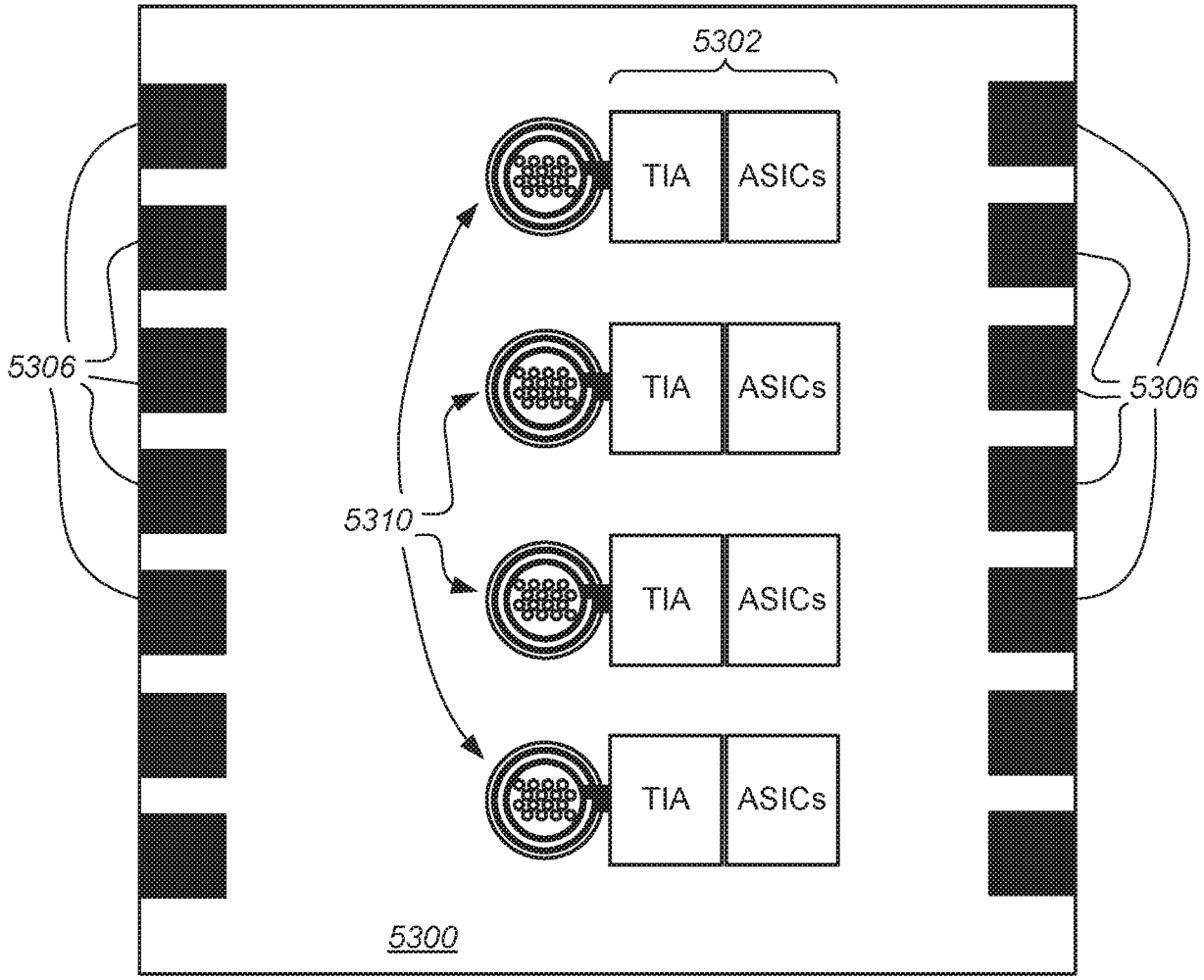

5302
TIA
ASICs
TIA
ASICs
TIA
ASICs
TIA
ASICs
5306
5306
5310
5300

FIG. 53

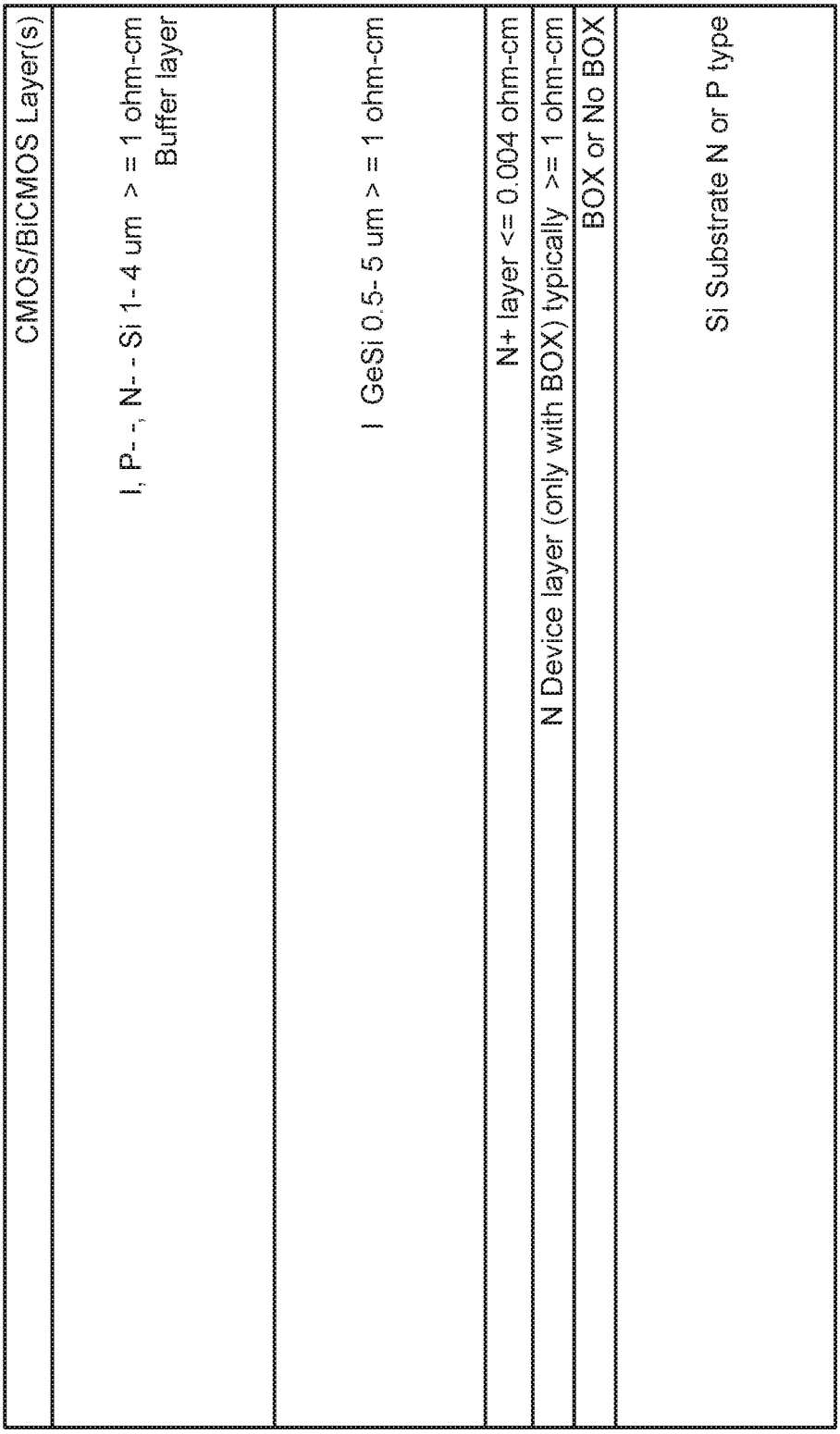

CMOS/BiCMOS Layer(s)
I, P- -, N- - Si 1- 4 um > = 1 ohm-cm
Buffer layer
I GeSi 0.5- 5 um > = 1 ohm-cm
N+ layer <= 0.004 ohm-cm
N Device layer (only with BOX) typically >= 1 ohm-cm
BOX or No BOX
Si Substrate N or P type

FIG. 54

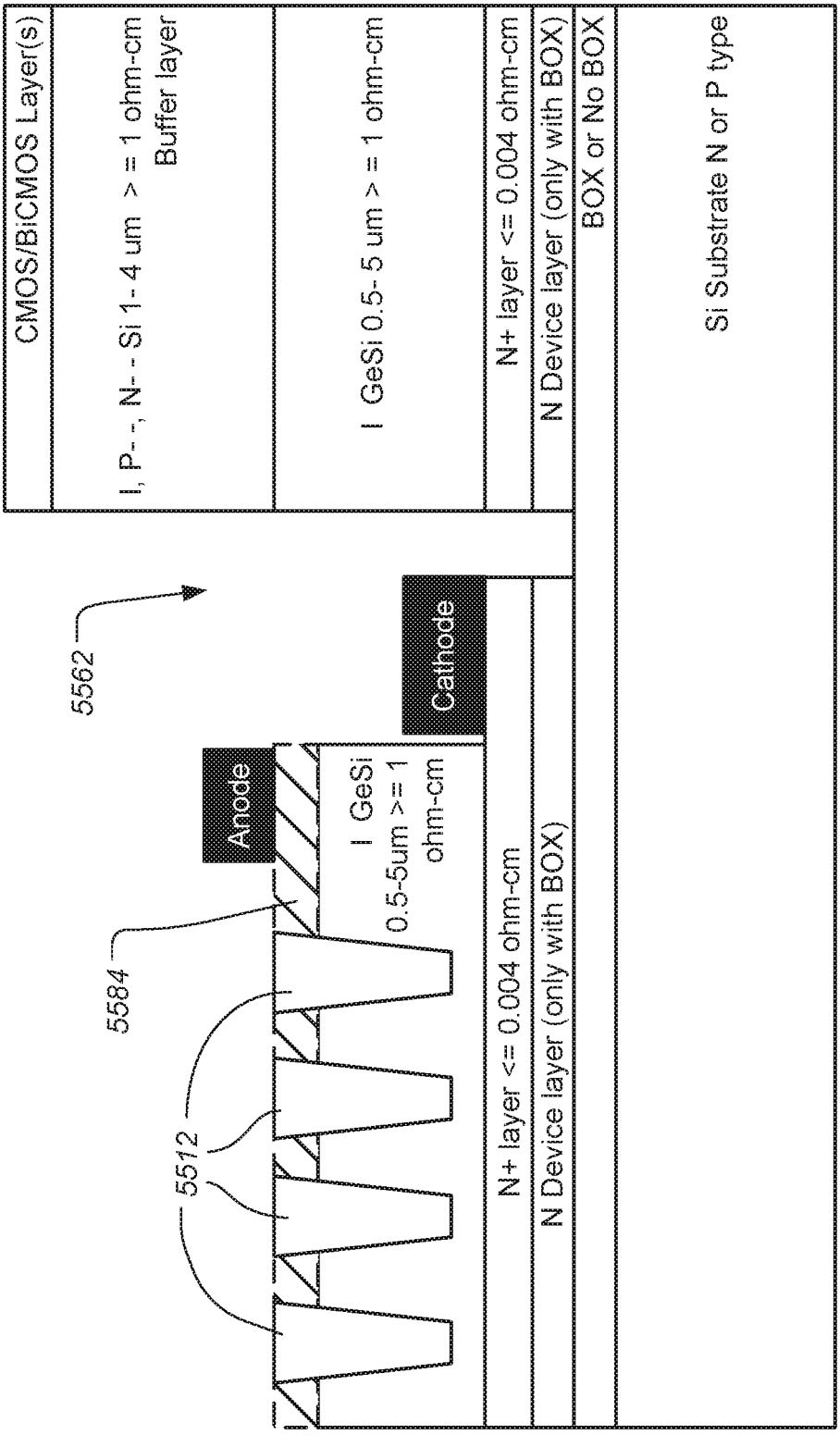

CMOS/BiCMOS Layer(s)
I, P- -, N- - Si 1- 4 um > = 1 ohm-cm
Buffer layer
I GeSi 0.5- 5 um > = 1 ohm-cm
N+ layer <= 0.004 ohm-cm
N Device layer (only with BOX)
BOX or No BOX
Si Substrate N or P type
5562
Cathode
Anode
I GeSi
0.5-5um > = 1
ohm-cm
5584
5512
N+ layer <= 0.004 ohm-cm
N Device layer (only with BOX)

FIG. 55

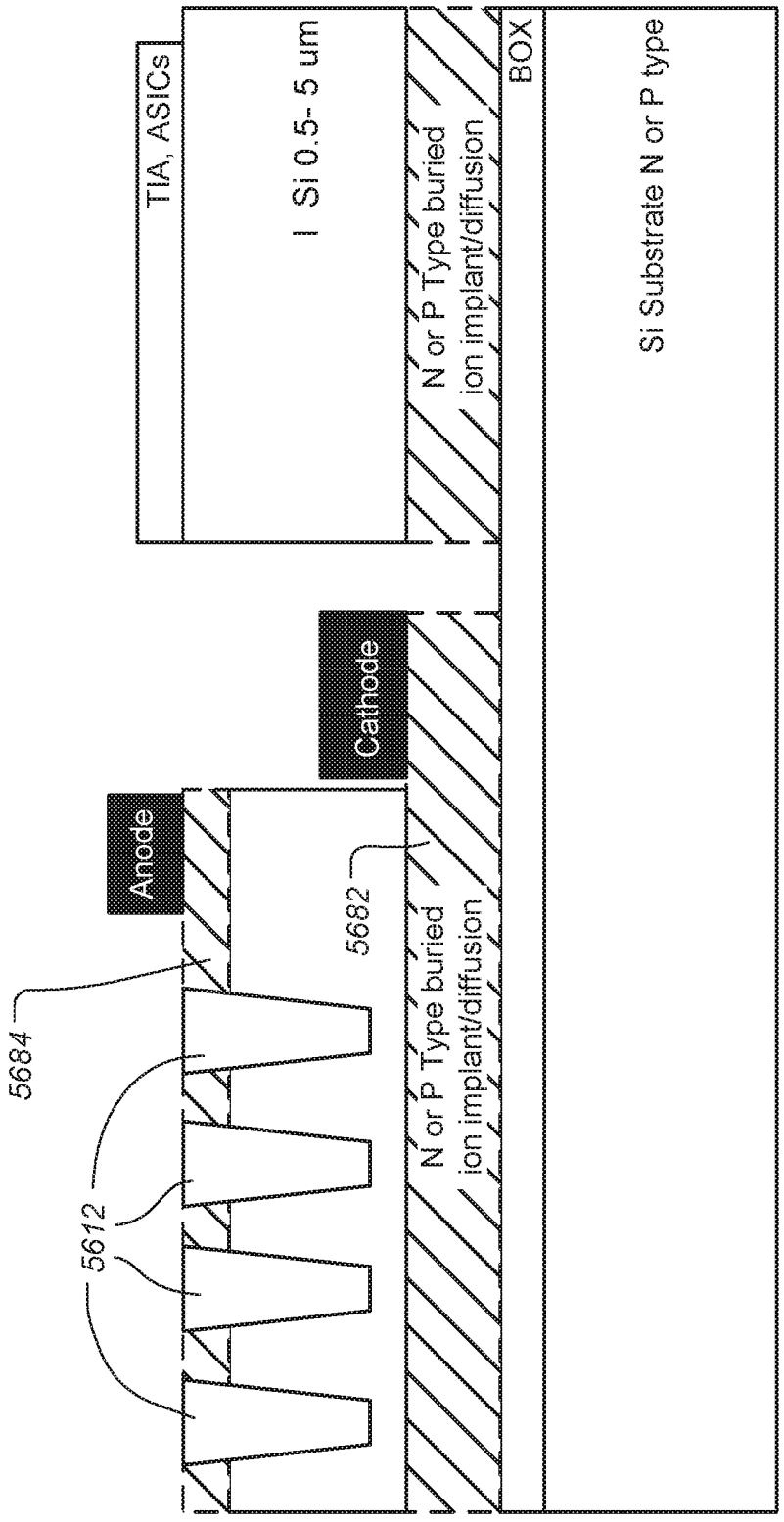

TIA, ASICs
I Si 0.5- 5 um
N or P Type buried ion implant/diffusion
BOX
Si Substrate N or P type
Cathode
Anode
5682
5684
5612
N or P Type buried ion implant/diffusion

FIG. 56

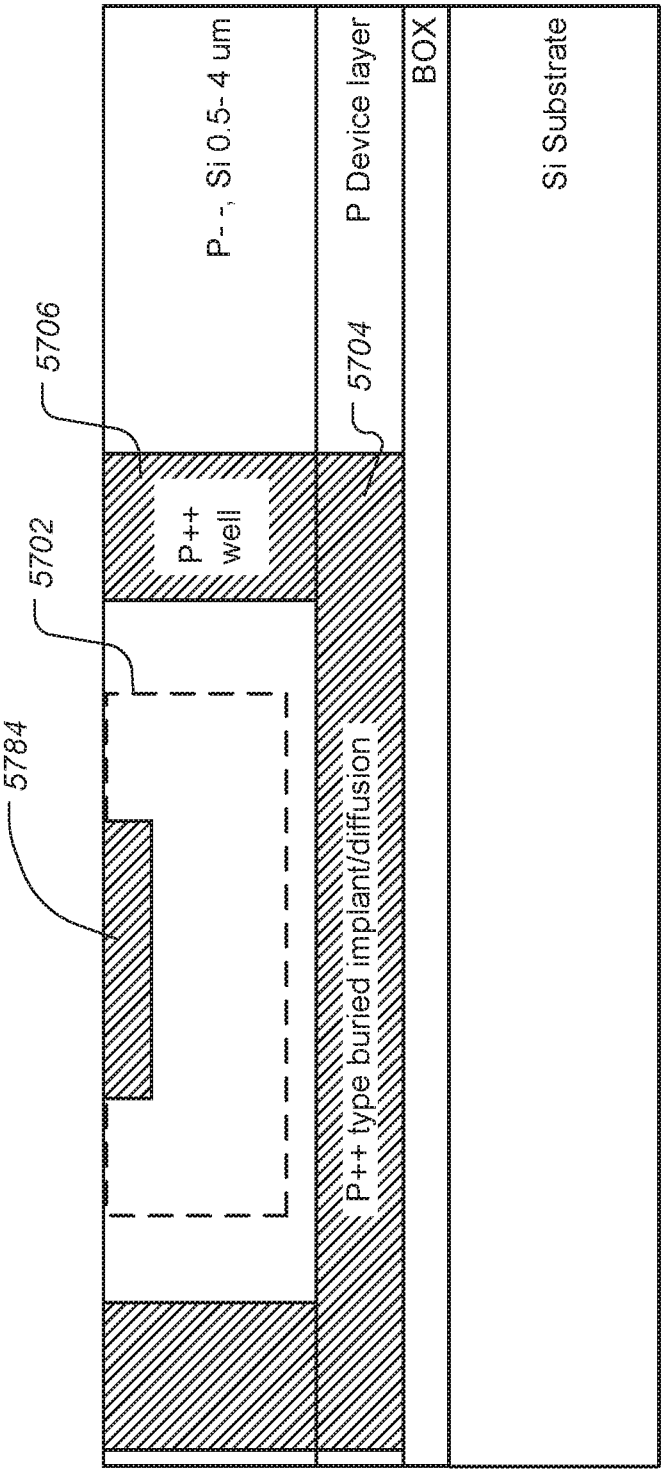

P- -, Si 0.5- 4 um
P Device layer
BOX
Si Substrate
5706
5704
5702
5784
P++
well
P++ type buried implant/diffusion

FIG. 57

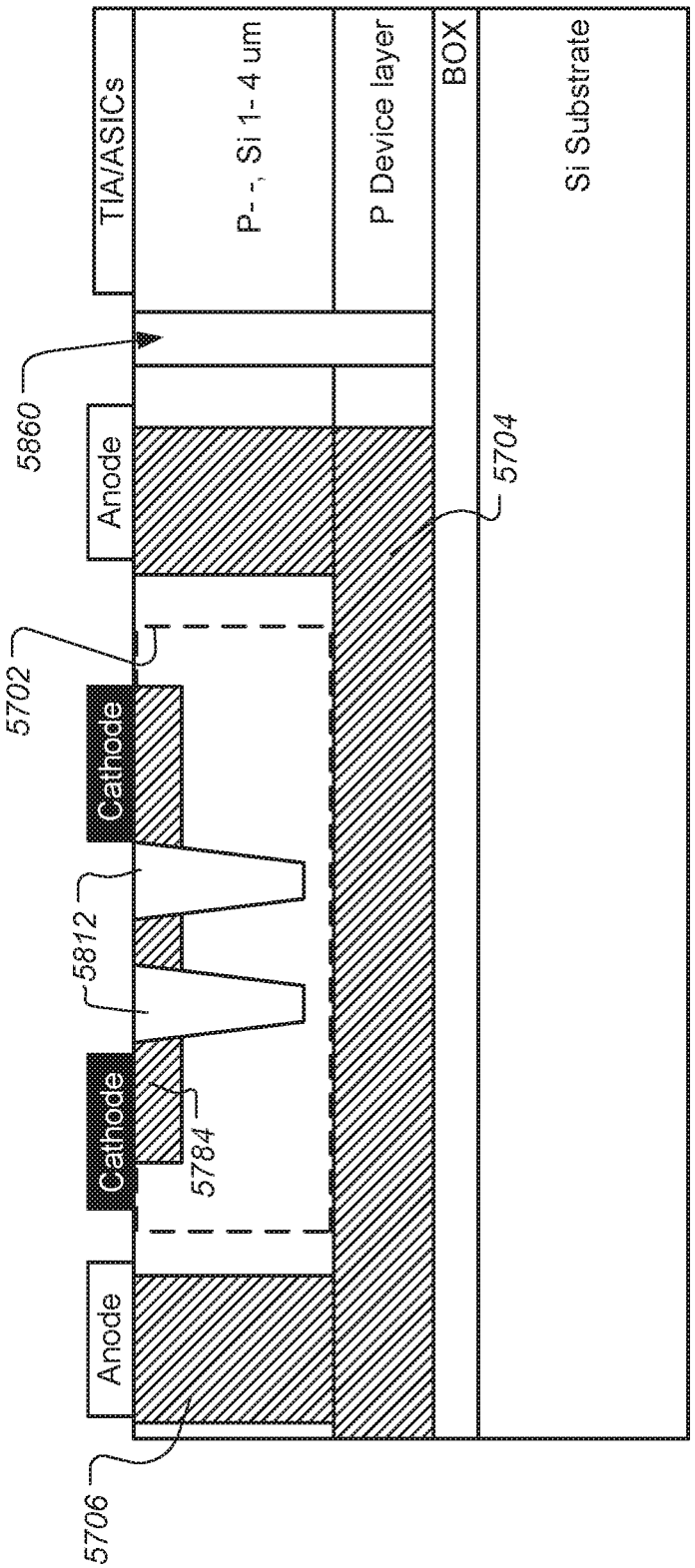

TIA/ASICs
P- -, Si 1- 4 um
P Device layer
BOX
Si Substrate
5860
Anode
5704
5702
Cathode
5812
Cathode
5784
Anode
5706

FIG. 58

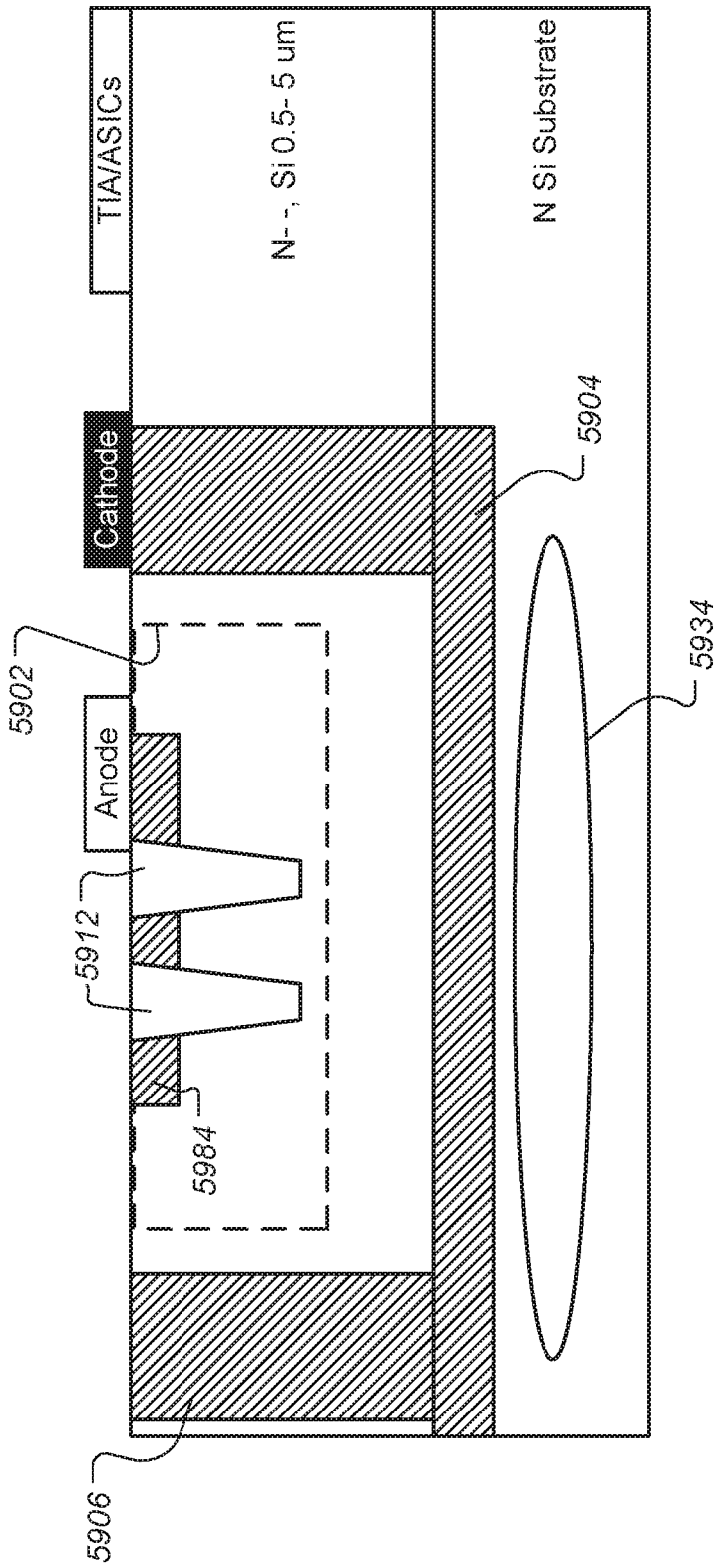

TIA/ASICs
N- -, Si 0.5- 5 um
N Si Substrate
Cathode
5904
5902
Anode
5912
5984
5934
5906

FIG. 59A

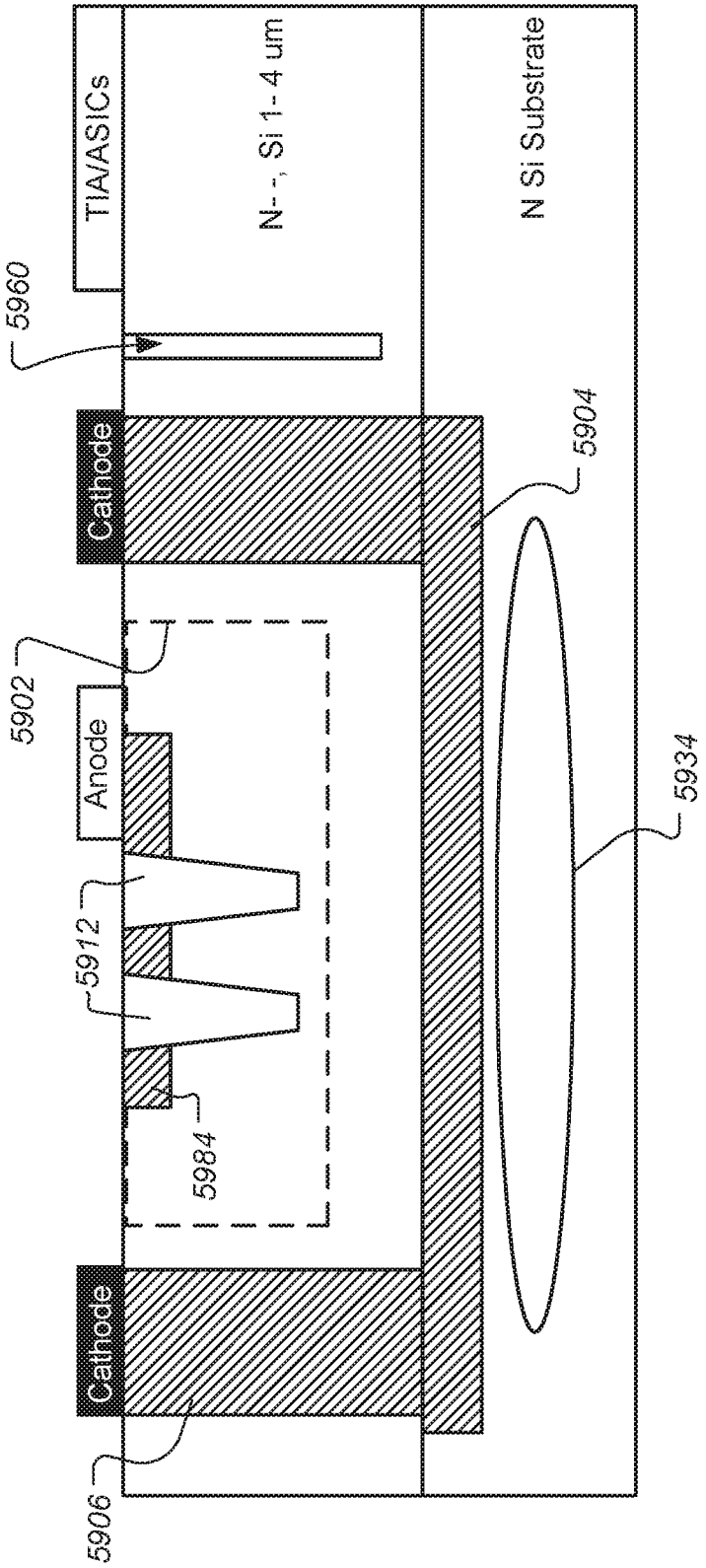

TIA/ASICs
N- -, Si 1- 4 um
N Si Substrate
5960
Cathode
5904
5902
Anode
5912
5984
5934
Cathode
5906

FIG. 59B

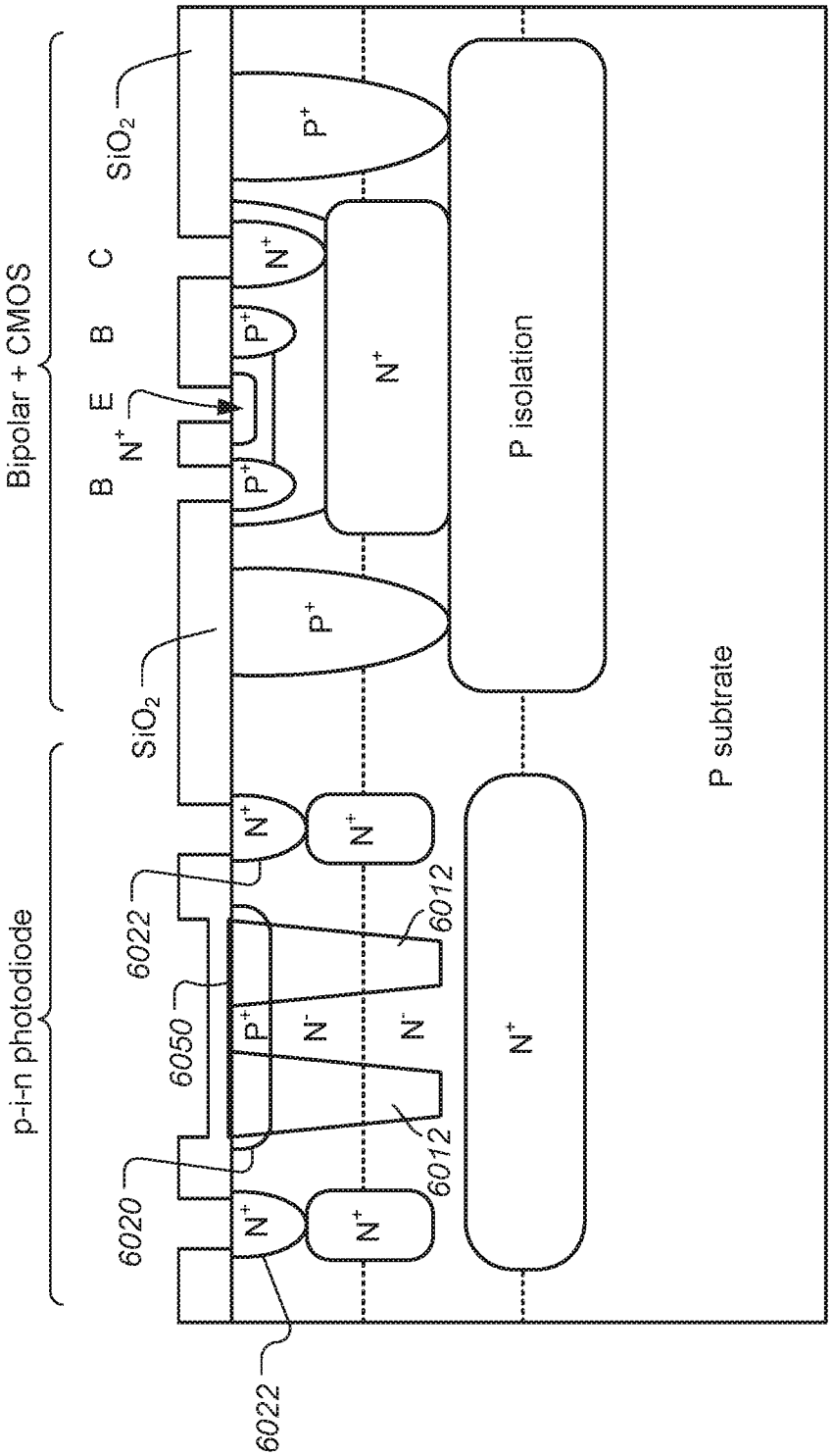

Bipolar + CMOS
p-i-n photodiode
SiO2
SiO2
B
E
B
C
B
N+
P+
N+
P+
P+
N+
P+
N+
N+
N+
N+
N+
P isolation
P subtrate
6022
6050
6020
6022
6012
6012
N-
N-

FIG. 60

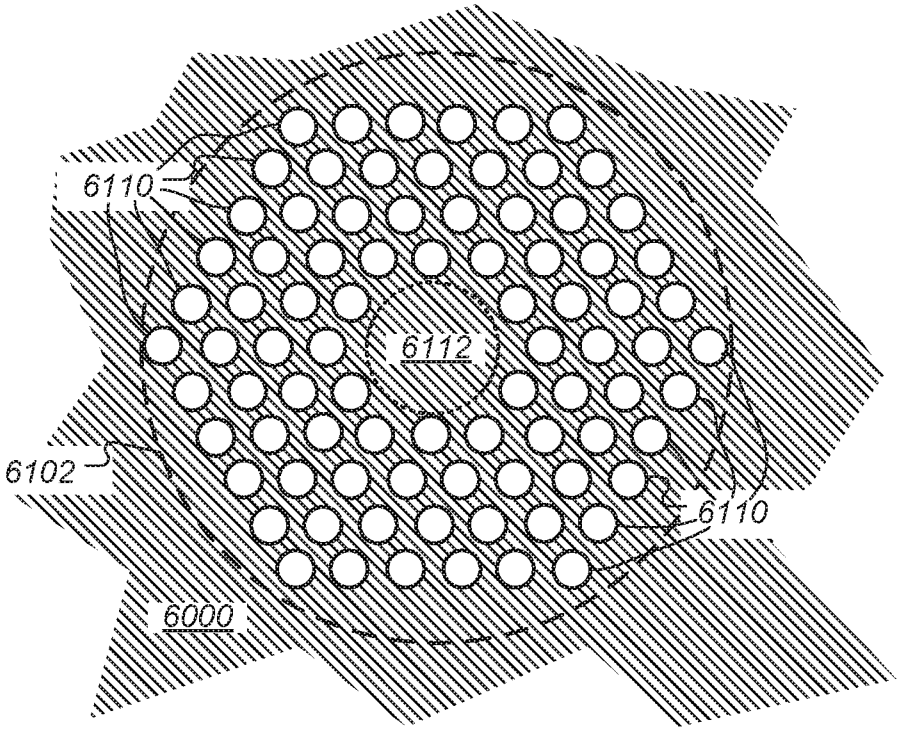


FIG. 61A

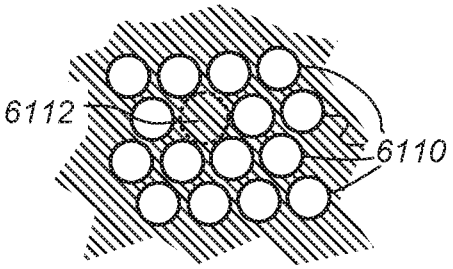


FIG. 61B

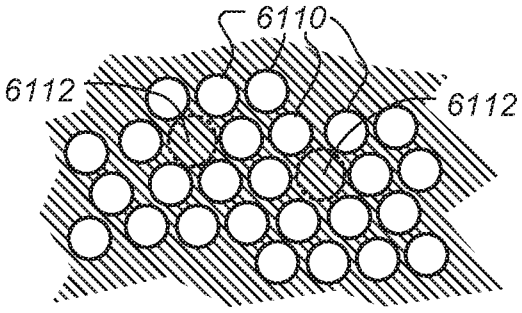


FIG. 61C

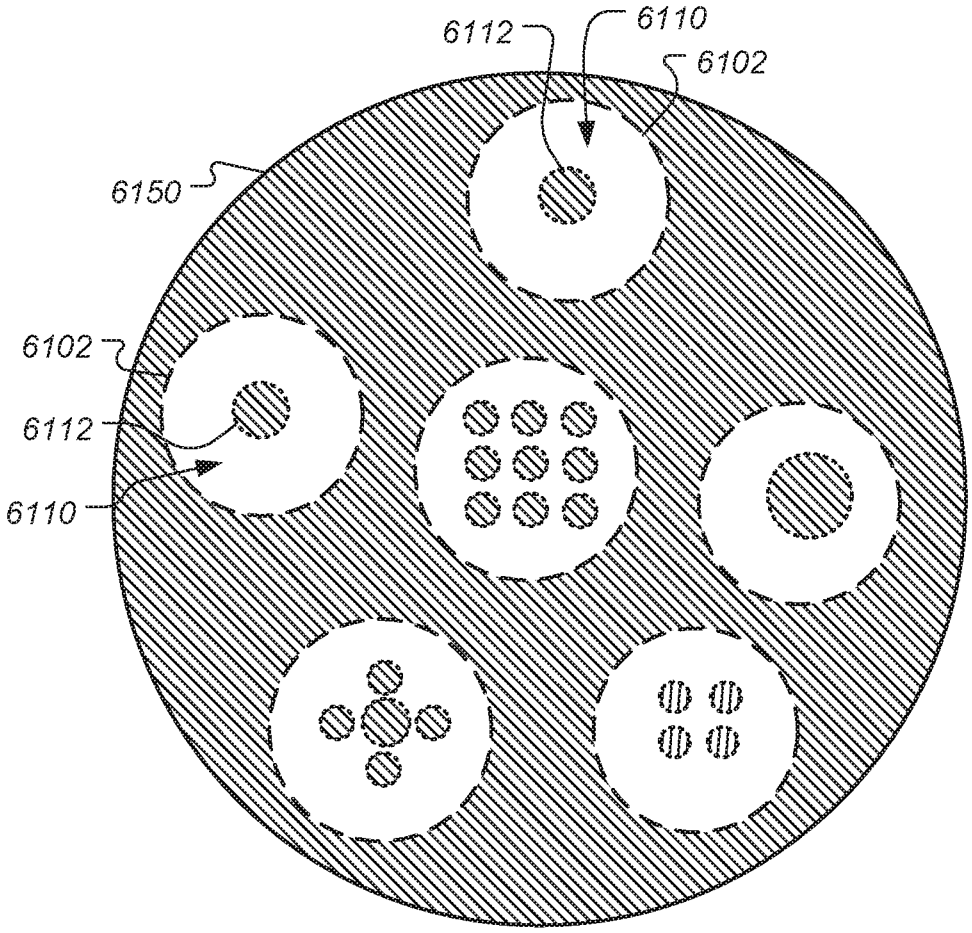


FIG. 61D

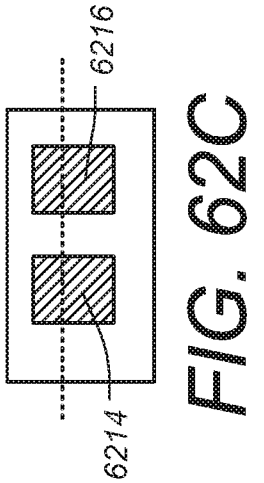


FIG. 62C

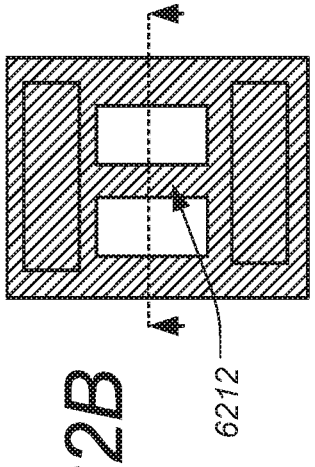


FIG. 62B

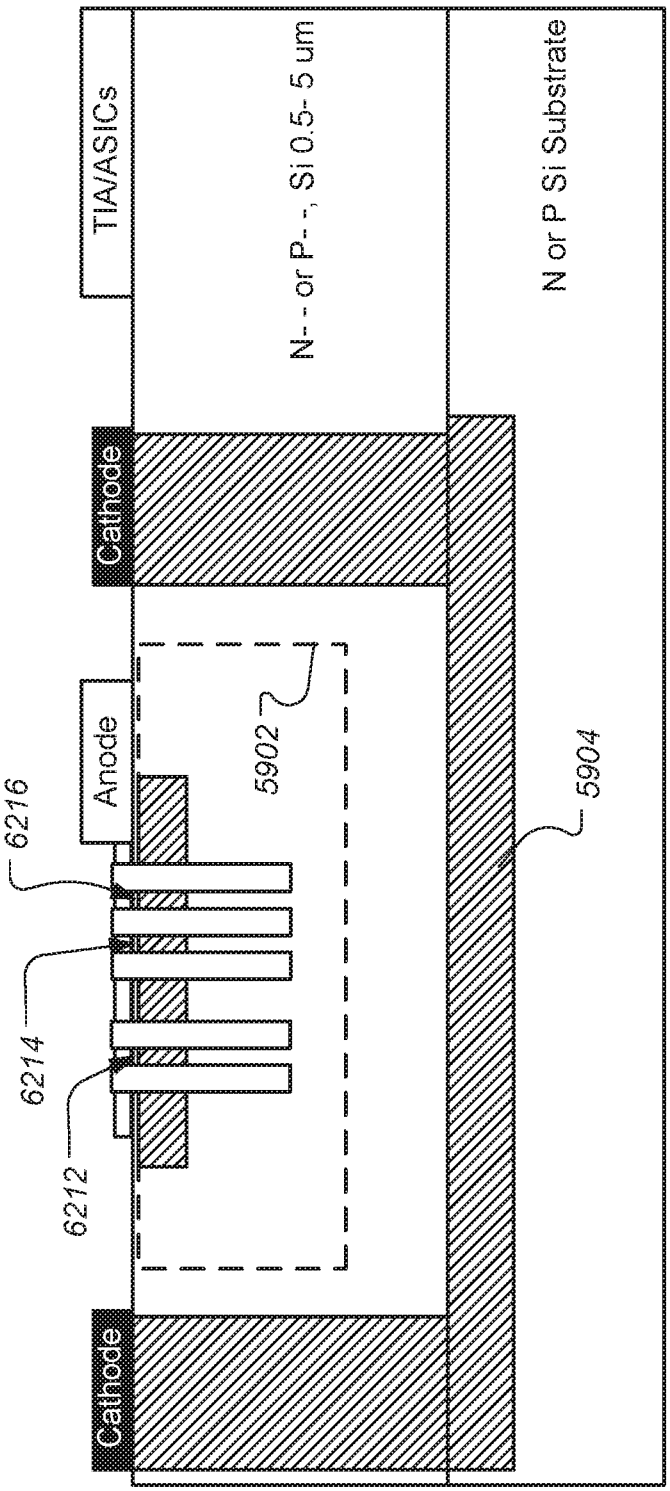


FIG. 62A

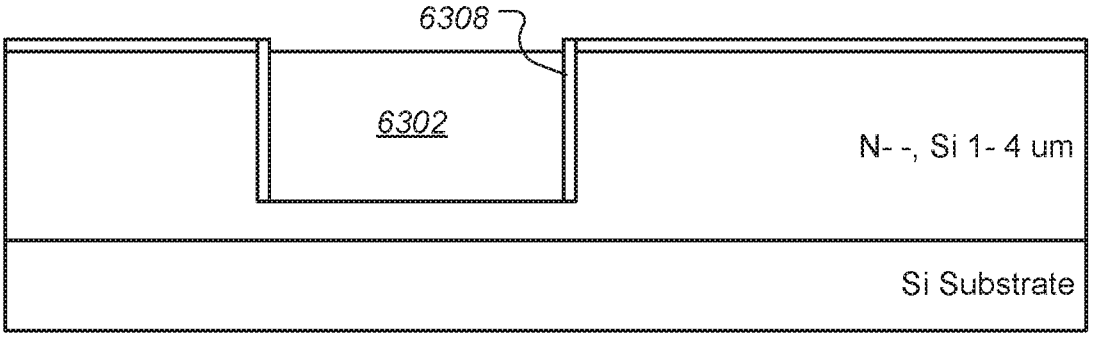


FIG. 63A

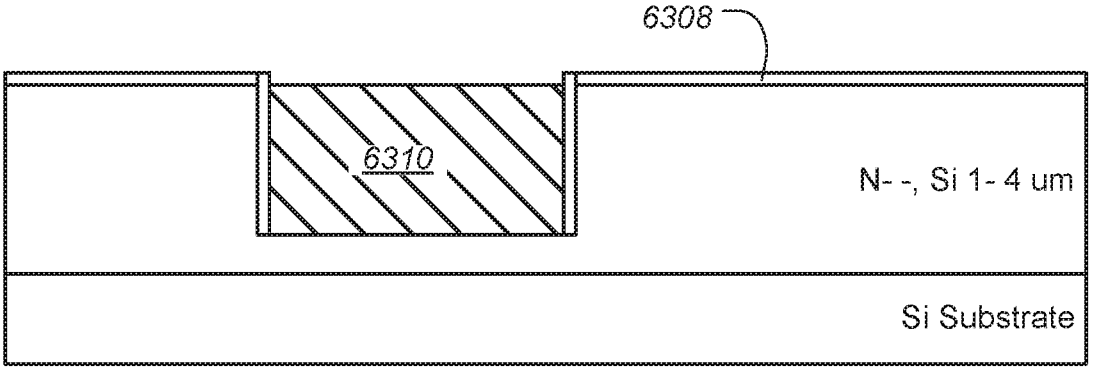


FIG. 63B

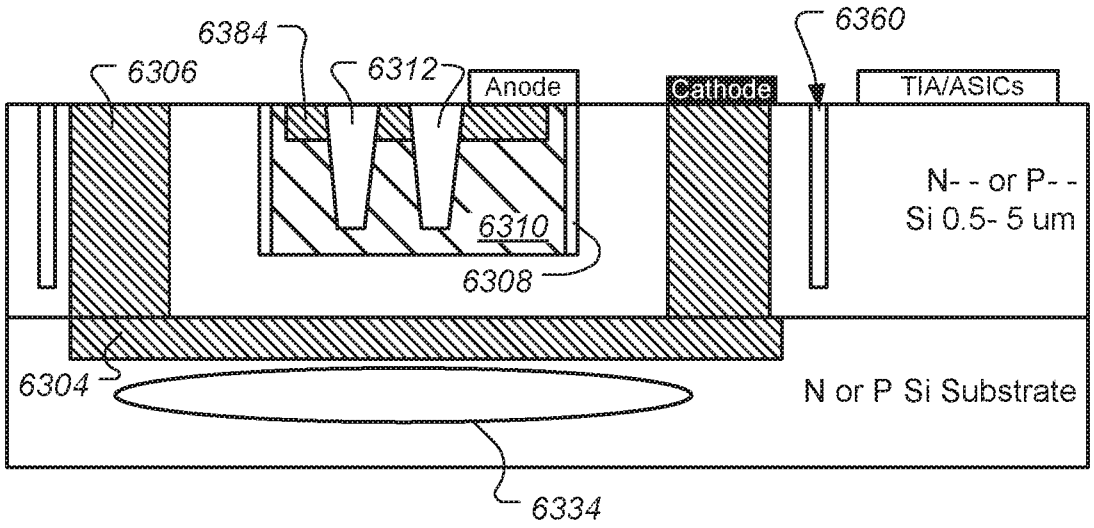

6384
6306
6312
Anode
Cathode
6360
TIA/ASICs
N- - or P- -
Si 0.5- 5 um
6310
6308
6304
N or P Si Substrate
6334

FIG. 63C

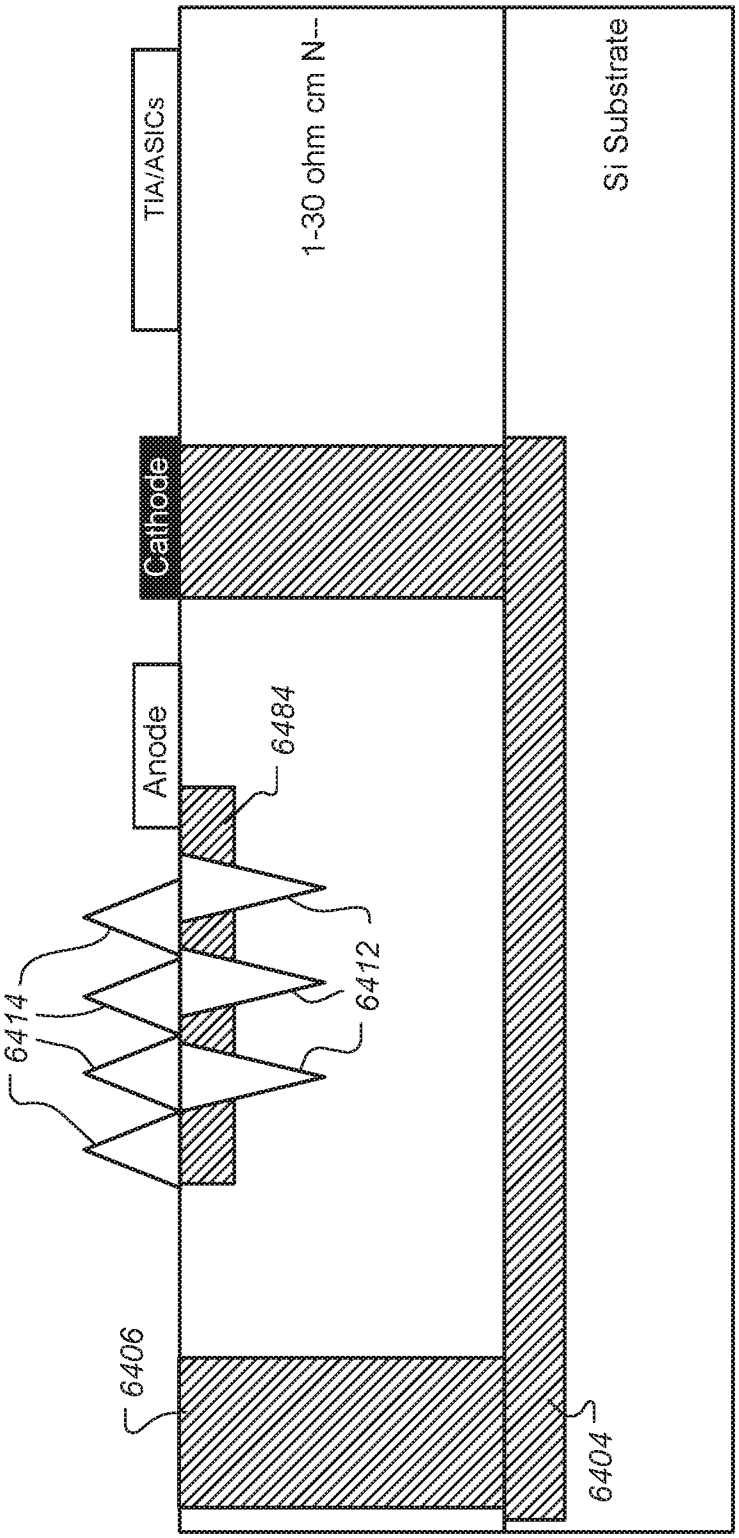

TIA/ASICs
1-30 ohm cm N--
Si Substrate
Cathode
Anode
6484
6412
6414
6406
6404

FIG. 64

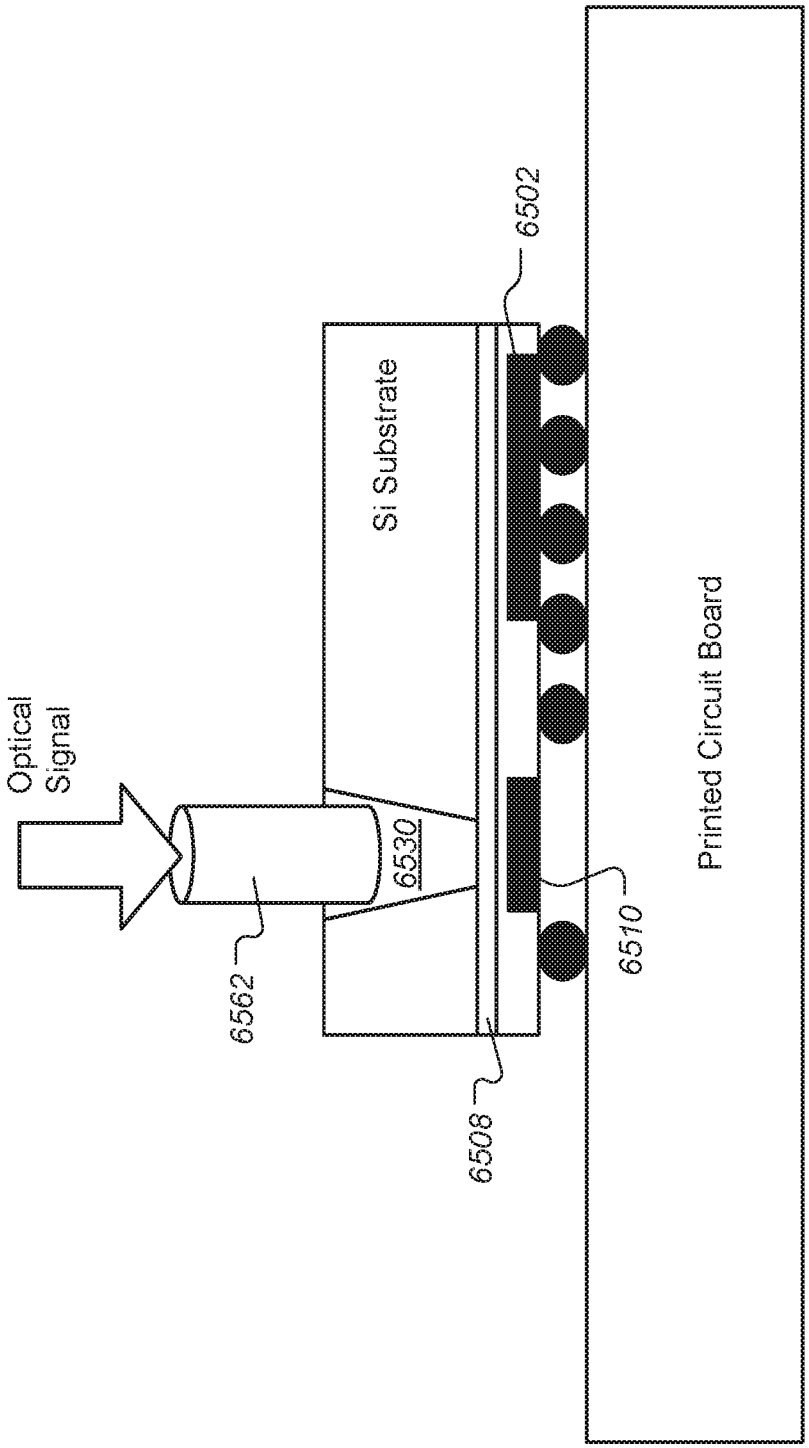

Optical Signal
6562
6530
Si Substrate
6502
6508
6510
Printed Circuit Board

FIG. 65

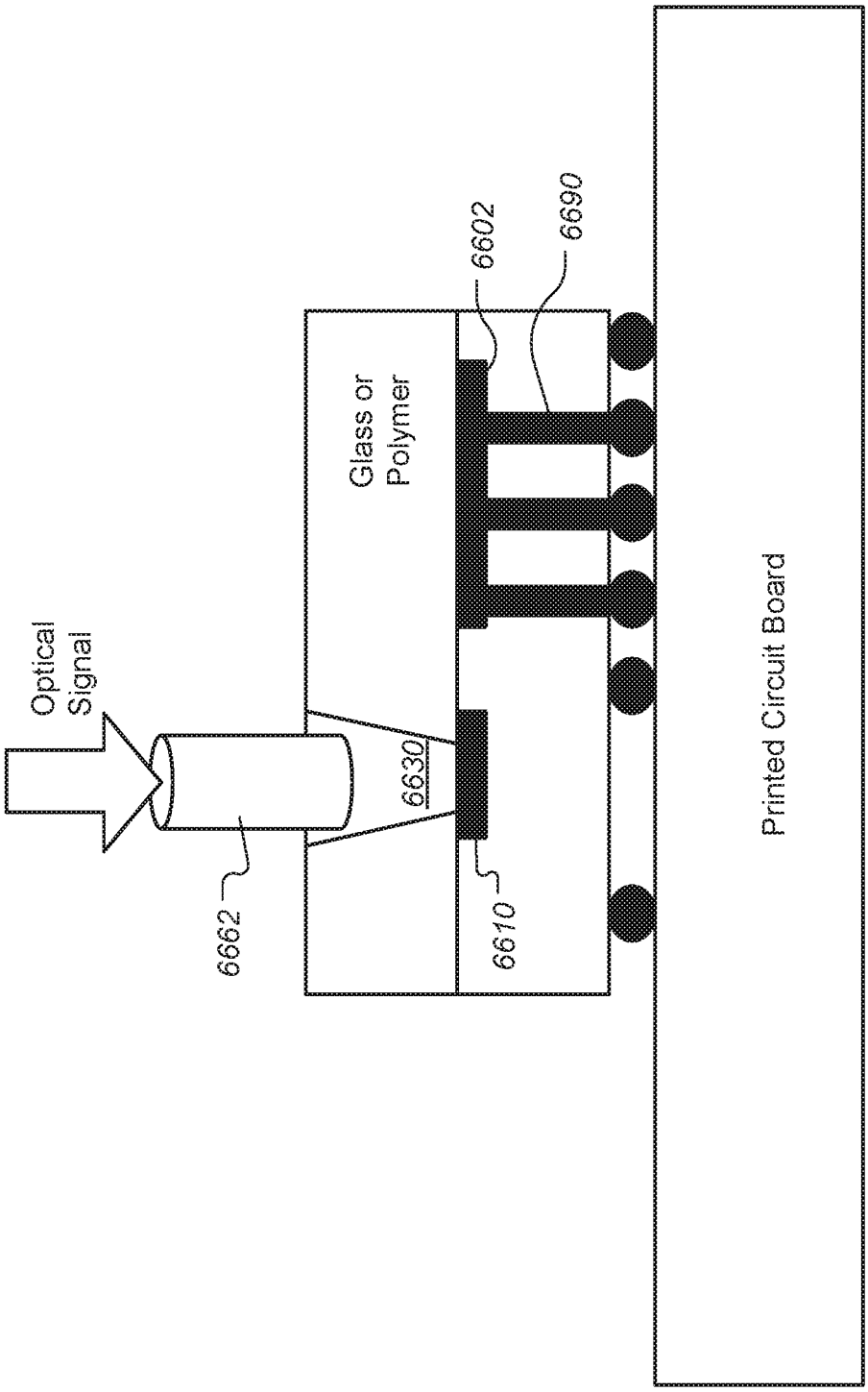

Optical Signal
6662
6630
Glass or Polymer
6602
6690
6610
Printed Circuit Board

FIG. 66

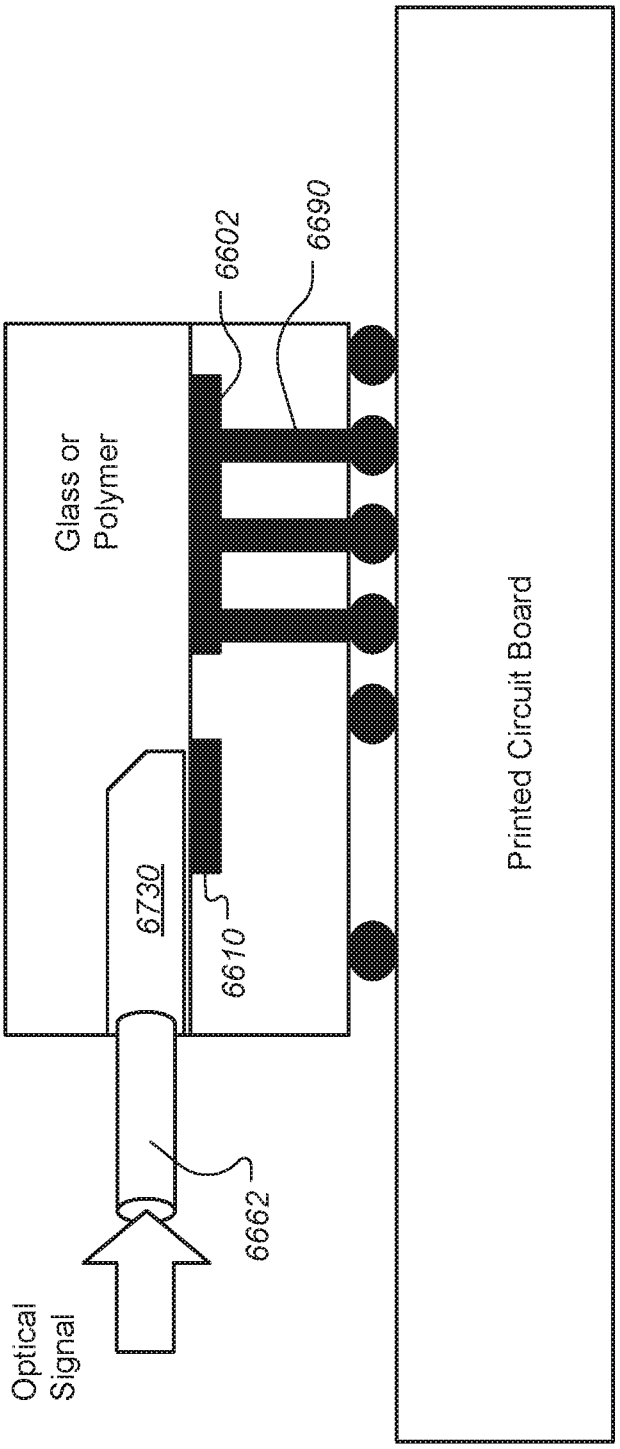

6602
6690
Glass or Polymer
6730
6610
6662
Optical Signal
Printed Circuit Board

FIG. 67

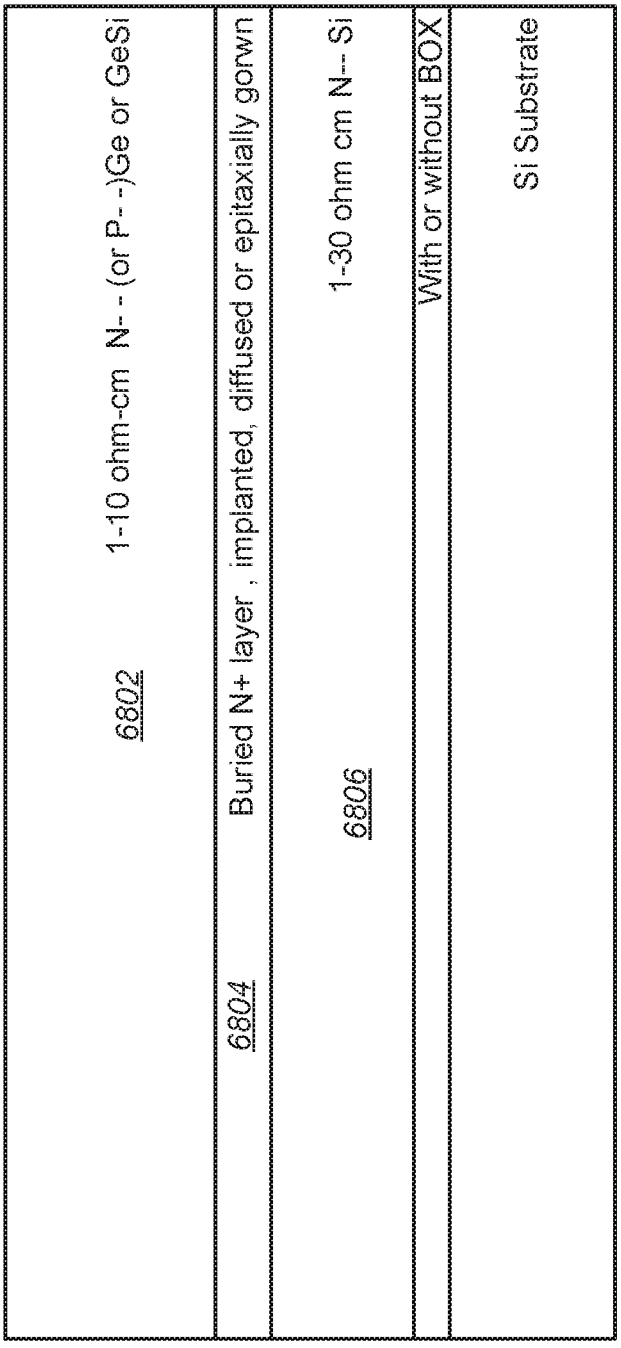

6802
1-10 ohm-cm N- - (or P- -)Ge or GeSi
6804
Buried N+ layer , implanted, diffused or epitaxially gorwn
6806
1-30 ohm cm N-- Si
With or without BOX
Si Substrate

FIG. 68A

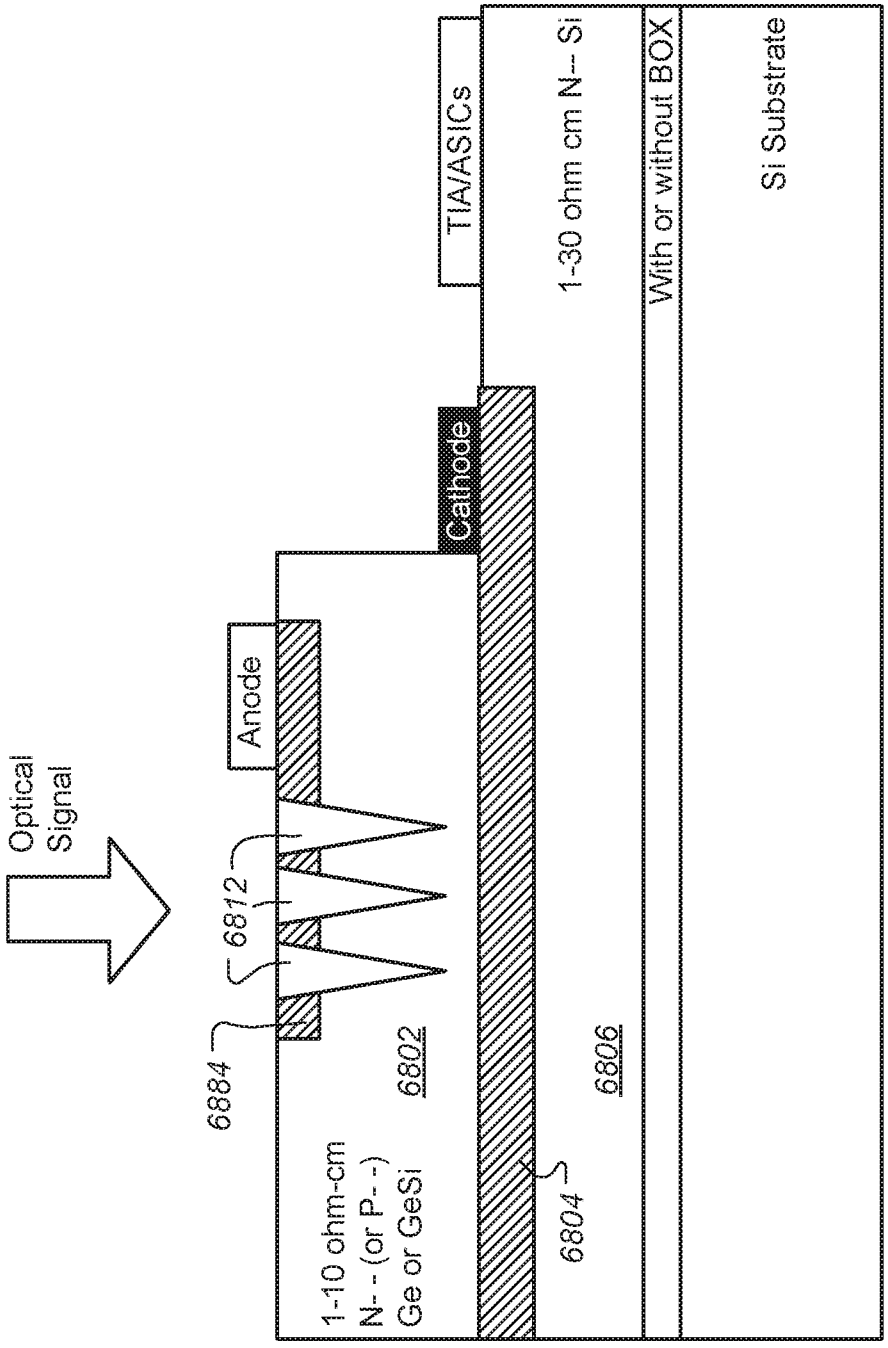

Optical Signal
Anode
Cathode
TIA/ASICs
1-30 ohm cm N-- Si
With or without BOX
Si Substrate
6812
6884
6802
6806
6804
1-10 ohm-cm
N- - (or P- -)
Ge or GeSi

FIG. 68B

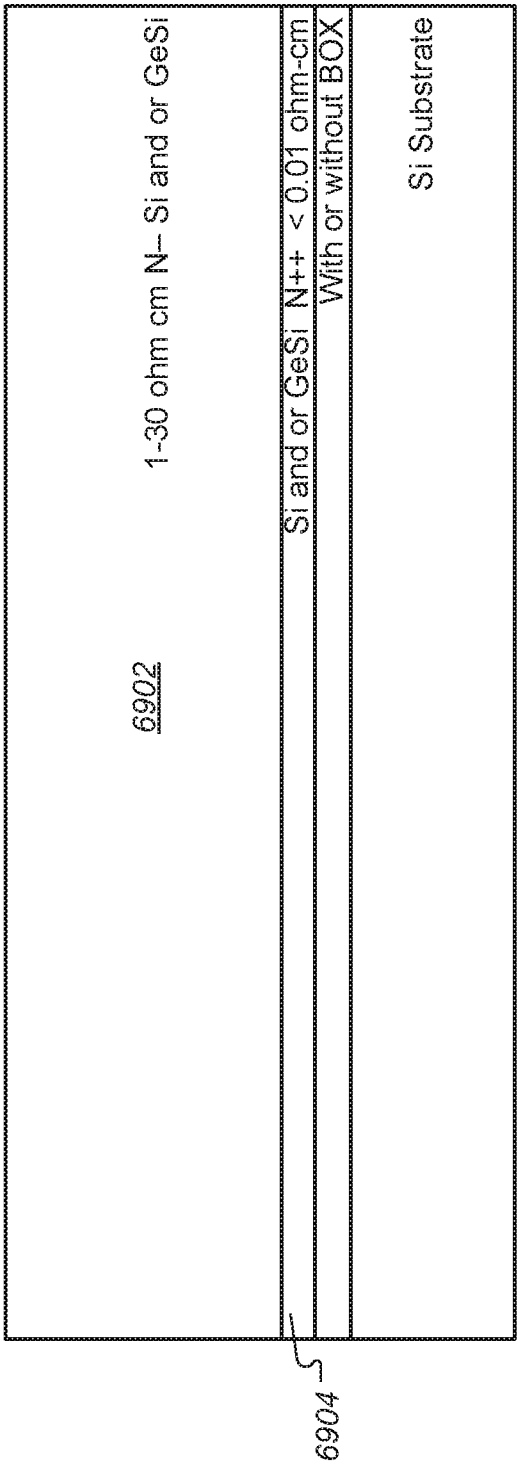

1-30 ohm cm N– Si and or GeSi
6902
Si and or GeSi N++ < 0.01 ohm-cm
With or without BOX
Si Substrate
6904

FIG. 69A

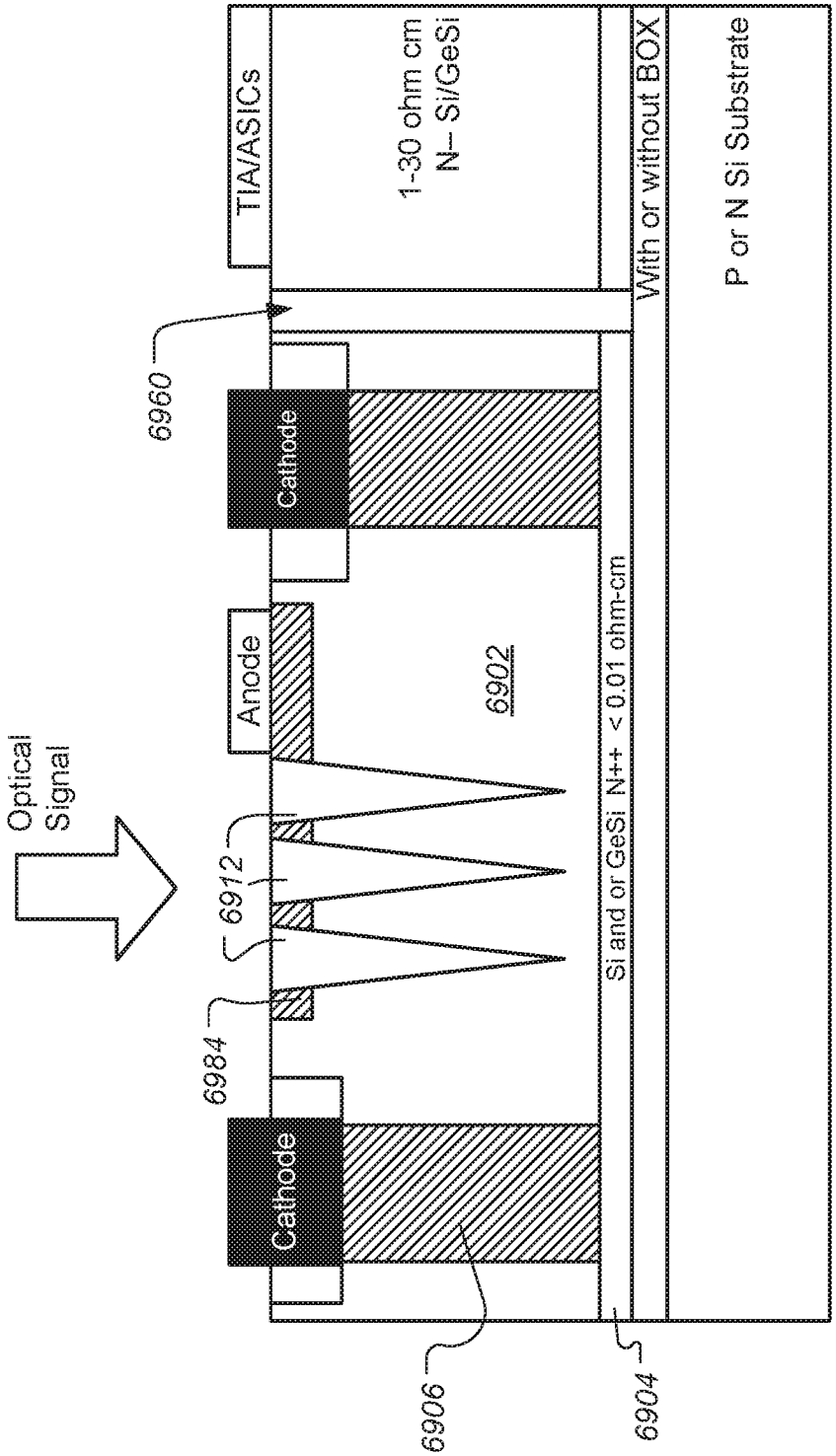

TIA/ASICs
1-30 ohm cm
N– Si/GeSi
With or without BOX
P or N Si Substrate
6960
Cathode
Anode
6902
Optical
Signal
6912
6984
Cathode
Si and or GeSi N++ < 0.01 ohm-cm
6906
6904

FIG. 69B

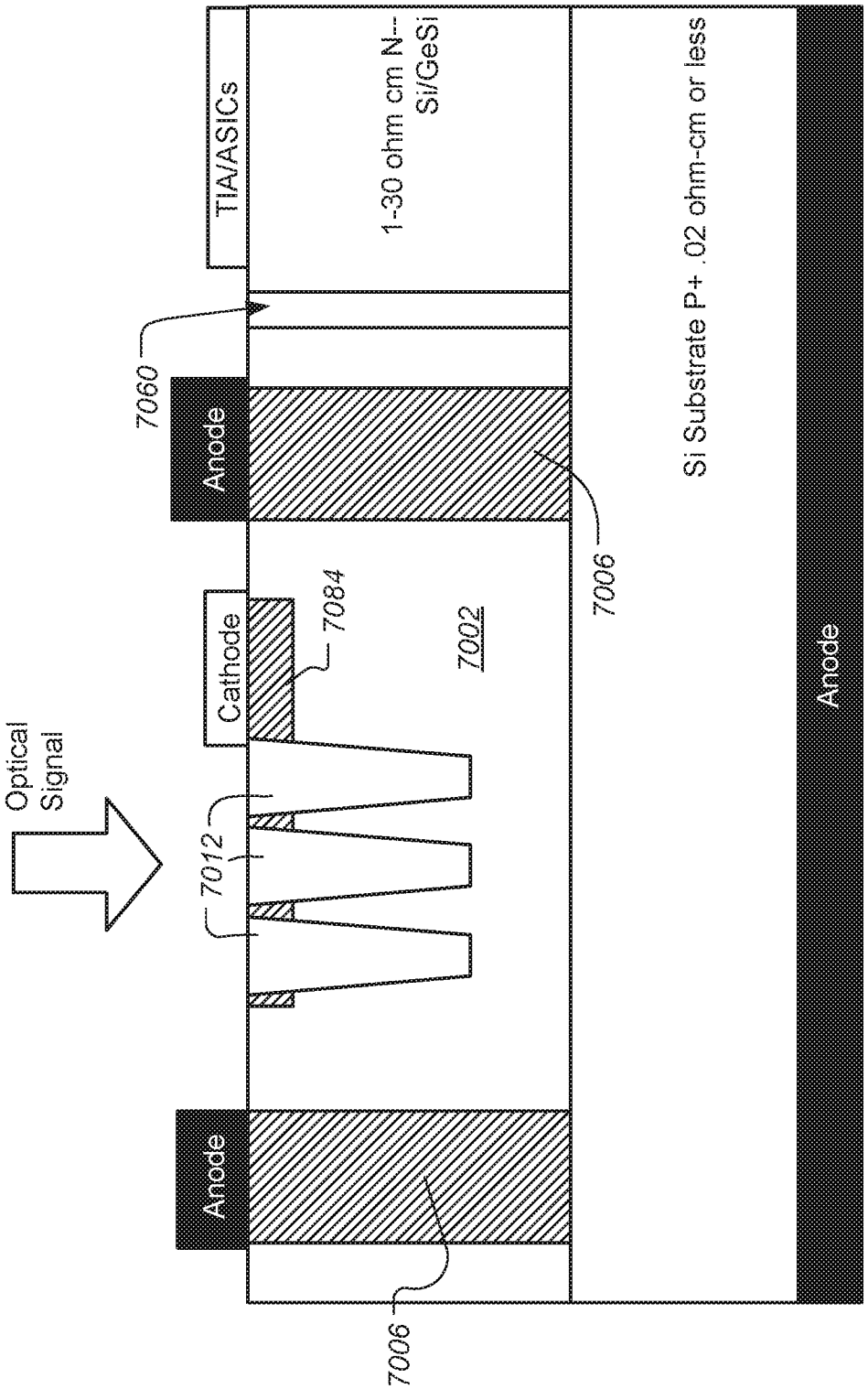

TIA/ASICs
1-30 ohm cm N--
Si/GeSi
Si Substrate P+ .02 ohm-cm or less
7060
Anode
7006
7084
Cathode
7002
Optical
Signal
7012
Anode
Anode
7006

FIG. 70A

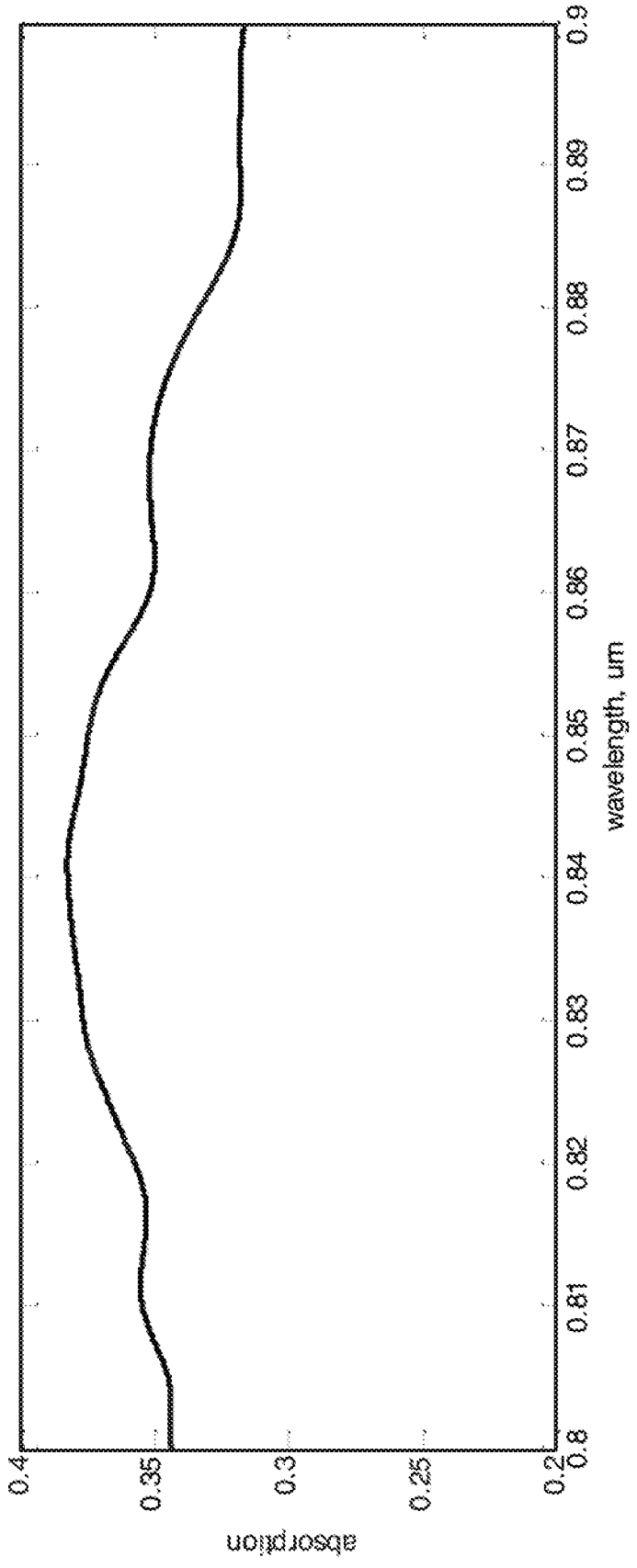

absorption
0.4
0.35
0.3
0.25
0.2
wavelength, um
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9

FIG. 70B

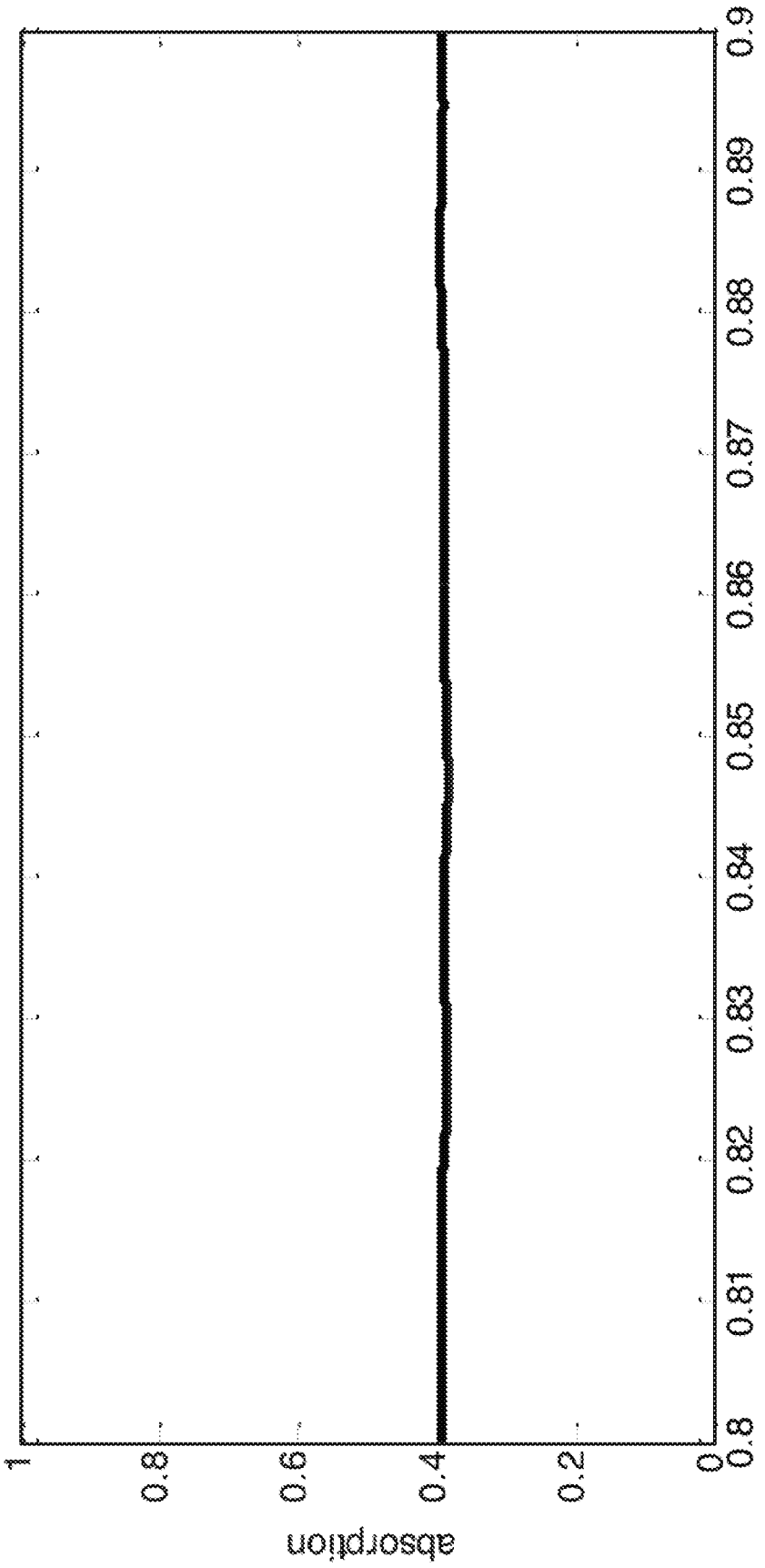

absorption
1
0.8
0.6
0.4
0.2
0
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9
wavelength, um

FIG. 70C

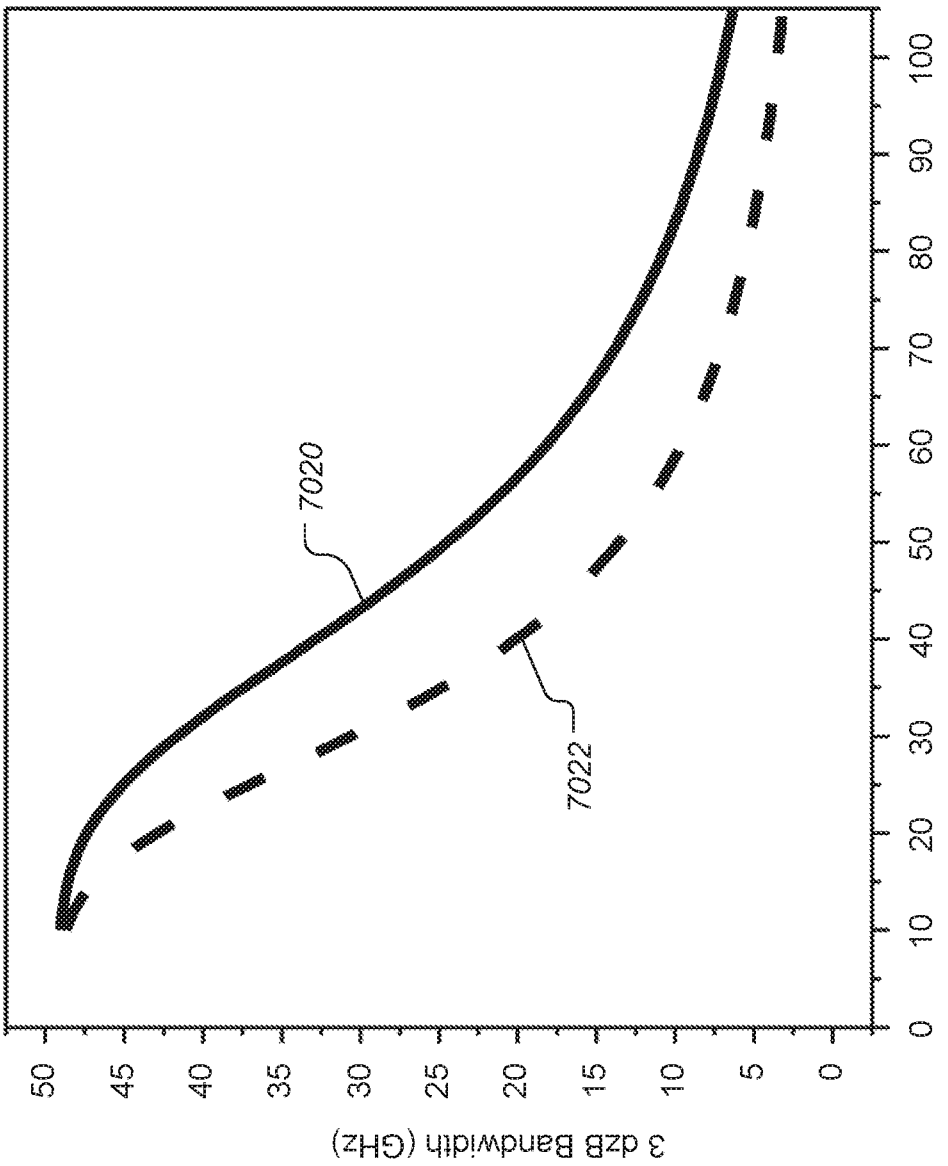

3 dzB Bandwidth (GHz)
0
5
10
15
20
25
30
35
40
45
50
PD diameter (um)
0
10
20
30
40
50
60
70
80
90
100
7020
7022

FIG. 70D

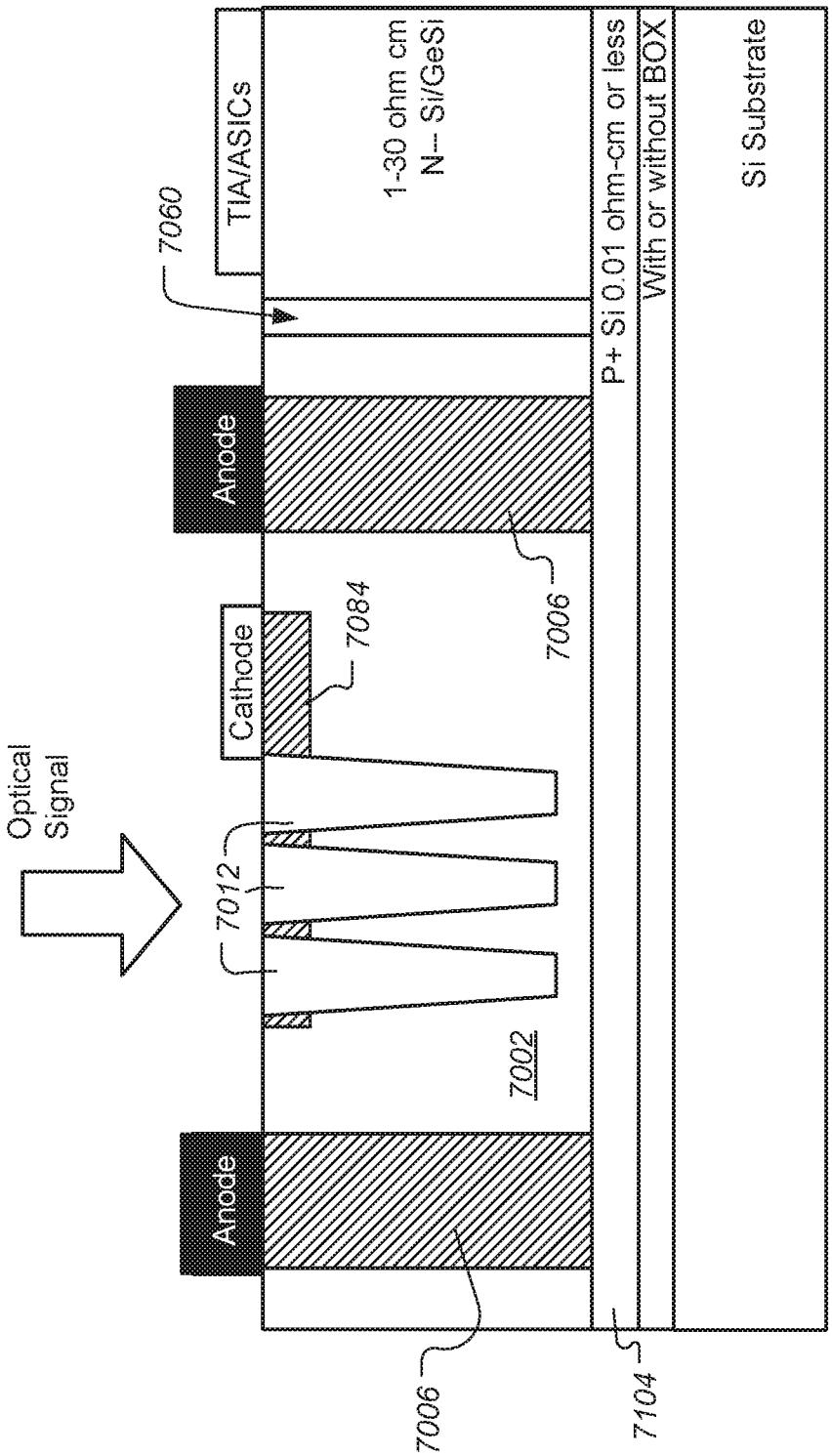

7060
TIA/ASICs
1-30 ohm cm
N– Si/GeSi
P+ Si 0.01 ohm-cm or less
With or without BOX
Si Substrate
Anode
Cathode
7084
7006
Optical
Signal
7012
7002
Anode
7006
7104

FIG. 71

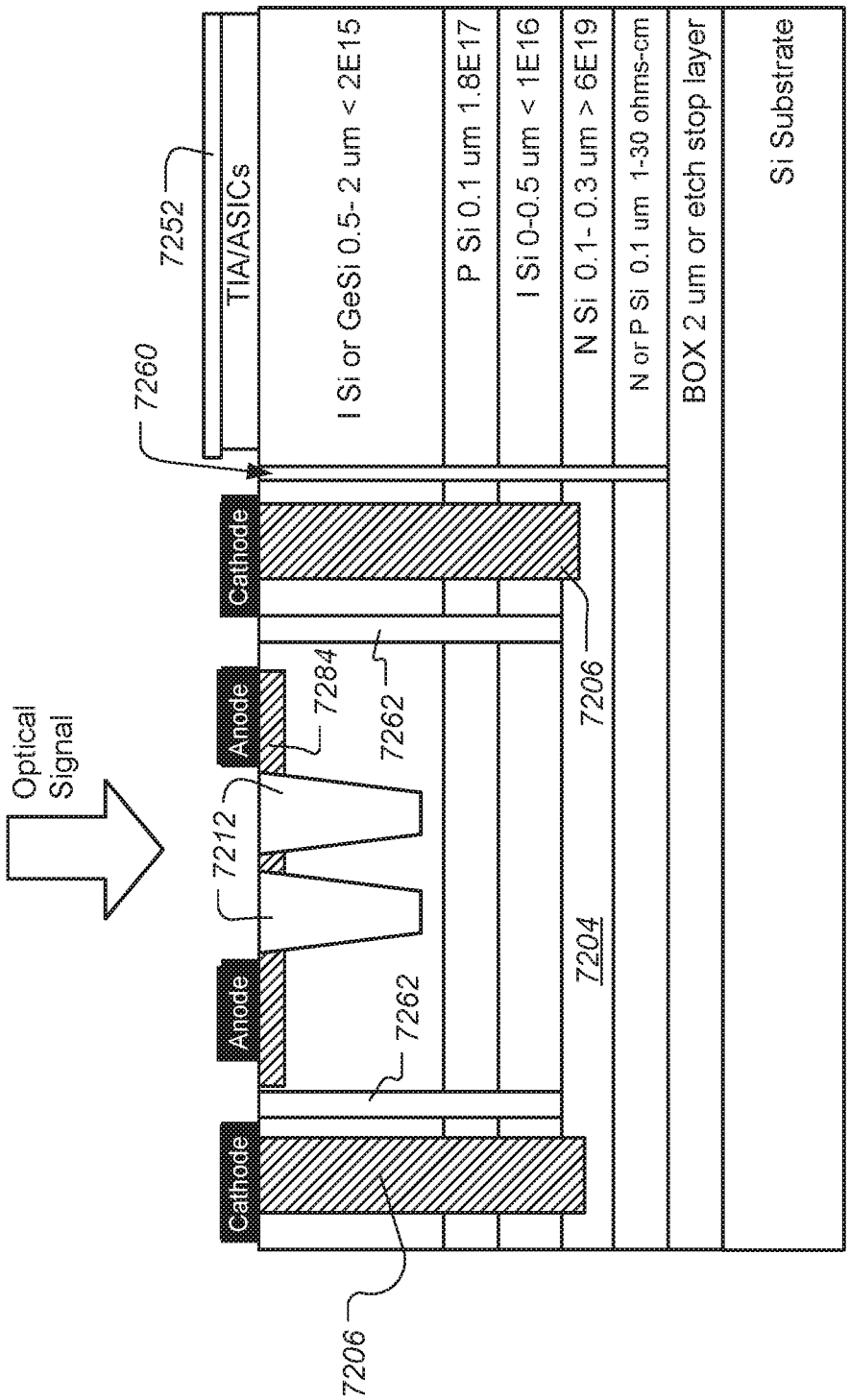

Optical Signal
7212
Anode
7284
7262
Anode
7262
Cathode
Cathode
7206
7206
7204
7260
7252
TIA/ASICs
I Si or GeSi 0.5- 2 um < 2E15
P Si 0.1 um 1.8E17
I Si 0-0.5 um < 1E16
N Si 0.1- 0.3 um > 6E19
N or P Si 0.1 um 1-30 ohms-cm
BOX 2 um or etch stop layer
Si Substrate

FIG. 72

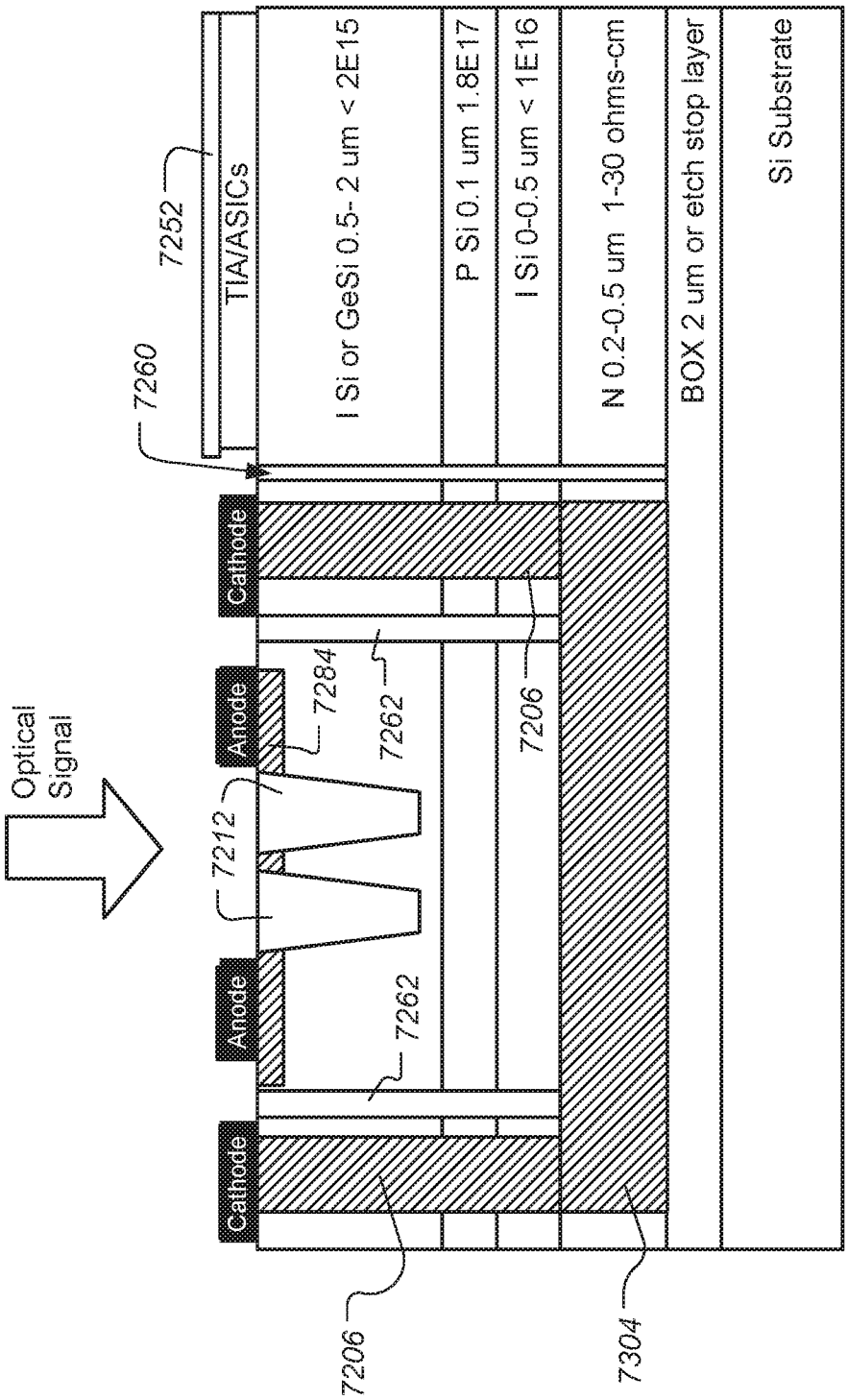

Optical Signal
7252
TIA/ASICs
7260
I Si or GeSi 0.5- 2 um < 2E15
P Si 0.1 um 1.8E17
I Si 0-0.5 um < 1E16
N 0.2-0.5 um 1-30 ohms-cm
BOX 2 um or etch stop layer
Si Substrate
Cathode
Anode
Anode
Cathode
7284
7262
7212
7262
7206
7206
7304

FIG. 73

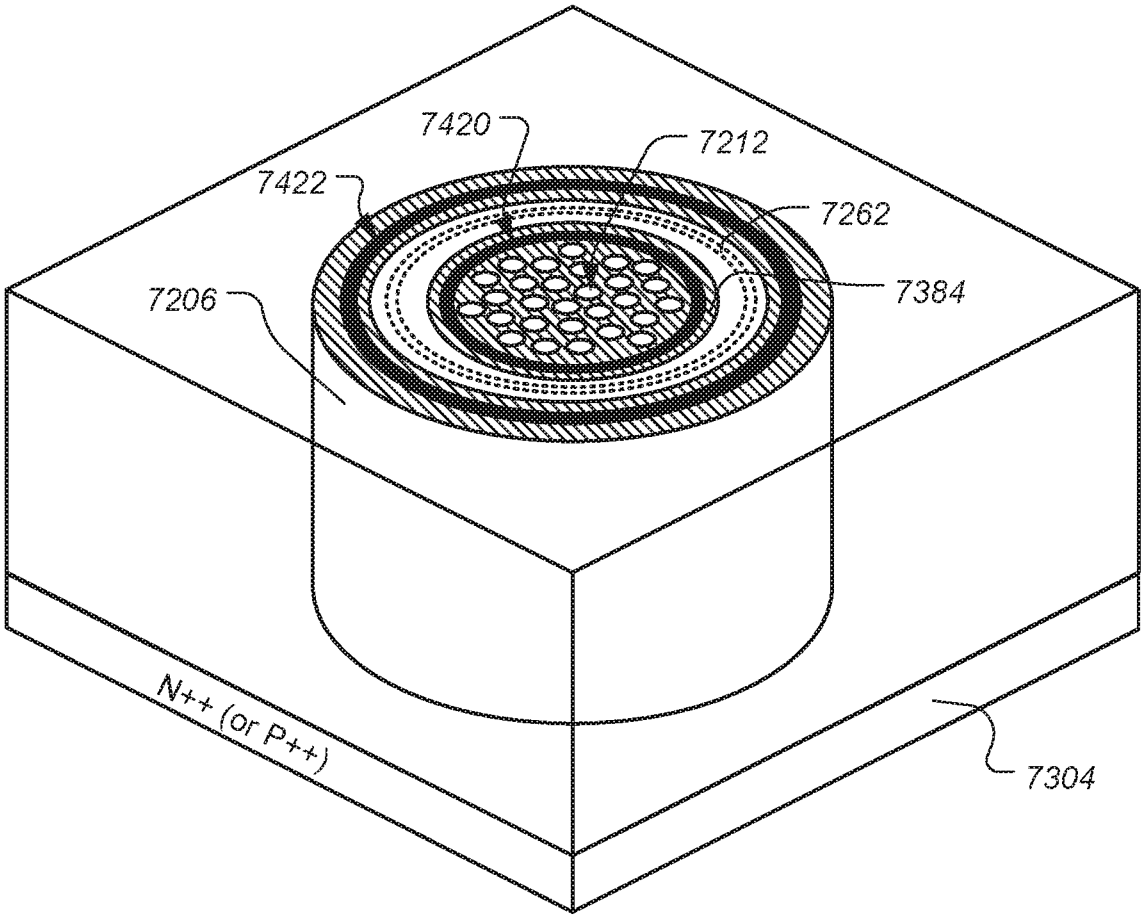


FIG. 74

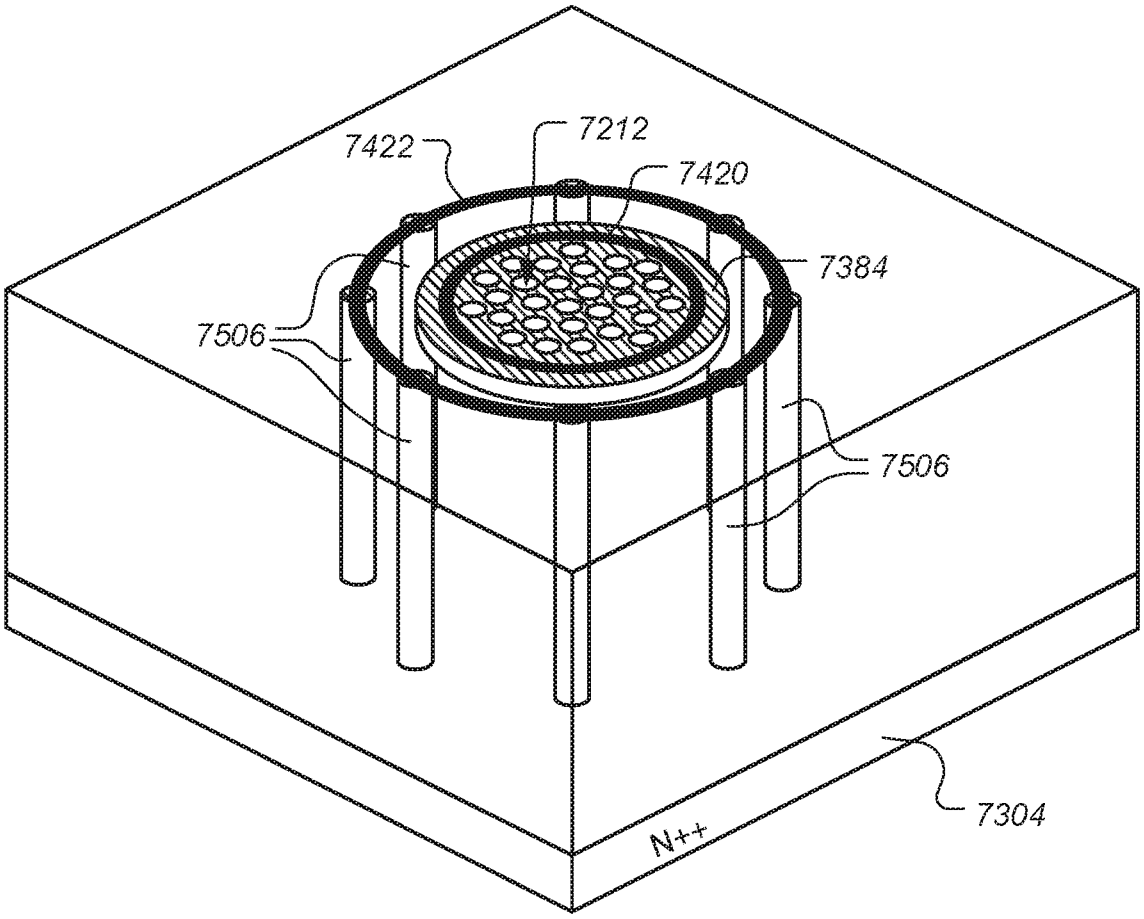


FIG. 75

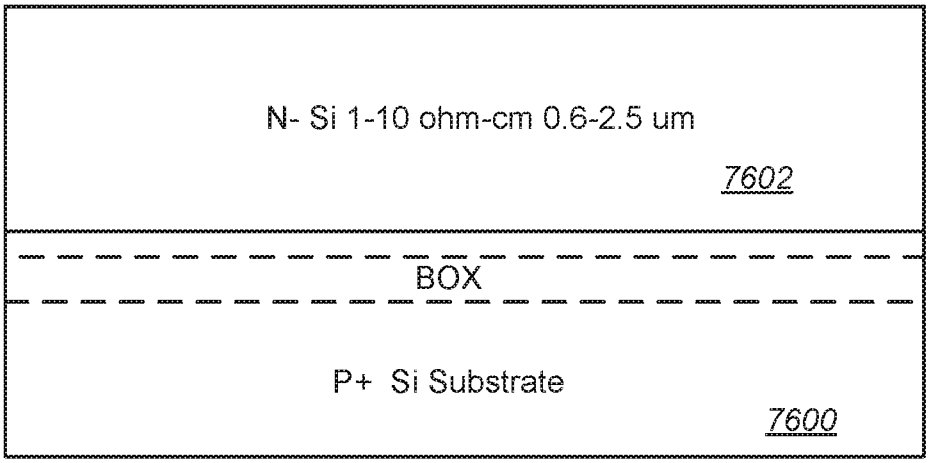


FIG. 76A

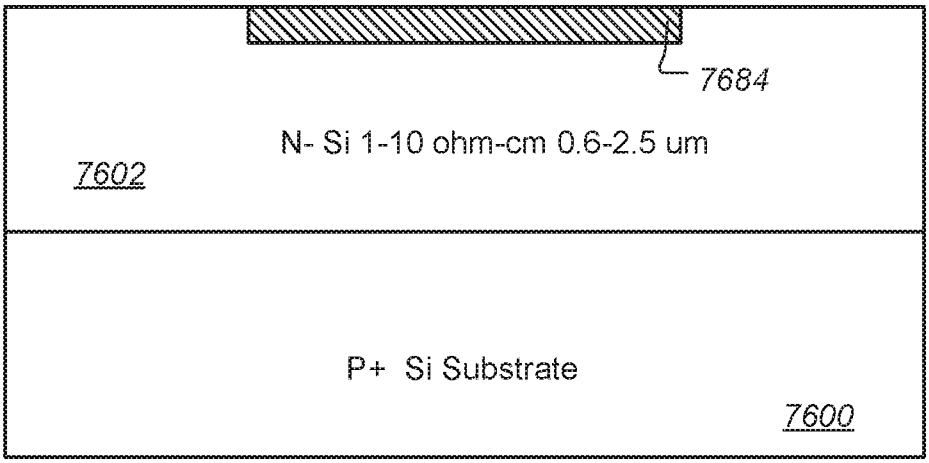


FIG. 76B

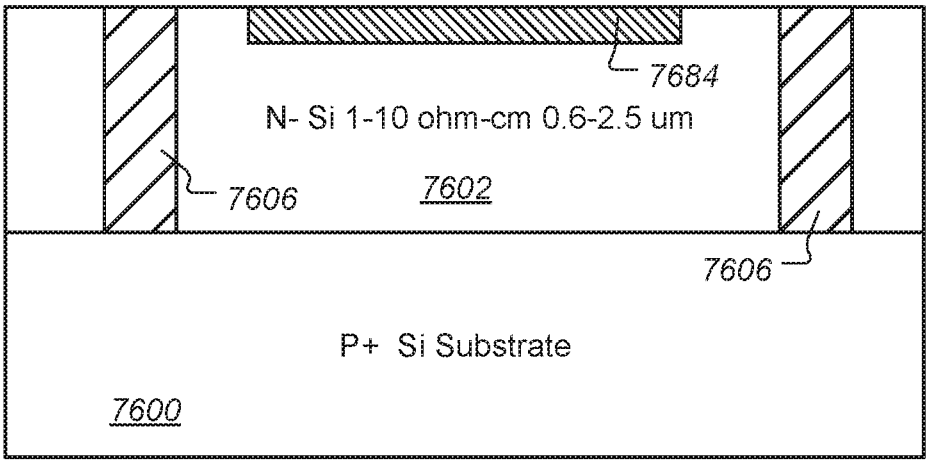


FIG. 76C

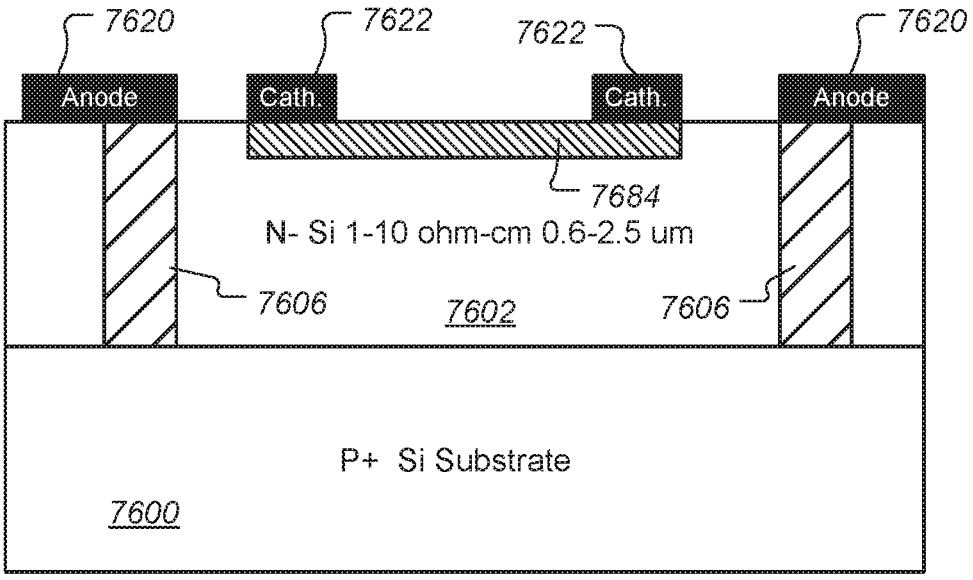


FIG. 76D

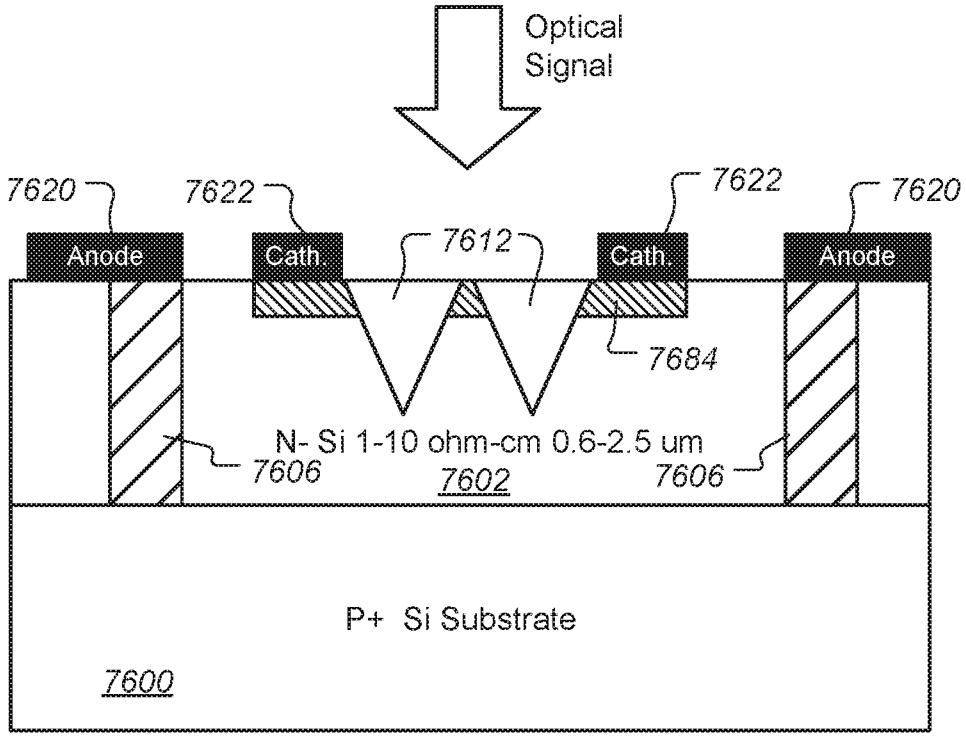


FIG. 76E

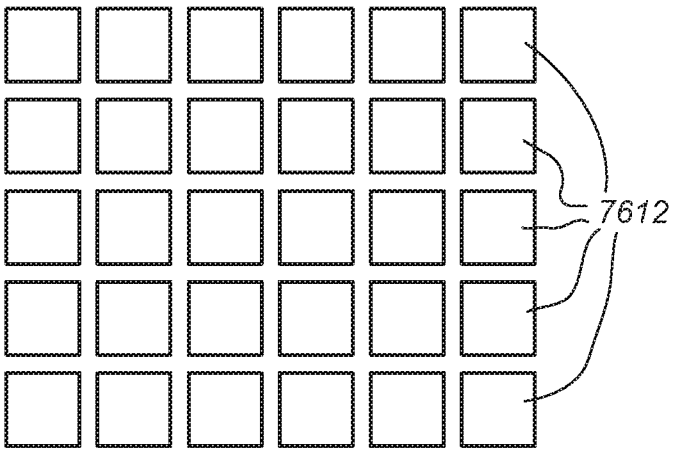


FIG. 76F

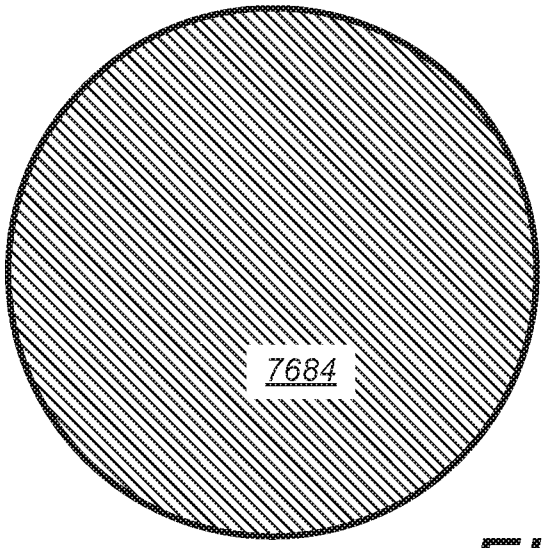


FIG. 76G

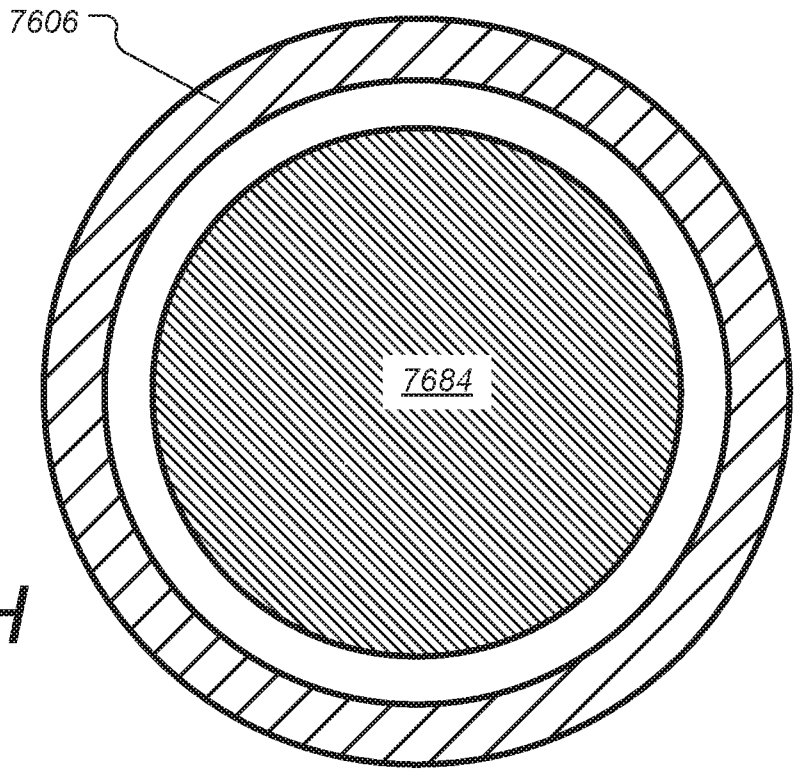


FIG. 76H

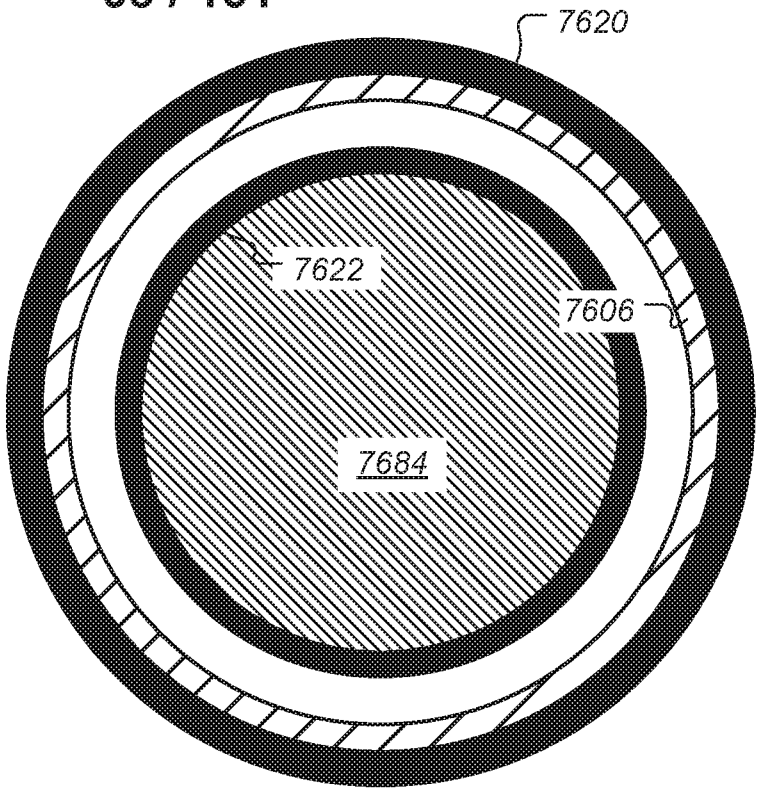


FIG. 76I

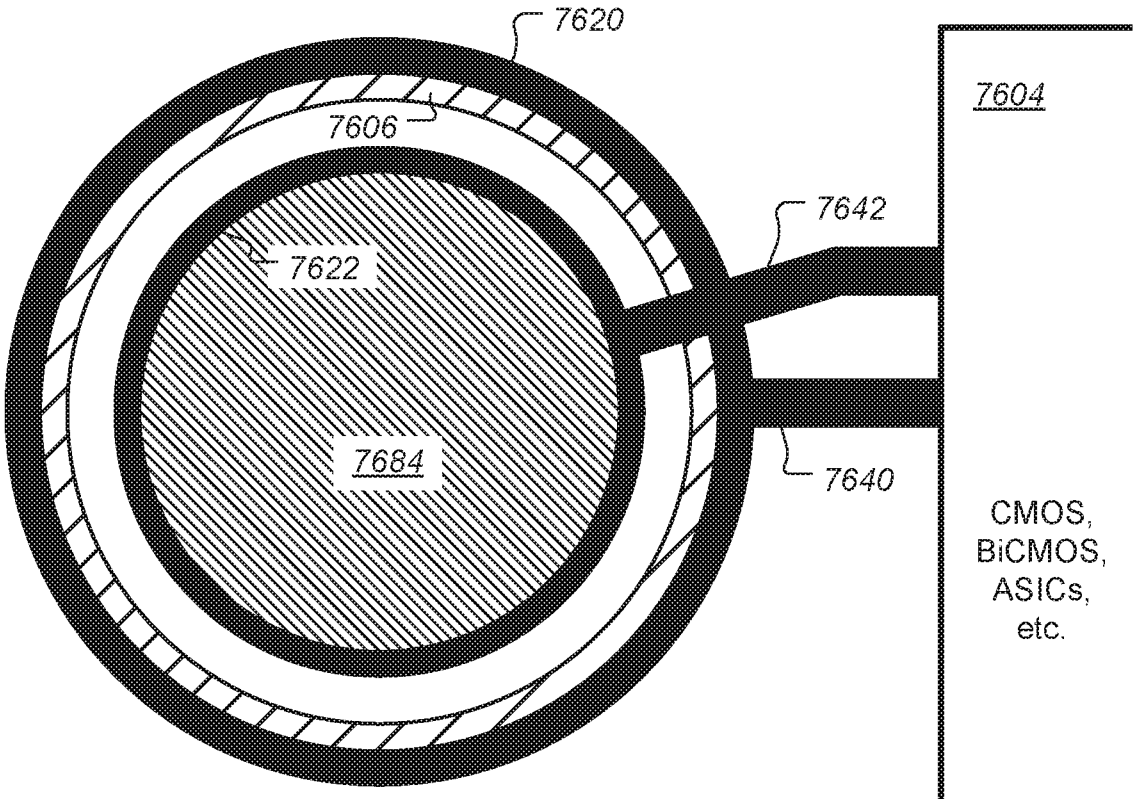


FIG. 76J

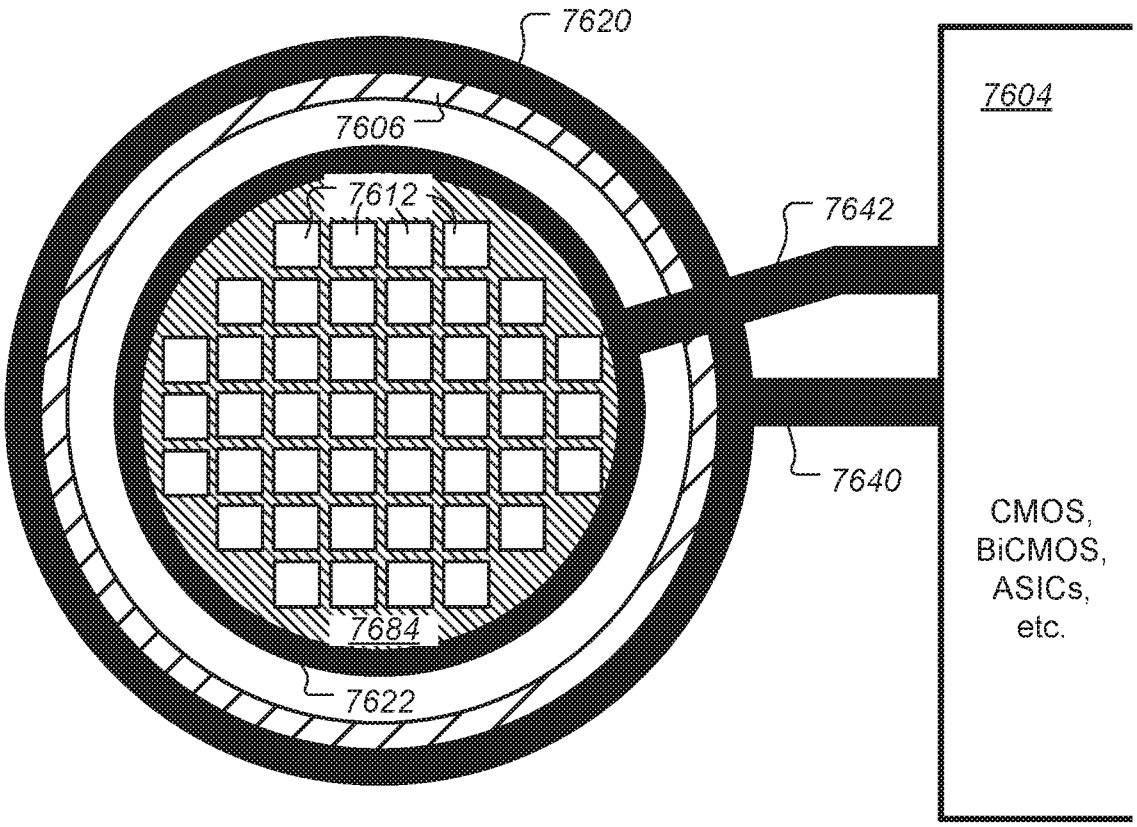

7620
7606
7612
7642
7604
7640
CMOS,
BiCMOS,
ASICs,
etc.
7684
7622

FIG. 76K

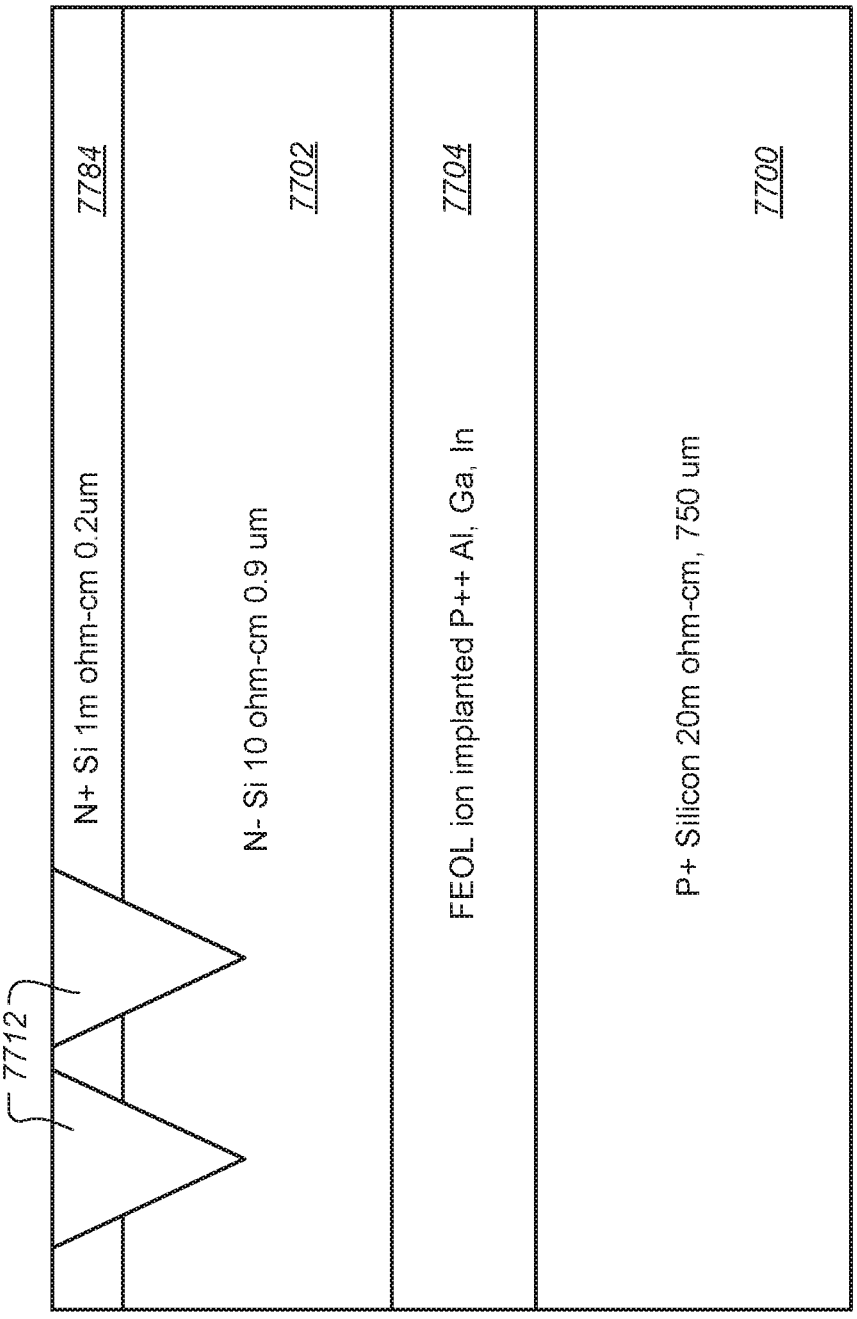

7784
N+ Si 1m ohm-cm 0.2um
7702
N- Si 10 ohm-cm 0.9 um
7704
FEOL ion implanted P++ Al, Ga, In
7700
P+ Silicon 20m ohm-cm, 750 um
7712

FIG. 77A

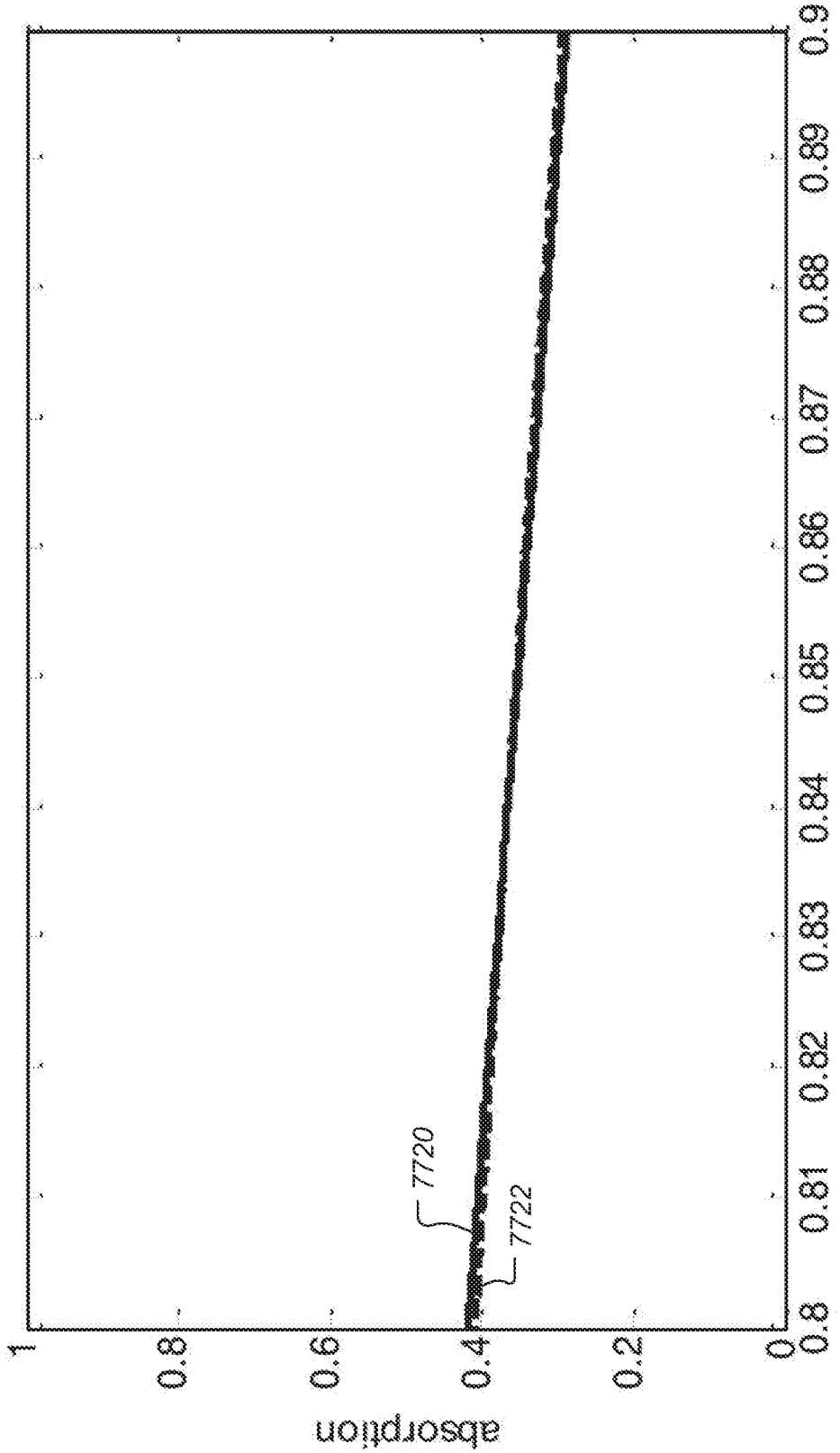

absorption
1
0.8
0.6
0.4
0.2
0
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9
wavelength, um
7720
7722

FIG. 77B

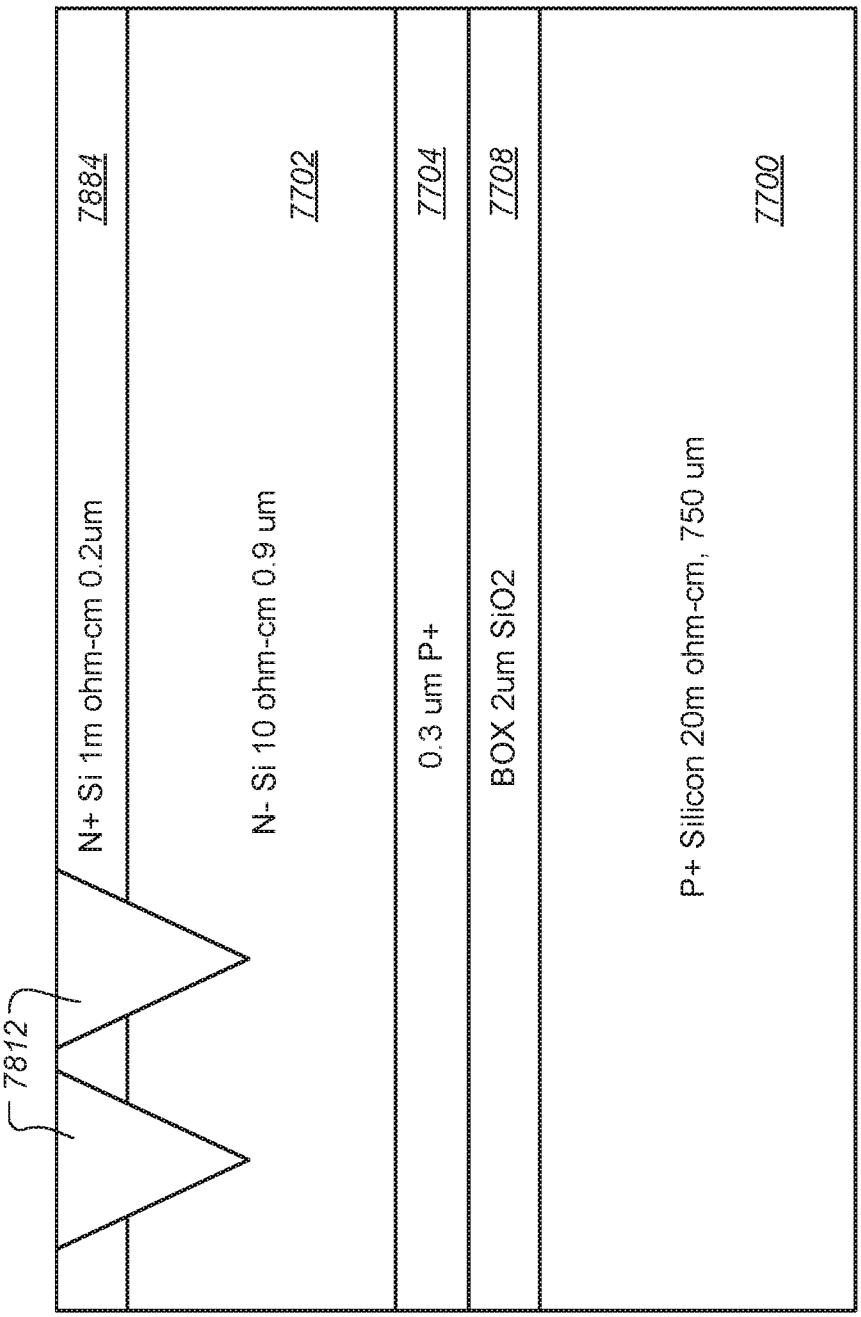

7884
7702
7704
7708
7700
N+ Si 1m ohm-cm 0.2um
N- Si 10 ohm-cm 0.9 um
0.3 um P+
BOX 2um SiO2
P+ Silicon 20m ohm-cm, 750 um
7812

FIG. 78

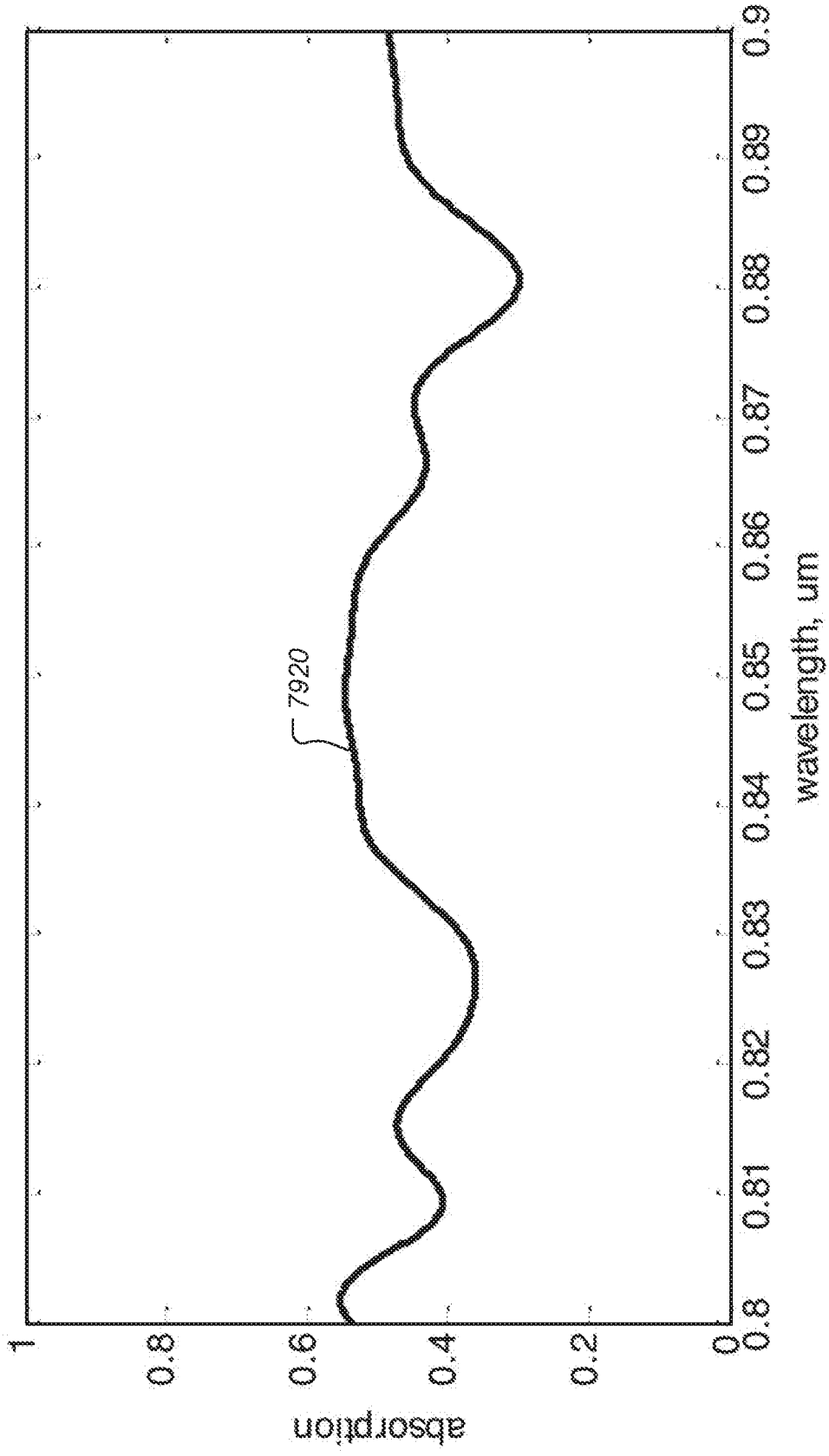

absorption
1
0.8
0.6
0.4
0.2
0
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9
wavelength, um
7920

FIG. 79

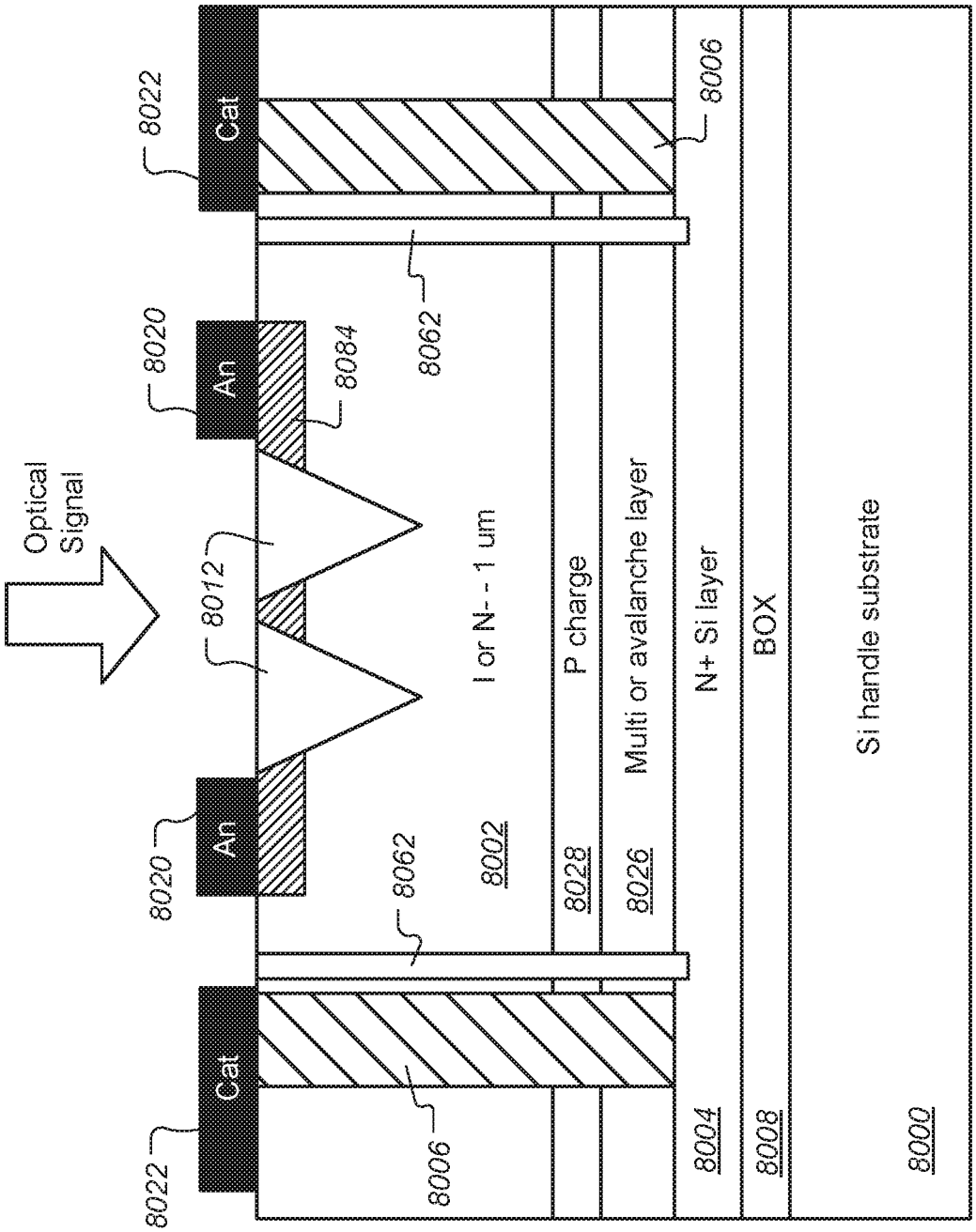

Optical Signal
8012
8022
Cat
8020
An
8084
8062
8006
I or N- - 1 um
8002
P charge
8028
Multi or avalanche layer
8026
N+ Si layer
8004
BOX
8008
Si handle substrate
8000

FIG. 80

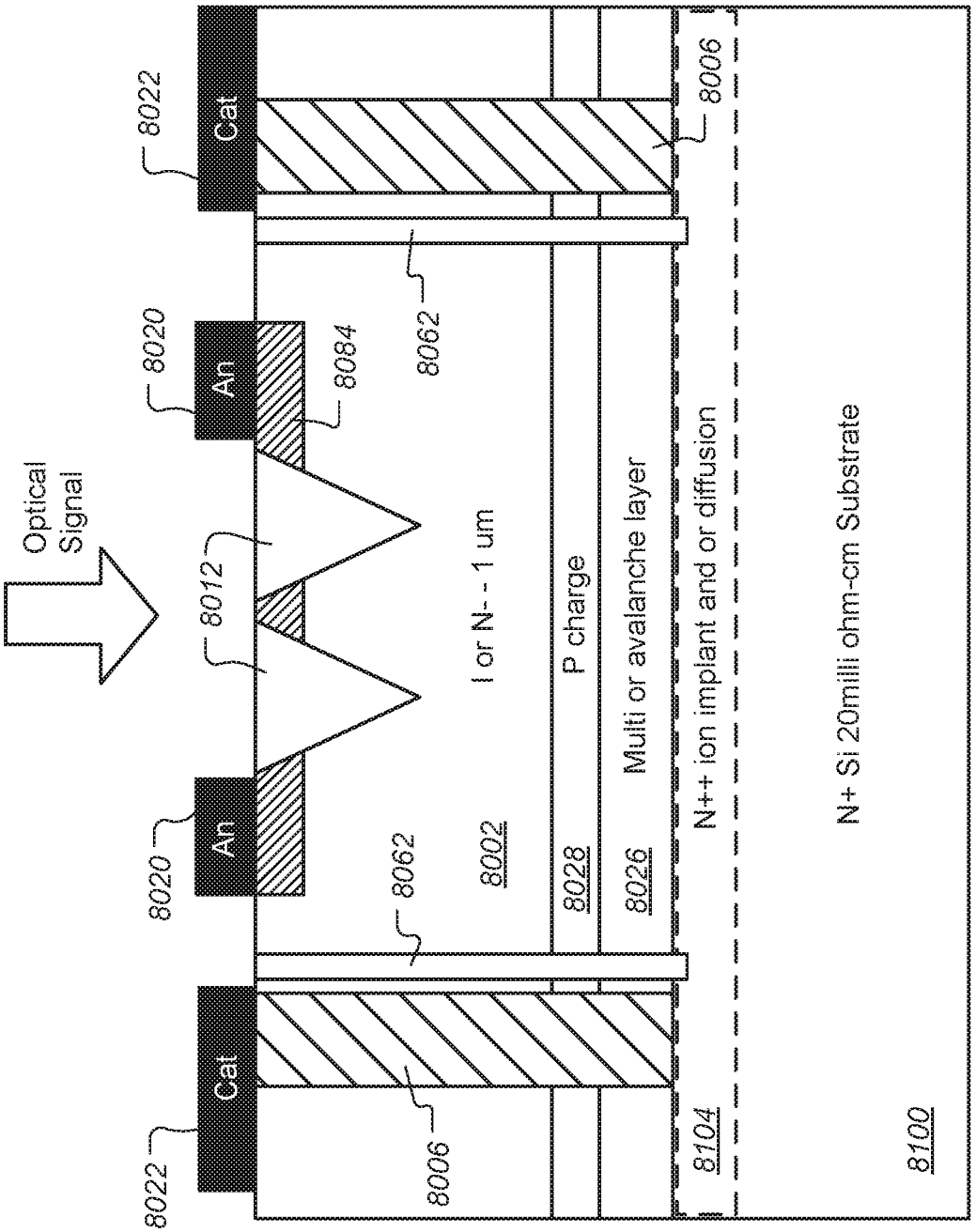

Optical Signal
8012
8020
An
8084
8062
8022
Cat
8006
I or N- - 1 um
8002
P charge
8028
Multi or avalanche layer
8026
N++ ion implant and or diffusion
8104
N+ Si 20milli ohm-cm Substrate
8100

FIG. 81

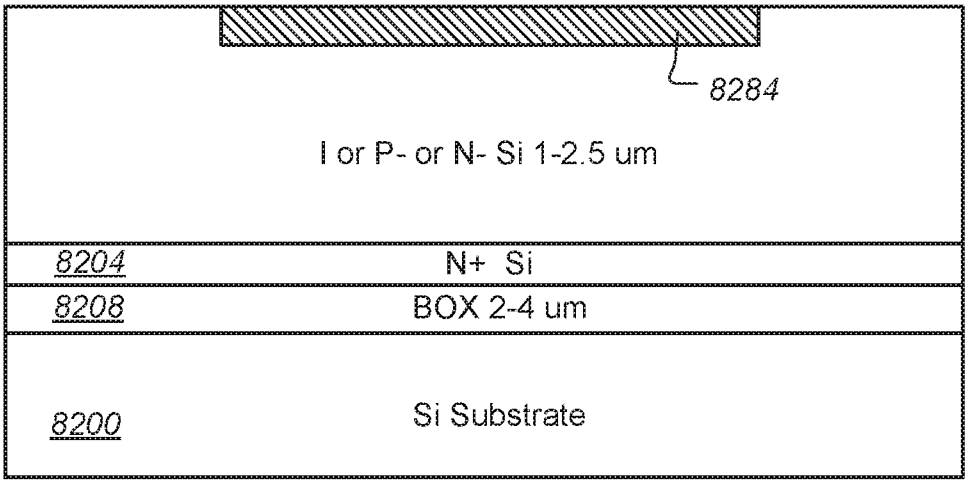


FIG. 82A

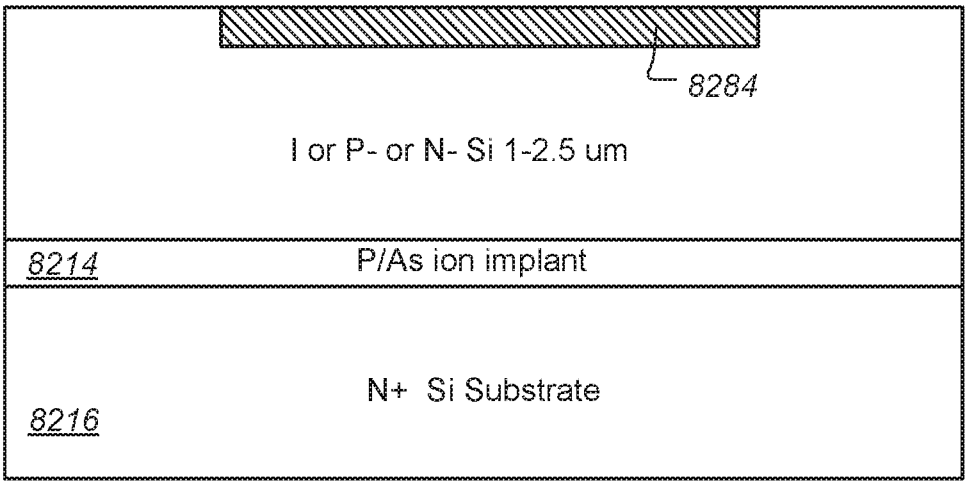


FIG. 82B

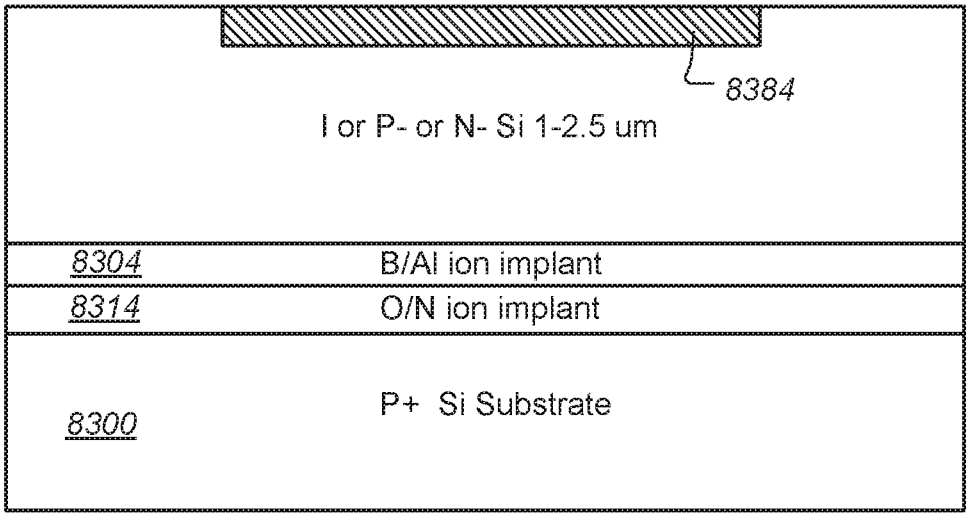

8384
I or P- or N- Si 1-2.5 um
8304
B/Al ion implant
8314
O/N ion implant
8300
P+ Si Substrate

FIG. 83

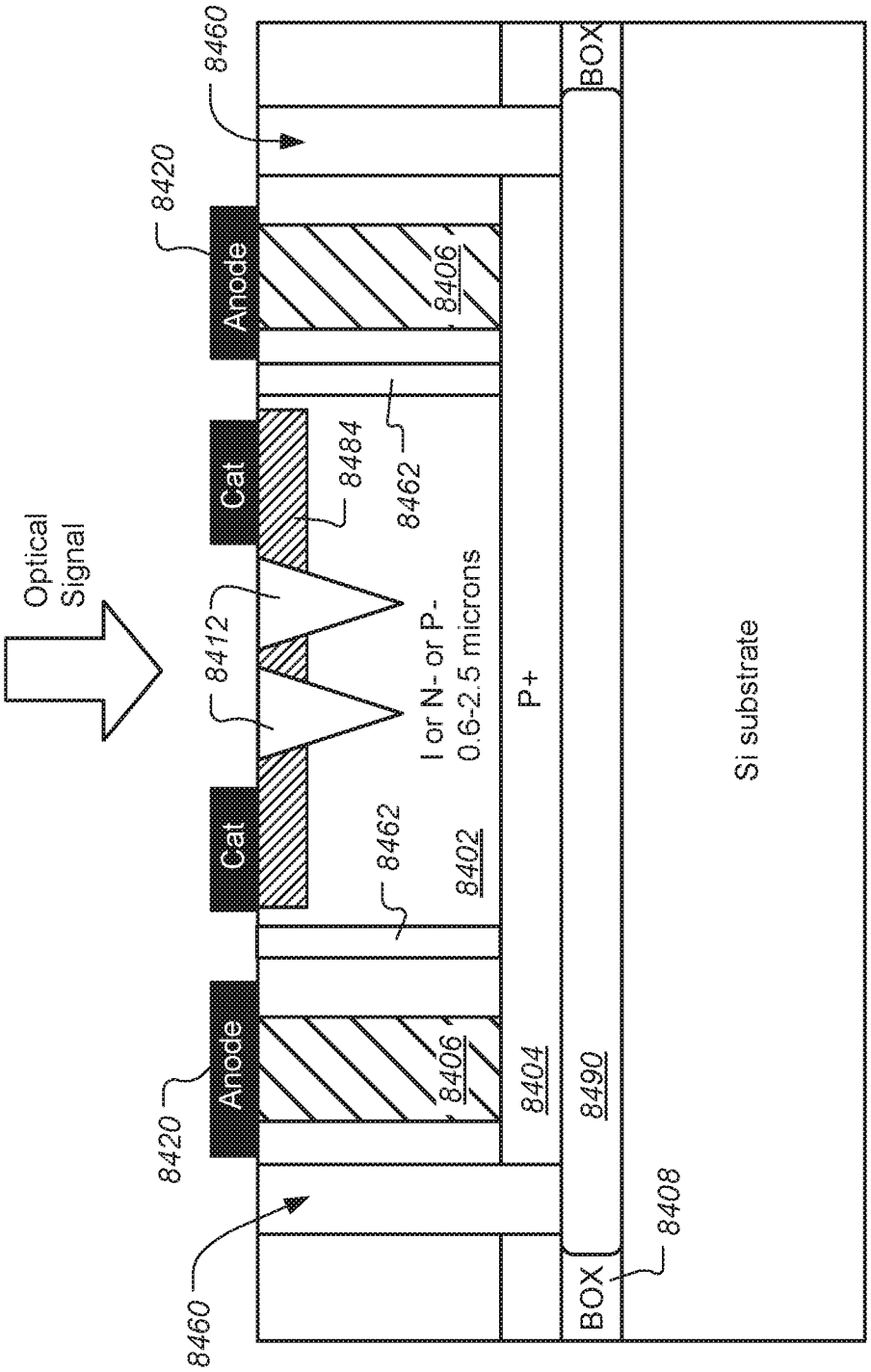

Optical Signal
8460
8420
Anode
8406
8484
8462
Cat
8412
I or N- or P-
0.6-2.5 microns
8402
P+
BOX
Si substrate
8404
8490
8408

FIG. 84A

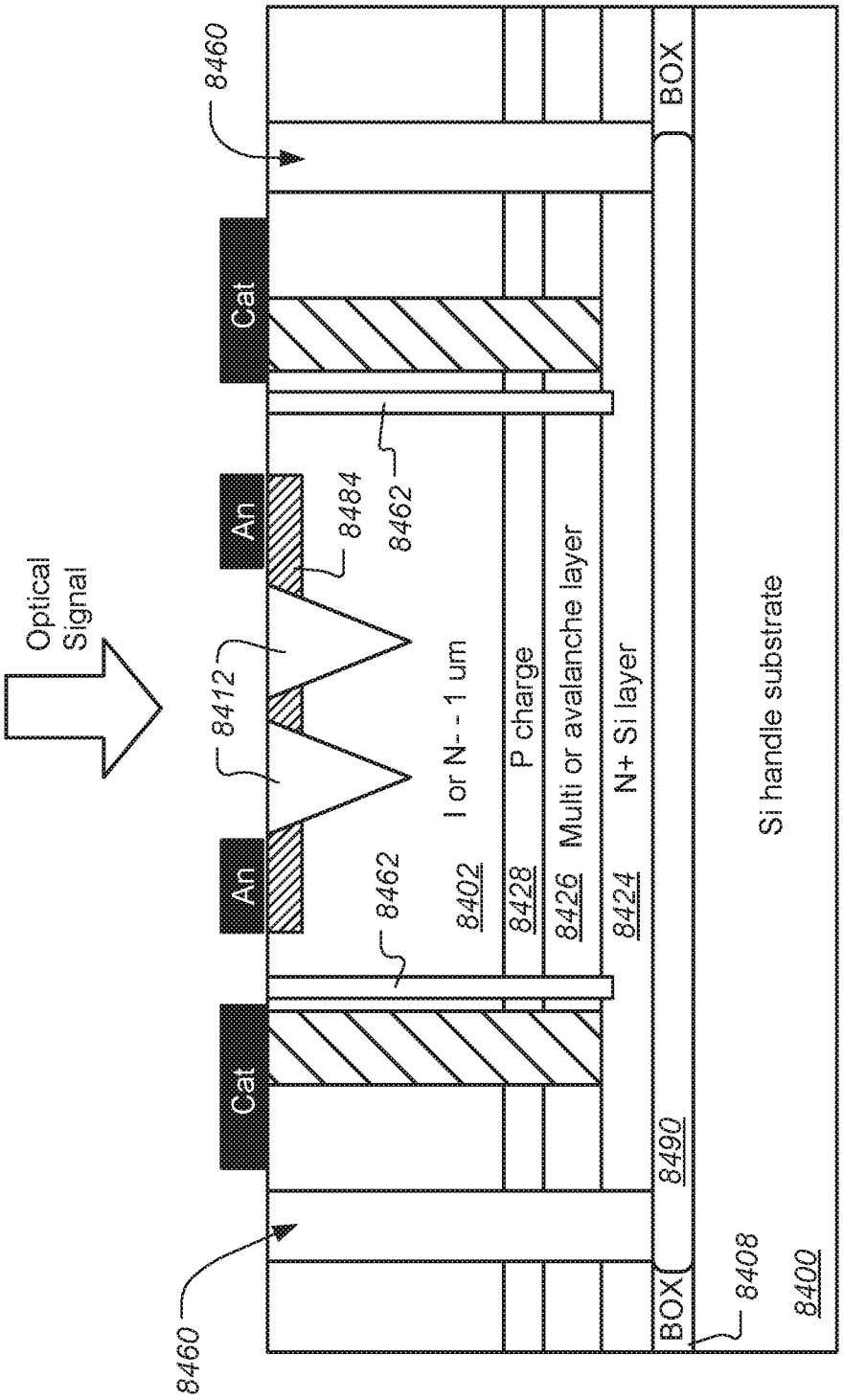

8460
BOX
Cat
An
8484
8462
Optical Signal
8412
I or N- - 1 um
8402
P charge
8428
Multi or avalanche layer
8426
N+ Si layer
8424
Si handle substrate
8462
Cat
8490
8460
BOX
8408
8400

FIG. 84B

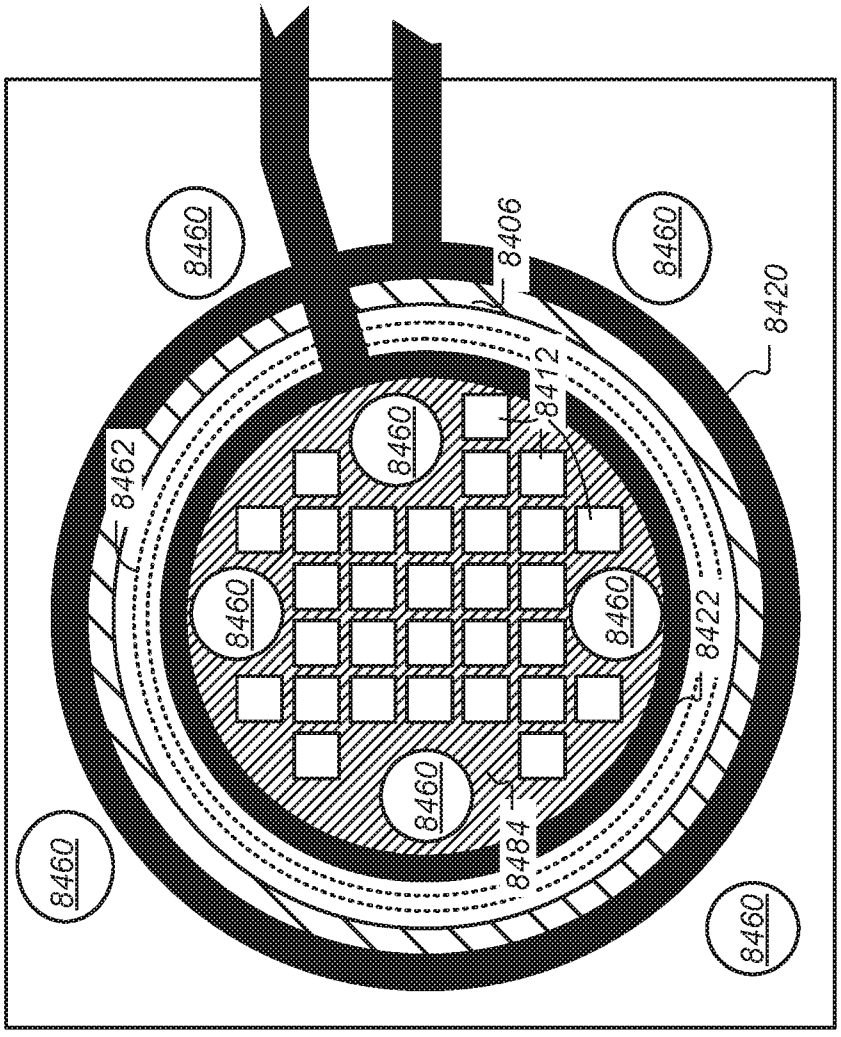

8460
8406
8460
8420
8412
8462
8460
8460
8422
8460
8484
8460
8460

FIG. 85

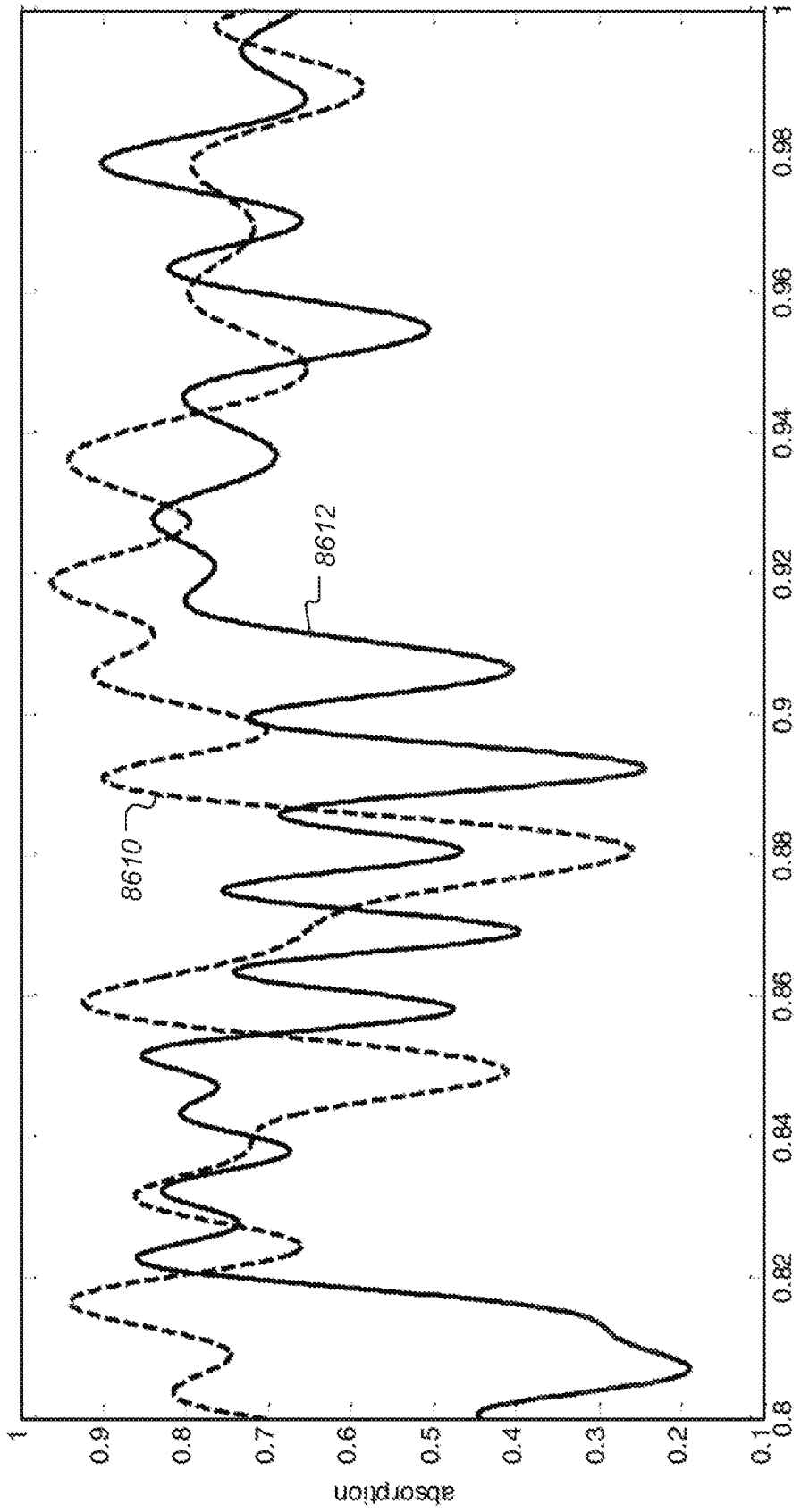

absorption
wavelength, um
8610
8612
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.8
0.82
0.84
0.86
0.88
0.9
0.92
0.94
0.96
0.98
1

FIG. 86

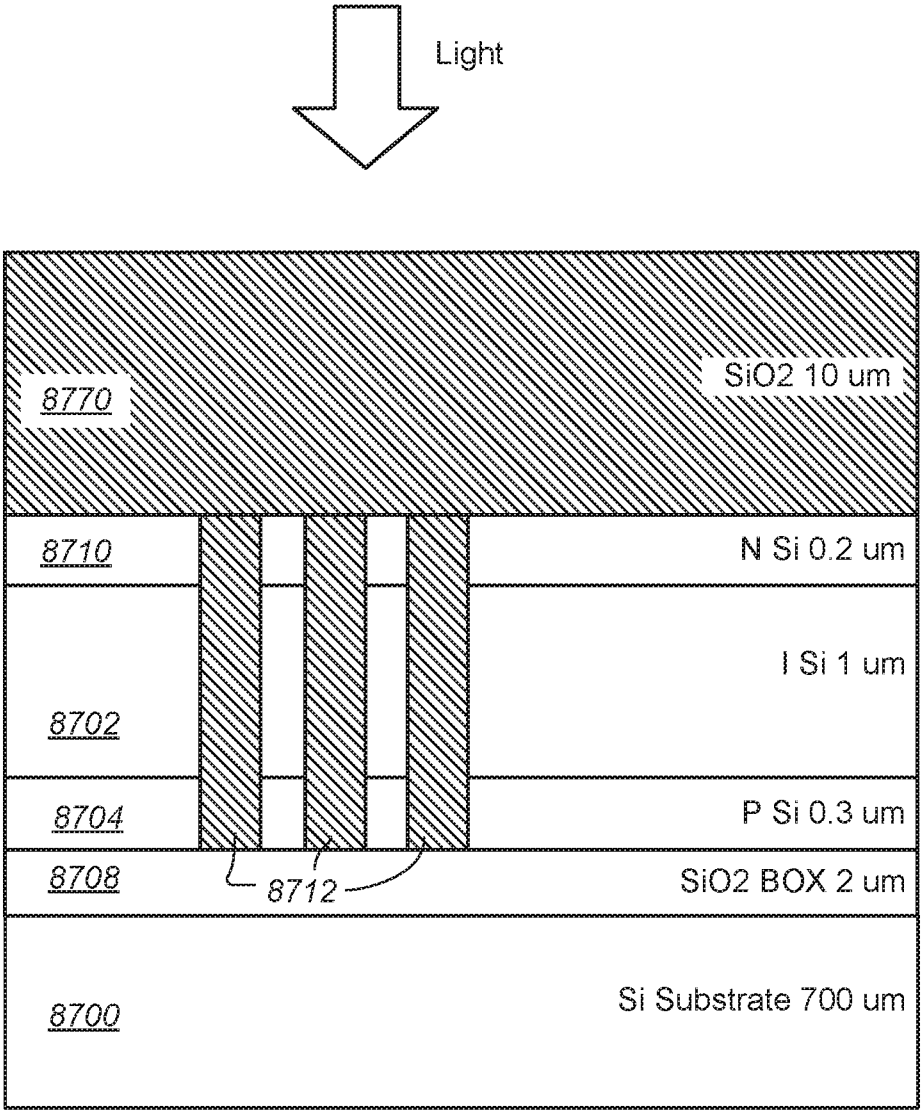

Light
8770
SiO2 10 um
8710
N Si 0.2 um
I Si 1 um
8702
8704
P Si 0.3 um
8708
8712
SiO2 BOX 2 um
8700
Si Substrate 700 um

FIG. 87

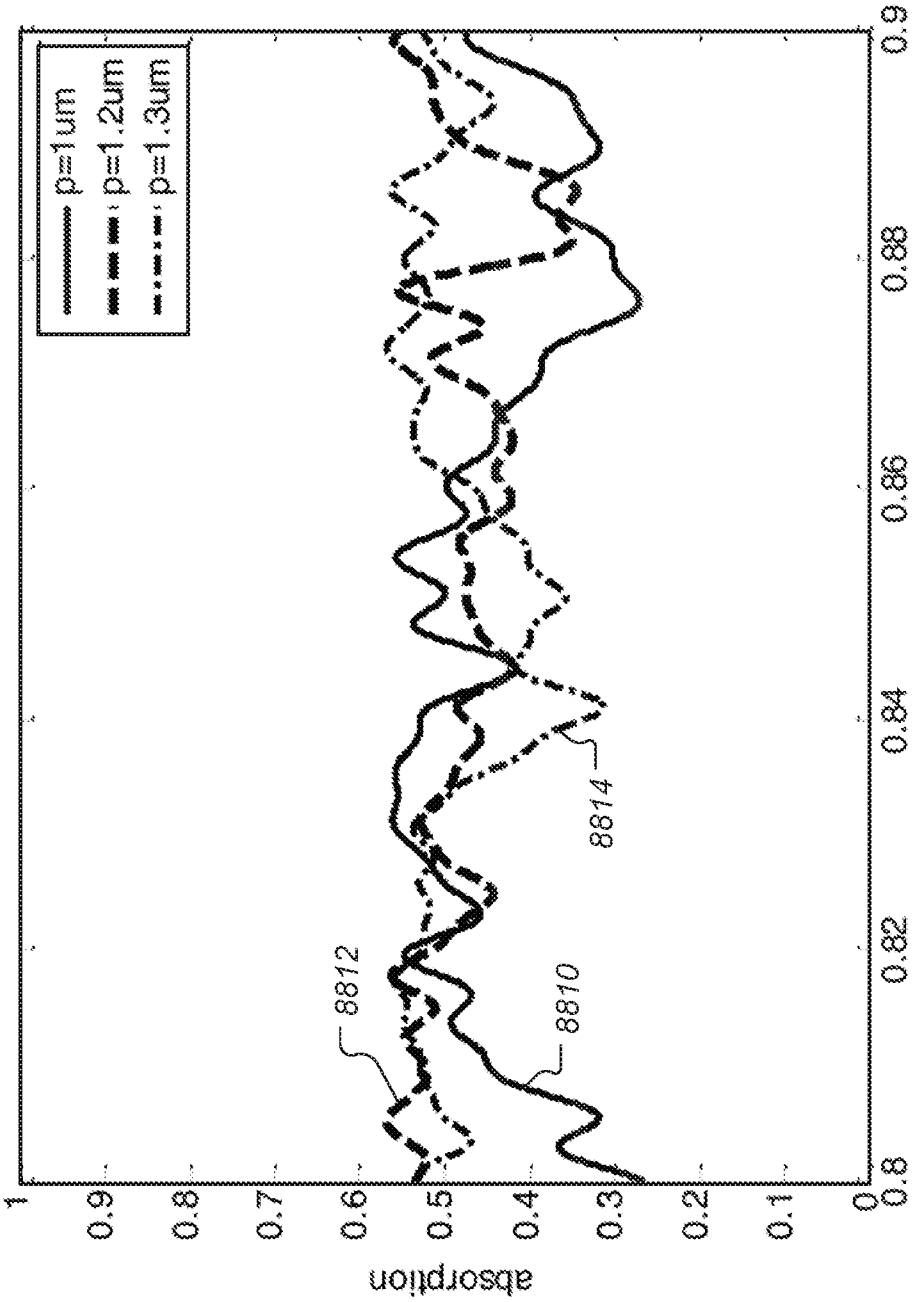

p=1um
p=1.2um
p=1.3um
8812
8810
8814
absorption
wavelength, um
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.82
0.84
0.86
0.88
0.9

FIG. 88

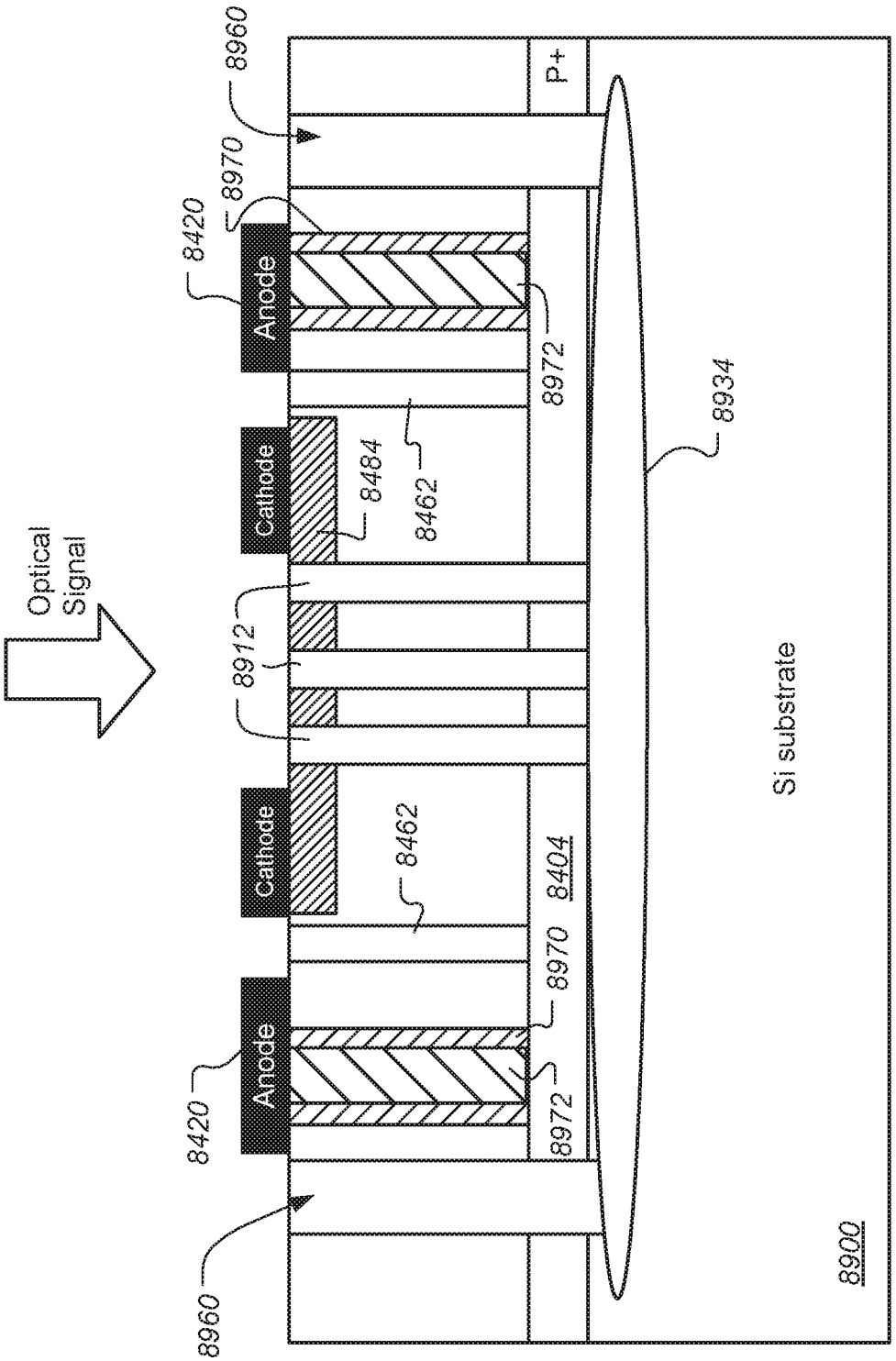

Optical Signal
8960
8970
8420
Anode
Cathode
Cathode
Anode
8420
8960
8912
8484
8462
8462
8404
8970
8972
8972
P+
8934
Si substrate
8900

FIG. 89

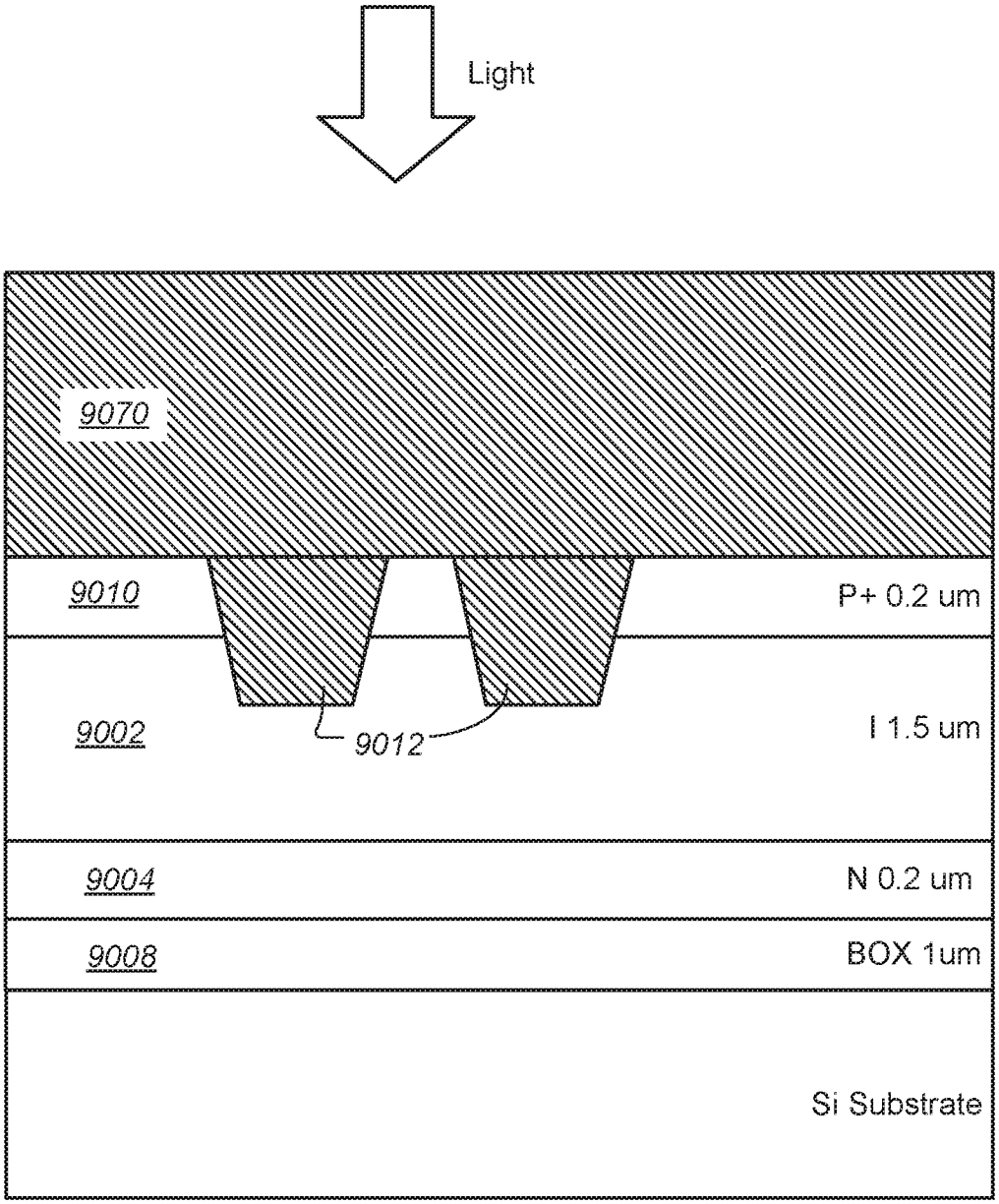

Light
9070
9010
P+ 0.2 um
9002
I 1.5 um
9012
9004
N 0.2 um
9008
BOX 1um
Si Substrate

FIG. 90

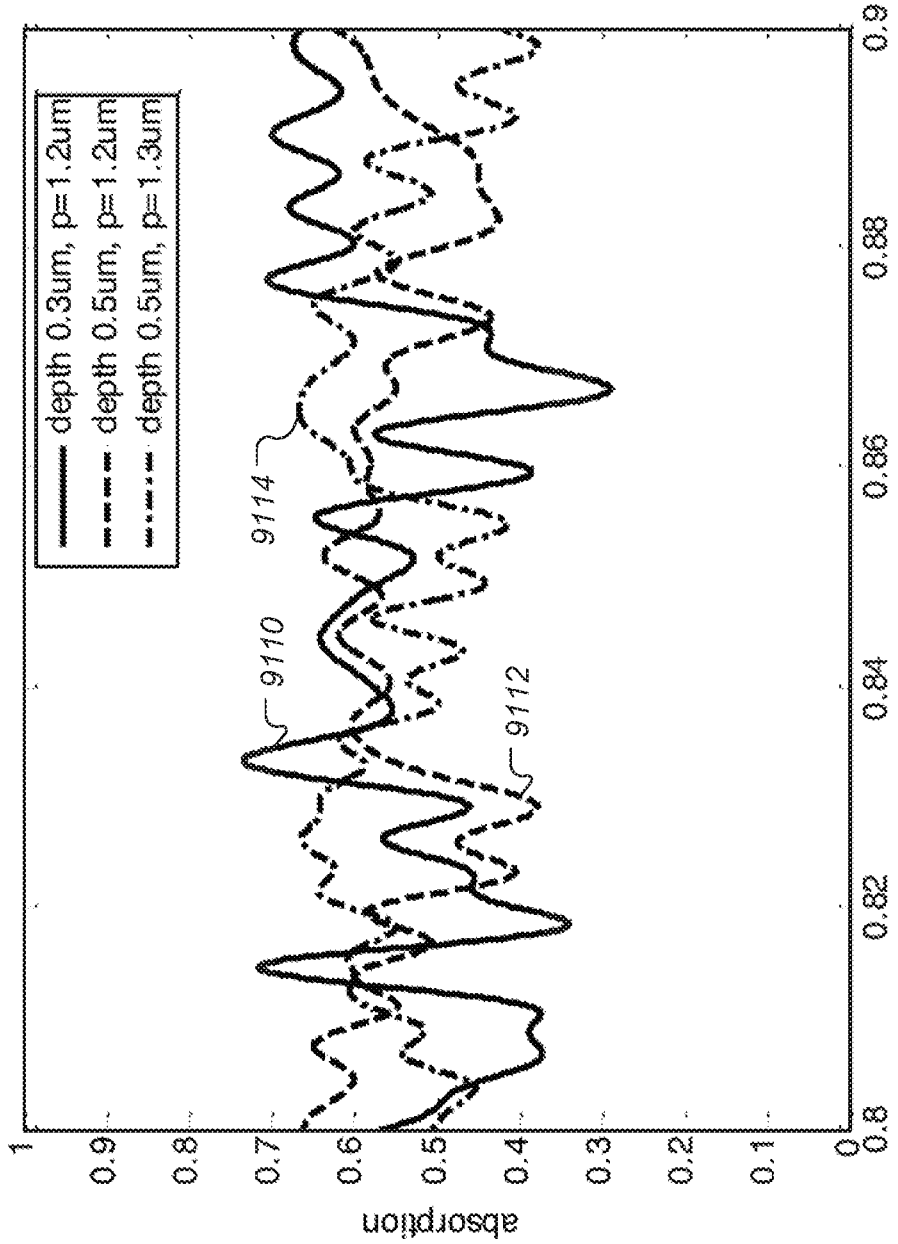

depth 0.3um, p=1.2um
depth 0.5um, p=1.2um
depth 0.5um, p=1.3um
9110
9112
9114
absorption
wavelength, um
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0.8
0.82
0.84
0.86
0.88
0.9

FIG. 91

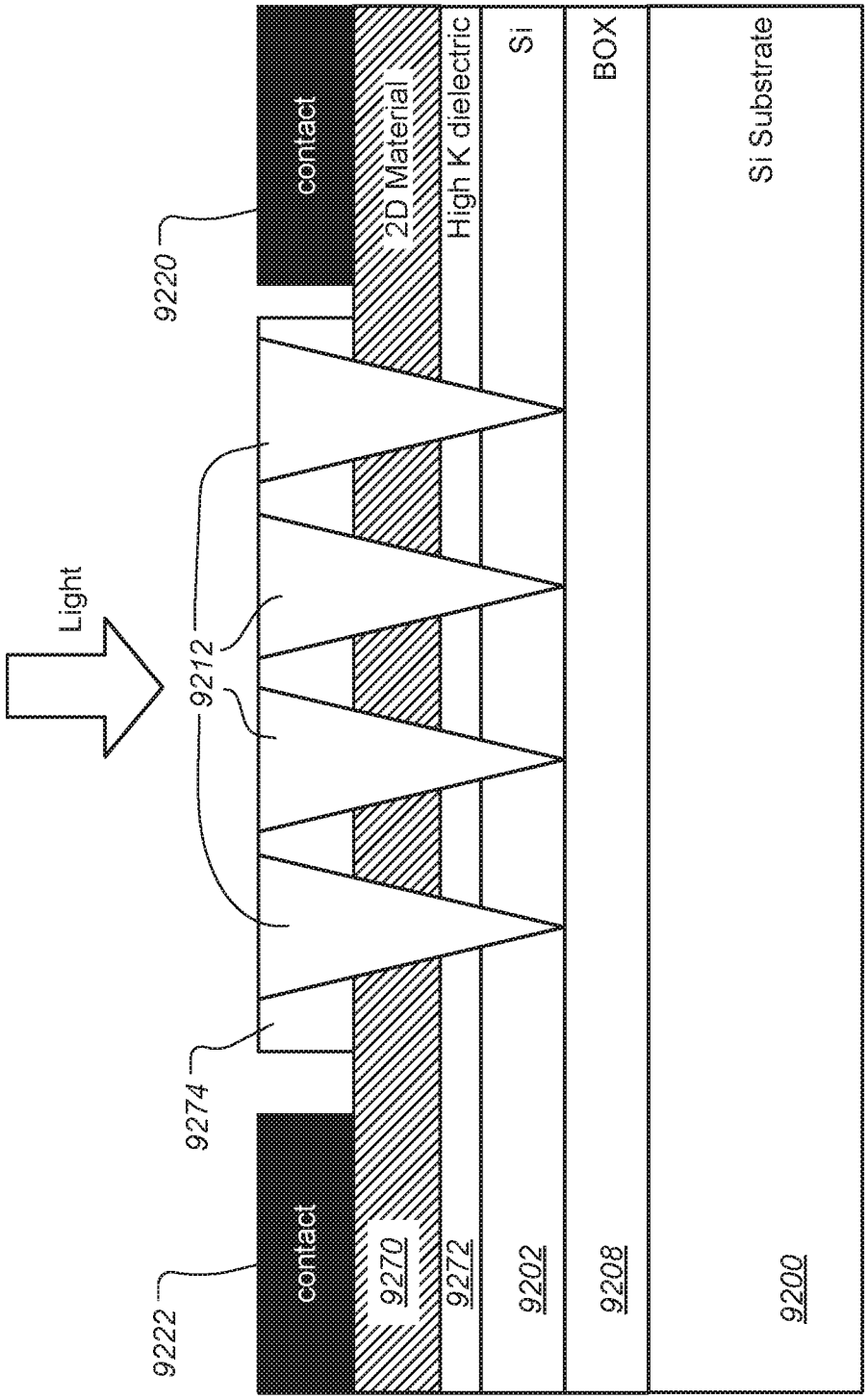

Light
9212
9220
9222
9274
contact
contact
2D Material
High K dielectric
Si
BOX
Si Substrate
9270
9272
9202
9208
9200

FIG. 92

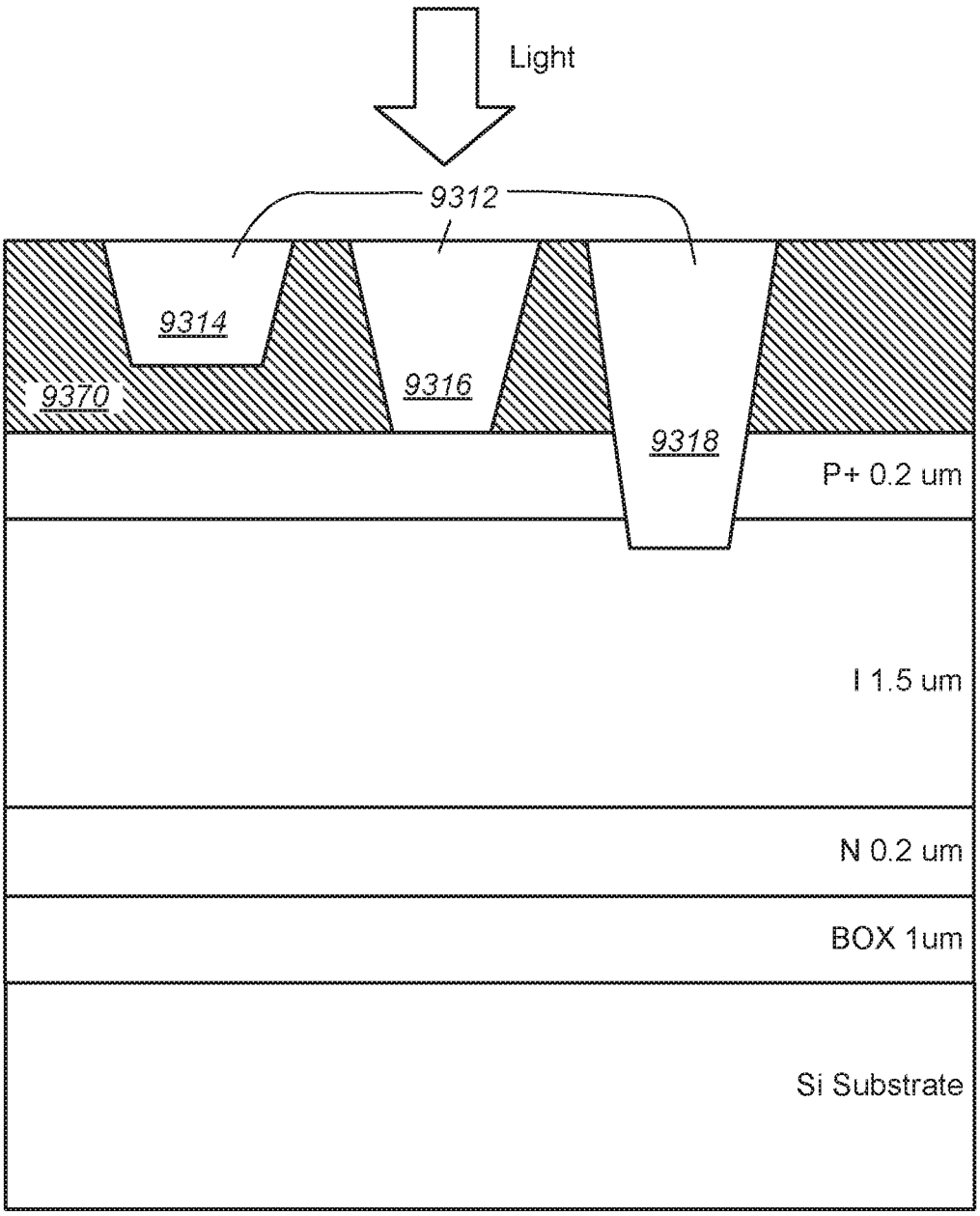

Light
9312
9314
9316
9318
9370
P+ 0.2 um
I 1.5 um
N 0.2 um
BOX 1um
Si Substrate

FIG. 93

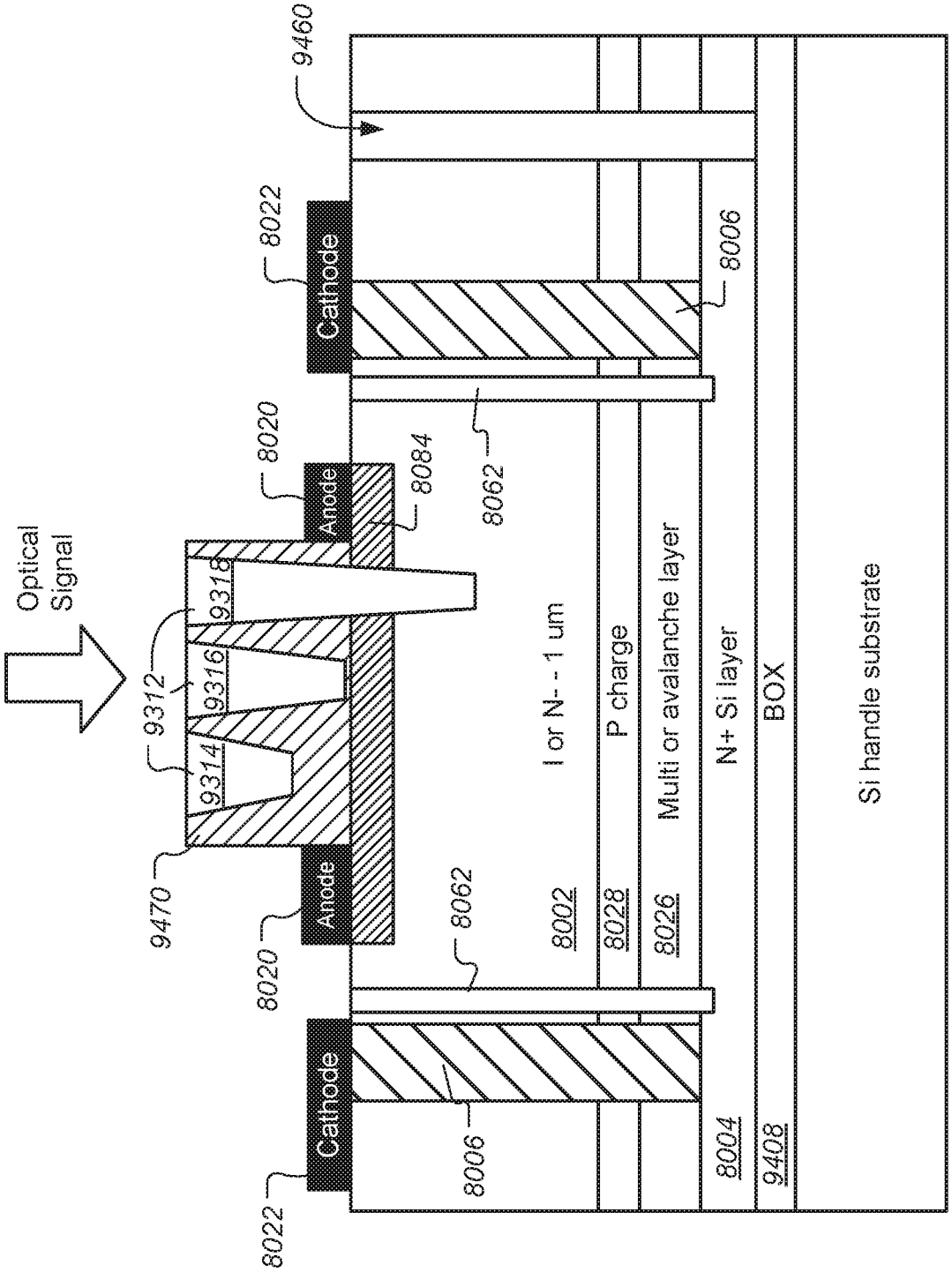

Optical Signal
9460
8022
Cathode
8006
8020
Anode
8084
8062
9318
9312
9316
9314
9470
I or N- - 1 um
P charge
Multi or avalanche layer
N+ Si layer
BOX
Si handle substrate
8002
8028
8026
8004
9408

FIG. 94

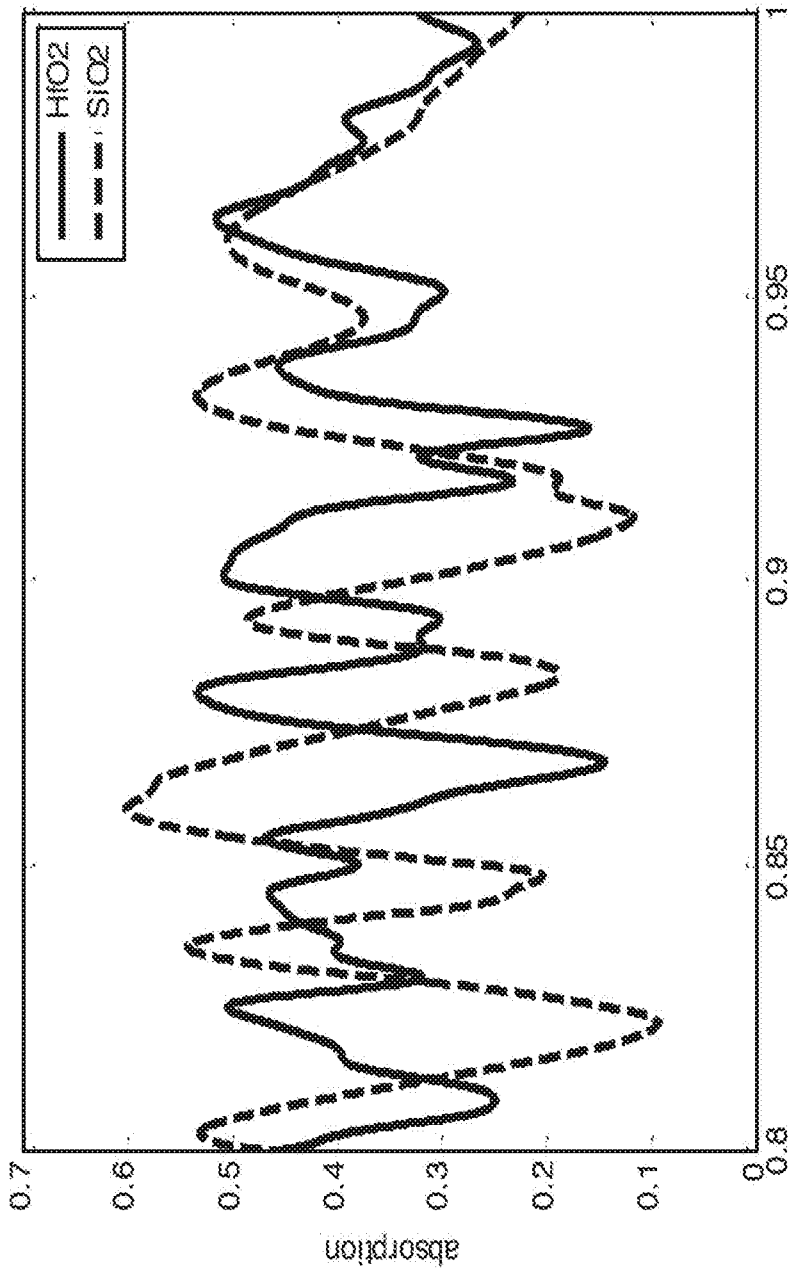

HfO2
SiO2
absorption
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.8
0.85
0.9
0.95
1
wavelength, um

FIG. 95A

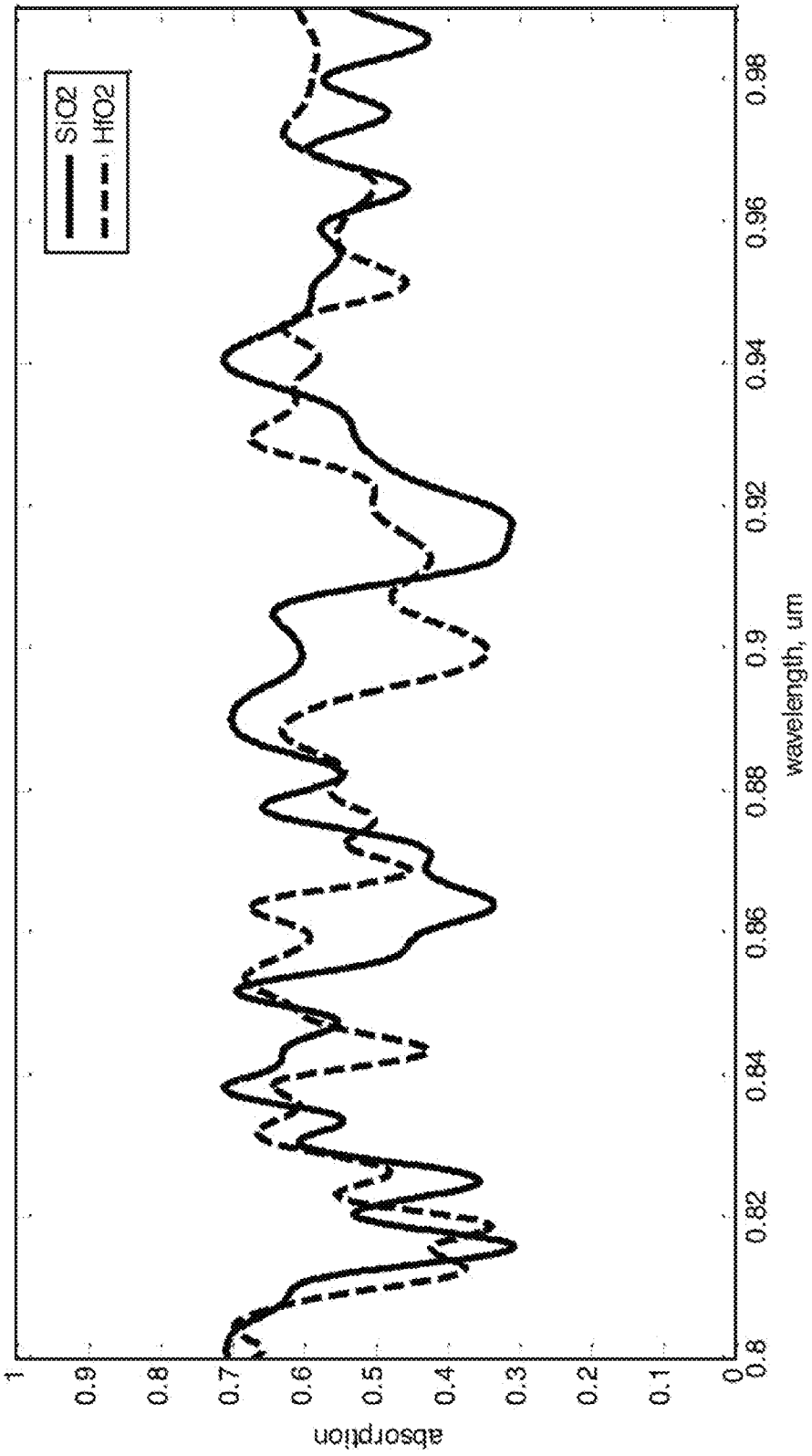

SiO2
HfO2
absorption
wavelength, um
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.82
0.84
0.86
0.88
0.9
0.92
0.94
0.96
0.98

FIG. 95B

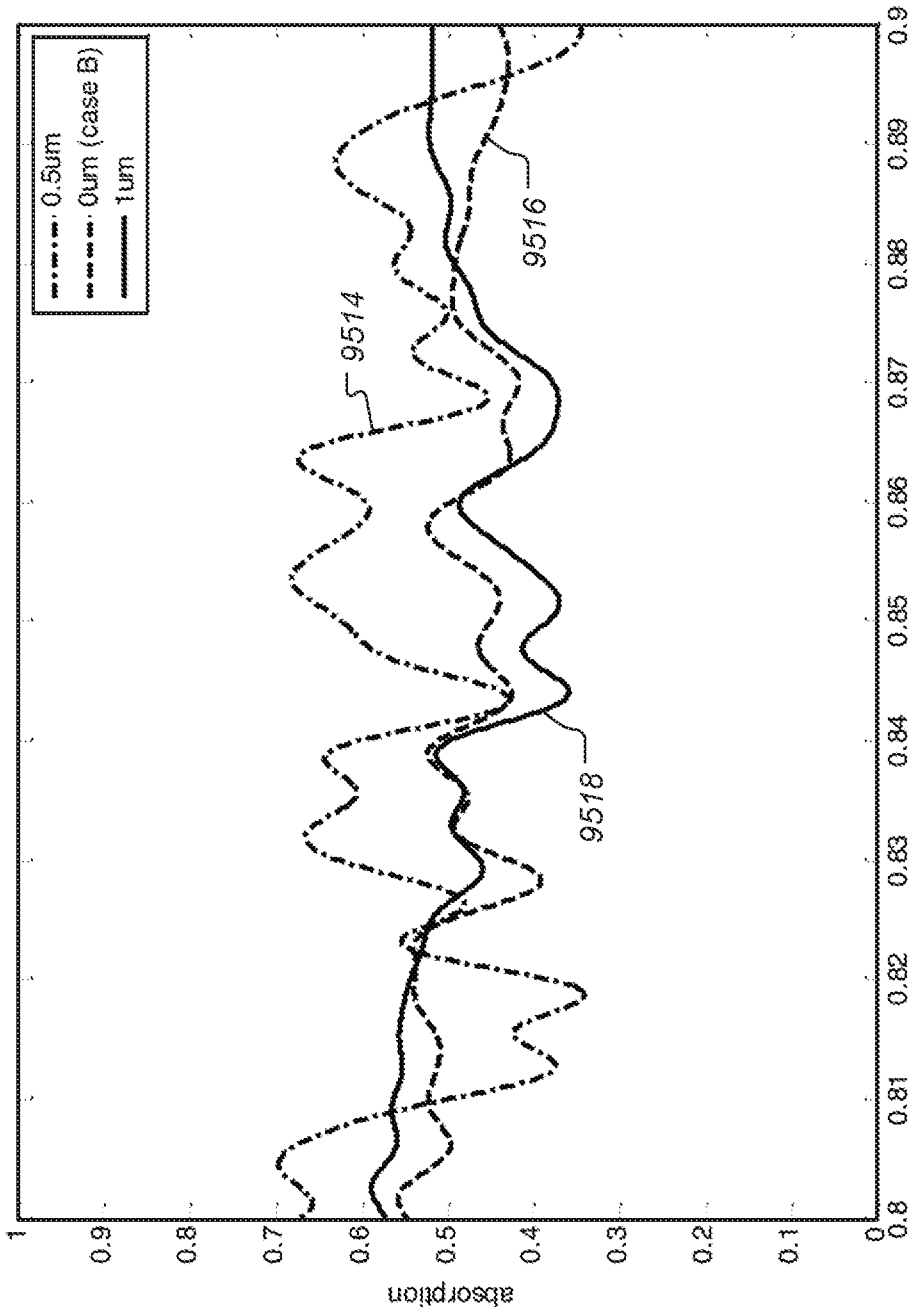

0.5um
0um (case B)
1um
9514
9516
9518
absorption
wavelength, um
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.81
0.82
0.83
0.84
0.85
0.86
0.87
0.88
0.89
0.9

FIG. 95C

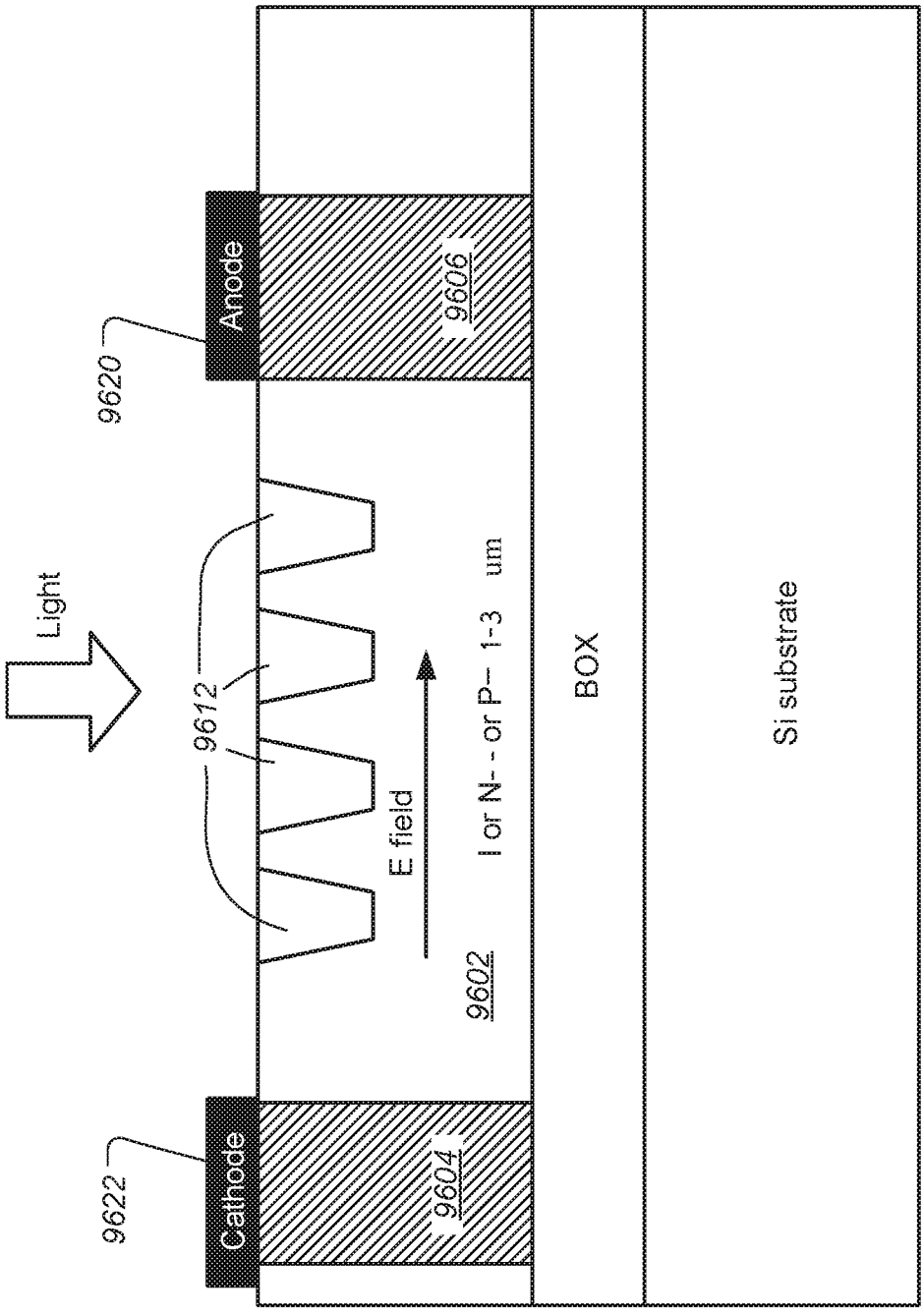

Light
9620
Anode
9606
9612
E field
9602
I or N- - or P- 1-3 um
BOX
Si substrate
9622
Cathode
9604

FIG. 96

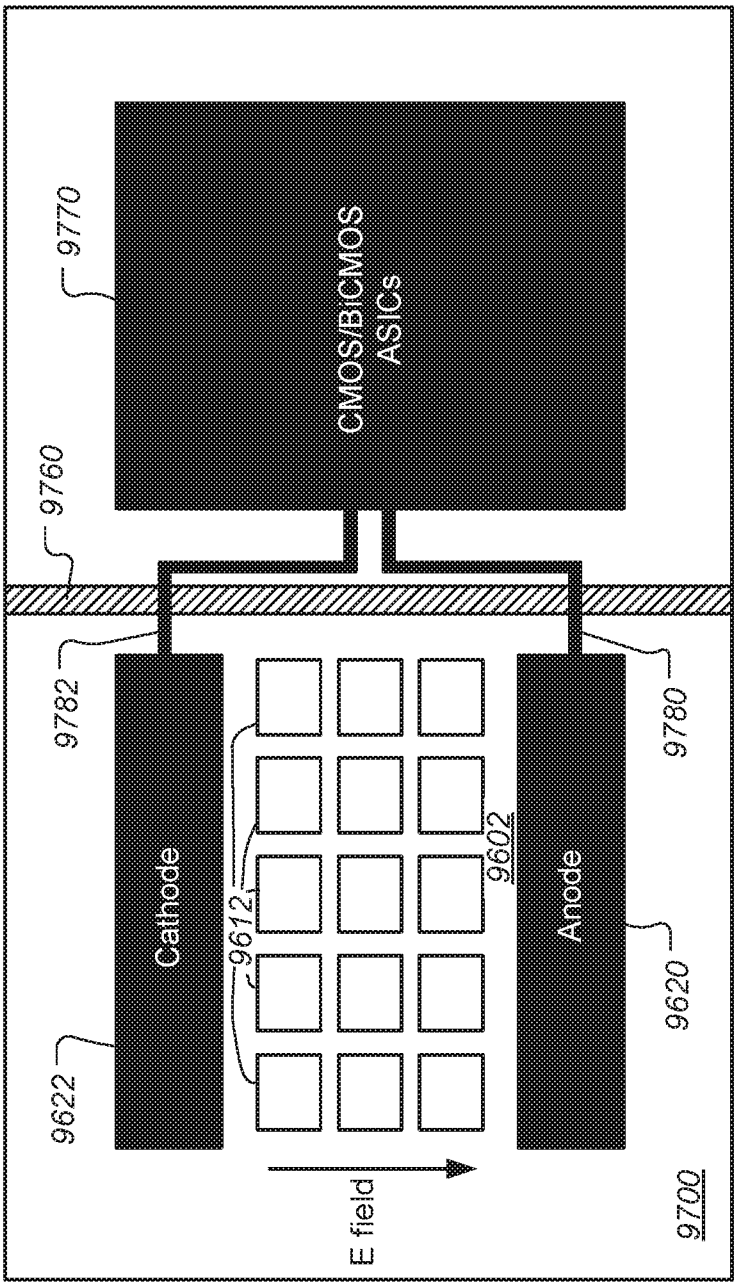

9770
CMOS/BiCMOS
ASICs
9760
9782
9780
Cathode
9602
9612
Anode
9620
9622
E field
9700

FIG. 97

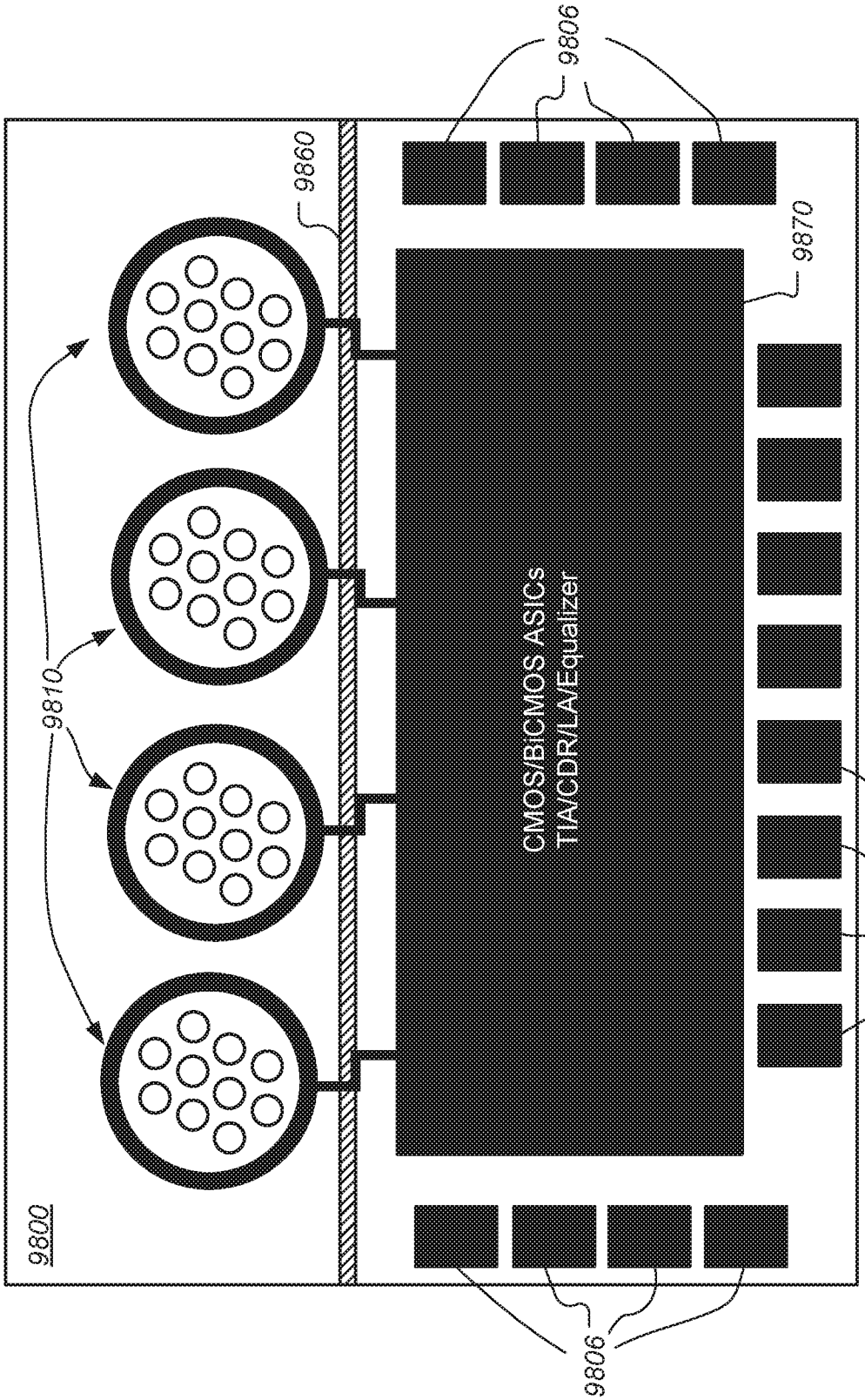

9806
9860
9870
9810
CMOS/BiCMOS ASICs
TIA/CDR/LA/Equalizer
9800
9806
9806

FIG. 98

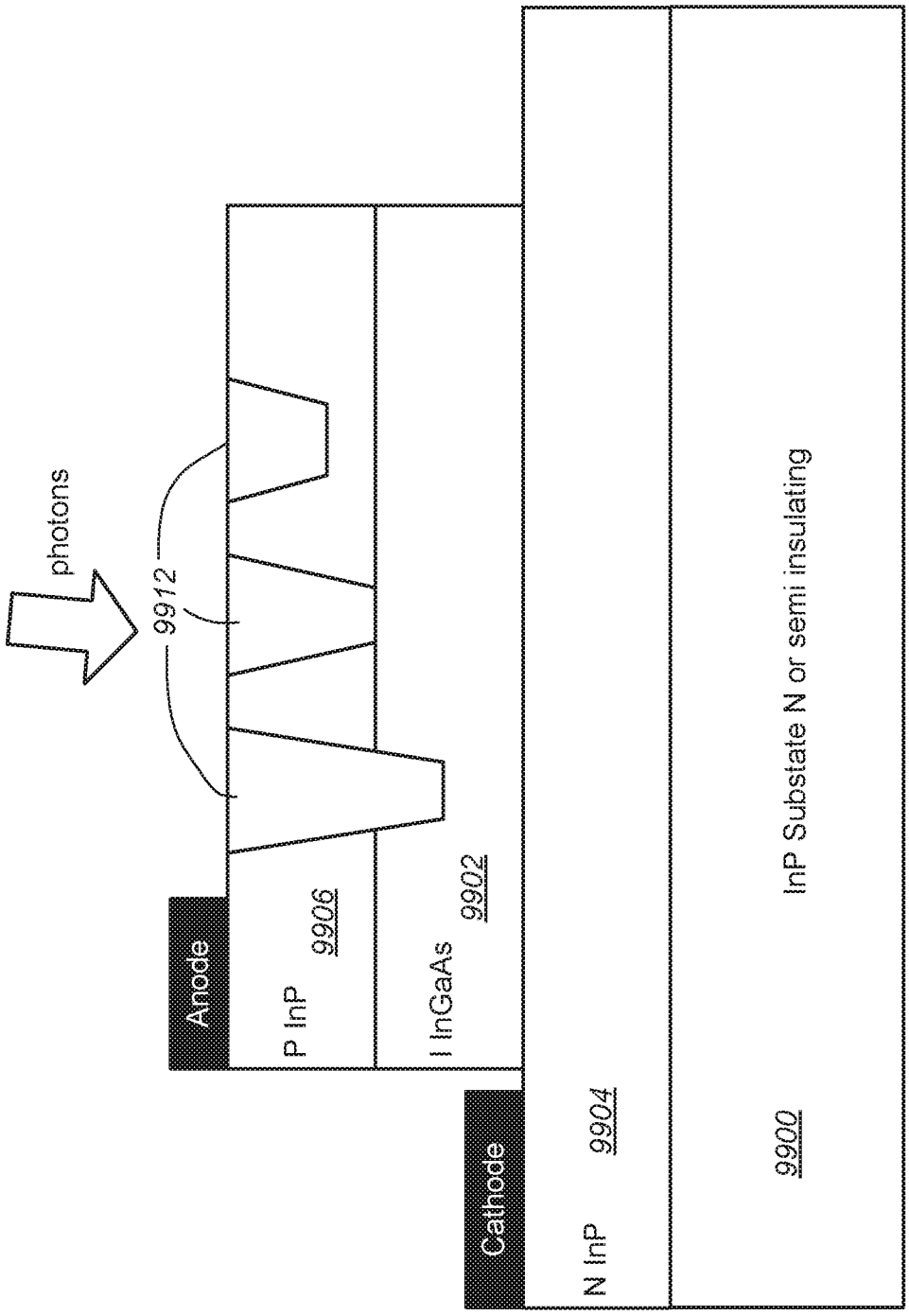

photons
9912
Anode
P InP
9906
I InGaAs
9902
Cathode
N InP
9904
InP Substate N or semi insulating
9900

FIG. 99A

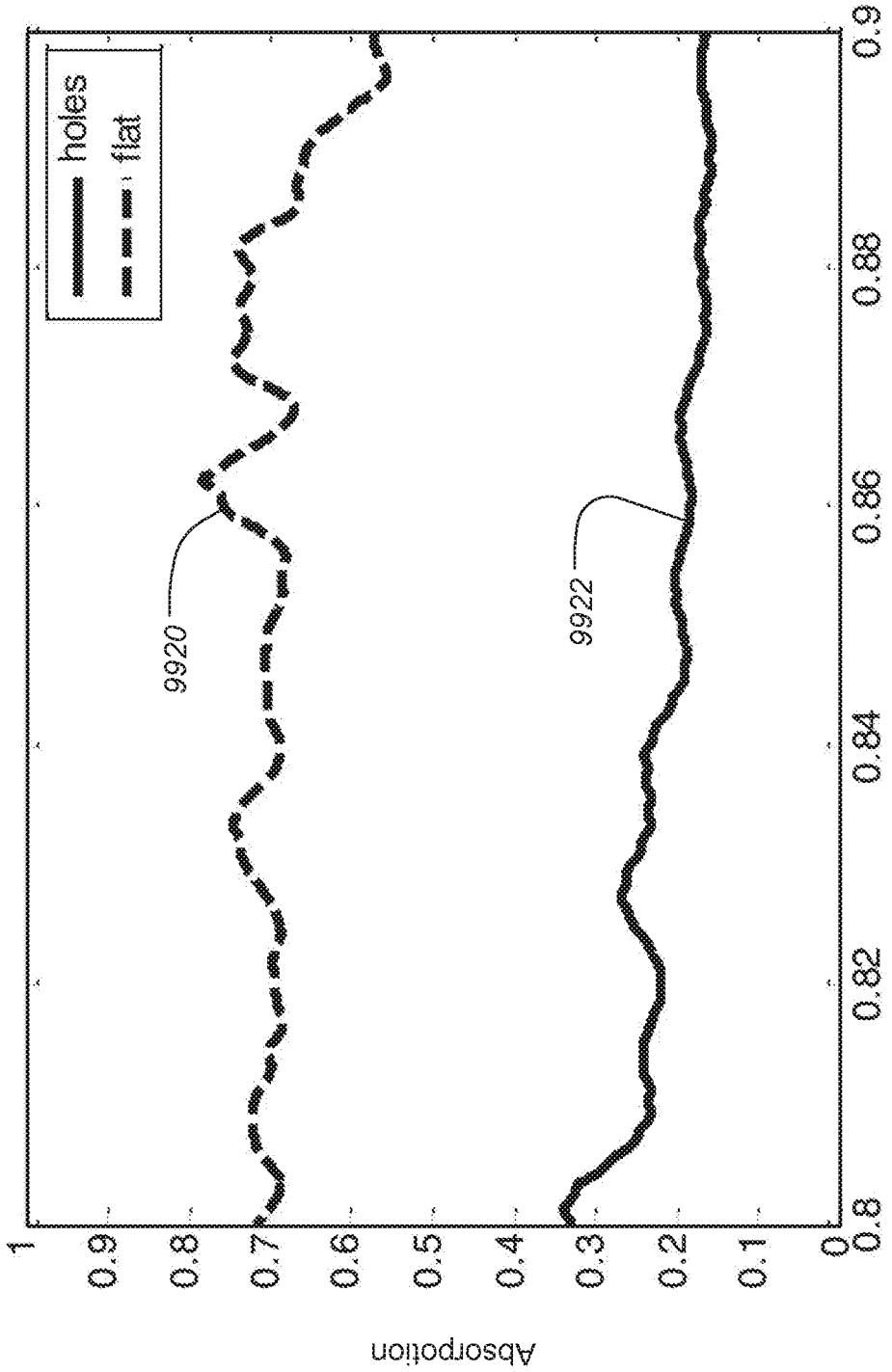

holes
flat
9920
9922
Absorption
wavelength, um
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.82
0.84
0.86
0.88
0.9

FIG. 99B

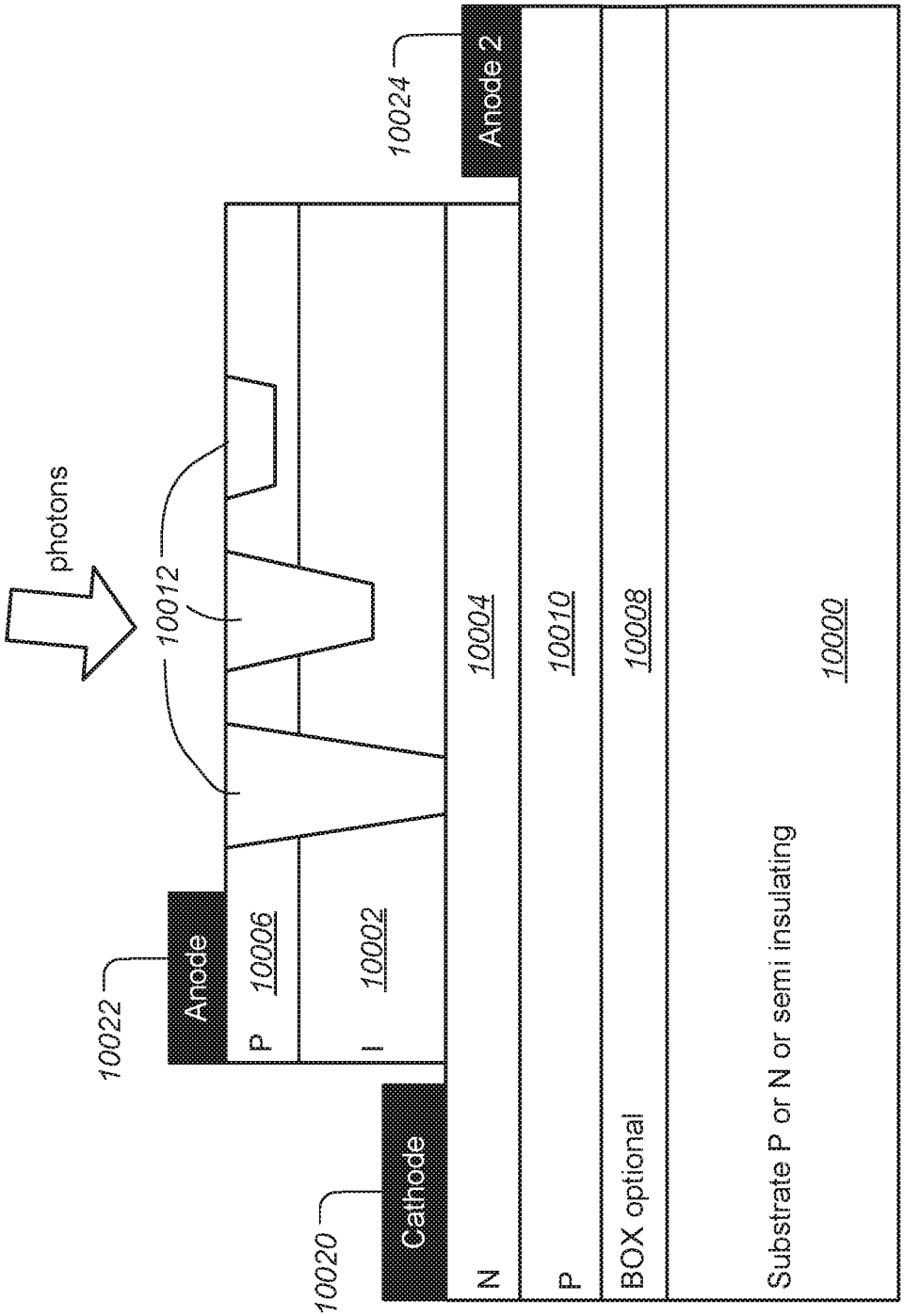

photons
10012
10022
Anode
P 10006
I 10002
10024
Anode 2
10020
Cathode
N 10004
P 10010
BOX optional 10008
Substrate P or N or semi insulating 10000

FIG. 100

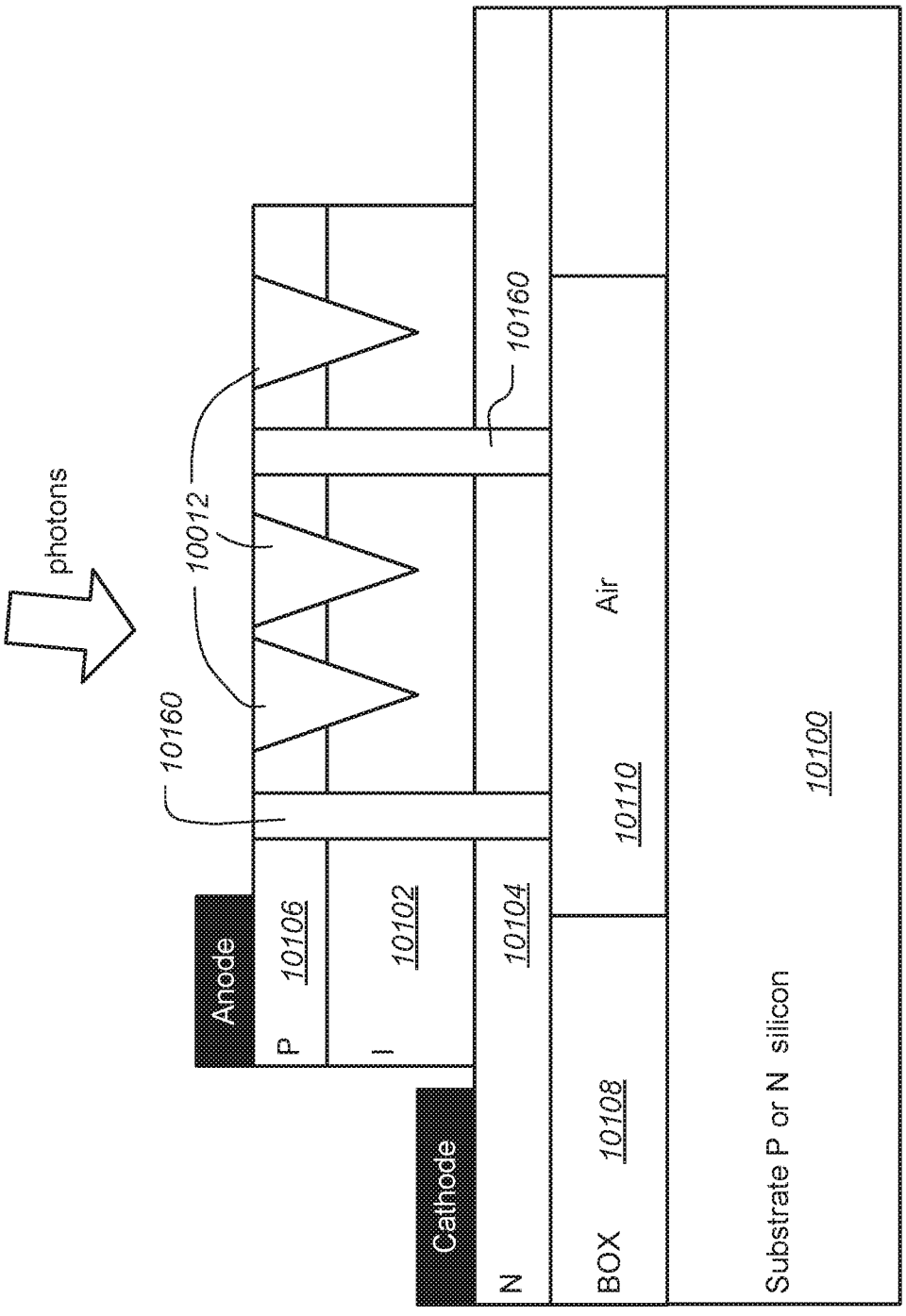

photons
10012
10160
10160
Anode
P
10106
I
10102
N
10104
Cathode
BOX
10108
10110
Air
Substrate P or N silicon
10100

FIG. 101

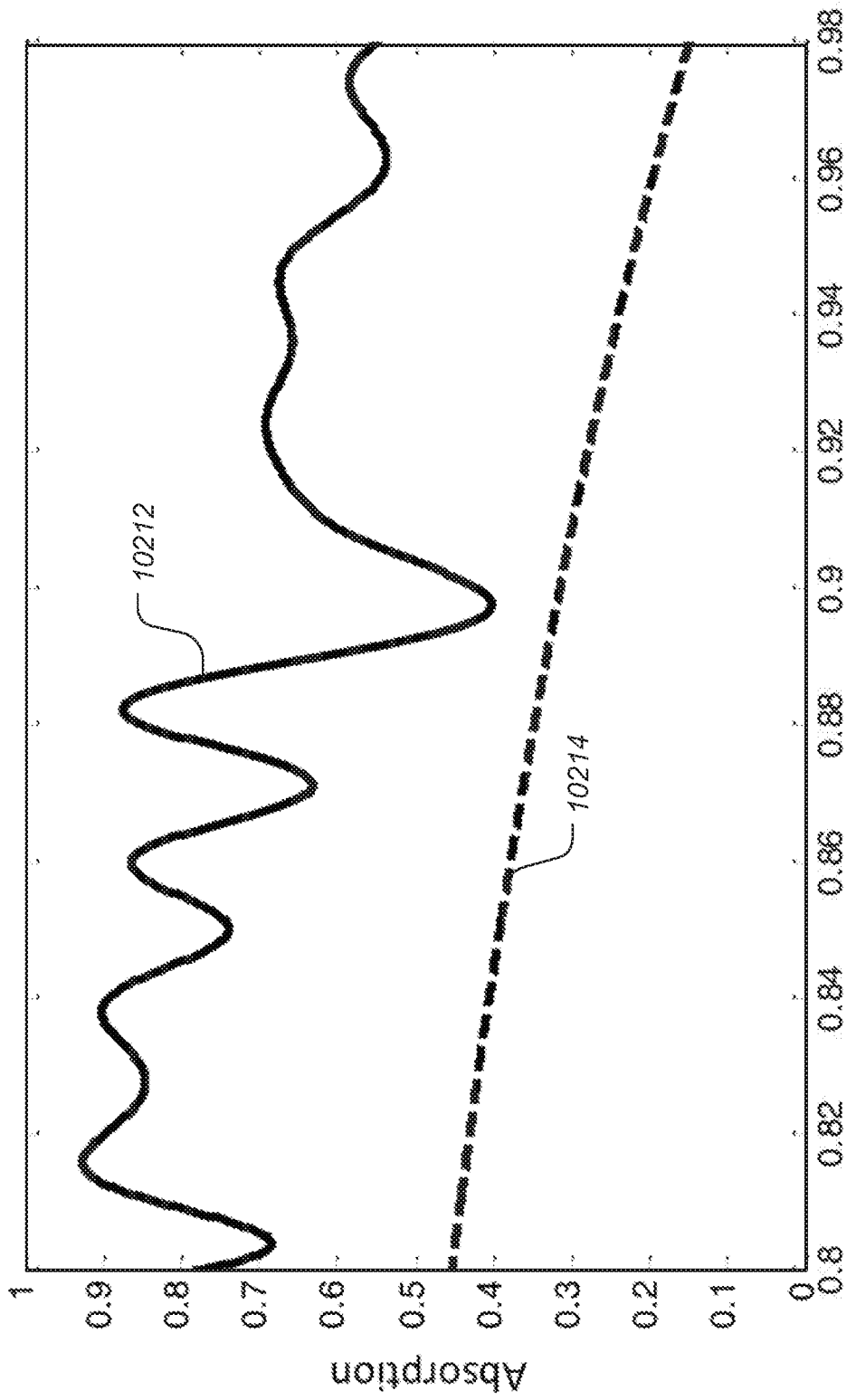

Absorption
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.8
0.82
0.84
0.86
0.88
0.9
0.92
0.94
0.96
0.98
wavelength, um
10212
10214

FIG. 102

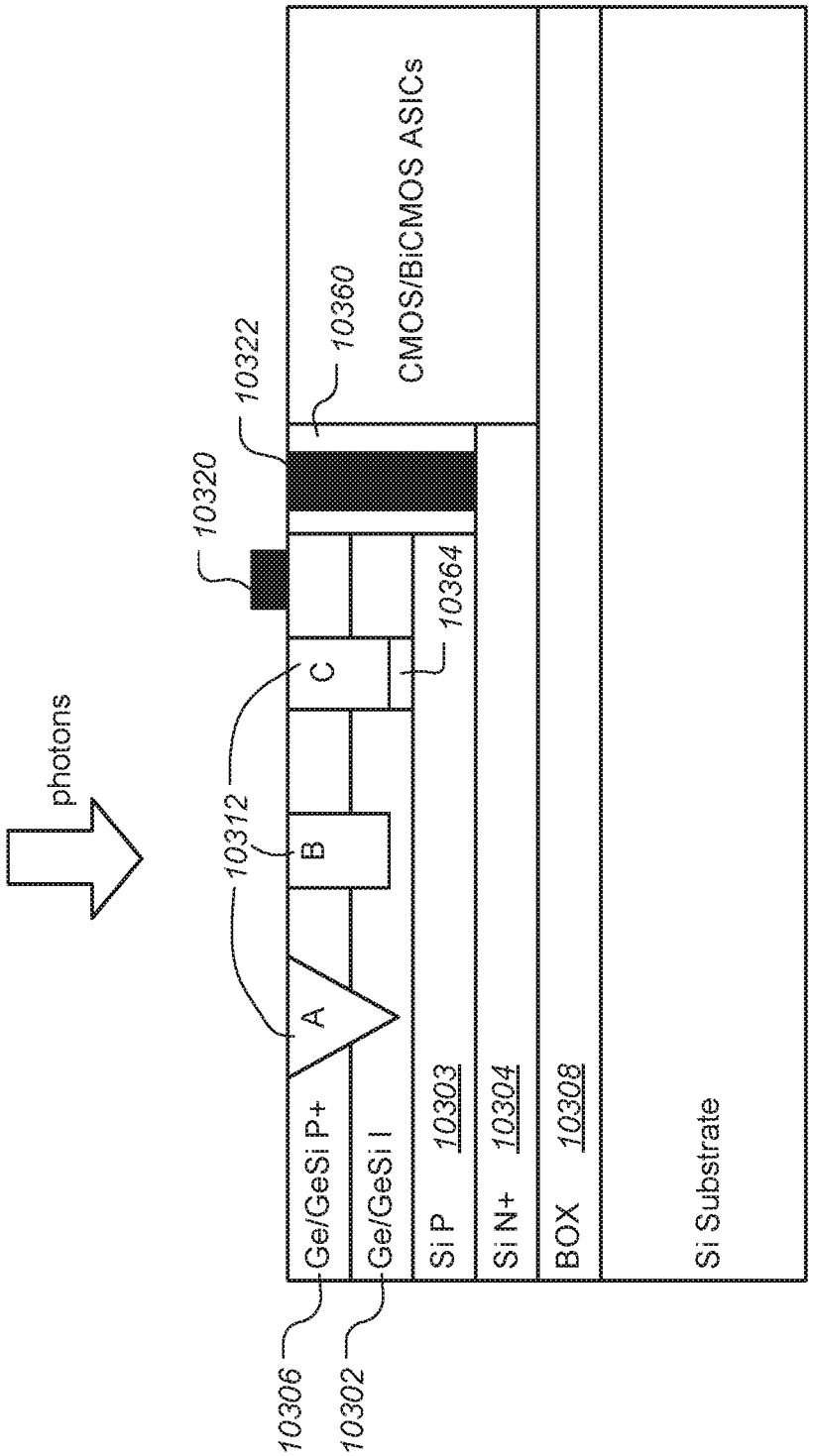

photons
10312
10320
10322
10360
CMOS/BiCMOS ASICs
10364
A
B
C
Ge/GeSi P+
Ge/GeSi I
Si P 10303
Si N+ 10304
BOX 10308
Si Substrate
10306
10302

FIG. 103

ABSTRACT

Microstructure enhanced photodiodes and avalanche photodiodes are monolithically integrated with CMOS/BiCMOS circuitry such as transimpedance amplifiers. Microstructures, such as holes, can improve quantum efficiency in silicon and III-V materials and can also reduce avalanche voltages for avalanche photodiodes. Applications include optical communications within and between datacenters, telecommunications, LIDAR, and free space data communication.

CLAIMS

1. A single-chip device comprising an integrated combination of a microstructure-enhanced photodetector (MSPD) and an active electronic circuit, both formed on or in a single substrate and configured to receive an optical input that in cross-section is substantially continuous spatially at least some of time, convert the optical input to an electrical output, and process the electrical output into a processed output, wherein:

the MSPD on or in said single substrate comprises an intermediate layer, a first layer at one side of the intermediate layer, and a second layer at an opposite side of the intermediate layer, wherein:

each of the layers comprises Silicon, Germanium, or an alloy thereof;

at least one of said layers, or an overlying covering layer that may be present, has holes intentionally formed therein, extending in directions transverse to the layers;

each of the first and second layers comprises a doped material;

the intermediate layer comprises a material that is less doped than at least one of the first and second layers or is undoped, wherein the degree of doping is the same or different for different positions in the intermediate layer;

an input portion configured to concurrently receive at a plurality of said holes said optical input that has said substantially continuous cross-section; and

an output portion configured to provide said electrical output from the MSPD; and

the active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:

amplification to form said processed output from the single-chip device;

processing other than or in addition to amplification to form said processed output from the single-chip device; and

routing to one or more selected destinations; and

a communication channel on or in said single-chip device, configured to deliver the electrical output from the MSPD to the active electronic circuit.

2. The single-chip device of claim 1, in which said active electronic circuit is at least partly extends beyond said substrate.

3. The single-chip device of claim 1, in which said active electronic circuit is at least partly inside said substrate.

4. The single-chip device of claim 1, in which said overlying layer is present as a superstrate at one side of said first, intermediate, and second layers, and contains said holes.

5. The single-chip device of claim 1, in which said MSPD comprises a III-V materials family photodiode.

6. The single-chip device of claim 1, further including an air-filled volume between the substrate and the MSPD.

7. The single-chip device of claim 1, further including a layer of a dielectric material that covers the holes and is in the propagation path of said optical input.

8. The single-chip device of claim 1, further including an avalanche region at one side of the MSPD, forming therewith an avalanche microstructured photodiode (MSAPD).

9. The single-chip device of claim 1, in which said holes are present in said intermediate layer.

10. The single-chip device of claim 1, in which said holes are present in said intermediate layer as well as in at least one of the first and second layers.

11. The single-chip device of claim 1, in which said holes are present in each of the first, second, and intermediate layer.

12. The single-chip device of claim 1, in which each of said first and second layers and said intermediate layer has a thickness and at least some of said holes extend through the entire thickness of said intermediate layer and of one of said first layer and second layer and through at least a part of the thickness of the other one of said first and second layers.

13. The single-chip device of claim 1, in which at least some of said holes are shaped as inverted pyramids.

14. The single-chip device of claim 1, in which at least some of said holes have triangular sections in planes transverse to said layers.

15. The single-chip device of claim 1, in which at least some of said holes have triangular sections in planes transverse to said layers, with vertices within the intermediate layer.

16. The single-chip device of claim 1, in which at least some of said holes have sidewalls that slope in planes transverse to said layers.

17. The single-chip device of claim 1, in which at least some of said holes have sidewalls with plural different slopes along the inside walls of the holes.

18. The single-chip device of claim 1, in which at least some of said holes differ from each other in at least one of (i) distance by which the holes extend in said directions, (ii) shape of the holes, and (iii) spacing of the holes from each other.

19. The single-chip device of claim 1, in which the holes are in the intermediate layer and wherein one of said first and second layers conformally covers inside walls of the holes as well as spaces between the holes.

20. The single-chip device of claim 1, in which the holes are at least partly filled with a dielectric material.

21. The single-chip device of claim 1, in which the holes are entirely filled with a dielectric material.

22. The single-chip device of claim 1, in which said optical input enters the MSPD through one or both of said first and second layers, and each of the first and second layers through which the optical input enters is no more than 500 nanometers thick.

23. The single-chip device of claim 1, in which at least one of the first layer, the second layer, and the intermediate layer comprises a material represented by $Ge_x Si_{1-x}$, where x is greater than zero.

24. The single-chip device of claim 1, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD.

25. The single-chip device of claim 1, in which the MSPD further includes ohmic contacts to said first and second layers, at least one of said ohmic contact being through a via in said substrate.

26. The single-chip device of claim 1, further comprising a light guide to said MSPD for directing said optical input thereto, and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip device.

27. The single-chip device of claim 1, further comprising a light guide to said MSPD configured to bend the optical input from an initial propagation direction to a propagation direction transverse to said layers, and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip device.

28. The single-chip device of claim 1, further comprising one or more additional MSPD on or in the same substrate, and respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input.

29. The single-chip device of claim 1, further comprising one or more additional MSPDs on or in said single substrate, one or more additional active electronic circuits on or in the said single substrate, and one or more additional communication channels configured to supply electrical outputs from the MSPDs to the one or more of the active electronic circuits.

30. The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate.

31. The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate and comprise one or more transimpedance amplifiers (TIAs) and one or more application specific integrated circuits (ASICs).

32. The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate and comprise one or more of CMOS, BiCMOS, and bipolar active devices.

33. The single-chip device of claim 1, further comprising one or more additional MSPDs in an array on or in said single substrate and one or more additional active electronic circuits also on or in said single substrate, said MSPDs and active electronic circuits being configured into an optical communication structure or a light distance and ranging (LIDAR) structure.

34. The single-chip device of claim 1, further comprising a laser emitter formed on or in said single substrate.

35. The single-chip device of claim 1, further including a layer of selected material that is over a side of one of the first and second layers facing away from the intermediate layer and is configured to reduce sheet resistance.

36. The single-chip device of claim 1, further including a layer of selected material that is over a side of one of the first and second layers facing away from the intermediate layer and is configured to reflect light that has passed through the intermediate layer back toward the intermediate layer.

37. The single-chip device of claim 1, further including a deliberately textured surface at a side of one of said first and second layers facing away from the intermediate layer.

38. The single-chip device of claim 1, further including a layer of micro-nano structures formed at of one of said first and second facing, at a surface thereof facing away from the intermediate layer.

39. The single-chip device of claim 1, further including one or more distributed Bragg reflectors formed at one of said first and second layers, at a surface thereof away from the intermediate layer.

40. The single-chip device of claim 1, further including an isolation trench between the MSPD and the active electronic circuit.

41. The single-chip device of claim 1, further including a light shield layer over said active electronic circuit.

42. The single-chip device of claim 1, wherein the optical input and the electrical output are each modulated at a frequency of at least 30 Gigabits per second.

43. The single-chip device of claim 1, wherein the quantum efficiency of the MSPD that is at least 1.5 times greater than that of an otherwise same photodetector that does not include said holes.

44. The single-chip device of claim 1, further including a hermetic seal integral with the device.

45. A microstructure-enhanced photodetector (MSPD) configured to convert to an electrical output an optical input that in cross-section is essentially continuous spatially at least some of the time, comprising:

a substrate and a top layer, a bottom layer, and an intermediate layer between the top and bottom layers formed on or in the substrate, wherein:

at least one of the layers has holes intentionally formed therein, extending in directions transverse to the layers;

each of the top and bottom layers comprises a doped material;

the intermediate layer comprises a material that is undoped or is less doped than the top or bottom layer, wherein the degree of doping is the same or different for different positions in the intermediate layer;

an input portion configured to receive, concurrently at a plurality of said holes, said optical input that has said essentially continuous cross-section; and

an output portion configured to provide said electrical output.

46. The MSPD of claim 45, in which the top layer is no more than 500 nm thick and the holes are at least in the top layer.

47. The MSPD of claim 45, further including an air-filled volume between the substrate and the MSPD.

48. The MSPD of claim 45, further including a layer of a dielectric material that is at a surface of said substrate, over the holes and spaces between the holes, and in the path of said optical input.

49. The MSPD of claim 45, further including an avalanche region under the MSPD, forming therewith an avalanche microstructured photodiode (MSAPD).

50. The MSPD of claim 45, in which said holes are present in said intermediate layer.

51. The MSPD of claim 45, in which said holes are present in said intermediate layer as well as in at least one of the top and bottom layers.

52. The MSPD of claim 45, in which said holes are present in each of the top, bottom, and intermediate layer.

53. The MSPD of claim 45, in which each of said top and bottom layers and said intermediate layer has a thickness and at least some of said holes extend through the entire thickness of said intermediate layer and of one of said top and bottom layers and through at least a part of the thickness of the other one of said top and bottom layers.

54. The MSPD of claim 45, in which at least some of said holes are shaped as inverted pyramids.

55. The MSPD of claim 45, in which at least some of said holes have triangular sections in planes transverse to said layers.

56. The MSPD of claim 45, in which at least some of said holes have triangular sections in planes transverse to said layers, with vertices within the intermediate layer.

57. The MSPD of claim 45, in which at least some of said holes have sidewalls that slope in planes transverse to said layers.

58. The MSPD of claim 45, in which at least some of said holes have sidewalls with plural different slopes along inside walls of the holes.

59. The MSPD of claim 45, in which at least some of said holes differ from each other in at least one of (i) distance by which the holes extend in said directions, (ii) shape of the holes, and (iii) spacing of the holes from each other.

60. The MSPD of claim 45, in which the holes are in the intermediate layer and wherein one of said top and bottom layers conformally covers inside walls of the holes as well as spaces between the holes.

61. The MSPD of claim 45, in which the holes are at least partly filled with a dielectric material.

62. The MSPD of claim 45, in which the holes are entirely filled with a dielectric material.

63. The MSPD of claim 45, in which at least one of the top and bottom layers and the intermediate layer comprises a material represented by $Ge_x Si_{1-x}$, where x is greater than zero but less than unity.

64. The MSPD of claim 45, in which at least one of the top and bottom layers and the intermediate layer comprises a material represented by $Ge_x Si_{1-x}$, where x is zero or unity or a value between zero and unity.

65. The MSPD of claim 45, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD.

66. The MSPD of claim 45, in which the MSPD further includes ohmic contacts to said top and bottom layers, wherein at least one of said ohmic contact being through a via in said substrate.

67. The MSPD of claim 451, further comprising a light guide to said MSPD for directing said optical input thereto.

68. The MSPD of claim 45, further comprising a light guide to said MSPD configured to bend the optical input from an initial propagation direction to a propagation direction transverse to at least some of said layers.

69. The MSPD of claim 45, further comprising one or more additional MSPDs formed on or in the single substrate, and respective different optical bandpass filters coupled with respective ones of the MSPDs, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input.

70. The MSPD of claim 45, further comprising one or more additional MSPDs in an array on or in said single substrate, said MSPDs being configured into an optical communication structure or a light distance and ranging (LIDAR) structure.

71. The MSPD of claim 45, further comprising a laser emitter formed on or in said single substrate.

72. The MSPD of claim 45, further including a material that is over a side of one of the top and bottom layers facing away from the intermediate layer and is configured to reduce sheet resistance.

73. The MSPD of claim 45, further including a material that is over a side of one of the top and bottom layers facing away from the intermediate layer and is configured to reflect light that has passed through the intermediate layer back toward the intermediate layer.

74. The MSPD of claim 45, further including a deliberately textured surface at a side of one of said top and bottom layers facing away from the intermediate layer.

75. The MSPD of claim 45, further including a layer of micro-nano structures formed at a side of one of said top and bottom layers facing away from the intermediate layer.

76. The MSPD of claim 45, further including one or more distributed Bragg reflectors formed at a surface of one of said top and bottom layers facing away from the intermediate layer.

77. The MSPD of claim 45, further including one or more active electronic circuits formed on or in said substrate and coupled to said MSPD to receive said electrical output therefrom and process it into a processed output, thereby constituting a single-chip integrated circuit configured to receive said optical input, convert it to said electrical output, and provide said processed output.

78. The MSPD of claim 45, wherein the optical input and the electrical output are each modulated at a frequency of at least 30 Gigabits per second.

79. The MSPD of claim 45, wherein the quantum efficiency of the MSPD is at least 1.5 times greater than that of an otherwise the same photodetector lacking said holes.

80. The MSPD of claim 45, further including a hermetic seal integral with the MSPD.

81. A method of making a microstructure-enhanced photodetector (MSPD) configured to convert an optical input that at least some of the time has a cross-section that is essentially continuous spatially to an electrical output, comprising:

providing a substrate and forming on or in said substrate a top layer, a bottom layer, and an intermediate layer between the top and bottom layers, wherein:

at least one of the layers has holes intentionally formed therein, extending in directions transverse to the layers;

each of the top and bottom layers comprises a doped material;

the intermediate layer comprises a material that is undoped or is less doped than the top or bottom layer, wherein the degree of doping is the same or different for different positions in the intermediate layer;

forming an input portion configured to receive, concurrently at a plurality of said holes, said optical input that has said essentially continuous cross-section; and

forming an output configured to provide said electrical output.

82. The method of claim 81, in which the step of forming the top layer comprises limiting the top layer to a thickness of no more than 500 nm, and the step of forming the holes comprises forming the holes at least in the top layer.

83. The method of claim 81, further including forming an air-filled volume between the substrate and the MSPD.

84. The method of claim 81, further including a layer of a dielectric material that is at a surface of said substrate, over the holes and spaces between holes, and in the path of said optical input.

85. The method of claim 81, further including forming on or in said substrate an avalanche region under the MSPD, forming therewith an avalanche microstructured photodiode (MSAPD).

86. The method of claim 81, in which forming said holes comprises including the holes in said intermediate layer.

87. The method of claim 81, in which forming said holes comprises including said holes in said intermediate layer as well as in at least one of the first and second layers.

88. The method of claim 81, in which forming said holes comprises forming the holes in each of the top, bottom, and intermediate layer.

89. The method of claim 81, in which each of said top and bottom layers and said intermediate layer has a thickness and the forming of the holes comprises extending the holes through the entire thickness of said intermediate layer and of one of said top layer and bottom layer and through at least a part of the thickness of the other one of said top and bottom layers.

90. The method of claim 81, in which forming of the holes comprises forming at least some of said holes in the shape of inverted pyramids.

91. The method of claim 81, in which at least some of said holes have triangular sections in planes transverse to said layers.

92. The method of claim 81, in which forming the holes comprises forming at least some of said holes with triangular sections in planes transverse to said layers, with vertices within the intermediate layer.

93. The method of claim 81, in which forming said hoes comprises forming at least some of said holes with sidewalls that slope in planes transverse to said layers.

94. The method of claim 81, in which forming said holes comprises forming at least some of said holes with sidewalls that have plural different slopes along inside walls of the holes.

95. The method of claim 81, in which forming said holes comprises forming at least some of said holes such that they differ from each other in at least one of (i) distance by which the holes extend in said directions, (ii) shape of the holes, and (iii) spacing of the holes from each other.

96. The method of claim 81, in which forming said holes comprises forming at least some of the holes in the intermediate layer and forming said top and bottom layers comprises forming at least one of the top and bottom layers to conformally cover inside walls of the holes as well as spaces between the holes.

97. The method of claim 81, including at least partially filling the holes with a dielectric material.

98. The method of claim 81, including completely filling the holes with a dielectric material.

99. The method of claim 81, in which forming the layers comprises forming at least one of the top layer, the bottom layer, and the intermediate layer of a material represented by $Ge_x Si_{1-x}$, where x is greater than zero.

100. The method of claim 81, in which forming the layers comprises forming at least one of the top layer, the bottom layer, and the intermediate

layer of a material represented by $Ge_x Si_{1-x}$, where x is zero or unity or a value between zero and unity.

101. The method of claim 81, further comprising forming ohmic contacts configured for reverse-bias the MSPD.

102. The method of claim 81, further comprising forming a light guide to said MSPD for directing said optical input thereto, said light guide bending the optical input from an initial propagation direction to a propagation direction transverse to said layers.

103. The method of claim 81, further comprising forming one or more additional MSPD on or in said substrate for receiving respective optical inputs, and forming respective different bandpass filters for said optical inputs, thereby configuring different MSPDs on said substrate to respond to different wavelength ranges that are within said optical input.

104. The method of claim 81, further comprising forming one or more additional MSPDs in an array on or in said substrate, said MSPDs being configured into an optical communication structure or a light distance and ranging structure (LIDAR).

105. The method of claim 81, further comprising forming a laser emitter on or in said substrate.

106. The method of claim 81, further including forming a layer of selected material that is over a side of one of the top and bottom layers facing away from the intermediate layers and is configured to reduce sheet resistance.

107. The method of claim 81, further including forming a layer of selected material that is over a side of one of the first and second layers facing away from the intermediate layer and is configured to reflect light that has passed through the intermediate layer back toward the intermediate layer.

108. The method of claim 81, further including deliberately texturing a surface at a side of one of said top and bottom layers facing away from the intermediate layer.

109. The method of claim 81, further including forming a layer of micro-nano structures formed at of one of said top and bottom layers, at a surface thereof facing away from the intermediate layer.

110. The method of claim 81, further including forming one or more distributed Bragg reflectors at one of said top and bottom layers, at a surface thereof away from the intermediate layer.

111. The method of claim 81, further including forming, on or in said substrate, one or more active electronic circuits configured to process the electrical output from the MSPD into a processed output, thereby forming a single-chip integrated circuit configured to receive said optical input, convert it to said electrical output, and provide said processed output.

112. The method of claim 81, further including hermetically sealing the MSPD with a coating integral therewith.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Vishal Parikh
Attorney Docket Number:	5176/88184-CIP

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	70	70
UTILITY SEARCH FEE	2111	1	300	300
UTILITY EXAMINATION FEE	2311	1	360	360
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	92	40	3680
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**4410**

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of each U.S. Patent Appl. Ser. No. 15/309,922 filed November 9, 2016, allowed 6/30/2017.

This application also is a continuation-in-part of each of U.S. Patent Appl. Ser. No. 14/947,718 filed November 20, 2015, and International Patent Appl. No. PCT/US16/67977 filed December 21, 2016 published as WO 2017/112747.

[0002] This application incorporates by reference, and claims the benefit of the filing date of each of the above-identified three patent application, as well as of the applications that they incorporate by reference, directly or indirectly, and the benefit of which they claim, including U.S. provisional applications, U.S. non-provisional applications, and International applications.

[0003] Said Appl. Ser. No. 15/309,922 is a continuation of each of (i) U.S. Patent Appl. Ser. No. 14/943,898 (now Patent 9,530,905), (ii) U.S. Patent Appl. Ser. No. 14/945,003 (now Patent 9,525,084), and International Patent Appl. No. PCT/US15/061120, and incorporates each by reference and claims the benefit of the filing date of each as well as of each of the U.S. Provisional Patent applications the benefit of which they claim.

[0004] Said Appl. Ser. No. 14/947,718 is a continuation of International Patent Appl. No. PCT/US14/39208, published as WO 2014/190189, and incorporates each by reference and claims the benefit of the filing date thereof and of each of the U.S. Provisional Patent applications the benefit of which it claims. U.S. Appl. Ser. No. 14/892,821, now Patent 9,496,435, is a national stage application of said PCT/US14/39208.

[0005] This patent application claims the benefit of and incorporates by reference each of the following provisional applications:

U.S. Prov. Ser. No. 62/465,734 filed March 1, 2017;

U.S. Prov. Ser. No. 62/474,179 filed March 21, 2017;

U.S. Prov. Ser. No. 62/484,474 filed April 12, 2017;

U.S. Prov. Ser. No. 62/487,606 filed April 20, 2017;

U.S. Prov. Ser. No. 62/488,998 filed April 24, 2017;

U.S. Prov. Ser. No. 62/500,581 filed May 3, 2017;

U.S. Prov. Ser. No. 62/505,974 filed May 14, 2017;

U.S. Prov. Ser. No. 62/509,093 filed May 20, 2017;
U.S. Prov. Ser. No. 62/510,249 filed May 23, 2017;
U.S. Prov. Ser. No. 62/514,889 filed June 4, 2017;
U.S. Prov. Ser. No. 62/521,504 filed June 18, 2017;
U.S. Prov. Ser. No. 62/522,169 filed June 20, 2017;
U.S. Prov. Ser. No. 62/527,962 filed June 30, 2017;
U.S. Prov. Ser. No. 62/530,281 filed July 09, 2017;
U.S. Prov. Ser. No. 62/533,078 filed July 16, 2017;
U.S. Prov. Ser. No. 62/533,603 filed July 17, 2017;
U.S. Prov. Ser. No. 62/535,801 filed July 21, 2017;
U.S. Prov. Ser. No. 62/540,524 filed August 2, 2017;
U.S. Prov. Ser. No. 62/542,243 filed August 7, 2017;
U.S. Prov. Ser. No. 62/547,728 filed August 18, 2017;
U.S. Prov. Ser. No. 62/553,844 filed September 2, 2017;
U.S. Prov. Ser. No. 62/556,426 filed September 10, 2017; and
U.S. Prov. Ser. No. 62/561,869 filed September 22, 2017.

[0006] All of the above-referenced provisional and non-provisional patent applications are collectively referenced herein as “the commonly assigned incorporated applications.”

FIELD

[0007] This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.

BACKGROUND

[0008] Fiber-optic communication is widely used in applications such as telecommunications, communication within large data centers, and communications between data centers. Because of attenuation losses associated with using shorter optical wavelengths, most fiber-optic data communication uses optical wavelengths of 800 nm and longer. Commonly used multimode and single mode optical fiber uses wavelengths between 800 nm and 1675 nm. A main component of optical receivers used in fiber-optic communication system is the

photo detector, usually in the form of a photodiode (PD) or avalanche photodiode (APD).

[0009] High-quality low-noise APDs can be made from silicon. However, while silicon will absorb light in the visible and near infrared range, it becomes more transparent at longer optical wavelengths. Silicon PDs and APDs can be made for optical wavelengths of 800 nm and longer by increasing the thickness of the absorption "I" region of the device. However, in order to obtain adequate quantum efficiency (also known as external quantum efficiency), the thickness of the silicon "I" region becomes so large that the device's maximum bandwidth (also referred to as "data rate") is too low for many current and future telecom and data center applications.

[0010] To avoid the inherent problem that silicon PDs and APDs have with longer wavelengths and higher bandwidths, other materials are used. Germanium (Ge) APDs detect infrared out to a wavelength of 2000 nm, but has relatively high multiplication noise. InGaAs APDs can detect out to longer than 1600 nm, and have less multiplication noise than Ge, but still far greater multiplication noise than silicon APDs. InGaAs is known to be used as the absorption region of a heterostructure diode, most typically involving InP as a substrate and as a multiplication layer. This material system is compatible with an absorption window of roughly 900 to 1700 nm. However, both InGaAs PD and APD devices are relatively expensive and have relatively high multiplication noise when compared with silicon and are difficult to integrate with Si electronics as a single chip.

[0011] Information published by a major company in the business of photodetectors (See http://files.shareholder.com/downloads/FNSR/0x0x382377/0b3893ea-fb06-417d-ac71-84f2f9084b0d/Finisar_Investor_Presentation.pdf,) indicates at page 10 that the current market for optical communication devices is over 7 billion U.S. dollars with a compounded annual growth rate of 12%. Photodiodes (PD) used for 850-950 nm wavelength employ GaAs material and for 1550-1650 nm wavelength photodiodes are InP material based, which is both expensive and difficult to integrate with Si based electronics. Therefore, there is a large market and a long-felt need that has not been met for the development of a better device. To date there are no Si material based photodiodes nor avalanche photodiodes (APD) for

850-950 nm and no Ge on Si material based photodiodes nor avalanche photodiodes for 1550-1650 nm that are top-surface or bottom-surface illuminated, with a data rate of at least 25 Gb/s, and are monolithically integrated with CMOS/BiCMOS silicon electronics on a single chip that are commercially available to the knowledge of the inventors herein. However, there has been no lack of trying to develop a better device for this large market. For example, there have been proposals for resonant photodiodes fabricated in Si material (see *Resonant-Cavity-Enhanced High-Speed Si Photodiode Grown by Epitaxial Lateral Overgrowth*, Schaub et al., IEEE PHOTONICS TECHNOLOGY LETTERS, VOL. 11, NO. 12, DECEMBER 1999), but they have not reached the known commercial market. Other forms of high speed photodiodes in a waveguide configuration have been proposed, such as in *40 GHz Si/Ge uni-traveling carrier waveguide photodiode*, Piels et al, DOI 10.1109/JLT.2014.2310780, Journal of Lightwave Technology (incorporated herein by reference); *Monolithic germanium/silicon avalanche photodiodes with 340 GHz gain–bandwidth product*, NATURE PHOTONICS | VOL 3 | JANUARY 2009 | www.nature.com/naturephotonics (incorporated herein by reference and referred to herein as "Kang et al. 2009"); High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide, Feng et al., Applied Physics Letters 95, 261105 (2009), doi: 10.1063/1.3279129 (incorporated herein by reference); where light is coupled edge-wise into an optical waveguide and where the absorption length can be 100 um or longer to compensate for the weak absorption coefficient of Ge at 1550 nm. In these previously proposed waveguide photodiode structures, light propagates along the length of the waveguide and the electric field is applied across the PIN waveguide such that the direction of light propagation and the direction of the electric field are predominantly perpendicular in this waveguide configuration. Since light in Si travels approximately 1000 times faster than the saturated velocity of electrons/holes, a waveguide PD can be 200 microns long for example and the "I" in the PIN can be 2 microns, for example, and achieve a bandwidth of over 10 Gb/s. Such edge coupling of light is costly in packaging as compared to surface illumination as described in this patent specification, where dimensions of the waveguide cross section are typically a few microns as compared to tens of microns for known surface illuminated photodiodes or avalanche photodiodes.

Known waveguide PD/APD are often only single mode optical systems whereas surface illuminated PD/APD described in this patent specification can be used in both single and multimode optical systems. In addition, known waveguide photodiodes are difficult to test at wafer level, whereas surface illuminated photodiodes described in this patent specification can be easily tested at wafer level. Known waveguide photodiodes/avalanche photodiodes are used mostly in specialty photonic circuits and in many cases require careful temperature control, which can be costly and inefficient in a hostile data center environment. A top or bottom illuminated Si and Ge on Si or GeSi on Si PD/APD that can be integrated with Si is not known to be commercially available at data rates of 25 Gb/s or more at wavelengths of 850-950 nm, 1250-1350 nm and 1550-1650 nm. In contrast, photodiodes on Si based material, as described in this patent specification, can be monolithically integrated with integrated electronic circuits on a single Si chip, thereby significantly reducing the cost of packaging. In addition, the microstructured PD/APD at 850 nm, 1300 nm and 1550 nm nominal wavelengths described in this patent specification can be predominantly for short haul (short reach), medium haul (reach gap) and long haul (long reach), distances less than 300 meters, in certain cases less than 2000 meters, in certain cases less than 10000 meters and in certain cases greater than 10000 meters optical data transmission. The microstructured PD/APD direction of incident optical beam and the electric field in the “I” region of a PIN or NIP structure, are predominately collinear and/or almost collinear. This patent specification enables such a device and is expected to transform the current data centers to almost all optical data transmission between blades, within a blade, between racks and/or between data centers, that will vastly increase the data transmission bandwidth capabilities and significantly reduce electrical power usage.

[0012] The subject matter claimed herein is not limited to embodiments that solve any specific disadvantages or that operate only in environments such as those described above. Rather, this background is only provided to illustrate one exemplary technology area where some embodiments described herein may be practiced.

[0013] Each published document referenced in this patent specification is hereby incorporated by reference.

SUMMARY

[0014] According to some embodiments, a single-chip device comprises an integrated combination of a microstructure-enhanced photodetector (MSPD) and an active electronic circuit, both formed on or in a single substrate and configured to receive an optical input that in cross-section is substantially continuous spatially at least some of time, convert the optical input to an electrical output, and process the electrical output into a processed output. The MSPD on or in said single substrate comprises an intermediate layer, a first layer at one side of the intermediate layer, and a second layer at an opposite side of the intermediate layer, wherein: each of the layers comprises Silicon, Germanium, or an alloy thereof; at least one of said layers, or an overlying covering layer that may be present, has holes intentionally formed therein, extending in directions transverse to the layers; each of the first and second layers comprises a doped material; the intermediate layer comprises a material that is less doped than at least one of the first and second layers or is undoped, wherein the degree of doping is the same or different for different positions in the intermediate layer; an input portion configured to concurrently receive at a plurality of said holes said optical input that has said substantially continuous cross-section; and an output portion configured to provide said electrical output from the MSPD. The active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto: amplification to form said processed output from the single-chip device; processing other than or in addition to amplification to form said processed output from the single-chip device; and routing to one or more selected destinations. A communication channel on or in said single-chip device is configured to deliver the electrical output from the MSPD to the active electronic circuit.

[0015] The active electronic circuit can at least partly extend beyond said substrate, or can be at least partly inside said substrate. An overlying layer can be present as a superstrate at one side of said first, intermediate, and second layers, and can contain said holes. The MSPD can comprises a III-V materials family photodiode. An air-filled volume can be formed between the substrate and the MSPD. A layer of a dielectric material that is in the propagation path of said optical input can be provided to cover the holes as well as spaces between the holes. An

avalanche region can be provided at one side of the MSPD, forming therewith an avalanche microstructured photodiode (MSAPD). The holes can be present in said intermediate layer, in at least one of the first and second layers, or in each of the three layers. Each of said first and second layers and said intermediate layer has a thickness and at least some of said holes extend through the entire thickness of the intermediate layer and of one of said first layer and second layer and through at least a part of the thickness of the other one of said first and second layers.

[0016] At least some of said holes can be shaped as inverted pyramids, can have triangular sections in planes transverse to said layers, and the vertices of the pyramids of the triangular sections can be within the intermediate layer. The holes can have sidewalls that slope in planes transverse to said layers, and the holes can have plural different slopes along their inside walls. At least some of said holes on the same substrate can differ from each other in at least one of (i) distance by which the holes extend in said directions, (ii) shape of the holes, and (iii) spacing of the holes from each other. When the intermediate layer includes holes, one of the first and second layers can be in the form of a layer that conformally covers inside walls of the holes as well as spaces between the holes. The holes can be partly or entirely filled with a dielectric material.

The optical input enters the MSPD through one or both of said first and second layers, and each of the first and second layers through which the optical input enters can be no more than 500 nanometers thick.

[0017] At least one of the first layer, the second layer, and the intermediate layer comprises a material represented by $Ge_x Si_{1-x}$, where x is greater than zero.

[0018] The MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD, and at least one of said ohmic contact can be through a via in said substrate.

[0019] The single-chip device can further comprise a light guide to said MSPD for directing said optical input thereto, and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip device. The light guide can be configured to bend the optical input from an initial propagation direction to a propagation direction transverse to said layers.

[0020] The single-chip device can have one or more additional MSPD on or in the same substrate, one or more additional active electronic circuits, and

respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs can be configured to respond to different wavelength ranges that are within said optical input. The additional active electronic circuits can comprise one or more transimpedance amplifiers (TIAs) and one or more application specific integrated circuits (ASICs), and any of them can comprise CMOS, BiCMOS, and/or bipolar active devices. The single-chip device can be configured into an optical communication structure or a light distance and ranging (LIDAR) structure, and can include a laser emitter formed on or in said single substrate.

[0021] The MSPD in the single-chip device can include a layer of selected material that is over a side of one of the first and second layers facing away from the intermediate layer and is configured to reduce sheet resistance. In another example, the layer of selected material can be configured to reflect light that has passed through the intermediate layer back toward the intermediate layer. In yet another example, a deliberately textured surface is formed at a side of one of said first and second layers facing away from the intermediate layer. A layer of micro-nano structures can be formed at of one of said first and second facing, at a surface thereof facing away from the intermediate layer. One or more distributed Bragg reflectors can be formed at one of said first and second layers, at a surface thereof away from the intermediate layer. An isolation trench between the MSPD and the active electronic circuit can be included in the single-chip device, and a light shield layer can be formed over said active electronic circuit.

[0022] The optical input to the MSPD in the single-chip device and the electrical output from the MSPD can each be modulated at a frequency of at least 30 Gigabits per second, and the MSPD can operate at quantum efficiency of at least 1.5 times greater than that of a photodetector that is otherwise the same but lacks said holes.

[0023] According to some embodiments, the single-chip device is hermetically sealed, for example with a dielectric such as silicon oxide or nitride and/or a polymer. This may obviate a need for additional hermetic packaging in practical applications of the single-chip device, such as in data centers.

[0024] According to some embodiments, a microstructure-enhanced photodetector (MSPD) configured to convert to an electrical output an optical input

that in cross-section is essentially continuous spatially at least some of the time, comprises a substrate and a top layer, a bottom layer, and an intermediate layer between the top and bottom layers formed on or in the substrate, wherein: at least one of the layers has holes intentionally formed therein, extending in directions transverse to the layers; each of the top and bottom layers comprises a doped material; and the intermediate layer comprises a material that is undoped or is less doped than the top or bottom layer, wherein the degree of doping is the same or different for different positions in the intermediate layer. The MSPD includes an input portion configured to receive, concurrently at a plurality of said holes, said optical input that has said essentially continuous cross-section; and an output portion configured to provide said electrical output.

[0025] In some embodiments, the top layer is no more than 500 nm thick and the holes are at least in the top layer, an air-filled volume is provided between the substrate and the MSPD, a layer of a dielectric material is provided that is at a surface of said substrate, over the holes and spaces between the holes, and in the path of said optical input.

[0026] The MSPD can further include an avalanche region under the MSPD, forming therewith an avalanche microstructured photodiode (MSAPD).

[0027] The holes in the MSPD can be in the intermediate layer, in one of the top and bottom layers, or through the entire thickness of all three layers, or through the entire thickness of one of the top and bottom layers but only partly into the other.

[0028] A least some of said holes can be shaped as inverted pyramids, can have triangular sections in planes transverse to said layers, the vertices of the pyramids and triangular sections can be within the intermediate layer, the holes can have sidewalls that slope in planes transverse to said layers, and there can be plural different slopes along inside walls of the holes. At least some of said holes in the same substrate can differ from each other in at least one of (i) distance by which the holes extend in said directions, (ii) shape of the holes, and (iii) spacing of the holes from each other.

[0029] When the holes extend into the intermediate layer, one of said top and bottom layers can conformally cover inside walls of the holes as well as spaces

between the holes. The holes can be partly or entirely filled with a dielectric material.

[0030] At least one of the top and bottom layers and the intermediate layer can comprise a material represented by $Ge_x Si_{1-x}$, where x is greater than zero but less than unity, or where x is zero or unity or a value between zero and unity.

[0031] The MSPD can further further comprise ohmic contacts configured for reverse-biasing the MSPD, and at least one of said ohmic contact can be through a via in said substrate. The MSPD can further comprise a light guide for directing said optical input thereto. The light guide can be configured to bend the optical input from an initial propagation direction to a propagation direction transverse to at least some of said layers. The MSPD can further comprise one or more additional MSPDs formed on or in the same substrate, and respective different optical bandpass filters coupled with respective ones of the MSPDs, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input. The plural MSPDs on or in the same substrate can be configured into an optical communication structure or a light distance and ranging (LIDAR) structure. The MSPD can further comprise a laser emitter formed on or in said single substrate.

[0032] The MSPD can include a material that is over a side of one of the top and bottom layers facing away from the intermediate layer and is configured to reduce sheet resistance, a material that is over a side of one of the top and bottom layers facing away from the intermediate layer and is configured to reflect light that has passed through the intermediate layer back toward the intermediate layer, a deliberately textured surface at a side of one of said top and bottom layers facing away from the intermediate layer, a layer of micro-nano structures formed at a side of one of said top and bottom layers facing away from the intermediate layer, and/or one or more distributed Bragg reflectors formed at a surface of one of said top and bottom layers facing away from the intermediate layer.

[0033] When one or more active electronic circuits are formed on or in the same substrate as the MSPD and coupled to said MSPD to receive said electrical output therefrom and process it into a processed output, the resulting combination forms a single-chip integrated circuit configured to receive said optical input, convert it to said electrical output, and provide said processed output.

[0034] The MSPD is configured to operate when its optical input and electrical output are each modulated at a frequency of at least 30 Gigabits per second, at a quantum efficiency of at least 1.5 times that of an otherwise the same photoconductor lacking said holes.

[0035] According to some embodiments, the MSPD is hermetically sealed, for example with a dielectric such as silicon oxide or nitride and/or a polymer. This may obviate a need for additional hermetic packaging in practical applications of MSPD, such as in data centers.

[0036] According to some embodiments, a method of making a microstructure-enhanced photodetector (MSPD) configured to convert an optical input that at least some of the time has a cross-section that is essentially continuous spatially to an electrical output, comprises: providing a substrate and forming on or in said substrate a top layer, a bottom layer, and an intermediate layer between the top and bottom layers, wherein at least one of the layers has holes intentionally formed therein, extending in directions transverse to the layers, each of the top and bottom layers comprises a doped material, the intermediate layer comprises a material that is undoped or is less doped than the top or bottom layer, wherein the degree of doping is the same or different for different positions in the intermediate layer. The method further includes forming an input portion configured to receive, concurrently at a plurality of said holes, said optical input that has said essentially continuous cross-section, and forming an output configured to provide said electrical output.

[0037] The step of forming the top layer can comprise limiting the top layer to a thickness of no more than 500 nm, and the step of forming the holes can comprise forming the holes at least in the top layer. The method can further include forming an air-filled volume between the substrate and the MSPD, a layer of a dielectric material that is at a surface of said substrate, over the holes and spaces between holes, and in the path of said optical input, and an avalanche region under the MSPD, forming therewith an avalanche microstructured photodiode (MSAPD). Forming the holes can comprise including the holes in said intermediate layer, in said intermediate layer as well as in at least one of the top and bottom layers, and/or forming the holes in each of the first, second, and intermediate layer.

[0038] The method of claim 1, in which each of said top and bottom layers and said intermediate layer has a thickness and the forming of the holes comprises

extending the holes through the entire thickness of said intermediate layer and of one of said top layer and bottom layer and through at least a part of the thickness of the other one of said top and bottom layers.

[0039] The method can include forming at least some of said holes in the shape of inverted pyramids, with triangular sections in planes transverse to said layers, with vertices of the pyramids or triangular sections in the intermediate layer, and/or with plural different slopes along inside walls of the holes. The forming of holes can comprise forming at least some of said holes such that they differ from each other in at least one of (i) distance by which the holes extend in said directions, (ii) shape of the holes, and (iii) spacing of the holes from each other.

[0040] When the holes extend into the intermediate layer, the method can include forming one of the top and bottom layers to conformally cover inside walls of the holes as well as spaces between the holes. The method can include partially or entirely filling the holes with a dielectric material, and forming at least one of the top layer, the bottom layer, and the intermediate layer of a material represented by $Ge_x Si_{1-x}$, where x is greater than zero or where x is zero or unity or a value between zero and unity. The method can further comprise forming ohmic contacts configured for reverse-bias the MSPD, forming a light guide to said MSPD for directing said optical input thereto, where the light guide can bend the optical input from an initial propagation direction to a propagation direction transverse to said layers, and forming one or more additional MSPD formed on or in said substrate for receiving respective optical inputs, and forming respective different bandpass filters for said optical inputs, thereby configuring different MSPDs on said substrate to respond to different wavelength ranges that are within said optical input.

[0041] According to some embodiments, the method includes forming one or more additional MSPDs in an array on or in the same substrate, said MSPDs being configured into an optical communication structure or a light distance and ranging structure (LIDAR), forming a laser emitter on or in said substrate, forming a layer of selected material that is over a side of one of the top and bottom layers facing away from the intermediate layers and is configured to reduce sheet resistance and/or to reflect light that has passed through the intermediate layer back toward the intermediate layer, deliberately texturing a surface at a side of one of said top and bottom layers facing away from the intermediate layer, forming a layer of

micro-nano structures formed at of one of said top and bottom layers, at a surface thereof facing away from the intermediate layer, and/or forming one or more distributed Bragg reflectors at one of said top and bottom layers, at a surface thereof away from the intermediate layer.

[0042] According to some embodiments, the method further includes forming, on or in the same substrate as the MSPD, one or more active electronic circuits configured to process the electrical output from the MSPD into a processed output, thereby forming a single-chip integrated circuit configured to receive said optical input, convert it to said electrical output, and provide said processed output.

[0043] According to some embodiments, the method further includes hermetically sealing the MSPD and/or the single-chip device, for example with a dielectric such as silicon oxide or nitride and/or a polymer. This may obviate a need for additional hermetic packaging in practical applications of the single-chip device and/or the MSPD, such as in data centers.

[0044]

BRIEF DESCRIPTION OF THE DRAWINGS

[0045] To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments thereof are illustrated in the appended drawings. It should be appreciated that these drawings depict only illustrative embodiments and are therefore not to be considered limiting of the scope of this patent specification or the appended claims. The subject matter hereof will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[0046] FIGs. 1A-1H are top-view scanning electron micrographs of inverted pyramid holes used in a microstructure high speed photodiode (MSPD) and/or a high speed microstructure avalanche photodiode (MSAPD), according to some embodiments;

[0047] FIGs. 2A-2D are cross-section scanning electron microscope (SEM) micrographs of holes that are first wet etched using KOH and then dry etched using deep reactive ion etching (DRIE), according to some embodiments;

[0048] FIG. 3 is a schematic cross section of a N-I-P photodiode structure that can be grown on a silicon substrate or a SOI substrate, according to some embodiments;

[0049] FIG. 4 is a cross sectional schematic drawing of a possible MSPD using the layers shown in FIG. 3, according to some embodiments;

[0050] FIG. 5 is a schematic cross section of a MSPD with N-I(N^-)-P structure on P silicon substrate or SOI substrate where the microstructure holes have an initial funnel followed by a more cylindrical hole, according to some embodiments;

[0051] FIGs. 6A-6D are diagrams illustrating forming of silicon on holes (SOH), according to some embodiments;

[0052] FIG. 6E is a cross sectional schematic diagram showing the device in FIG 5 fabricated on a substrate SOH (silicon on holes), according to some embodiments;

[0053] FIG. 7A is a top view of GeSi and/or Ge on silicon, according to some embodiments;

[0054] FIG. 7B is a top view of a spherical grid pattern of GeSi and/or Ge on silicon, according to some embodiments;

[0055] FIG. 7C shows three examples of nano/micro structure holes filled or partially filled with GeSi and/or Ge, according to some embodiments;

[0056] FIG. 8 is a diagram illustrating a monolithically integrated single silicon chip that can include single and/or multiple combinations of devices, according to some embodiments;

[0057] FIGs. 9A and 9B are schematic cross sections of a possible MSPD P-I-N structure, according to some embodiments;

[0058] FIG. 10 is a cross section view of three funnel shaped holes, according to some embodiments;

[0059] FIG. 11 is a plot showing a FDTD (Finite Difference Time Domain) simulation for the optical field in a structure as shown in FIG. 10;

[0060] FIG. 12A is a plot of a FDTD simulation of a hexagonal lattice with holes given in FIG. 10 where the holes are funnel shaped with a funnel slope of 61 degrees;

[0061] FIG. 12B is a plot showing the QE of a MSPD as in curve 1216 of FIG. 12A;

[0062] FIG. 13 is a plot showing the enhanced absorption vs. wavelength from 800-900 nm for an all silicon structure shown in FIG. 10;

[0063] FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments;

[0064] FIG. 15 is a plot of a FDTD simulation of absorption for a structure similar to FIG. 10;

[0065] FIG. 16 is a plot of a FDTD simulation of a structure similar to that of the plot in FIG. 15 except with a thinner top layer;

[0066] FIG. 17 is a plot of a FDTD simulation of a structure similar that plotted in FIG. 15 except with P and N layers being 100 nm thickness;

[0067] FIG. 18A-18E are schematic diagrams of microstructured holes positioned on a photosensitive surface of a MSPD/MSAPD, according to some embodiments;

[0068] FIGs. 19A-19D are a series of cross section views illustrating holes being etched into a buried oxide layer of a SOI wafer, according to some embodiments;

[0069] FIGs. 19E-19H are a series of cross section views illustrating shows holes etched into the oxide of a SOI wafer that are filled with a high index dielectric, according to some embodiments;

[0070] FIG. 19I is a diagram showing a silicon wafer having hole patterns etched for bandpass filtering in locations where MSPDs/MSAPDs are to be fabricated, according to some embodiments;

[0071] FIG. 20 is a cross sectional diagram showing several filters, each having a different passband for each of several MSPDs, according to some embodiments;

[0072] FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics, according to some embodiments;

[0073] FIGs. 22A and 22B are diagrams illustrating cost savings from using a monolithically integrated MSPD(s)/MSAPD(s) with ASIC(s);

[0074] FIG. 23 is a simple schematic diagram showing MSPDs/MSAPDs in an array, according to some embodiments;

[0075] FIGs. 24 and 25 are schematic cross section views of a MSAPD with holes that can have various shapes, according to some embodiments;

[0076] FIG. 26 is schematic diagram illustrating integration of the MSAPD structure in FIG. 24 with CMOS and/or BiCMOS electronics, according to some embodiments;

[0077] FIG. 27 is schematic diagram illustrating integration of the MSAPD structure in FIG. 24 with CMOS and/or BiCMOS electronics, according to some other embodiments;

[0078] FIG. 28 is a table showing experimental measurements of a MSPD with approximately 1000 nm thick I layer, 200 nm N layer and approximately 1500 nm P layer on 2000 nm BOX on silicon substrate, according to some embodiments;

[0079] FIG. 29 is a schematic drawing of a vertical cavity surface emitting laser (VCSEL) being used together with a MSPD/MSAPD that is monolithically integrated with ASIC CMOS and/or BiCMOS electronics for close proximity free space optical data link, according to some embodiments;

[0080] FIG. 30 is a cross section view of a basic epitaxial layer structure for monolithic integration of a MSPD with ASICs such as a TIA, according to some embodiments;

[0081] FIG. 31 is a cross section view showing some aspects of a MSPD integrated with CMOS/BiCMOS ASICs, according to some embodiments;

[0082] FIG. 32 is a diagram showing a monolithically integrated MSPD with TIA and other ASICs that is flip chip mounted on a printed circuit board using solder bump technology, according to some embodiments;

[0083] FIG. 33 is a diagram showing a similar structure to FIG. 30 but with selective P layer growth, diffusion and/or ion implantation on parts of the I layer surface, according to some embodiments;

[0084] FIG. 34 is a cross section view showing some aspects of a MSPD integrated with TIA/ASICs using a layer structure as in FIG. 33, according to some embodiments;

[0085] FIG. 35 is a cross section view showing an epitaxial layer structure for an MSAPD monolithically integrated with CMOS/BiCMOS ASICs, according to some embodiments;

[0086] FIG. 36 is a cross section view showing some aspects of a MSAPD monolithically integrated with CMOS/BiCMOS TIA/ASICs, according to some embodiments;

[0087] FIG. 37 is a top view showing some aspects of a MSPD/MSAPD monolithically integrated with a TIA/ASICs without the solder bumps and/or bond pads, according to some embodiments;

[0088] FIG. 38 is cross section view showing some aspects of a MSPD/MSAPD monolithically integrated with a TIA/ASICs, according to some embodiments;

[0089] FIG. 39 is a cross section view an epitaxial layer structure, according to some embodiments;

[0090] FIG. 40 is a cross section view illustrating some aspects of MSPD - ASIC monolithic integration, according to some embodiments;

[0091] FIG. 41 is a cross section view illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments;

[0092] FIG. 42 is a cross section view illustrating aspects of MSPD monolithically integrated with CMOS/BiCMOS electronics, according to some embodiments;

[0093] FIG. 43 is a cross section view of a structure similar to FIG. 41 except that the holes are etched through the P-I-N structure, according to some embodiments;

[0094] FIGs. 44A-44C are cross section views illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments;

[0095] FIG. 45 is a cross section view as in FIGs. 44A-44C illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments;

[0096] FIG. 46 is a cross section view illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments;

[0097] FIG. 47 is a cross section view illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments;

[0098] FIG. 48 is a cross section view illustrating some further aspects of MSPD - ASIC monolithic integration similar to FIG. 47, according to some embodiments;

[0099] FIGs. 49, 50A and 50B are top views and a cross section view illustrating some aspects of selective ion implantation for MSPD - ASIC monolithic integration, according to some embodiments;

[00100] FIG. 51 is a cross sectional view of a microstructured avalanche photodiode (MSAPD) with a $P^+ P^{--} PN^+$ structure on SOI wafer, according to some embodiments;

[00101] FIG. 52 is a cross section view of a MSAPD integrated with CMOS/BiCMOS ICs such as TIA and other ASICS for signal processing, according to some embodiments;

[00102] FIG. 53 is a top view schematic of an array of MSPDs/MSAPDs integrated with CMOS/BiCMOS ICs such as TIA and other signal processing ASICs, according to some embodiments;

[00103] FIG. 54 is a cross section of a possible layer structure for integrating MSPD/MSAPD with CMOS/BiCMOS electronics, according to some embodiments;

[00104] FIG. 55 is a cross section view illustrating some aspects of MSPD/MSAPD integration with CMOS/BiCMOS integrated circuits, according to some embodiments;

[00105] FIG. 56 is a cross section view illustrating some aspects of MSPD/MSAPD integration with CMOS/BiCMOS integrated circuits, according to some embodiments;

[00106] FIG. 57 is cross section view of a CMOS/BiCMOS wafer on SOI for use in integration with MSPDs/MSAPDs, according to some embodiments;

[00107] FIG. 58 is cross section showing some aspects CMOS/BiCMOS integration with MSPDs/MSAPDs, according to some embodiments;

[00108] FIGs. 59A and 59B are cross sections illustrating some aspects of a MSPD integrated with CMOS/BiCMOS ASICs that include a TIA on a CMOS/BiCMOS compatible silicon substrate, according to some embodiments;

[00109] FIG. 60 is a cross section view of a silicon PIN photodiode integrated with TIA and other ASICs, according to some embodiments;

[00110] FIGS. 61A-61D are top views illustrating aspects of microstructured optical waveguides, according to some embodiments;

[00111] FIG. 62A is a cross section view showing aspects of a microstructured optical waveguides photodiode (MSOWPD) integrated with CMOS/BiCMOS ASICs, according to some embodiments;

[00112] FIGs. 62B and 62C are top views showing further aspects of microstructured optical waveguides photodiodes according to some embodiments;

[00113] FIGs. 63A-63C are cross section views illustrating aspects of MSPDs integrated with CMOS/BiCMOS circuitry utilizing selective area growth of Ge and/or GeSi on silicon, according to some embodiments;

[00114] FIG. 64 is a cross section view showing aspects of a MSPD/MSAPD/MSOWPD/MSOWAPD having surface microstructures and is monolithically integrated with CMOS and/or BiCMOS ICs, according to some embodiments;

[00115] FIGs. 65, 66 and 67 are cross sectional views showing aspects of monolithically integrated MSPDs and CMOS/BiCMOS ICs with a through silicon via (TSV), according to some embodiments;

[00116] FIG. 68A is a cross section showing a layer structure of Ge and/or GeSi on Si for monolithic integration of an MSPD with CMOS/BiCMOS ASICs, according to some embodiments;

[00117] FIG. 68B is a cross section showing some further aspects of a monolithically integrated CMOS/BiCMOS ASICs with a MSPD using a Ge and/or GeSi on Si, according to some embodiments;

[00118] FIG. 69A and 69B are cross section views showing some aspects of monolithic integration of a MSPD with CMOS/BiCMOS ASICs, according to some embodiments;

[00119] FIG. 70A is a cross section illustrating some aspects of integration of a MSPD with CMOS/BiCMOS ASICs, according to some embodiments;

[00120] FIG. 70B is a plot showing absorption for an MSPD simulated using using finite difference time domain analysis (FDTD), according to some embodiments;

[00121] FIG. 70C is a plot showing a FDTD simulation of the optical field in the microstructure holes, according to some embodiments;

[00122] FIG. 70D is a plot of a data rate bandwidth calculation, according to some embodiments;

[00123] FIG. 71 is cross section view similar to FIG. 70A with the addition of a BOX (buried oxide) layer;

[00124] FIG. 72 is a cross section showing some aspects of a MSAPD monolithically integrated with CMOS/BiCMOS ICs, according to some embodiments;

[00125] FIG. 73 is a cross section view of a structure that is similar to that of FIG. 72 except that a buried N type device layer is included;

[00126] FIGs. 74 and 75 are perspective views showing some aspects of a connecting wells for connecting surface electrodes to lower layers, according to some embodiments;

[00127] FIGs. 76A to 76K are diagrams illustrating aspects of a basic process flow for fabricating MSPDs monolithically integrated with CMOS/BiCMOS ASICs, according to some embodiments;

[00128] FIG. 77A is cross section view of an MSPD, according to some embodiments;

[00129] FIG. 77B is a plot showing a FDTD simulation of the optical field spanning wavelengths from 800 nm to 900 nm interacting with microstructure holes, according to some embodiments;

[00130] FIG. 78 is a cross section view of a structure similar to FIG. 76A with a BOX layer (or on a SOI wafer), according to some embodiments;

[00131] FIG. 79 is a plot showing a FDTD simulation of the structure shown in FIG. 78 of the optical field interacting with the microstructure holes in silicon;

[00132] FIG. 80 is a cross section illustrating some aspects of a MSAPD with microstructure holes, according to some embodiments;

[00133] FIG. 81 is a cross section similar to FIG. 80, and illustrating some aspects of a MSAPD with microstructure holes, according to some embodiments;

[00134] FIGs. 82A and 82B are cross sectional views of layer structures prior to integration of a MSPD with CMOS/BiCMOS ASICs, according to some embodiments;

[00135] FIG. 83 is a cross section view showing aspects of a starting layer structure with N^+ surface well, according to some embodiments;

[00136] FIGs. 84A and 84B are cross sectional views of a MSPD/MSAPD on SOI and/or a sacrificial layer, according to some embodiments;

[00137] FIG. 85 is a top view of a MSPD/MSAPD integrated with CMOS/BiCMOS, according to some embodiments;

[00138] FIG. 86 is a plot showing the results of a FDTD simulation of the optical field on inverted pyramid holes on 1 micron thick silicon with air interfaces on both the top and bottom;

[00139] FIG. 87 is a cross section view of a N-I-P photodiode structure on SOI with a BOX layer, according to some embodiments;

[00140] FIG. 88 is a plot showing a FDTD simulation of absorption of the incident photons in the I or low doped layer as a function of wavelength from 800-900 nm for the structure shown in FIG. 87;

[00141] FIG. 89 is a cross section view of an MSPD, according to some embodiments;

[00142] FIG. 90 is a cross section view of a MSPD PIN structure that can be monolithically integrated with CMOS/BiCMOS ASICs on a SOI wafer, according to some embodiments;

[00143] FIG. 91 is a plot showing a FDTD simulation of the optical field from 800-900 nm wavelength impinging on the top surface of a structure shown in FIG. 90;

[00144] FIG. 92 is a cross section view of a two-dimensional (2D) material photodetector that can have an absorption enhancement by employing micro and/or nano holes for photon trapping, according to some embodiments;

[00145] FIG. 93 is a cross section view of a MSPD PIN structure similar to that shown in FIG. 90, according to some embodiments;

[00146] FIG. 94 is cross section showing a structure similar to FIG. 80 except with the addition of a superstrate as shown in FIG. 93;

[00147] FIGs. 95A to 95C are plots showing a FDTD simulation of the optical field absorption in the I or low doped layers of FIGs 93 and 94;

[00148] FIG. 96 is a cross section view of a lateral P-I-N photodiode structure that is surface illuminated, according to some embodiments;

[00149] FIG. 97 is a top view of the structure shown in FIG. 96, according to some embodiments;

[00150] FIG. 98 is a top view of an integrated MSPD/MSAPD, according to some embodiments;

[00151] FIG. 99A is a cross section schematic of a microstructure enhanced III-V photodiode, according to some embodiments;

[00152] FIG. 99B is a plot showing an FDTD simulation of the the structure shown in FIG. 99A;

[00153] FIG. 100 is a cross section of a MSPD, according to some embodiments; and

[00154] FIG. 101 is a cross section of a MSPD (or MSAPD) with a mesa and the regions under the microstructure holes selectively removed, according to some embodiments;

[00155] FIG. 102 is a plot showing an FDTD simulation of the optical field absorption enhancement verses wavelength for a MSPD structure and with either a PIPN or PIPIN structure for a MSAPD device, according to some embodiments; and

[00156] FIG. 103 is a cross section of an MSPD or MSAPD having Ge and/or GeSi layers grown on Si that is monolithically integrated with CMOS/BiCMOS ASICs, according to some embodiments.

DETAILED DESCRIPTION

[00157] A detailed description of examples of preferred embodiments is provided below. While several embodiments are described, it should be understood that the new subject matter described in this patent specification is not limited to any one embodiment or combination of embodiments described herein, but instead encompasses numerous alternatives, modifications, and equivalents. In addition, while numerous specific details are set forth in the following description in order to provide a thorough understanding, some embodiments can be practiced without some or all of these details. Moreover, for the purpose of clarity, certain technical material that is known in the related art has not been described in detail in order to avoid unnecessarily obscuring the new subject matter described herein. It should be clear that individual features of one or several of the specific embodiments described herein can be used in combination with features or other described embodiments. Further, like reference numbers and designations in the various drawings indicate like elements.

[00158] Microstructures in photodiodes and microstructures avalanche photodiodes can enhance the absorption of incident signal photons and can result in a larger external quantum efficiency over a similar structure without microstructures for enhancement of the absorption over a given wavelength range. Enhancement of the absorption can also be viewed as an enhancement in the absorption length. Light can interact with absorbing layer(s) for a longer length of time, which if velocity is constant can equivalently be longer distance. The optical modes excited in a microstructured photodiode/avalanche photodiode can propagate in a direction that is the same and/or different from the incident photon direction impinging in the microstructured photodiode/avalanche photodiode (MPD/APD) which can include a predominantly lateral direction in the plane of the epitaxial layers and/or a mixture of lateral and vertical stationary and/or propagating optical modes. The optical modes can be any arithmetic combination of vertical and lateral modes which are complex coupled modes of many resonators that may be similar and/or different. In addition, slow waves can be generated by the microstructures that further enhance absorption and therefore quantum efficiency (external quantum efficiency where reflection off the incident surface and transmission through the structure and any scattering can be accounted for, when quantum efficiency is mentioned it is always the external quantum efficiency) which is proportional to absorption in the case of photodiodes. Ratios of quantum efficiency to absorption can range from 1 to 0.3, for example. For a heterostructure photodiode, for example a P-I-N structure where the P and N are silicon and the I can be GeSi alloy, at longer wavelengths, for example, 950 nm or longer, the P and N will absorb less and most of the absorption will occur in the I GeSi layer. This can result in a quantum efficiency to absorption ratio closer to 1, for example 0.6-0.99. In the case of avalanche photodiode where there is gain, quantum efficiency can often be greater than 100%; for example with an absorption of 60% and a ratio of quantum efficiency to absorption ratio of 70% (in the case of unity gain) the quantum efficiency is 42% and with a gain of 2 (3dB) the quantum efficiency can be 84% and with a gain of 4 (6dB) the quantum efficiency can be 164%.

[00159] The microstructured photodiodes and microstructured avalanche photodiodes are predominantly surface illuminated where the optical signal

impinges on either the top or bottom or both surfaces of the photodiode/avalanche photodiode. The angle of the incident photon, depending on the numerical aperture and/or angle of the fiber, can range in angles from 80 degrees off normal to normal.

[00160] The microstructure holes can be etched in a KOH solution, see Refs. Fan et al, Differences in etching characteristics of TMAH and KOH on preparing inverted pyramids for silicon solar cells, Applied Surface Science *264 (2013) 761–766*; and Mavrokefalos et al, Efficient Light Trapping in Inverted Nanopyramid Thin Crystalline Silicon Membranes for Solar Cell Applications, Nano Lett. 2012, 12, 2792−2796 (both incorporated herein by reference).

[00161] In addition, holes can be etched with any combinations of wet and dry etching and also can have a multiple of wet/dry/wet/dry/wet etchings to define different hole shapes, different features such as nano glass to reduce reflections, and different wet and dry etching methods and chemicals.

[00162] FIGs. 1A-1H are top-view scanning electron micrographs of holes in the shape of inverted pyramids used in a microstructure high speed photodiode (MSPD) and/or a high speed microstructure avalanche photodiode (MSAPD), according to some embodiments. The microstructures were etched using a KOH anisotropic etch for holes ranging in diagonal from 250 nm to 700 nm and period ranging from 500 nm to 1000 nm. In some cases, the hole diameters can range from 200 nm to 2500 nm and periods can ranging from 300 nm to 3000 nm. An etch depth of 0.5-1.2 microns is shown, depending on hole diameter or diagonal. In some cases, etch depth can range from 0.2 to 10 microns for example. These microstructures resemble invented pyramids. Inverse pyramids are illustrated in Zhang et al, Silicon single-photon avalanche diodes with nano-structured light trapping, Nature Communications, 8:628, published online 20 September 2017 (DOI 10:1038/s41467-017-00733-y; www.nature.com/naturecommunications). The stated publication date of this paper is later than the filing dates of all but the most recent of the provisional applications the benefit of which this patent specification claims directly. While there are significant differences between the paper and the embodiments described in this patent specification, the paper can be considered a confirmation of benefits of inverted (inverse) pyramids illuminated by a beam of light.

[00163] FIGs. 2A-2D are cross-section scanning electron microscope (SEM) micrographs of holes that are first wet etched using KOH and then dry etched using deep reactive ion etching (DRIE), according to some embodiments. See e.g., Wu et al, High aspect ratio silicon etch: A review, J. Appl. Phys. 108, 051101 ∟2010 (incorporated herein by reference and referred to herein as "Wu et al"). Some nano-grass can also appear after dry etching due to any contaminants such as flakes of silicon nitride etch mask, that may be on the surface of the holes after the wet etch. The nano-grass can help reduce reflections and improve the enhancement of absorption and therefore the quantum efficiency. The nano-grass can also be removed by further wet etching. Cycles of wet and dry etching can be repeated to generate the desired hole profile for optimizing the absorption enhancements over a certain wavelength range, spanning from a few nanometers to tens of nanometers to hundred nanometers or more. In FIGs. 1A-1H and 2A-2D the material is silicon for wavelength ranges from 800 nm to 980 nm and in some cases from 840 nm to 960 nm and in some cases from 850 nm to 950 nm. According to some embodiments, the material can be germanium in silicon, Ge_xSi_{1-x}, where x can range from 0 to 1, and in some cases 0.01 to 0.1 and in some cases from 0.1 to 0.2 and in some cases from 0.2 to 0.4 and in some cases from 0.4 to 0.8. With the addition of Ge and if the layers are not relaxed, or with strain, the wavelength range can be extended beyond 900 nm, in some cases beyond 1000 nm, in some cases beyond 1200nm, in some cases beyond 1400 and in some cases beyond 1550 nm. In all cases the wavelength range is above the bandgap energy of the GeSi alloy with strain which can further reduce the bandgap energy, and in some cases without strain. The quantum efficiency can range from 40% to 90% or more in at least one wavelength in these wavelength ranges, and in some cases from 50% to 80% or more and in some cases from 60% to 80% or more.

[00164] Microstructure enhancement of the absorption where the bulk absorption without micro/nano-structures can be in the range of a few hundred cm^{-1}, can range from 2 to 10, in some cases from 10 to 50, in some cases 50 to 100 and in some cases more than a 100 times in either Si and/or GeSi alloys PIN, PIPIN photodiode and/or avalanche photodiode structures. In some cases, a strongly absorbing layer of 8000 cm^{-1} or more can be very thin, for example 1 micron or less, such that the absorption can be weak and microstructure holes can

enhance the absorption. In these cases, the incident photons can be mostly collinear with the electric field in the I region. However once the optical field is trapped in the microstructures and propagates within the microstructure and its proximity, the optical mode and field can be very complex and may have some components that may be collinear with the applied electric field in the I region.

[00165] FIG. 3 is a schematic cross section of a N-I-P photodiode structure that can be grown on a silicon substrate or a SOI substrate, according to some embodiments. The I layer can be intrinsic (I) not intentionally doped and/or very low background with a N type doping N^-. In some cases it can be very low background P type doping P^-. In FIG. 3, the I or N^- layer is Ge_xSi_{1-x} alloy with x ranging from greater than 0 to 1, for example for a few percent of x, 1-10% or more, and in some cases 4-8% and in some cases 10-20%, and in some cases 20-40% or more. Due to lattice mismatch between GeSi alloy and Si, a strain is created that can result in a electric field that can assist the transport of electron hole pairs that are generated by photoabsorption. The strain also can narrow the bandgap of the GeSi alloy. By taking advantage of the strain electric field in the same direction as a reverse bias electric field, the photogenerated carriers can be more effectively swept through the I or low doped regions to generate an electrical signal in the external circuits attached to the anode and cathode of the photodiode and/or avalanche photodiode.

[00166] FIG. 4 is a cross sectional schematic drawing of a possible MSPD using the layers shown in FIG. 3, according to some embodiments. The top N^+ layer can have a thickness of 0.1-0.5 microns and doping in the range of greater than $5x10^{18}$ cm^{-3}, and in some cases greater than $2x10^{19}$ cm^{-3} of phosphorous and/or arsenic for example. A thin layer of transparent conducting oxide and/or metal can also be included on top of the N^+ layer to further reduce the sheet resistance. The N^+ layer can be SI and/or GeSi with thickness ranging from 0.1 to 0.5 microns and with doping greater than $2x10^{19}$ cm^{-3}. The I intrinsic layer, or the very low doped N^- (or P^-) layer can have a thickness ranging from 0.5 -3 microns, and in some cases 1.8-2.2 microns, can have a background doping of less than $5x10^{15}$ cm^{-3} and in some cases less than $2x10^{15}$ cm^{-3}. The I or N^- layer can be Ge_xSi_{1-x} with x between greater than 0 and less than or equal to 1. The bottom P layer can be Si and/or GeSi alloy, with thickness ranging from 0.1 to 0.5 microns with doping greater than

$5x10^{19}$ cm^{-3} and in some cases greater than $1x10^{20}$ cm^{-3} with boron and/or aluminum for example. Other dopants may be used in the periodic table for P and N such as carbon, antimony, to name a few but these are less common and seldom used in CMOS processing. The N-I-P layers can be grown on a silicon substrate that can be either P or N doping, or on a SOI (silicon on insulator) substrate with a device layer of either P or N. Microstructure holes 412 are etched into the N-I-P (or P-I-N, or P-I-P-I-N for MSAPDs) structure using both wet anisotropic etch, isotropic etch and dry etching such as DRIE, ICP (inductive coupled plasma), HAR (high aspect ratio) etching as in Wu et al. A mixture of wet and dry etching can be used with a final wet etch to remove any dry etching damage to the Si, GeSi. Hole dimensions, diameter, diagonal, sides, major and minor semi-axis, can range from 200 nm to 3000 nm and in some cases 400 nm to 2000 nm and in some cases from 500 nm to 1800 nm, and spacing between the micro/nano structures can be periodic, aperiodic and/or any combination or periodic and aperiodic; the spacing can range from 0 nm (touching and/or intersecting) to 5000 nm, and in some cases 100 nm to 3000 nm and in some cases 100 nm to 2000 nm and in some cases 100 nm to 1500 nm. The spacing in the lateral directions, such as the x and y directions on a plane for example, can be different and/or the same, can be periodic and/or aperiodic and/or any combination of periodic and aperiodic. Other geometries such as hexagonal, the distance to the nearest neighbor holes can be same or different and can be periodic and/or aperiodic and/or any combination of periodic and aperiodic. Hole dimension can also be different and/or the same as adjacent holes, hole etch depth can also be different and/or the same, hole depth can range from 0.2 microns to 10 microns. As shown in FIG. 4, the holes 412 can be trapezoidal, and/or can have any number of slopes of its sidewalls and can be etched within the top N or P layer, partially into the I layer, through the I layer, partially into the bottom P or N layer, through the P or N layer to the silicon dioxide layer of a SOI wafer for example or to an etch stop layer in a bulk silicon substrate for example.

[00167] Light impinges from the top layer at an angle normal to 50 degrees off normal. The MSPD is operated at a reverse bias voltage applied between the anode and cathode, ranging from -1 to -10 volts and for a MSAPD, a reverse bias voltage is applied between the anode and cathode ranging from -4 to -45 volts.

Electrical signal is extracted via the anode 420 and cathode 422 connected to a transmission line that in turn is connected to signal processing and biasing circuits which can be monolithically integrated with the MSPD/MSAPD into a single chip.

[00168] The wavelength range, depending on the percentage of Ge in Si, for 0% Ge can range from 840 – 960 nm, and with 10% Ge or less in GeSi alloy that is either relaxed or not relaxed, the wavelength can range from 840-990 nm for not relaxed GeSi layer and 840-960 nm for relax, for 20% or less Ge, the wavelength can be extended to 1000 nm and in some cases to 1250 nm for not relaxed GeSi layer and for 40% or less Ge, the wavelength can be extended to 1310 nm. Depending on the amount of strain, the bandgap narrowing of GeSi alloy can vary over a wider or narrower range of wavelengths. Quantum efficiency can be 40% or more at at least one or more wavelengths in the wavelength range.

[00169] With zero external bias, the MSPD with strained GeSi layer can operate in a photovoltage mode and it can be seen that the addition of strain can result in an electric field that can assist in the collection of photogenerated carriers between the N and P regions that can result in a higher quantum efficiency for the photovoltaic cell; quantum efficiency greater than 25% and in some cases greater than 28% under one sun at sea level, air mass 1 (AM1).

[00170] FIG. 5 is a schematic cross section of a MSPD with N-I(N^-)-P structure on P silicon substrate or SOI substrate where the microstructure holes have an initial funnel followed by a more cylindrical hole, according to some embodiments. The shapes of holes 512 can be accomplished by a combination of wet and dry etching, see FIG. 2. The layer structures, microstructure hole dimensions, depth can be similar to those in FIG. 4, with the addition of additional micro/nano structure holes 532 that are etched from the bottom substrate that may or may not include a SOI. The substrate can be thinned from its usual 600-700 microns thickness to under 200 microns for example. These bottom holes 532 can be photonic crystal in design to provide a reflectivity of optical waves that impinge from the top surface back toward the light trapping micro/nano structures for absorption enhancements and therefore the enhancement of the quantum efficiency. Also, the bottom holes 532 can provide a lower effective refractive indices such that optical signal from the top can be reflected back toward the photon trapping structures. The bottom holes can have any shape, periodic and/or aperiodic and the etch

depth can be to the bottom P layer, before the bottom P layer and/or partially into the bottom P layer. The bottom holes can have shapes of cylindrical, pyramidal, trapezoidal, polygonal, rectangular, oval, and any combination of shapes and dimensions.

[00171] FIGs. 6A-6D are diagrams illustrating forming of silicon on holes (SOH), according to some embodiments. The SOH can be formed where the bottom holes 632 can be formed first on a different substrate (FIG. 6B) and subsequently wafer bonded to another wafer using SOI manufacturing methods (FIG. 6C). See, e.g., Singh et al, SILICON ON INSULATOR TECHNOLOGY REVIEW, International Journal of Engineering Sciences & Emerging Technologies, May 2011, Volume 1, Issue 1, pp: 1-16 ©IJESET (incorporated herein by reference and referred to herein as "Singh"), discussing holes similar to silicon dioxide can be buried and the MSPD/MSAPD/CMOS, BiCMOS layers can be grown to the buried hole device layer. The basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene, ceramic, amorphous semiconductor, transparent conducting oxides, spin on glass to name a few, and can be periodic, aperiodic, and any combination of periodic and aperiodic, different and/or same dimensions, different and/or same shaped holes, different and/or same spacings with its nearest neighbor holes. The holes 632 can be filled with gas such as He, Ar, N, Xe, H, to name a few. In addition the holes can be over the entire wafer and/or over only partial of the wafer and/or any patterns on the wafer. The holes 632 in addition to different dimensions can also have different depths. Alignment registration holes can be included such that different devices can be positioned over different hole patterns for that particular functionality. The wafer with holes or any other patterns of voids is then flipped over and wafer bonded to a handle wafer which can include etch stop layers, device layers such as PN junctions, P-I-N or N-I-P layers, and/or any other layers for device fabrication. It can also include ion implanted layers such as H, N, Ar, Xe, Ni, Al, B, As, P, Ga, In, Ge, Si, V, He, Mg, Mn, and/or other elements in the periodic table. Using techniques developed for SOI manufacturing, the device wafer is cut and chemical mechanical polished (CMP) (FIG. 6D) and is ready for growth of further device layers such as MSPD, MSAPD, CMOS and/or BiCMOS for application specific integrated circuits

(ASIC), and other structures such as microwave transmission lines, microwave devices, light emitting diodes, lasers, surface emitting lasers to name a few for monolithic integration into a single silicon chip.

[00172] FIG. 6E is a cross sectional schematic diagram showing the device in FIG 5 fabricated on a substrate SOH (silicon on holes), according to some embodiments. Using similar methods as SOI manufacturing, the oxide layer is replaced by holes 632 that are etched and then bonded to a handle wafer and using SmartCut (as described in Singh) a thin device layer above the holes can be formed and with subsequent chemical mechanical polishing the surface of the device layer can be used for subsequent epitaxial layer growth to fabricate MSPD,MSAPD, CMOS, BiCMOS, lasers, surface emitting lasers, microwave transmission lines, solar cells, and any other optical, electrical, mechanical, chemical, devices, sensors for example. All the MSPD,MSAPD, monolithic integration with CMOS, BiCMOS mentioned in this application can be fabricated on a SOH wafer, in addition to SOI and bulk wafers.

[00173] FIG. 7A is a top view of GeSi and/or Ge on silicon, according to some embodiments. The GeSi and/or Ge can have a top layer of Si and/or GeSi. Due to the lattice difference between the GeSi and/or Ge on Si, the wafer tends to bow after the growth of GeSi and/or Ge on Si layers on silicon wafer, especially for thick layers of GeSi and/or Ge of 1-3 micron range and in some cases 0.5-2 micron range in the case where the GeSi and/or Ge is not relaxed and under strain. For photodetectors, it can be desirable for the GeSi and/or Ge to be under strain as this tends to narrow the bandgap (in lasers strain tend to increase the gain), thereby extending the usable wavelength further into the infrared. However, the bowing of the wafer can be undesirable in high volume manufacturing as many machines used in manufacturing require wafers to be flat or at least with minimal bowing. To remove the overall stain and just allow local strain, a grid pattern in a Manhattan geometry, shown in FIG. 7A, can be etched or in any other pattern such that strain is only at local areas. Material can be etched to the Si layer such that only patches of GeSi and/or Ge remain on the Si, SOI or SOH substrate. In some cases not all the GeSi and/or Ge need to be removed; only sufficient material is etched so that the bowing is less. The wafer can also be planarized with the addition of dielectric, amorphous semiconductor for example and followed by

chemical mechanical polishing. Once it is flat and/or almost flat, high resolution photolithography as those used in CMOS manufacturing, can be used.

[00174] In addition, the islands of GeSi/Si and/or Ge layers can be formed by selective area epitaxial growth where patterns of dielectric such as grids can be deposited on the Si and/or SOI/SOH wafers such that epitaxial Ge and/or GeSi, and/or Si are grown on bare Si surfaces and amorphous Ge and/or GeSi and/or Si can be deposited on the dielectric layer which can be silicon dioxide, silicon nitride, silicon carbide to name a few, and/or no significant deposition occur on the dielectrics.

[00175] In some cases, using selective epitaxial growth, the GeSi alloy and/or Ge can also be grown within the nano/micro structured holes to partially and/or fully fill the holes and/or mushroom over the top surface. The GeSi and/or Ge can be doped P-I-N to match the doping approximately of the layers outside the nano/micro structure holes which can be Si and/or GeSI and/or Ge and/or any combination thereof. See, Montalenti et al, Fully coherent growth of Ge on free-standing Si(001) nanomesas, PHYSICAL REVIEW B 89, 014101 (2014) (incorporated herein by reference).

[00176] FIG. 7B is a top view of a spherical grid pattern of GeSi and/or Ge on silicon, according to some embodiments. As in the case of FIG. 7A, the pattern relieves bowing of a GeSi and/or Ge on Si. The dark lines represent the etched part and the dotted line represent the edge of the wafer. Different grid spacing, and pie cut angles other than 30 degrees, can be used and different etch trench width can be used to optimize device density and tradeoff between grid spacing and bowing tolerance.

[00177] FIG. 7C shows three examples of nano/micro structure holes filled or partially filled with GeSi and/or Ge, according to some embodiments. The holes 712 can be partially filled, fully filled and overflowing with GeSi and/or Ge on a Si and/or SiGe and/or Ge P-I-N (or N-I-P or P-I-P-I-N) structure and any combination of Si, GeSi, Ge layers. For example, the bottom of the hole can be Si, GeSi and/or Ge, the I layer can be Si, GeSi and/or Ge and the top P layer can be Si, GeSi and/or Ge.

[00178] In some cases, the region without the nano/microstructured holes can be Si P-I-N and in some cases it can be Si/GeSi/Si P-I-N and in some cases it can

be Si/GeSi or Si/GeSi or Si or Ge P-I-N (or N-I-P or P-I-P-I-N for MSAPD where P-I-P can be Si and/or GeSi and/or Ge and I-N can be Si for example). After selective area growth of GeSi and/or Ge, additional nano/micro structured holes 714 can be etched to further optimize the enhancement of absorption by photon trapping and/or slow waves for example.

[00179] FIG. 8 is a diagram illustrating a monolithically integrated single silicon chip that can include single and/or multiple combinations of devices, according to some embodiments. Silicon chip 800 can any combination of the following devices: MSPDs; MSAPDs; vertical cavity surface emitting lasers (VCSEL) that are either wafer bonded to the chip and/or have a precision cavity for dropping the VCSEL into as in a silicon platform; CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers; holes for thermal removal, ventilation of the chip; thermal barriers; transmission lines; and microwave components such as inductors. The VCSEL 810, typically made of III-V material can be fluidically assembled on to the monolithic integrated chip with electronics and photodetectors. With post processing steps, electrodes can be attached to the VCSEL to connect the VCSEL(s) to the driver electronics. The VCSEL 810 is positioned in a slot or precision cavity in chip 800. A heat sink at the bottom of the precision cavity can be magnetic to attract the VCSEL and rapid thermal annealing can be used to attach the VCSEL 810. Post processing such as metallic plating can attach the microwave transmission lines from the ASIC 808 to the VCSEL 810.

[00180] FIGs. 9A and 9B are schematic cross sections of a possible MSPD P-I-N structure, according to some embodiments. The device can also be a MSAPD P-I-P-I-N structure where the layers can be Si and/or GeSi and/or Ge compositions and any combinations of Si, GeSi and Ge. The P-I-N layers can be Si and/or GeSi and/or Ge and/or any combination thereof. CMOS and/or BiCMOS layer(s) can be grown on top of the P-I-N (or N-I-P) with or without additional layers.

[00181] The top P^+ layer can be SI and/or GeSi and/or Ge with a thickness ranging from 0.1 to 0.5 microns with a doping greater than $1x10^{20}$ cm^{-3} with boron for example. The I intrinsic layer, or the very low doped N^- (or P^-) layer can have a thickness ranging from 0.5 -3 microns, and in some cases 1.8-2.2 microns, and can have a background doping of less than $5x10^{15}$ cm^{-3} and in some cases less than

$2x10^{15}$ cm^{-3}. The I or N^- layer can be Ge_xSi_{1-x} with x between 0 (and including 0) and less than or equal to 1. The bottom N layer can be Si and/or GeSi alloy and/or Ge, with thickness ranging from 0.1 to 0.5 microns with doping greater than $2x10^{19}$ cm^{-3} with arsenic and/or phosphor for example. Other dopants may be used in the periodic table for P and N such as carbon, antimony, to name a few but these are less common and seldom used in CMOS processing. The P-I-N layers can be grown on a silicon substrate that can be either P or N doping, or on a SOI (silicon on insulator) substrate with a device layer of either P or N and/or on a SOH wafer with device layers of either N or P.

[00182] Microstructure holes 912 are etched into the P-I-N (or N-I-P, or P-I-P-I-N for MSAPD) structure using both wet anisotropic, isotropic etch and dry etching such as DRIE, ICP (inductive coupled plasma), HAR (high aspect ratio) etching as in Wu et al. A mixture of wet and dry etching can be used with a final wet etch to remove any dry etching damage to the Si, GeSi, Ge. Hole dimensions, diameter, diagonal, sides, major and minor semi-axis, can range from 200 nm to 3000 nm and in some cases 400 nm to 2000 nm and in some cases from 500 nm to 1800 nm, and spacing between the micro/nano structures can be periodic, aperiodic and/or any combination or periodic and aperiodic; the spacing can range from 0 nm (touching and/or intersecting) to 5000 nm, and in some cases 100 nm to 3000 nm and in some cases 100 nm to 2000 nm and in some cases 100 nm to 1500 nm. The spacing in the lateral directions, such as the x and y directions on a plane for example, can be different and/or the same, can be periodic and/or aperiodic and/or any combination of periodic and aperiodic. Other geometries such as hexagonal, the distance to the nearest neighbor holes can be same or different and can be periodic and/or aperiodic and/or any combination of periodic and aperiodic. Hole dimension can also be different and/or the same as adjacent holes, hole etch depth can also be different and/or the same, hole depth can range from 0.2 microns to 10 microns. As shown in FIG. 9B, the holes 912 can be trapezoidal, and/or can have any number of slopes of its sidewalls and can be etched within the top P layer, partially into the I layer, through the I layer, partially into the bottom N layer, through the N layer to the silicon dioxide layer of a SOI wafer for example or to an etch stop layer in a bulk silicon substrate or SOI or SOH for example. Ohmic contacts 920 can be added as shown, for reverse biasing.

[00183] The wavelength range, depending on the percentage of Ge in Si, for 0% can range from 840 – 960 nm and in some cases 840 nm to 990 nm, and with 10% Ge or less in GeSi alloy that is either relaxed or not relaxed, the wavelength can range from 840-990 nm and in some cases 840 nm to 1000 nm for not relaxed GeSi layer and 840-960 nm for relax, for 20% or less Ge, the wavelength can be extended to 1000 nm and in some cases to 1250 nm for not relaxed GeSi layer and for 40% or less Ge, the wavelength can be extended to 1310 nm and in some cases to 1400 nm. Depending on the amount of strain, the bandgap narrowing of GeSi alloy can vary over a wider or narrower range of wavelengths. Quantum efficiency can be 40% or more at at least one or more wavelengths in the wavelength range.

[00184] Etch stop layer(s) can be included, for example heavily doped P layer with boron, or carbon and Ge can sometimes be added to compensate for the strain, or a thin layer of GeSi alloy, silicon dioxide buried layer, and/or nitrogen implant. See e.g., Paneva et al, Nitrogen implanted etch-stop layers in silicon, Microelectronic Engineering 27 (1995) 509-512 (incorporated herein by reference). The etch stop layer can be grown on bulk silicon substrate, SOH or SOI wafers. In the case of bulk Si wafer, a via 930 can be etched to remove most or all of the substrate to the etch stop layer which can in addition be patterned with nano-micro structures 914 and/or can be coated with dielectric distributed Bragg reflectors. By removing most and/or all of the substrate beneath the MSPD/MSAPD, provides a semiconductor-air interface and allow optical signal to reflect and/or to be confined mostly in the I region allowing more efficient lateral propagation and improving photon trapping. The lateral propagation of the optical signal within the MSPD/MSAPD can be Bloch modes, slow waves, transverse modes, total internal reflection waves, that can increase the interaction distance and duration of the optical signal with the I layer which contribute the bulk of the photogenerated carriers that are swept out toward the anode and cathode under an externally applied bias voltage which then result in an electrical signal in the external circuits that are connected to the anode and cathode (930).

[00185] As shown in FIG. 9B, the MSPD/MSAPD can be monolithically integrated with silicon electronics such as CMOS and/or BiCMOS ASIC that provide signal processing, amplification, storage, analysis, transmission. Arrays of

MSPD/MSAPD can be monolithically integrated with CMOS/BiCMOS electronics. Such arrays greatly simplify the assembly and packaging of multichannel optical receivers.

[00186] The optical signal can impinge from either the top or bottom surfaces and can be normal and/or off normal by as much as 45 degrees or more. The fiber input angle can range from 0 (normal) to 50 degrees and/or the MSPD/MSAPD can be tilted by 0 (no tilt) to 50 degrees from the vertical axis. The launching of the optical signal off normal can improve the trapping of the optical signal with the MSPD/MSAPD thereby improving the external quantum efficiency (QE) and also reducing the reflection back into the optical fiber which can affect the performance of the optical system.

[00187] FIG. 10 is a cross section view of three funnel shaped holes, according to some embodiments. Within the about the first 400 nm from the surface the holes have a funnel with different sidewall angles of 61 degrees (hole 1016), 68 degrees (hole 1014) and 82 degrees (hole 1012), all measured from the horizontal plane. Each of the holes have a cylindrical portion of approximately 2100 nm with a diameter of 500 nm. The diameters of the top funnel holes are 940 nm at 61 degree slope (hole 1016), 820 nm at 68 degree slope (hole 1014) and 610 nm at 82 degree slope (hole 1012). The period of the holes is 1000 nm in a hexagonal lattice. All the material in this example is silicon. The bottom layer of the holes is silicon dioxide of 2000 nm thick on Si substrate. The diameters, slopes, and three-dimensional shapes can be same for all holes that are in or on the same substrate or can differ between holes in or on the same substrate, for this and other embodiments described in this patent specification. FIG. 11 is a plot showing a FDTD (Finite Difference Time Domain) simulation for the optical field in a structure as shown in FIG. 10. The funnel holes are in a hexagonal lattice with a period of 1000 nm with a certain sidewall angle. The structure is a P-I-N on SOI with 400 nm P layer, 1200 nm I layer and 1100 nm N layer on 2000 nm silicon dioxide on silicon for example (this was the non optimal structure after epitaxial growth where the dopant diffused as used in an experimental testing). The plot shows the QE due to enhanced absorption in the I layer verses incident optical photon wavelength from 800 nm to 900 nm. The solid curve 1116 is for a funnel with a slope of 61 degrees, the dash curve 1114 is for a slope of 68 degrees and the dash dot curve 1112 is for

a slope of 83 degrees. As can be seen from the simulation, the shallow slope funnel of 61 degrees gave the highest QE of approximately 60% from 800-900 nm with a slight droop toward the 900 nm wavelength. For this simulation, the material was all silicon, however the general trend holds for other material such as GeSi and Ge homojunctions, single heterojunctions and/or double heterojunctions and for other wavelength ranges such as 840 nm to 960 nm, 840 nm to 1000 nm, 900 nm to 1250 nm, 1250 nm to 1350 nm, 1350 nm to 1450 nm, 1450 nm to 1550 nm, 1550 nm to 1650 nm, and any wavelength between the ranges mentioned. QE can be 40% or greater at least for wavelengths in the ranges and/or between the ranges.

[00188] Experimental results of QE (external quantum efficiency) of 50-60% were observed at 800-850 nm wavelength with this structure.

[00189] It can be seen that nano/micro structured holes with a wide funnel can be more efficient at absorbing and trapping photons that a similar hole with a higher sloped funnel and/or no funnel.

[00190] FIG. 12A is a plot of a FDTD simulation of a hexagonal lattice with holes given in FIG. 10 where the holes are funnel shaped with a funnel slope of 61 degrees. The vertical axis is QE and the horizontal axis is optical wavelength from 800-900 nm and the material is silicon on SOI. The solid line (1212) is a P-I-N or N-I-P structure on 2000 nm silicon dioxide on silicon substrate where the layer thicknesses are 400 nm for the top doped P or N layer, 1200 nm not intentionally doped and/or intrinsic I layer, and 1100 nm oppositely doped from the top layer N or P layer on 2000 nm SiO_2 on silicon substrate. QE is between 50 and 60% in the wavelength span of 800-900 nm. Dashed line (1214) is for a thinner layer structure of 300 nm doped top layer P or N, 2000 nm I layer, 300 nm oppositely doped from the top layer N or P on 2000 nm SiO_2 on silicon substrate, the QE is between 60 and 70% in the wavelength span of 800-900 nm. Dash dot line (1216) is for a layer structure of 300 nm doped top layer of P or N, 2000 nm I layer, 100 nm oppositely doped from the top layer N or P on 2000 nm SiO_2 on silicon substrate, the QE is between 70-80% for wavelength ranges 800-900 nm. To reduce the series resistance of the thin top layer, transparent conducting metal oxide such as indium tin oxide (ITO) for example, can be used as an additional layer on top of the top 100 nm layer. The ITO is transparent at the infrared wavelengths and can range in

thicknesses of 20nm to 300 nm for example or any thickness that can reduce the sheet resistances to less than 200 ohm square and in some cases less than 100 ohms square and in some cases less than 50 ohms square.

[00191] FIG. 12B is a plot showing the QE of a MSPD as in curve 1216 of FIG. 12A. The MSPD has a P-I-N or N-I-P layer thickness of 100 nm top P or N layer, 2000 nm I layer and 300 nm N or P layer on buried oxide (BOX) layer of 2000 nm on silicon substrate. The QE which is equivalent to absorption in the I layer is between 70-80% in the wavelength range from 800-900 nm. The device layer of the SOI can be P or N for either P-I-N or N-I-P structures. In some cases a pn junction can be formed between the SOI device layer and the bottom layer of a P-I-N or N-I-P MSPD which may or may not have an etch stop layer. The pn junction in some cases can help push away photogenerated carriers in the P or N layer away from the I layer thereby reducing a diffusion of minority carriers to the I region which can cause a slow response due to a "tail" in the impulse response of the MSPD.

[00192] The same thin structures can also be applied to MSAPD where the P-I-P layers are kept thin, of less than 300 nm and in some cases less than or equal to 100 nm.

[00193] Thinner P and N layers can result in higher QE and faster response of the MSPD/MSAPD. The same can be implemented in MSAPD where the P-I-P-I-N, the top layer P can be thin with an additional transparent metal oxide layer to reduce the sheet resistance.

[00194] Bandwidth of the thinner P and N layers MSPD can be greater than 10 Gb/s and in some cases greater than or equal to 20 Gb/s and in some cases greater than or equal to 25 Gb/s and in some cases can be greater than or equal to 30 Gb/s and in some cases greater than or equal to 40 Gb/s and in some cases greater than or equal to 50 Gb/s. With thinner I layer, 50Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved.

[00195] The thin P and N layers can be implemented in P-I-N (or N-I-P) layer structures such as $Si/Ge_xSi_{1-x}/Si$ (P/I/N) double heterostructures, where x can have values from greater than 0 to 1, and in some cases $Ge_ySi_{1-y}/Ge_xSi_{1-x}/Si$ where x and y can have same and/or different values and can range from 0 to 1, and in some cases $Ge_ySi_{1-y}/Ge_xSi_{1-x}/Ge_zSi_{1-z}$ where x, y and z can be same and/or

different values ranging from 0 to 1. It is desirable in optimizing QE and speed of response of the MSPD. The absorbing I layer can be cladded by wider bandgap material that can be less absorbing so that most of the photo generated electrons and holes are generated in the I region of the MSPD/MSAPD (MSAPD have two I regions, one for the absorption of light and the other I region for multiplication; the multiplication I region can be silicon and the absorption I region can be Ge_xSi_{1-x} where x can have values from 0 to 1 and in some cases greater than 0 to 1).

[00196] FIG. 13 is a plot showing the enhanced absorption (1-reflection-transmission) on the vertical axis and wavelength on the horizontal axis from 800-900 nm for an all silicon structure shown in FIG. 10. The total thickness is 2500 nm on 2000 nm of SiO_2 on a silicon substrate. The three plots are for different slope of the funnel, the best result is for a funnel slope of 61 degrees in this example. Over 90% enhanced absorption can be achieved over a wavelength span of 800-900 nm. To maximize the absorption in the I layer, it is desirable to have thin P and N layers in the cases where P and N layers can also absorb photons such as all silicon P-I-N MSPD/MSAPD and in some cases Ge P-Ge I-Si N, and in some cases GeSi P-GeSi-I-Si N, in cases where at least one junction is a homojuction for example. Double heterojuctions where the P and N have larger bandgaps than the I layer, and where the P and N are weakly absorbing, can minimize the generation of photogenerated electron hole pairs in the P and N regions. In addition the optical refractive index of larger bandgap material is in general lower than the refractive index of smaller bandgap material, therefor in the case of a double heterojunction P-I-N where P and N have higher bandgap than the I region can help confine the lateral propagating waves, Bloch waves, slow waves, within mostly the I layer, can improve the absorption of the photons in the I layer which can further enhance the absorption and increase the quantum efficiency. Examples of double heterojunctions are Si P- Ge_xSi_{1-x} I- Si N where x can be greater than 0 but less than or equal to 1. Other examples are Ge_xSi_{1-x} P – Ge_ySi_{1-y} I –Ge_zSi_{1-z} N and where y is greater than x and z and x and z can be the same or different value. X,y,z can have values from 0 to 1. In some cases the x and/or y and/or z can be graded where the values can vary within each P,I,N region. Grading can further help confine lateral photons within mostly the I region such as for a graded index optical fiber or optical waveguide.

[00197] In dry etching there are many techniques of monitoring etch depth, one of the method involves optical interference and/or monitoring the chemical species that are in the etch chamber or exhaust using spectroscopy. See e.g., Collot et al, Dry-etch monitoring of III–V heterostructures using laser reflectometry and optical emission spectroscopy, J. Vac. Sci. Techno!. B 9 (5), Sep/Oct 1991 (incorporated herein by reference). Similarly, in etching Si, GeSi, Ge with P and N dopings optical interference can be used where GeSi/Si can form an optical interference layer, and/or sensing the species of Ge, As, B in the reaction by product during dry etching using a spectrometer either optical and/or mass spectrometer.

[00198] Using etch depth monitoring, thin P and N layers can be used in the P-I-N MSPD (also MSAPD for P-I-P-I-N layers), the thin layers of P and/or N can be fortifiled with transparent conducting metal oxide such as indium tin oxide and/or metal layers to reduce the sheet resistivity. P and N layers can be as thin as 100 nm or less, and can be Si, and/or GeSi and/or Ge.

[00199] FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits. Each such integrated chip can be the optical receiver for either unidirectional and/or bidirectional optical fiber using a single fiber and/or multiple fibers and/or free space applications for optical data communications. On a bulk Si substrate of either N or P doping, and/or a SOI substrate where the device layer can be either N or P doping and/or on a SOH wafer where the device layer can be either N or P doping, on which an etch stop layer of GeSi and/or Si layer(s) can be grown of thickness ranging from 50 nm to 200 nm or more, followed by a highly doped and/or degenerately doped N Si and/or GeSi layer(s) of thickness ranging from 50 nm to 300 nm or more, followed by an intrinsic I layer that is not intentionally doped and/or lightly doped with doping level less than $3x10^{15}$ cm^{-3} that is Si and/or GeSi layer(s) with thickness ranging from 500 nm to 5000 nm and in some cases from 500 nm to 2000 nm followed by highly doped ($5x10^{18}$ – 10^{20} cm^{-3} dopant concentration or higher) and/or degenerately doped (10^{21} cm^{-3} or higher dopant concentration) P Si and/or GeSi layer(s) with thicknesses ranging from 30 nm to 300 nm or more, followed by a buffer Si and/or GeSi layer(s) if necessary and

followed by Si and/or GeSi layer(s) for CMOS/BiCMOS electronics which can have multiple layers of CMOS/BiCMOS electronics which are electrically connected to one or more MSPD and/or MSAPD. In the case of MSAPD, P-I-P-I-N layers are used and where each layer can be Si and/or GeSi layer(s), and in some cases the multiplication I layer adjacent to the N layer is Si. In all the GeSi layer(s), the fraction of Ge in each layer(s) can be same and/or different, and in some cases it is desirable that the I absorbing layer is cladded by higher bandgap material, for example the cladding P and N layers have less Ge and/or no Ge than the I GeSi layer. It should be noted that all layers absorb photons to some extend, but the photogenerated carriers in the I absorbing layer contribute the most to the high speed properties of the MSPD and/or MSAPD. Photogenerated carriers in the P and N regions can result in minority carrier diffusion back to the high electric field I absorbing region that can result in a slow tail to the fast impulse response of the MSPD/MSAPD that can degrade the speed or bandwidth of the MSPD/MSAPD.

[00200] Also shown in FIG. 14 is a via 1430 where the substrate is mostly and/or entirely removed and micro and/or nano structures can be etched or not etched into the bottom layer(s) and further the bottom layer can be coated with a transparent conducting metal oxide such as indium tin oxide and/or semitransparent metal layer and/or metal layer and/or dielectric Bragg reflector layer(s). The Bragg reflector layers can also be a bandpass filter for coarse wavelength division multiplexing (CWDM) applications and light can impinge from the bottom and the via can be a guide for the fiber for example. The top layer(s) can be etched with micro-nano structure holes 1412 using dry and/or wet etching methods and the depth of the holes can range from 50 nm to 3000 nm or more, and in some cases partially into the I layer, and/or through the I layer and/or past the I layer as shown in FIG. 14. The holes 1412 can be periodic in a lattice structure and/or non periodic and/or in a random and/or pseudo random pattern, the holes can have any shape and the shape can vary with depth into the layer(s), the diameter and/or diagonal and/or a measure of its size, can range in value from 250 nm to 5000 nm and in some cases from 350 nm to 2300 nm for wavelength ranges of 800 nm to 1600 nm depending on the composition of the I absorbing layer(s) which can be Si and/or Ge_xSi_{1-x} layer(s) with Ge fraction x ranging from 0 to 1. External quantum efficiency can range from 15% to 90% or more at at least

one of the wavelengths in the range. In some cases for Si I absorbing layer the wavelength can range from 800 to 990 nm with the quantum efficiency (or absorption in the I layer) ranging from 20% to 90% at some wavelengths in the range. In some cases at 990 nm the QE can be equal to and/or greater than 20% and in some cases equal to and/or greater than 40% for a MSPD. Data rate bandwidths can be 10 Gb/s and in some cases 25 Gb/s and in some cases 50 Gb/s and in some cases greater than 50 Gb/s.

[00201] Layer 1450 is a thin ITO like material, and/or thin metal material with thickness ranging from 5 nm to 500 nm or more that can be deposited on the P and/or N layer(s) to reduce the sheet resistance of these layers. In some cases with the addition of transparent conductive metal oxide and/or metal layers the P and N layers can be medium doped ($10^{17} – 10^{18}$ cm^{-3} concentration of dopants) and/or low doped (10^{16} cm^{-3} dopant concentration or less). Ohmic contacts 1420 to the P and N regions are made and transmission lines 1442 connect the MSPD and/or MSAPD to the CMOS/BiCMOS electronics. A reverse bias is applied between the anode and cathode, the bias voltage can range from -2 to -4V and in some cases -2 to -6V for MSPD and -10 to -50V for MSAPD. Light can impinge from the top surface at a normal and/or almost normal incidence to the surface, and in some cases it can be off normal by an angle ranging from 5 degrees to 50 degrees off normal. In some cases, off normal provides less reflection back into the fiber. Reflection can be as low as 5% or less and in some cases 3% or less and in some cases 1% or less from the surface of the MSPD/MSAPD back into the fiber and/or back toward the incident beam of light. The schematic in FIG. 14 only shows basic features for clarity.

[00202] FIG. 15 is a plot of a FDTD simulation of absorption in the I layer which is equivalent to the quantum efficiency of a structure similar to FIG. 10. The funnel angle is 61 degrees and 400 nm in depth followed by a cylindrical section of 2200 nm. The MSPD P-I-N structure is 300 nm P, 2000 nm I and 300 nm N on SOI where the oxide is 2000 nm thick on silicon substrate. The vertical axis is QE (or absorption in the I layer only), and the horizontal axis is wavelength from 800 nm to 990 nm. The material is all silicon. The simulation shows that the QE range from over 70% to approximately 60% over the wavelength span of 800-980 nm, The funnel diameter is 940 nm and the cylindrical diameter is 500 nm, with a period of

1000 nm in a hexagonal lattice. This is just one example of the hole dimensions, other dimensions ranging from 300 nm to 3000 nm and spacing between holes ranging from 50 nm to 3000 nm can be other examples.

[00203] In some cases, the QE at 980 nm can be 10% or greater, and in some cases the QE at 980 nm can be 20% or greater, and in some cases the QE at 980 nm can be 30% or greater and in some cases the QE can be 40% or greater at 980 nm and in some cases the QE can be 50% or greater at 980 nm where the absorbing I layer is silicon. The lower QE can be due to other effects such as scattering and losses due to roughness of the hole's sidewalls. In some cases, smooth side walls of the holes can reduce scattering losses and therefor increase the Q of the collectively connected resonant hole structure for enhancement of the absorption. Q values can range from 2 to 500 or more for example for the microstructured holes for the enhancement of absorption. The Q is typically higher when the material absorption coefficient is low, for example less than 200 cm^{-1} .

[00204] Ingham, Future of Short-Reach Optical Interconnects based on MMF Technologies, OFC 2017 © OSA 2017 (incorporated herein by reference and referred to herein as "Ingham"); and Sun et al, SWDM PAM4 Transmission Over Next Generation Wide-Band Multimode Optical Fiber, JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 35, NO. 4, FEBRUARY 15, 2017 (incorporated herein by reference and referred to herein as "Sun") discuss the use of wavelengths 850, 880, 910, 940, 980 nm for coarse wavelength division multiplexing and using PAM-4 (pulse amplitude modulation using 4 pulses) for an aggregated data rate of over 200 Gb/s on a single multimode fiber. In such applications the linearity of the MSPD is important and MSPD have shown that the linearity of photocurrent vs input optical power is linear to over 10 mW.

[00205] Ingham and Sun discuss an application of MSPD in short reach optical data links. In some cases the MSPD can be monolithically integrated with CMOS and/or BiCMOS electronics such as transimpedance amplifier for example, which can greatly reduce the cost of the transceiver. See, e.g., Tekin, Review of Packaging of Optoelectronic, Photonic, and MEMS Components, IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, VOL. 17, NO. 3, MAY/JUNE 2011 (incorporated herein by reference) and Orcutt et al, Monolithic Silicon Photonics at 25 Gb/s, OFC 2016 © OSA (2016) (incorporated herein by

reference) where cost of packaging can be significantly reduced with monolithic integration of components.

[00206] FIG. 16 is a plot of a FDTD simulation of a structure similar to that of the plot in FIG. 15 but with a thinner top layer of 100 nm rather than 300 nm. The MSPD (can also be MSAPD with the addition of charge and multiplication layers for the situation where gain is 1) P-I-N (can also be N-I-P) where all the layers are silicon with the following thicknesses, P Si 100 nm, I Si 2000 nm and N Si 300 nm on SOI where the buried oxide layer is 2000 nm on a silicon substrate. The thinner top P layer allow more photons into the I layer resulting in an improvement in the QE of the MSPD/MSAPD. The simulation shows response to 990 nm with QE above 60% and in some cases with QE above 20% at 980 nm and in some cases with QE above 30% at 980 nm and in some cases with QE above 40% at 980 nm. The lower QE at 980 nm may be due to scattering losses. The Q at 980 nm may range from 4 to 100 or more.

[00207] A transparent conducting metal oxide such as indium tin oxide can be used on the top layer to reduce the sheet resistivity. The ITO thickness can range from 10 nm to 400 nm. See, e.g., Eshaghi et al, Optical and electrical properties of indium tin oxide (ITO) nanostructured thin films deposited on polycarbonate substrates "thickness effect", Optik *125 (2014) 1478–1481* (incorporated herein by reference).

[00208] FIG. 17 is a plot of a FDTD simulation of a structure similar that plotted in FIG. 15 but with P and N layers of 100 nm thick, for a MSPD P-I-N structure as P Si 100 nm, I Si 2000 nm, N Si 100 nm on SOI with oxide thickness of 2000 nm on silicon substrate. As shown in FIG. 14, materials other than SOI may be used, for example, bulk Si where a via is etched and/or on SOH substrate and where the SOH substrate and/or SOI wafer may have different hole pattern and/or photonic crystal and/or high contrast grating (HCG) and/or grating filters for each MSPD in an array for CWDM where light can impinge from the substrate side through a via. With thinner P and N layers more photons are absorbed in the I layer resulting in higher QE over the wavelength span from 800-990 nm. The Y axis shows absorption in the I layer which is equivalent to QE and the X axis is the wavelength in microns. With the thin P and N layers, metal layers, thin semitransparent metal layers, transparent conducting metal oxide may be used to reduce the sheet

resistance. As shown in FIG. 14 a via in the backside can be etched to allow the coating of a metal or ITO type material to reduce sheet resistance and other dielectrics for reflectivity such as Bragg reflectors. The via can also be used as a light guide and/or to guide an optical fiber toward the MSPD/MSAPD.

[00209] QE can be as high as over 80% at some wavelengths in the range from 800-980 nm, and in some cases over 20% and in some cases over 30% and in some cases over 40% and in some cases over 50% and in some cases over 60%.

[00210] FIG. 18A-18E are schematic diagrams of microstructured holes positioned on a photosensitive surface of a MSPD/MSAPD, according to some embodiments. In FIG. 18A, the microstructure holes 1812 for enhancing absorption can be grouped near the center of the MSPD/MSAPD photosensitive region that can be defined by a mesa 1802 for example. For clarity other components of the MSPD/MSAPD are not shown such as the P or N metal ohmic contacts, electrodes, mesas, passivations, dielectic and/or polyimide, antireflection coatings.

[00211] FIG. 18B shows that in addition to the microstructure holes 1812 in the center for absorption enhancement, the periphery of the photosensitive area of a MSPD/MSAPD can have photonic crystal holes 1814 to reflect laterally propagation optical modes back toward the photon absorbing and absorption enhancement regions.

[00212] FIG. 18C shows microstructured holes 1812 can be in a aperiodic and/or non periodic arrangements as compared to a periodic arrangement shown in FIGs 18A and 18B.

[00213] FIG. 18D shows that the microstructured holes 1812 can have different shapes and sizes and can be periodic and/or non periodically arranged.

[00214] FIG 18E shows that the microstructured holes 1812 can cover most of the photosensitive areas of a MSPD/MSAPD.

[00215] The holes in FIGs. 18A-E, can have characteristic dimensions (diameter, diagonal, average dimensions) that range from 100 nm to 3000 nm and in some cases from 250 nm to 2000 nm and in some cases from 500 nm to 1500 nm and in some cases from 600 nm to 2500 nm. Spacing between adjacent holes and/or nearest neighbor holes can range from 10 nm to 5000 nm and where the holes can be periodic, non periodic, partially periodic, and/or any combination of periodic and/or non periodic and/or randomness. The diameter or characteristic

dimension of the photosensitive area can range from 5 micrometer to 500 micrometers or more. In some cases for high speed applications, the diameter of the photosensitive area can range from 5 micrometers to 100 micrometers and in some cases from 30 micrometers to 80 micrometers.

[00216] FIGs. 19A-19D are a series of cross section views illustrating holes being etched into a buried oxide layer of a SOI wafer, according to some embodiments. FIG. 19A shows the starting wafer. FIG. 19B shows oxide 1904 formed on wafer 1902 and holes 1914 etched in the oxide. In FIG. 19C, the wafer and oxide 1902 and 1904 are flipped and bonded to a handle silicon wafer 1906. In FIG. 19D, the wafer 1902 is cut and/or subjected to CMP. The pattern of holes 1914 can be a one or two dimensional grating, photonic crystal lattice and/or any other hole patterns that can be used as a filter such that a bandpass region exist in the wavelength span. FIGs. 6A-6Dshow an alternative where the holes 632 can be etched directly into silicon. For photons with energies greater than the Si bandgap, oxide with holes is less absorbing and for photon energies less than the Si bandgap, silicon with holes can be used since it is minimally absorbing.

[00217] These holes 1914 are etched in a pattern to allow a bandpass and are etched at specific locations on the wafer such that MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array. This enables coarse wavelength division multiplexing (CWDM) optical signal to be selectively detected by the MSPD/MSAPD and/or photodiodes without absorption enhancement hole arrays.

[00218] Alignment marks can be provided in the oxide and/or silicon such the photolithographic process using stepper at the device level can align to the patterns in the SOI with holes and/or SOH substrates.

[00219] FIGs. 19E-19H are a series of cross section views illustrating holes etched into the oxide of a SOI wafer that are filled with a high index dielectric, according to some embodiments. Examples of the high index dielectric include: hafnium oxide; silicon nitride; zirconium oxide; hafnium nitride; and zirconium. This provides a higher index grating. The holes can be etched partially into the oxide, through the oxide, and/or into the silicon handle substrate. The holes 1916 can be

partially filled, and/or completely filled with another dielectric(s) and/or amorphous semiconductor and can be multiple layers. Surface normal color filters can be fabricated in this manner. See, e.g., Uddin et al, Highly efficient color filter array using resonant Si3N4 gratings, 20 May 2013 | Vol. 21, No. 10 | DOI:10.1364/OE.21.012495 | OPTICS EXPRESS 12497 (incorporated herein by reference and referred to herein as " Uddin"); Jacob et al, Normally incident resonant grating reflection filters for efficient narrow-band spectral filtering of finite beams, Vol. 18, No. 9/September 2001/J. Opt. Soc. Am. A (incorporated herein by reference); and Zhou et al, Surface-normal emission of a high-Q resonator using a subwavelength high-contrast grating, 27 October 2008 / Vol. 16, No. 22 / OPTICS EXPRESS 17282 (incorporated herein by reference). The filter can be photonic crystal, grating and high contrast grating in one and/or two dimensions that are photo lithographically imaged and wet and/or dry etched in to silicon dioxide, any high dielectric such as hafnium oxide, silicon layer(s) substrate prior to epitaxial deposition of MSPD P-I-N layers and/or MSAPD P-I-P-I-N layers in Si and/or GeSi epitaxial layers.

[00220] In some cases photons with wavelengths from 900 nm to 1100 nm can be used with silicon as a photonic crystal, grating and/or high contrast grating Ref. Zhou. For wavelengths 1000 nm and/or longer, Si can be used as a grating and/or high contrast grating and/or photonic crystal.

[00221] FIG. 19I is a diagram showing a silicon wafer having hole patterns etched for bandpass filtering in locations where MSPDs/MSAPDs are to be fabricated, according to some embodiments. Wafer 1950 is a silicon wafer that can be a SOI and/or bulk where holes and/or gratings 1914 (see FIG. 19B) are formed in one or two dimensions. The holes and/or gratings 1914 are etched in specific locations which match the position 1952 where MSPDs/MSAPDs are to be fabricated. The MSPSs/MSAPDs can be fabricated on epitaxial layers grown on the substrate with the holes and/or gratings 1914 forming a bandpass filter and can select the wavelength in a CWDM or dense wavelength division multiplexing (DWDM) optical signal impinging on the bandpass filter prior to impinging on the MSPD/MSAPD. This arrangement allows integration of a bandpass filter specific to each MSPD/MSAPD in an array of two or more MSPD/MSAPD photodetectors that

are monolithically integrated with CMOS and/or BiCMOS electronics including ASICs such as transimpendance amplifiers for example.

[00222] Bandpass filters can also be fabricated on the top surface where the microstructured holes for absorption enhancement are etched. By using a viscous spin on glass polymer, a glassy film can be deposited over the microstructured holes without filling the holes. Subsequent silicon nitride or hafnium oxide can be deposited and a grating in one and/or two dimension can be etched to form a bandpass filter. See, e.g., Uddin.

[00223] FIG. 20 is a cross sectional diagram showing several filters, each having a different passband for each of several MSPDs, according to some embodiments. Note that some or all of the MSPDs can also be MSAPDs. The MSPDs form an array where each MSPD1, MSPD2, MSPD3, … MSPD*n* has a bandpass filter with its own unique bandpass wavelength. Having a different bandpass wavelength for each of the MSPD in the array allows for the selection of specific wavelengths in a CWDM optical signal. One example is to bounce the incoming CWDM signal 2060 off a reflector 2052 and through the first bandpass filter 2014 and into MSPD1 2024. Bandpass filter 2014 is configured such that only a specific wavelength range is transmitted to MSPD1 2024 and the rest of the CWDM signal 2056 is reflected back toward the reflector 2052 where it is bounced into the second MSPD2 2026 and a specific wavelength range is selected for transmitting through the bandpass filter 2016 toward MSPD2 2026, the rest of the CWDM wavelengths 2058 are reflected back toward the reflector 2052 where it then bounce to the next MSPD in the array (MSPD3 2028, having its own bandpas filter 2018). For light impinging from the bottom though a via, the top surface of each MSPD that includes microstructured holes for absorption enhancement can be covered with a dielectric such as spin on glass followed by a metal layer to reflect light that propagates through the P-I-N structure and reflect back toward the microstructured holes for absorption enhancement.

[00224] FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics, according to some embodiments. The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142. Directly below the MSPD/MSAPD are the bandpass filter grating/holes and

via (dotted circle 2130) for allowing light to impinge on the bottom surface and/or to act as a light guide for optical fibers. Each MSPD/MSAPD can have a different bandpass filter that allows a specific wavelength span to be transmitted to the MSPD/MSAPD. The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power. The monolithic integration also significantly reduces parasitic capacitance, inductance and resistances and can significantly improve the performance of the monolithically integrated optical receiver.

[00225] FIGs. 22A and 22B are diagrams illustrating cost savings from using a monolithically integrated MSPD(s)/MSAPD(s) with ASIC(s). FIG. 22A shows a conventional packaging arrangement used in short, medium and long reach optical data communication links. FIG. 22B shows a packaging arrangement according to some embodiments of this disclosure wherein an MSPD/MSAPD is monolithically integrated with ASIC(s) which can include TIA(s), signal processors, storage, transmission electronics, central processing units (CPU), pre amplifiers, amplifiers, etc. into a single silicon chip. In both FIG. 22A and 22B the optical fiber 2250 (e.g MMF) received the optical signal from a VCSEL 2280. The VCSEL 2280 is mounted along with an LD driver 2282 to a multichip carrier 2270. The carrier 2270 in turn is mounted, for example using solder bumps, to a printed circuit board 2260. In FIG. 22A, the photodiode (PD) 2290 is separate from the ASIC 2292 such as TIA (transimpedance amplifier). The PD 2290 and TIA 2292 are each bonded to a substrate 2250, which in some cases is a ceramic multichip carrier, in some cases a glass substrate, and in some cases another silicon piece. FIG. 22B shows an arrangement according to some embodiments of this disclosure, where for short reach, medium reach and long reach optical data communication, the MSPD(s)/MSAPD(s) are monolithically integrated with ASIC(s) on a single silicon substrate 2200 thereby significantly reducing the cost of packaging and parts needed, in addition to improving performance of the optical receiver. See, e.g., Tekin, Review of Packaging of Optoelectronic, Photonic, and MEMS Components, IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, VOL. 17, NO. 3, MAY/JUNE 2011 (incorporated herein by reference); and Doany et al, 300 Gb/s 24-Channel Bidirectional Si Carrier Transceiver Optochip for Board-Level

Interconnects, 2008 Electronic Components and Technology Conference (incorporated herein by reference) which discusses cases where the PD and TIA are separate chips and need to be attached to a third common substrate.

[00226] FIG. 23 is a simple schematic diagram showing MSPDs/MSAPDs in an array, according to some embodiments. Although FIG. 23 illustrates MSPDs/MSAPDs 2300 arranged in a two-dimensional array, in some cases they can be arranged in a one-dimensional array, and in some cases they can be arranged in a three-dimensional array. In all cases the MSPD/MSAPD in the array are monolithically integrated with ASIC(s). The transmission lines from the MSPD/MSAPD are not shown for simplicity. The array can be used for optical data communication. According to some embodiments, the array can be used for light distance and ranging (LIDAR) applications, such as for: vehicles, robots, wheel chairs, drones, and/or smart canes for people with sight impairments. Silicon MSPDs/MSAPDs can be used in wavelength ranges from 780-990 nm, and GeSi MSPD/MSAPD can be used in wavelength ranges 850-1400 nm and longer depending on the Ge fraction in GeSi for the absorbing I layer. The two-dimensional array of MSPDs/MSAPDs can offer an imaging of the light bouncing back from an object or objects. See, e.g., Poulton et al, http://spectrum.ieee.org/tech-talk/semiconductors/optoelectronics/mit-lidar-on-a-chip (incorporated herein by reference); and Rasshofer et al, Influences of weather phenomena on automotive laser radar systems, Adv. Radio Sci., 9, 49–60, 2011 (incorporated herein by reference). Conventional Si PDs can reach 3 Gb/s in the near infrared wavelength ranges. For higher data rates, MSPDs/MSAPDs as described herein can be used. According to some embodiments, MSPDs/MSAPDs as described herein can provide data rates of 5, 10, 20, 25 Gb/s or more with QE better than 30% at near infrared wavelengths. The QE can be further improved using MSAPD for example.

[00227] In some cases, the array can be MSAPDs for LIDAR applications where the I or low doped layer for photon absorption and trapping can be GeSi where the Ge fraction can range from 0 to 1. The structure can be a PIPIN avalanche photodiode structure where the avalanche and/or gain can take place in a Si and/or GeSi I layer, as shown in multiple examples of MSAPDs throughout this disclosure. The data rate bandwidth can be less than a few Gb/s, in some cases

less than 10 Gb/s, in some cases less than 25 Gb/s and in some cases less than 1 Gb/s. The addition of microstructure holes for photon trapping can reduce the overall thickness of the APD and can result in a reduction of the avalanche voltage which can be desirable in some applications, such as those requiring reliability in hostile environments. The photosensitive diameter or lateral dimension of each MSAPD can range from 100 microns to 1000 microns or more. In some cases the lateral dimension of the photosensitive area of a MSAPD in the array can range from 50 microns to 5000 microns. The monolithically integrated chip can have a dimensions such as: millimeters by millimeters; millimeters by centimeters; and centimeters by centimeters. The microstructure holes can be fully passivated to reduce any excess dark current and the MSAPDs can be entirely passivated for reliability. The I low doped layer for photon absorption and trapping can have a thickness ranging from 2 to 10 microns and can be tailored for the data rate bandwidth, responsivity or QE and avalanche voltage.

[00228] In some cases, three-dimensional arrays can be made by stacking two-dimensional arrays (such as shown in FIG. 23) on top of each other and where the top arrays are silicon for example and response to wavelengths from 700-1000 nm and the middle array can be GeSi responding to wavelengths from 1150-1350 nm and the bottom array can be Ge responding to wavelengths of 1400-2000 nm for example and where light impinge from the top surface and where the shorter wavelengths are absorbed first and the top array can be transparent to the longer wavelengths and allow it to pass through. This can be used in LIDAR and/or CWDM and other applications that may have large wavelengths spans. In this described example thee stacked 2D arrays can be provided. According to some embodiments, more than 3 may be possible with changes of Ge fraction in the GeSi alloy.

[00229] In FIGs. 21 and 23 the array of MSPDs/MSAPDs can also include bandpass filters such that specific wavelengths can be addressed to each MSPD/MSAPD and is some cases groups of MSPDs/MSAPDs can have specific bandpass filters. By using color filters and single and/or multiple arrays of MSPDs/MSAPDs, single and/or multiple wavelength imaging LIDAR can be provided for further image processing and enhancement for example to remove background noise and interference.

[00230] In LIDAR applications, the array of microstructured photodetectors (MS-PD) can be microstructured avalanched photodiodes (MSAPD) and where the photosensitive area of the MSAPD can be larger than for a high speed MSAPD for data communications. For LIDAR, the diagonal, assume a square photosensitive region, can range from 50 to 500 micrometers and the thickness of the I layer where photogenerated carriers are swept out due to the high electric field, can range from 500 nm to 5000 nm and in some cases from 500 nm to 2000 nm and in some cases from 500 nm to 1200 nm. LIDAR time resolution can range from 100 ps to nanoseconds. MSAPD allow the layers to be thin and therefore the avalanche voltage can be lower. See e.g., Youn et al, 10-Gb/s 850-nm CMOS OEIC Receiver with a Silicon Avalanche Photodetector, IEEE JOURNAL OF QUANTUM ELECTRONICS, VOL. 48, NO. 2, FEBRUARY 2012 (incorporated herein by reference and referred to herein and "Youn et al"), which shows less than 11V reverse bias and Kang et al, Epitaxially-grown Ge/Si avalanche photodiodes for 1.3μm light detection, 23 June 2008 / Vol. 16, No. 13 / OPTICS EXPRESS 9366 (incorporated herein by reference and referred there herein as "Kang et al 2008"), which shows an approximately -27V reverse bias. With MSAPDs, the mircrostructure holes allowing photon trapping can have thinner layers and therefore lower reverse bias voltage which is desirable in system applications. Reverse bias voltages in the range -6 to -25 volts for MSAPD can be developed and integrated with CMOS/BiCMOS electronics for signal and/or image processing. By timing the time of flight for photons pulses from a vertical cavity surface emitting laser (VCSEL) array at wavelengths that can range from 780nm to 1350 nm and in some cases 850 nm to 980 nm and the time the MSPD and/or MSAPD receives the signal, the distance and/or the image such as the shape of the object reflecting the laser pulses can be determined. For LIDAR applications, sensitivity of the photodetector is important as well as voltage for system reliability, and MSPD and/or MSAPD can be used. As will be described *infra*, microstructure optical waveguide photodiode and/or avalanche photodiode (MSOWPD/MSOWAPD) may also be used for this application.

[00231] FIGs. 24 and 25 are schematic cross section views of a MSAPD with holes that can have various shape, according to some embodiments. Microstructure holes 2412 in general can have any shape, and in some cases are

pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes. Various fabrication techniques can be used alone or in combination including: wet etching; dry etching; ion milling; and other ways of removing semiconductor and/or non semiconductor material. Starting with a silicon substrate that can have a buried oxide (BOX) layer and/or buried hole layer (SOH silicon on hole), and/or with or without an etch stop layer and/or the device layer of the SOI can be N and/or P on which cathode N layer is grown with doping concentration ranging from $5x10^{18}$ to $2x10^{20}$ /cm^3 and thickness ranging from 50 nm to 500 nm; the multiplication Si layer is grown with doping concentration ranging from $1x10^{15}$ to $2x10^{16}$ /cm^3 and thickness ranging from 200 nm to 800 nm and in some cases the multiplication layer can be Ge_xSi_{1-x} where the Ge alloy fraction x can range from less than 1% to 10% or more, followed by a charge layer that can be Si and/or GeSi where the Ge alloy fraction can range from less than 1% to 10% or more and is grown with p-type doping concentration ranging from $8x10^{16}$ to $5x10^{17}$ /cm^3 and thickness ranging from 50 nm to 200 nm; followed by an I (intrinsic and/or not intentionally doped) high field layer where photons absorbed in this region contribute the bulk of the high speed response of the MSAPD to an optical signal, in some cases also called the absorption layer (even though other layers may also absorb photons but have less contribution to the high speed response of the MSAPD to an optical signal), that can be Si and/or GeSi with the Ge alloy fraction ranging from less than 1% to 100% (all Ge) and is grown with doping concentration ranging from $5x10^{13}$ to $6x10^{15}$ /cm^3 and thickness ranging from 500 nm to 5000 nm; followed by the anode P layer which can be Si and/or GeSi where the Ge alloy fraction can range from less than 1% to 100% and is grown with doping concentration ranging from $5x10^{19}$ to $5x10^{20}$ /cm^3 and thickness ranging from 50 nm to 500 nm and in some cases 10 nm to 10000 nm; and in some cases a thin metal such as Ag, Au, Pt, Ni, Cr, Al, Zr, and/or metal alloys and/or silicide such as AlSi, NiSi to name a few and/or transparent metal oxide such as indium tin oxide and/or any combination of metal, transparent metal oxide, silicide and/or other conducting transparent semitransparent to the optical signal material may be used on the surface of the P anode layer to further reduce sheet resistance of the anode layer. Thickness of such layers can range from 5 nm to 500 nm.

[00232] Holes 2412 can have diameters and/or a significant dimension such as a diagonal, ranging from 100 nm to 5000 nm and in some cases ranging from 500 nm to 2500 nm and in some cases ranging from 600 nm to 1500 nm, the hole depth can range from 300 nm to 5000 nm or deeper and in some cases can be partially in the I layer and in some cases to the P charge layer and in some cases partially into the multiplication layer and in some cases to the N cathode layer and in some cases partially into the N cathode layer and in some case through the N cathode layer. A backside via 2430 can be etched to remove the substrate to the oxide layer and/or to the etch stop layer and/or to the N layer which can also be a Si/GeSi Bragg layer. A coating of metal, transparent conducting metal oxide, can be applied to reduce the sheet resistance and in addition a dielectric Bragg reflector and/or dielectric 2432 can be applied to further enhance absorption by reflecting stray light. In addition the Bragg dielectric stack 2432 can be a bandpass filter to allow only certain wavelengths of light to pass through for certain applications where wavelength selective detection is desired such as CWDM and/or bi directional free space optical communication.

[00233] Operational wavelengths for all Si layers can range from 780nm to 980 nm and in some cases from 820 nm to 880 nm and in some cases from 820 nm to 950 nm and in some cases from 840 nm to 980 nm with quantum efficiencies better or equal to 20 % and/or with responsivity better or equal to 0.1 A/W (amp per watt). In some cases the quantum efficiency can be better than and/or equal to 50% at at least one wavelength in the wavelength range of 800 nm to 980 nm.

[00234] With the addition of Ge in the I layer to form GeSi alloy, with the Ge alloy fraction ranging from a few percent to tens of percent, the wavelength can be extended beyond 1000 nm and in some cases to 1300 nm and in some cases to 1450 nm with high Ge alloy percentages. QE can be 50% or better at at least one wavelength in the range 980 nm to 1300 nm and in some cases in the range 980 nm to 1450 nm. In some cases the QE can be 30% or better in at least one wavelength in the wavelength range 980 nm to 1450 nm.

[00235] Metal ohmics and metal electrodes are applied to the anode and cathode layers and a reverse bias voltage ranging from -15 to -45 volts can be applied to the anode and cathode. Light can impinge from the top surface and/or from the bottom surface. Gain bandwidth product of the MSAPD can range from 10

Gb/s to 100 Gb/s or more and in some cases can range from 20 Gb/s to 200 Gb/s or more and in some cases from 100 Gb/s to 300 Gb/s or more.

[00236] The MSPD and MSAPD can be thought of as lossy high contrast gratings with Q ranging from 2 to 1000 as compared to a silicon high contrast grating operating at wavelengths less than the silicon bandgap, and the Q can be as high as one million. In some cases, the smoothness of the side wall of the microstructured holes may be important to achieve Q greater than 20 for example to Q of 100 that can increase the effective optical path in the I layer by 40 to 200 times.

[00237] In addition, metal nanoparticles and/or III-V quantum dots added to the holes, and/or on the surface of the holes, can further assist in the absorption of photons. In some cases, a via may not be implemented.

[00238] FIG. 25 is similar to FIG. 24 except with the addition of a Bragg reflector region at the charge layer of Si/GeSi layers that can be one or multiple periods to reflect partially and/or entirely optical signals that are transmitted through the I layer to further enhance the absorption. The design of the Bragg layer is well known in prior art and consist of quarter wavelength thickness layers ranging from 60-90 nm in thickness per layer at near infrared wavelengths. For example one period Bragg reflector at 980 nm wavelength can be approximately 140 nm thick. In some cases a via may not be required.

[00239] FIG. 26 is schematic diagram illustrating integration of the MSAPD structure in FIG. 24 with CMOS and/or BiCMOS electronics, according to some embodiments. Other possible configurations are also possible and this is just one example. The MSAPD layers are grown first followed by the CMOS and/or BiCMOS layer(s) if any. Not shown in FIG. 26, the anode and cathode of the MSAPD are connected to the electronics circuits and bias circuits of the ASIC CMOS and/or BiCMOS electronics for signal processing, equalization, conditioning, amplification and transmission. The integration of the MSAPD can be a single device and/or an array of MSAPD with a single ASIC and/or an array of ASIC and in some cases, the MSAPD can have bandpass filters for example in the photonic crystal holes in the substrate that can select certain wavelengths of light to convert to electron hole pairs for high speed detection. In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped with

resistivity in the neighborhood of 1-30 ohm-cm or more, and thicknesses ranging from 0.5 to 5 micrometers and in some cases 0.5-2 micrometers and in some cases about 1 micrometer. A P well can be formed on the top I layer by diffusion and/or ion implantation of P type ions such as boron to a thickness ranging from 100 nm to 500 nm and in some cases 100 nm to 300 nm with a resistivity in the neighborhood of 0.01 to 0.001 ohm-cm or less. In some cases a transparent conducting metal oxide such as indium tin oxide and/or a thin metal layer of less than 5nm thick such as platinum can be used on the P doped top surface to reduce the series resistence. CMOS/BiCMOS electronics can be formed on the top I layer with proper P and N wells, dielectrics and metal interconnects as in Swoboda et al, 11Gb/s Monolithically Integrated Silicon Optical Receiver for 850nm Wavelength, 006 IEEE International Solid-State Circuits Conference (incorporated herein by reference and referred to herein as “Swoboda"). In some cases a via 2430 may not be implemented.

[00240] FIG. 27 is schematic diagram illustrating integration of the MSAPD structure in FIG. 24 with CMOS and/or BiCMOS electronics, according to some other embodiments. FIG. 27 is similar to FIG. 24 except only the I layer is GeSi or Si and all other layers are Si. In the case of GeSi I layer, the P is doped by diffusion and/or ion implantation into the I layer as in FIG. 26, the N layer can be Si and is less absorbing to incident photons for example in the 950-980 nm range and the GeSi I layer can be more absorbing. Such double heterojunction is conducive to improving the QE of the MSAPD (MSPD) and can reduce the diffusion of photogenerated carriers in the P and N region which can result in a slower response time for the MSAPD/MSPD. Doping and thickness ranges are similar to those in FIG. 24 except for the surface P doped region into the I layer. An example of integration of the MSAPD with CMOS and/or BiCMOS electronics can be seen showing only the basic layers. CMOS and/or BiCMOS layers and/or P and N wells can be formed directly on the I layer and/or can be grown on top of the I layer. The CMOS and/or BiCMOS electronics can be fabricated first togethter with any concurrent or similar steps such as diffusion and/or doping for the MSAPD/MSPS. This can be followed by forming the MSAPD (MSPD) microstructure holes and the anode and cathode of the MSAPD connected by a transmission line to the electronics and biasing circuits. Reverse bias voltage can range from -6 to -26

volts. Optical signal can impinge either from the top or bottom surface. Metal, transparent conducting metal oxides can be used on the P and N surfaces to reduce sheet resistance. In addition metal and/or dielectric mirrors such as Bragg reflectors can be used on the bottom surface after a via to further enhance the QE of the MSAPD/MSPD. Only the very basic elements are shown for simplicity, passivation, planarization, and many other processing steps and elements are not shown. In some cases, via 2430 may not be implemented.

[00241] FIG. 28 is a table showing experimental measurements of a MSPD with approximately 1000 nm thick I layer, 200 nm N layer and approximately 1500 nm P layer on 2000 nm BOX on silicon substrate, according to some embodiments. The funnel hole structure and spacing is similar to those shown in FIG. 10. The responsivity range from 0.4 A/W to 0.1 A/W in the wavelength range from 800nm to 1000nm. In the KOH only etched holes, the holes are rectangular inverted pyramids. The MSPD have over 10X higher responsivity than a similar photodiode without microstructures to enhance the absorption and therefore the quantum efficiency.

[00242] FIG. 29 is a schematic drawing of a vertical cavity surface emitting laser (VCSEL) being used together with a MSPD/MSAPD that is monolithically integrated with ASIC CMOS and/or BiCMOS electronics for close proximity free space optical data link, according to some embodiments. Device A 2910 includes an optical transmitter 2912 at wavelength 1 and an optical receiver 2914 at wavelength 2. Device B 2920 includes an optical transmitter 2922 and an optical receiver 2924. The two devices 2910 and 2920 can transfer data to each other using the two wavelengths 1 and 2 as shown. The close proximity free space (i.e. no optical cable) link can be used for example with: mobile devices such as tablets, laptops, and smartphones; home entertainment boxes; home security boxes; secure payment at stores; and devices to secure bank transactions. Since the laser light can diverge quickly over short distances, for example less than one meter and in some cases less than 10 centimeters, and in some cases less than 2 centimeters, the communication between devices can be very secure and not picked up by unintended recipients. An example of the close proximity optical link is shown, where the transmitter and receiver can be paired with a certain wavelength in one direction and another wavelength in the opposite direction to minimize cross

talk. According to some embodiments, each mobile device can have multiple ports such that it can multitask several transfers of data simultaneously from multiple devices. Data rates can range from 1 Gb/s to 25 Gb/s or more and in some cases can range from 6 Gb/s to 30 Gb/s or more.

[00243] Safety features can include low power pinging to see if a recipient receiver is nearby in close proximity before increasing the laser power for high data rate low error transfers.

[00244] Other applications can include blade-to-blade free space optical communication in close proximity with multiple high-speed ports at 25 Gb/s and greater and in some cases at 50 Gb/s or greater. The optical transceiver ports can be located on any surface of the blade or mobile device and/or can be attached to an umbilical cord that can be magnetically coupled to another transceiver to complete the optical data link. Arrays of optical ports can be implemented on blades and/or mobile and non mobile devices to increase the aggregated data rates to greater than 40 Gb/s and in some cases greater than 100 Gb/s and in some cases greater than 1 Tb/s. Multiple wavelengths can be used in such arrays to avoid cross talks; wavelengths such as 780, 800, 820, 840, 860, 880, 900, 920, 940, 960, 980, 1000 nm for example and any other wavelengths in between and beyond the ranges given.

[00245] In some cases, RF and microwave frequencies can be used for proximity data transmission. In many prior art proximity RF data links, the RF field is propagating and can be detected by unintended recipients thereby compromising security. Instead of propagating RF or microwave fields, evanescent RF and/or microwave field should be used such that the field is not propagating and can only be transmitted by a close proximity receiver that can couple the evanescent field to the receiver. An example of evanescent RF/microwave field is the use of metamaterial such a RF/microwave superlens where the RF/microwave after the superlens is a near field or evanescent field and decays rapidly over a wavelength distance approximately and can couple to another superlens that is in close proximity of about one wavelength distance and can be detected. Other elements may be also used to detect the evanescent wave such as a microwave coupler.

[00246] FIG. 30 is a cross section view of a basic epitaxial layer structure for monolithic integration of a MSPD with ASICs such as a TIA, according to some embodiments. The layers can be grown on a silicon substrate N or P type, and/or a SOI (silicon on insulator) with a buried oxide (BOX) layer and/or with an etch stop layer and/or with buried holes. If SOI is used, the device layer can be P or N with any resistivity and with a layer thickness ranging from 0.05-0.3 micrometers (micron, um). An N layer (N and P can be interchanged, PIN can also be NIP for different applications and/or fabrication requirements) of Si and/or GeSi where the Ge fraction can range from 0.001 to 0.6 has a thickness ranging from 0.05-0.5 microns and in some cases 0.05 to 0.3 microns (micrometers) and in some cases 0.1 to 0.2 microns, and a doping (xEy is the same as x 10^y dopants/cm^3) of greater than 3E19 and in some cases greater than 6E19 or a resistivity in the range of 0.005 to 0.001 ohm-cm or less. An I Si and/or GeSi layer where the Ge fraction can range from 0.001 to 1, has a thickness ranging from 0.5 to 5 microns and in some cases 0.5 to 2 micrometers and in some cases approximately 1 micrometer. Doping of the I layer is less than 2E15 and/or a resistivity in the neighborhood of 1-30 ohm-cm or greater. The I layer may not be intentionally doped and can have very low P or N doping. In some cases ion implantation during the CMOS integration process and/or diffusion process can form a P^+ region on the surface of the I layer with resistivity in the neighborhood of 0.01-0.001 ohm-cm or less and with a thickness ranging from 50 nm to 500 nm and in some cases 50 nm to 300 nm and in some cases 200 nm. In addition, a Schottky contact and/or ohmic contact with semi transparent metal such as Pt, Al, Cu, Au, Ni, of 50 nm or less thickness and in some cases 10 nm or less, and/or transparent conducting metal oxide such as indium tin oxide (ITO) can be used to further reduce the sheet reisitance of the P^+ layer which can have microstructured holes. In some cases a very thin P layer of 0.05 microns or less can be used and fortified with ITO to reduce the sheet resistance.

[00247] CMOS and/or BiCMOS layer(s) in some cases may be grown on the I layer and if it is not compatible with MSPD/MSAPD processing, the layer(s) can be selectively etched off prior to MSPD/MSAPD processing.

[00248] According to some embodiments, many variations to the structure shown in FIG. 30 are possible such as addition of buffer layers, low temperature

Ge layers, polysilicon layers, other heterogeneous layers such as GaP, InP, GaAs, InN, GaN, AlN, and AlP.

[00249] FIG. 31 is a cross section view showing some aspects of a MSPD integrated with CMOS/BiCMOS ASICs, according to some embodiments. The CMOS/BiCMOS ASICs can include one or more of the following: TIAs; clock data recovery (CDR) circuitry; equalizers; and limiting amplifiers (LA), as some examples. Additional epitaxial layers can be used for the integration of the ASICs can be formed directly on the I layer with P and N wells as discussed in Swoboda. The CMOS and/or BiCMOS ASICs can be first fabricated and some of the steps such as diffusion, ion implantation, and thermal annealing can be grouped together for the MSPD (or MSAPD) processing steps. Ion implantation can be applied to both the ASICs and the MSPD if needed and can be activated together for example. In general, the ASICs can be first fabricated, with some processing steps that can be shared with the MSPD/MSAPD, followed by MSPD microstructure hole etching, wet and/or dry, mesa etching if needed to the cathode N layer and passivation. Anode and cathode ohmics and transmission lines connecting the MSPD to the TIA can be formed after an air bridging, if needed, and/or other insulating step where the transmission lines do not add to extra parasitic capacitance and/or resistances and/or inductances. Mesa diameters can range from 10 to 1000 microns, and in some cases from 20 to 80 microns. Other form of defining the photosensitive area can be disordering of the semiconductor, pn junction isolation, selective P and N junctions on the surface of the I layer, for example. However mesa can have the lowest fringing capacitance. Passivation to the mesa and microstructure holes can be applied to reduce surface recombination.

[00250] The P surface well, for the P-I-N photodetector can be formed by diffusion and/or by ion implantation of P type ions such as boron for example, to a thickness ranging from 50 nm to 500 nm and in some cases 50 nm to 300 nm with a resistivity ranging from 0.01 to 0.001 ohm-cm or less, and in some cases semitransparent metal film such as Pt, Ag, Au, Cu, Ni, or V can be deposited on the surface of the P shallow well prior to hole etch. Thickness of the metal can range from 1 nm to 50 nm. In some cases transparent conducting metal oxide can be used such as indium tin oxide.

[00251] The diameter or diagonal of holes 3112 can range from 200 to 3000 nm and in some cases from 400 to 2500 nm and in some cases from 600 to 1800 nm. Holes 3112 can have same and/or different diameters. Spacing of the holes can range from 10 to 5000 nm and in some cases 10 to 2000 nm and in some cases 10 to 1000 nm and in some cases at least one point of the hole touches the adjacent hole. Holes 3112 can be periodic or aperiodic. The pattern can be periodic in groups of holes while being aperiodic within the group. Holes 3112 can be shaped as a funnel, inverted pyramid, cylindrical, hourglass, rectangular, polygonal, amoebic, and/or other shapes. The sidewalls can be smooth and/or textured. The holes 3112 can be etched to a depth ranging from 0.2 to 5 microns, and in some cases partially into the I layer and in some cases through the I layer and in some cases to and/or into the N (orP) layer and in some cases through the N (or) layer.

[00252] Transparent and/or semi transparent metal and/or transparent conducting metal oxide 3150, such as ITO can be used on the P and N layer to reduce the sheet resistance as shown in FIG. 31.

[00253] A via 3130 can be etched through the substrate to the BOX and/or etch stop layer and/or to the N cathode layer such that a metal and/or ITO and/or dielectric layer(s) 3132 can be deposited to reduce the sheet resistance and/or to reflect optical signal back toward the microstructure region for further absorption enhancements. The bottom N layer can be textured and/or with microstructure holes.

[00254] Tavernier et al, Power Efficient 4.5Gbit/s Optical Receiver in 130nm CMOS with Integrated Photodiode; Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European (incorporated herein by reference and referred to herein as “Tavernier 2008”) discusses a silicon photodiode integrated with CMOS electronics. The stand alone silicon photodiode has reported bandwidth of 500 MHz and responsivity of 5mA/W at 850 nm. With integration to a TIA, the bandwidth improved to 4.5 Gb/s and responsivity improved to 74mA/W. Monolithic integration can significantly improve the performance of a stand alone MSPD or MSAPD.

[00255] CMOS Manufacturing Process, EE141 UCBerkeley, http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_s02/Lectures/Lecture5-

Manufacturing.pdf (incorporated herein by reference) discusses basic processes for CMOS process which are compatible with MSPD/MSAPD processes.

[00256] Data rates can range from 3 to 100 Gb/s or more; operating wavelength range for all silicon layers can range from 800-1000 nm with responsivity greater than or equal to 100mA/W and in some cases greater than or equal to 300mA/W and in some cases greater than or equal to 600 mA/W and in some cases greater than or equal to 800 mA/W for at least one wavelength in the range.

[00257] With a GeSi I layer and with Ge fraction ranging from 0.01 to 1, the wavelength can range from 800-1600 nm and in some cases from 900 to 1100 nm and in some cases from 950-1350 nm and in some cases from 990 to 1350 nm and in some cases from 990 to 1100 nm and in some cases from 1250-1550 nm and in some cases from 1250 to 1450 nm. The responsivity can be greater than or equal to 100mA/W and in some cases greater than or equal to 300mA/W and in some cases greater than or equal to 600 mA/W and in some cases greater than or equal to 800 mA/W for at least one wavelength in the range.

[00258] A reverse bias voltage ranging from -2 to -10 Volts or more and in come cases -1 to -4V and in some cases -3.3V can be applied to the anode and cathode of the MSPD or MSAPD.

[00259] Light shields can be added on top of the TIA/ASICs so that stray light does not interfere with the CMOS operation. The light shield can be a low dielectric constant polymer, black paint, and/or any other material to block the light illuminating the CMOS ASICs. The light shield can be on the front and/or on the back of the substrate. The backside via is optional and is used if optical signals impinge from the backside. In some cases the via can be etched to the BOX layer.

[00260] FIG. 32 is a diagram showing a monolithically integrated MSPD with TIA and other ASICs that is flip chip mounted on a printed circuit board using solder bump technology, according to some embodiments. The MSPD has microstructure holes 3212. The via 3230 can be also used to guide a multi mode and/or single mode optical fiber 3260 to the MSPD thus simplifying significantly the optical alignment process. The via 3230 can also be at an angle off normal such that the fiber can have an angle off normal to reduce back reflected optical signal back into the optical fiber. Anti reflection coating 3232 can be applied to the back Si surface to further reduce reflection.

[00261] In some cases, the optical signal can impinge from the top surface (lower in FIG. 32), and the monolithically integrated chip can be solder bumped to the printed circuit board using through silicon vias (TSV) to connect the solder bump pads on the bottom surface with the electrode pads on the front surface for example.

[00262] FIG. 33 is a diagram showing a similar structure to FIG. 30 but with selective P layer growth, diffusion and/or ion implantation on parts of the I layer surface, according to some embodiments. The P layer can have a different bandgap material than that of the I layer. The CMOS/BiCMOS layer(s) can be selective area growth on the I layer if needed and can be P and/or N type. The P layer for the PIN MSPD can be formed with ion implantation process for example, using P type dopants such as B,C, Al, Ga, and/or In. A thermal anneal step is used to activate the dopants implanted and/or the P layer can be selective area grown with the same and/or different bandgap as the I layer. The substrate can be silicon p or n type with or without etch stop layers and/or SOI.

[00263] FIG. 34 is a cross section view showing some aspects of a MSPD integrated with TIA/ASICs using a layer structure as in FIG. 33, according to some embodiments. The P layer adjacent to the I layer can be ion implanted and/or selective area grown. Metal film and/or ITO 3450 can be applied as in FIG. 31 to reduce the sheet resistances. Not shown as in FIG. 31 are the transmission lines from the MSPD to the TIA/ASICs. Other features are similar to FIG. 31 including optional via 3430 and metal, ITO and/or dielectric layer(s) 3432.

[00264] In addition, in all the MSPD/MSAPD monolithic integration with CMOS ICs, a light shield 3452 can be added over the CMOS TIA/ASICs such that stray light from the optical signal is kept from impinging on the CMOS transistors, capacitors, which can degrade performance and cause errors. A light shield 3434 can also be added on the bottom of the substrate for bottom illuminated MSPD, MSAPD and/or the light shield can be added on both surfaces, top and bottom. The light shield(s) can be an opaque (to the wavelengths of the optical signal and other light sources) polymer, black form, metal, a combination of dielectric and metal, or other materials that are mostly opaque to near infrared radiation and/or visible radiation.

[00265] If the optical signal is impinging on the top surface where the microstructured holes 3412 are, a via 3430 may not be provided, and in some cases the substrate can be a N or P Si substrate instead of a SOI substrate. In the case of a N substrate, the cathode can also be on the bottom of the N substrate for example.

[00266] FIG. 35 is a cross section view showing an epitaxial layer structure for an MSAPD monolithically integrated with CMOS/BiCMOS ASICs, according to some embodiments. The structure is similar to that of FIG. 30 with the addition of a charge and multiplication layers. The charge P layer can be Si and/or GeSi with Ge fraction ranging from 0.001 to 0.6 or higher and thickness ranging from 0.05 to 0.25 microns and in some cases from 0.1 to 0.3 microns and doping ranging from 8E16 to 3E17 and is between the absorption I layer and the multiplication I layer. The multiplication I layer on top of the cathode N layer can be Si and/or GeSi with Ge fraction ranging from 0.001 to 0.6 and thickness ranging from 0.3 to 1.0 microns and in some cases from 0 to 0.5 microns and doping can range from 1E15 to 1E16 or less or a resistivity of 1-10 ohm-cm or higher. The N layer can have a thickness ranging from 0.2 to 0.5 microns or more, and a resistivity ranging from 0.01 to 0.001 ohm-cm or lower. In some cases a BOX layer may not be provided and a N type silicon substrate may be used.

[00267] Similarly to FIG. 33, the P top layer can be formed by selective ion implantation of dopants such as B, Al, C, Ga, and/or In. Any additional CMOS/BiCMOS layer(s) may be included on the I layer and in some cases, the CMOS/BiCMOS P and N wells can extend into the I layer as discussed in Swoboda. In some cases, the MSAPD process can incorporate any CMOS/BiCMOS layer by either diffusion doping and/or ion implantation and forming a shallow P well. The CMOS/BiCMOS layers can be selectively etched off areas where the MSAPD will be formed. As in FIG. 30 the substrate can be silicon N or P type with or without an etch stop layer, or SOI with p or n device layer.

[00268] FIG. 36 is a cross section view showing some aspects of a MSAPD monolithically integrated with CMOS/BiCMOS TIA/ASICs, according to some embodiments. Features shown in FIGs. 31 and 32 can be applied to this structure including optional via 3630, optional ITO/metal/dielectric coating 3650, and optional light shields 3652 and 3634. With a reverse bias applied between the anode and

cathode of the MSAPD with voltages ranging from -8 to -25 volts, the gain can range from greater than 1 to 10 or more, in some cases the gain can range from 2 to 4 and in some cases the gain can range from 2 to 8 or more. Gain bandwidth product can range from 20 to 300 Gb/s or more. Gain the quantum efficiency can be 50% or greater and in some cases 80% or greater and in some cases 100% or greater and in some cases 200% or greater. Responsivity can be 0.5A/W (amperes/watt) or greater and in some cases 1A/W or greater for some wavelengths in the range 800-1600 nm depending on the Ge fraction in the GeSi alloy which can range from 0 (all Si) to 1 (all Ge). A shallow P^+ well is formed on the surface of the I layer by diffusion of P type dopants and/or by ion implantation of P type ions. The P^+ well completes the P-I-P-I-N MSAPD structure, and can have a thickness ranging from 50 to 500 nm and in some cases 100 nm to 300 nm and can have a resistivity in the neighborhood of 0.01 to 0.001 ohm-cm or lower, In addition, a thin semitransparent metal layer with thickness ranging from 1-50 nm and/or transparent conducting metal oxide (TCMO) such as ITO with thickness ranging from 1nm to 500 nm can be deposited on the P shallow well prior to microstructure hole etch. The addition of metal and/or TCMO can assist in reducing the series sheet resistance of the P^+ shallow well. In some cases, it is desirable to have thin P^+ shallow wells to reduce the generation of photocarriers in the P^+ well that can reduce the overall quantum efficiency and/or reduce the data rate bandwidth of the MSAPD due to photogenerated carriers in the P^+ region diffusing to the high field region in the I layer that can result in a slow “tail” in the impulse response. The wavelength range is similar to the device in Fig 31. Light shield 3652 can be added to protect the CMOS electronics from stray lights, stray optical signals. The I layer GeSi can have Ge fraction ranging from 0 to 1 ($Ge_x Si_{1-x}$ where x can range from 0 to 1)

[00269] In FIG. 1 of Kang et al 2008, a Ge on Si avalanche photodiode is shown. A similar structure can be fabricated with microstructured holes 3612 and where the holes can be etched through the contact layer and into the absorption layer partially and/or entirely. In some cases the holes can be etched to the charge layer and in some cases through the multiplication layer and in some cases to the bottom contact layer. As in Kang et al 2008, passivation can be amorphous silicon (a-Si) and/or silicon nitride.

[00270] FIG. 37 is a top view showing some aspects of a MSPD/MSAPD monolithically integrated with a TIA/ASICs without the solder bumps and/or bond pads, according to some embodiments. The integrated chip 3700 shown can be for a single MSPD/MSAPD 3710 or an array of MSPDs/MSAPDs. The TIA/ASICs 3702 can also have an opaque coating and/or cover 3752 such that any stray light does not impinge on the CMOS that can interfere with the CMOS operation. Light absorbed in the CMOS transistors can generate undesirable electron hole pairs that can change its operating parameters and can cause errors.

[00271] The coating 3752 can be an opaque form like material with low dielectric constant such that is does not load the CMOS. The opaque material can cover the top surface of the TIA/ASIC 3702 for a top illuminated MSPD/MSAPD 3710 and/or the bottom surface of the TIA/ASIC 3702 for bottom illuminated MSPD/MSAPD 3710. For a bottom surface coating (such as coatings 3434 and 3634 in FIGs. 34 and 36), it can be an opaque polymer for example such as black paint.

[00272] Basic fabrication steps can include: CMOS TIA/ASIC steps; etching microstructure holes; forming P ohmic; mesa etch; forming N ohmic; and forming transmission line connecting MSPD/MSAPD anode and cathode to the TIA/ASICs. In some cases, passivation can be inserted before ohmic metal deposition. For example, such passivation can include: oxidation; deposition of aluminum oxide on the side walls using atomic layer deposition; depositing poly silicon and/or a-Si; and depositing dielectrics such as hafnium oxide, silicon dioxide silicon nitride and other dielectrics using atomic layer deposition.

[00273] Data rates can range from 3 to 100 Gb/s or more for the integrated chip consisting of MSAPD/MSPD and TIA and other signal processing and enhancing ASICs, and each MSPD/MSAPD can detect the same wavelength and/or different wavelength with the addition of a bandpass filter that can be deposited on the MSPD/MSAPD in the form of dielectric starts such as Bragg filters for example. Detection at different wavelengths can avoid cross talk.

[00274] The MSAPD/MSPD 3710 can have a photosensitive area that can be circular, square, polygonal and can have a diameter and/or diagonal ranging from 20 microns to 1000 microns and in some cases for high data rate applications from 20 microns to 100 microns and for LIDAR applications from 100 microns to 1000 microns. The distance of the MSAPD/MSPD 3710 to the CMOS/BiCMOS

electronics ICs 3702 can range from a few microns to 1000 microns and in some cases from 10 to 250 microns. The first inner ring can be the anode 3720 and the outer ring can be the cathode 3722 for a P-I-P-I-N MSAPD or a P-I-N MSPD structure.

[00275] FIG. 38 is cross section view showing some aspects of a MSPD/MSAPD monolithically integrated with a TIA/ASICs, according to some embodiments. The structure is similar to that of FIGs. 31 and 34, including microstructure holes 3812, optional via 3830, optional ITO/metal/dielectric coating 3850, and optional light shields 3852 and 3634. In FIG. 38, however, a bottom ion implantation process 3880 is provided, which can either be a blanket ion implantation into the entire bottom surface of the wafer and/or masked such that only certain areas receive the ions from ion implantation. The ion implantation process 3880 can be N type ions such as C, N, P, As, Sb, and/or Bi, implanted into the N layer (or P type ions can be implanted in P layer, ions such as C, B, Al, Ga, and/or In) to further increase the doping concentration that can reduce the sheet resistance and the minority carrier lifetime. A thermal anneal can activate the implanted ions and remove some of the damage caused by ion implantation. See, e.g., Williams, Ion Implantation of Semiconductors, Materials Science and Engineering A253 (1998) 8–15 (incorporated herein by reference).

[00276] In some cases, ions such as Ar, N, O, He, H, and/or Xe can be used to cause damage to the semiconductor in the N or P layer which can further reduce minority carrier lifetime. In addition, in some cases, buried or not buried silicon oxide, silicon nitride layers can be formed with O and/or N ions implanted into the silicon.

[00277] According to some embodiments, ion implantation can also be performed with or without a conducting layer such as a metal and/or silicode layer where the ions can penetrate the metal and/or silicode layer and into the silicon layer and can be followed by a rapid thermal anneal.

[00278] The optical signal can impinge from the top surface and/or from the bottom surface as in FIG. 32. If light is impinging from the bottom surface, the top surface can include a reflector such that light not absorbed can be reflected back toward the absorption enhancing microstructures.

[00279] FIG. 39 is a cross section view an epitaxial layer structure, according to some embodiments. The epitaxial layers are grown on a N or P wafer and where the layers can consist of an intrinsic I Si and/or GeSI layer where the background doping of N or P type is less than $2x10^{15}$ /cm^3 (< 2E15) and can have a thickness ranging from 500 nm to 2500 nm and in some cases 500 nm to 3500 nm or more. CMOS layer(s) for TIA/ASICs and other electronics can be grown on the I layer. Not shown are etch stop layers that can be grown prior to the I layer, marker layer(s) which can contain a signature ion that can be inactive and/or active, used for dry etching and the etch is monitored by a mass spectroscopy where when the signature ions are detected, it is know that etching has reached that layer. Other etch depth monitoring techniques include the use of optical interference, and can include one or more different optical refractive index layers to monitor etch depth. Other etch depth monitoring techniques such as electro chemical etching, resistance monitoring, may also be used.

[00280] Buffer layers, superlattice layers such as Si/GeSi/Si/GeSi for etch depth monitoring, lattice matching, bandgap grading, carrier lifetime reduction, isolation, PN junctions, stress reduction and/or enhancement are not shown but can be included between the Si substrate and/or the I layer and/or between the I layer and/or the CMOS layer(s) and in some case can be embedded in the I layer at any location.

[00281] The Ge fraction of the GeSi in the I layer can have single and/or multiple values, and can range from less than 1% to 100%, (Ge_xSi_{1-x} where x can range from < 0.01 to 1). In some cases Ge fraction range from 1% to 10% and in some cases range from 8% to 20% and in some cases range from 20% to 40% or more and the GeSi layer can be relaxed and/or not relaxed.

[00282] FIG. 40 is a cross section view illustrating some aspects of MSPD - ASIC monolithic integration, according to some embodiments. The CMOS electronics can fully or partially fabricated first. In the cases where there are common processing steps between the electronics and the MSPD, the steps can be grouped together if possible. For example, in the case where the fabrication processes for the CMOS electronics and the MPSD both call for ion implantation of N and/or P type dopants, the rapid thermal anneal process to activate the implanted ions can be processed together for the CMOS electronics and the

MSPD. Other examples of processes that can be grouped together are the ohmic contact anneals for the CMOS electronics and the MSPD.

[00283] In FIG. 40, after TIA/ASICs are mostly formed, P type ions using B for example, can be implanted into the CMOS layer and/or the CMOS layer can be first partially and/or entirely removed to expose the I layer, and P type ions can be implanted into the partial CMOS and/or I layer. P type ions can include B, C, Al, Ga, In for example. A P type region 4084 can be created with doping ranging from $5x10^{19}/cm^3$ to $2x10^{20}/cm^3$ or higher (5E19 to 2E20 or higher) and an implant range from 50 to 250 nm. See, e.g., Table III of Gibbons, Ion Implantation in Semiconductors-Part I Range Distribution Theory and Experiments, PROCEEDINGS OF THE IEEE, VOL. 56. NO. 3, M29A5RCH 1968 (incorporated herein by reference and referred to herein as "Gibbons") which gives the P and N type ions and ion implant energies in to Si with peak position of the ions in Si R_p and the width of the distribution ΔR_p. For example, a multiple staggered implant with energies of 10, 20, 40, 60, 80, 100 KeV can be used to reach a peak depth of 328 nm of B ions and/or a single implant of 100 KeV. The doping is approximately given by dose (ions/cm^2)/ ΔR_p so that to reach 2E20 at 328 nm depth the dose is approximately $1.5x10^{15}$ ions/cm^2.

[00284] A via 4030 is etched in the backside of the Si N (can be P if N and P are interchanged) type substrate to the I layer and/or almost to the I layer and/or to the etch sop/monitoring layers, and/or to the super lattice and ion implant of N type ions such as N, P, As, Sb as given in Table III of Gibbons, can be implanted to create an N type region 4082 with doping ranging from $3x10^{19}/cm^3$ to $2x10^{20}/cm^3$ or higher (3E19 to 2E20 or higher) and with a thickness of implanted ion range of 225 nm at 180 KeV using P ions. Multiple energies can be used to create a smoother distribution of ions in the N region. Dose of approximately 1E15 can be used to reach a doping of approximately 2E20 with 180 KeV P ions in Si. A rapid thermal anneal can be performed to activate the implanted ions.

[00285] According to some embodiments, the P and N regions 4084 and 4082 can also be formed by diffusion. In such cases, dopants of P and/or N type can be diffused into Si thermally from either a solid source that can be deposited on Si surface and/or in close proximity and/or from a gaseous source.

[00286] In addition, Schottky (metal-semiconductor) type junction(s) can be formed at least on either the top and/or bottom Si surface replacing one or both P to I junction and/or N to I junction in the MSPD/MSAPD. In addition to integration, the implant process can also be used for MSPD single and/or array photodiodes.

[00287] Ion implantation processes can also be used for isolation, where ions such as H, O, and/or N can be used and where in some cases O and/or N ions can be implanted to form oxides and/or nitrides of silicon. This method of isolation can be used by it self and/or in conjunction with mesa etching.

[00288] FIG. 41 is a cross section view illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments. From the structure shown in FIG. 40, microstructure holes 4112 are etched into the I layer and in some case can be through the I layer to the N layer and in some case can be into the N layer and in some cases through the N layer. A mesa etch 4160 can also be provided to such that cathode ohmic metal can be deposited on the N region and anode ohmic metal can be deposited on the P region. Interconnect transmission lines from the MSPD cathode and anode to the TIA/ASICs are not shown. Also not shown are passivation and planarization layers. A metal and/or transparent conducting metal oxide such as ITO and/or silicide and/or dielectric and/or Bragg reflectors/filters 4150 and 4132 can be deposited on the P and N regions. The metal, ITO and silicide can reduce the sheet resistance and also provide a more uniform distribution of the electric field to deplete the I layer during reverse bias. A reverse bias of -2 to -10 volts can be applied between the anode and cathode. In some cases, the reverse bias is -2 to -4 volts.

[00289] The optical signal can impinge from either the top (as shown) and/or bottom surface. In addition, as in FIG. 32, the monolithically integrated MSPD and CMOS ASICs can be solder bumped. In some cases, through substrate vias (TSVs) can be implemented on the monolithically integrated MSPD/MSAPD and CMOS TIA/ASICs such that solder bumps can be attached on the substrate side and attached to the PCB. In this case, using the TSVs, a flip chip configuration can be avoided.

[00290] Hole spacing, size, depth, shape, wavelength ranges, QE, responsivity, and data rates can be as described in elsewhere herein, such as in connection with FIGs. 31, 32, 34, 36, 38. Data rates of 3 Gb/s to 60 Gb/s or higher can be attained

by the MSPD/MSAPD. Optical signal wavelengths can range from 800-1000 nm and in some cases 800 nm to 1100 nm and in some cases 800 nm to 1400 nm and in some cases 800 nm to 1600 nm and the QE can be 20% or greater at at least one or more wavelengths in the range and in some cases the QE can be 50% or greater at at least one or more wavelength in the range and in some cases the QE can be 70% or greater at at least one or more wavelength in the range.

[00291] Hole diameters and/or diagonals and/or width range from 350 nm to 2500 nm and in some cases from 400 nm to 3000 nm and in some cases 500 nm to 2000 nm and in some cases 500 nm to 1300 nm. Hole spacing can range from 10 nm to 3000 nm at the surface and in some cases can intersect at at least one point with an adjacent hole. Hole diameter/width can vary as depth and in some cases the diameter/width becomes smaller with depth and in some cases can vary with depth. Holes can be etched wet and/or dry partially into the I layer, through the I layer, to the N or P layer at the bottom, into and/or through the P and/or N layer and in some cases can be etched completely through to the bottom surface.

[00292] In addition, the MSPD and MSAPD have very linear output current verses optical input power. The MSPD have been experimentally observed to have a linear photocurrent-input optical power from less than a mW to over 10 mW. Linearity is important for pulse amplitude modulation (PAM-4). See, e.g., Ingham, Future of Short-Reach Optical Interconnects based on MMF Technologies, OFC 2017 © OSA 2017 (incorporated herein by reference).

[00293] Monolithic integration of MSPD/MSAPD with CMOS ASICs is expected to significantly reduce the cost of an optical transceiver. See, e.g., Assefa et al, Monolithically Integrated Silicon Nanophotonics Receiver in 90nm CMOS Technology Node, OFC/NFOEC Technical Digest © 2013 OSA (incorporated herein by reference), where the authors from IBM state in the introduction: "Monolithic integration of optical transceivers in a standard CMOS foundry is expected to significantly reduce the cost of optical communication links for their wide deployment in datacenters and high- performance computing systems ..".

[00294] In addition, in some applications in high performance computing wavelength ranges include 900-1100 nm and in some cases 900-1065 nm. See, e.g., Taubenblatt, Optical Interconnects for High-Performance Computing, JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 30, NO. 4, FEBRUARY 15,

2012 (incorporated herein by reference). MSPDs/MSAPDs in Si and/or GeSi can address these wavelengths and still be monolithically integrateable with CMOS/BiCMOS ICs such as TIA and/or ASICs for functions such as signal amplification, conditioning, normalization, processing, storage, transmission and other signal enhancements for error reduction processing.

[00295] FIG. 42 is a cross section view illustrating aspects of MSPD monolithically integrated with CMOS/BiCMOS electronics, according to some embodiments. The CMOS/BiCMOS electronics can be for a TIA and can include other ASICs for signal processing, conditioning and transmission. The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer with resistivity of 1 ohm-cm or greater and in some cases 10 ohm-cm or greater and with a thickness ranging from 0.5 to 5 micrometers and in some cases from 0.5 to 2 micrometers. After the microstructure hole etch, the P^+ (or N^+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants. Inverted pyramid holes are shown in FIG. 42 that can be wet etched in KOH solutions and also can be wet etch and/or dry etched to form holes of different shapes. The bottom N layer 4282 can be epitaxially grown on a SOI wafer with a BOX and in some cases on a N type Si wafer without a BOX. Layer 4282 can also be ion implantation and/or diffused with dopants into the device layer of the SOI. In cases where a N substrate is used without BOX and the substrate resistivity is in the range of 0.01 ohm-cm or less, the additional doping and N^+ epitaxial layer may not be provided. A N^+ connecting well 4260 formed by ion implantation and/or diffusion can connect the cathode on the surface to the N^+ layer/region 4282 and in the case of a N substrate the cathode can be on the bottom of the substrate with or without additional connect wells. In some cases a TSV (through silicon via) and/or a deep trench may be provided to connect the bottom cathode to the surface ASICs in cases where a surface cathode is not available. Not shown, for simplicity, are the connecting transmission line electrodes from the MSPD/MSAPD to the electronics ASICs.

[00296] In all ion implantation situations, multiple energy can be used, and single and/or multiple types of ions can be used that can be P type and/or N type

and/or isoelectronic type. Various isolation, formation of dielectrics and N and P type doped regions can be formed to optimize the performance of the MSPD and MSAPD.

[00297] Recently, experimental results were published on the microstructured hole silicon photodiode. See, Gao et al, Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes, PUBLISHED ONLINE: 3 APRIL 2017 | DOI: 10.1038/NPHOTON.2017.37 (incorporated herein by reference and referred to herein as "Gao et al"); which discussed data rates as high as 25 Gb/s attained with quantum efficiency of 50% or greater at 850 nm. Note that in FIG. 5B of Gao et al, the optical current verses power is linear to over 25 mW of optical power. Such linearity of output current to input optical power makes the MSPD attractive for PAM-4 type multi-level amplitude modulation to increase the bit rate of a given optical channel.

[00298] In addition, the number of holes can be singular and/or multiple and the spacing between holes can vary from 10 nm to 10000 nm and the holes can have different shapes such as square, rectangle, and/or polygon with diagonals ranging from 200 nm to 5000 nm and in some cases 500 nm to 2500 nm and can be aperiodically and/or periodically arranged on the surface of the MSPD/MSAPD. In addition, the diameter and/or diagonal and/or a significant measure of dimension of the hole can change with depth and can range from 0 nm (come to a point such as the point at the apex of an inverted pyramide) to 5000 nm.

[00299] The microstructure holes are etched partially into the I or low doped or undoped region, in some cases 10% or less into the I or low doped region, and in some cases 20% or less and in some cases 30% or less and in some cases 40% or less and in some cases 50% or less and in some cases 60% or less and in some cases 70% or less and in some cases 80% or less and in some cases 90% or less.

[00300] FIG. 43 is a cross section view of a structure similar to FIG. 41 except that the holes are etched through the P-I-N structure, according to some embodiments. The holes 4312 can be bound both top and bottom by air and in some cases at least one side (surface) is bound by a dielectric and/or dielectrics and/or metal.

[00301] The bottom surface doping, N type (can be P type with P and N interchanged) can be ion implanted with N type ions such as N, P, As, Sb, Bi, C and in some cases the N layer 4082 can be epitaxially grown in which case the N layer extends past the via 4030 and is between the substrate and the I layer and in some cases can have other layers in between such as etch stop layer(s), buffer layers, buried oxide and/or nitride layer(s), amorphous silicon layers, and/or polycrystalline silicon layers. In addition, with an epitaxial and/or amorphous and/or microcrystalline and/or polycrystalline layer(s), ion implantation can still be used to increase the doping concentration of N (or P) type ions to reduce lifetime and to reduce sheet resistance.

[00302] With the I layer thickness ranging from 300 nm to 3000 nm or thicker, and the P and N layers/regions thicknesses ranging from 100 nm (and in some cases less than 100 nm) to 300 nm (and in some cases more than 300 nm), the bulk of the optical absorption occurs in the I layer and can increase the quantum efficiency. The thin P and N layer/regions 4084 and 4082 can have a transparent metal conducting oxide such as indium tin oxide and/or semitransparent metal layer(s) 4050 and 4032 on their surfaces to reduce the sheet resistance. Doping concentration of the P and N layer/region 4084 and 4082 can range from $5x10^{18}$ /cm^3 to $5x10^{20}$ /cm^3 or greater. The higher doping concentrations also reduce the minority carrier lifetime and therefore any diffusion of photogenerated carriers in the P and/or N layer/region.

[00303] The surface of the holes 4312 can be passivated with native oxide and/or dielectric and/or semiconductor crystalline and/or microcrystalline material. The passivation can also be chemical such as with an HF treatment to reduce surface recombination that can reduce the quantum efficiency. In some cases surface recombination at the surface of holes in the P and/or N layer/region can help reduce the diffusion of photogenerated carriers in the P and/or N layer/region into the high field I region which can degrade the speed/bandwidth response of the MSPD, MSAPD. Thin layer/region of N and P type can reduce the amount of photogenerated carriers in the P and N layer/region and therefore reduce the amplitude of the diffused current. In addition with thinner P and N layer/region the time to diffuse of the photogenerated carriers in the P and N layer/region is shorter and therefore the "tail" of diffusion current is correspondingly shorter. Damage due

to ion implantation, high doping levels are all methods that can be used to reduce the lifetime of minority carriers in the P and N layer/region.

[00304] In some cases, the surface of the substrate, that can be N or P type and with resistivity than can range from 0.1 to 100 ohm-cm for example, can have a surface ion implant of: N and/or P type ions; O and/or nitrogen ions; an inert ion such as Ar, Ne, Xe; and/or ions such as Al, Ni, Pt, Zr, and/or Cr. Such ions can be implanted at and/or beneath the surface of the substrate prior to I layer growth where the I layer can have a resistivity of approximately greater than 8 ohm-cm and in some cases greater than 12 ohm-cm and in some cases greater than 10 ohm-cm and in some cases greater than 5 ohm-cm with a thickness ranging from 500 nm to 3000 nm and in some cases to 5000 nm or more. The implanted ions can behave as an etch stop layer and/or a buried dielectric layer that can also be used for etch stop and/or as a marker layer when the etching is dry etching and the exhaust is monitored by a mass spectrometer such that when it detects Ar and/or Xe and/or other marker ions, then the etching has reached those marker layers. Such methods can be used to precisely etch the via to the correct depth desired.

[00305] In some cases, the I layer can be grown on a SOI wafer where the device layer can be a few to tens of ohm-cm resistivity and the buried oxide can have a thickness ranging from 100 nm to 2000 nm and where the device layer can have a thickness ranging from 50 nm to 500 nm and in some cases the device layer can be greater than 500 nm for high resistivity device layers with resistivity ranging from 5-30 ohm-cm or greater. The I layer can be grown on the device layer with resistivity ranging from 3 to 30 ohm-cm or higher and thickness ranging from 300 nm to 5000 nm and in some cases from 500 nm to 2500 nm. A via can be etched to the buried oxide layer on the substrate side and ion implantation can be implanted through the oxide layer and into the device and/or I layer. Multiple ion energies can be used to create a more uniform distribution of dopant in the device and/or I layer. Single and/or multiple kinds of ions can also be used as dopants.

[00306] FIGs. 44A-44C are cross section views illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments. FIG. 44A is similar to FIG. 41. An isolation trench 4462 is shown that electrically isolates to some extent the MSPD from the CMOS and/or BiCMOS electronics such as TIA and other ASICs. The electrical isolation would be more complete if the substrate

was SOI and the trench 4462 was etched to the buried oxide. Ion implantation to form region 4482 can be implemented from the bottom surface by first etching a via 4430 with a thickness from the implanted bottom region by 10 or 10s or less than 10 micrometers or so to provide some rigidity during thermal anneal. The bottom implant can be P or N type ions. In addition in some cases, bottom implant can be achieved by implanting through the top surface and create a buried P or N type ions in the bottom region. If ion implantation for the bottom P or N type region is initiated from the top surface, then a via will may not be implemented until after thermal anneal and all other processing is complete. A bottom via 4430 can then be etched that can provide higher refraction index contrast and also transparent metal oxide layer and/or metal layers can be deposited as in FIG. 41 to reduce series resistance and sheet resistance.

[00307] In addition in FIG. 44A, P well 4470 and N well 4474 are implanted, P channel 4476 and N channel 4472 are also implanted for the CMOS/BiCMOS electronic transistors. Other layers are not shown for simplicity. See, e.g., Tavernier 2008; Chen et al, A 1.8-V 10-Gb/s Fully Integrated CMOS Optical Receiver Analog Front-End, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 6, JUNE 2005 (incorporated herein by reference). Data rates of 5, 10, 25, 50 Gb/s or higher BiCMOS TIA are possible. See, e.g: Kuchta et al, A 55Gb/s Directly Modulated 850nm VCSEL-Based Optical Link, IEEE Photonics Conference 2012 (IPC 2012) Post Deadline Paper PD 1.5 (incorporated herein by reference); and Lengyel et al, Sensitivity Improvements in an 850-nm VCSEL-Based Link Using a Two-Tap Pre-Emphasis Electronic Filter, JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 35, NO. 9, MAY 1, 2017 (incorporated herein by reference), where MSPDs/MSAPDs can be integrated into such CMOS and/or BiCMOS electronics, ICs for optical receiver applications.

[00308] In addition, complex micro electro mechanical systems (MEMS) can be integrated with CMOS electronics. See, e.g., Ghosh et al, On Integrated CMOS-MEMS System-on-Chip, IEEE-NEWCAS Conference, 2005. The 3rd International (incorporated herein by reference); where such processing methods can be used in the MSPD/MSAPD integration with CMOS ICs for optical receiver applications.

[00309] In addition, FIG. 44A shows a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N, so that using a mass

spectrometer to monitor the exhaust of etching process if such a monitor ion is detected, the etch depth can be determined. Also shown are upper ion implanted region 4484, mesa etch 4460, microstructure holes 4412, and optional ITO, metal, dielectric coatings 4450.

[00310] FIG. 44B shows that after bottom ion implantation and thermal anneal(s) in the integration fabrication process, the via 4430 can be further etched to the desired depth for optimal or near optimal MSPD (or MSAPD) operation.

[00311] FIG. 44C shows that a transparent conducting metal oxide such as indium tin oxide (ITO), and/or a metal layer and/or dielectric coatings 4432 can be used on either the bottom and/or the top surface to reduce sheet resistance.

[00312] FIG. 45 is a cross section view as in FIGs. 44A-44C illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments. In this example, the via 4430 can be filled with another material 4532 such as metal, dielectric, poly silicon, amorphous silicon either fully and/or partially to provide heat sinking and/or possibly reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics.

[00313] In all of the TIAs, ASICs, and any other electronics described herein, the process can be with CMOS technology and/or BiCMOS technology. Bipolar transistors are known to be able to provide high speed at a larger node. See, e.g., Kalogerakis et al, A Quad 25Gb/s 270mW TIA in 0.13μm BiCMOS with <0.15dB Crosstalk Penalty, ISSCC 2013 / SESSION 7 / OPTICAL TRANSCEIVERS AND SILICON PHOTONICS / 7.1 (incorporated herein by reference); Knochenhauer et al, 40 Gbit/s transimpedance amplifier with high linearity range in 0.13 mm SiGe BiCMOS, ELECTRONICS LETTERS 12th May 2011 Vol. 47 No. 10 (incorporated herein by reference); Nishihara et al, 10.3 Gbit/s burst-mode PIN-TIA module with high sensitivity, wide dynamic range and quick response, ELECTRONICS LETTERS 31st January 2008 Vol. 44 No. 3 (incorporated herein by reference); and Racanelli et al, SiGe BiCMOS Technology for Communication Products, IEEE 2003 CUSTOM INTEGRATED CIRCUITS CONFERENCE (incorporated herein by reference).

[00314] FIG. 46 is a cross section view illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments. The starting wafer is a SOI (silicon on insulator) wafer that can have a P type device layer of

thickness 50-500 nm or more and doping range from less than $1x10^{15}$ /cm^3 to greater than $1x10^{20}$ /cm^3 and where to reduce the sheet resistivity, the device layer can be pre selective area ion implanted and annealed with P (or N) type dopants to a doping concentration ranging from $2x10^{19}$/cm^3 to $5x10^{20}$ /cm^3 or greater to reduce the series and sheet resistance (region 4682). A via 4630 can be opened on the substrate side for additional ion implantation and anneal to further reduce the sheet resistance. The I layer is not intentionally doped and can have a very low N type and in some cases a P type ion concentration of less than $2x10^{15}$ /cm^3 and with a thickness ranging from 500nm to 5000 nm and in some cases more than 5000 nm in thickness, and an N type ion such as P, As, Sb can be ion implanted to form a N type region with doping concentration ranging from $1x10^{19}$ /cm^3 to $2x10^{20}$/cm^3 or greater. Thermal annealing can be used to activate the implanted ions. The N type region 4684 thickness can have a range from 50 nm to 500 nm and can be covered with a transparent conducting metal oxide such as ITO 4650 and the microstructured holes 4612 are etch through the ITO and into the I silicon layer and/or I GeSi layer where the Ge fraction can range from 1% or less to 100% where the layer is all Ge. (In all the discussions herein of the I layer, the I layer can be Si and/or GeSI alloy with the Ge fraction ranging from less than 1% to 100%).

[00315] An electrical isolation trench 4662 is etched between the MSPD/MSAPD and the CMOS/BiCMOS electronics to minimize electrical interference. The trench can be etched to the BOX layer. Also shown in FIG. 46 are implanted P well 4670 and N well 4674, and P channel 4676 and N channel 4672 for the CMOS/BiCMOS electronic transistors.

[00316] FIG. 47 is a cross section view illustrating some further aspects of MSPD - ASIC monolithic integration, according to some embodiments. In this example, the MSPD has an I layer that is Si and/or GeSi integrated with CMOS and/or BiCMOS integrated circuits (IC). The circuits can be for amplification and signal processing and can include TIA and other signal processing electronics for an application. An SOI substrate with an N type device layer with resistivity less than or equal to 0.03 ohm-cm and in some cases greater than 0.03 ohm-cm. See e.g., http://www.pveducation.org/pvcdrom/materials/general-properties-of-silicon (incorporated herein by reference). In some cases ion implantation of N type ions can be implanted to decrease the resistivity of the region 4782 below the MSPD to

less than and/or equal to 0.002 ohm-cm. The N type ion implant can either be implanted from the bottom through the BOX layer which can have a thickness from 500 nm to 4000 nm and/or from the starting SOI wafer where selective area ion implantation can be achieved on the device layer and anneal. The MSPD/MSAPD can then be aligned over the region where the N type ions are implanted and the CMOS/BICMOS can be over regions where it is not ion implanted with N type ions.

[00317] In some cases a buried N or P type region can be created by ion implanting through the top surface at high enough energy, 200-400 KeV for example, such that N or P type ions can be implanted in the region at or near the bottom of the I layer and/or the device layer adjacent to the BOX for example.

[00318] A via 4730 can be etched to the BOX layer and/or before the BOX layer and additional reflector such as metal and/or Bragg reflectors can be deposited to reflect back the any optical signal that are not absorbed. In addition, the back Si and/or silicon dioxide layer can be patterned with micro/nanostructures to further improve the enhanced absorption of the I layer.

[00319] The I layer can be very low doped P or N type, with resistivity greater than 2 ohm-cm for N type and greater than 6 ohm-cm for P type, and in some cases greater than 0.2 ohm-cm. The I layer thickness can range from 500 nm to 5000 nm. The CMOS/BiCMOS layers can be etched off partially and/or completely and P type ions can be implanted at single and/or multiple energies and single and/or multiple species of ions (also applicable to bottom N type ion implant), to create a P type doped region 4784 with thickness ranging from 50 nm to 500 nm and with resistivity less than or equal to 0.002 ohm-cm, and in some cases greater than 0.002 ohm-cm. A transparent conducting metal oxide such as indium tin oxide layer 4750 can be used on the top surface where the holes 4712 can be etched through to reduce the sheet resistivity. An electrical isolation trench 4762 can be etched between the MSPD/MSAPD and the CMOS/BiCMOS ICs. Microstructured holes 4712 can have any shape and can be periodic and/or aperiodic; the surface diameter and/or significant dimension of the holes can range from 300 nm to 3000 nm and in some cases from 400 nm to 2500 nm and in some cases from 500 nm to 3500 nm and spacing between nearest neighboring holes can range from 0 nm to 5000 nm or more. Hole depth can range from 200 nm to 5000 nm and the hole can be etched partially into the I layer, and/or through the I layer and/or pass the I layer

to the bottom N or P type layer and/or to the BOX (buried oxide) layer. The hole can have a combination of shapes such as funnel, inverted pyramid, cylindrical, hourglass, spherical, and combination of shapes at different depth of the hole. Hole depth can be uniform and/or non uniform, hole shape can be the same for each hole and/or different for some and/or all holes, hole diameter can be the same and/or different for some and/or all holes, hole spacing with adjacent neighboring holes can be the same and/or different for some and/or all holes. This applies to both MSPDs and MSAPDs. In some cases the microstructure hole depth can range from 50 nm to 5000 nm or more from the surface of the semiconductor.

[00320] The MSPD is connected to the CMOS/BiCMOS ICs with a transmission line (not shown) and the MSPD/MSAPD can be 10 to 300 micrometers or more separated from the CMOS/BiCMOS to reduce optical interference with the CMOS/BiCMOS transistors and other circuit elements. A reverse bias is applied to the anode and cathode of -2 to -10 volts and in some cases -2 to -4 volts for MSPD and -5 to -40 volts for MSAPD. Operating wavelength range for Si I layer can range from 750 nm to 1070 nm and for GeSi can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy.

[00321] Quantum efficiency can be 20% or greater at at least one or more wavelengths in the wavelength span, and in some cases QE can be 30% or greater and in some cases QE can be 40% or greater and in some cases QE can be 50% or greater and in some cases QE can be 60% or greater and in some cases QE can be 70% or greater and in some cases QE can be 80% or greater and in some cases QE can be 90% or greater for MSPD/MSAPD. MSAPD can have over 100% QE with gain and in some cases over 200% QE with gain and in some cases over 300% QE with gain and in some cases over 400% QE with gain.

[00322] Data rates can range from 5 Gb/s to 60 Gb/s or higher and in some cases 10 Gb/s to 25 Gb/s and in some cases 25 Gb/s to 50 Gb/s or more. Also shown in FIG. 47 are mesa etch 4760, as well as implanted P well 4770, N well 4774, P channel 4776 and N channel 4772 for the CMOS/BiCMOS electronic transistors.

[00323] FIG. 48 is a cross section view illustrating some further aspects of MSPD - ASIC monolithic integration similar to FIG. 47, according to some embodiments. The N type device layer of the SOI has sufficiently low resistivity, ranging from 0.005 ohm-cm or less and a thickness range from 100 nm to 500 nm. In some cases the device layer has a resistivity of 1 ohm-cm or more and with a thickness ranging from 50-150 nm, in which case an epitaxial growth of a highly doped N layer is needed with a resistivity of 0.005 ohm-cm or less and with the N layer thickness ranging from 100 nm to 500 nm.

[00324] The holes 4712 as in FIG. 47 can be etched partially into the I layer and/or through the I layer and/or to the BOX layer (thickness can range from 100 nm to 5000 nm and in some cases 500 nm to 2000 nm). The I layer can be Si and/or GeSi alloy with the Ge fraction ranging from less than 1% to 100%.

[00325] Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.

[00326] FIGs. 49, 50A and 50B are top views and a cross section view illustrating some aspects of selective ion implantation for MSPD - ASIC monolithic integration, according to some embodiments. FIG. 49 is a top view showing a starting Si or SOI wafer 4900 where it was masked for selective area ion implantation and where the square or any other shapes such as rectangular, oval, circular, and any combination of shapes, regions 4982 on the surface are areas that are implanted with P and/or N type ions to a resistivity ranging from equal to or less than 0.01 ohm-cm to equal to or less than 0.001 ohm-cm following a thermal anneal process, usually rapid thermal anneal. In addition to the P and/or N type regions 4982 selectively implanted with single and/or multiple ion species and single and/or multiple ion implantation energies, other regions 4966 can be implanted with marker ions such as Ar, Ne, Xe, N, O, and/or Al, at the same and/or different energies. Typically higher energies are used for deeper implants, as an aid for back side via etching to determine the depth of the etching process by monitoring the exhaust from the etching chamber with a mass spectrometer

analyzer. Once the marker ions are seen on the mass spectrometer, the approximate depth of the etching can be determined. Further alignment marks 4960 can be created by etching a mesa or by implanting a metal ion such as Al, Cu, Ni and/or V, so that alignment marks 4960 can be seen by a backside infrared illumination and the mask can be placed such that the MSPD/PSAPD is over the N and/or P type implanted areas 4982. Other alignment marks may also be used for example O and/or N ion implant to create an oxide or nitride rich region such that subsequent epitaxial growth over the alignment marks can result in a polycrystalline, microcrystalline and/or amorphous Si so that it appears different from a shiny single crystal epitaxial regions.

[00327] FIG. 50A is a top view of a Si or SOI wafer shown in FIG. 49 that was selective area ion implanted, thermally annealed and an I layer 5002 of Si and/or GeSi and CMOS/BiCMOS layer(s) grown on top of the selective area implanted Si or SOI wafer. FIG 50B is cross sectional view showing the buried selective area ion implanted regions 4982 and an MSPD/MSAPD 5004 fabricated over one of the selective area ion implanted regions 4982 and the CMOS/BiCMOS IC 5006 is fabricated over areas not directly above regions 4982 that have a buried P and/or N type ions.

[00328] FIG. 51 is a cross sectional view of a microstructured avalanche photodiode (MSAPD) with a $P^+ P^{--} PN^+$ structure on SOI wafer, according to some embodiments. The MSAPD can also be formed on a P or N type silicon wafer, in which case a via (not shown) may be etched on the bottom as described elsewhere herein for MSPD structures. The layer structure for the MSAPD is similar to that of a conventional silicon APD. See e.g., WÊGRZECKA et al, Design and properties of silicon avalanche photodiodes, OPTO-ELECTRONICS REVIEW **12**(1), 95–104 (2004) (incorporated herein by reference). In the MSAPD structure, some and/or all the layers can be Si and/or GeSi grown either on Si P or N type or SOI wafers. The N^+ layer can be grown on a SOI wafer with a device layer that is N type for example and where the device layer thickness can range from 50 nm to 200 nm and the N^+ layer can have a thickness ranging from 100 nm to 500 nm. In some cases, as described herein for MSPDs the device layer can either be selective area implanted with N type dopant and/or implanted from the bottom through a via and through the BOX layer and/or from the top surface at a high ion acceleration

energy and create a buried implant into the device layer. The N^+ layer can have a resistivity ranging from equal to or less than 0.006 ohm-cm. The P layer adjacent to the N^+ layer can have a thickness ranging from 50 nm to 650 nm with a resistivity ranging from 0.2 to 0.06 ohm-cm followed by a P^{--} layer with a thickness ranging from 500nm to 5000 nm with a resistivity ranging from equal to or greater than 3 ohm-cm followed by P^+ layer that can be ion implanted with ions such as B, Al, Ga, In for example with a thickness ranging from 50 nm to 500 nm and with a resistivity ranging from equal to or less than 0.002 ohm-cm. The top surface can include a transparent conducting metal oxide such as indium tin oxide (ITO) (not shown) to further reduce the sheet resistivity. The microstructure holes 5112 can be etched through the ITO and partially into the I layer that can be Si and/or GeSi where the Ge fraction can be less than 1% to 100%. The holes are as described elsewhere herein for MSPDs and can have any shape and/or combination of shapes that include funnel, inverted pyramids, cylindrical, spherical, polygonal, hourglass, and can be etched partially into the I layer and/or through the I layer and/or into the bottom P layer and/or to the bottom N^+ layer and/or to the BOX layer. The hole diameter and/or significant lateral dimension can range from 350 nm to 5000 nm and in some cases from 500 nm to 2500 nm and can have uniform hole diameters and/or non uniform hole diameters and the spacing of the holes with adjacent neighboring holes can range from 0 nm to 5000 nm and in some cases from 100 nm to 3000 nm. The cathode is formed on the N^+ layer (in mesa etch 5160) and the anode formed on the P^+ layer. The MSAPD can be operated in a reverse bias mode between the cathode and anode with w voltage range of -6 Volts to -25 Volts. The MSAPD can have a gain of 2 to 10 dB or more and can have a gain bandwidth product of 60 Gb/s or higher and in some cases 100Gb/s or higher and in some cases 200 Gb/s or higher and in some cases 300 Gb/s or higher. The operation wavelength can have a range from 750 nm to 1070 nm and in some cases 850-950 nm and in some cases 900 nm to 1060 nm and in some cases 950 nm to 1250 nm and in some cases 1250-1350 nm and in some cases 1250 to 1550 nm and in some cases 1000 nm to 2000 nm. In some cases, an I layer can be between the P and N^+ layer and can be called the multiplication layer as discussed previously in MSAPD structures. In FIG. 51, the multiplication takes place in and around the PN+ interface where the electric field is the highest.

[00329] The light and/or optical signal can impinge from the surface with the holes and in some cases, with a via (not shown), light can impinge from the bottom substrate side.

[00330] FIG. 52 is a cross section view of a MSAPD integrated with CMOS/BiCMOS ICs such as TIA and other ASICS for signal processing, according to some embodiments. As in earlier discussions herein on selective area ion implantation, the N^+ layer can be a selective area ion implanted region in which case only a P layer need to be grown on the substrate followed by P^{--} followed by CMOS and/or BiCMOS layer(s) and the P^+ region for the MSAPD can be ion implanted with P type ions. In addition in some cases as discussed earlier for MSPD, ion implantation for the N^+ layer can be implanted with N type ions from the bottom through a via and through the BOX, in which case the device layer of the SOI can be N or N^- doping.

[00331] The device layer of a SOI (layer on top of the BOX) is typically low doped P or N and can have a thickness ranging from 50-300 nm which is not shown in FIG. 52 for simplicity. A N^+ layer is grown on the device N layer with resistivity of 0.006 ohm-cm or less and with a thickness range of 100-500 nm, followed by a P layer of resistivity ranging from 0.07 to 0.3 ohm-cm and a thickness ranging from 50 to 700 nm (in some cases an I layer can be inserted between the N^+ and P to form a N^+IP structure where the I layer can have a resistivity of 0.3 ohm-cm or higher and in some cases 1 ohm-cm or higher and a thickness ranging from 300 to 600 nm) followed by a P^{--} layer with resistivity of 1 ohm-cm or greater and in some cases 8 ohm-cm or greater and in some cases 30 ohm-cm or greater, and with a thickness range of 200 nm to 5000 nm followed by P type ion implantation to the top surface of the P^{--} layer to form P^+ region with resistivity less than or equal to 0.002 ohm-cm and with a thickness ranging from 50 nm to 500 nm. Ion implantation can have single and/or multiple acceleration energies and can have single and/or multiple ion species for either the top and/or bottom implants and/or selective area ion implants. A rapid thermal anneal activate the implanted ions and anode and cathode and microstructure holes 5212 can be formed as in FIG. 51.

[00332] An electrical isolation trench 5262 is etched as shown in FIG. 52 to isolate the MSAPD from the CMOS/BiCMOS electronics. In some cases, the

electronics can be shielded from stray optical signal with a light blocking polymer form for example. Other light blocking methods such as metal, polymer, form can be used. Black polymer form layer can have a low dielectric constant and can be less of a loading factor to the high frequency microwave signals. The isolation trench 5262 can also be partially or fully filled with a light blocking material such as a polymer form, and/or dielectric and/or metal layer for example.

[00333] Optical signals can impinge from the top (surface illuminated) and/or from the bottom through a via (bottom illuminated) and the whole integrated chip can be attached to a printed circuit board either holes facing up or holes facing down using solder bump technology and TSV (through silicon via) to connect the integrated chip electrical and microwave connections to the printed circuit board and/or other boards to external electronics.

[00334] A reverse bias is applied to the anode and cathode of the MSAPD with voltages ranging from -6 volts to -25 volts, in some cases -10 V to -25V.

[00335] The diameter of the mesa formed by mesa etch 5260 that defines the junction area and therefor the junction capacitance can range from 20 to 200 micrometers and in some cases 30 to 100 micrometers and in some cases 30 to 80 micrometers for the MSPD/MSAPD structures. The mesa can also have other shapes such as square, rectangular, polygonal, to name a few. For lower data rate applications, less than 5 Gb/s, the diameter or diagonal can range from 100 to 500 micrometers. The smaller diameters are mainly for high data rate applications with datarate equal to or greater than 10 Gb/s and in some cases equal to or greater than 25 Gb/s and in some cases equal to or greater than 50 Gb/s.

[00336] FIG. 53 is a top view schematic of an array of MSPDs/MSAPDs integrated with CMOS/BiCMOS ICs such as TIA and other signal processing ASICs, according to some embodiments. A single chip 5300 with bond pads 5306 includes an array of MSPDs/MSAPDs 5310 integrated with electronics 5302. In some cases the electronics 5302 can be a single block with transmission lines running to different MSPDs/MSAPDs 5310. The number of MSPDs/MSAPDs 5310 in an array can be 1 to 100 or more and in some cases from 2-16 and can be arranged in any fashion. The distance of the MSPDs/MSAPDs 5310 to the electronics 5302 can have a range from 10 micrometer or less to 300 micrometers

or more, and depends on the size of the array and bandwidth of the application and size of the MSPD/MSAPD.

[00337] In addition, MEMS (microelectromechanical systems) structures can be implemented on top and/or below the MSPD/MSAPD such that a tunable filter can be integrated together on the MSPD/MSAPD and CMOS/BiCMOS electronics to allow coarse wavelength division multiplexing.

[00338] A silicon process allows the integration of MEMS, MSPD/MSA{D and CMOS/BiCMOS ICs to be integrated on a single silicon chip. See e.g., Xie et al, Post-CMOS Processing for High-Aspect-Ratio Integrated Silicon Microstructures, JOURNAL OF MICROELECTROMECHANICAL SYSTEMS, VOL. 11, NO. 2, APRIL 2002 (incorporated herein by reference).

[00339] FIG. 54 is a cross section of a possible layer structure for integrating MSPD/MSAPD with CMOS/BiCMOS electronics, according to some embodiments. In the structure shown, a buffer layer of an intrinsic I layer and/or very low doped P^{-} $^{-}$ type layer, often also referred to as a π layer and/or a very low doped N^{-} $^{-}$ type layer also referred to as an ν layer in the scientific literature. The very low doping layers can have a resistivity of greater than or equal to 1 ohm-cm and in some cases greater than or equal to 10 ohm-cm. The Si buffer layer can have a thickness range of 1 to 4 micrometers. In some cases, the Si buffer layer may contain Ge such that it can be GeSi with Ge fraction less than a few percent. The buffer Si (or GeSi) layer can be between the CMOS/BiCMOS layer(s) and the GeSi I layer (which can be low and/or very low doped P and N type material also with resistivity greater than or equal to 1 ohm-cm.) The GeSi I layer can range in thickness from 0.5 to 2 micrometers and in some cases can range from 0.5 to 5 micrometers. Below this I Ge Si layer can be a Si or GeSi N^{+} layer with resistivity less than or equal to 0.006 ohm-cm with thickness ranging from 0.05 to 0.5 micrometers. Below the Si of GeSi N^{+} layer is can be an N type device layer with thickness ranging from 0.05 to 0.5 micrometers and typically with a resistivity equal to or greater than 1 ohm-cm. Below this can be a BOX layer with thickness ranging from 0.5 to 5 micrometers on top of a handle silicon wafer that can be N type and in some cases P type.

[00340] According to some embodiments, all herein described ranges and/or values in thicknesses, resistivity, doping, ion implant depth and energies, hole

diameters/diagonals, hole spacing, hole depth, quantum efficiencies, responsivity, bias voltages, data rates, operational wavelengths, sheet resistances, photosensitive areas and diameters/diagonals, capacitances, and any other ranges/parameters are not fixed and can vary outside the range suggested by from plus or minus a few percent to 50% or more.

[00341] The buffer layer may or may not be needed for CMOS/BiCMOS device fabrication to minimize interference with its standard process. In some cases the BOX may not be needed. In some cases a via (not shown) can be opened to allow further ion implantation into the N and N^+ layers (in some cases it can be P and P^+ type layers depending on the MSPD/MSAPD layer doping structures) and in some cases, the wafer can be selective area ion implanted such that the MSPDs/MSAPDs are over the heavily doped areas of the silicon or SOI wafer.

[00342] FIG. 55 is a cross section view illustrating some aspects of MSPD/MSAPD integration with CMOS/BiCMOS integrated circuits, according to some embodiments. The MSPD(s) and/or MSAPD(s) with the inclusion of an avalanche region(s), are integrated with CMOS/BiCMOS integrated circuits such as TIA(s), and/or other signal enhancements and/or processing and/or storage and/or communication ASICs. Many parts are not shown such as CMOS/BiCMOS transistors, capacitors, inductors, resistors, interconnect layers to form the ICs, transmission line between the MSPD(s)/MSAPD(s) to the ICs, isolation layers, additional transparent conducting metal oxide layer(s) to reduce sheet resistance, anti-reflection coatings, and passivations for simplicity and clarity.

[00343] The CMOS/BiCMOS ICs are first processed fully and/or partially followed by the processing of the MSPD/MSAPD. The buffer layer can be etched off and selective area ion implantation, by masking off regions not intended for ion implantation with polymer and/or metal layer(s), of P type ions can be implanted into the I GeSi layer (or Si layer in some cases) to form a highly doped P type region 5584 with resistivity less than or equal to 0.003 ohm-cm with a thickness ranging from 0.05 to 0.3 micrometers using single and/or multiple ion implant energies and single and/or multiple ion implant species. A transparent conducting metal oxide (not shown) can be deposited on the P region to further reduce the sheet resistance. Holes 5512 can then be etched through the transparent conducting metal oxide such as indium tin oxide and into the I GeSi (or in some

cases Si layer) as also described herein *supra*. In some cases the P and N type can be reversed, where the top implant can be N type and the bottom layer can be P type. The anode is formed on the P type region 5584 and cathode on the N type layer/regions. An electrical isolation trench 5562 can be etched between the MSPD/MSAPD and the CMOS/BiCMOS ICs.

[00344] In some cases, the bottom N or P layer can be formed by ion implantation from the top surface at high energy creating a buried N or P region. BOX layer can be used to minimize diffusion current generated outside the high field I or low doped regions; however without BOX then an etch stop layer such as a highly doped P layer can be used when etching vias.

[00345] The GeSi I layer or very low doped layer can have Ge fraction ranging from a few percent to 100 percent. In some cases the Ge fraction can range from 1 to 10%, in some cases between 10 and 20%, and in some cases between 20-40% and in some cases between 40-80% and in some cases between 80-100%.

[00346] The microstructured holes 5512 can be etched wet and/or dry partially into the I layer and/or through the I layer and/or to the BOX layer. The holes can be funnel, cylindrical, rectangular, triangular, polygonal, and can vary in lateral dimension as a function of etch depth. Hole diameter, diagonal can range from 300 nm to 5000 nm and in some cases from 450 nm to 2500 nm and in some cases from 500 nm to 2500 nm. Hole spacing can range from 50 nm to 5000 nm and in some cases from 300 nm to 3000 nm. Operating wavelength can range from 750 nm to 2000 nm and in some cases 840 nm to 1065 nm and in some cases 1100 nm to 1350 nm and in some cases 1550 nm to 2000 nm and in some cases from 1200 nm to 1550 nm. Data rates can range from 1 Gb/s to 5 Gb/s and in some cases 1 Gb/s to 10 Gb/s and in some cases 5 Gb/s to 25 Gb/s and in some cases 4 Gb/s to 10 Gb/s and in some cases to 50Gb/s or higher. Responsivity can be 0.2A/W or higher at at least one of the wavelengths in the wavelength span. And in some cases 0.1A/W or higher at at least on wavelength and in some cases 0.3 A/W or higher at at least one wavelength in the span and in some cases responsivity can be 0.5A/W or higher at at least one wavelength in the wavelength span.

[00347] The optical signal can impinge from the top surface where the microstructured holes 5512 are etched and in some cases the optical signal can

impinge from the bottom surface through a via (not shown) such as a through a silicon via (TSV).

[00348] Additional coatings can be included to further enhance the absorption by reflecting any stray optical signal back toward the microstructure holes as discussed earlier. The coating can be metal and/or dielectric on either of the top or bottom surfaces.

[00349] In addition, the die can contain either a single MSPD/MSAPD and CMOS/BiCMOS electronics or multiple MSPDs/MSAPDs and CMOS/BiCMOS electronics for parallel optical fiber applications or CWDM applications. Other applications can include LIDAR, free space optical links, sensors, data center optical interconnect, and fiber to the home.

[00350] In the integrated MSPD and CMOS/BiCMOS electronics the MSPD is operated at a reverse bias between the anode and cathode with applied reverse bias voltage ranging from – 1V to -5V.

[00351] Doped regions that are created by ion implantation methods can also be created using diffusion methods and/or a combination of diffusion and ion implantation.

[00352] FIG. 56 is a cross section view illustrating some aspects of MSPD/MSAPD integration with CMOS/BiCMOS integrated circuits, according to some embodiments. The MSPD/MSAPD is integrated with CMOS/BiCMOS electronics that are fabricated using standard CMOS/BiCMOS processes. The electronics may include additional CMOS/BiCMOS layer(s). The structure uses an I or very low doped P or N type Si layer on an optional BOX. The bottom N or P type region 5682 can be buried ion implanted and/or diffusion before the growth of the I layer and/or low doped layer. In some cases the buried implant can be a selective area implant such that only regions under the photodiode is implanted and/or selective area diffusion. In some cases, a blanket ion implantation and/or diffusion may be used. Thermal anneal can be used to activate the ion implanted areas with P and/or N type dopants. The buried N or P layer 5682 can be close to the BOX layer, when a BOX layer is included. The buried N or P layer 5682 can have a resistivity of less than or equal to 0.01 ohm-cm and in some cases less than or equal to 0.002 ohm-cm. The buried implanted region 5682 can have a thickness of 100 nm to 500 nm. In some cases the buried N or P type layer 5682 can be doped

using a diffusion method instead of ion implantation and the diffusion of dopants can be selective area diffusion. The N or P doped region 5682 can then be buried by the growth of the I or low doped layer. In some cases, during epitaxial growth, some dopant may diffuse into the I or low dope region. See, e.g., Swoboda. The I or low doped region can have a layer thickness ranging from 0.5 to 5 microns and in some cases 0.5 to 2 microns and a resistivity in the neighborhood fo 1-10 ohm-cm or greater.

[00353] The top surface layer 5684 can be P (or N) type ion implantation and/or diffusion also with resistivity less than or equal to 0.002 ohm-cm with a thickness ranging from 100-500 nm. In addition a transparent conducting metal oxide can be used on the top surface to further reduce the sheet resistance.

[00354] The microstructured holes 5612 can be etched wet and/or dry partially into the P or N doped region and/or partially into the I layer or low doped P or N layer, and/or through the I layer or low doped P or N layer, and/or to the BOX layer and/or to the bottom doped layer in the case without a BOX. The holes 5612 can be funnel, cylindrical, inverted pyramid, ball shaped, rectangular, triangular, polygonal, and can vary in lateral dimension as a function of etch depth. Hole diameter, diagonal can range from 300 nm to 3500 nm and in some cases from 450 nm to 2500 nm and in some cases from 500 nm to 2500 nm. Hole spacing can range from 50 nm to 3500 nm and in some cases from 300 nm to 3000 nm. Operating wavelength can range from 750 nm to 1065 nm and in some cases 840 nm to 1065 nm and in some cases 950 nm to 1065 nm and in some cases 840 nm to 1100 nm. Data rates can range from 1 Gb/s to 5 Gb/s and in some cases 1 Gb/s to 10 Gb/s and in some cases 10 Gb/s to 25 Gb/s and in some cases 4 Gb/s to 10 Gb/s and in some cases 25-50 Gb/s or higher. Responsivity can be 0.2A/W or higher at at least one of the wavelengths in the wavelength span. And in some cases 0.1A/W or higher at at least on wavelength. And in some cases 0.3A/W or higher at at least on wavelength. And in some cases 0.4A/W or higher at at least on wavelength. And in some cases 0.5A/W or higher at at least on wavelength.

[00355] The integrated MSPD is operated at a reverse bias between the anode and cathode with a reverse bias voltage ranging from -1 V to -5 V.

[00356] The integrated MSPD/MSAPD and CMOS/BiCMOS electronics can be a single or multiple MSPD/MSAPD and electronics for parallel fiber and/or CWDM

applications. Other applications can include LIDAR, free space optical communication, data center optical interconnect, high performance computing, fiber to the home, sensors, and Lifi.

[00357] The optical signal can impinge from the top, surface illuminated, and/or from the bottom through a via (not shown).

[00358] The photosensitive region of the MSPD/MSAPD can be circular, rectangular, polygonal, quarter circle, or any other shape. For circular photosensitive the diameter can range from 10 micrometer to 500 micrometer or more depending on the application and data rate needed. For data rates of 10Gb/s to 25 Gb/s the diameter can range from 20 micrometer to 80 micrometer or more for example. For lower data rate applications, larger area MSPD/MSAPD can be used with diameter ranging from 50 to 500 micrometers or more.

[00359] In some cases, using a standard CMOS wafer and fabricating a silicon photodiode as discussed in Tavernier 2008, the responsivity at 850 nm was reported as 5mA/W. With the addition of microstructured holes to the silicon photodiode, the responsivity can be significantly improved by several factors and in some cases by order of magnitude or more. With the addition of microstructured holes, the absorption of silicon photodiodes can be enhanced and extend the operational wavelength to 900 nm and in some cases to 990 nm and in some cases to 1065 nm and in some cases to 1100 nm and in some cases to 1170 nm. See, e.g., Tavernier 2008. With the addition of a few percent or more of Ge to form a GeSi I layer, the wavelength can be further extended beyond 1170 nm.

[00360] FIG. 57 is cross section view of a CMOS/BiCMOS wafer on SOI for use in integration with MSPDs/MSAPDs, according to some embodiments. The structure has a low doped P^{--} layer on a P device layer. The resistivity of the P^{--} layer can be equal to or greater than 1-10 ohm-cm and in some cases equal to or greater than 20 ohm-cm, with a thickness of 0.5 to 5 micrometers and in some cases 1-3 micrometers and in some cases 0.5-2 micrometers. A buried P^{++} well 5704 with resistivity that can be equal to or less than 0.01-0.001 ohm-cm, can be ion implanted and/or diffused as in Swoboda, close to the BOX layer with a thickness ranging from 0.1 to 0.5 micrometers and/or entirely the P device layer. As in Swoboda, the buried P^{++} region 5704 can be formed by epitaxially growing the I or low doped layer subsequently. The buried P^{++} region can be selective area

and/or blanket area. A P^{++} connecting well 5706 with resistivity equal to or less than 0.01- 0.001 ohm-cm, can be implanted or diffused to intercept and/or in close proximity to the buried P^{++} well 5704 which in some cases may require multiple epitaxial growth as discussed in Swoboda, and form the outside circumference of the photosensitive area. A N^{++} well 5784 can be ion implanted or diffused on the top surface, with resistivity less than or equal to 0.01-0.005 ohm-cm and a thickness ranging from 0.05 to 0.5 micrometers. In some cases a thin semitransparent metal layer (not shown) such as Pt, Au, Cu, V, Ni, Ag, Al, and/or Cu, with thicknesses ranging from 1 nm to 50 nm and/or transparent conducting metal oxide with thickness in the range of 10 nm to 1000 nm, can be deposited on the N^{+} region prior to hole etch. The N^{++} doped region 5784 defines the photosensitive area of the MSPD and can be circular, square, polygonal and/or any combinations of shapes with lateral dimensions such as diameter and/or diagonal ranging from 20-1000 microns and in some cases from 20 to 100 microns and in some cases 30 to 100 microns.

[00361] Thermal annealing can be done together with CMOS/BiCMOS thermal anneal step to activate the P and N type ion implanted regions or in some cases it can be thermally annealed prior to CMOS/BiCMOS device processing. See, e.g., Huang et al, A 10-Gb/s OEIC with Meshed Spatially-Modulated PhotoDetectorin0.18- umCMOSTechnology, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 5, MAY 2011 (incorporated herein by reference and referred to herein as "Huang et al"), which shows a deep N well, which in some cases may require multiple epitaxial growth, connected to an N well (FIG. 6 of Huang et al). See also: Tavernier et al, High-Speed Optical Receivers With Integrated Photodiode in 130 nm CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 10, OCTOBER 2009 (incorporated herein by reference and referred to herein as "Tavernier 2009"), which shows a surface N well; Kao et al, A 5-Gbit/s CMOS Optical Receiver With Integrated Spatially Modulated Light Detector and Equalization, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS (incorporated herein by reference and referred to herein as "Kao et al"), which shows a spatially modulated photodetector with guard rings; Youn et al, which shows a P in an N well avalanche photodiode; Hartman et al, A Monolithic Silicon Photodetector/Amplifier IC for Fiber and

Integrated Optics Application, Journal of Lightwave TECHNOLOGY, VOL. LT-3, NO. 4, AUGUST 1985 (incorporated herein by reference), which shows a PIN photodiode integrated with IC electronics; and Radovanovic´ et al, A 3-Gb/s Optical Detector in Standard CMOS for 850-nm Optical Communication, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 8, AUGUST 2005 (incorporated herein by reference), which shows an interdigitated silicon photodiode. Swoboda shows a PIN silicon photodiode integrated with TIA and other ASIC electronics.

[00362] The Si photodiode structures in these references can be used with the addition of microstructure holes and/or other microstructures such as microstructure optical waveguide photodetectors as in FIG. 61, *infra*, to enhance the absorption and further improve its performances and perhaps use less complex electronics for signal processing. A higher signal to noise ratio can be desirable and the system can be more stable in adverse operating conditions such as high temperatures environments in data centers and high performance computing and LIDAR for example. In addition, low reverse bias voltages for MSPD in the range -1 to -4V and MSAPD in the range -6 to -25 V can be desirable for reliable system operation and/or compatible with CMOS/BiCMOS voltages. The dotted line 5702 represents the depletion when a reverse bias is applied to the anode and cathode (not shown).

[00363] FIG. 58 is cross section showing some aspects CMOS/BiCMOS integration with MSPDs/MSAPDs, according to some embodiments. The layer structures and implanted and/or diffused regions as shown in FIG. 57 are used. Shown is a monolithically integrated MSPD in a N-I-P configuration with CMOS/BiCMOS TIA and any other signal processing, enhancing, transmitting ASICs into a single chip. Note that although the layer structures and implanted and/or diffused regions shown in FIG. 57 are used, the ions activation by rapid thermal annealing can occur before, during or after the CMOS/BiCMOS processing is partially and/or fully completed. Microstructured holes 5812 can be etched into the top surface with depth ranging from 100 nm to 10000 nm and in some cases from 200 nm to 5000 nm and in some cases 500 nm to 2500 nm and in some cases 500 nm to 1100 nm. The holes can be partially into the N region 5784, and/or partially into the I or low doped high field I or P^{--} region and/or through the low doped region and and/or to the P^{+} doped region 5704 and/or to the Box layer.

The holes 5812 can be circular, square, polygonal, oval, amoeba, hourglass or other shape. The lateral dimension, diameter/diagonal/significant length of the holes can range from 200 nm to 5000 nm and in some cases from 450 nm to 2000 nm and in some cases 500 nm to 1650 nm. Spacing between holes can range from 50 nm to 3000 nm and in some cases from 100 nm to 2000 nm. The holes cross section can be of any shape, for example funnel, inverted pyramid, cylindrical, V shape, polygonal, ball like, hourglass, and/or any combination of shapes that can be dry and/or wet etched and/or electrochemically etched. The holes can be period, aperiodic and/or combination of periodic and aperiodic. In some cases prior to hole etch, a layer of transparent conducting metal oxide (not shown) can be deposited on the N surface to assist in the reduction of sheet resistivity. The N and P type can be reversed to form an P-I (P^{--} or N^{--} region) on N and for MSAPD a charge and multiplication region can be added). The cathode and anode can be formed on the surface and the device for MSPD is operated at a reverse bias voltage ranging from -1 to -5 volts and for MSAPD the reverse bias voltage can range from -6 to -30 volts. The cathode and anode are connected to the TIA and/or other ASICs and can include an inductor and/or other circuit elements in the transmission line and/or ASICs such as equalizers for peaking the frequency response of the photodiode integrated with TIA and other ASICs. Passivations, planarization, metal interconnects, transistors, capacitors, resistors, inductors, memory elements, to name a few are not shown.

[00364] An optical and/or electrical isolation or attenuation region 5860 can be included to avoid light interference with the IC electronics. This isolation region can be a trench, and/or an ion implanted region to create an amorphous semiconductor region where it has poor electrical conductivity and high optical absorption. It can also be implanted with O, N ions and/or metal ions.

[00365] Light can impinge from the surface where the holes are etched and/or from the bottom where a via (not shown) can be etched to the BOX layer.

[00366] By etching microstructured holes 5812, the absorption of light at wavelengths 800-1170 nm can be significantly enhanced for Si and/or GeSi where Ge fraction is less than 0.1 and in some cases less than 0.2 for example. For example, in Tavernier 2008, at 850 nm the responsivity observed was 5mA/W whereas with absorption enhancing microstructured holes and microstructured

optical waveguides, 350mA/W can be observed. At 1000 nm wavelength responsivity of 150mA/W have been observed on Si photodiodes with microstructure holes for absorption enhancements and can reach data rates in excess of 20 Gb/s. Data rates of 25 Gb/s and 50 Gb/s can be achieved with equalization, and other electronic signal conditioning methods for silicon photodiodes with microstructured holes at wavelength range from 800- 1000 nm and in some cases from 840 nm to 1100 nm.

[00367] With the addition of Ge to form GeSi alloy the wavelength can be further extended to 1350 nm and in some cases to 2000 nm depending on the Ge content and can also depend if the layers are relaxed or not relaxed.

[00368] In some cases the MSPD/MSAPD can be fabricated on a silicon wafer and where a BOX layer and/or SOI wafer may not be needed and in some cases a buried oxide layer can be implemented by ion implantation of O ions into the silicon substrate and can be a blanket implant and/or selective area implant followed by a second buried implant and/or diffusion of shallower depth of P or N type dopants that can be thermally anneal to activate the dopants and recrystallize the Si if necessary followed by epitaxial growth of the I or low doped layer. The purpose of the buried O implant is to reduce the photogenerated carrier lifetime that are generated outside the high electric field region and may diffuse slowly back to the high field region that may result in a slow component in the impulse response of the MSPD/MSAPD. The buried O ions can have a doping range of 1E18 to 1E21 and the P or N buried dope layer can have a resistivity in the range 0.01 to 0.001 ohm-cm or less and a thickness range of 100 nm to 500 nm. In addition a back side via is an option for backside optical signal illumination. This can also apply to any other figures herein where a BOX is included.

[00369] In known references on integration of silicon photodiode and TIA and other electronics, such as Huang et al, which presented a summary of silicon photodiode integrated with TIA and additional ASICs for signal enhancement and processing, the responsivity, photodetector bandwidth and bias voltage can be key parameters. In many cases the responsivity is either too low, thus requiring low noise amplifiers of several stages which can increase power consumption, or more sensitive to noise due to a low signal to noise ratio caused by, for example, hot environments or electromagnetic interference. Low photodetector bandwidth may

lead to the use of significant signal processing electronics to achieve good responsivity, which can further reduce the responsivity at high frequency and in many cases high bias voltages. See. e.g., Swoboda, where their P-I-N silicon photodiode had a 10 micrometers thick I layer to achieve a responsivity of 260 mA/W at 850 nm and a data rate bandwidth of 2.2 GHz, required a bias voltage of – 17V.

[00370] With the addition of microstructured holes on a silicon photodiode, as disclosed in herein, a thinner I layer can be used to achieve a high responsivity due to absorption enhancements, resulting in high data rate bandwidth, high responsivity and low bias voltage which are desirable for low power consumption electronics, high signal to noise ratio and high data rate bandwidth that can simplify electronics resulting in a more stable system in adverse environments.

[00371] FIGs. 59A and 59B are cross sections illustrating some aspects of a MSPD integrated with CMOS/BiCMOS ASICs that include a TIA on a CMOS/BiCMOS compatible silicon substrate, according to some embodiments. FIG. 59A shows a N type substrate, 0.5-5 micrometer thick N^{--} layer with resistivity equal to or greater than 1 ohm-cm and in some cases greater than or equal to 10 ohm-cm, is epitaxially grown on buried N^{+} implanted and/or diffused region 5904 and oxygen ion implanted region 5934 below the N^{+} region 5904 in the N substrate. In some cases if the N substrate resistivity is 0.01 ohm-cm or less, the N^{+} buried implant may not be necessary. Further CMOS/BiCMOS layer(s) may be formed. As discussed in Swoboda, there may be no further CMOS/BiCMOS layers (see, e.g., FIG. 13.5.1 of Swoboda). It may also be the case for some other MSPDs/MSAPDs integrated with CMOS/BiCMOS ICs that no further CMOS/BiCMOS epitaxial layers are necessary and the layer(s) maybe just be low doped N^{--} or P^{--}type layer(s) with resistivity greater than or equal to 1 ohm-cm and in some cases greater than or equal to 3 ohm-cm. In some cases, extra CMOS/BiCMOS layers will be provided such as where GeSi is used in the transistor process.

[00372] In FIG. 59A, a P-I-N MSPD is formed with buried N^{++} type well 5904 implanted/diffused and N^{++} type connecting well 5906 that can be implanted and/or diffused and a P^{++} type well 5984 that can be implanted or diffused. The N^{++} type wells can have resistivity equal to or less than 0.004 ohm-cm and the P^{++} type well

can have resistivity equal to or less than 0.004 ohm-cm. The depth of the deep N^{++} type well, which may require multiple epitaxial growths, can range from 0.5 to 5 micrometers and in some cases from 0.5 to 2 micrometers and in some cases 0.5 to 2.5 micrometers. The microstructured holes 5912, including their size, shape and spacings are as described elsewhere herein, and can be etched wet and/or dry into the P^{++} layer and/or partially into the N^{--} layer and/or partially into the N^{++} layer and/or through the N^{++} layer. In some cases a transparent conducting metal oxide such as indium tin oxide layer can be applied to the top surface prior to hole etching to assist in reducing the sheet resistivity.

[00373] In some cases, N^{+} buried layer 5904 may not be necessary if the N substrate resistivity is 0.01 ohm-cm or less.

[00374] The dotted line 5902 represents the depletion when a reverse bias is applied to the anode and cathode. Reverse bias voltages can range from -1 to -5V and in some cases -1 to -3.3 V.

[00375] In some cases, a deep buried ion implantation of oxygen ions and/or nitrogen ions can be used to create a buried oxide and/or oxygen rich layer and/or a nitride and/or a nitrogen rich layer 5934. This buried oxide and/or nitride layer 5934 can be to reduce photogenerated carriers outside the high field region which can create a slow diffusion current that can degrade the bandwidth of the MSPD/MSAPD. In addition such a buried oxide and/or nitride layer 5934 can also help reflect any stray signal photons back toward the microstructured holes for further absorption enhancements. In some cases ions such as O, N and/or metal ions such as Al, Cu, Be, and/or Mg create a disorder region such that optical absorption and recombination of minority carriers time is short to reduce diffusion current generated away from the high field depletion region. In some cases, the implants can be buried by multiple epitaxial growths where the ions are first implanted and followed by epitaxial growth to bury the implant. Doping density of the O, N and other ions can range from $1E18/cm^3$ to $1E22/cm^3$ for example. In some cases, the buried O, N and/or other ions for reducing minority carrier lifetimes may not be provided. Other methods may be the use of heavily doped N or P regions with resistivity less than 0.01-0.001 ohm-cm to reduce minority carrier lifetimes. In some cases, PN junctions, single and/or multiple such as PNPNPNPN

may be used to impede minority carriers from diffusing back to the high field region of the I layer/region.

[00376] The optical signal can impinge from the surface, surface illuminated, where the holes are etched and/or from the bottom through a via.

[00377] The optical signal wavelength can range from 810 nm to 1100 nm and in some cases 750 nm to 1100 nm and in some cases 840 nm to 1070 nm and where the responsivity can be 100mA/W or higher at at least one wavelength in the range, and in some cases 200 mA/W or higher at at least one wavelength in the range and in some cases 300 mA/W or higher at at least one wavelength in the range and in some cases 400 mA/W or higher at at least one wavelength in the range and in some cases 500 mA/W at at least one wavelength in the range. Data rate bandwidths can range from 1-50 Gb/s or higher and in some cases 15-25 Gb/s or higher and in some cases 25-50 Gb/s or higher and in some cases 1-25 Gb/s or higher. Diameter/Diagonal of the photosensitive area can range from 15-500 micrometers or more and in some cases 30-100 micrometers.

[00378] As discussed herein *supra*, the MSPD/MSAPD integrated with TIA and other signal processing/storage/transmitting ICs can be single and/or multiple, for example a quad for parallel fiber links where the aggregated signal is 4X that of a single MSPD/MSAPD and ICs, it can be 16X, 32X, or 64X.

[00379] The MSPD and TIA and other ASICs integration can also apply to MSAPDs and TIAs and other ASICs with the addition of a charge and multiplication layers such that instead of a P-I-N, it can be P-I-PN or P-I-P-I-N as described elsewhere in this disclosure. See e.g., Youn et al. According to some embodiments, Si avalanche photodiodes with microstructured holes can have higher data rate bandwidth, higher responsivity and lower reverse bias voltage than a comparable Si avalanche photodiode without microstructured holes for enhancement of the absorption of the optical signal photons.

[00380] FIG. 59B shows a simple cross section of a MSPD integrated with TIA and other ASICs similar to FIG. 59A with the addition of an isolation trench 5960 that can have a depth ranging from 0.1 to 10 micrometers and can have a width of 0.1 to 10 micrometers or more that can be around the MSPD and/or MSAPD completely or partially. In addition, it can be a single trench as shown and/or multiple trenches and in some cases the trench spacings and width can satisfy the

Bragg condition for a distributed Bragg reflector. The trench can be for electrical and/or optical isolation. In some cases, the trenches can be filled fully and/or partially with a dielectric and/or polymer and/or metallic material and/or metallic like material.

[00381] FIG. 60 is a cross section view of a silicon PIN photodiode integrated with TIA and other ASICs, according to some embodiments. Note that many of the cross sections shown in this disclosure have been simplified for purposes of clarity. Techniques according to embodiments of this disclosure are used to modify a structure disclosed in Swoboda. In FIG. 13.5.1 of Swoboda the distance between the top surface P^+ region and buried N^+ region is about 10 micrometers and a reverse bias voltage of -17 V is used to reach a bandwidth of 2.2 GHz. According to some embodiments of this disclosure, microstructured holes 6012 are etched wet and/or dry, as a back end of the line (BEOL) CMOS/BiCMOS process and/or as a part of the CMOS/BiCMOS trench processes. By etching the microstructured holes, the silicon photodiode is converted to a MSPD with absorption enhancement. The thickness between the P^+ and N^+ region can be reduced to 1-5 micrometers and in some cases from 0.5 to 3 micrometers and in some cases 0.5-2 micrometers. With N^- regions resistivity in the range 1-10 ohm-cm or greater, a reverse bias voltage of -2 to -4 V can deplete the N- region. In some cases a reverse bias voltage of -2 to -3.3 V can deplete the N- region of 0.5-2 micrometers approximately. In some cases a reverse bias voltage of -2 to -3.3 V can deplete the N- region of about 1 micrometer, in some cases about 2 micrometers, and in some cases 0.5-5 micrometers. The microstructured holes 6012 can be etched such as described herein *supra*. The holes 6012 can have cross sectional shapes such as funnel, inverted pyramid, cylindrical, trapezoidal, polygonal, hourglass, ball and/or any combination of shapes. The holes can have diameter/diagonal/ significant lateral dimensions ranging from 350 nm to 2000 nm, from 500 nm to 1700 nm and in some cases 250 nm to 3000 nm. The holes can have spacing from 50 nm to 3000 nm and in some cases 100 nm to 2000 nm. The etch depth can range from 100 nm to 2000 nm, from 200 nm to 2500 nm, from 250 nm to 6000 nm, and in some cases from 50 nm to 5000 nm. The holes can be partially in the P^+ region and/or first doped region, and/or partially into the N^- region and/or low doped region and/or intrinsic region, and/or partially into the N^+ region and/or the second doped

region and/or through the second doped region. With microstructured holes the responsivity can be 100mA/W or higher for at least one wavelength in the range 800 nm to 960 nm, and in some cases from 840 nm to 1100 nm. Responsivity can be 200mA/W or greater for at least one wavelength in the range 800 nm to 1100 nm, and in some cases responsivity can be 300mA/W or greater for at least one wavelength in the range 800 nm to 1100 nm. In some cases responsivity can be 400mA/W or higher for at least one wavelength in the range 800 -1100 nm. In some cases responsivity can be 500mA/W or higher for at least one wavelength in the range 800-1100 nm.

[00382] Data rate bandwidths can range from 1-5 Gb/s and in some cases 3-10 Gb/s and in some cases from 10-25 Gb/s and in some cases 25-50 Gb/s and in some cases 50-100 Gb/s or higher from the monolithically integrated MSPD and TIA and ASICs chip.

[00383] Diameter/diagonal of the MSPD photosensitive area and/or area defining the capacitance of the P-I-N or N-I-P structure, (lateral width of the N^+ region and/or first doped region, and/or width of the mesa) can range from 20 to 100 micrometers, in some cases 30 to 80 micrometers, in some cases 100 to 500 micrometers, and in some cases 10 microns to 1000 microns. Also shown in FIG. 60 are P^+ anode 6012, N^+ cathode 6022 and antireflection coating 6050. The dash lines in Fig. 60 represent multiple epitaxial layer growths as discussed in Swoboda.

[00384] Without microstructured holes, as discussed in Swoboda, silicon PIN photodiodes can achieve a responsivity of 260mA/W at 850 nm wavelength for the 10 micrometer thick I or N- region resulting in a 2.2GHz photodiode bandwidth at -17V bias. Complex signal processing electronics are required to achieve a 11 Gb/s data rate bandwidth resulting in a high power consumption of 310 mW. Such high reverse bias and power consumption are not desirable. In addition, such a structure will be difficult to push the “chip” (integrated PD and TIA and ASICs) bandwidth to 25 Gb/s. Whereas, using embodiments of this disclosure, with thinner I layer of 0.5-2 microns together with microstructure holes and/or microstructure optical waveguides as in FIG. 61, *infra*, for photon trapping and absorption enhancements, chip data rate output of 25, 50, 80 and 100 Gb/s can be achieved.

[00385] In some cases the resistivity of the P^+ and/or N^+ regions discussed earlier and thereafter, can be 0.1 ohm-cm or less, and in some cases 0.01 ohm-cm

or less and in some cases 0.001 ohm-cm or less. N- and P- regions, the low doped regions and/or intrinsic regions, can have resistivity or 0.2 ohm-cm or greater and in some cases 1 ohm-cm or greater and in some cases 10 ohm-cm or greater.

[00386] Csutak et al, High-Speed Monolithically Integrated Silicon Photoreceivers Fabricated in 130-nm CMOS Technology, JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 20, NO. 9, SEPTEMBER 2002 (incorporated herein by reference) shows a lateral P-I-N. According to some embodiments of the present disclosure, microstructured holes can be etched in an I region of a lateral P-I-N structure which will enhance the absorption of optical signal and improve the responsivity.

[00387] Note that in Swoboda, two epitaxial growths represented by the dotted lines are grown to bury the deep N^+ and P Isolation regions that can be formed by diffusion of dopants and/or ion implantation. The second epitaxial growth is used form the connecting N^+ wells of the P-I-N photodiode and the elements for a bipolar transistors for the TIA and equalizer ICs. In Swoboda, however, the thickness of the 10 micron I layer limits to chip data rate bandwidth to 11 Gb/s.

[00388] FIGS. 61A-61D is a top views illustrating aspects of microstructured optical waveguides, according to some embodiments. In FIG. 61A, a basic microstructured optical waveguides (MSOW) structure is shown. In a material 6000, a number of holes 6110 are formed. The holes 6110 are confined within a region 6102, marked with dashed line. At the core of the region 6102 there is a region 6112 marked with a dotted line that is free of holes 6110. The MSOW is formed by a high optical refractive index, hole-free core region 6112 surrounded by a region 6102 that a low optical refractive index due to the presence of holes 6110. The lateral dimensions of the core region 6112 ranges from sub optical wavelengths to tens of optical wavelengths. FIGs. 61B and 61C show further MSOW examples, in this case where the core(s) 6112 are closer to the size of the holes 6110. FIG. 61D is a wider view wherein the individual holes 6110 are not shown for clarity. In that example several MSOWs are shown in close proximity to one another on an isolated mesa 6150. Two of the MSOWs have a single central core such as shown in FIG. 61A. Other examples of MSOWs are shown that have larger cores, non-centered cores, and multiple cores in various arrangements.

[00389] The close proximity of the MSOWs allows cross coupling of the optical fields of adjacent microstructured optical waveguides thereby promoting a collective ensemble of coupled microstructure optical waveguides with optical waves propagating laterally. This results in absorption enhancements of the signal photons by the silicon photodiodes with microstructured optical waveguides or microstructured optical waveguide photodiodes (MSOWPDs) and equivalently a microstructured optical waveguide avalanche photodiode (MSOWAPDs). As used herein the terms "microstructure hole" and "microstructure photodetector" can also refer to MSPD, MSOWPD, MSAPD and MSOWAPD.

[00390] For silicon I and/or low doped layer, where I can represent undoped, intrinsic and low doped, the wavelength can range from 800-1100 nm, and in some cases from 840 to 960 nm and in some cases from 840 to 1070 nm. Microstructure holes 6110 can have shapes which are circular, oval, rectangular, polygon, hourglass and/or any other shapes and/or combination of shapes. The holes can have a lateral dimension, diameter, diagonal, ranging from 300 nm to 5000 nm. The core 6112 can be circular, rectangular, polygonal, oval and/or any other shapes and/or combination of shapes. The core can have a lateral dimension, diameter, diagonal ranging from 200 nm to 4500 nm and a single microstructure hole can have a single and/or multiple cores of same and/or different diameters for example.

[00391] For GeSi I or low doped layer, depending on the Ge fraction, the wavelength can range from 800 nm to 2000 nm. For Ge fraction less than or equal to 50%, the wavelength span can range from 800 nm to 1350 nm and for Ge fraction less than or equal to 80% the wavelength can range from 800 nm to 1550 nm and for 100 % Ge fraction the wavelength can be extended to 2000 nm. For high data rate applications of 10 Gb/s or greater and in some cases 25Gb/s or greater, the thickness of the I or low doped layer can range from 0.5 to 5 micrometers and in some cases 1 to 3 micrometers and in some cases 1 to 2 micrometers. The thinner I layer is not only for high data rate but also for low voltage reverse bias, since in most system, the voltage range from 1 to 5 V and in some cases 1 to 3.3 volts.

[00392] For lower data rate applications, I layer thickness of 3-5 micrometers may be used together with a larger photosensitive area, for example a diameter or

diagonal of 100 micrometer or larger. For high data rate applications, data rates of 10-50 Gb/s the diameter/diagonal of the photosensitive area can range from 20 to 80 micrometers. In some cases 25 to 50 micrometers.

[00393] Within a photosensitive area of an MSPD or MSAPD (such as a mesa 6150 shown in FIG. 61D), the microstructured optical waveguides can have different configurations, for example with single or multiple cores, cores diameter can be different, the confining microstructure hole can be different shape and/or dimensions, and the core and/or the MSOWs can can periodic and/or aperiodic and/or any combination of shape, dimensions, number of cores. These variation can result in a responsivity vs wavelengths that is smoother and has less undesirable resonances.

[00394] The photosensitive area can be defined by a mesa and/or a diffused P or N region and can be circular, oval, rectangular, triangular, hour glass, polygon and/or any other shapes and combination of shapes. In some cases, it can be a single photosensitive area and/or a multiple of photosensitive areas such as an array that can be a stand-alone array and/or the array can be integrated with CMOS/BiCMOS ASICs for signal processing, image processing, sensings, for applications such as optical data communications, LIDAR, LiFi, and free space optical communications.

[00395] The hole-free areas 6112, shown as a dotted circles, form an optical waveguide, and can also be a photonic crystal waveguide and/or in some cases where the holes are not regular, and/or periodic, and/or a certain size, can be a guided refractive index waveguide. In some cases the optical mode in the waveguide can interact with optical modes in the holes to generate photon trapping and/or slowing effects for example. Single and/or multiple such waveguides can be provided can also couple to each other and the holes dimensions and periods around each waveguide can be same and/or different from adjacent waveguides and can be periodic and/or aperiodic and/or combination of periodic and aperiodic.

[00396] FIG. 62A is a cross section view showing aspects of a microstructured optical waveguides photodiode (MSOWPD) integrated with CMOS/BiCMOS ASICs, according to some embodiments. The MSOWPD replaces the MSPD as in FIG. 58, 59 and 60. Microstructured optical waveguide avalanche photodiodes (MSOWAPDs) can similarly be fabricated and integrated with the addition of a

charge and multiplication (avalanche) layers/regions to create a P-P-PN or P-I-P-I-N structure. The cores (e.g. 6212, 6214 and 6216) of the MSOWPDs can be connected by first coating the surface with the MSOWPD with a polymer such as polyimide that can fill only the top gaps due to its viscosity and surface tension. After curing, a plasma ashing can be performed to remove the polymer from the surface but not in the gaps, exposing the top of the cores. This layer is not shown in FIG. 62A for simplicity. A transparent conducting metal oxide can be deposited on the top surface to connect the cores and the top surface electrically such that a reverse bias can be applied to the cores and the top surface anode and cathode. A reverse bias voltage can range from -1 to -5 volts.

[00397] As shown in FIG. 62A the structure except for the MSOWPD, is similar to FIG. 59A and 59B and in some cases a BOX can be included as in FIG. 58.

[00398] The microstructure optical waveguide (MSOW) can be etched partially into the I or low doped region and/or though the I or low doped region and in some cases to the N^{++} doped region and in some cases pass the N^{+} doped region. The lateral dimension of the MSOW which can consist of a microstructured hole and one or more microstructure cores, can range from 500nm to 8000 nm and the core lateral dimension can range from 300 nm to 7500 nm and spacing between the MSOW can range from 50 nm to 5000 nm.

[00399] The MSOW core shape can be circular, oval, hourglass, square, polygon for example. The core shape can also be circular, oval, square, or polygonal. The cores can be uniformly space and/or not uniformly spaces. The MSOW can be periodic and/or aperiodic.

[00400] The dimension of the MSOWs range from sub wavelength to 10 wavelength and can have photon trapping properties, slow wave effects, that can enhance the absorption of material with weak absorption for wavelengths at or just shorter than the bandgap wavelength of an indirect bandgap semiconducting material. Weak absorption can mean at certain wavelengths of light, the material bulk absorption coefficient is between 10s to 100s cm^{-1}. In certain cases, when the material is strained the bandgap can be smaller than the same material that is not strained. Use of microstructure holes and/or waveguides can enhance the absorption of both relaxed and non-relaxed semiconductors resulting in higher

responsivity over the same material without microstructure holes and/or waveguides for absorption enhancements.

[00401] Rectangular cross sectional holes are shown in FIG. 62 for the MSOW, the holes can be funnel shaped for example and the core can have a varying diameter such as a tapered core for example. Other shapes can include trapezoidal, and inverted bottle shaped.

[00402] FIGs. 62B and 62C are top views showing further aspects of microstructured optical waveguides photodiodes according to some embodiments. As can be seen, different topographies can be provided. In FIG. 62B, rectangular holes are on either side of the middle core 6212s. In FIG. 62C two cores 6214 and 6216 are surrounded by larger rectangular hole.

[00403] The MSOWPD/MSOWAPD can also be fabricated in a mesa structure as shown for example in FIG. 56 with or without a BOX. The optical signal can impinge from the top surface and in some cases can impinge from the bottom surface through a via.

[00404] Data rates of 3- 50 Gb/s or higher can be achieved and in some cases data rates from 3-10 Gb/s and in some cases from 20-30 Gb/s and in some cases from 25 – 50 Gb/s or higher. Signal wavelengths as in earlier discussions can span from 800-1100 nm and in some cases from 800 to 1350 nm depending on the Ge fraction in GeSi alloy and strain. And in some cases from 1250 nm to 1550 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy and strain.

[00405] In all the MSPD/MSAPD/MSOWPD/MSOWAPD integration with CMOS/BiCMOS TIA, equalizers, limiting amplifiers and/or other ASICs as necessary, a trench and/or multiple trenches as in FIG. 59B can be included.

[00406] See, e.g., Yin et al, Integrated ARROW waveguides with hollow cores, 14 June 2004 / Vol. 12, No. 12 / OPTICS EXPRESS 2710 (incorporated herein by reference); and Litchinitser et al, Antiresonant reflecting photonic crystal optical waveguides, OPTICS LETTERS / Vol. 27, No. 18 / September 15, 2002(incorporated herein by reference and referred to herein as “Litchinitser et al”); In FIG. 1C of Litchinitser et al, a MSOW is shown with one core in the middle. In contrast, according to embodiments of this disclosure, single and/or multiple cores of same or different dimensions can be provided. In addition, it should be noted

that the cores surfaces can be contiguous with the surface surrounding the holes as in FIG. 1C of Litchinitser et al. Where as in the embodiments shown in FIGs. 61A-61D, the cores can also be represented by hole-free areas or regions and in some cases the holes can be photonic crystal. According to embodiments of present disclosure, an MSOW can be a variation of ARROW waveguides with a solid core or cores and a propagation distance in the vertical direction along the waveguide of 0.5 to 10 micrometers.

[00407] Microstructured photodetectors (MS-PD) can be made polarization insensitive or polarization sensitive by the shape and arrangements of the microstructure holes. Microstructured holes that are asymmetric in direction tend to be polarization sensitive and microstructure holes that are symmetric in directions (X-Y) tend to be polarization insensitive.

[00408] FIGs. 63A-63C are cross section views illustrating aspects of MSPDs integrated with CMOS/BiCMOS circuitry utilizing selective area growth of Ge and/or GeSi on silicon, according to some embodiments. A silicon wafer is used with epitaxial layer(s) that are compatible with CMOS/BiCMOS fabrication that can also include a BOX (buried oxide) layer. In FIG. 63A, a void 6302 is etched into the N^{--} or P^{--} layer and where the top surface and sidewalls can be coated with a dielectric 6308 such as silicon oxide, silicon nitride. In FIG. 63B, selective area growth of Ge and/or GeSi alloy 6310 with Ge fraction ranging from 0 to 100%. The selective area growth of Ge and/or GeSi 6310 can be undoped and/or lightly doped with doping levels less than $5x10^{16}$ /cm^3 and in some cases less than $3x10^{15}$ /cm^3 and in some cases less than $3x10^{17}$ /cm^3. Thicknesses of the Ge and/or GeSi 6310 can range from 300 nm to 5000 nm and in some cases from 500 nm to 2500 nm. The shape of Ge and/or GeSi 6310, as viewed from the top, can be circular, rectangular, polygonal, diamond shaped, oval, and/or a combination of those and other shapes. Ge and/or GeSi 6310 can have a lateral dimension ranging from 10 micrometers to 500 micrometers or more and in some cases from 25 micrometers to 100 micrometers. The cross sectional shape can be a rectangle (as shown in FIG. 63B), and in some cases can follow the lattice plane of the Si in an anisotropic wet etch and in some cases can be polygonal and the shape in the two perpendicular lateral directions can be different. See, e.g., Michel et al, High-performance Ge-on-Si photodetectors, 30 JULY 2010 | DOI: 10.1038/NPHOTON.2010.157