

Electrical Properties of ITO/Crystalline-Silicon Contact at Different Deposition Temperatures

Giampiero de Cesare, *Member, IEEE*, Domenico Caputo, *Member, IEEE*, and Mario Tucci

Abstract—In this letter, the effect of deposition temperature on the barrier height between indium tin oxide (ITO) and crystalline silicon (c-Si) is presented. ITO films have been deposited by RF magnetron sputtering in the range between room temperature and 200 °C on both p- and n-type doped c-Si substrates. From current-voltage and capacitance-voltage characteristics of the ITO/c-Si junctions, we found that ITO deposited on 1-Ω · cm n-type doped silicon forms a rectifying junction with barrier heights varying from 0.9 to 0.3 eV, while at room temperature, an ohmic behavior on 1-Ω · cm p-type c-Si is obtained.

Index Terms—Indium tin oxide (ITO), ITO/crystalline-silicon (c-Si) junctions, semiconductor-metal interfaces, work function.

I. INTRODUCTION

VARIOUS kinds of transparent conducting oxide (TCO) thin films such as zinc oxide, impurity-doped indium oxides, and tin oxides have been widely used as transparent conductors in many thin-film devices. In particular, indium tin oxide (ITO) film exhibits excellent light transmission characteristics in the visible region of spectrum while maintaining high electrical conductivity [1].

Due to these unique properties, ITO has been used in a wide range of applications: as transparent electrodes in flat panel displays [2] and solar cells [3], [4], surface heaters for automobile windows, camera lenses and mirrors, and transparent heat-reflecting window material for buildings, lamps, and solar collectors [5]. Moreover, ITO films have also been widely utilized as the anode contact in organic light-emitting diodes (OLEDs) [6], [7].

Physical and electrical properties of ITO depend on its crystal structure, imperfections, oxidation level, and impurities. These factors are mainly controlled by the deposition techniques used to grow the ITO thin films, including chemical vapor deposition [8], magnetron sputtering [9], evaporation [10], and spray pyrolysis [11].

The energy barrier height formed at the interface between ITO and semiconductors plays a crucial role. Indeed, in OLEDs, the barrier height controls the efficiency of carrier injection into organic layers [12]. In amorphous-silicon/

crystalline-silicon (c-Si) heterojunction solar cells, due to the extremely thin emitter layer, the cell built-in potential (closely related to the cell open-circuit voltage) depends on the barrier height at the ITO/amorphous-silicon junction [13], [14].

In this letter, we study the effect of deposition temperature of ITO sputtered on c-Si to investigate the electrical properties of device contacts and to evaluate the barrier height to carrier collection.

II. EXPERIMENTAL RESULT AND DISCUSSION

Experiments have been performed by growing ITO films on 1-Ω · cm ⟨100⟩ p- and n-type doped polished c-Si wafers. This resistivity determines work functions of 5.17 and 4.1 eV for the p- and n-type doped wafers, respectively. Before ITO deposition, wafers were RCA cleaned, dipped in 1% HF solution, rinsed, and immediately positioned inside the RF magnetron sputtering system in order to avoid the formation of the native oxide and to reduce the density of surface states at the silicon/ITO interface. For each deposition run, both doped substrates have been positioned on the temperature-controlled chuck of the system. Eighty-nanometer-thick layers have been sputtered from a 6-in-diameter ITO target (with 90% In₂O₃–10% SnO₂ in weight composition), at 200 W of RF power, 2.7 mtorr of pressure process, and 25 sccm of argon flow. The substrate temperature has been varied from room temperature (25 °C) to 200 °C. Under these conditions, a deposition rate of about 4.5 Å/s has been achieved, independently of the deposition temperature. It is worth noticing that this temperature range is compatible with all the technological steps involved in the fabrication of devices utilizing ITO.

The electrical properties of the ITO/c-Si interface have been investigated by measuring the current flowing at different applied voltages between two coplanar ITO pads, sputtered on the c-Si surface through a physical mask. Results for the samples deposited at room temperature on p- and n-type doped c-Si substrates are shown in Fig. 1 as continuous line and open circles, respectively.

The nonlinear I – V curve measured on the ITO/n-type sample remarks the presence of two Schottky barriers, in back-to-back configuration, at the interfaces between n-type c-Si and ITO layers, while the linear behavior of the current-voltage (I – V) characteristics of the ITO/p-type c-Si sample indicates the formation of ohmic contacts. In particular, 71.43-mΩ · cm² specific contact resistivity has been evaluated by TLM measurement [15].

The achievement of an ohmic contact on a p-type c-Si substrate at room temperature is an interesting result since the

Manuscript received November 15, 2011; revised December 5, 2011; accepted December 9, 2011. Date of publication January 31, 2012; date of current version February 23, 2012. This work was supported in part by the European Community's Seventh Framework Program [FP7/2007-2013] under Grant agreement 232245. The review of this letter was arranged by Editor C. Bulucea.

G. de Cesare and D. Caputo are with the Department of Electronic Engineering, University of Rome "La Sapienza," 00184 Rome, Italy (e-mail: decesare@die.uniroma1.it; caputo@die.uniroma1.it).

M. Tucci is with the Casaccia Research Center, ENEA, 00123, Rome, Italy (e-mail: mario.tucci@enea.it).

Digital Object Identifier 10.1109/LED.2011.2180356

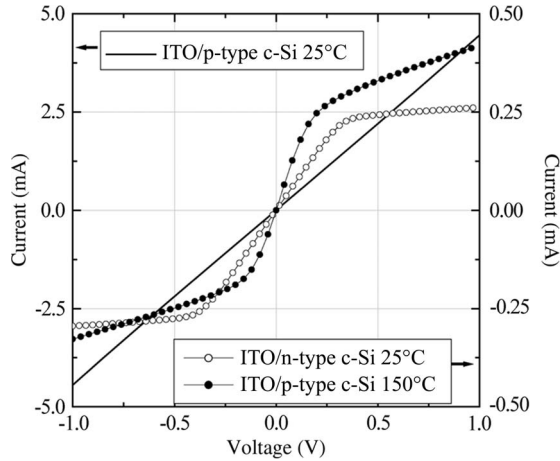


Fig. 1. Current-voltage characteristics of ITO/p-type c-Si at (continuous line) 25 °C and (solid circles) 150 °C and (open circles) ITO/n-type c-Si at 25 °C. The vertical left axis refers to the continuous line, and the right refers to the circles.

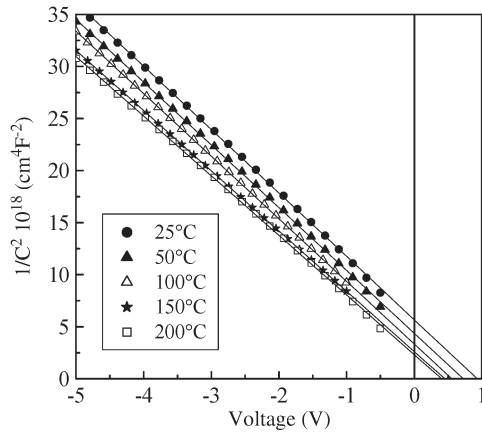


Fig. 2. $1/C^2$ -versus-voltage plot of ITO/n-type c-Si interface for different ITO temperature depositions. The continuous lines are linear extrapolation of data for the barrier height evaluation. The data are collected at 100 kHz using 50-mV signal probe.

different methods utilized up to now to accomplish this goal involve high-temperature steps [16], heterojunction formation [17], or laser-fired treatment [18].

To achieve quantitative information on the ITO/c-Si barrier heights, capacitance–voltage (C – V) measurements have been performed between an ITO pad grown on top of the n-type c-Si wafer and a eutectic InGa electrode deposited on the rear surface of the substrate after native oxide removal. The eutectic InGa has a work function equal to 4.1 eV and therefore ensures an ohmic contact with the n-type c-Si. The amplitude and frequency of the ac probe during the C – V measurement have been set to 50 mV and 100 kHz, respectively. At this frequency, the contribution to the capacitance due to defect density at the ITO/c-Si interface can be neglected. The $1/C^2$ -versus-voltage plot for the samples grown at the different temperatures, indicated by symbols, is shown in Fig. 2. Solid lines in the same figure represent the linear interpolations of the measured data, useful to infer the ITO/c-Si barrier heights from the intercept of the experimental data with the voltage axis. The extrapolated ITO/c-Si barrier heights versus ITO deposition temperature

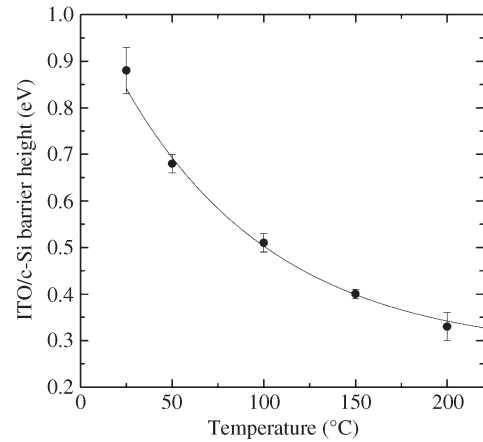


Fig. 3. Barrier heights as derived from $1/C^2$ plot of ITO/n-type c-Si structure. Line is a guide for the eye. The error bars refer to measurements made on 12 samples.

(T_{dep}) are shown in Fig. 3, where the error bars refer to the same measurements performed on 12 samples. From the figure, it is evident that, increasing T_{dep} from room temperature to 200 °C, the barrier height decreases monotonically from 0.9 to 0.3 eV. The achieved range of modulation is comparable with those obtained by other authors with more complex techniques, by using KrF excimer laser irradiation [19] or ultraviolet/ O_3 treatment [20].

The different values of ITO work function can be ascribed to different morphologies of the material deposited at different temperatures [21]. In this letter, we are focused only on the electronic properties of the junction. In particular, the barrier height decrement with increasing ITO deposition temperature determines a change in the electrical properties of the ITO/p-type c-Si interface and a change in the I – V characteristics of this interface due to Schottky barrier formation. Clear evidence can be inferred from Fig. 1, comparing the curves achieved by depositing ITO films at 150 °C (solid circles) and at room temperature (solid line).

Barrier height value at the ITO/c-Si interface is determined by the difference in the energy values of the Fermi level (E_F) in the two materials. Since E_F in c-Si is mainly fixed by the doping and the surface defect density is temperature independent in the investigated range of ITO film deposition, we ascribe the barrier height variation shown in Fig. 3 mainly to changes in the ITO film electrical characteristics.

To confirm this assumption, the surface resistivity (ρ_{sheet}) and the Hall mobility of an ITO sample sputtered on a glass substrate with the same deposition condition reported previously have been measured. Results shown in Fig. 4 demonstrate the modulation of the ITO electronic properties with deposition temperature. Increasing the deposition temperature, both the decrease of the film ρ_{sheet} and the increase of Hall mobility imply a higher position of the Fermi level within the conduction band and, then, a lowering of the barrier height.

The same samples have been used to measure the optical transmittance of the ITO films in the wavelength range of 350–1200 nm. We found transmittance values ranging from 75% to 85%, with 2% variation between different samples and a variation peak of 6% at around 390 nm.

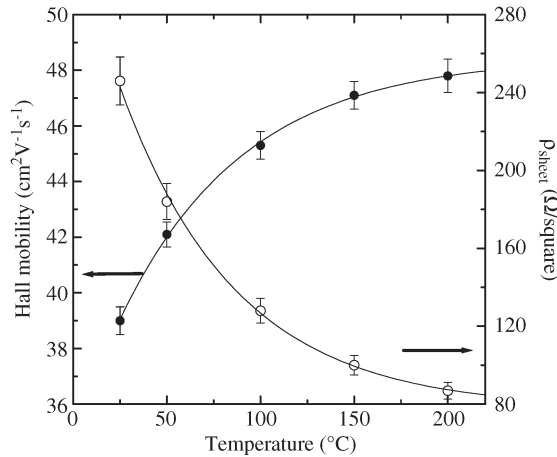


Fig. 4. Hall mobility and ρ_{sheet} values of ITO layers sputtered on glass at different temperatures. Lines are guides for the eye. The error bars refer to the measurement uncertainties.

III. CONCLUSION

In this letter, the modulation of the barrier height at the ITO/c-Si interface by varying the deposition temperature of ITO sputtered films has been demonstrated. The achieved variation of 0.6 eV comes from a temperature increase from 25 °C to 200 °C, temperatures that guarantee the suitability of this modulation in a wide range of applications where low-temperature technological process is required. The formation of ohmic contact on a p-type doped c-Si at room temperature has been also achieved.

REFERENCES

- [1] R. Groth, "Investigation of semiconducting indium oxide," *Phys. Stat. Sol.*, vol. 14, pp. 69–75, 1966.
- [2] M. Stewart, R. S. Howell, L. Pires, and M. K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 845–851, May 2001.
- [3] A. N. Tiwari, G. Khrypunov, F. Kurdzesau, D. L. Batzner, A. Romeo, and H. Zogg, "CdTe solar cell in a novel configuration," *Progr. Photovolt., Res. Appl.*, vol. 12, no. 1, pp. 33–38, Jan. 2004.
- [4] T. Mizrah and D. Adler, "Indium tin oxide silicon heterojunction photovoltaic devices," *IEEE Trans. Electron Devices*, vol. ED-24, no. 4, pp. 458–462, Apr. 1977.
- [5] Y. Leterrier, L. Medico, F. Demarco, J. A. E. Manson, U. Betz, M. F. Escola, M. Kharrazi Olsson, and F. Atamny, "Mechanical integrity of transparent conductive oxide films for flexible polymer-based displays," *Thin Solid Films*, vol. 460, no. 1/2, pp. 156–166, Jul. 2004.
- [6] L. Ke, R. S. Kumar, P. Chen, L. Shen, S. J. Chua, and A. P. Burden, "Au-ITO anode for efficient polymer light-emitting device operation," *IEEE Photon. Technol. Lett.*, vol. 17, no. 3, pp. 543–545, Mar. 2005.
- [7] L. Ke, P. Chen, R. S. Kumar, A. P. Burden, and S. J. Chua, "Indium-tin-oxide-free organic light-emitting device," *IEEE Trans. Electron Devices*, vol. 53, no. 6, pp. 1483–1486, Jun. 2006.
- [8] S. V. N. Pammi, H. J. Jung, and S. G. Yoon, "Low-temperature nanocluster deposition (NCD) for improvement of the structural, electrical, and optical properties of ITO thin films," *IEEE Trans. Nanotechnol.*, vol. 10, no. 5, pp. 1059–1065, Sep. 2011.
- [9] J. O. Park, J. H. Lee, J. J. Kim, S. H. Cho, and Y. K. Cho, "Crystallization of indium tin oxide thin films prepared by RF-magnetron sputtering without external heating," *Thin Solid Films*, vol. 474, no. 1/2, pp. 127–132, Mar. 2005.
- [10] Y. Meng, X. Yang, H. Chen, J. Shen, Y. Jiang, Z. Zhang, and Z. Hua, "A new transparent conductive thin film In₂O₃:Mo," *Thin Solid Films*, vol. 394, no. 1, pp. 218–222, Aug. 2001.
- [11] M. Ait Ouaja, R. Diaz, A. Belayachia, F. Rueda, and M. Abd-Lefdila, "Comparative study of ITO and FTO thin films grown by spray pyrolysis," *Mater. Res. Bull.*, vol. 44, no. 7, pp. 1458–1461, Jul. 2009.
- [12] C. H. Yen, Y. J. Liu, P. L. Lin, T. P. Chen, L. Y. Chen, T. H. Tsai, N. Y. Huang, C. Y. Lee, and W. C. Liu, "On an AlGaInP-based light-emitting diode with an ITO direct ohmic contact structure," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 359–361, Apr. 2009.
- [13] E. Centurioni, D. Iencinella, R. Rizzoli, and F. Zignani, "Silicon heterojunction solar cell: A new buffer layer concept with low-temperature epitaxial silicon," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1818–1824, Nov. 2004.
- [14] D. Caputo, G. de Cesare, and M. Tucci, "Built-in enhancement in a-Si:H solar cell by chromium silicide layer," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 689–691, Jul. 2010.
- [15] H. H. Berger, "Models for contacts to planar devices," *Solid State Electron.*, vol. 15, no. 2, pp. 145–158, 1972.
- [16] V. Vasu and A. Subrahmanyam, "Photovoltaic properties of indium tin oxide (ITO)/silicon junctions prepared by spray pyrolysis-dependence on oxidation time," *Semicond. Sci. Technol.*, vol. 7, no. 3, pp. 320–323, Mar. 1992.
- [17] M. Tucci, L. Serenelli, S. De Iulii, M. Izzi, G. de Cesare, and D. Caputo, "Back contact formation for p-type based a-Si:H/c-Si heterojunction solar cells," *Phys. Stat. Sol. (C)*, vol. 8, no. 3, pp. 932–935, Mar. 2011.
- [18] E. Schneiderlochner, A. Grohe, C. Ballif, S. W. Glunz, R. Preu, and G. Willeke, "Investigations on laser-fired contacts for passivated rear solar cells," in *Proc. 9th IEEE Photovoltaic Spec. Conf.*, 2002, pp. 300–303.
- [19] Y. J. Lin, C. W. Hsu, Y. M. Chen, and Y. C. Wang, "Increase mechanism of indium-tin-oxide work function by KrF excimer laser irradiation," *J. Electronic Materials*, vol. 34, no. 3, pp. L9–L11, Mar. 2005.
- [20] S. H. Kim, J. Jang, B. D. Chin, and J. Y. Lee, "Relationship between work function of indium tin oxide and device performances of C60 modified organic light-emitting diodes," *Current Appl. Phys.*, vol. 8, no. 3/4, pp. 475–478, May 2008.
- [21] Y. S. Jung, D. W. Lee, and D. Y. Jeon, "Influence of DC magnetron sputtering parameters on surface morphology of indium tin oxide thin films," *Appl. Surf. Sci.*, vol. 221, no. 1–4, pp. 136–142, Jan. 2004.