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Microelectronic Circuits

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Cover Photo: This 3D IC system demonstrates the concept of wireless power delivery and communication through multiple layers of CMOS chips. The communication circuits were demonstrated in an IBM 45 nm SOI CMOS process. This technology is designed to serve a multi-Gb/s interconnect between cores spread across several IC layers for high-performance processors.

(Photo Credit: The picture is courtesy of Professor David Wentzloff, Director of the Wireless Integrated Circuits Group at the University of Michigan, and was edited by Muhammad Faisal, Founder of Movellus Circuits Incorporated.)

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EXERCISES

3.7 Show that

$$V_0 = \frac{1}{2} \left(\frac{q}{\epsilon_s} \right) \left(\frac{N_A N_D}{N_A + N_D} \right) W^2$$

3.8 Show that for a pn junction in which the p side is much more heavily doped than the n side (i.e., $N_A \gg N_D$), referred to as a p^+n diode, Eqs. (3.26), (3.27), (3.28), (3.29), and (3.30) can be simplified as follows:

$$W \simeq \sqrt{\frac{2\epsilon_s}{qN_D} V_0} \quad (3.26')$$

$$x_n \simeq W \quad (3.27')$$

$$x_p \simeq W(N_A/N_D) \quad (3.28')$$

$$Q_J \simeq AqN_D W \quad (3.29')$$

$$Q_J \simeq A\sqrt{2\epsilon_s q N_D V_0} \quad (3.30')$$

3.9 If in the fabrication of the pn junction in Example 3.5, it is required to increase the minority-carrier concentration in the n region by a factor of 2, what must be done?

Ans. Lower N_D by a factor of 2.

3.5 The pn Junction with an Applied Voltage

Having studied the open-circuited pn junction in detail, we are now ready to apply a dc voltage between its two terminals to find its electrical conduction properties. If the voltage is applied so that the p side is made more positive than the n side, it is referred to as a forward-bias⁶ voltage. Conversely, if our applied dc voltage is such that it makes the n side more positive than the p side, it is said to be a reverse-bias voltage. As will be seen, the pn junction exhibits vastly different conduction properties in its forward and reverse directions.

Our plan is as follows. We begin by a simple qualitative description in Section 3.5.1 and then consider an analytical description of the i - v characteristic of the junction in Section 3.5.2.

3.5.1 Qualitative Description of Junction Operation

Figure 3.11 shows the pn junction under three different conditions: (a) the open-circuit or equilibrium condition studied in the previous section; (b) the reverse-bias condition, where a dc voltage V_R is applied; and (c) the forward-bias condition, where a dc voltage V_F is applied.

⁶For the time being, we take the term *bias* to refer simply to the application of a dc voltage. We will see in later chapters that it has a deeper meaning in the design of electronic circuits.

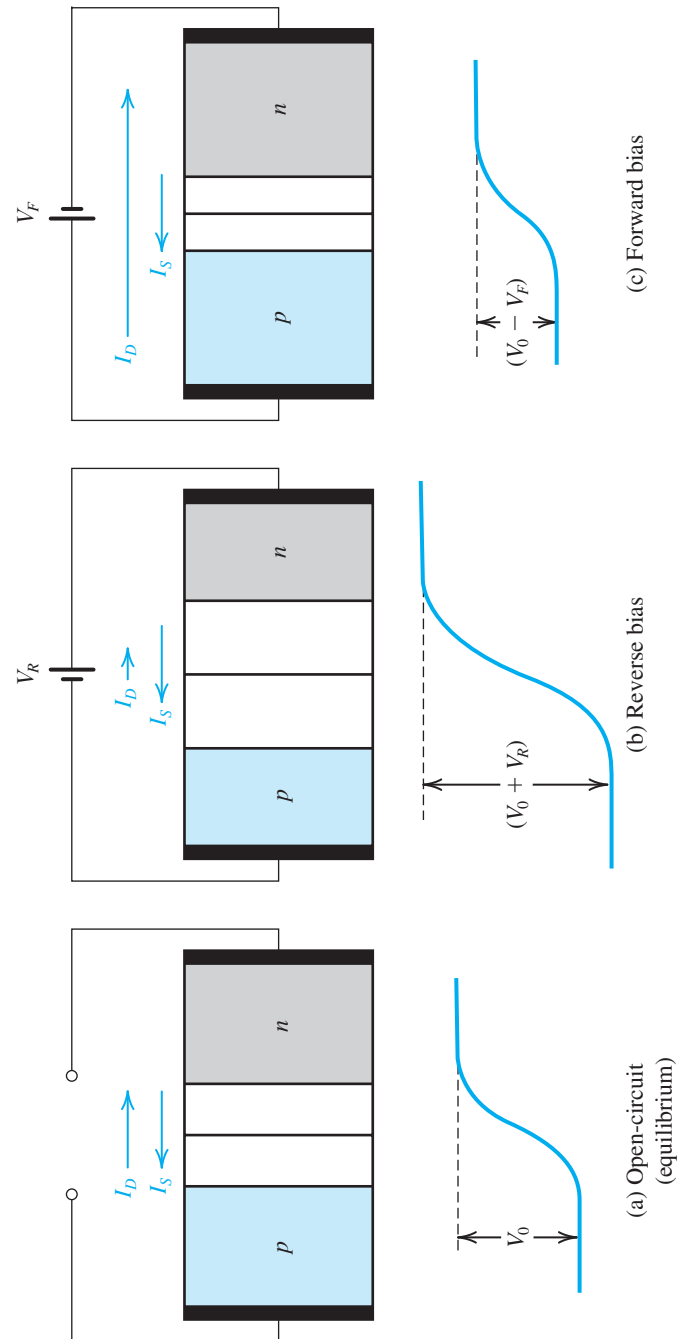


Figure 3.11 The pn junction in: (a) open-circuit; (b) reverse bias; (c) forward bias.