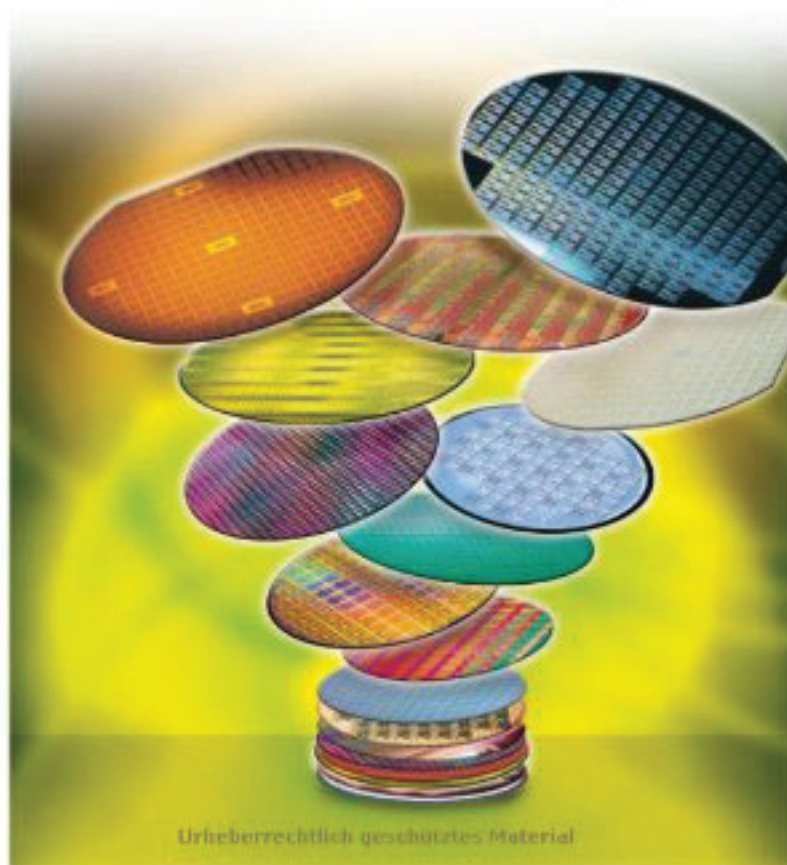


Urheberrechtlich geschütztes Material

Edited by Peter Ramm, James J.-Q. Lu,
Maaïke M. V. Taklo

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Handbook of Wafer Bonding



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Handbook of Wafer Bonding

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Library of Congress Card No.: applied for

British Library Cataloguing-in-Publication Data

A catalogue record for this book is available from the British Library.

Bibliographic information published by the Deutsche Nationalbibliothek

The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available on the Internet at <<http://dnb.d-nb.de>>.

© 2012 Wiley-VCH Verlag & Co. KGaA,
Boschstr. 12, 69469 Weinheim, Germany

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Cover Design Adam-Design, Weinheim

Typesetting Toppan Best-set Premedia Limited,
Hong Kong

Printing

Binding

Printed in

Printed on acid-free paper

Print ISBN: 978-3-527-32646-4

ePDF ISBN: 978-3-527-64424-7

oBook ISBN: 978-3-527-64422-3

ePub ISBN: 978-3-527-64423-0

Mobi ISBN: 978-3-527-64425-4

Other nonlithographic methods to pattern a polymer adhesive include spray coating of a liquid polymer with a shadow mask, local dispensing of a liquid polymer, or screen printing of a liquid polymer. The lamination of polymer sheets that are patterned by punching or cutting with a water jet or laser, is another suitable way to apply a polymer adhesive only on certain wafer areas. However, many of these methods have limitations concerning control of the polymer thickness and the smallest achievable feature sizes of the locally bonded and unbonded areas.

Localized polymer adhesive wafer bonding has also been combined with other localized bonding techniques such as direct metal or solder bonding in the same wafer bonding step [10]. In these techniques, the minimum required bonding temperature for one bond type (e.g., the direct bond) must not be higher than the maximum temperature stability of the second bond type (e.g., the polymer adhesive bond). These hybrid localized metal and polymer wafer bonding technologies are described in Chapter 11 of this book.

3.4

Wafer-to-Wafer Alignment in Polymer Adhesive Wafer Bonding

For many applications of polymer adhesive wafer bonding, accurate alignment between the bonded wafers is essential. For precise wafer-to-wafer alignment in wafer bonding, various techniques have been implemented, including wafer back-side alignment with a digitized image, the SmartView[®] method, intersubstrate microscopy, infrared transmission microscopy, transparent wafer with optical microscopy, and through-wafer holes with optical microscopy [2]. However, polymer adhesive wafer bonding is based on reflow or deformation and subsequent hardening of the intermediate polymer adhesive, and thus the polymer reflow process can cause problems for the achievable post-bond wafer-to-wafer alignment accuracy. When the wafer stack is pressed together with the bond chucks during the bonding process, shear forces acting in parallel to the bond line almost inevitably occur. If the polymer adhesive attains a low-viscosity phase during the bonding process, these shear forces can result in the wafers shifting relative to each other and thereby very significantly reducing the post-bond wafer-to-wafer alignment accuracy. One possibility to reduce this effect would be to use fixed and well-aligned bond chucks that do not introduce shear forces that cause the wafers to shift relative to each other during the bonding process. However, current state-of-the-art wafer bonding equipment typically does not provide these features. Nonetheless, there are a number of alternative approaches available to prevent large alignment shifts.

One approach that can prevent or reduce bonding-induced alignment shifts in polymer adhesive wafer bonding is the use of polymer adhesives that do not reflow and transform into a low-viscosity phase during the bonding process [6]. This can be achieved by using a thermosetting polymer that is partially crosslinked before bonding to an extent that it does not significantly reflow during bonding or by using a thermosetting polymer that is heated during bonding below the melting

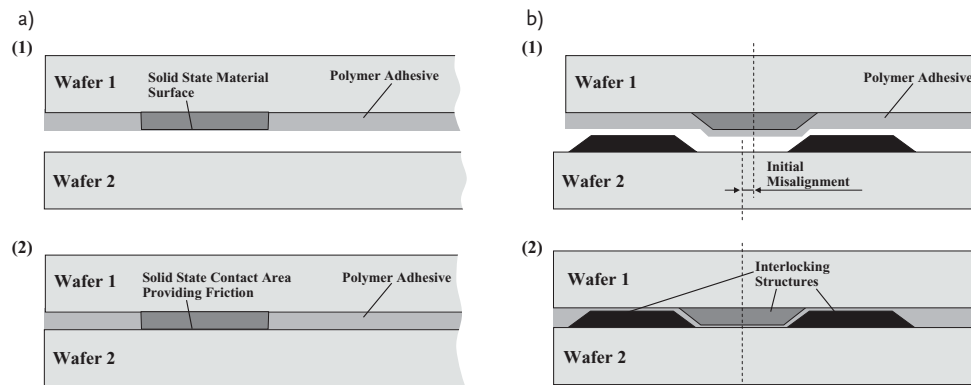


Figure 3.6 Techniques to improve obtainable wafer-to-wafer alignment in polymer adhesive wafer bonding (a) with frictional nonreflowable surface structures [45] and (b) with interlocking or keyed alignment structures [46]. (1) Before bonding; (2) after bonding.

point of the polymer. A disadvantage of this approach is that it is only practical for bonding wafers with low or no surface topographies where the polymer does not have to be redistributed significantly to prevent void formation. This approach is not suitable for bonding of wafers with high surface topographies.

A second approach that can prevent or reduce bonding-induced alignment shifts is to introduce surface structures on the wafers that are not covered with the polymer adhesive and that do not reflow during the bonding process as shown in Figure 3.6a. Such structures create frictional forces between the two wafer surfaces and can prevent the wafers from shifting relative to each other while the intermediate polymer is in a low-viscosity state in the bonding process [45]. These frictional structures may consist of metals, inorganic materials, or fully crosslinked thermosetting polymers that do not reflow during bonding.

A third approach, which is possible for submicrometer wafer-to-wafer alignment, is to introduce keyed alignment structures [46] that mechanically interlock the wafers and prevent them from shifting relative to each other or even provide a mechanical self-alignment function as shown in Figure 3.6b. Such corresponding interlocking structures may be etched into the wafer surfaces or deposited and patterned using dielectric materials, metals, or crosslinked thermosetting polymers. The placement accuracy of the corresponding interlocking structures on the wafer surfaces is only limited by the overlay accuracy of the photolithography and the etching processes used. Although added process steps are needed for keyed alignment during bonding, excellent post-bond wafer-to-wafer alignment accuracies of less than $1\text{ }\mu\text{m}$ have been reported [46].

When wafers are bonded that consist of dissimilar materials having different CTEs, additional problems for the obtainable post-bond wafer-to-wafer alignment accuracy can be expected. For a temperature increase of 100°C , the difference in thermal expansion between two wafers consisting of dissimilar materials can be several tens of micrometers. If the wafers are joined and bonded to each other

at an increased temperature, the difference between the thermal expansions of the two wafers from the temperature increase will result in a misalignment that is of the same order as the difference in thermal expansion of the two wafers. To accurately align and bond wafers that consist of dissimilar materials either their CTEs must match or the bonding must be performed near room temperature.

3.5

Examples for Polymer Adhesive Wafer Bonding Processes and Programs

In this section, process parameters and programs for wafer bonding with three different polymer adhesives are presented. The proposed program sequences and parameter sets represent possible processes that provide good bonding results. They are not optimized with respect to short bond cycle times. The programs should be viewed as examples that can serve as a starting point for the development of optimized, application-specific polymer adhesive wafer bonding programs. The program parameters may be adapted, the process sequence may be changed, and/or process steps may be added or removed. To counteract possible void formation at the bond interface, the indicated bonding pressure may generally be increased as long as the wafers do not break during bonding. When developing new or improved polymer adhesive wafer bonding process sequences and programs, it is useful to perform initial bonding experiments with glass wafers. This allows visual inspection of the bond interface through the glass wafers and observation of possible void formation.

3.5.1

Bonding with Thermosetting Polymers for Permanent Wafer Bonds (BCB) or for Temporary Wafer Bonds (mr-I 9000)

Dry-etch BCB is a thermosetting B-stage polymer that is compatible with semiconductor environments. BCB is a suitable polymer for permanent adhesive wafer bonds, which are very strong, resistant to various acids and solvents, and can withstand temperatures well above 200°C. BCB layer thicknesses from below 0.3 µm to above 10 µm have been successfully used in adhesive wafer bonding [6, 29]. The excellent reflow capabilities of BCB during bonding as indicated in Figure 3.2a makes wafer bonding with BCB layers comparatively tolerant to topographies and particles at the wafer surfaces. BCB is supplied by Dow Chemical Company in the USA. Table 3.4 gives and Figure 3.7 depicts an example of a preparation sequence and a wafer bonding program for wafer bonding with dry-etch BCB as intermediate polymer adhesive, respectively. Soft-baked or partially cured BCB coatings can be stored for several days or weeks in particle-free environments before the actual wafer bonding is performed without compromising the bonding results.

The nano-imprint resist series mr-I 9000 is a thermosetting B-stage polymer that is compatible with semiconductor environments. It is a suitable polymer for

4

Anodic Bonding

Adriana Cozma Lapadatu and Kari Schjølberg-Henriksen

4.1

Introduction

The anodic bonding technique, also known as “field-assisted sealing” or “electrostatic bonding,” was described for the first time by Wallis and Pomerantz in 1968 [1, 2]. The process has been demonstrated to be possible with a number of material combinations, but the pair that accounts for most applications is silicon and Pyrex glass. Joining silicon wafers with glass wafers by anodic bonding has proven to be a reliable method for packaging at the wafer level. Currently it is a well-established industrial technique that is reported to account for the majority of packaging applications for microelectromechanical systems (MEMS) [3].

Ceramics can also be used instead of glass [4]. Bonding of glass and ceramics can be done against metals [5], alloys, and other semiconductors, provided the thermal expansion coefficients of the two materials are closely matched. There are certain metals, such as aluminum and Kovar (a Fe–Ni–Co alloy), that because of the thermal mismatch cannot be sealed to glasses in their bulk form, but can be bonded as thin films or foils [2].

Anodic bonding is in essence a relatively simple process that provides high-quality hermetic seals. It involves bonding at elevated temperature, using the assistance of a strong electrostatic field. The bonding temperature is relatively low (300–450 °C for bonding silicon to borosilicate glass wafers), allowing the process to be performed at the end of the fabrication sequence. One of the main advantages of this process is that it can tolerate rougher surfaces than silicon direct bonding and does not impose the same very strict restrictions on the cleanliness of the bonding environment. On the other hand, it involves the use of alkali-containing glasses and it necessitates strong electric fields, which make it incompatible with some microelectronic devices. Another drawback is the thermal residual stress in the bonded structures, although the thermal expansion coefficients of silicon and glasses that are used for bonding are fairly close to each other.

Joining two silicon wafers by anodic bonding using a thin intermediate glass film, deposited by sputtering [6–9] or by vacuum evaporation [10, 11], has also attracted the attention of both academia and industry.

As dimensions of devices decrease, while their density and complexity increase, the requirements that must be fulfilled by anodic bonding equipment are more and more strict. Accurate alignment with tolerances in the micrometer range is required, often for multiple wafer stacks. A high bonding yield is required and this depends on the ability to ensure a uniform heating and voltage distribution over the wafers. The need to bond in controlled environments (gas composition and pressure) adds to the challenges. With the transition of microsystems technology from the development stage to industrial production, a high throughput becomes necessary for cost-efficient production.

4.2

Mechanism of Anodic Bonding

4.2.1

Glass Polarization

Anodic bonding is an electrochemical process that relies on the polarization of alkali-containing glasses. It can be achieved by setting the two wafers to be bonded together on a hotplate (300–450 °C), so that the glass becomes sufficiently conductive, and applying a high DC voltage to the pair (400–1000 V) such that the glass is negative with respect to the silicon. The bonding temperature is well below the glass transition temperature (~600 °C) and thus there is no macroscopic deformation of the glass during the bonding process.

The phenomenon of glass polarization has been extensively studied, both experimentally and theoretically, under steady-state or slowly varying conditions [12–14]. When a DC voltage is applied to such a glass at elevated temperatures, the alkali cations are depleted from the vicinity of the anode and transported towards the cathode, as illustrated in Figure 4.1. For most of the glasses used for anodic bonding the conduction is primarily realized by Na^+ ions and to a very small extent by K^+ ions. As the positive alkali ions are displaced towards the cathode, they leave

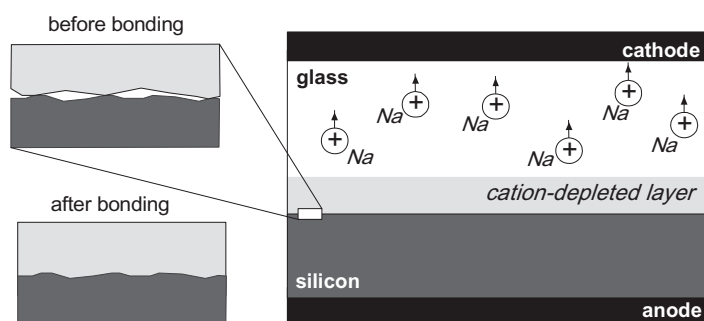


Figure 4.1 Mechanism of silicon–glass anodic bonding.

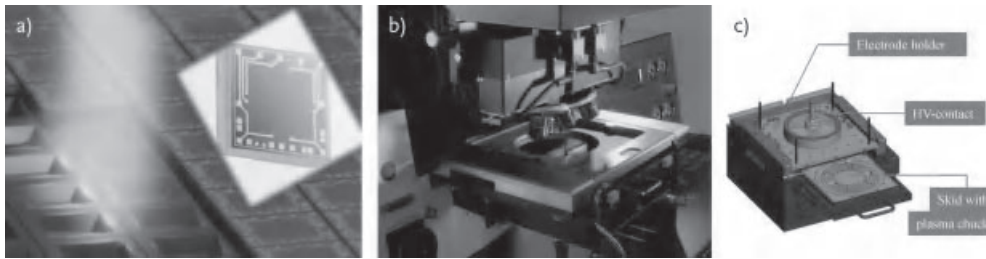


Figure 6.7 (a) Pressure sensor (in cooperation with EPCOS AG). (b) Mask aligner. (c) Tool for an atmospheric-pressure plasma activation system (upgradable in the SUSS Mask Aligner) [42].

6.5.1

Pressure Sensor

Figure 6.7a shows a pressure sensor (EPCOS AG) used as a demonstrator for atmospheric-pressure PAB. Here, a DBD activation of silicon wafers was applied at the Fraunhofer Institute for Surface Engineering and Thin Films. A grounded chuck acting as wafer carrier and an indium tin oxide (ITO)-coated high-voltage glass electrode are used for the activation equipment. In this case the ITO layer is the real electrode and the $750\mu\text{m}$ thick glass substrate is the dielectric barrier. The gas-flushed gap between the substrate surface and the counter electrode has an operating distance of $500\mu\text{m}$. The discharge is powered by a corona generator which operates at a frequency of 28.5 Hz. The transfer of this technique within a mask aligner is currently planned (Figures 6.7b and c).

Before low-temperature bonding of the pressure sensor at the Fraunhofer Research Institution for Electronic Nano Systems, the ideal plasma parameters have to be determined. Hence, the process gases nitrogen and synthetic air (80 vol.% N_2 + 20 vol.% O_2) and a process time of 40 s were chosen. Before and after the atmospheric-pressure plasma treatment a cleaning step using deionized water was applied [30]. To increase the bonding strength an annealing at 350°C for 6 h in nitrogen atmosphere was carried out. After dicing the sensors were characterized by burst tests. The bond strength of a synthetic air plasma-activated specimen was two times higher than that of nonactivated ones [42, 43].

6.5.2

Optical Microsystem

The development of a high-density optical microsystem applied to laser Doppler velocimeter sensors is presented by Higurashi and coworkers [39, 44]. Here, a two-step PAB technique is used as an alternative to eutectic AuSn or Au–Au thermocompression bonding.

Due to the high process temperatures (above 300°C) of AuSn and Au–Au thermocompression bonding, Higurashi and coworkers developed an Au–Au surface-

activated bonding technique. To clean the surfaces, low-pressure plasma activation with argon as process gas is applied. Subsequently Au–Au chip bonding takes place by contacting the substrates in ambient air for 30 s at temperatures below 250 °C [45]. Higurashi [44] asserted that an Au–Au bonded laser diode did not show any significant changes in electrical and optical performance compared with an unbonded one. After the first bonding step a further surface-activated bonding step is introduced to fabricate the microsystem (Figure 6.8). In this step, the optical bench including the bonded laser diode, micromirrors, and electrodes onto patterned silicon and a glass substrate including a photodiode, electrical interconnections, and microlenses are bonded at 150 °C.

6.5.3

Microfluidics Packaging

Howlader *et al.* developed a room temperature PAB technique using sequential plasma activation [25]. At first the wafers are exposed to an oxygen RIE treatment. After this process a microwave nitrogen radical treatment is applied. By using the sequential plasma activation as an *in situ* process, contamination is negligible. The implemented ion trap has two main functions. First, in the RIE mode the ion trap works as the counter electrode. Second, during the microwave treatment the trap operates as a filter to separate the uncharged radicals. The typical parameters for the oxygen RIE treatment are 13.56 MHz, 30 Pa chamber pressure, 200 W generator power, and 60 s process time. For the microwave plasma typical parameters are 2.45 GHz, 100 Pa chamber pressure, and 2000 W generator power. After the plasma activation the wafers were pre-bonded and kept in atmospheric air. Howlader *et al.* characterizes the bond strength by tensile testing. With this sequential plasma activation bond strengths similar to those of the bulk material (silicon or glass) could be achieved. To test the hermeticity a krypton-85 leak test was applied. The sealed cavities were placed in a high-pressure chamber with radioisotope krypton-85 gas mixture. To measure the radiation coming out of the specimen a scintillation counter was used. With this method the leak rate was determined to be lower than $1 \times 10^{-9} \text{ Pa m}^3 \text{ s}^{-1}$.

Howlader *et al.* used the technique described above to produce a glass–glass microfluidic device. Based on the high bonding strength, and the hermetic sealing behavior, this technique can be used for such microfluidic applications. Furthermore, the low bonding temperature guarantees the survival of living cells in the microchip.

6.5.4

Backside-Illuminated CMOS Image Sensor

Optical devices such as image sensors are another application for PAB. Dragoi *et al.* [46] bonded a fully processed CMOS wafer to a blank one using PAB. First, the CMOS wafer was polished to achieve a flat surface which corresponds to the requirements of direct bonding. After that, plasma-enhanced chemical vapor

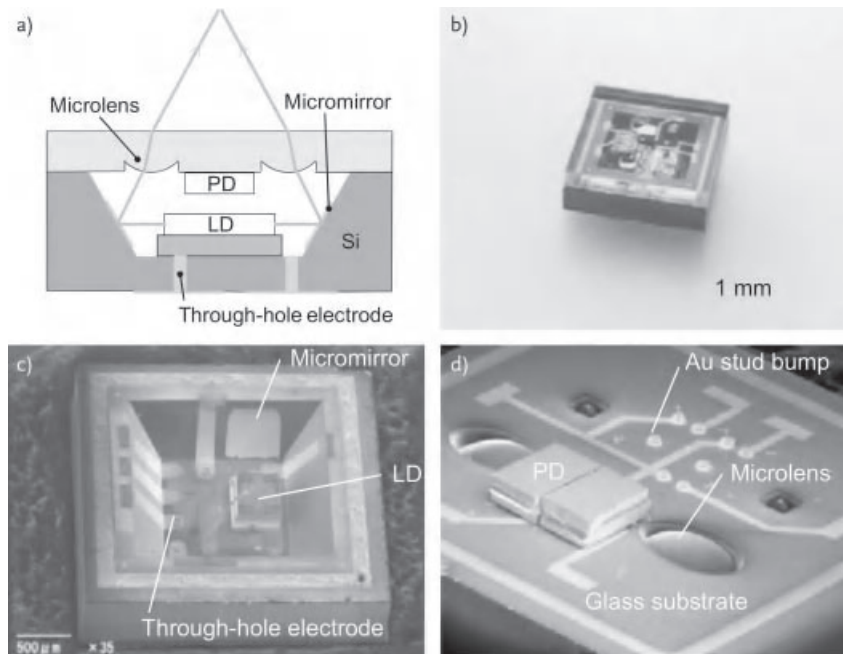


Figure 6.8 High-density optical microsystem: (a) cross-sectional assembly; (b) fabricated system; (c) integrated laser diode (LD) on optical bench; (d) integrated photodiode (PD) on Pyrex glass [44].

deposition was applied to form a silicon dioxide coating on both wafers. Subsequently an oxide layer densification was used to remove gas from the oxide layer. The oxide was then polished using standard chemical mechanical polishing (CMP). In the second step both wafers were plasma-activated and aligned by edge-to-edge alignment and optical alignment followed by spontaneous pre-bond at room temperature. After pre-bonding, the wafer stacks were annealed at 200–400 °C. The CMOS substrate was back-thinned by grinding and etching. The final technology step for processing the CMOS image sensor was adhesive wafer bonding of the optical elements like filters, lenses, and spacers.

6.5.5

CMOS Compatibility of Low-Pressure PAB

Sanz-Velasco *et al.* [47] determined the compatibility to the CMOS process with an oxygen plasma treatment prior to direct bonding. This is difficult because the impact of the plasma treatment on the electrical properties of the bonded interface and on the reliability of standard electronics is unclear. The plasma can have an influence on the components by contaminations or radiation damage. Here, contamination can be induced by the deposition of nonvolatile contaminants from the sputtering procedures or mobile ion contamination. The potential difference

between the plasma and the wafer and the plasma and the chamber walls justifies this sputtering procedure. For RIE, the wafer is exposed to a bombardment by energetic ions, electrons, and photons, for example UV radiation. The photons can cause radiation damage in the materials. Such damage can be in the form of electron traps in gate oxides which are the reason for shifts in the threshold voltages of MOS devices. Atoms in the surface can also be displaced and implanted. Furthermore, destruction of the gate oxide can occur.

In order to test CMOS compatibility, Sanz-Velasco *et al.* investigated the influence of plasma activation on application-specific integrated circuits. For this they manufactured test structures using the CMOS CYE 0.8 μm process from Austria Mikro Systeme International AG. According to the CYE process a top passivation layer, consisting of 1 μm silicon oxynitride and 1 μm silicon nitride, is superimposed on the electronics to protect them during the plasma treatment. Only the contact pads are treated. ICP-RIE was used with a gas pressure of 40 mtorr, a radio-frequency power of 15 W, and a coil power of 800 W to expose the components for 30 s to the oxygen plasma [47].

To characterize the various influences, Sanz-Velasco *et al.* measured the I - V characteristics of MOS transistors, the C - V characteristics of MOS gate capacitances, and the frequency of oscillators prior and after the plasma treatment. All measurements showed no significant change. Thus, the authors concluded that the oxygen plasma treatment in ICP-RIE can be used for CMOS applications.

6.6

Conclusion

PAB is a fully CMOS-compatible technology that provides unique possibilities for fabrication and improvement of three-dimensional integrated microsystems. Process flow, limitations, and parameters for PAB at low and atmospheric pressure with sufficient bond strength, packaging reliability, and defect-free bonding interfaces are readily available in the literature. The main advantages of PAB are the low bonding temperature, the compatibility with standard integrated wafer processing, and the wafer bonding of heterogeneous materials with a high CTE mismatch or temperature-sensitive materials. However, PAB requires special wafer surface preparation such as CMP to reduce surface roughness, wafer flatness, and minimal surface contamination. For defect-free PAB, cleanliness prior to bonding should be at a very high level. In conclusion, PAB is a well-known technology and one possibility for three-dimensional wafer stacking used in MEMS packaging.

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