UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR LLC,

Petitioner,

v.

W&WSENS DEVICES INC.,

Patent Owner.

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Case IPR2025-00995
U.S. Patent No. 10,468,543

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**DECLARATION OF DR. MICHAEL LEBBY, PH.D.,
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 10,468,543**

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A. Ground 1: Grounds 1A/1B: Claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 Are Anticipated by *Kuboi* (Ground 1A) and Obvious over *Kuboi* (Ground 1B) 47

1. Independent Claim 1 47

a. [1pre(a)]: "A single-chip device comprising an integrated combination of a microstructure-enhanced photodetector (MSPD) configured for reverse-bias operation and an active electronic circuit," 47

b. [1pre(b)]: "both formed on or in a single substrate" 56

c. [1pre(c)]: "and configured to receive an optical input that in cross-section is substantially continuous spatially, convert the optical input to an electrical output, and process the electrical output into a processed output, wherein:" 59

d. [1a]: "the MSPD on or in said single substrate comprises an intermediate region, a first region at one side of the intermediate region, and a second region at an opposite side of the intermediate region, wherein:" 66

e. [1b]: "each of the regions comprises Silicon, Germanium, or an alloy thereof;" 67

f. [1c]: "at least one of said regions, and an optional overlying covering region, have holes intentionally formed therein" 68

g. [1d]: "each of the first and second regions comprises a doped material;" 75

h. [1e]: "the intermediate region comprises a material that is less doped than at least one of the first and second regions or is undoped, wherein the degree

of doping is the same or different for different positions in the intermediate region;”.....76

i. [1f]: “an input portion configured to concurrently receive at a plurality of said holes said optical input that has said substantially continuous cross-section; and ” 83

j. [1g]: “an output portion configured to provide said electrical output from the MSPD;”.....85

k. [1h]: “the MSPD includes reverse-bias contacts coupled therewith to establish an electrical field therein when energized to thereby sweep in a selected direction electrical charges generated in the MSPD by said optical input;”.....87

l. [1i]: “the active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:” 91

m. [1j]: “amplification to form said processed output from the single-chip device;” 93

n. [1k]: “processing other than or in addition to amplification to form said processed output from the single-chip device; and” 96

o. [1l]: “routing to one or more selected destinations; and”.....97

p. [1m]: “a communication channel on or in said single-chip device, configured to deliver the electrical output from the MSPD to the active electronic circuit.”.....101

2. Claim 2.....103

a. [2]: “The single-chip device of claim 1, in which said active electronic circuit at least partly extends beyond said substrate.” 103

3. Claim 3 106

a. [3]: "The single-chip device of claim 1, in which said active electronic circuit is at least partly inside said substrate." 106

4. Claim 4 107

a. [4]: "The single-chip device of claim 1, in which said overlying region is present as a superstrate at one side of said first, intermediate, and second regions, and contains said holes." 107

5. Claim 7 109

a. [7]: "The single-chip device of claim 1, further including a region of a dielectric material that covers the holes and is in the propagation path of said optical input." 109

6. Claim 9 112

a. [9]: "The single-chip device of claim 1, in which said holes are present in said intermediate region." 112

7. Claim 10 114

a. [10]: "The single-chip device of claim 1, in which said holes are present in said intermediate region as well as in at least one of the first and second regions." 114

8. Claim 11 115

a. [11]: "The single-chip device of claim 1, in which said holes are present in each of the first, second, and intermediate region." 115

9. Claim 12 115

a. [12]: "The single-chip device of claim 1, in which each of said first and second regions and said intermediate region has a thickness and at least

some of said holes extend through the entire thickness of said intermediate region and of one of said first region and second region and through at least a part of the thickness of the other one of said first and second regions." 115

10. Claim 16 119

a. [16]: "The single-chip device of claim 1, in which at least some of said holes have sidewalls that slope in planes transverse to said regions." 119

11. Claim 17 123

a. [17]: "The single-chip device of claim 1, in which at least some of said holes have sidewalls with plural different slopes along the inside walls of the holes." 123

12. Claim 20 124

a. [20]: "The single-chip device of claim 1, in which the holes are at least partly filled with a dielectric material." 124

13. Claim 21 126

a. [21]: "The single-chip device of claim 1, in which the holes are entirely filled with a dielectric material." 126

14. Claim 24 129

a. [24]: "The single-chip device of claim 1, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD." 129

15. Claim 25 131

a. [25]: "The single-chip device of claim 1, in which the MSPD further includes ohmic contacts to said first and second regions, at least one of said ohmic contact[s] being through a via in said substrate." 131

16. Claim 26 137

a. [26a]: "The single-chip device of claim 1, further comprising a light guide to said MSPD for directing said optical input thereto," 137

b. [26b]: "and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip device." 140

17. Claim 28 142

a. [28a]: "The single-chip device of claim 1, further comprising one or more additional MSPD on or in the same substrate," 142

b. [28b]: "and respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input." 145

18. Claim 29 147

a. [29]: "The single-chip device of claim 1, further comprising one or more additional MSPDs on or in said single substrate, one or more additional active electronic circuits on or in the said single substrate, and one or more additional communication channels configured to supply electrical outputs from the MSPDs to the one or more of the active electronic circuits." 147

19. Claim 30 150

a. [30]: "The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate." 150

20. Claim 32 151

a. [32]: "The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate and comprise one or more of CMOS, BiCMOS, and bipolar active devices." 151

21. Claim 35 152

a. [35]: "The single-chip device of claim 1, further including a region of selected material that is over a side of one of the first and second regions facing away from the intermediate region and is configured to reduce sheet resistance." 152

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I. INTRODUCTION

1. I, Michael Lebby, Ph.D., have been retained as an independent expert by Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC (collectively, "Samsung" or "Petitioner") in connection with an *inter partes* review (IPR) of U.S. Patent No. 10,468,543 ("the '543 Patent") (Ex. 1042). I have prepared this declaration in connection with Samsung's Petition for *Inter Partes* Review.

2. Specifically, this document contains my opinions about the technology in claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 of the '543 Patent and the grounds against these claims that have been asserted by Samsung. I was not asked to provide any opinions about the '543 Patent that are not expressed herein.

II. SUMMARY OF OPINIONS

3. This declaration considers claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 of the '543 Patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

4. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of May 22, 2013), it is

my opinion that claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 of the '543 Patent would have been anticipated and/or obvious based on the asserted grounds discussed below.

5. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A to this declaration.

7. Based on my education, research, and work experience, I am knowledgeable about the subject matter of the '543 Patent and the related prior art.

8. In what follows, I provide a short summary of my qualifications.

9. I am an engineer with a Ph.D. in Electrical and Electronic Engineering and have worked extensively with optoelectronics, photonics, electrical and electronic circuits, optical systems, as well as integrated circuit semiconductors for both optoelectronic and electronic solutions. Overall, I have approximately 40 years of experience working in industry to develop new electronic, photonic, display, and optics-based products, which I have taken from research to manufacturing.

10. I received a Bachelor of Engineering degree in Electrical and Electronic Engineering in 1984 from the University of Bradford, United Kingdom. I also received a Ph.D. in Electrical and Electronic Engineering in 1987 from the University of Bradford, United Kingdom. I also received a second doctorate degree: a Doctor of Engineering degree (D.Eng) in electrical and electronic engineering in 2004 from the University of Bradford, United Kingdom.

11. I am currently Chief Executive Officer (CEO) and Chief Technology Officer (CTO) of GenusTechnik Inc., which is my consulting company, through which I engage in my expert witness work.

12. I recently retired in late 2024 as Chairman and CEO of Lightwave Logic Inc. (NASDAQ: LWLG), where I served as a Director of the Board of Directors since 2015.

13. I am a named inventor on over 225 U.S. utility patents. My work has also led to me either being an inventor or co-inventor in subjects such as: semiconductors, electronics, optics, displays, high frequency optical and electronic products such as lasers and LEDs, as well as photonic integrated circuits. I am the author of more than 60 publications.

14. I am a Fellow grade of three professional organizations: IEEE (Institute of Electrical and Electronic Engineers), NAI (National Academy of Inventors), and Optica (Optical Society of America).

15. As described in this Section, and further detailed in my *curriculum vitae* (Appendix A) over the course of my 40-year career in electronics and optoelectronics, I have worked in nearly every aspect of the electronic, semiconductor, and optoelectronics business, ranging from wafers to components, to modules, displays, optics, connectors and cable technology. At the wafer level, I have experience in epitaxial wafer growth (compound semiconductors). I also have experience in electrical and optoelectronic device and circuit design, using modeling and simulation, electrical and optoelectronic device and component fabrication, testing, and qualification, implementation of devices such as laser diodes, light emitting diodes, photodetectors etc., into packages, connectors, and panels, both hermetic and non-hermetic, as well as analysis of package/panel materials such as plastics (including plastic housings such as resin-packaged lead frame housings), optical plastics, metallic-based packages, semiconductor-based packages, and ceramic-based packages for fiber optics, displays, and data-communications industries. I have also designed device packages (through-pin, surface mount, flip-chip, and various combinations thereof) for printed circuit board mounting as well as electrical and optical components for various industrial

and environmental applications. Many of the designed components were implemented into technology applications both as manufactured products as well as components for testing, characterization and analysis of qualified products for volume scaling. The components were designed to work at both at optical and RF frequencies that include both optical and RF wireless as well as fiber-optics based applications. I have also worked in commercially based industrial research-and-development laboratories to bring new high-performance optoelectronic- and photonic-based technologies from the research proof-of-concept phase through prototyping up to and including qualified manufacturing for volume release. This has included both transfer of as well as the design of optics and optical systems for various commercial systems.

16. I have been both an entrepreneur (*e.g.*, Ignis Optics Inc, One Chip Photonics, Lightwave Logic Inc.), as well as an intrapreneur (*e.g.*, Motorola, Intel, TE Connectivity (previously Tyco Electronics), AT&T Bell Labs), creating innovative new high technology programs, both as venture backed start-ups as well as corporate funded divisions. I have built these entities to develop optical, electronic, optoelectronics, and photonics technology from the laboratory and fabrication clean room to production factories.

17. My career started in the late 1970s at the Ministry of Defense in the United Kingdom where I spent time at a number of their R&D facilities including

Malvern (RSRE – Royal Signals and Radar Establishment). There, I worked on electronic and optoelectronic semiconductor device design, as well as basic and high frequency telecommunications and data-communications electronics for module, cable, connector, and circuit implementation. My research work in electronics then took me to AT&T Bell Laboratories in 1985, where I pursued research in novel electronic and optoelectronic semiconductor material systems that included laser diodes, LEDs, photodetectors, optical waveguides, optics, and standard electronic devices as well as the processing and fabrication for such devices. The devices researched at Bell Labs became in part the subject of my Ph.D. thesis for which I was granted a doctoral degree in 1987.

18. I moved to Motorola in 1989 to further develop my skills in consumer commercial application of technology and focused on optoelectronics, and semiconductor engineering and development. I became a Research and Development Manager in Motorola, until I left the company in 1998. During my time at Motorola, I worked on many photonic, electronic, and optical technology projects that included projection, display, optics, LEDs, OLEDs, laser diodes, phosphors, cameras, as well as the packaging and reliability of mobile product prototypes. At that time, I was particularly interested in miniaturization of electronics, optics, and optoelectronics, and worked on novel optical designs that included portable heads-up displays, optical heads for storage, and various light-

based prototypes as well as advanced prototypes of futuristic communications and consumer hardware and cameras.

19. The research work at Motorola also included work on displays and in particular, miniature displays, arrays, imagers, projection systems, and optics for pagers, clam-shell phones, and head-mounted displays that included mounting onto eyeglasses (similar in concept to Google glass™) as well as techniques for electrical and optical connections in these applications.

20. I also initiated Motorola's work in optical interconnect (Optobus™) technology, that incorporated both transfer and injection molded optical parts and included the design of electrical and optical connector technology. This project involved the research and development of a multi-channel electronic IC chip for parallel optical interconnects as well as optical simulations of performance.

21. I was one of Motorola's most prolific inventors, having over 150 issued utility patents as an inventor or a co-inventor by the late 1990s. Many of the photonics and optical prototypes with which I was involved were subject to reliability and stress testing as well as optical measurement analysis. These consumer products all were driven using standard electronic ICs and electronic signaling where I had a role in design and simulation of these circuits.

22. Between 1998 and 1999, I worked as the Director of Technology/ BD (Fiber Optics) for Tyco Electronics (previously AMP). I joined Tyco Electronics as a business development director and director of advanced technology for the telecommunications and data-communications industries. I was responsible for growing the optical and optoelectronic technology business through external interactions that included mergers, acquisitions, strategic alliances, and technical strategic planning as well as leading new technology projects.

23. In 1999, I left Tyco and started employment at Intel. At Intel, I was involved heavily in photonic technology, especially technology that supported silicon photonic device platforms with different types of displays and optical systems. As a culmination of this work, I was one of Intel's founders of its silicon photonics division in the year 2000, and worked to set up a fabrication facility in South San Jose, California, USA. The work involved integrating silicon FET electronics with optoelectronics and optics onto the same silicon semiconductor wafer. This included CMOS detectors and arrays. I was also part of Intel Capital's optical investment team, and participated in over 30 photonics investment projects into photonics, optics, and optoelectronics. My focus included optical devices, packaging and modules for optical storage, consumer applications such as displays, cameras, projection, communications, and sensing. The technologies that I

investigated included lasers, LEDs, optics, LCDs, optical waveguides, cameras, imagers, and optical displays.

24. At the end of 2000, I left Intel and raised venture capital funding for a company called Ignis Optics Inc. The main goal of the company was to design and manufacture, in high volume, very high-performance optoelectronic modules. These fiber optic transceiver modules have the capability of transmitting and receiving optical signals that are controlled using programmable electronics and packaged optoelectronics chips, such as laser diodes, optical lenses, and photodetectors.

25. In 2005, I took up employment for a trade association, based in Washington, D.C., called IEEE Optoelectronics Industry Development Association (OIDA). As head of this trade association, and with electronics, photonics and optics manufacturers that included manufacturers of projection displays, optical systems, fiber optics, display, cameras, sensing, defense, aerospace, LED lighting, and automotive vendors as members, I was responsible, in part, for industry-based technology roadmaps; and I implemented common industry roadmap methodologies with common features such as “Red Brick Walls” and transferred them into technology roadmaps for the industry in which displays, optics, optical sensors, telecommunications cables, fiber-optic cables, fiber, cameras, and their

associated technology platforms, were featured. OIDA roadmaps featured purple brick walls, to show differentiation from the semiconductor industry.

26. In 2010, I became the General Manager and CTO of Translucent, Inc., a high-tech start-up company which developed and manufactured silicon and rare earth oxide based epitaxial semiconductor wafers. I patented a number of optoelectronic and electronic device designs using rare earth oxides and phosphors while employed at Translucent.

27. Throughout my career, I have also had an active role in a number of technical professional organizations, including, among others, IEEE Components, Packaging, and Manufacturing Technology (CPMT), IEEE Electronic Components and Technology Conferences (ECTC); IEEE TC-10 (Technical Committee on Optoelectronics), and IEEE Optoelectronics Industry Development Association (OIDA). Through these organizations, I have consistently been a part of committees, events, and workshops relating to semiconductor, optoelectronics, electronics, and packaging technology.

28. I also serve as a Technical Expert/Consultant for the European Commission. In my work at the European Commission, I review and advise on general optics, photonics, electronics, telecommunications, semiconductors, optoelectronics, imaging, sensing, cameras, display (*e.g.*, LCD, LED, OLED, etc.), and related Information and Communications Technology (ICT).

29. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which is attached to this declaration as Appendix A.

IV. MATERIALS CONSIDERED

30. In forming my opinions, I have analyzed the materials listed in the Table below. My opinions are based on my experience, knowledge of the relevant art, the documents identified in the Table below, as well as the documents directly cited to in this declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 10,446,700 to Wang et al. ("'700 Patent")
Ex. 1003	Prosecution History of the '700 Patent (downloaded from Public PAIR)
Ex. 1004	U.S. Patent Application Publication No. 2012/0049044 A1 to Kuboi ("*Kuboi*")
Ex. 1005	U.S. Patent Application Publication No. 2012/0033119 A1 to Shinohara ("*Shinohara*")
Ex. 1006	European Patent Application EP 2 172 974 A1 to NXP B.V. ("*NXP*")
Ex. 1007	U.S. Patent Application Publication No. 2008/0259981 A1 to Wang et al. ("*Wang*")
Ex. 1008	U.S. Patent Application Publication No. 2009/0133741 A1 to Higuchi et al. ("*Higuchi*")
Ex. 1009	Tapan K. Gupta, *Copper Interconnect Technology*, (Springer Science+Business Media, LLC 2009), pp. 67-71.
Ex. 1010	Zhihong Huang et al., *Microstructured silicon photodetector*, Applied Physics Letters, Vol. 89 (2006), pp. 033506-1 to -3.

Exhibit	Description
Ex. 1011	Richard A. Myers et al., *Enhancing near-infrared avalanche photodiode performance by femtosecond laser microstructuring*, Applied Optics, Vol. 45, No. 35 (Dec. 2006), pp. 8825-31.
Ex. 1012	Abbas El Gamal et al., *CMOS Image Sensors*, IEEE Circuits & Devices Magazine (2005), pp. 6-20.
Ex. 1013	Eric R. Fossum, *CMOS Image Sensors: Electronic Camera-On-A-Chip*, IEEE Transactions on Electron Devices, Vol. 44, No. 10 (Oct. 1997), pp. 1689-98.
Ex. 1014	Sunetra Mendis et al., *CMOS Active Pixel Image Sensor*, IEEE Transactions on Electron Devices, Vol. 41, No. 3 (Mar. 1994), pp. 452-53.
Ex. 1015	Renato Turchetta et al., *Introduction to CMOS Image Sensors*, Molecular Expressions™ Optical Microscopy Primer: Digital Imaging in Optical Microscopy - Introduction to CMOS Image Sensors (July 16, 2004), pp. 1-9, *available at* https://web.archive.org/web/20120508153832/https://micro.magnet.fsu.edu/primer/digitalimaging/cmosimagesensors.html
Ex. 1016	Ming-Dou Ker et al., *Investigation on Device Characteristics of MOSFET Transistor Placed Under Bond Pad for High-Pin-Count SOC Applications*, IEEE Transactions on Components and Packaging Technologies, Vol. 27, No. 3 (Sept. 2004), pp. 452-60.
Ex. 1017	Paul Horowitz et al., *The Art of Electronics* (Cambridge University Press, New York 3d ed. 2016), pp. 1, 11, 52, 71.
Ex. 1018	*Electrical Engineering Dictionary* - CRC*netBase* (Phillip A. Laplante editor-in-chief, CRC Press LLC 2000), pp. 1-6.
Ex. 1019	S.M. Sze et al., *Semiconductor Devices Physics and Technology*, (John Wiley & Sons, Inc. 3d ed. 2012), pp. 205-10, 325-26, 392-400, 416-417, 466-67.
Ex. 1020	John P. Uyemura, *CMOS Logic Circuit Design* (Kluwer Academic Publishers 2002), pp. 64, 74-102, 315-17, 458-60.
Ex. 1021	Khalil Jumah Tawfiq Hamam, Organic Solar Cells Based on High Dielectric Constant Materials: An Approach to Increase Efficiency (June 2013) (Ph.D. dissertation, Western Michigan University), pp. 1-122.

Exhibit	Description
Ex. 1022	P. Kalugasalam et al., *Dielectric and AC Conduction Studies of Lead Phthalocyanine Thin Film*, Chalcogenide Letters, Vol. 6, No. 9 (Sept. 2009), pp. 469-76.
Ex. 1023	Gopal G. Pethuraja et al., *Current-Voltage Characteristics of ITO/p-Si and ITO/n-Si Contact Interfaces*, Advances in Materials Physics and Chemistry, Vol. 2 (2012), pp. 59-62.
Ex. 1024	Giampiero de Cesare et al., *Electrical Properties of ITO/Crystalline-Silicon Contact at Different Deposition Temperatures*, IEEE Electron Device Letters, Vol. 33, No. 3 (Mar. 2012), pp. 327-29.
Ex. 1025	Wen-Jang Jiang et al., *The effect of indium tin oxide as an ohmic contact for the 850 nm GaAs oxide-confined VCSELs*, Solid-State Electronics, Vol. 46 (2002), pp. 1945-48.
Ex. 1026	*IEEE 100 - The Authoritative Dictionary of IEEE Standards Terms*, IEEE (7th ed. 2000), pp. 333, 1205.
Ex. 1027	Christian C. Fesenmaier et al., *Optical confinement methods for continued scaling of CMOS image sensor pixels*, Optics Express, Vol. 16, No. 25 (Dec. 2008), pp. 20457-70.
Ex. 1028	Leonard Rubin et al., *Ion Implantation in Silicon Technology*, Industrial Physicist, 9(3), (Jun/July 2003), pp. 12-15.
Ex. 1029	Jurgen Michel et al., *Advances in fully CMOS integrated photonic devices*, Proceedings of SPIE, Vol. 6477 (2007), pp. 64770P-1 to -11.
Ex. 1030	Mark Beals et al., *Process Flow Innovations for Photonic Device Integration in CMOS*, Proceedings of SPIE, Vol. 6898 (2008), pp. 689804-1 to -14.
Ex. 1031	Donald A. Neaman, *Semiconductor Physics and Devices – Basic Principles* (McGraw Hill 3d ed. 2003), pp. 247-50, 260-61.
Ex. 1032	Adel S. Sedra et al., *Microelectronic Circuits* (Oxford University Press 7th ed. 2015), pp. 155-56.
Ex. 1033	Chung-Wei Chang et al., *High Sensitivity of Dielectric films Structure for Advanced CMOS Image Sensor Technology*, 2007

Exhibit	Description
	International Image Sensor Workshop, IEEE Electron Devices Society (2007), pp. 207-10.
Ex. 1034	Matthew Sauceda, *Porphyrin Thin Film Dielectrics*, SUNFEST Technical Report TR-CST01NOV04, Center for Sensor Technologies, Univ. of Pennsylvania, Philadelphia, PA (2004), pp. 181-98.
Ex. 1035	N. Venkatramaiah et al., *Spectroscopic and dielectric studies of meso-tetrakis(p-sulfonatophenyl) porphyrin doped hybrid borate glasses*, Journal of Alloys and Compounds, Vol. 509 (2011), pp. 2797-803.
Ex. 1036	Tom J. Savenije, *Photogeneration and transport of charge carriers in a porphyrin p/n heterojunction*, Physical Review B, Vol. 55, No. 15 (Apr. 1997), pp. 9685-92.
Ex. 1037	Ümit Salan et al., *Synthesis, characterization, electrical and dielectric permittivity measurements of 2,9,16,23-tetra(4-ferrocenylimino-3-nitrophenoxy)phthalocyanines*, Journal of Porphyrins and Phthalocyanines, Vol. 10 (2006), pp. 1263-70.
Ex. 1038	Teresa M. Figueira-Duarte et al., *Pyrene-Based Materials for Organic Electronics*, Chemical Reviews, Vol. 111 (2011), pp. 7260-314.
Ex. 1039	*Handbook of Wafer Bonding* (Peter Ramm et al. eds., Wiley-VCH Verlag & Co. KGaA 2012), pp. 52-54, 63-64, 112-15.
Ex. 1042	U.S. Patent No. 10,468,543 B2 to Wang et al. ("'543 Patent")
Ex. 1044	Prosecution History of the '543 Patent (downloaded from Public PAIR)
Ex. 1045	J. W. Levell et al., *A hybrid organic semiconductor/silicon photodiode for efficient ultraviolet photodetection*, Optics Express, Vol. 18, No. 4 (2010), pp. 3219-3225.
Ex. 1046	*W&Wsens Devices Inc. v. Samsung Electronics Co. Ltd. et al.*, Case No. 2:24-cv-00854, Plaintiff's Infringement Contentions, Appendix C-1 (Jan. 7, 2025)

Exhibit	Description
Ex. 1047	*W&Wsens Devices Inc. v. Samsung Electronics Co. Ltd. et al.*, Case No. 2:24-cv-00854, Plaintiff's Infringement Contentions, Appendix C-2 (Jan. 7, 2025)

V. LEGAL STANDARDS

31. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

32. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can "anticipate" a claim. Second, I have been informed that the prior art can render a claim "obvious" to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

33. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

34. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 of the ’543 Patent from the perspective of a person of ordinary skill in the art at the ’543 Patent’s earliest claimed priority date (May 22, 2013), as described in more detail below.

35. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

36. For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

37. I have been informed that a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

38. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

39. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as "prior art." I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the "effective filing date"). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

C. Anticipation

40. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if it is not novel, including if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is

anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

41. I have been informed that under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

42. I have been informed that a proper obviousness analysis includes the following:

a. Determining the scope and content of the prior art;

b. Ascertaining the differences between the prior art and the claims at issue;

c. Resolving the level of ordinary skill in the pertinent art; and

d. Considering evidence of secondary indicia of non-obviousness (if available). I am not aware of any evidence of

secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the ’543 Patent.

43. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the Challenged Claims is May 22, 2013. My opinions would not change if I assumed a later date of invention.

44. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art’s own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

45. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or

individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

46. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success"—but not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

47. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of

ordinary skill in the art would have had a good reason to pursue those known options.

48. I have been informed that the law permits the application of "common sense" in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

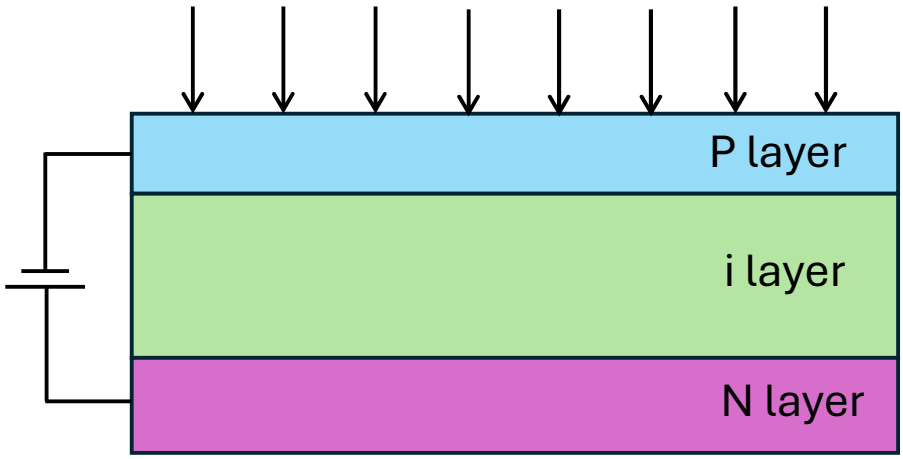
49. I have been informed that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine references. But I also understand that the "teaching, suggestion, or motivation" test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

50. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE PRIOR ART

A. Photodetectors

51. A photodetector is a semiconductor device that transforms photons into electrical signals, enabling electrical circuits to detect and measure incident light. As illustrated below, a PiN photodetector is a specific type of photodiode characterized by an intrinsic (undoped) layer positioned between highly doped P-type and N-type semiconductor layers (hence the name "PiN"):



52. When light enters the photodetector, photons are absorbed in the intrinsic layer, generating electron-hole pairs. Applying a negative bias across the photodetector causes the separated electrons to move towards the N-type layer and the holes towards the P-type layer, producing a measurable photocurrent.

B. Microstructure-Enhanced Photodetectors

53. Conventional silicon photodetectors exhibit high responsivity at wavelengths of light less than about 850 nm. Ex. 1010, 1. The prior art recognized that tailoring the microstructure of silicon can extend the operability of these photodetectors to longer wavelengths, such as infrared. For instance, etching the surface of a silicon photodetector to create micron-sized pillars or grooves was known to enhance a photodetector's responsiveness at longer wavelengths. Ex. 1010, 1-2; Ex. 1011, 1-6. The images below illustrate photodiodes with laser-etched microstructures designed to enhance their responsiveness at longer wavelengths.

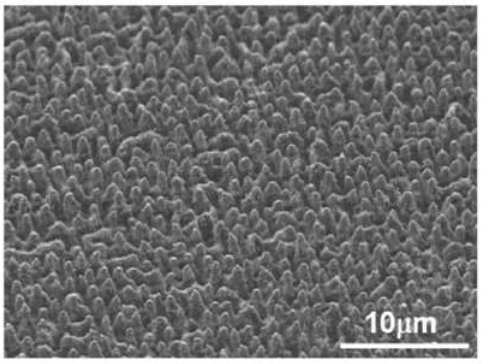


FIG. 1. Scanning electron micrographs of microstructured Si surface.

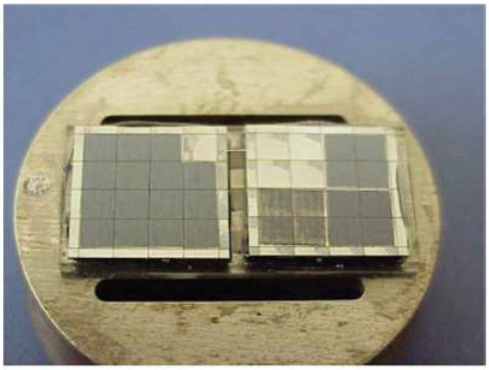


Fig. 1. (Color online) Picture of two microstructured APD arrays prior to packaging. Structuring was performed with an 800 nm fs laser operating at a fluence of 3.5 kJ/m^2 in an atmosphere of SF_6. The array on the right had four different structured regions with a pulse number ranging from 0 to 300. The shiny area is the bare silicon.

Ex. 1010, 1 (left); Ex. 1011, 2 (right).

54. Photodetectors featuring microstructures enhanced by etched holes were widely known and utilized well before the purported invention. For example, *NXP* (Ex. 1006) discloses a single-chip device 1300 where a silicon PiN photodiode is integrated with CMOS signal processing circuitry (not shown in Figure 13 below) on the same substrate 102. *NXP*, ¶¶[15], [32], [42], [85].

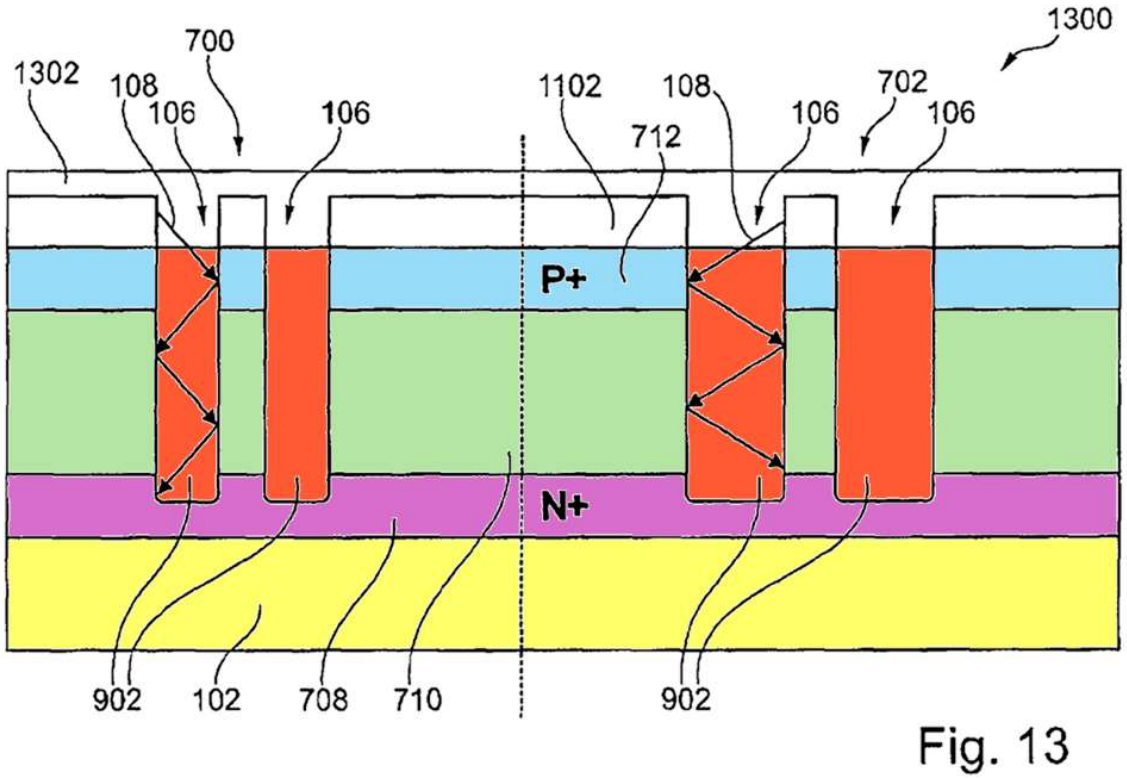


Fig. 13

NXP, Fig. 13.[1]

[1] All color and colored annotations in the figures of this Declaration have been added.

55. The PiN photodiode above includes an intrinsic layer 710 disposed between an N^+ layer 708 and a P^+ layer 712 and holes or pores 106 formed on the PiN layers by etching. *NXP*, ¶¶[77]-[78]. *NXP* discloses that the presence of pores 106 in the PiN photodiode increases the quantum efficiency of the photodiode. *NXP*, ¶¶[13], [15], [38]. Quantum efficiency is a measure of how effectively the photodiode converts incoming optical energy into electrical signals. *See* Ex. 1012, 4; Ex. 1013, 4.

56. As another example, *Wang* (Ex. 1007) discloses a photonic device 100 comprising a PiN structure with a stacked p-semiconductor region 108, intrinsic semiconductor region 110, and an n-semiconductor region 106. *See Wang*, ¶[28], Figs. 1-2. A thin doped region 112 overlays the surface of the p-region 108, and a periodic array of holes or recesses 116 extends into the PiN structure through the overlying region 112. *Wang*, ¶¶[29]-[32].

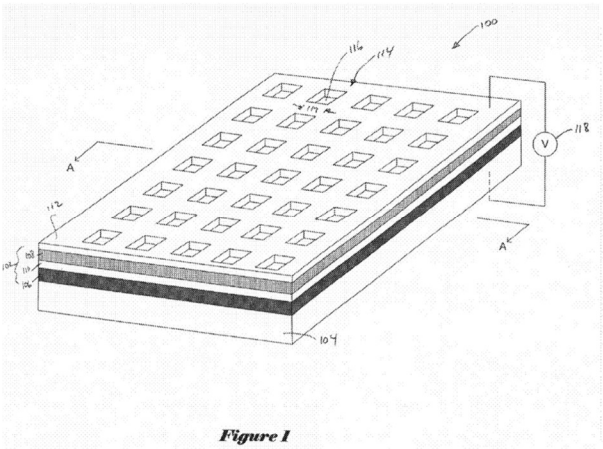


Figure 1

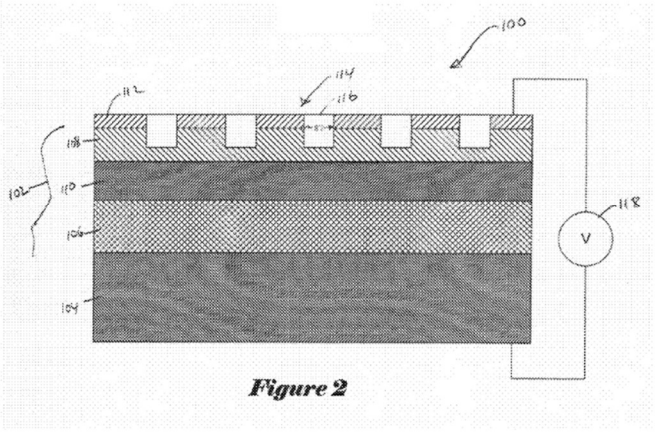


Figure 2

Wang, Figs. 1, 2.

C. Photodetectors and Processing Circuitry on a Single Substrate

57. The integration of photodetectors and signal processing circuitry on a single substrate to form a single-chip device was known long before the purported invention date of the ’543 Patent. Ex. 1012, 1-14; Ex. 1013, 1-8; Ex. 1014, 1-2. For instance, *NXP* teaches that integrating signal processing circuitry and the photodiode on the same substrate “may be more reliable than a discrete solution” and result in a smaller package, which is advantageous for mobile applications. *NXP*, ¶¶[16], [32], [37].

58. Beginning in late 1980s, advancements in CMOS technology enabled the fabrication of both photodetectors and signal processing electronics on the same substrate. Ex. 1012, 2-3, 10. For example, researchers at NASA’s Jet Propulsion Laboratory developed the CMOS active pixel sensor (“APS”), which integrated a photodiode, amplifier, and signal processing circuitry within each pixel of an image sensor. Ex. 1012, 2-3. This allowed for on-chip conversion of light to electrical signals and immediate processing. Ex. 1012, 2-3; Ex. 1013, 4. This CMOS APS is shown below:

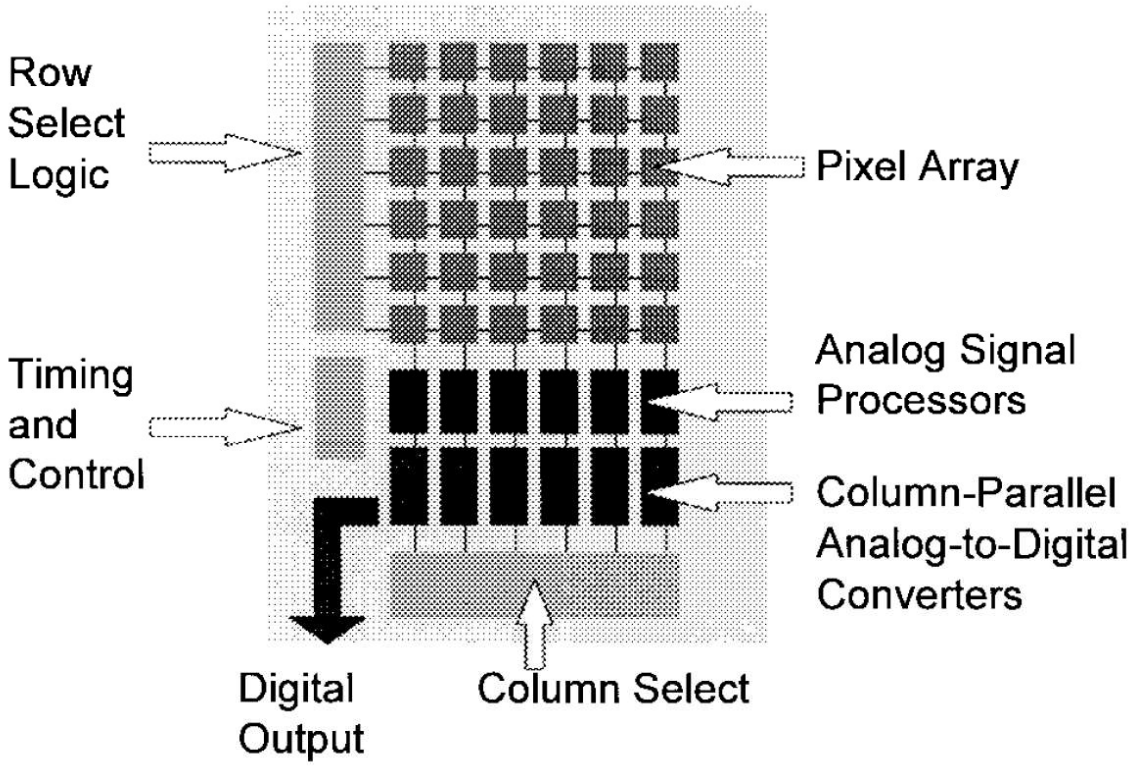
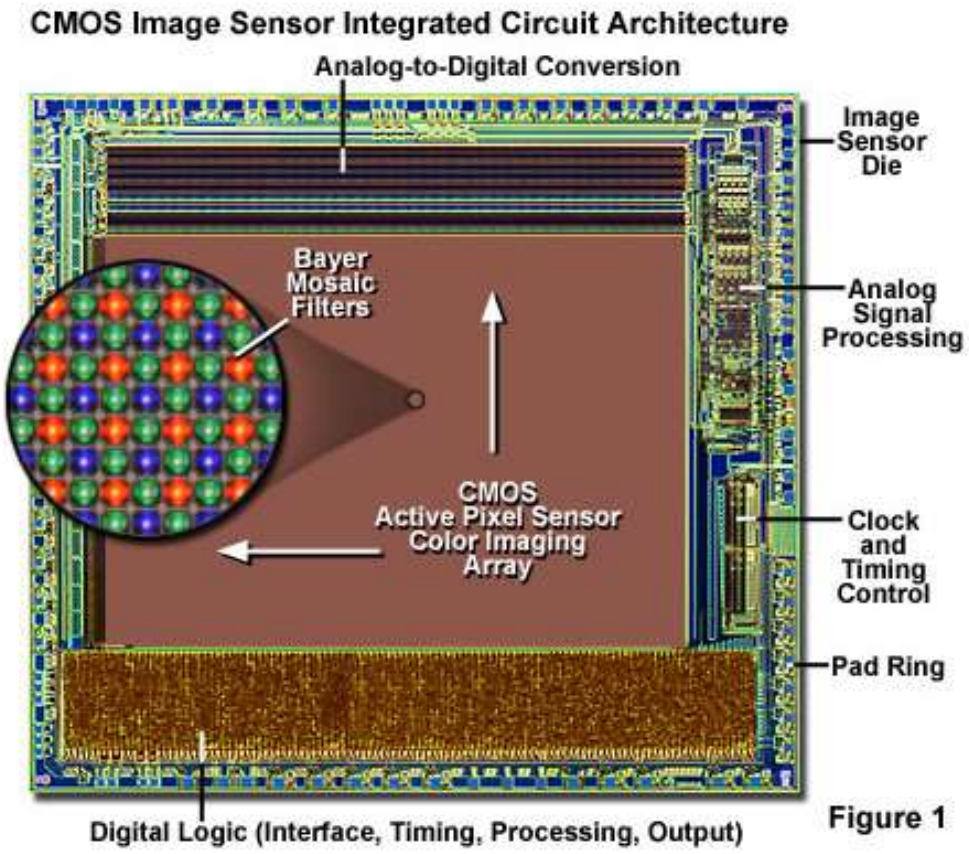


Fig. 2. CMOS APS integrates timing and control, ADC, and other circuitry on the same chip.

Ex. 1013, 3.

59. The integration of the photodiode and processing circuitry on the same chip reduced power consumption, lowered manufacturing costs, and allowed for smaller, more efficient imaging devices. Ex. 1012, 3, 10, 12; Ex. 1013, 8.

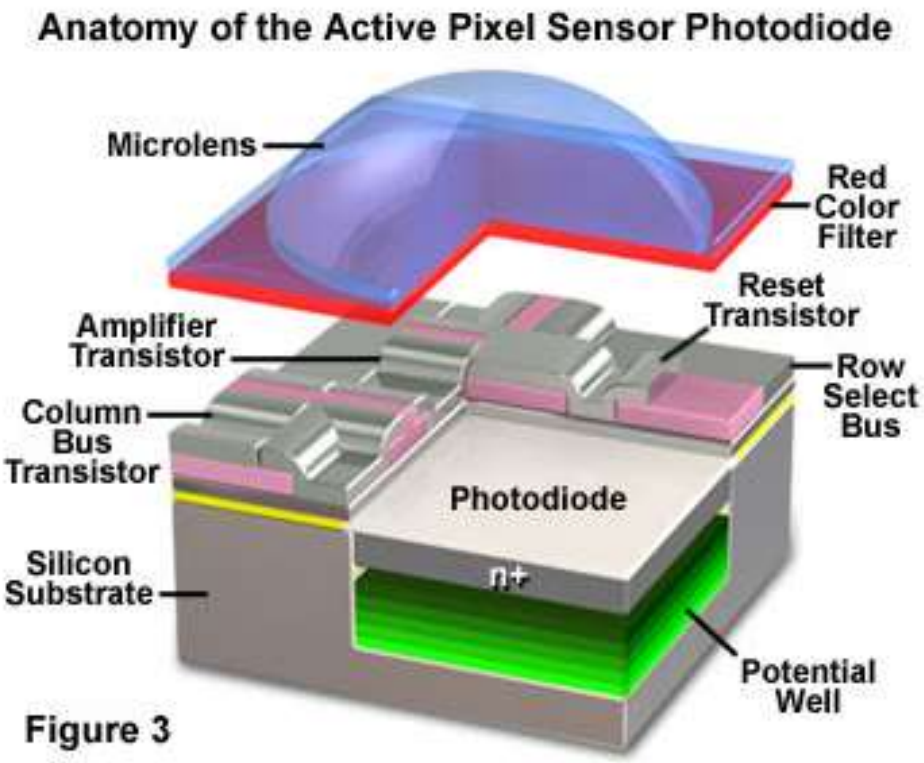
60. By the early 2000s, APS technology was prevalent in consumer electronics such as digital cameras, smartphones, and webcams. Ex. 1012, 1-3; Ex. 1015, 9. An image of a CMOS APS image sensor die is shown below.



Ex. 1015, 1.

61. This image sensor die includes an array of photodiodes (640 x 480 pixels) located in the large reddish-brown central area of the chip and analog signal processing circuitry to collect and interpret the signals generated by the photodiode array. Ex. 1015, 2-3, Fig. 1.

62. A three-dimensional cutaway drawing of the above image sensor is shown below, illustrating a single photodiode and associated transistors that process the signals produced by the photodiode on a single substrate. Ex. 1015, 3-5.

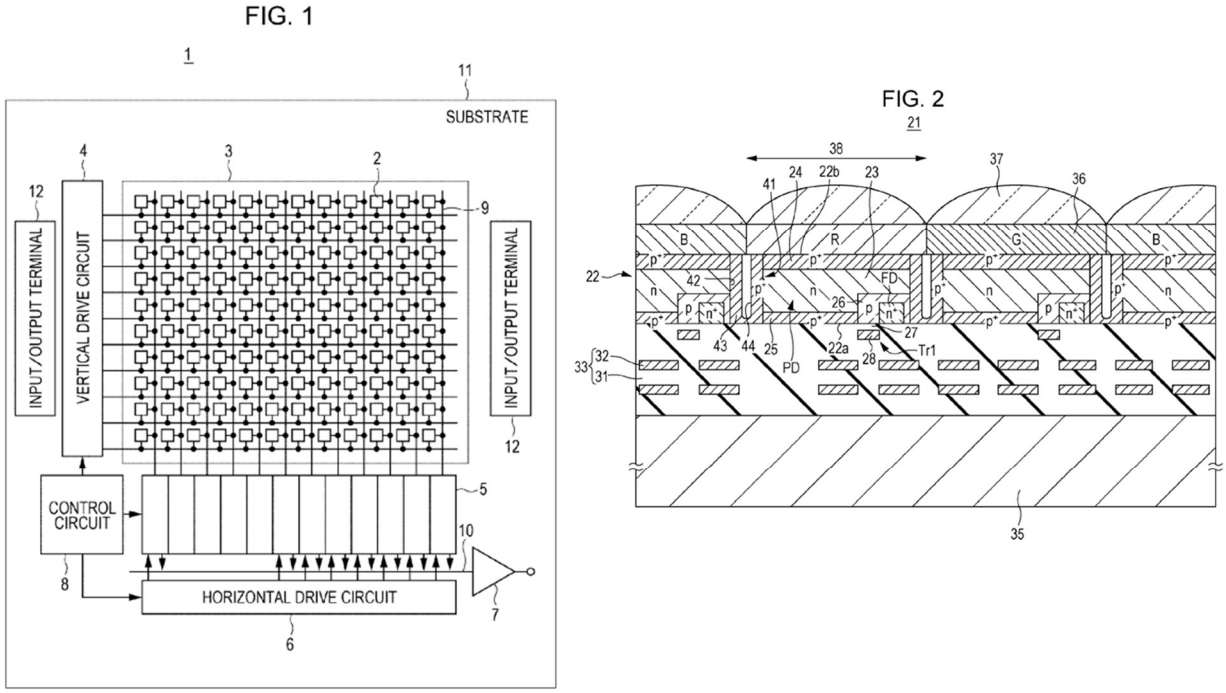


Ex. 1015, 3.

63. To focus the incident light on the photodiode, the photodiode is positioned beneath a microlens and a color filter to capture color information from the incident light. Ex. 1015, 3-4, Fig. 3.

64. Well before the purported invention date of the ’543 Patent, numerous published references disclosed single-chip devices integrating photodetectors and signal processing circuitry on a single substrate. For example, *Kuboi* (Ex. 1004), discussed below, describes such a device. *Infra* VIII.A. Moreover, *Kuboi* discloses all features of the challenged claims. *Infra* XI.A. *Shinohara* (Ex. 1005) discloses a

similar single-chip device incorporating photodetectors and signal processing circuitry. *See Shinohara*, Figs. 1-2, ¶¶[51]-[63].



Shinohara, Figs. 1, 2.

65. Like *Kuboi*'s imaging device 201 (*see Kuboi*, Fig. 15, ¶¶[48]-[54]), *Shinohara*'s imaging device 1 features a pixel region 3 with a two-dimensional pixel array 2 and a peripheral circuit portion integrated on the same semiconductor substrate 11. *See Shinohara*, ¶[51]; *see infra* VIII.A. In *Shinohara*, each pixel 2 contains a photoelectric conversion portion and four pixel transistors, similar to *Kuboi*. *Shinohara*, ¶[51]; *see Kuboi*, ¶[48]; see *infra* VIII.A. Additionally, akin to *Kuboi*, *Shinohara*'s peripheral circuit portion includes various logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive

circuit 6, an output circuit 7, and a control circuit 8. *Shinohara*, ¶[52]; *see Kuboi*, ¶[49]; see *infra* VIII.A. In *Shinohara*'s imaging device 1, the photodiode-based photoelectric conversion portion and pixel transistors are formed on a single semiconductor substrate (substrate 22), along with the logic circuits of the peripheral circuit portion. *See Shinohara*, ¶¶[3]-[4], [58], [81].

VII. THE '543 Patent

A. Alleged Invention of the '543 Patent

66. The '543 Patent details a single-chip device that integrates photodetectors (referred to as MSPDs and MSAPDs) with CMOS active electronic circuits on a single substrate. '543 Patent, 2:64-67, 4:65-5:5, 6:24-29.

67. The photodetectors disclosed by the '543 Patent include a silicon substrate with a first layer (a P layer), a very low doped N or P layer called the intermediate layer (or i layer), and a second layer (an N layer) with holes etched in one or more of the PiN layers. '543 Patent, 22:9-41, 16:38-42, 26:29-27. The '543 Patent discloses that optical signals impinge on the top and/or bottom surfaces of the photodetectors. '543 Patent, 16:23-27. According to the '543 Patent, because of the holes, light interacts with the absorbing layer(s) for a longer length of time, resulting in enhanced light absorption and a larger external quantum efficiency over a similar structure without holes. '543 Patent, 15:48-56. Figure 14, which is shown below, depicts the photodetector disclosed by the '543 Patent:

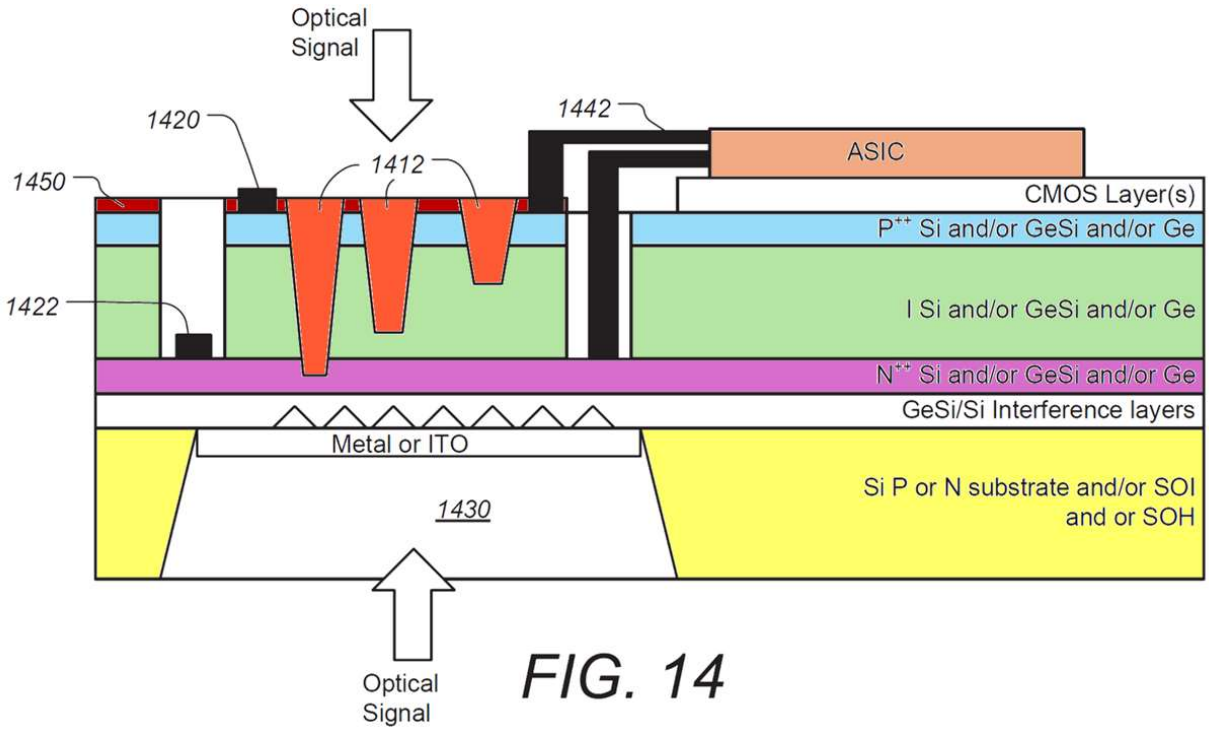


FIG. 14

'543 Patent, Fig. 14, 10:60-62, 26:42-44.

68. The photodetector of the '543 Patent is monolithically integrated with signal processing circuits (such as ASIC) on the same substrate to form a single-chip device. '543 Patent, 19:2-6, 23:43-46, 26:42-44. Notably, the '543 Patent recognizes that it was well known to integrate photodetectors with signal processing circuits on a single silicon substrate to reduce cost and improve performance. '543 Patent, 28:58-29:3, 32:50-67, 47:11-21.

B. Prosecution History

69. The application that resulted in the '543 Patent (or the "'543 application") was filed on March 8, 2019, as a continuation application of the '700

Patent, and claiming priority to several patent applications, the earliest of which was filed on May 22, 2013. Ex. 1044, 257-638.

70. The originally-filed claims of the ’543 application closely resemble those issued in the ’700 Patent (Ex. 1001). *See* Ex. 1044, 632-633; ’700 Patent, 118:25-119:4. Originally filed independent claim 113 of the ’543 application—now independent claim 1 of the ’543 Patent—is presented below, with changes from the independent claim of the ’700 Patent indicated using underlines and strikethroughs.

> 113. A single-chip device comprising an integrated combination of a microstructure-enhanced photodetector (MSPD) configured for reverse-bias operation and an active electronic circuit, both formed on or in a single substrate and configured to receive an optical input that in cross-section is substantially continuous spatially, convert the optical input to an electrical output, and process the electrical output into a processed output, wherein:
>
> > the MSPD on or in said single substrate comprises an intermediate ~~layer~~ region, a first ~~layer~~ region at one side of the intermediate ~~layer~~ region, and a second ~~layer~~ region at an opposite side of the intermediate ~~layer~~ region, wherein:

each of the ~~layers~~ regions comprises Silicon, Germanium, or an alloy thereof;

at least one of said ~~layers~~ regions, or an overlying covering ~~layer~~ region that may be present, has holes intentionally formed therein~~, extending in directions transverse to the layers~~;

each of the first and second ~~layers~~ regions comprises a doped material;

the intermediate ~~layer~~ region comprises a material that is less doped than at least one of the first and second ~~layers~~ regions or is undoped, wherein the degree of doping is the same or different for different positions in the intermediate ~~layer~~ region;

an input portion configured to concurrently receive at a plurality of said holes said optical input that has said substantially continuous cross-section; and

an output portion configured to provide said electrical output from the MSPD;

the MSPD includes reverse-bias ~~electrodes~~ contacts coupled therewith to establish an electrical field therein when energized to thereby

sweep in a selected direction electrical charges generated in the MSPD by said optical input;

said reverse-bias electrodes being free of a pattern of openings that matches said holes; and

the active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:

amplification to form said processed output from the single-chip device;

processing other than or in addition to amplification to form said processed output from the single-chip device; and

routing to one or more selected destinations; and

a communication channel on or in said single-chip device, configured to deliver the electrical output from the MSPD to the active electronic circuit.

Compare Ex. 1044, 632-633, *with* '700 Patent, 118:25-119:4.

71. Regarding the limitation highlighted in the red box above, during prosecution of the '700 Patent, the Examiner indicated that the phrase "overlying covering layer that may be present … merely states [that] the overlying layer [is] an optional component," and does not require the presence of this overlying layer. Ex. 1003, 387. Later, during prosecution of the '543 Patent, the same Examiner

noted this claim limitation could introduce "potential 112 scope of enablement issues" as it might be interpreted to restrict the presence of holes solely to the covering region, an interpretation unsupported by the disclosure. Ex. 1044, 124-125. To address this concern, the Examiner proposed—and the Patent Owner agreed—to amend "overlying covering region that may be present" to "optional overlying covering region." Ex. 1044, 124-125, 136. Thus, in my opinion, the Examiner viewed the "***optional*** overlying covering region" to be an "overlying covering region ***that may be present***" without mandating its presence.

72. The claims were then allowed with the Examiner noting that the "prior art discloses a single chip device comprising a microstructure enhanced photodetector and an electronic circuit, but fails to disclose the specific characteristic recited in the claims." Ex. 1044, 135-137. However, the Examiner did not consider *Kuboi*, which teaches all of these characteristics and renders the challenged claims unpatentable.

C. Claim Construction

73. I have been instructed that the "intrinsic record" includes the patent itself, including the claims, description, and figures (Ex. 1042), and the patent's prosecution history (Ex. 1044)—i.e., the record of proceedings at the U.S. Patent and Trademark Office ("Patent Office") concerning the patent. I understand that, like the claims and written description, the prosecution history provides evidence

to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term's plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent's written description, the patent's prosecution history, or both.

74. I understand that claim interpretation may also be informed by "extrinsic evidence" (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the art (POSITA) in the relevant time period.

75. I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '543 Patent. Based on my review of the materials and my personal knowledge and experience, I have considered each term of the '543 Patent as it would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '543 Patent (May 22, 2013).

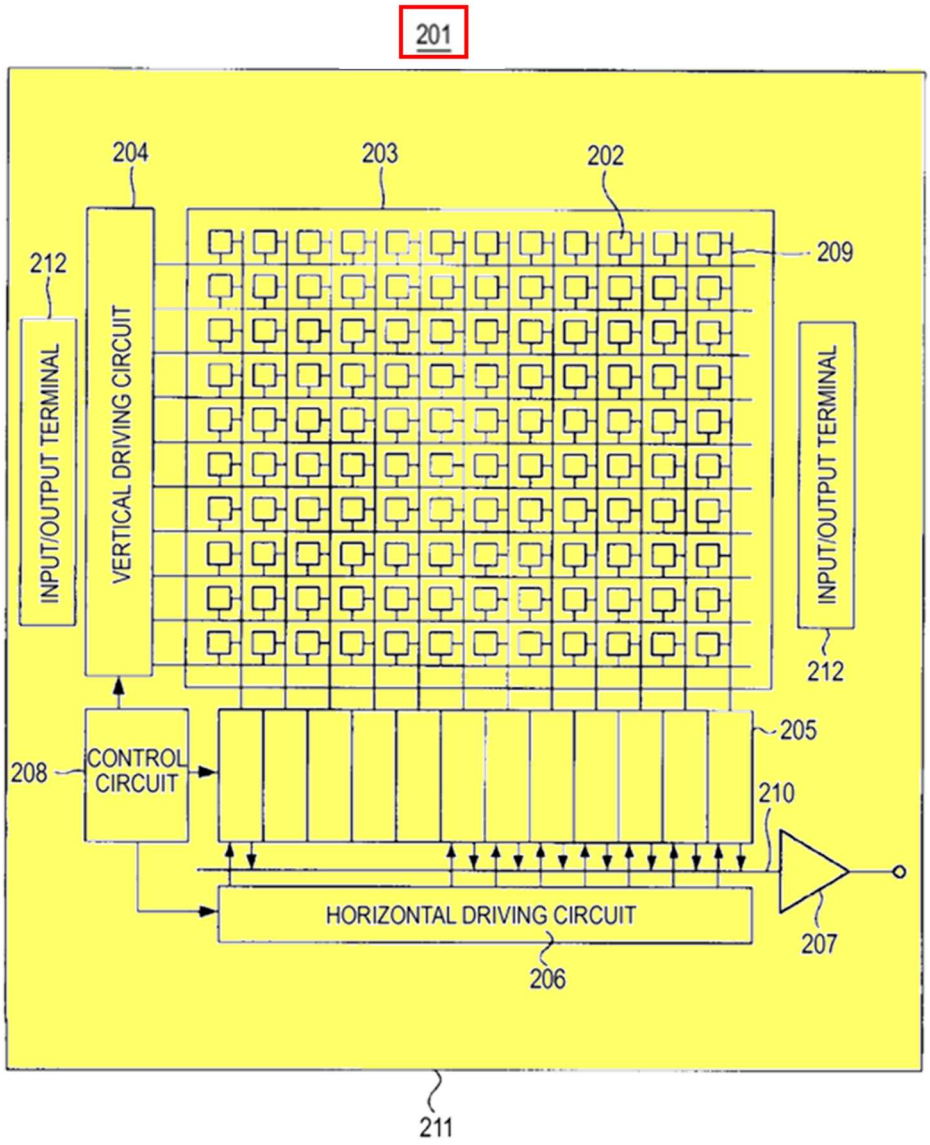
VIII. SUMMARY OF THE PRIOR ART

A. *Kuboi*

76. *Kuboi*, titled Solid-State Imaging Device, Manufacturing Method Thereof, and Electronic Apparatus, was filed on August 19, 2011, and published as U.S. Patent Publication No. 2012/0049044 on March 1, 2012. I understand that *Kuboi* is prior art to the '543 Patent.

77. *Kuboi* discloses a CMOS solid-state imaging device 201 that includes a pixel region 203 and a peripheral circuit portion on a single semiconductor substrate 211. *Kuboi*, ¶[48], Fig. 15.

FIG.15



Kuboi, Fig. 15.

78. Pixel region 203 of substrate 211 comprises a plurality of pixels 202 arranged in a two-dimensional array. *Kuboi*, ¶[48]. Each pixel 202 contains one photoelectric conversion portion (or a photodiode) and four pixel transistors. *Kuboi*, ¶[48]. The peripheral circuit portion includes "logic[] circuits" (such as a vertical driving circuit 204, column signal processing circuits 205, horizontal

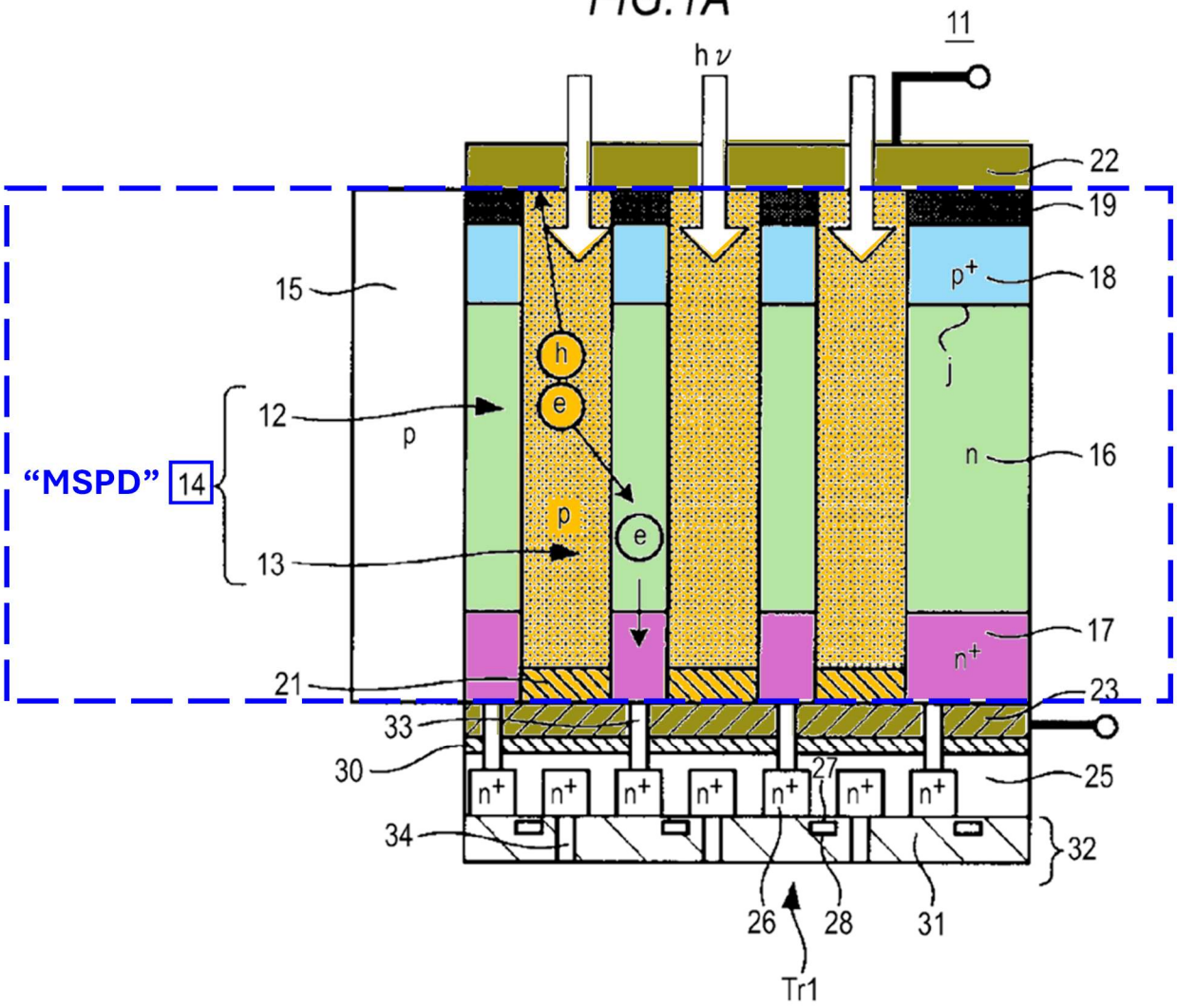
driving circuit 206, output circuit 207, and control circuit 208), which process the electrical output of the pixels and then output it. *Kuboi*, ¶¶[49]-[54]. The pixels and the peripheral circuit portion are fabricated on a single substrate, and the pixel transistors are fabricated on another substrate and the two substrates are bonded together. *Kuboi*, ¶¶[62], [70], [78].

79. *Kuboi* describes photoelectric conversion portions suitable for use in imaging device 201. *Kuboi*, ¶[48]. For example, *Kuboi* discloses a basic pixel configuration with reference to Figures 1A/1B. *Kuboi*, ¶[55]. *Kuboi* likewise discloses a pixel configuration in Figures 6A/6B, explaining that the disclosed red and green pixels 53R and 53G have a structure that is the same as the basic configuration of Figures 1A/1B. *Kuboi*, ¶¶[90], [95], [69]. *Kuboi* also discloses that Figure 13 includes pixels 53R, 53G, and 53B, having configurations that are the same as the pixels of Figures 1A/1B. *Kuboi*, ¶[181]. Similarly, *Kuboi* describes Figure 15 as applicable to all of *Kuboi*'s embodiments. *Kuboi*, ¶¶[35], [48]. Further, *Kuboi*'s Figures 4A-4F show a method of manufacturing the basic pixel configuration of Figures 1A/1B. *Kuboi*, ¶¶[69]-[76]. Thus, in my opinion, a person of ordinary skill would have recognized that Figures 1A/1B, 6A/6B, 13, and 15 all disclose the pixel configuration of the same imaging device. And Figures 4A-4F of *Kuboi* disclose methods of manufacturing that same pixel configuration. Accordingly, this Declaration relies on Figures 1A/1B, 4A-4F, 6A/6B, 13, and 15,

and *Kuboi*'s associated disclosures as representative of the pixel configuration of the same imaging device 201. In addition, I believe that a person of ordinary skill would have found it obvious to combine the elements illustrated and disclosed in these figures.

80. Figure 1A, which is shown below, illustrates a photoelectric conversion portion 14 in a pixel 11 that may be used in imaging device 201. *Kuboi*, ¶¶[48], [55]-[56]. *Kuboi* explains that pixel 11, including the photoelectric conversion portion 14, can be utilized in imaging device 201. *Kuboi*, ¶¶[48], [55].

FIG.1A

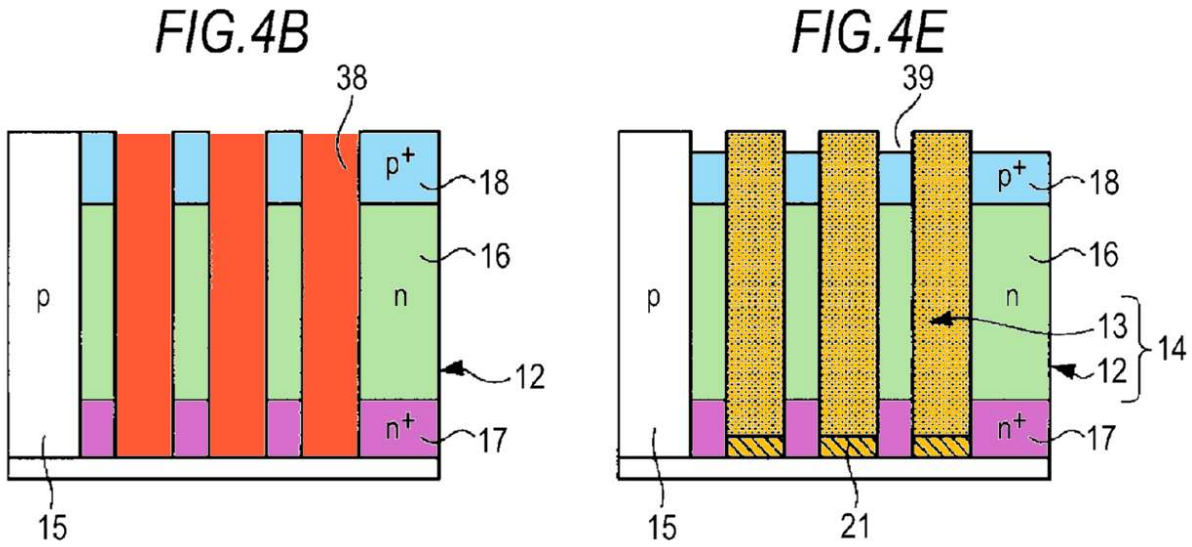


Kuboi, Fig. 1A.

81. According to *Kuboi*, photoelectric conversion portion 14 comprises a silicon semiconductor layer 12 that includes multiple embedded organic material layers 13. *Kuboi*, ¶[55]. The silicon semiconductor layer 12 is implanted with different impurities (or doped) to form an n-type semiconductor (or "intermediate") region 16 with a p^+-type semiconductor region 18 on one side and an n^+-type semiconductor region 17 on the opposite side (i.e., stacked PiN regions).

Kuboi, ¶¶[56], [71]. The doping of layer 12 is such that the p^+-type region 18 and the n^+-type region 17 have a higher concentration of impurities than the n-type region 16. *Kuboi*, ¶[56].

82. After forming regions 18, 16, and 17, vertical holes 38 extending from the p^+-type region 18 to the n^+-type region 17 are etched into the PiN regions (below left). *Kuboi*, ¶¶[71]-[72].



Kuboi, Figs. 4B, 4E.

83. Then, the organic material that forms the photoelectric conversion film 13 is deposited in these holes 38 (above right). *Kuboi*, ¶¶[72]-[73].

84. A metal light shielding film 19 is then applied to the surface of the p^+-type region 18 such that only the holes 38 containing films 13 are exposed to incident light (hν), *Kuboi*, ¶¶[59], [76], Figs. 1A, 4F. An upper electrode 22 and a lower electrode 23 are formed on opposite sides of the PiN regions, and a reverse

bias is applied. *Kuboi*, ¶¶[60], [64]. Photoelectric conversion of the incident light (hν) within films 13 (inside the holes 38) generates electron-hole pairs that pass through the depleted semiconductor layer 12 into a charge accumulation region 26 of the transfer transistor (Tr1) of the corresponding pixel 11 (via conductors 33). *Kuboi*, ¶¶[62], [64]. After initial signal processing (e.g., amplification) by the pixel transistors, the electrical signals from pixel 11 are sent to the peripheral circuits for further processing. *Kuboi*, ¶¶[48]-[49], [61]-[62].

IX. LEVEL OF ORDINARY SKILL IN THE ART

85. In rendering the opinions set forth in this declaration, I have been asked to consider the '543 Patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as "one skilled in the art," "skilled artisan," "POSITA," or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

86. Taking the factors described in the Legal Standards – Level of Ordinary Skill section into consideration, it is my opinion that a person of ordinary skill in the art pertinent to the '543 Patent (May 22, 2013) would have had at least a master's degree in electrical engineering or a similar field and at least five years

of experience working with semiconductor systems and semiconductor devices. Additional relevant work experience can compensate for less education, and vice versa.

87. I was a person of ordinary skill in the art at least as of May 22, 2013.

X. GROUNDS OF UNPATENTABILITY

88. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my opinion that claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 of the ’543 Patent would have been anticipated and/or obvious to one of ordinary skill in the art.

89. In particular, it is my opinion that claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 of the ’543 Patent would have been anticipated and/or obvious to a person of ordinary skill in the art based on the prior art shown below:

Ground	Challenged Claims	Basis	Prior Art
1A	1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35	§102	*Kuboi*
1B	1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35	§103	*Kuboi*

XI. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

90. In my opinion, claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 of the '543 Patent would have been anticipated and/or obvious to one skilled in the art as of the earliest priority date (May 22, 2013) of the '543 Patent.

A. Ground 1: Grounds 1A/1B: Claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 Are Anticipated by *Kuboi* (Ground 1A) and Obvious over *Kuboi* (Ground 1B)

1. Independent Claim 1

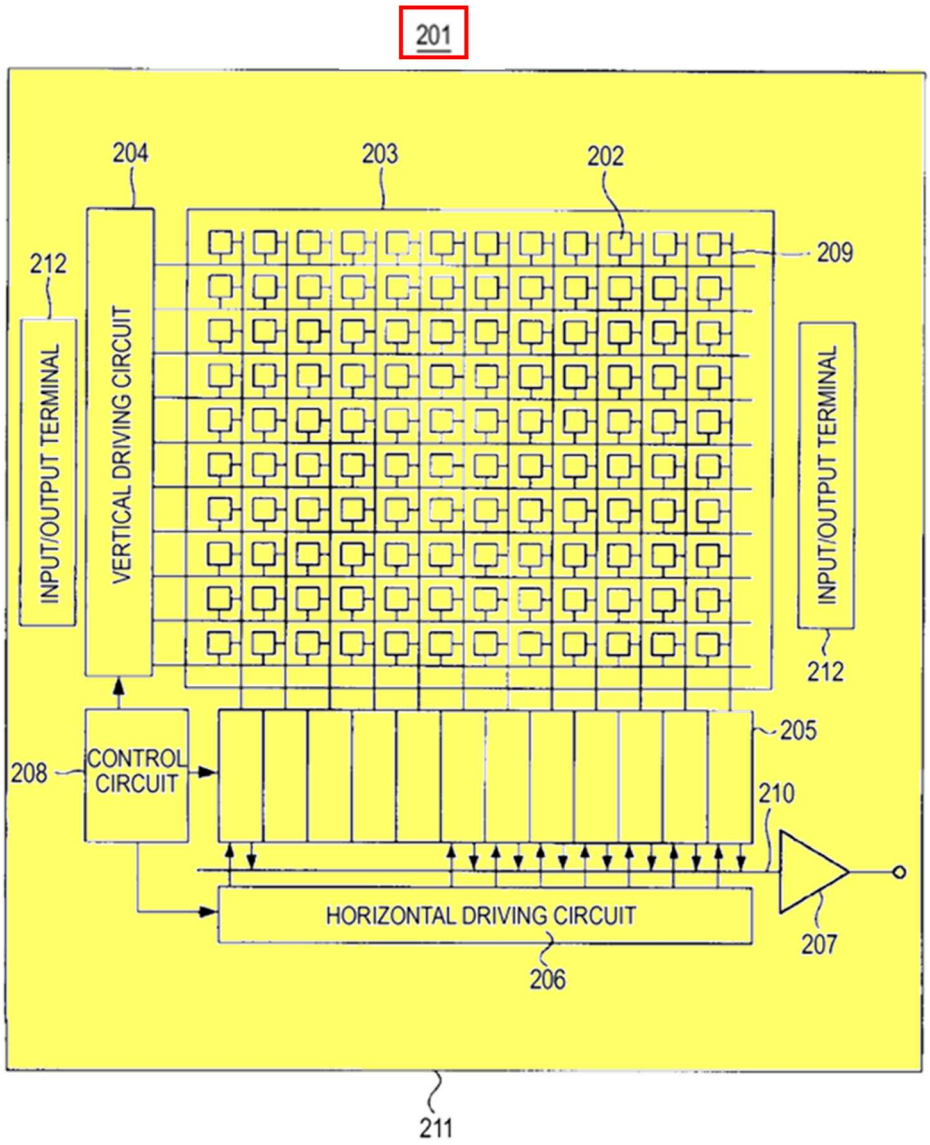
a. [1pre(a)]: "A single-chip device comprising an integrated combination of a microstructure-enhanced photodetector (MSPD) configured for reverse-bias operation and an active electronic circuit,"

91. To the extent the preamble is limiting, *Kuboi* discloses this portion of it because its CMOS solid-state imaging device ("single-chip device") is a single chip that includes multiple pixels, with hybrid microstructure-enhanced photoelectric conversion portions ("MSPD") configured for reverse-bias operation, integrated with an active electronic circuit on a single semiconductor substrate 211. *Kuboi*, ¶¶[48], [64], Fig. 15.

92. *Kuboi* discloses the claimed "single-chip device" and "microstructure-enhanced photodetector (MSPD)." *Kuboi*'s imaging device 201 "include[s] a pixel region (so-called an imaging region) 203 and a peripheral circuit portion which are

provided on a semiconductor substrate 211 (e.g., a silicon substrate)." *Kuboi*, ¶[48]. This "single-chip device" is shown below:

FIG.15

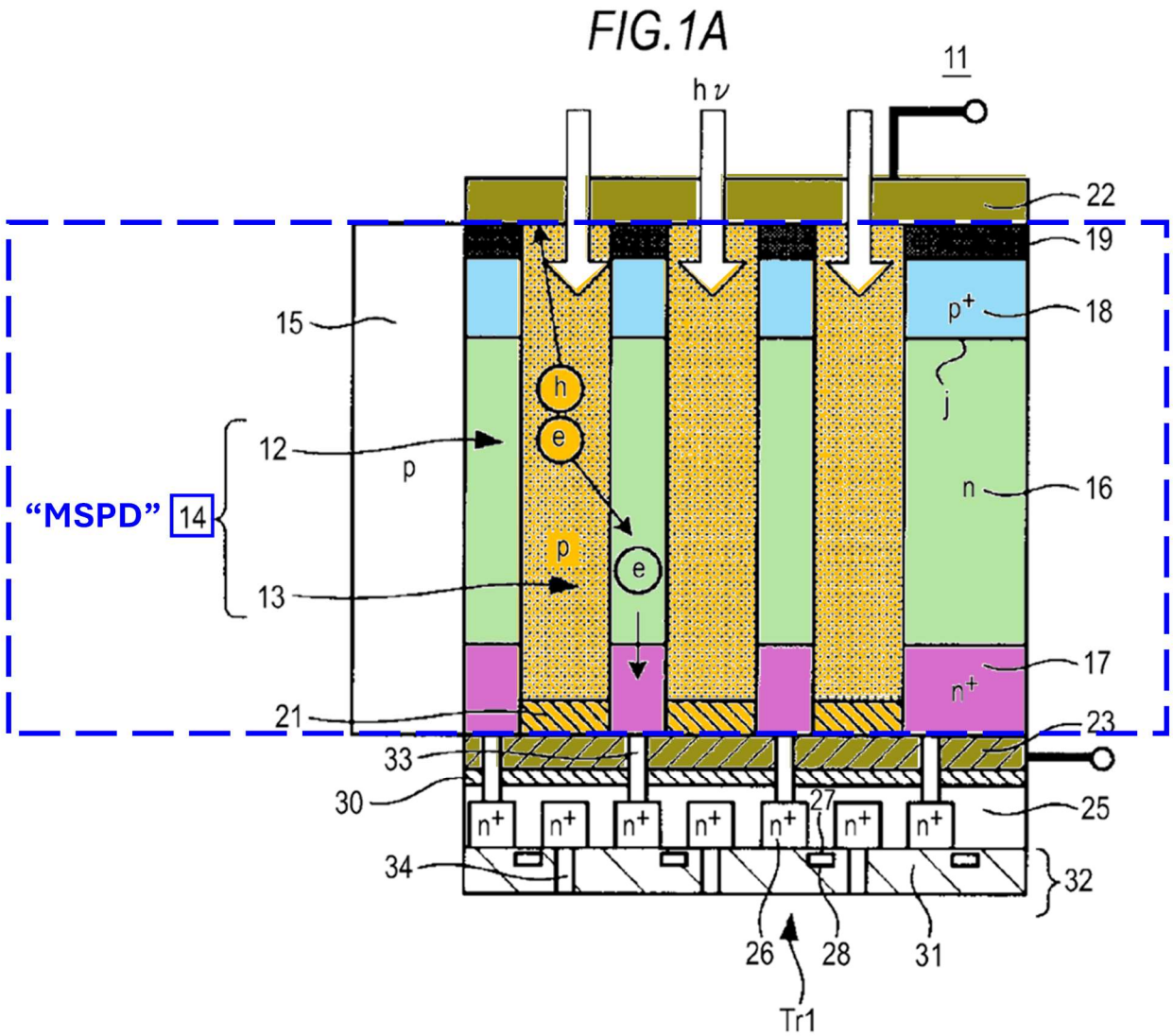


Kuboi, Fig. 15.

93. Pixel portion 203 includes a plurality of pixels 202 (elsewhere designated "pixel 11"), each of which includes a microstructure enhanced

photodetector in the form of photoelectric conversion portion 14 ("MSPD"), regularly arranged in a two-dimensional array. *Kuboi*, ¶¶[48], [55].

94. Figure 1A, which is shown below, illustrates an exemplary pixel 11, including photoelectric conversion portion 14, that may be used in imaging device 201. *Kuboi*, ¶¶[48], [55].

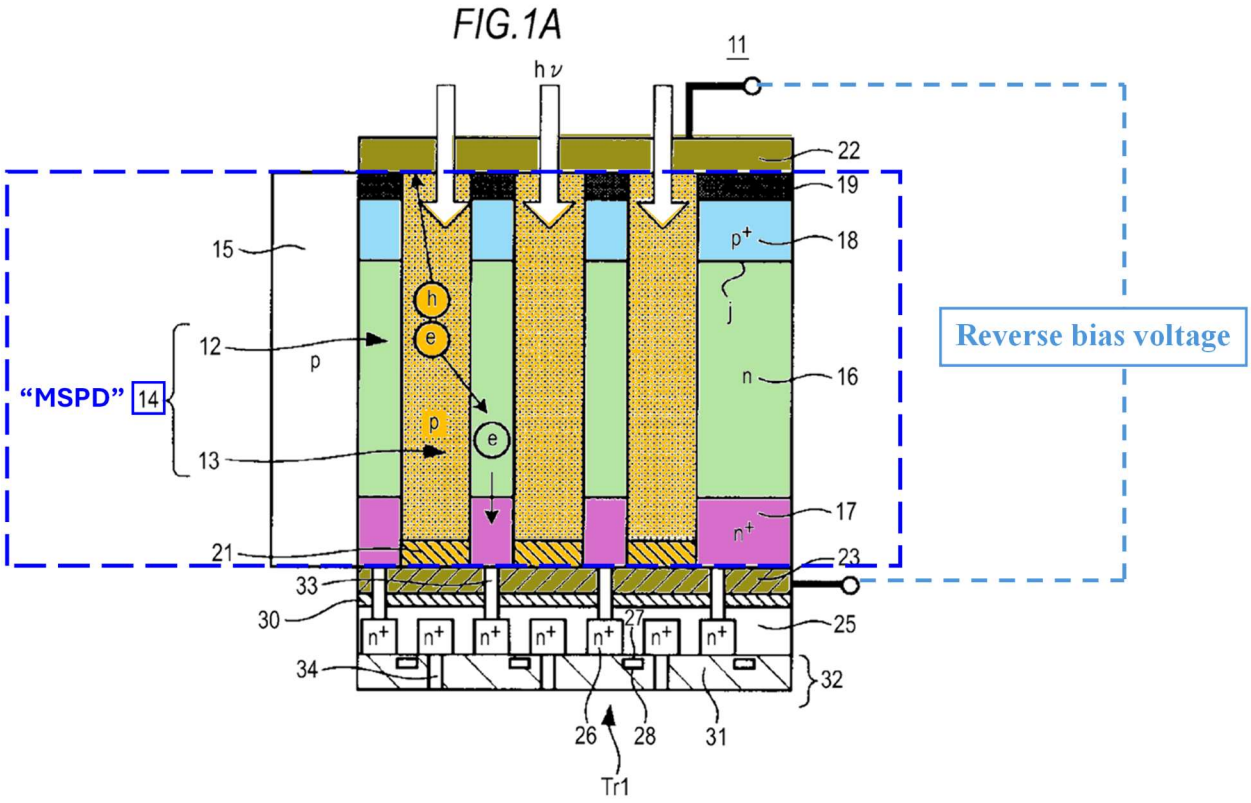


Kuboi, Fig. 1A.

95. *Kuboi*'s photoelectric conversion portion 14 comprises a semiconductor layer 12 made of silicon and doped with different concentrations of impurities to form a p^+-type region 18 and an n^+-type region 17 on opposite sides of an n-type region 16 creating a PiN photodiode. *Kuboi*, ¶¶[55]-[56], [71], Fig. 4A.

96. *Kuboi* discloses that etching vertical holes 38 and embedding photoelectric conversion films 13 in photoelectric conversion portion 14 enhances the microstructure and improves light absorption of the pixel's photoelectric conversion portion. *Kuboi*, ¶¶[72], [80]-[84], [107]-[108]. Vertical holes 38 extending from p^+-type region 18 to n^+-type region 17 are dry-etched into the semiconductor layer 12, and organic photoelectric conversion films 13 are embedded in the holes 38. *Kuboi*, ¶¶[57]-[58], [71]-[75], Figs. 4A-4E. A metal light shielding film 19 is arranged on the surface of p^+-type region 18 such that only the embedded photoelectric conversion films 13 are exposed to incident light (hν). *Kuboi*, ¶¶[57]-[59], [72]-[76]. Incident light enters photoelectric conversion films 13 and undergoes photoelectric conversion to generate electric charges corresponding to the amount of light received. *Kuboi*, ¶¶[51], [64]. *Kuboi* notes that embedding photoelectric conversion films 13 in holes in the PiN regions increases light absorption compared to photoelectric conversion portions without the embedded films 13. *Kuboi*, ¶¶[12], [71]-[75], [80]-[82], [107].

97. In my opinion, photoelectric conversion portion 14 is configured for "reverse-bias operation," as claimed. *Kuboi*, ¶¶[64], [87], [149], [171], [186], Fig. 1A. As the figure below shows, an upper electrode 22 formed on top of the metal film 19 of photoelectric conversion portion 14 makes electrical contact with the p^+-type region 18, and a lower electrode 23 is coupled to—and makes electrical contact with—the surface of the n^+-type region 17. *Kuboi*, ¶¶[59]-[60], [77], Fig. 1A.



Kuboi, Fig. 1A.

98. *Kuboi* discloses that voltage bias is applied between these electrodes, causing upper electrode 22 to have a negative potential and lower electrode 23 to

have a positive potential. *Kuboi*, ¶¶[64], [87]. This creates a depletion layer in the semiconductor layer 12. *Kuboi*, ¶¶[64], [87]. In my opinion, a person of ordinary skill would have understood that applying a voltage bias with a negative potential to the p^+-type region 18 and a positive potential to the n^+-type region 17 constitutes a reverse bias. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. For example, Exhibit 1031 discloses that reverse bias is "[t]he condition in which a positive voltage is applied to the n region with respect to the p region of a pn junction." Ex. 1031, 3-5, 8.

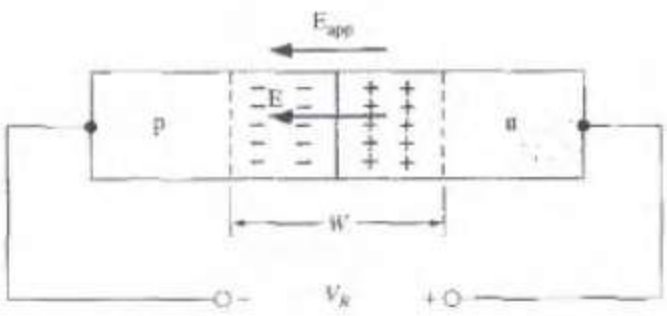
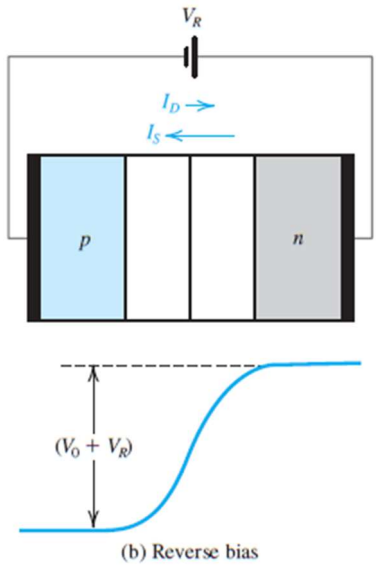


Figure 7.8 | A pn junction, with an applied reverse-bias voltage, showing the directions of the electric field induced by V_R and the space charge electric field.

Ex. 1031, 5.

99. In addition, Exhibit 1032 teaches that when a positive potential is applied to the n region and a negative potential to the p region of a pn junction, the resulting voltage bias establishes a reverse bias. Ex. 1032, 3-4 (*see* Fig. 3.11).

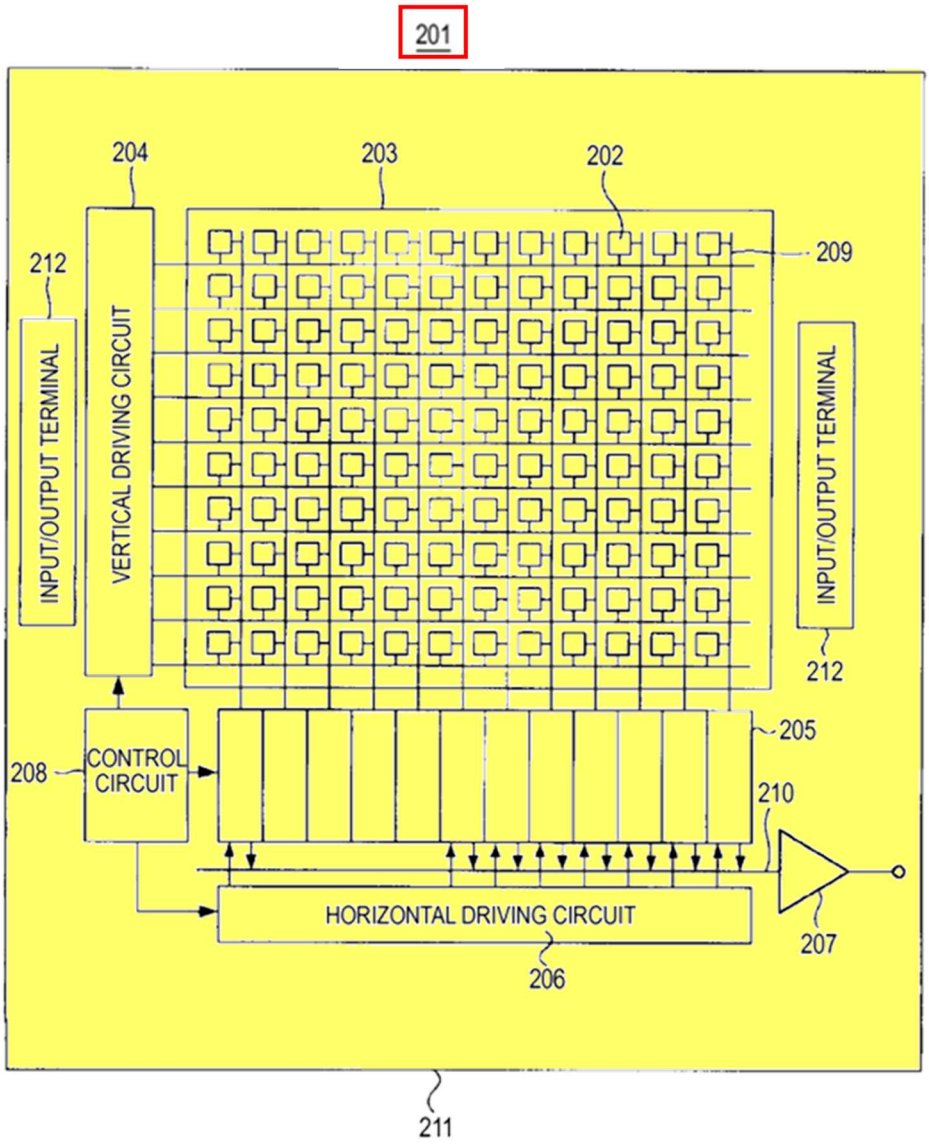


(b) reverse bias; (c) forward bias.

Ex. 1032, 4 (Fig. 3-11 cropped)

100. *Kuboi* also discloses the claimed "active electronic circuit," which is integrated with photoelectric conversion portion 14. Imaging device 201 includes a peripheral circuit portion with "logical circuits" (logic circuits). *Kuboi*, ¶¶[48]-[49], [78], Fig. 15. The "logic[] circuits" of the peripheral circuit portion include a vertical driving circuit 204, multiple column signal processing circuits 205, a horizontal driving circuit 206, an output circuit 207, and a control circuit 208. *Kuboi*, ¶[49]. Each can be seen below.

FIG.15



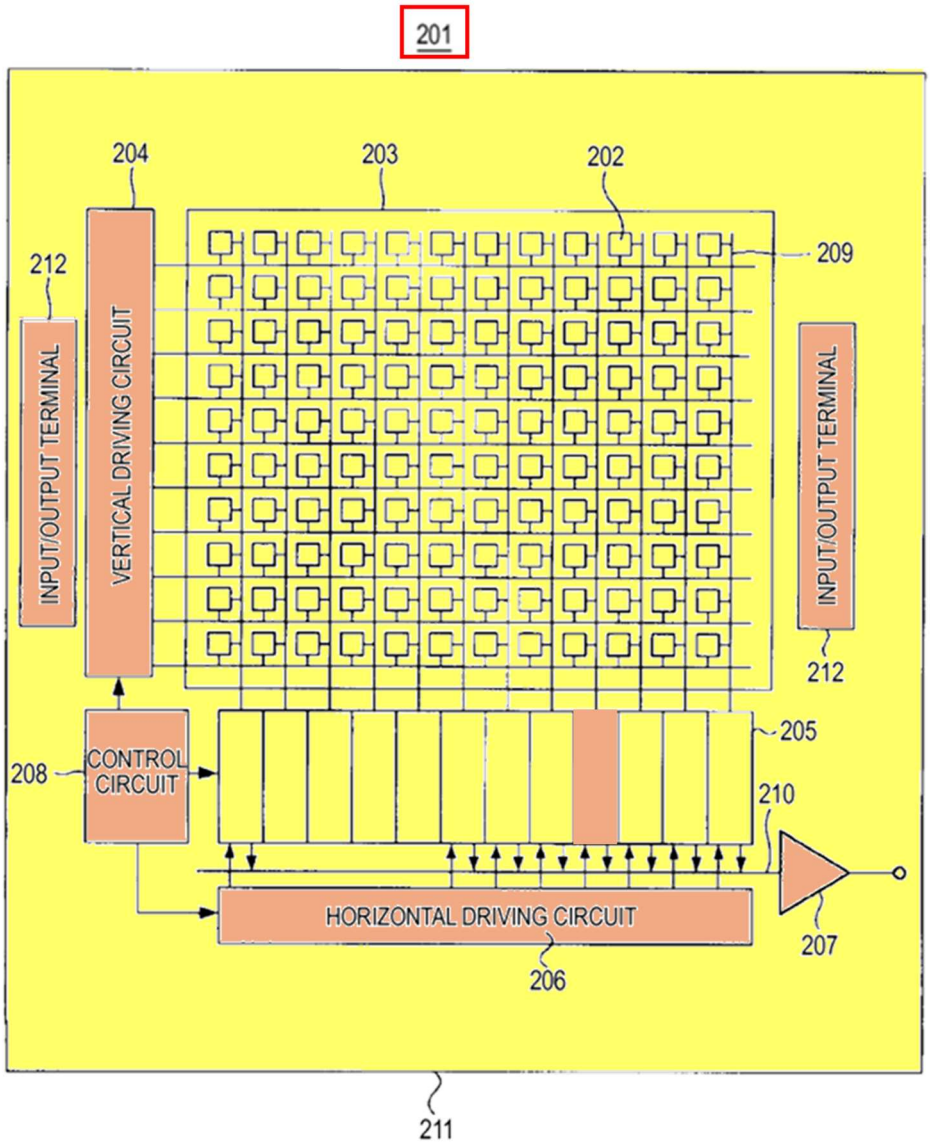
Kuboi, Fig. 15.

101. Vertical driving circuit 204 supplies pulses for activating the pixels in a selected row and channels pixel signals from each pixel to a corresponding column signal processing circuit 205, which performs signal processing tasks such as, e.g., signal amplification. *Kuboi*, ¶¶[51]-[52]. Horizontal driving circuit 206 sequentially selects a column signal processing circuit 205 and routes the

processed pixel signals from that circuit 205 to output circuit 207, which further processes the received signals and outputs the processed signals. *Kuboi*, ¶¶[53]-[54]. Meanwhile, control circuit 208 controls the other circuits of the peripheral circuit portion. *Kuboi*, ¶[50].

102. Each of these CMOS "logic[] circuits" of the peripheral circuit portion includes active components such as transistors, which activate circuits and amplify signals, thereby making them an active electronic circuit. *Kuboi*, ¶[49]. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. Ex. 1019, 4 ("Complementary MOS (CMOS) refers to a complementary *p*-channel and *n*-channel MOSFET pair."); Ex. 1017, 6 (describing amplifiers and logic circuits as "active circuits"), 7, 9 (describing transistors as the most important example of an "'active' component[]"), 8 (describing circuits with transistors as "active circuits"); Ex. 1019, 4 (describing logic circuits as including transistors); Ex. 1018, 4, 5; *see* Ex. 1026, 4. Thus, the logic circuits (vertical driving circuit 204, a column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208) of *Kuboi*'s peripheral circuit portion that process the signals from a pixel (pixel 11) and output it are the claimed active electronic circuit. The active electronic circuit is highlighted in the figure of imaging device 201 below.

FIG.15



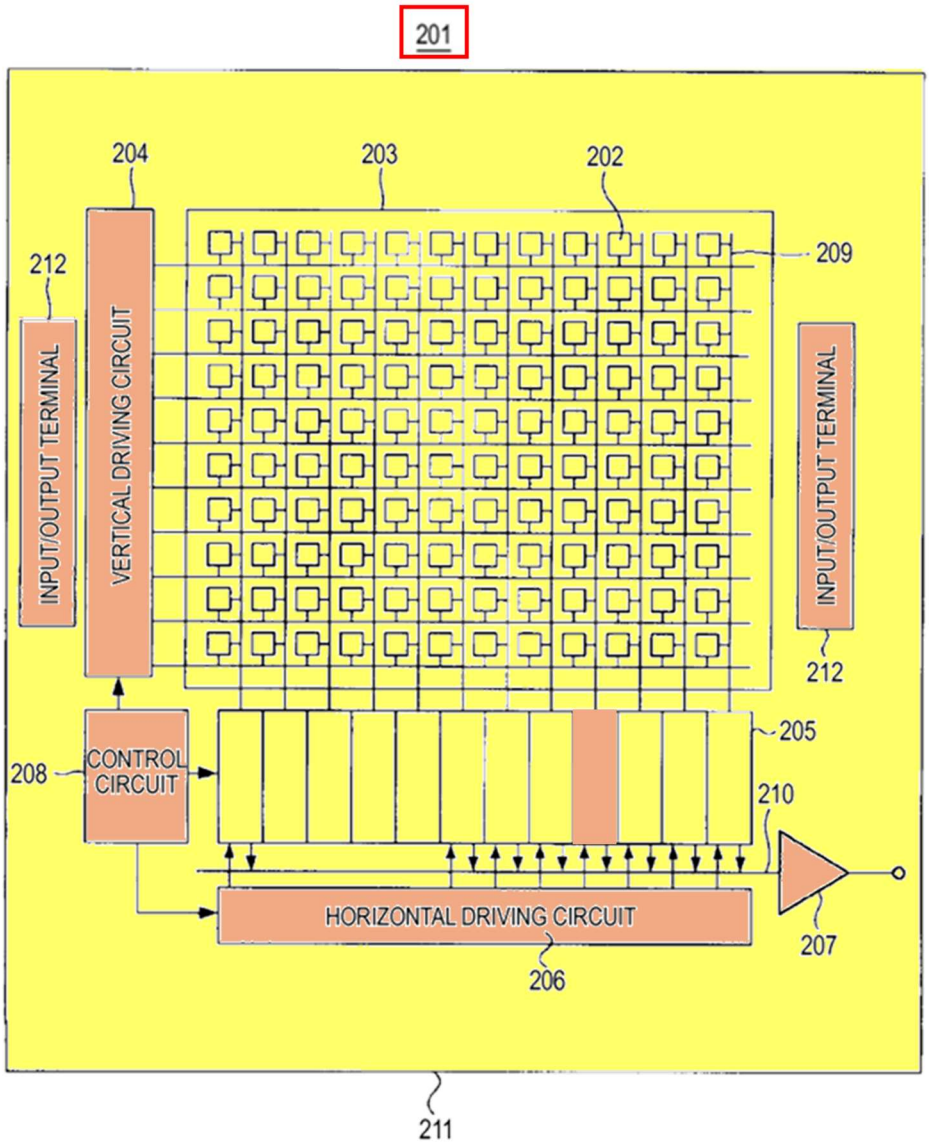
Kuboi, Fig. 15 (identifying an active electronic circuit).

b. [1pre(b)]: "both formed on or in a single substrate"

103. In my opinion, to the extent the preamble is limiting, *Kuboi* discloses this portion of it because imaging device 201's photoelectric conversion portions 14 and active electronic circuit are both formed on or in a single substrate.

104. In *Kuboi*'s imaging device 201, pixels 11 (including photoelectric conversion portions 14) and the peripheral circuit portion (which includes an active electronic circuit) "are provided on … semiconductor substrate 211." *Kuboi*, ¶¶[48], [78]-[79]; *see Kuboi*, Fig. 15. As shown below, the pixel region (including pixels 11) and the peripheral circuit portion (including vertical driving circuit 204, all column signal processing circuits 205, horizontal driving circuit 206, output circuit 207, and control circuit 208) "are provided on a semiconductor substrate 211." *Kuboi*, ¶¶[48]-[49].

FIG.15



Kuboi, Fig. 15.

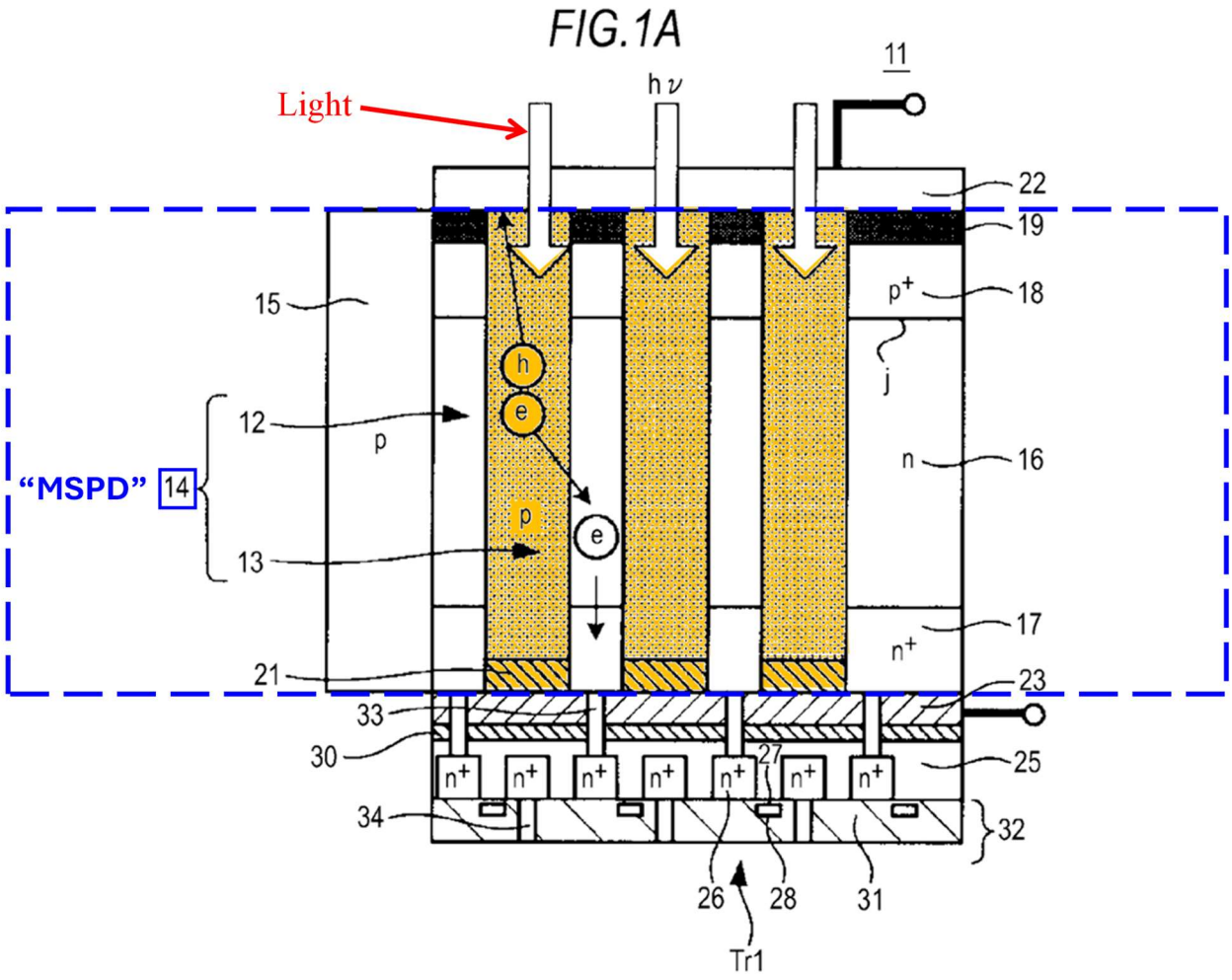
105. Indeed, consistent with the above figure's disclosure of a single substrate, *Kuboi* outlines a method for fabricating the imaging device in which the "pixel and logical circuit portion … [are] created in advance" and bonded to another substrate on which the pixel transistors are formed. *Kuboi*, ¶[78]. *Kuboi*'s disclosure, including Figure 15 and its method of fabrication, show that the pixels

(including microstructure-enhanced photodetectors) and the peripheral circuit portion (which includes the active electronic circuit, *supra*) are formed on a single substrate, substrate 211.

c. [1pre(c)]: "and configured to receive an optical input that in cross-section is substantially continuous spatially, convert the optical input to an electrical output, and process the electrical output into a processed output, wherein:"

106. In my opinion, to the extent the preamble is limiting, *Kuboi* discloses and renders obvious this portion of it because imaging device 201 and pixels 11 are configured to receive light (hγ) (the "optical input") that is substantially continuous in cross-section spatially, convert the received light to electrical charges, and process these electrical charges into a processed output.

107. Pixel 11 includes an on-chip microlens (not shown in the drawings) formed on transparent upper electrode 22. *Kuboi*, ¶¶[63]-[64]. A color filter is disposed between upper electrode 22 and the on-chip microlens. *Kuboi*, ¶¶[63]-[64], [90], Figs. 6A-6B. As illustrated below, light that passes through the on-chip microlens and the color filter passes through transparent upper electrode 22 and enters photoelectric conversion film 13 of photoelectric conversion portion 14 for photoelectric conversion. *Kuboi*, ¶¶[63]-[64], Fig. 1A.



Kuboi, Fig. 1A.

108. A person of ordinary skill would understand that light passing through upper electrode 22 after passing through a color filter will have the same color (or wavelength) as the color filter. *Kuboi*, ¶¶[63]-[64], [90], Figs. 6A-6B. As an example, if a red filter is used, the wavelength of incident light will be about 650 nm; if a green filter is used, the wavelength will be about 540 nm, and so on. *See Kuboi*, ¶¶[6], [90]. Thus, the wavelength of light received by photoelectric

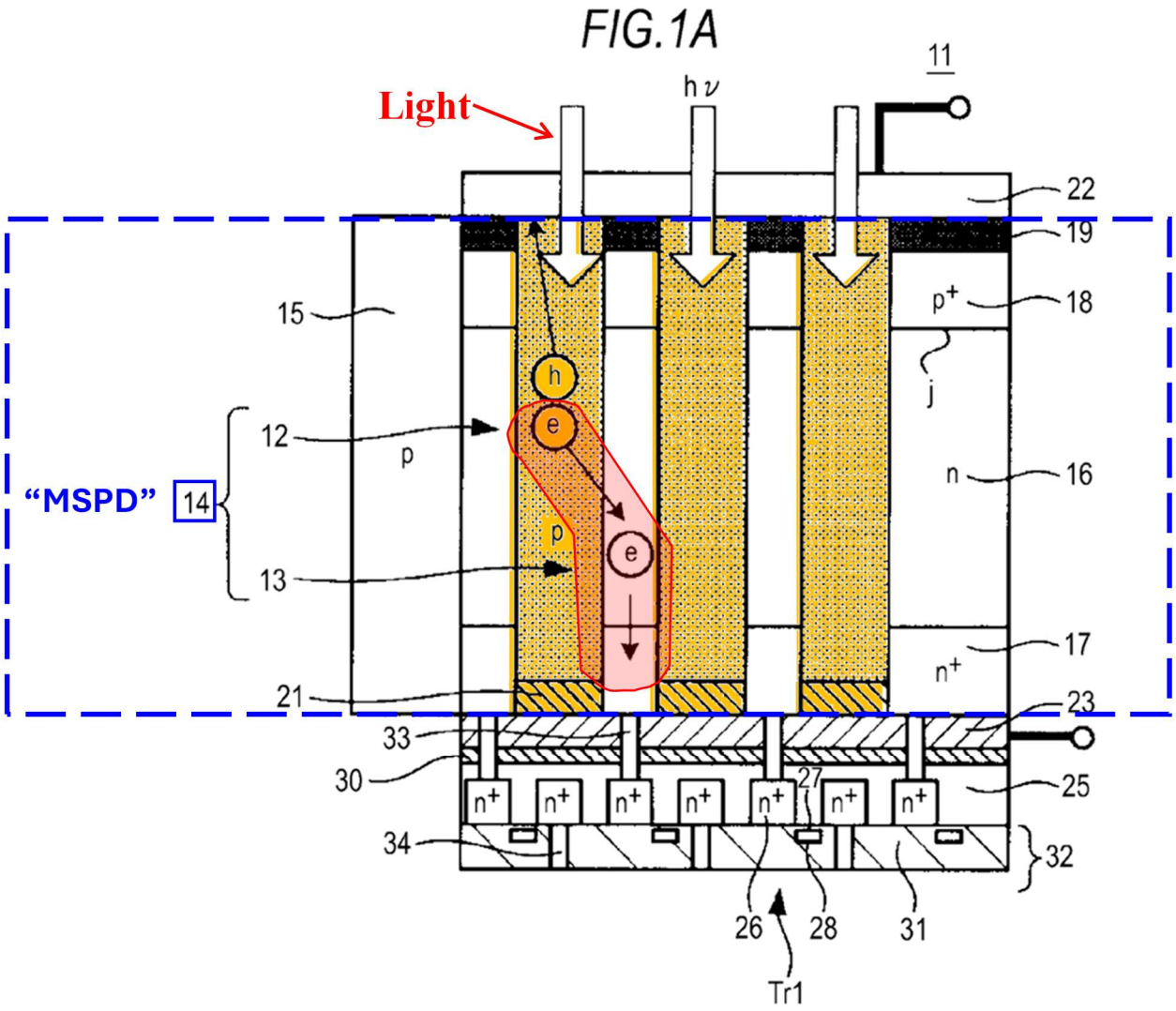
conversion portion 14 is "substantially continuous spatially" in cross-section, as claimed. *See Kuboi*, Fig. 1A. Moreover, based on the structure of pixel 11, a person of ordinary skill would have understood that light is uniformly received across the surface of the photoelectric conversion portion 14 beneath upper electrode 22, rather than being limited to specific locations. In addition, based at least on the size of the arrows that illustrate incident light on the pixels, a person of ordinary skill would have recognized that the magnitude of the light received by photoelectric conversion portions 14 is substantially continuous spatially in cross-section. *See Kuboi*, Figs. 1A, 3, 5A, 6A, 8A, 9, 10A, 13.

109. To the extent that *Kuboi* does not expressly disclose that light received by pixel 11 is substantially continuous in cross-section, this would have been obvious to a person of ordinary skill based on *Kuboi*. *Kuboi*'s imaging device 201 may be used in an imaging apparatus where light reflected from an object is guided to the pixels (including pixel 11) to capture an image of the object. *Kuboi*, ¶¶[48], [191]-[192], Fig. 16. A person of ordinary skill would have understood that each pixel receiving light that is substantially uniform in cross-section would assist in preserving the integrity of color reproduction and would enable the image sensor to produce sharper and more vivid images with reduced distortions. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. Ex. 1015, 4-6 (discussing the impact of color

variations and illumination levels on the pixels of an image sensor on the resulting image).

110. A person of ordinary skill would thus have been motivated to configure imaging device 201 such that the light received by pixel 11 is substantially uniform in cross-section, ensuring that the images produced by imaging device 201 are sharp and vivid. For example, a person of ordinary skill would have recognized that an optical system that guides light to the pixels can be configured such that the light received by pixel 11 is substantially uniform in cross-section. Given that this is a well-understood image sensor feature, the results would have been entirely predictable and a person of ordinary skill would have had a reasonable expectation of success in carrying out this modification.

111. Photoelectric conversion portion 14 converts the received light into electrical charges ("convert the optical input to an electrical output") and outputs it. As shown below, light that enters photoelectric conversion films 13 undergoes photoelectric conversion and generates electron-hole pairs. *Kuboi*, ¶[64].



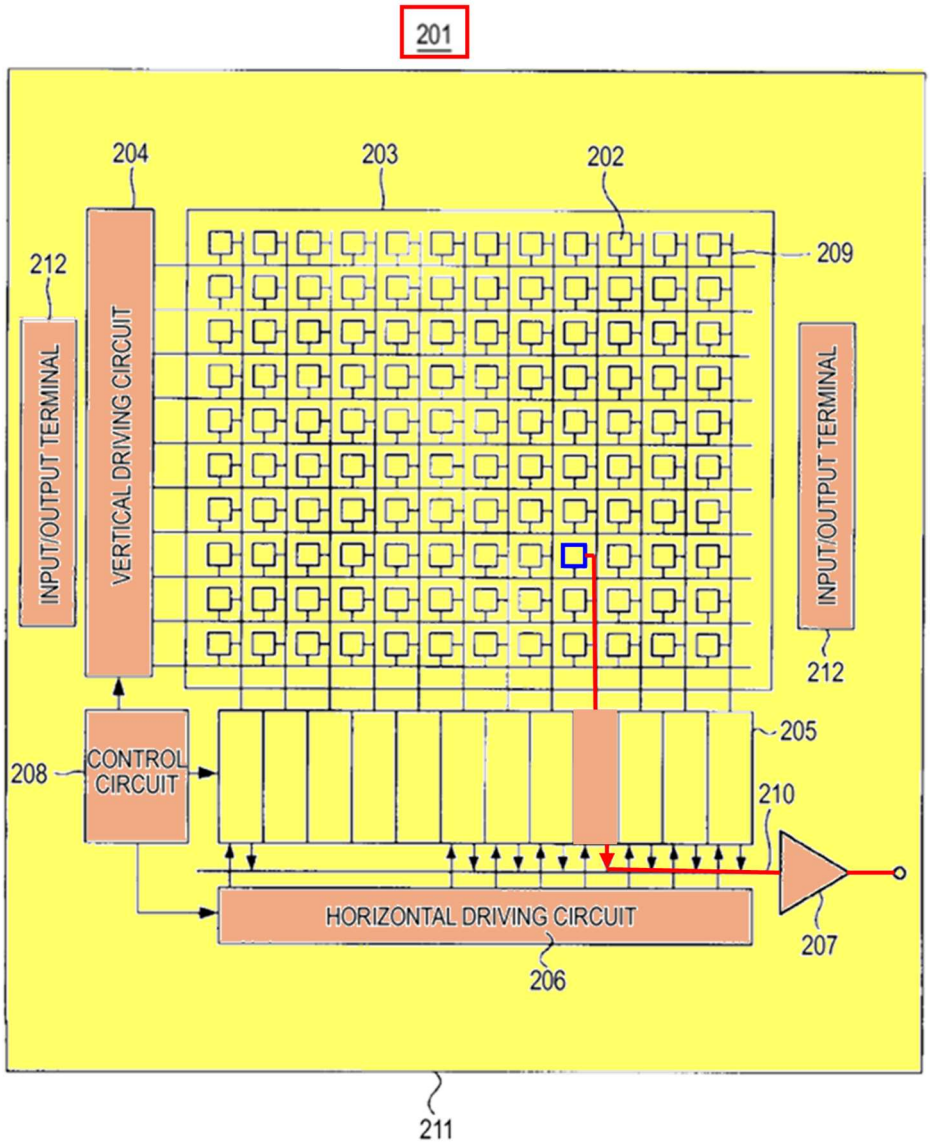
Kuboi, Fig. 1A.

112. The highlighted arrows above show how the separated electrons (e), which serve as signal charges, move from photoelectric conversion films 13 through the interface and semiconductor layer 12, and are output from photoelectric conversion portion 14 to a charge accumulation region 26 of the pixel transistors via conductors 33. *Kuboi*, ¶¶[61], [62], [64], Fig. 1A. Meanwhile, the holes (h) are discharged through upper electrode 22. *Kuboi*, ¶[64]. The signal

charges that are generated based on the amount of light received by photoelectric conversion portion 14 are pixel 11's electrical output. *Kuboi*, ¶¶[51], [62]-[64].

113. The peripheral circuit portion's logic circuits (that include vertical driving circuit 204, multiple column signal processing circuits 205, horizontal driving circuit 206, output circuit 207, and control circuit 208) process pixel 11's electrical output into a processed output. As indicated by the annotated red line below, vertical driving circuit 204 transfers the accumulated electrical output (via signal line 209) to the corresponding column signal processing circuit 205. *Kuboi*, ¶¶[51]-[52].

FIG.15

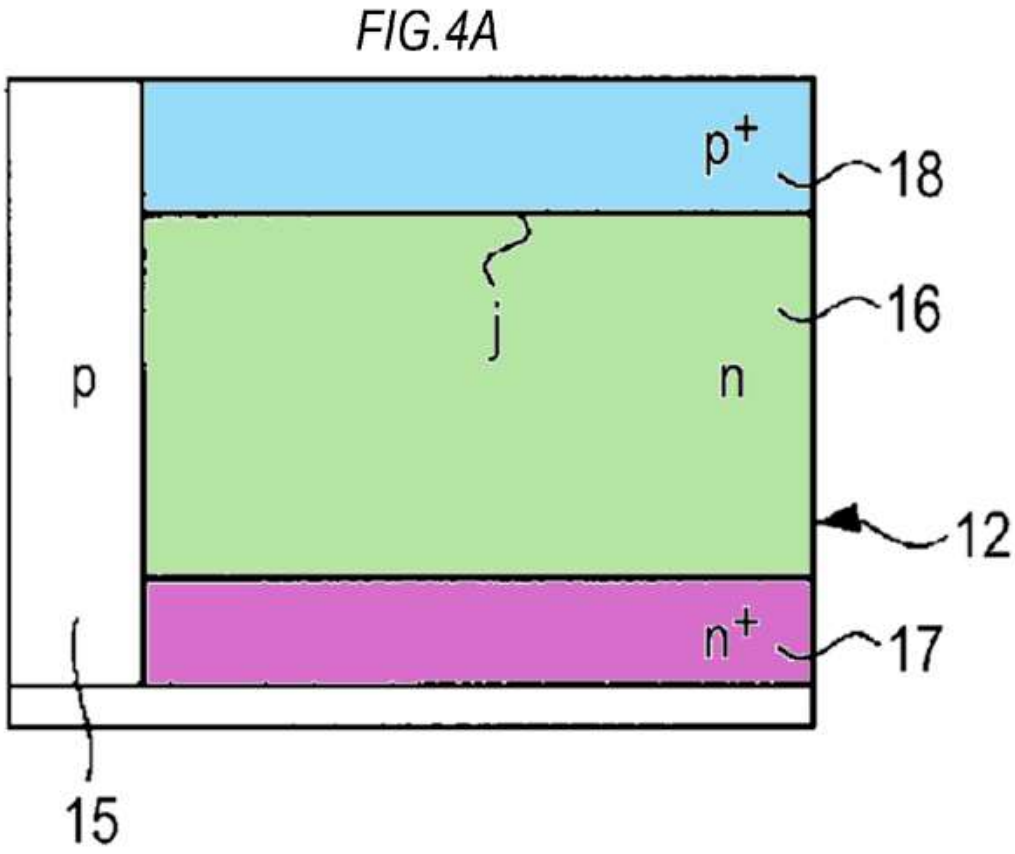


Kuboi, Fig. 15.

114. This circuit performs signal processing tasks such as signal amplification and then outputs the amplified signals (via signal line 210) to output circuit 207, which conducts further signal processing and outputs the processed signals. *Kuboi*, ¶¶[52]-[54]; *infra* XI.A.1.m (claim [1j]), XI.A.1.n (claim [1k]).

d. [1a]: "the MSPD on or in said single substrate comprises an intermediate region, a first region at one side of the intermediate region, and a second region at an opposite side of the intermediate region, wherein:"

115. In my opinion, *Kuboi* discloses this limitation because semiconductor layer 12 of photoelectric conversion portion 14 ("MSPD") comprises an n-type region 16 ("intermediate region"), a p^+-type region 18 ("first region") on one side of the n-type region 16, and an n^+-type region 17 ("second region") on the opposite side of the n-type region 16. *Kuboi*, ¶¶[55]-[56], [71], Figs. 3, 4A. These layers are illustrated below:



Kuboi, Fig. 4A.

116. Silicon semiconductor layer 12 is implanted with impurities to form an "n^+-type semiconductor region 17 (corresponding to the front surface side), a n-type semiconductor region 16 (corresponding to an intermediate region), and a p^+-type semiconductor region [18] (corresponding to the rear surface side) … in that order from the lower region of the drawing [of Figure 4A] in a region corresponding to one pixel." *Kuboi*, ¶¶[55]-[56], [71].

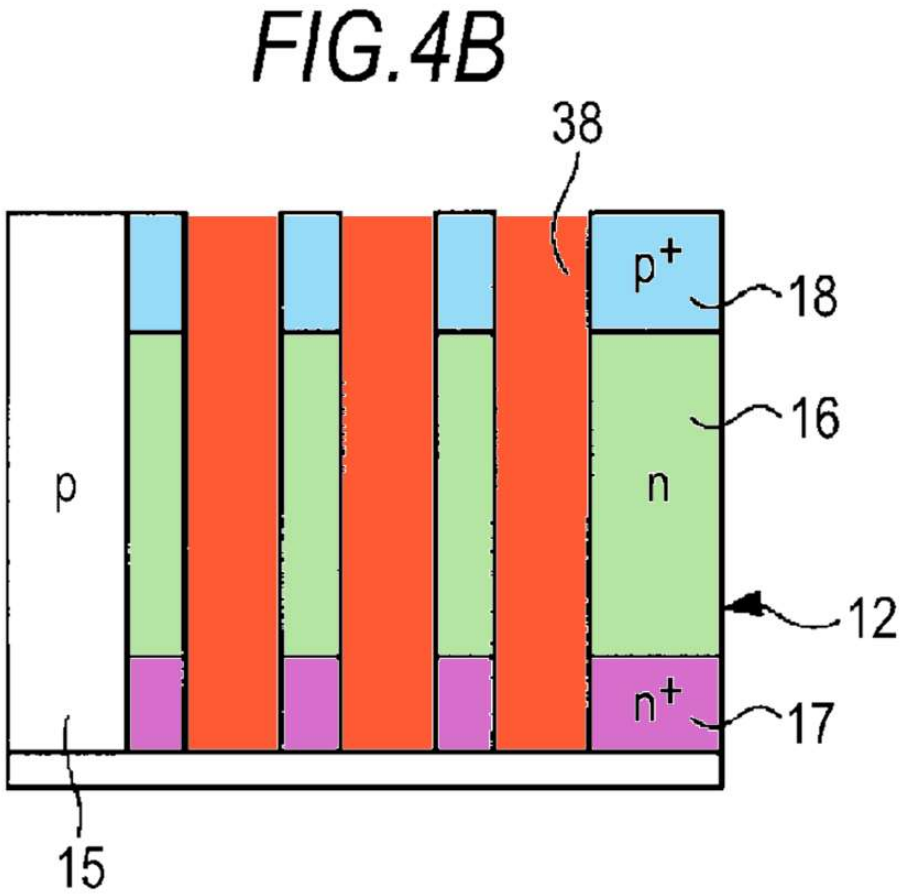
117. As discussed for claim [1pre(b)], photoelectric conversion portion 14 ("MSPD") (including semiconductor layer 12 and the layers discussed above) is formed on substrate 211 (the "single substrate"). *Supra* XI.A.1.b.

e. [1b]: "each of the regions comprises Silicon, Germanium, or an alloy thereof;"

118. In my opinion, *Kuboi* discloses this limitation because n^+-type semiconductor region 17 ("second region"), n-type semiconductor region 16 ("intermediate region"), and p^+-type semiconductor region 18 ("first region") are each formed by implanting the "semiconductor layer 12 formed of silicon" with impurities. *Kuboi*, ¶¶[55]-[56], [71]. Since these regions are created by implanting impurities into silicon, each region will comprise silicon. *Kuboi*, ¶[3] ("an impurity-implanted crystalline silicon layer"); *see also Kuboi*, ¶¶[6], [66], [110]-[111].

f. [1c]: "at least one of said regions, and an optional overlying covering region, have holes intentionally formed therein"

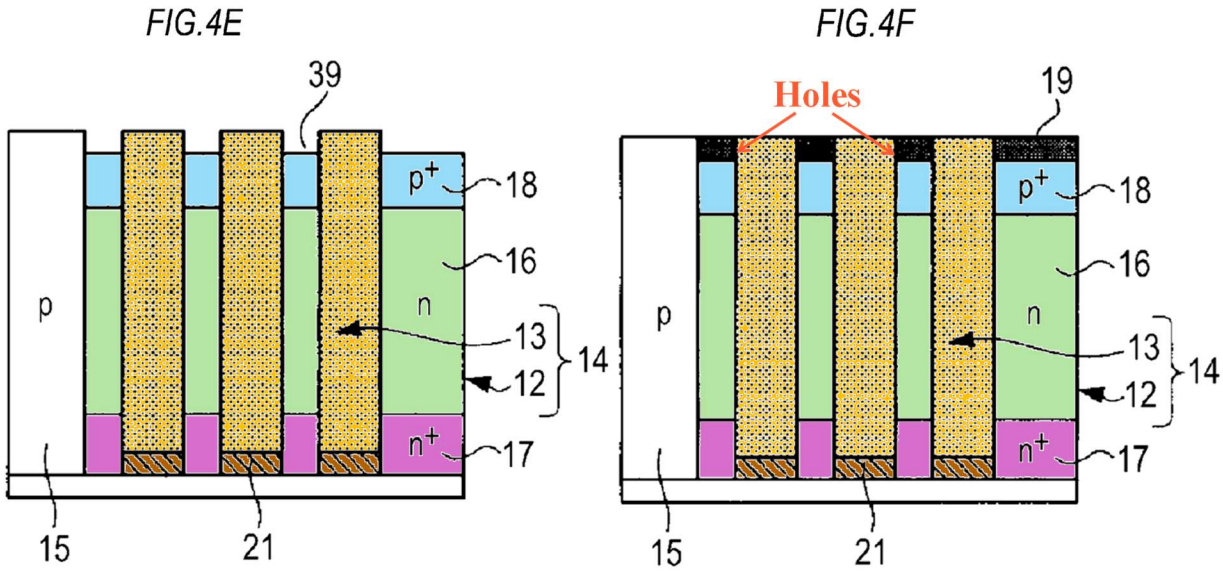
119. In my opinion, *Kuboi* discloses this limitation because *Kuboi*'s multiple vertical holes 38 ("holes intentionally formed") are dry-etched through the three regions of pixel 11's semiconductor layer 12: n^+-type region 17, n-type region 16, and p^+-type region 18. *Kuboi*, ¶¶[71]-[72], Fig. 4B. These holes 38 are shown below:



Kuboi, Fig. 4B.

120. After regions 16, 17, and 18 are formed on semiconductor layer 12, "vertical hole[s] 38" "extending from the p^+-type … region 18 to the n^+-type … region [17] [are] formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching." *Kuboi*, ¶¶[71]-[72]. These holes can be cylindrically shaped or may extend into the page to form a stripe shape in a plan view. *Kuboi*, ¶[57]; *see Kuboi*, Fig. 1B.

121. A light shielding film 19 ("an overlying covering layer"), which is formed on (and overlies) the light incident surface of p^+-type region 18, also contains holes that align with the holes in the underlying PiN regions. *Kuboi*, ¶¶[76], [91], Fig. 1A.



Kuboi, Figs. 4E, 4F.

122. After depositing photoelectric conversion films 13 into the holes 38 formed through regions 16, 17, and 18, the surfaces of films 13 are covered using a resist mask (not shown). *Kuboi*, ¶¶[73]-[75]. The exposed surface of p^+-type region 18 is then etched back, causing the embedded films 13 to protrude from the surface of p^+-type region 18. *Kuboi*, ¶[75], Fig. 4E. Then, a light shielding film 19 is applied on the etched surface of p^+-type region 18 around protruding films 13 so that incident light only enters exposed films 13 (and not p^+-type region 18). *Kuboi*, ¶¶[[59], [76]. Applying light shielding film 19 around protruding films 13 results in holes being formed in light shielding film 19 around films 13.

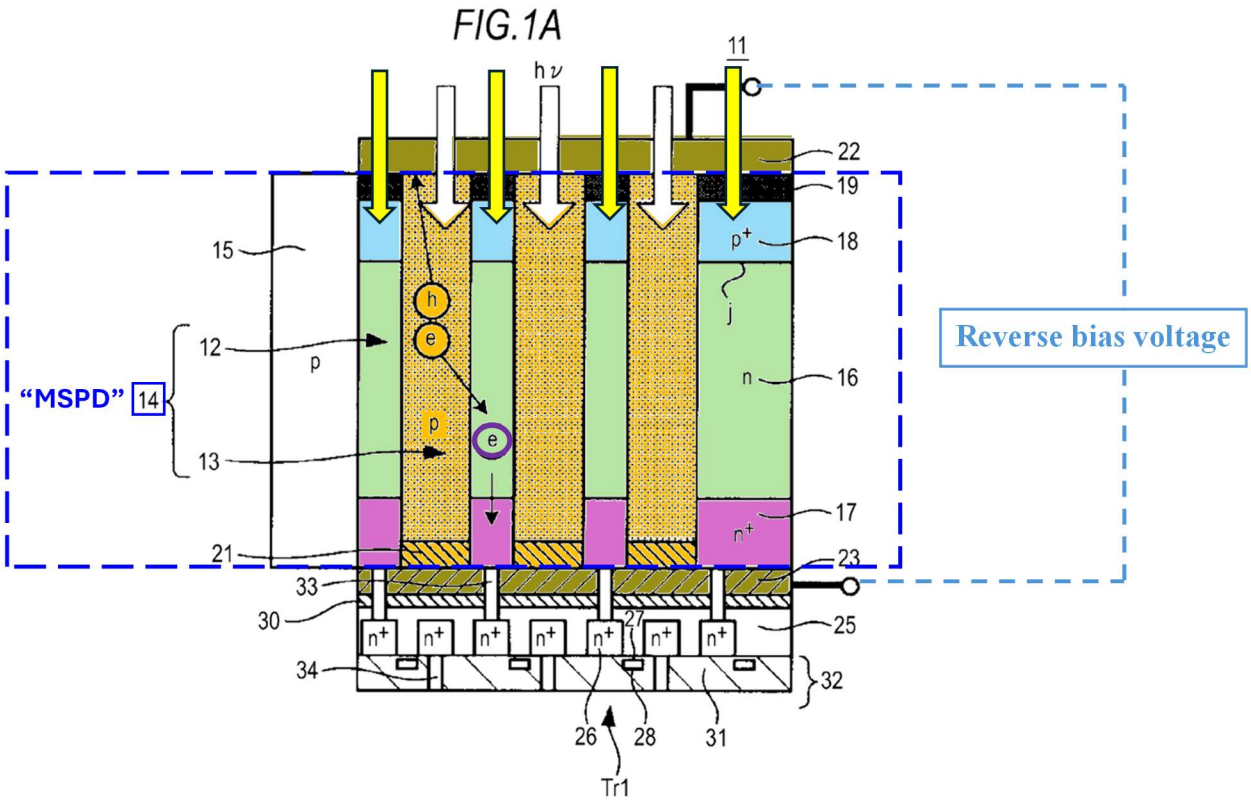
123. *Kuboi* discloses that vertical holes 38 extending through the PiN regions may be dry-etched "using a CCP (Capacitive Coupled Plasma) etching apparatus" or other apparatuses. *Kuboi*, ¶¶[72], [95]. Therefore, a person of ordinary skill would have understood that these holes 38 are intentionally created. Since the holes in the overlying light shielding film 19 are formed by etching back the p^+-type region 18 around the films 13 and forming light shielding film 19 around the protruding films 13, holes in the light shielding film 19 are also intentionally created. *Kuboi*, ¶¶[72], [75]-[76]. Furthermore, since the holes extend perpendicularly through the PiN regions, they extend transversely through these regions. *Kuboi*, ¶¶[72], [75]-[76], Figs. 1A, 4A-4F.

124. The adjective "optional" in the term "overlying covering layer" was introduced during prosecution to clarify that the overlying covering layer is not a mandatory feature and may or may not be included. Ex. 1044, 124-25, 136. Originally, the claim stated: "overlying covering region that may be present," resembling the language used in its direct predecessor, the '700 Patent. Ex. 1044, 632; '700 Patent, 118:39-40; *Supra* VII.B. During prosecution of the '700 Patent, the Examiner clarified that the phrase "overlying covering region that may be present" does not mandate the presence of the overlying layer but instead "merely states the overlying layer as an optional component." Ex. 1003, 387; *supra* VII.B. Later, during prosecution of the '543 Patent, the same Examiner recommended modifying this language to explicitly state "optional overlying covering region" to address potential §112 enablement concerns with the original phrasing. Ex. 1044, 124-125; *supra* VII.B. Accordingly, based on the Examiner's suggestion, "overlying covering region that may be present" was amended to "***optional*** overlying covering region." Ex. 1044, 136 (emphasis added); *supra* VII.B.

125. Consistent with this interpretation, the '543 Patent employs the term "optional" to denote nonmandatory features that might or might not be present on the device. '543 Patent, 41:16-19, 41:59-61, 42:47-55, 44:14-22, 75:30-32. Therefore, in my opinion, an "overlying covering region" is not required to satisfy this claim limitation. *Infra* VII.B. Despite this, *Kuboi* satisfies this limitation, as its

light shielding film 19 qualifies as an "overlying covering region" with deliberately created holes for the reasons discussed above.

126. Indeed, a person of ordinary skill would have understood that photoelectric conversion portion 14 ("MSPD") generates electrons (charge) through photoelectric conversion of light regardless of whether light shielding film 19 is present, so light shielding film 19 is "optional" in the same way that the overlying covering layer is optional in the '543 Patent. When light shielding film 19 covers the surface of semiconductor layer 12, light exclusively enters photoelectric conversion film 13, and as a result, photoelectric conversion occurs solely within film 13. *See Kuboi*, ¶¶[59], [64]. A person of ordinary skill would understand that, in the absence of light shielding film 19, light would enter both film 13 and semiconductor layer 12, leading to photoelectric conversion occurring in layer 12 and film 13. *See Kuboi*, ¶¶[91]-[92].

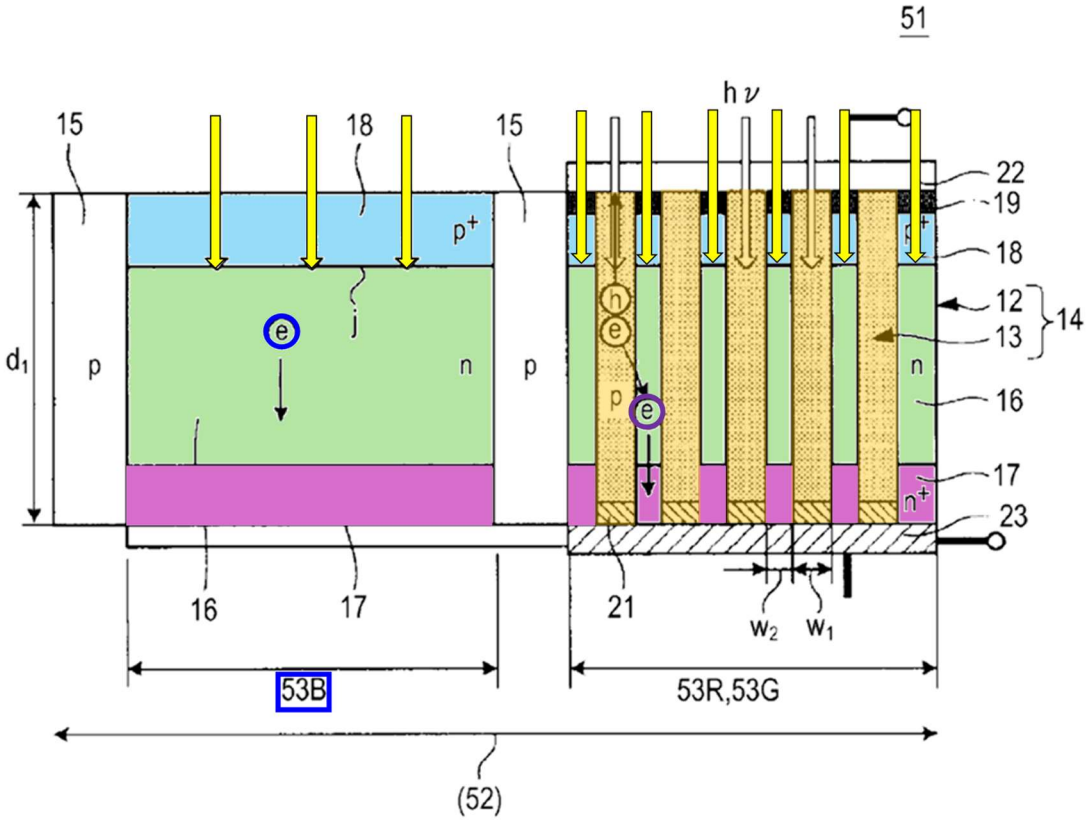


Kuboi, Fig. 1A.

127. In the absence of light shielding film 19, light would still enter the photoelectric conversion film 13, generating electrons ("e") just as it does when film 19 is present. *See Kuboi*, ¶[64]. A person of ordinary skill would understand that without film 19, light would also enter semiconductor layer 12, where photoelectric conversion would occur, producing electrons ("e") in a manner similar to electron generation in photoelectric conversion portion 53B, as depicted in the embodiment of Fig. 6A. *See Kuboi*, ¶¶[90]-[92], Fig. 6A. In my opinion, it would have been obvious to a person of ordinary skill that, if the electrically conductive film 19 is eliminated, the upper electrode 22 will be arranged to contact

the p^+-type region 18 to apply a reverse bias to photoelectric conversion portion 14 ("MSPD").

FIG.6A



Kuboi, Fig. 6A.

128. *Kuboi* discloses that in the embodiment shown in Fig. 6A, the semiconductor layer 12 has a thickness d1 of approximately 1.4 μm. *Kuboi*, ¶[94]. Additionally, *Kuboi* discloses that simulations indicate complete absorption of incident light within the semiconductor layer of a silicon-based photodiode occurs at a silicon film thickness of 1 μm, while a thickness of 3 μm is required to absorb 95% of green and red light. *Kuboi*, ¶[6]. Based on *Kuboi*'s disclosure, it is my

opinion that a person skilled in the art would recognize that, if film 19 is eliminated, a portion (depending on the color or wavelength of the entering light) of the light entering semiconductor layer 12 would be absorbed to produce electrons ("e"). Additionally, in my opinion, the same portion of light entering photoelectric conversion film 13 would continue to be absorbed and generate electrons ("e"), just as it does when film 19 is present. *See Kuboi*, ¶[64]. In my opinion, a person of ordinary skill would recognize that, without light shielding film 19, both electrons "e" (right) and "e" (left) would contribute to power generation in photoelectric conversion portion 14. A person of ordinary skill in the art would have understood that this approach—where photoelectric conversion of light occurs in both the silicon semiconductor layer and the organic film—is possible, given the existence of known hybrid photodetectors that generate power in a similar manner by integrating an organic film with a silicon photodetector. Ex. 1045, 1-7 (discussing the use of organic films to enhance the ultraviolet sensitivity of silicon photodetectors). Therefore, in my opinion, light shielding film 19 is not essential to the operation of MSPD 14 as it remains functional even in its absence, albeit with a modified performance.

g. [1d]: "each of the first and second regions comprises a doped material;"

129. In my opinion, *Kuboi* discloses this limitation because p^+-type region 18 ("first region") and n^+-type region 17 ("second region") of semiconductor layer

12 are formed by "implant[ing] … impurities" in silicon semiconductor layer 12. *Kuboi*, ¶¶[55]-[56].

130. According to *Kuboi*, "[t]he semiconductor layer 12 [formed of silicon] is implanted with impurities … [to form] a[n] n^+-type … region 17 having higher concentration [of impurities] than the n-type … region 16, and a semiconductor region 18 of second conductivity type (for example, p^+ type) having higher concentration [of impurities] than the n-type … region 16." *Kuboi*, ¶¶[55]-[56]; *see also Kuboi*, ¶¶[7], [111], [151]. A person of ordinary skill would have understood that the process of implanting impurities into silicon material is known as "doping" the silicon material and the result is a "doped material," as claimed. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. Ex. 1018, 3 (defining "doping" as "the process of introducing impurity atoms into pure silicon to change its electrical properties"); Ex. 1019, 23 ("Impurity doping is the introduction of controlled amounts of impurity dopants into semiconductor materials."); Ex. 1020, 4 ("A doped region is simply a section of the silicon into which impurity atoms have been purposely added to alter the electrical properties."); *see* Ex. 1026, 3. Therefore, in my opinion, *Kuboi*'s first and second regions comprise doped silicon.

h. [1e]: "the intermediate region comprises a material that is less doped than at least one of the first and second regions or is undoped, wherein the degree of

doping is the same or different for different positions in the intermediate region;"

131. In my opinion, *Kuboi* discloses this limitation because its n-type region 16 ("intermediate region") comprises silicon that is less doped than both p^+-type region 18 ("first region") and n^+-type region 17 ("second region"). *Kuboi*, ¶[56]. And, in addition, the degree of doping is the same or different at different positions in n-type region 16. *Kuboi*, ¶[56].

132. According to *Kuboi*, "[t]he semiconductor layer 12 [formed of silicon] is implanted with impurities … [to form] a semiconductor region 16 of first conductivity type (for example, n type), a[n] n^+-type semiconductor region 17 having higher concentration [of impurities] than the n-type semiconductor region 16, and a semiconductor region 18 of second conductivity type (for example, p^+ type) having higher concentration [of impurities] than the n-type semiconductor region 16." *Kuboi*, ¶¶[55]-[56]; *see also Kuboi*, ¶¶[7], [111], [151]. As explained for claim [1d], "the process of introducing impurity atoms into pure silicon" is doping the silicon material and results in a "doped material." Ex. 1018, 3; Ex. 1020, 4; *supra* XI.A.1.g. Thus, *Kuboi*'s n-type region 16 comprises doped silicon with a concentration of impurities (or degree of doping) less than that in p^+-type region 18 and n^+-type region 17.

133. *Kuboi* does not expressly describe the degree of doping at different positions in the n-type region 16 ("intermediate region"). However, in my opinion, a person of ordinary skill would have understood that the degree of doping would either be the same or different at different positions in n-type region 16 as no other possibilities exist. In *Kuboi*, the silicon semiconductor layer 12 is "implanted with impurities" in the n-type region 16. *Kuboi*, ¶¶[55]-[56], [71], Fig. 4A. In my opinion, a person of ordinary skill would have understood that "[d]iffusion and ion implantation are the two key methods of impurity doping" in CMOS technology. Ex. 1019, 23. In both methods, the doping concentration varies progressively with depth into the semiconductor. Ex. 1019, 23-24. *Kuboi* employs "ion implantation" for implanting impurities in semiconductor layer 12. *Kuboi*, ¶¶[7], [134].

134. In the ion implantation process, the dopant ions are implanted into the semiconductor by means of an ion beam, and "[t]he doping concentration has a peak distribution inside the semiconductor and the profile of the dopant distribution is determined mainly by the ion mass and the implanted-ion energy." Ex. 1019, 23. Specifically, during ion implantation, dopant ions are propelled to high velocities and embedded into the silicon wafer as shown in the figure below. Ex. 1020, 4. Through collisions with silicon atoms, the ions lose energy and settle within the wafer. Ex. 1020, 4.

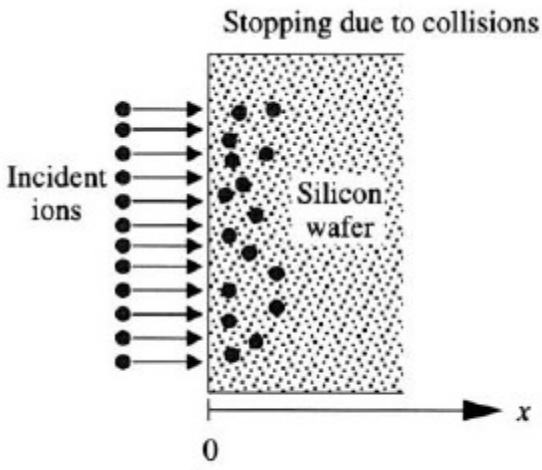


Figure 2.3 The ion stopping process

Ex. 1020, 4.

135. In ion implantation, the dopant concentration varies with wafer depth (*x* in the figure above) and can be approximated by a Gaussian distribution. Ex. 1020, 4. The figure below illustrates the dopant concentration as a function of depth when ion implantation is employed for doping.

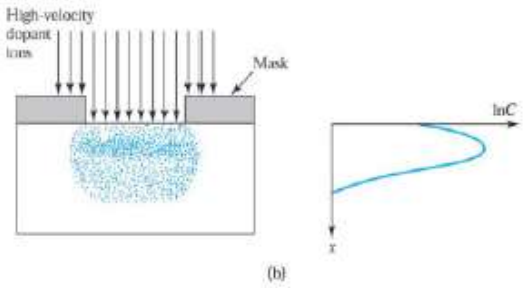


Fig. 1 **Comparison of (*a*) diffusion and (*b*) ion-implantation techniques for selective introduction of dopants into the semiconductor substrate.**

Ex. 1019, 24 (Fig. 1 cropped).

136. The figure above illustrates how dopant concentration varies with depth (*x*) in a semiconductor substrate after ion implantation. Ex. 1019, 23-24.

Based on the figure above, the dopant concentration at the same depth (in a direction perpendicular to *x* in the figure on the right above) would be the same. A similar dopant distribution pattern occurs when an n-type dopant is introduced into *Kuboi*'s silicon semiconductor layer 12 via ion implantation, to form n-type region 16 ("intermediate region"). Typically, arsenic (As) and phosphorus (P) serve as dopants for n-type regions. Ex. 1020, 4 ("Arsenic (As) and phosphorus (P) are used for n-type regions"); Ex. 1019, 24 (explains that "arsenic and phosphorus are used extensively as n-type dopants"). The figure below visually represents the dopant concentration profile as a function of depth when a silicon substrate undergoes implantation with arsenic (As) and phosphorus (P). *See* Ex. 1028, 1.

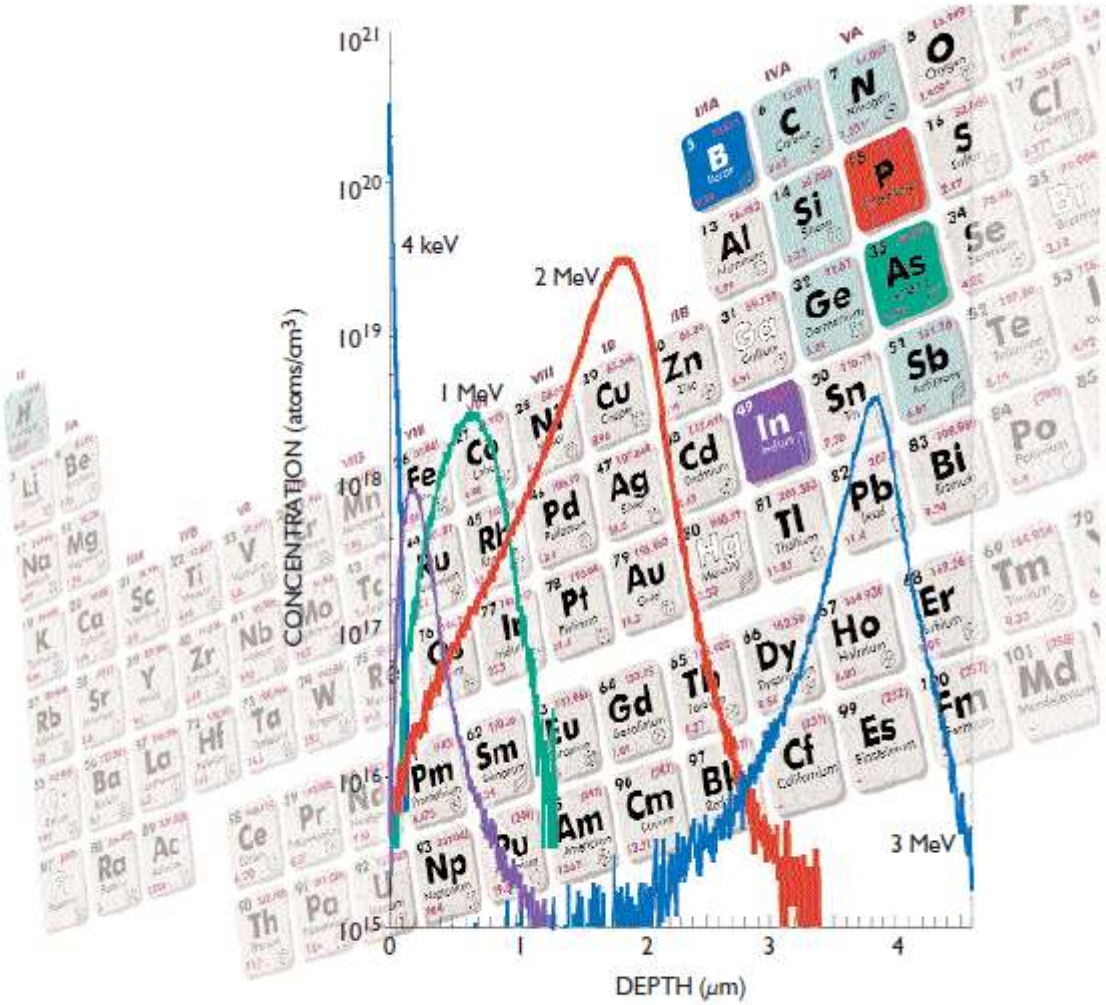
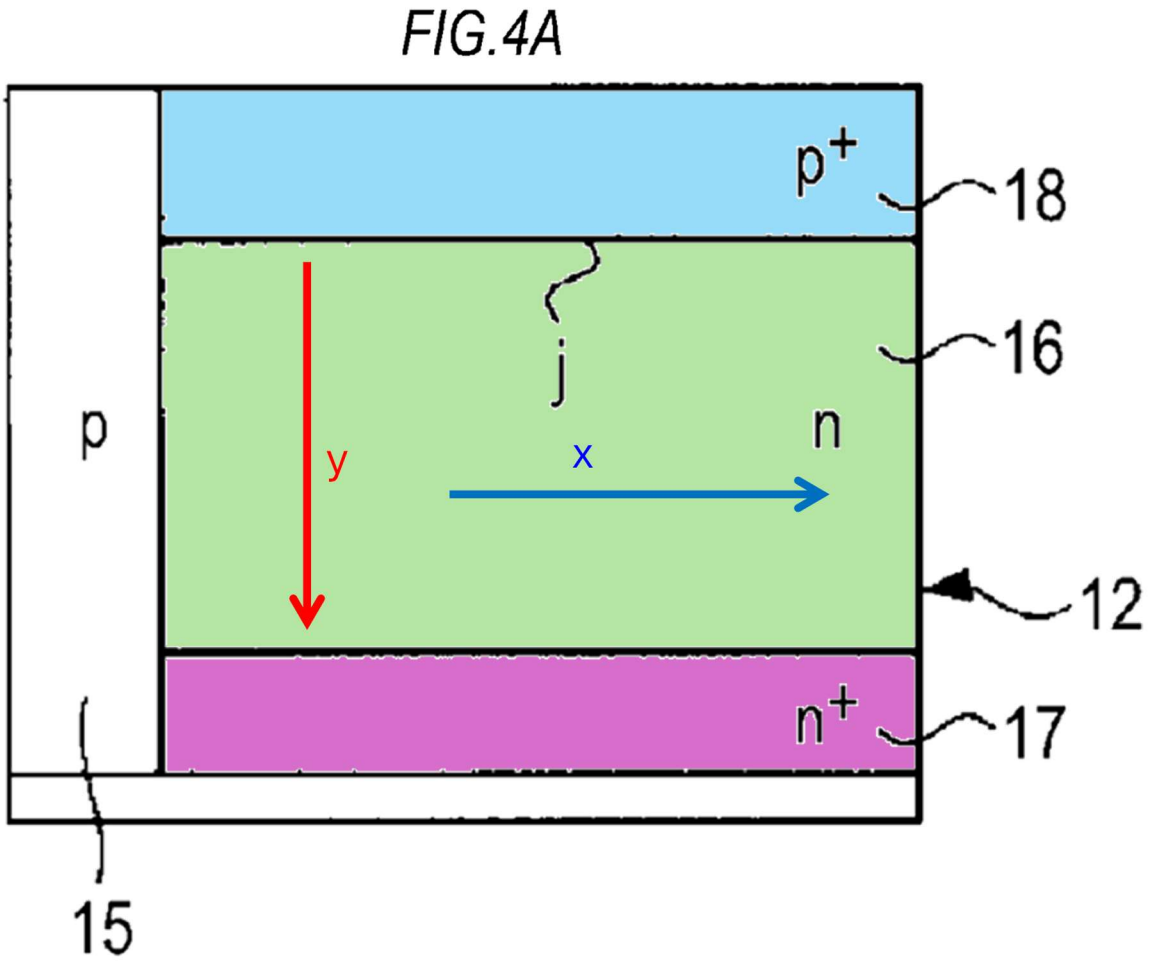


Figure 1. Some of the most commonly implanted species highlighted on the periodic table, along with typical concentration-versus-depth traces for various implant energies.

Ex. 1028, 1.

137. The red curve in the figure above illustrates how the concentration of phosphorus (P) atoms changes with depth when silicon undergoes ion implantation doping. *See* Ex. 1028, 1 (Figure 1). The green curve illustrates that a similar distribution pattern occurs when arsenic (As) is used as the dopant. *See* Ex. 1028, 1 (Figure 1). A person of ordinary skill would understand that the degree of

doping, or the dopant concentration, would vary in a similar manner in *Kuboi*'s n-type region 16 ("intermediate region").



Kuboi, Fig. 4A.

138. In other words, a person of ordinary skill would have understood that the degree of doping will be different at different positions along the depth (along line y in the figure above) of n-type region 16, and the degree of doping will be the same for different positions along the width (along line x in the figure above) of n-type region 16. A person of ordinary skill would have thus recognized that "the

degree of doping is the same or different for different positions" in *Kuboi*'s intermediate region as claimed.

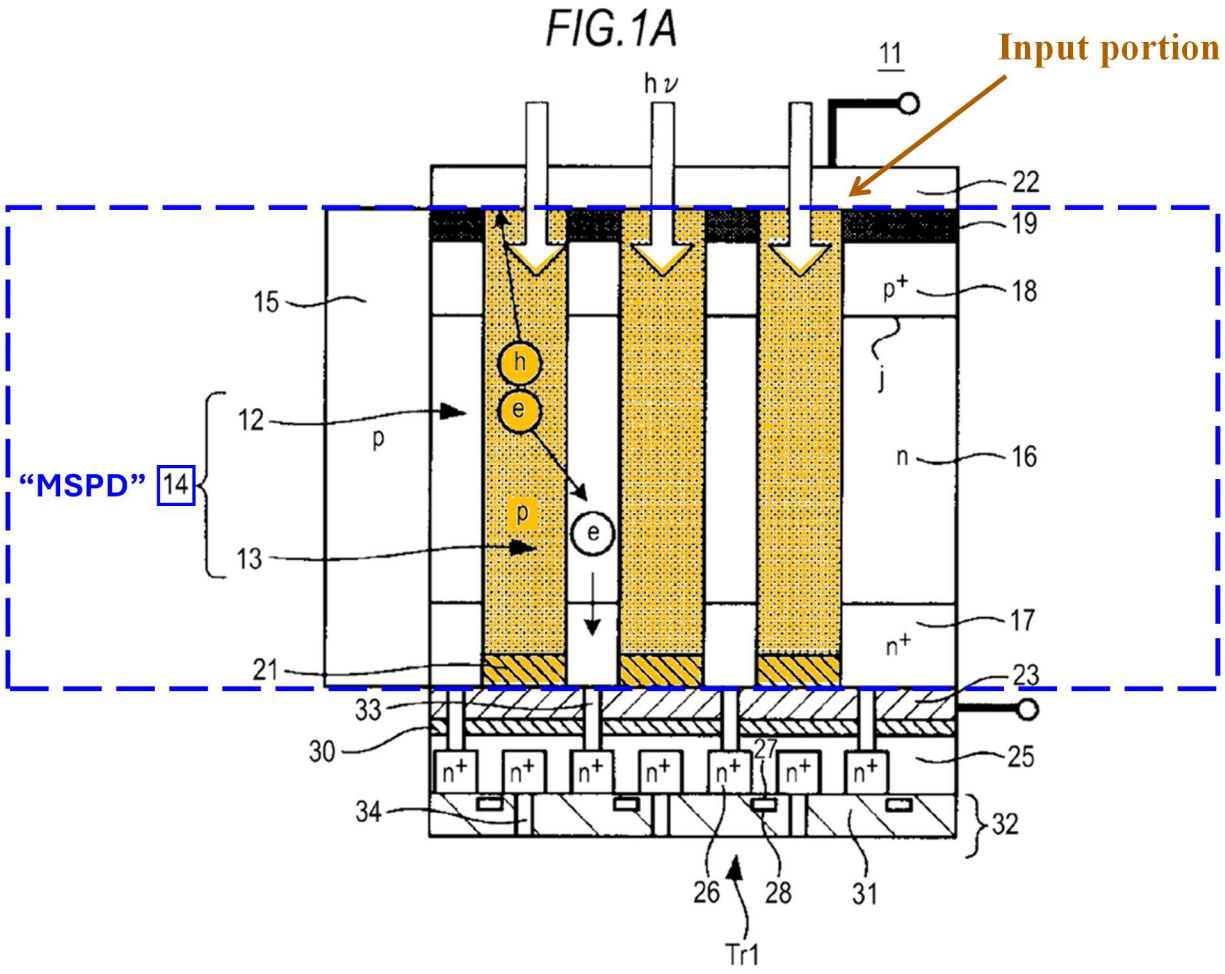
i. [1f]: "an input portion configured to concurrently receive at a plurality of said holes said optical input that has said substantially continuous cross-section; and "

139. In my opinion, *Kuboi* discloses and renders obvious this limitation because, as explained for claim [1pre(c)], light ("optical input") that passes through transparent upper electrode 22 of pixel 11 is substantially continuous in cross-section (or this would have been obvious), *supra* XI.A.1.c, and since light enters photoelectric conversion films 13 (extending through holes in semiconductor layer 12) through upper electrode 22, the holes are configured to concurrently receive light having substantially continuous cross-section.

140. *Kuboi* discloses that pixel 11 includes an on-chip microlens (not shown in the drawings) formed on transparent upper electrode 22 with a color filter therebetween. *Kuboi*, ¶¶[63]-[64], [90]. Light from the on-chip microlens passes through the color filter and upper electrode 22 and enters photoelectric conversion film 13 exposed through the light shielding film 19 of photoelectric conversion portion 14. *Kuboi*, ¶¶[63]-[64], Fig. 1A; *supra* XI.A.1.c (claim [1pre(c)]), XI.A.1.f (claim [1c]). According to *Kuboi*, the plurality of organic photoelectric conversion films 13 may be formed in a cylindrical hollow shape or a stripe shape as viewed

from the upper surface of photoelectric conversion portion 14. *Kuboi*, ¶[57], Fig. 1B.

141. As shown below, the upper surface of photoelectric conversion portion 14 (where films 13 are exposed through light shielding film 19) serves as an "input portion" through which light enters photoelectric conversion portion 14.



Kuboi, Fig. 1A.

142. As explained for claim [1c], photoelectric conversion films 13 are embedded in holes that extend vertically through the PiN regions of photoelectric

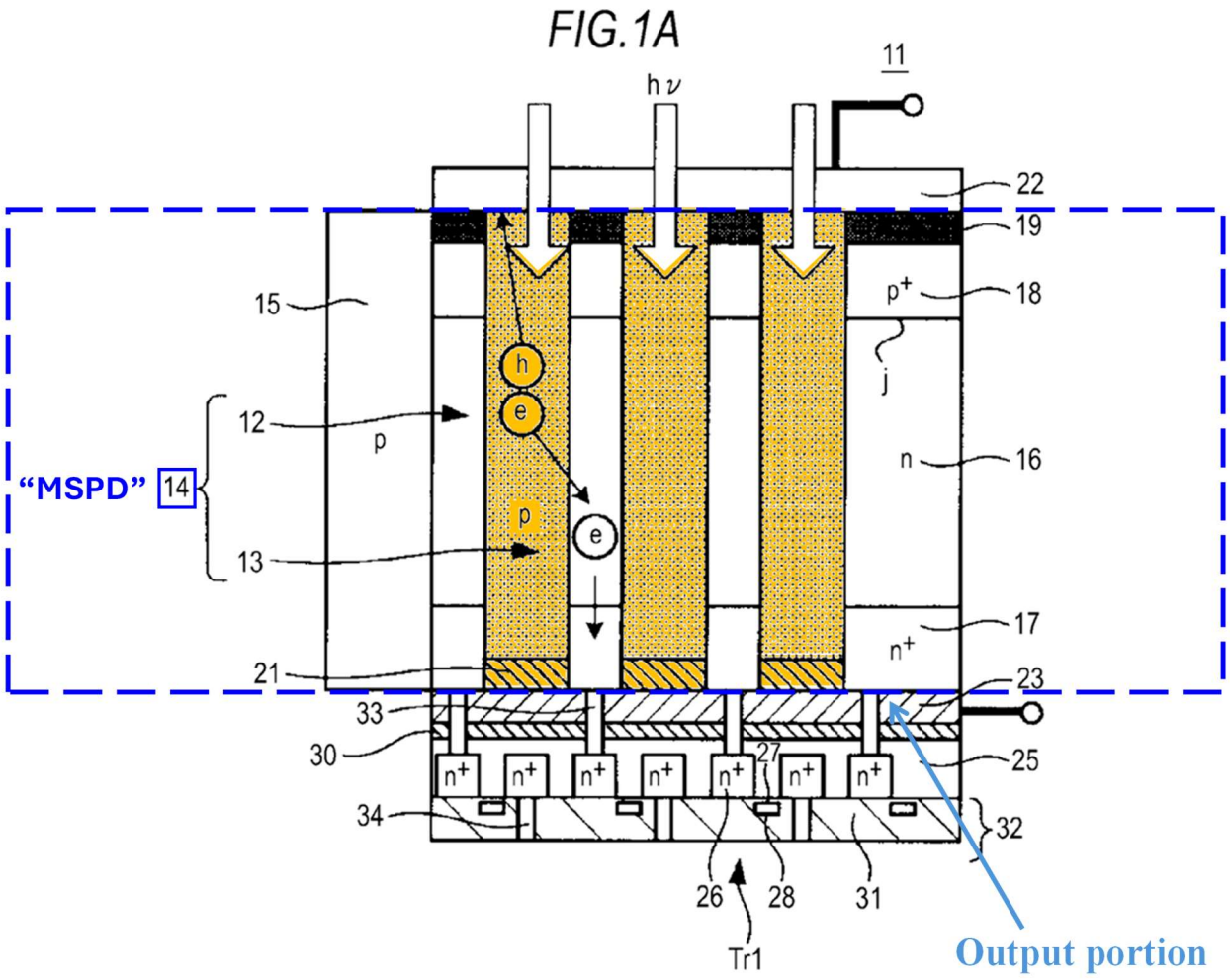
conversion portion 14. *Supra* XI.A.1.f. Thus, photoelectric conversion portion 14 has an input portion that is configured to receive, at a plurality of holes, light having a substantially continuous cross-section.

143. A person of ordinary skill would have recognized that all photoelectric conversion films 13 exposed at the input portion would receive light concurrently. *Kuboi* discloses that its imaging device may be used in a camera where an optical system guides incident light (e.g., light reflected from an object) to the pixel portion of the imaging device. *Kuboi*, ¶¶[191]-[192], Fig. 16. A person of ordinary skill would have understood that pixel 11 (including films 13 exposed at the input portion) receives the light reflected from the object concurrently so that the image of the object can be accurately recorded.

j. [1g]: "an output portion configured to provide said electrical output from the MSPD;"

144. In my opinion, *Kuboi* discloses this limitation because the electric charge carriers generated from the photoelectric conversion of light in photoelectric conversion films 13 are output through multiple conductors 33 exposed at the lower surface of the photoelectric conversion portion 14. *Kuboi*, ¶¶[62], [64], Fig. 1A. The lower surface functions as an "output portion," providing electrical output from photoelectric conversion portion 14.

145. *Kuboi* discloses that incident light that enters films 13 in photoelectric conversion portion 14 undergoes photoelectric conversion, generating electron-hole pairs. *Kuboi*, ¶[64]; *supra* XI.A.1.c (claim [1pre(c)]). As indicated by arrows in Figure 1A below, the separated electrons (e), which act as signal charges, travel from films 13 through the interface and semiconductor layer 12, exiting photoelectric conversion portion 14 via conductors 33. *Kuboi*, ¶¶[62], [64].



Kuboi, Fig. 1A.

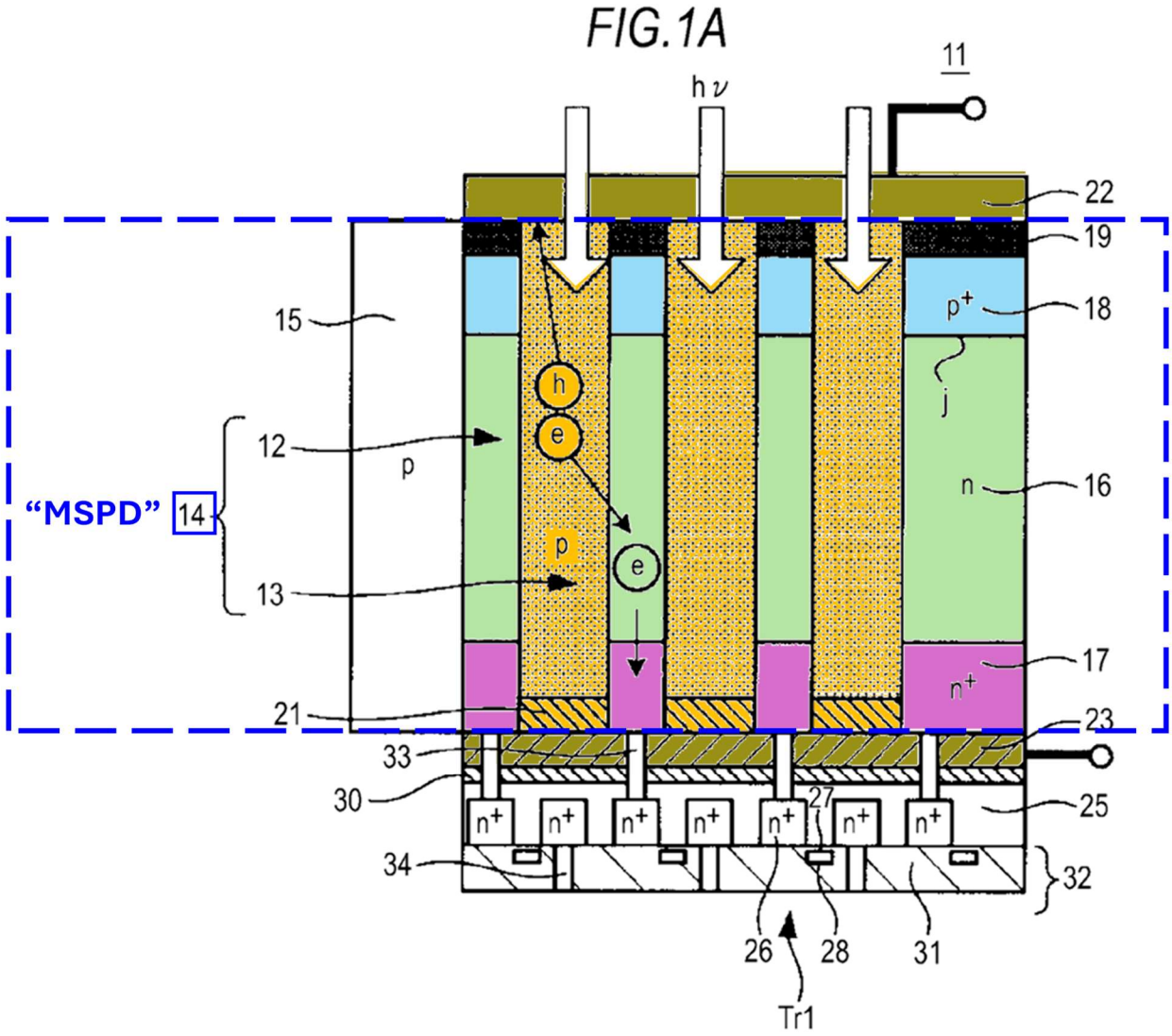
146. The signal charges, determined by the amount of light received by photoelectric conversion portion 14, form the photoelectric conversion portion 14's electrical output. *Kuboi*, ¶[51]; *supra* XI.A.1.c (claim [1pre(c)]). The signal charges are delivered from photoelectric conversion portion 14 to a charge accumulation region 26 of the pixel transistors via electrically isolated conductors 33 that are exposed at the lower surface of photoelectric conversion portion 14. *Kuboi*, ¶¶[62], [64]. The lower surface thus functions as an "output portion," as claimed, for providing electrical output from the photoelectric conversion portion 14.

k. [1h]: "the MSPD includes reverse-bias contacts coupled therewith to establish an electrical field therein when energized to thereby sweep in a selected direction electrical charges generated in the MSPD by said optical input;"

147. In my opinion, *Kuboi* discloses this limitation because photoelectric conversion portion 14 ("MSPD") includes reverse-bias upper and lower electrodes 22, 23 to establish an electric field in photoelectric conversion portion 14 to sweep the signal charges generated by photoelectric conversion of received light towards lower electrode 23 and conductors 33. *Kuboi*, ¶¶[62], [64].

148. *Kuboi* discloses that transparent upper electrode 22 is formed on light shielding film 19, covering the entire upper surface of photoelectric conversion portion 14 through which light enters. *Kuboi*, ¶¶[60], [77], Fig. 1A. Lower

electrode 23 is formed on the entire lower surface of photoelectric conversion portion 14 on n^+-type region 17. *Kuboi*, ¶¶[60], [77], Fig. 1A. Both electrodes are depicted below:



Kuboi, Fig. 1A.

149. Upper electrode 22 is in electrical contact with p^+-type region 18 (of semiconductor layer 12) through light shielding film 19, which is made of electrically conductive tungsten. *Kuboi*, ¶¶[59]-[60]. This is supported by other

prior art that demonstrates what would have been known to a person of ordinary skill in the art. Ex. 1019, 21-22 (discussing the use of tungsten as the first level metal and contact plugs of IC devices); Ex. 1020, 14 (discussing the use of tungsten plugs in electrically conductive vias between different metal layers of a CMOS chip), 15.

150. *Kuboi* discloses that a sufficient voltage is applied between upper and lower electrodes 22, 23 so that p^+-type region 18 is at a negative potential and n^+-type region 17 is at a positive potential. *Kuboi*, ¶¶[64], [87], Fig. 1A. The applied bias voltage creates a depletion layer in n-type region 16 between regions 17 and 18. *Kuboi*, ¶¶[64], [87]. As explained for claim [1pre(a)], a person of ordinary skill would have understood that applying a voltage bias with a negative potential to p^+-type region 18 and a positive potential to n^+-type region 17 constitutes a reverse bias. *Supra* XI.A.1.a. Thus, in my opinion, upper electrode 22 and lower electrode 23 are reverse-bias electrodes that are coupled to photoelectric conversion portion 14.

151. *Kuboi* discloses that when a reverse bias is applied and incident light (hγ) enters photoelectric conversion films 13, electrons (e) in the electron-hole pairs generated by photoelectric conversion of the light move from films 13 through the interface and semiconductor layer 12, which is depleted by the applied bias voltage, toward lower electrode 23 and exit photoelectric conversion portion

14 through conductors 33. *Kuboi*, ¶¶[62], [64], Fig. 1A. Meanwhile, the generated holes (h) move toward upper electrode 22 through photoelectric conversion films 13 and are discharged through upper electrode 22. *Kuboi*, ¶[64].

152. A person of ordinary skill would have understood that when a reverse bias is applied to photoelectric conversion portion 14, the electrodes establish an "electrical field," as claimed, in photoelectric conversion portion 14. This electrical field encourages the electron-hole pairs created by the photoelectric conversion of the light to separate and move towards respective electrodes. Ex. 1019, 10-11 (detailing how an electric field generated by electrodes in a reverse-bias arrangement separates electron-hole pairs and causes them to drift towards the electrodes).

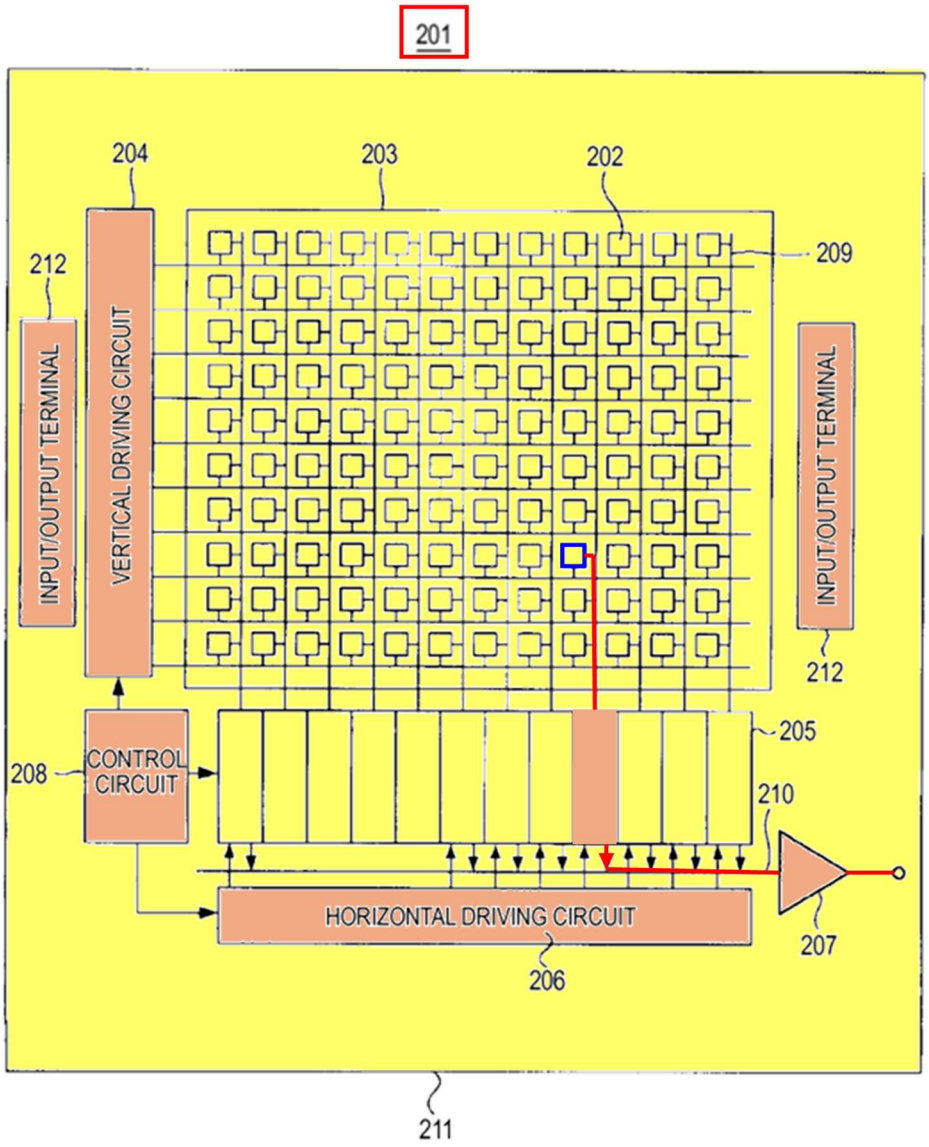
153. *Kuboi* explains that "[t]he hybrid photoelectric conversion portion is configured so that charges generated in the organic material layers through photoelectric conversion move inside the semiconductor layer so as to be guided to a charge accumulation region." *Kuboi*, ¶[11], claim 1. Thus, when a reverse bias is applied to upper and lower electrodes 22 and 23, the electrons generated in photoelectric conversion films 13 by the incident light are driven toward lower electrode 23 and conductors 33 ("to thereby sweep in a selected direction electrical charges generated in the MSPD by said optical input"), while the holes are swept toward upper electrode 22.

l. [1i]: "the active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:"

154. In my opinion, *Kuboi* discloses this limitation because the logic circuits of the active electronic circuit (vertical driving circuit 204, a column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208) perform signal processing of the electrical signals output from photoelectric conversion portion 14 ("MSPD") of pixel 11. *Kuboi*, ¶¶[49]-[52], Fig. 15. As discussed for claim [1pre(b)], all logic circuits of the peripheral circuit portion (including the active electronic circuit) are formed on or in substrate 211 along with the pixels. *Supra* XI.A.1.b.

155. *Kuboi*'s active electronic circuit processes the electrical output from photoelectric conversion portions 14. For instance, the column signal processing circuit 205 "perform[s] signal processing such as noise removal" for each pixel 202 (such as pixel 11 with photoelectric conversion portion 14) in a column. *Kuboi*, ¶[52]. According to *Kuboi*, "the column signal processing circuits 205 perform signal processing such as [correlated double sampling] CDS for removing fixed pattern noise inherent in the pixels 202, signal amplification, or AD conversion." *Kuboi*, ¶[52]. This is illustrated below:

FIG.15



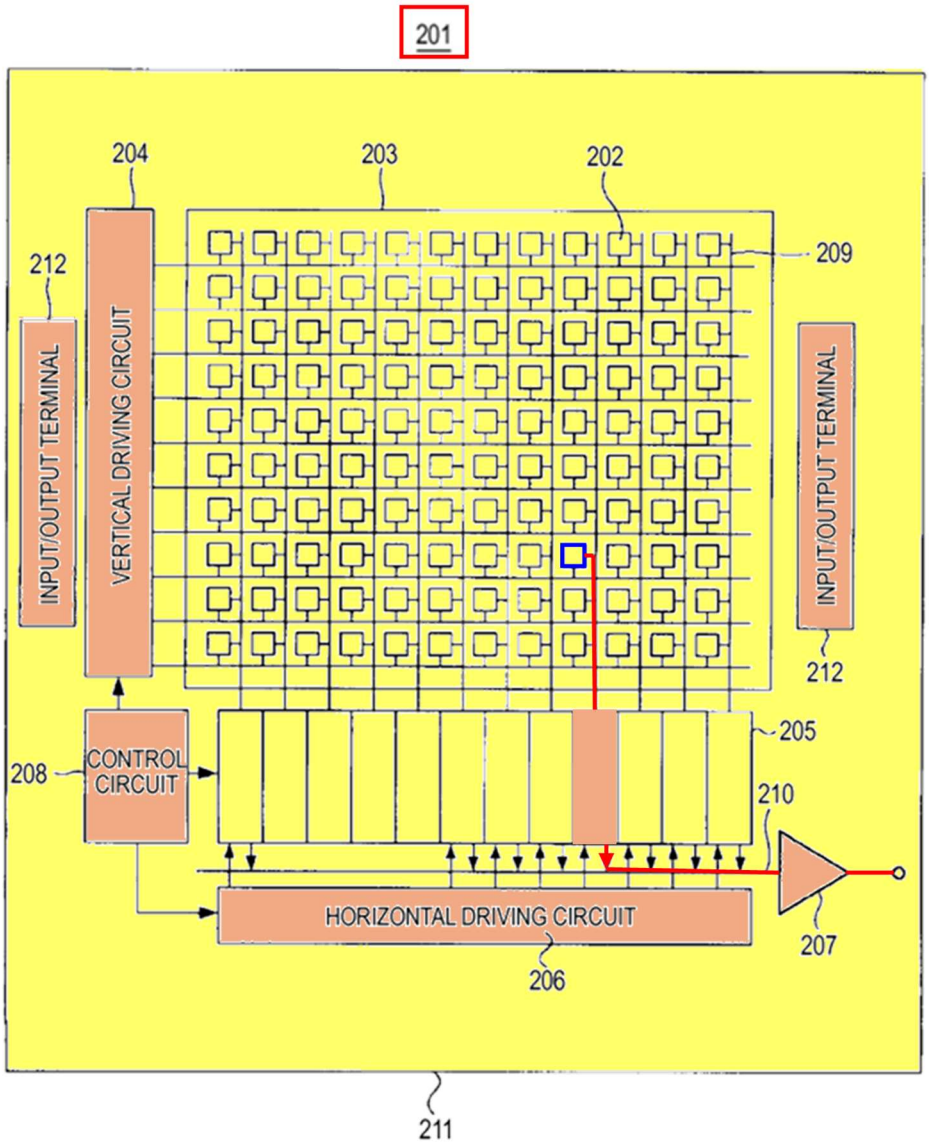
Kuboi, Fig. 15.

156. Thus, *Kuboi*'s "active electronic circuit" (vertical driving circuit 204, a column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208) processes the electrical output from photoelectric conversion portions 14. *Kuboi*, ¶¶[49], [52].

m. [1j]: "amplification to form said processed output from the single-chip device;"

157. In my opinion, *Kuboi* discloses this limitation. The logic circuits of *Kuboi*'s active electronic circuit amplify the electrical output of pixel 11 and outputs it from imaging device 201. *Kuboi*, ¶¶[48]-[49], [52]-[54]. Specifically, "column signal processing circuit[] 205 perform[s] signal processing such as … signal amplification" of the electrical output from a pixel (pixel 11 with photoelectric conversion portion 14). *Kuboi*, ¶[52]. *Kuboi* discloses that the horizontal driving circuit 206 sequentially selects and outputs the processed signals from column signal processing circuit 205 to output circuit 207, which then outputs the processed signals from imaging device 201. *Kuboi*, ¶¶[52]-[54]. This is shown below:

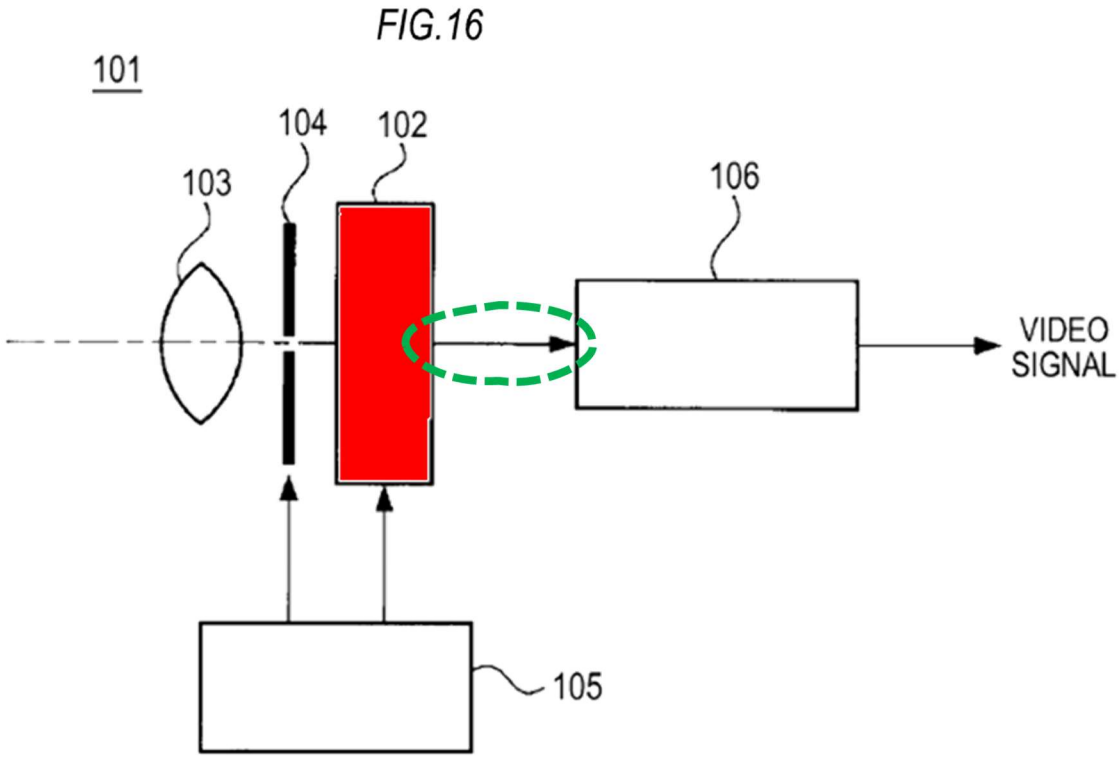
FIG.15



Kuboi, Fig. 15.

158. Thus, column signal processing circuit 205 amplifies the electrical output from photoelectric conversion portion 14, and the processed signal is output through output circuit 207.

159. *Kuboi* discloses that output circuit 207 outputs the processed electrical output of photoelectric conversion portion 14 from imaging device 102. *Kuboi*, ¶¶[54], [191]-[193]. For example, as illustrated below, imaging device 102 can be applied in an apparatus having an external signal processing circuit. *Kuboi*, ¶¶[191]-[193], Fig. 16.



Kuboi, Fig. 16.

160. In this application, output circuit 207 of imaging device 102 outputs the processed output of photoelectric conversion portion 14 to external signal

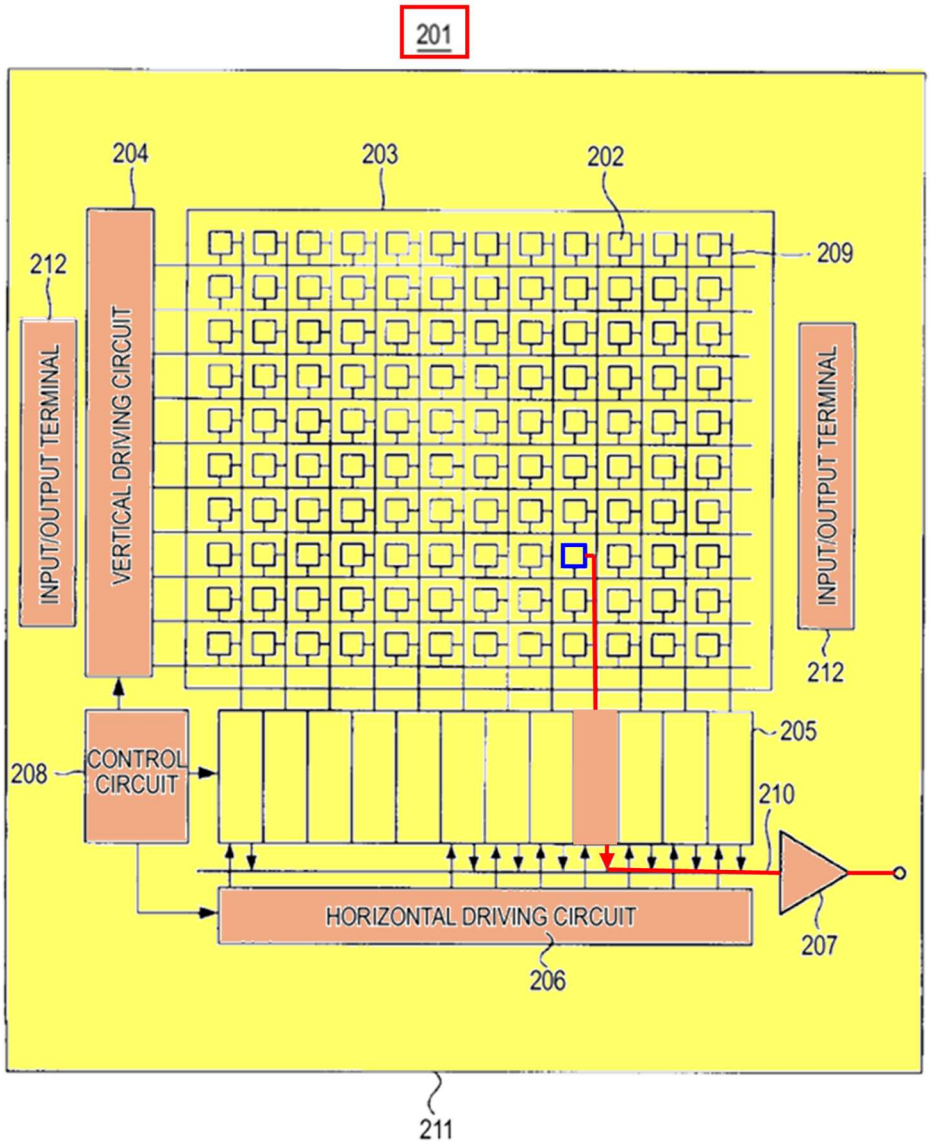
processing circuit 106 as shown in the figure above. *Kuboi*, ¶¶[54], [192], Fig. 16; *infra* XI.A.16.b (claim [26b]).

n. [1k]: "processing other than or in addition to amplification to form said processed output from the single-chip device; and"

161. In my opinion, *Kuboi* discloses this limitation. In addition to amplifying the electrical output received from pixels 11, *supra* XI.A.1.m (claim [1j]), the logic circuits of the active electronic circuit perform additional signal processing of the received signals before outputting the processed output. *Kuboi*, ¶¶[49], [54]. Specifically, "output circuit 207," which is part of the active electronic circuit, "performs signal processing on signals which are sequentially supplied from each of the column signal processing circuits 205 through the horizontal signal line 210 and outputs the processed signals." *Kuboi*, ¶[54].

162. For example, according to *Kuboi*, "output circuit 207 may perform only buffering and may perform black level adjustment, column fluctuation correction, various digital signal processings, and the like." *Kuboi*, ¶[54]. As a result, as shown below, output circuit 207 conducts further signal processing on the processed signals from column signal processing circuit 205 before outputting the processed output.

FIG.15



Kuboi, Fig. 15.

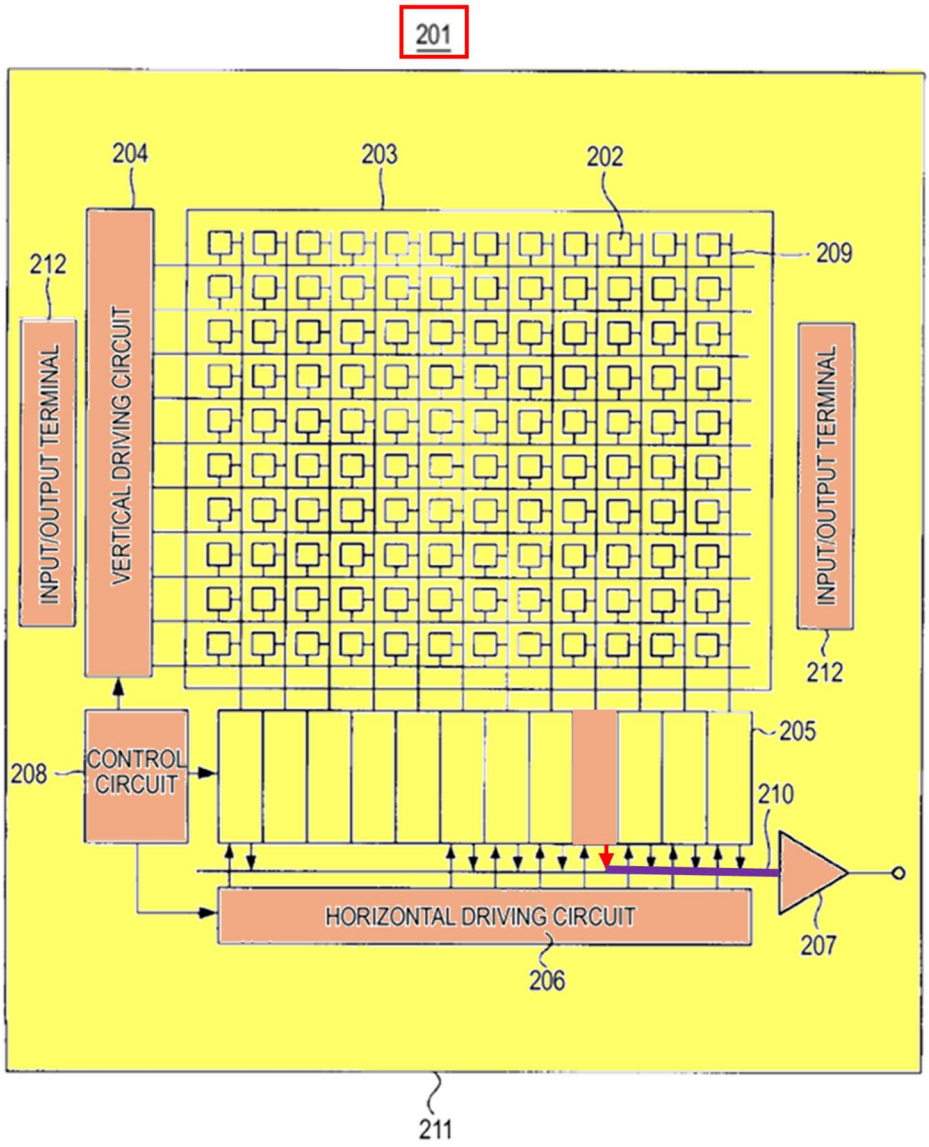
o. [1l]: "routing to one or more selected destinations; and"

163. In my opinion, *Kuboi* discloses this limitation. *Kuboi* discloses that horizontal driving circuit 206 of the active electronic circuit sequentially selects and outputs the processed signals from each column signal processing circuit 205

(including column signal processing circuit 205) to output circuit 207 through horizontal signal line 210. *Supra* XI.A.1.n (claim [1k]); *Kuboi*, ¶¶[53]-[54].

164. To the extent that the term "routing" refers to the physical connection to a destination, horizontal signal line 210, which delivers processed signals from column signal processing circuit 205 to output circuit 207, performs "routing." *See* Ex. 1020, 38 (describing "metal routing" that connects devices in a CMOS circuit). This routing is shown below:

FIG.15

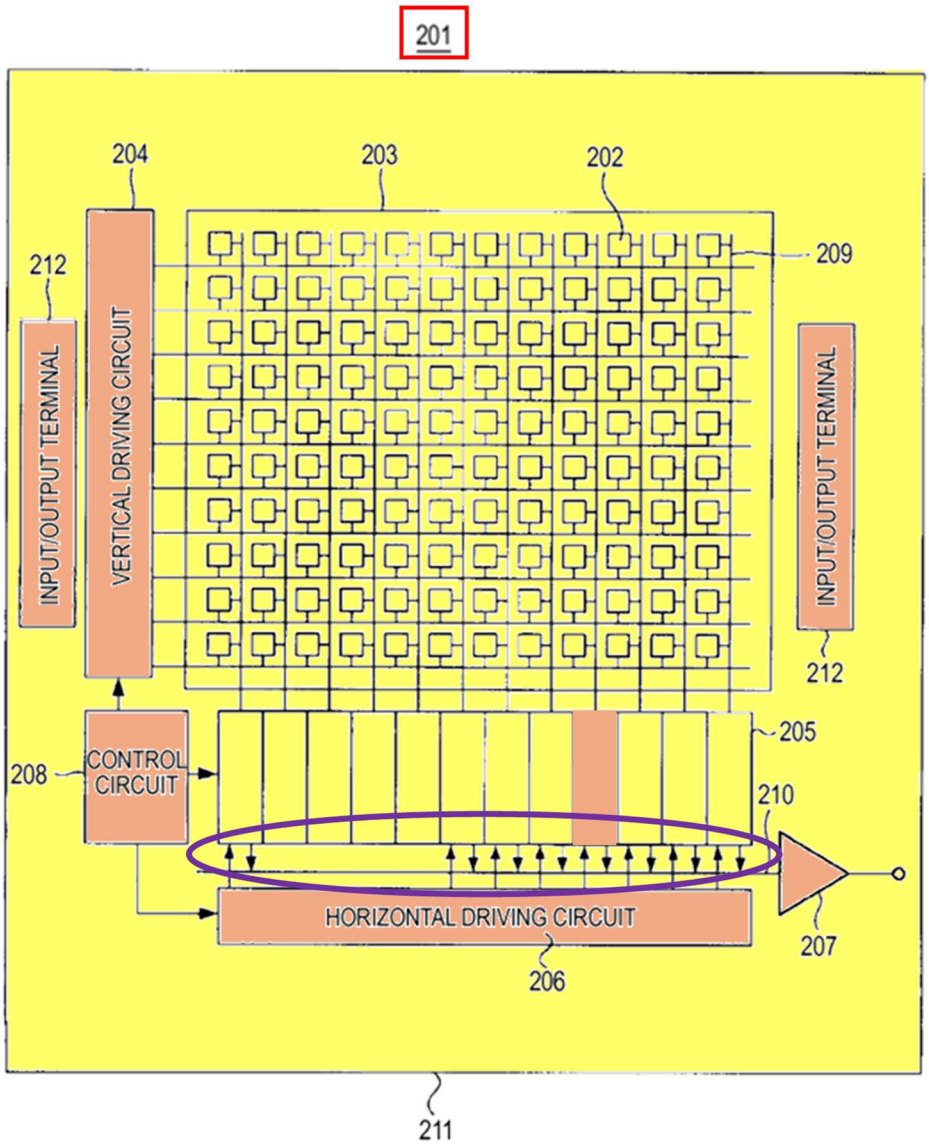


Kuboi, Fig. 15.

165. To the extent that the term "routing" refers to the process of delivering signals to a destination, *see* Ex. 1018, 6, horizontal driving circuit 206 sequentially selects each of column signal processing circuits 205 by sequentially outputting horizontal scanning pulses and delivers the processed signals from each of column signal processing circuits 205 to horizontal signal line 210. *Kuboi*, ¶[53]. *Kuboi*

discloses that output circuit 207 then performs signal processing on the signals sequentially supplied from each column signal processing circuit 205 through horizontal signal line 210. *Kuboi*, ¶[54]. This process is shown below:

FIG.15



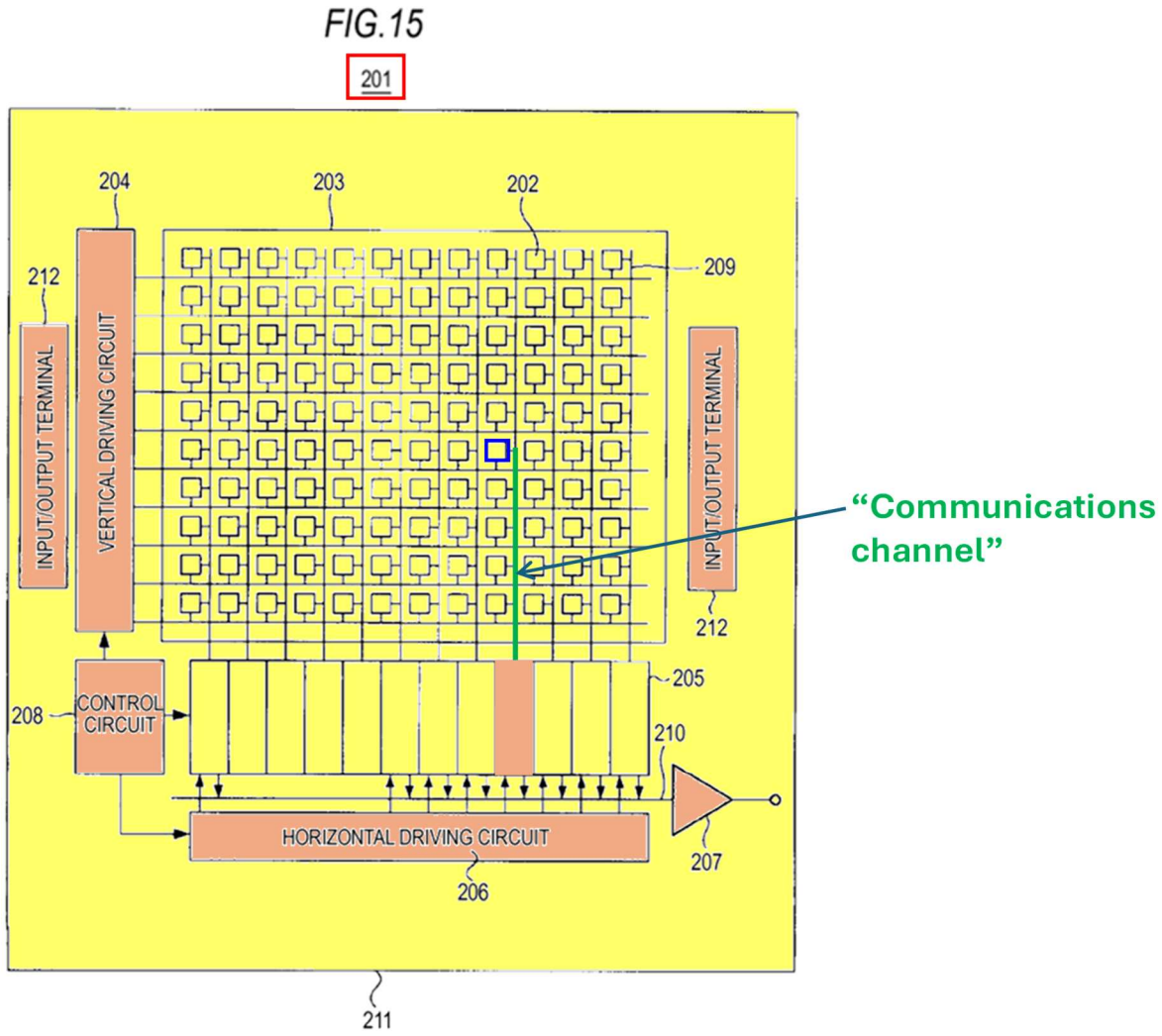
Kuboi, Fig. 15.

166. The process of sequentially selecting each column signal processing circuit 205 by applying scanning pulses (from horizontal driving circuit 206) to a

column signal processing circuit 205 to deliver the processed signals from that column signal processing circuit 205 to output circuit 207 constitutes "routing" the processed signals to the output circuit.

p. [1m]: "a communication channel on or in said single-chip device, configured to deliver the electrical output from the MSPD to the active electronic circuit."

167. In my opinion, *Kuboi* discloses this limitation. In particular, the electrical output from photoelectric conversion portion 14 is supplied to column signal processing circuit 205 of the active electronic circuit through a vertical signal line 209 that is on or in imaging device 201. *Kuboi*, ¶[51], Fig. 15. This is shown below:



Kuboi, Fig. 15.

168. Since both photoelectric conversion portions 14 of pixel 11 and column signal processing circuit 205 are on substrate 211 of imaging device 201, a person of ordinary skill would have recognized that vertical signal lines 209 (for transmitting signals between the aforementioned components) would also be on or

in imaging device 201. *Kuboi*, ¶¶[48]-[49], [51]. Moreover, Figure 15 shows vertical signal lines 209 as being on substrate 211.

2. Claim 2

a. [2]: "The single-chip device of claim 1, in which said active electronic circuit at least partly extends beyond said substrate."

169. In my opinion, *Kuboi* discloses or renders obvious this additional limitation. As explained for claim [1pre(a)], in *Kuboi*'s imaging device 201, the claimed "active electronic circuit" includes vertical driving circuit 204, a column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208. *Supra* XI.A.1.a; *Kuboi*, ¶[49]. As also explained for claim [1pre(a)], these CMOS logic circuits include transistors connected together. *Supra* XI.A.1.a; Ex. 1019, 4 ("Complementary MOS (CMOS) refers to a complementary *p*-channel and *n*-channel MOSFET pair.").

170. In my opinion, a person of ordinary skill would have known that logic circuits on CMOS imaging device 201 include multiple transistors connected together using metal interconnects that route signals between the transistors and other devices in the circuit. *Supra* XI.A.1.a; Ex. 1020, 9-14, Fig. 2.22. It would have been obvious to a person of ordinary skill that, although the transistors themselves are formed partly within the substrate, the metal interconnects that connect them are formed above the substrate using "above-wafer" steps. Ex. 1020,

10-12, 13 (Fig. 2.20 illustrates the "above-wafer" steps in the processing sequence); Ex. 1016, 1-3. For example, in the figure below, metal interconnects (Metal 1, Metal 2, etc.) are deposited above the substrate surface with dielectric layers in between to electrically insulate the transistors and the metal conductors. Ex. 1020, 10, 13-14, 25-26.

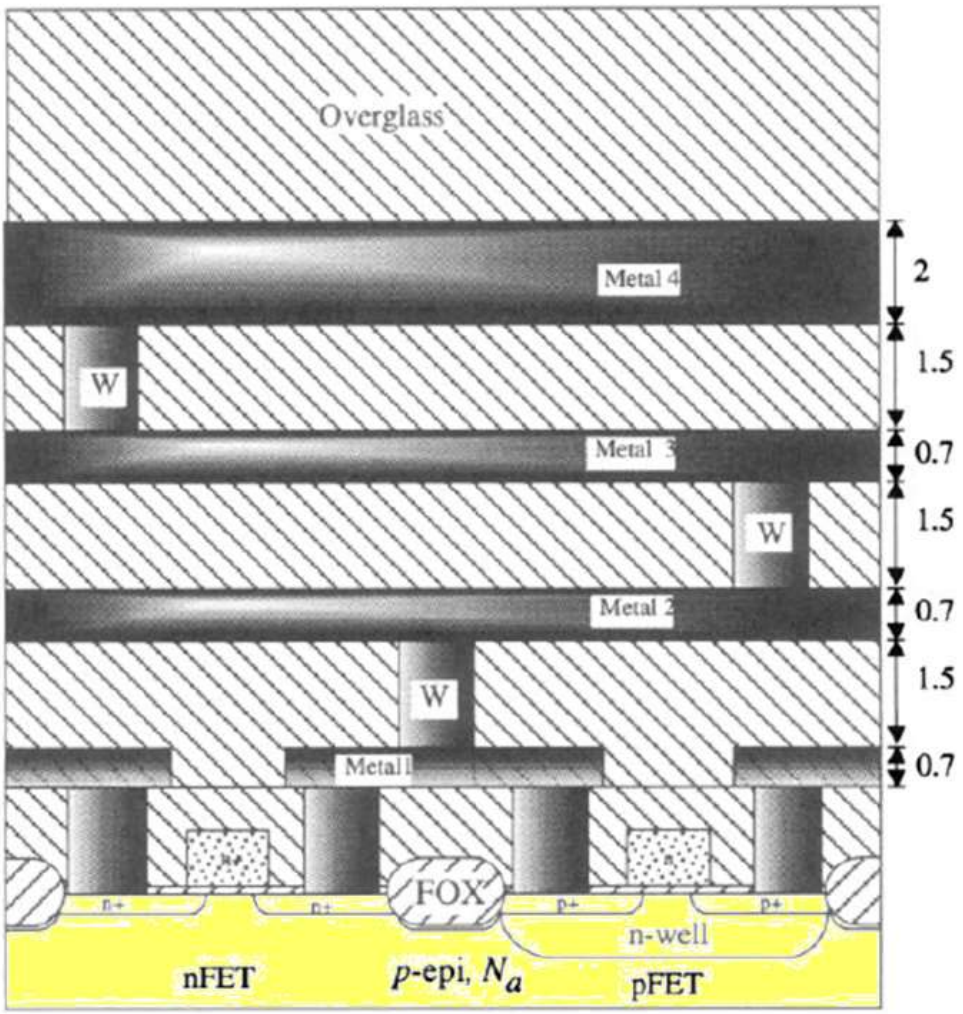


Figure 2.22 Visualization of 4-metal interconnect structure

Ex. 1020, 14.

171. In my opinion, it would have been obvious that *Kuboi*'s CMOS logic circuits (of the active electronic circuit) would use interconnects (or wiring) formed above the substrate surface to connect to the transistors of these circuits. For example, a person of ordinary skill would have known that CMOS logic circuits have "many [such] interconnect layers … to ease the layout and signal distribution problems." Ex. 1020, 10. Thus, a person of ordinary skill would have found it obvious that wiring that connects to the transistors of the active electronic circuit would at least partly extend beyond substrate 211.

172. A person of ordinary skill would have been motivated to incorporate wiring formed above substrate 211 to form electrical connections to the transistors of *Kuboi*'s logic circuits so that these logic circuits can be formed using conventional CMOS processes. *See* Ex. 1020, 10-14, 25-26. Imaging device 201 already incorporates such above-the-substrate wiring layers. *See Kuboi*, ¶[62]. For instance, a multilayer wiring layer 32, comprising multiple wiring layers separated by an insulating film 31, is formed on the substrate surface containing pixel transistors. *Kuboi*, ¶[62]. In my opinion, given the widespread use of wiring layers above the substrate in CMOS logic circuits and *Kuboi*'s existing implementation of such wiring layers, a person of ordinary skill would have reasonably expected success in forming above-substrate wiring layers to provide electrical connections to transistors of the active electronic circuit within substrate 211. As a result, in my

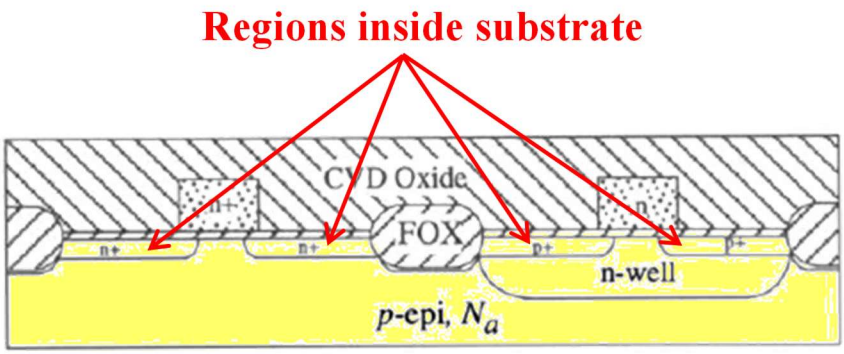
opinion, it would have been obvious to a person of ordinary skill that portions of *Kuboi*'s active electronic circuit, including above-the-substrate wiring layers, would at least partly extend beyond substrate 211.

3. Claim 3

a. [3]: "The single-chip device of claim 1, in which said active electronic circuit is at least partly inside said substrate."

173. In my opinion, *Kuboi* discloses this additional limitation. As explained *supra* for claim [1pre(a)], in *Kuboi*'s CMOS imaging device 201, the logic circuits of vertical driving circuit 204, column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208 are the claimed "active electronic circuit." *Supra* XI.A.1.a; *Kuboi*, ¶[49].

174. As explained for claims [1pre(a)] and [2], a person of ordinary skill would have known that CMOS logic circuits include transistors. *Supra* XI.A.1.a, XI.A.2.a. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. Ex. 1020, 9-14; Ex. 1019, 4 (describing logic circuits as including transistors). In my opinion, a person of ordinary skill would also have understood that transistors are formed by doping regions of the substrate with selected impurities to create the sources and drains of the transistors. Ex. 1020, 9-14; Ex. 1019, 4-9. This is further shown below:



(a) CVD oxide and planarization

Ex. 1020, 13.

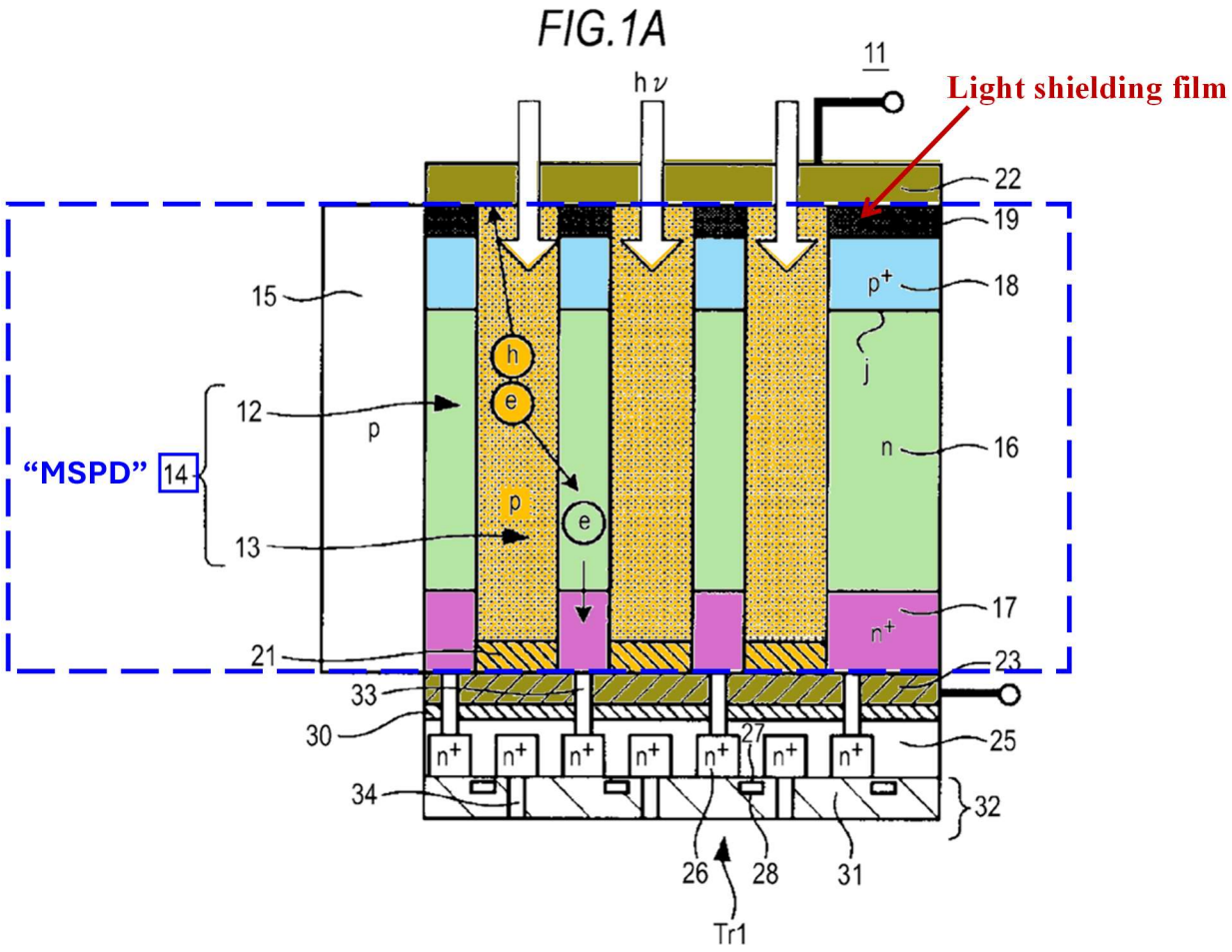
175. For example, an "n-well is created using a deep ion implant that is diffused deeper into the substrate," and "transistors … are formed by ion implants using the self-aligned scheme. pFETs are created using a p-type boron implant in which nFET locations are blocked …. Similarly, nFETs require an n-type implant for drain and source regions." Ex. 1020, 10. Thus, in my opinion, the doped regions of the transistors in *Kuboi*'s active electronic circuit are thus at least partly inside substrate 211.

4. Claim 4

a. [4]: "The single-chip device of claim 1, in which said overlying region is present as a superstrate at one side of said first, intermediate, and second regions, and contains said holes."

176. In my opinion, *Kuboi* discloses this additional limitation. As explained for claim [1c], *Kuboi* discloses a light shielding film 19 formed on the light incident surface of the semiconductor layer 12 that contains holes that align

with the holes in p^+-type region 18 ("first region"), n-type region 16 ("intermediate region"), and n^+-type region 17 ("second region"). *Supra* XI.A.1.f; *Kuboi*, ¶¶[59], [75]-[76], Fig. 1A. As shown below, light shielding film 19 is formed on top of the stacked p^+-type region 18 (P), n-type region 16 (I), and n^+-type region 17 (N), and is therefore a superstrate of the stacked PiN regions. *Kuboi*, ¶¶[59], [75]-[76], Fig. 1A.



Kuboi, Fig. 1A.

177. Moreover, light shielding film 19 is formed on the light receiving side of semiconductor layer 12, and as discussed for claim [1c], it contains holes. *Supra* XI.A.1.f; *Kuboi*, ¶¶[59], [75]-[76]; Fig. 1A.

5. Claim 7

a. [7]: "The single-chip device of claim 1, further including a region of a dielectric material that covers the holes and is in the propagation path of said optical input."

178. In my opinion, *Kuboi* discloses this additional limitation. *Kuboi* refers to dielectric films ("dielectric material") as "insulating films." *Kuboi*, ¶[59] ("an insulating film such as, for example, a silicon nitride (Si_3N_4) film, a silicon oxide (SiO_2) film, and the like"). A person of ordinary skill would have understood that silicon nitride and silicon oxide (SiO_2) are dielectric materials. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. Ex. 1020, 34-35; Ex. 1019, 9, 12; Ex. 1009, 5. *Kuboi* discloses that, "[a]lthough not shown in the drawing, an on-chip microlens is formed on the upper electrode 22 which is a transparent electrode with or without color filters disposed therebetween. The color filters are formed on the upper electrode 22 with or without an insulating film disposed therebetween." *Kuboi*, ¶¶[63], [73], [146].

179. In addition, a person of ordinary skill would have understood that an "insulating film" disposed between the microlens and the color filter of a CMOS

image sensor would be made of a dielectric material to provide a suitable surface for microlens formation. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. For example, as shown below, Exhibit 1027 describes a CMOS image sensor with a color filter and microlens formed over each photodiode on a substrate. Ex. 1027, 2-3.

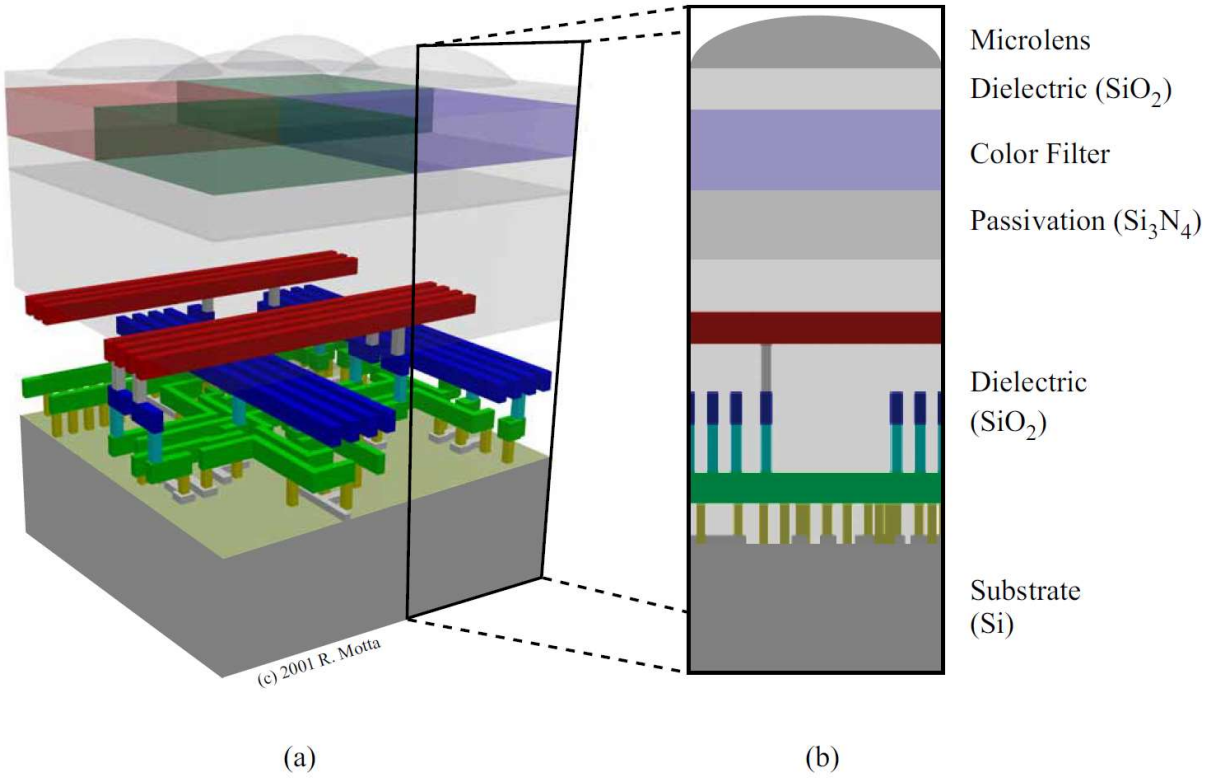


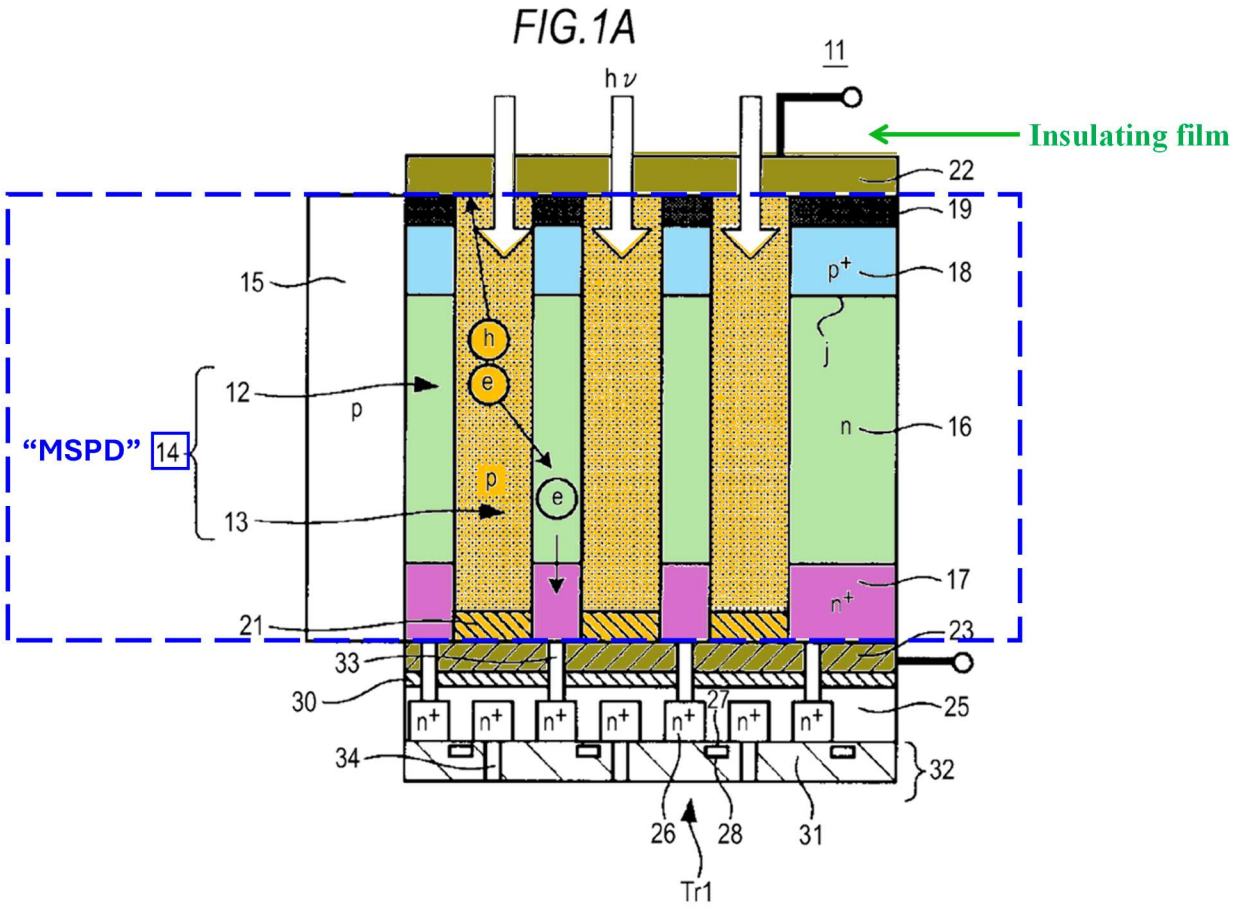
Fig. 1. (a). Three-dimensional (3D) structure of a typical four-pixel unit cell of a CMOS image sensor with a red-green-green-blue Bayer color filter array. (b) Single pixel side view, including the microlens, color filter, passivation layer, dielectric layers, metal interconnects, and silicon substrate.

Ex. 1027, 3.

180. A dielectric layer of silicon oxide is formed between the color filter and the microlens to "provide[] a suitable surface for microlens formation." Ex.

1027, 4. Thus, in addition to *Kuboi*'s express disclosure, a person of ordinary skill would have understood that *Kuboi*'s insulating film positioned between the color filter and on-chip microlens is an insulating film made of a "dielectric material," as claimed. Ex. 1012, 4 (describes a dielectric tunnel positioned between the microlens and the photodetector and illustrates this dielectric tunnel in Figure 4); Ex. 1033, 2-5 (explains that the microlens is typically constructed on a dielectric layer to ensure signal integrity).

181. Since light ("optical input") passing through the on-chip microlens to enter photoelectric conversion films 13 of pixel 11 would traverse the dielectric insulating film (positioned between the color filter and upper electrode 22), this insulating film "is in the propagation path of said optical input." *Kuboi*, ¶[64]. This is shown below:



Kuboi, Fig. 1A.

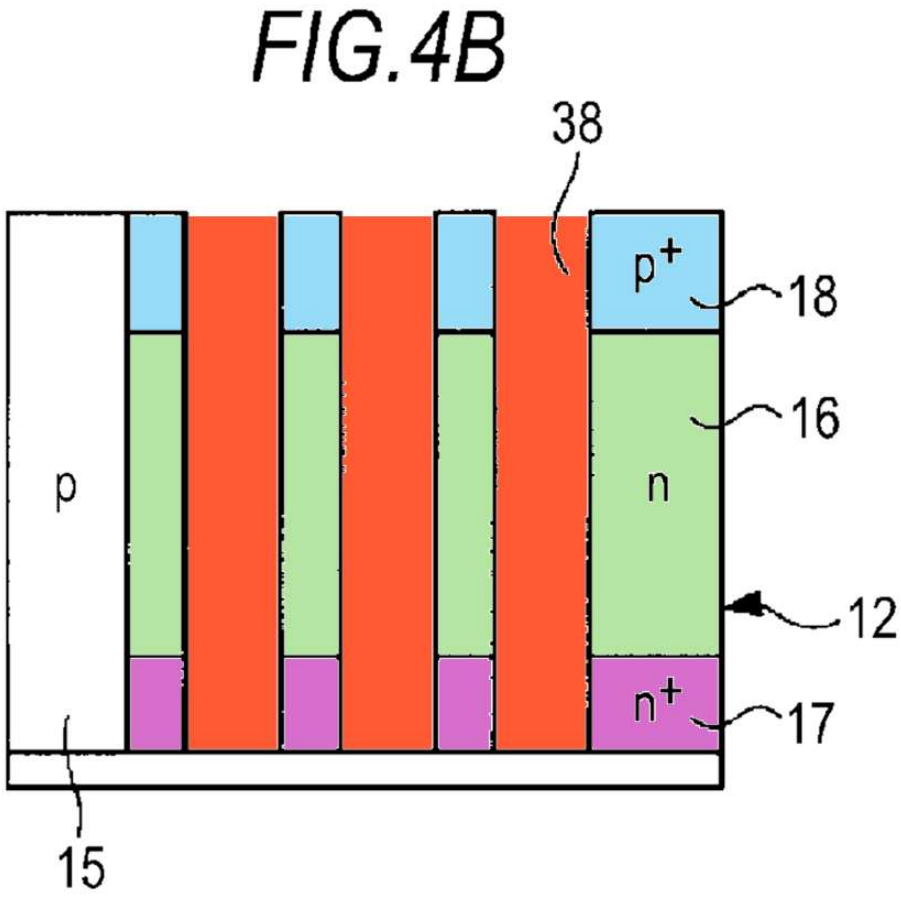
182. In my opinion, a person of ordinary skill would have recognized that an insulating film positioned in such a location would cover the holes in semiconductor substrate 12 through which films 13 extend.

6. Claim 9

a. [9]: "The single-chip device of claim 1, in which said holes are present in said intermediate region."

183. In my opinion, *Kuboi* discloses this additional limitation. As explained for claim [1c], after n^+-type region 17, n-type region 16, and p^+-type region 18 are formed on the semiconductor layer 12, "vertical hole[s] 38"

"extending from the p^+-type … region 18 to the n^+-type … region [17] [are] formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching." *Kuboi*, ¶¶[71]-[72]; *supra* XI.A.1.f. Vertical holes 38 are shown below:



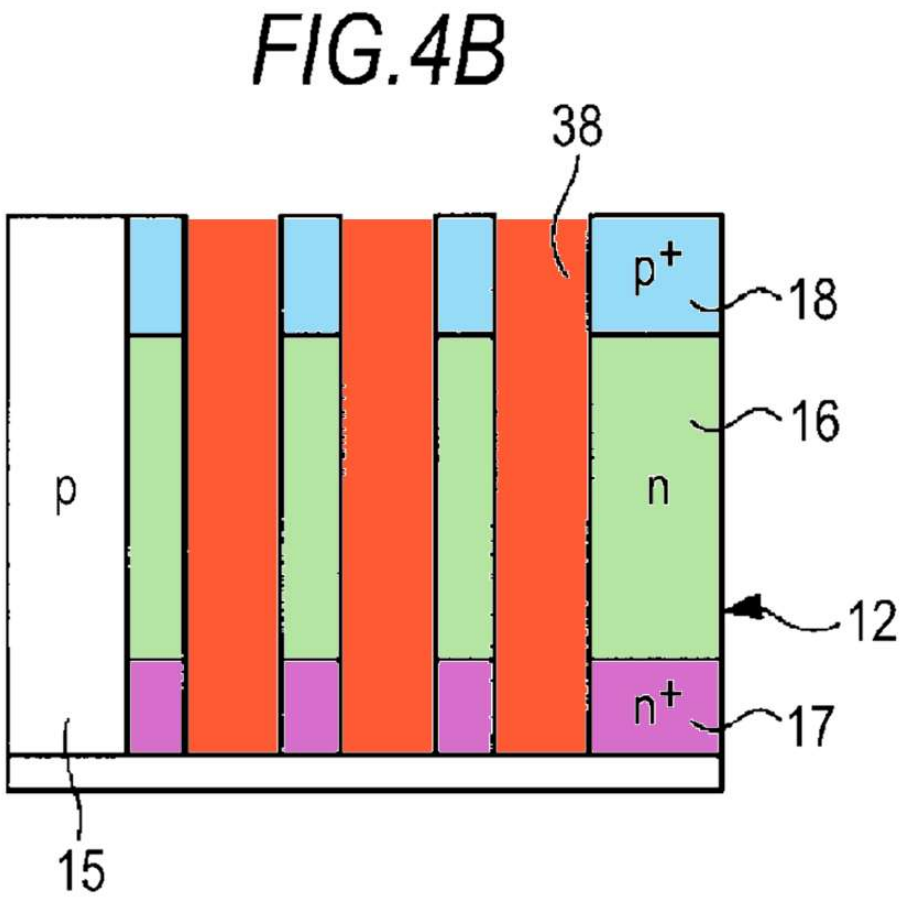
Kuboi, Fig. 4B.

184. Accordingly, in *Kuboi*, holes 38 are present in n-type region 16, which is the claimed "intermediate region." *Supra* XI.A.1.d (claim [1a]); *Kuboi*, ¶¶[71]-[72], Fig. 4B.

7. Claim 10

a. [10]: "The single-chip device of claim 1, in which said holes are present in said intermediate region as well as in at least one of the first and second regions."

185. In my opinion, *Kuboi* discloses this additional limitation. As explained for claims [1c] and [9], *Kuboi*'s "vertical hole[s] 38" "extending from the p^+-type … region 18 to the n^+-type … region [17] [are] formed in a region of the semiconductor layer 12." *Kuboi*, ¶¶[71]-[72]; *supra* XI.A.1.f, XI.A.6.a. These vertical holes 38 are shown below:



Kuboi, Fig. 4B.

186. Accordingly, holes 38 are present in n-type region 16 ("intermediate region"), p^+-type region 18 ("first region"), and n^+-type region 17 ("second region"). *Supra* XI.A.1.d (claim [1a]), XI.A.1.f (claim [1c]); *Kuboi*, ¶¶[71]-[72], Fig. 4B.

8. Claim 11

a. [11]: "The single-chip device of claim 1, in which said holes are present in each of the first, second, and intermediate region."

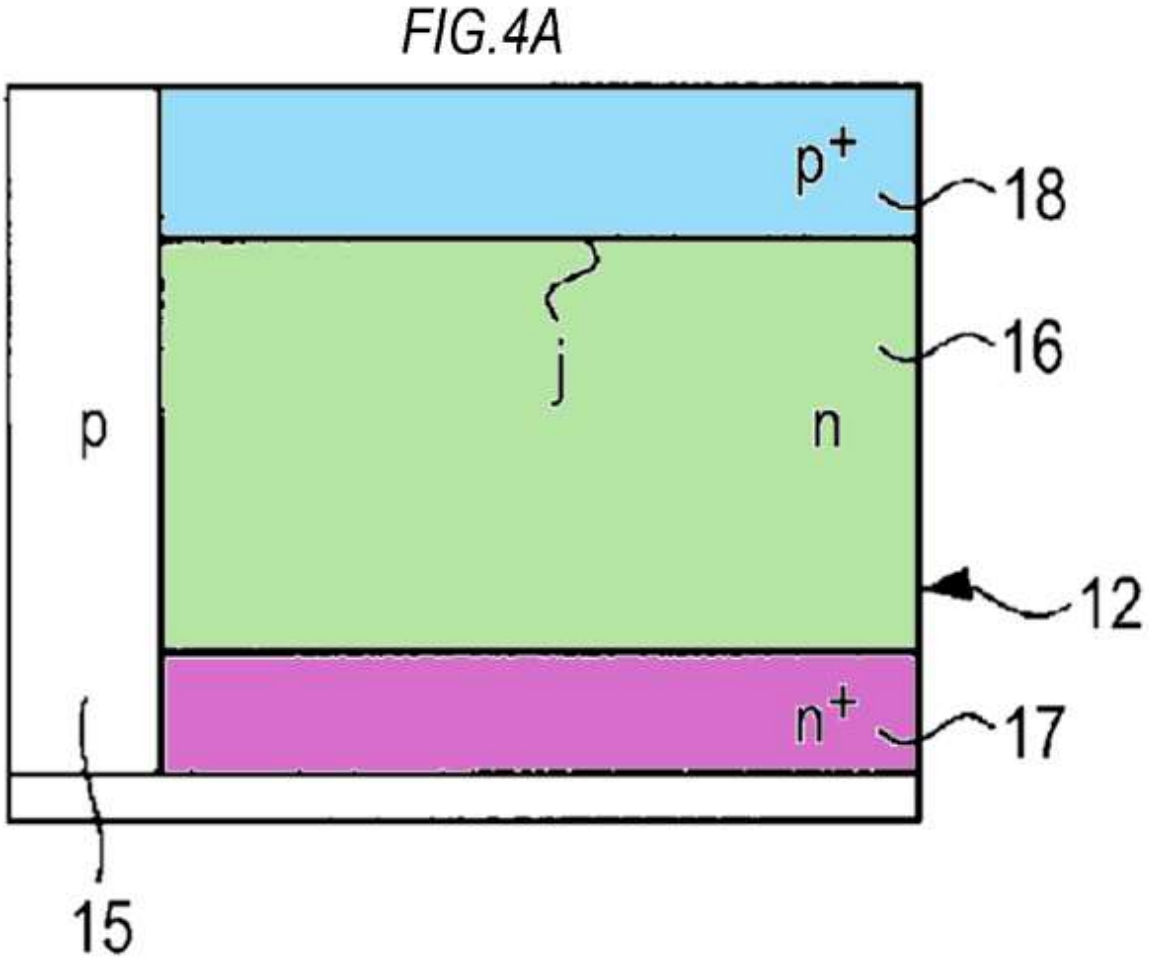
187. In my opinion, *Kuboi* discloses this additional limitation. As explained for claim [10], *Kuboi*'s holes 38 are present in n-type region 16 ("intermediate region"), p^+-type region 18 ("first region"), and n^+-type region 17 ("second region"). *Supra* XI.A.1.d (claim [1a]), XI.A.1.f (claim [1c]), XI.A.7.a (claim [10]); *Kuboi*, ¶¶[71]-[72], Fig. 4B.

9. Claim 12

a. [12]: "The single-chip device of claim 1, in which each of said first and second regions and said intermediate region has a thickness and at least some of said holes extend through the entire thickness of said intermediate region and of one of said first region and second region and through at least a part of the thickness of the other one of said first and second regions."

188. In my opinion, *Kuboi* discloses this additional limitation. *Kuboi* discloses that, during manufacturing, semiconductor layer 12 is implanted with impurities to form (in order) n^+-type region 17 ("first region"), n-type region 16

("intermediate region"), and p^+-type region 18 ("second region"). *Kuboi*, ¶¶[55]-[56], [71]; *supra* XI.A.1.d (claim [1a]). *Kuboi* shows all three regions in Figure 4A:



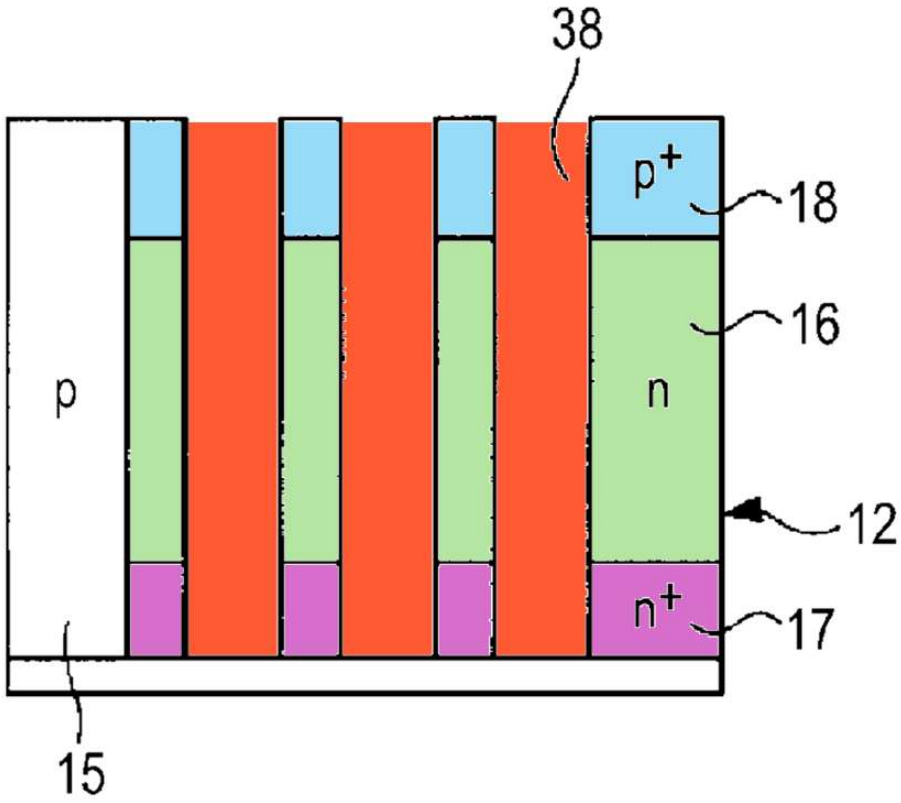
Kuboi, Fig. 4A.

189. In my opinion, a person of ordinary skill would have understood that each region has a thickness. *Kuboi*, Figs. 1A, 4A-4F. This is evident from the figures.

190. In addition, *Kuboi* discloses that, in one example, the total thickness (d1) of the semiconductor layer 12 is about 1.4 microns (μm). *Kuboi*, ¶[94]. In my opinion, a person of ordinary skill would have understood that this example makes clear that the regions in the figure would have at least some thickness, even if the figures themselves do not disclose specific dimensions. A person of ordinary skill would have further understood that when the 1.4-micron thick semiconductor layer 12 is implanted with impurities to form a stacked structure, each of the component regions will have a thickness that together sum to 1.4 microns. For example, a person of ordinary skill would have known that the total thickness of 1.4 microns will be a sum of the thicknesses of each component region - p^+-type region 18 ("first region"), n-type region 16 ("intermediate region"), and n^+-type region 17 ("second region").

191. *Kuboi* further discloses that, after forming the stacked structure, vertical holes 38 "extending from the p^+-type … region 18 to the n^+-type … region [17]" are dry-etched in semiconductor layer 12. *Kuboi*, ¶¶[71]-[72]; *supra* XI.A.1.f(claim [1c]), XI.A.6.a-XI.A.8.a (claims [9]-[11]). These are shown below:

FIG.4B



Kuboi, Fig. 4B.

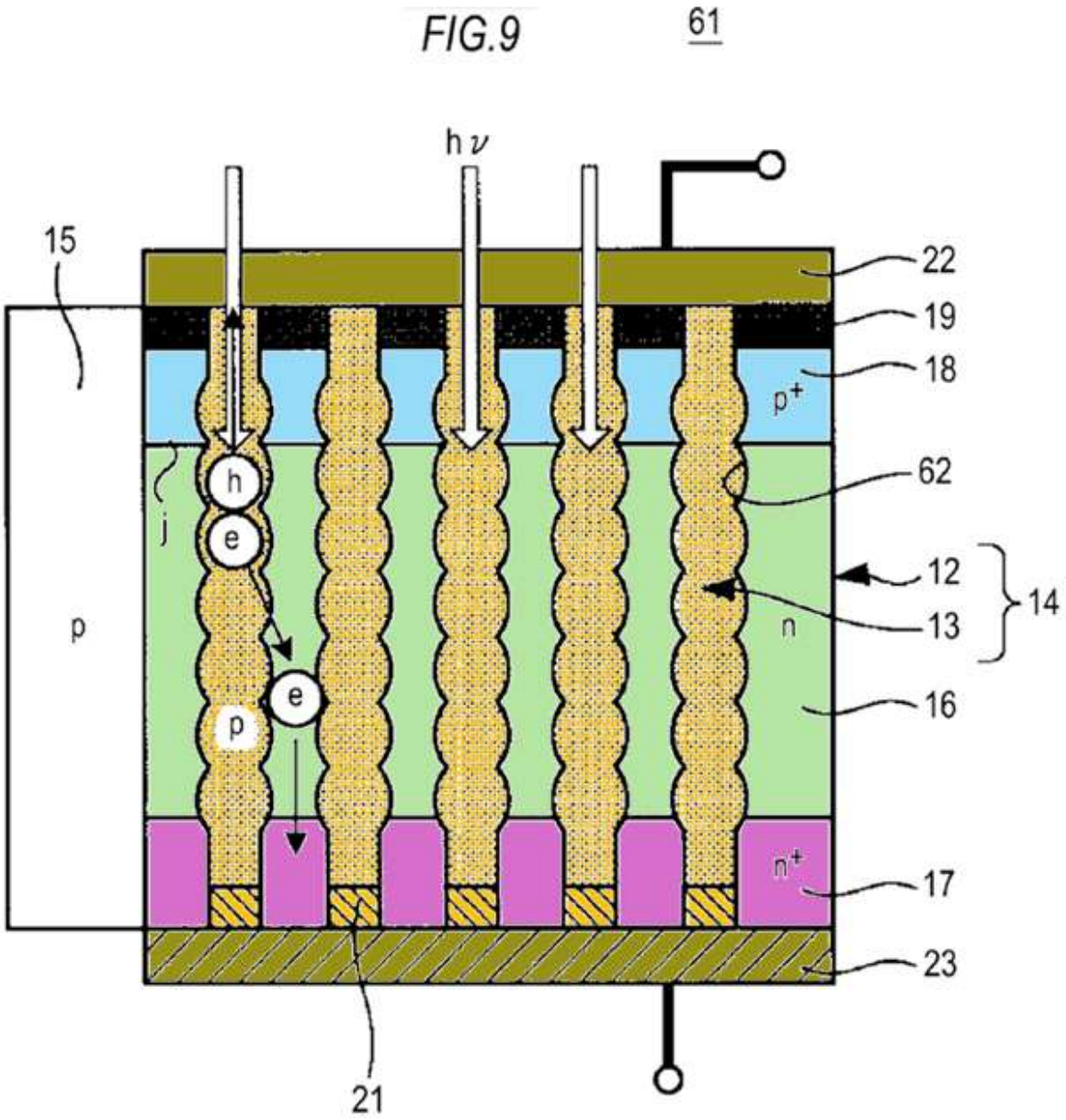
192. Accordingly, holes 38 extend through the entire thickness of n-type region 16 ("intermediate region") and p^+-type region 18 ("first region") and through at least a part of the thickness of n^+-type region 17 ("second region"). *Supra* XI.A.1.d (claim [1a]), XI.A.1.f (claim [1c]); *Kuboi*, ¶¶[71]-[72], Fig. 4B.

10. Claim 16

a. [16]: "The single-chip device of claim 1, in which at least some of said holes have sidewalls that slope in planes transverse to said regions."

193. In my opinion, *Kuboi* renders obvious this additional limitation. As explained for claim [1c], "vertical hole[s] 38" "extending from the p^+-type … region 18 to the n^+-type … region [17] [are] formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching." *Kuboi*, ¶¶[71]-[72]; *supra* XI.A.1.f. *Kuboi* further discloses that, by using "the Bosch process" for dry-etching the holes, "it is possible to form a concavo-convex shape on the lateral walls of the vertical holes 38." *Kuboi*, ¶[72], Fig. 9. These concavo-convex shaped holes meet the requirements of claim 16.

194. *Kuboi* explains that "[b]y forming the concavo-convex shape, it is possible to increase the area of the interface with the organic photoelectric conversion film formed in a subsequent step and to accelerate the movement of electrons (charges)," which increases light absorption efficiency and improves sensitivity. *Kuboi*, ¶¶[72], [80]. This concavo-convex shape on the lateral walls of vertical holes 38 is shown below:

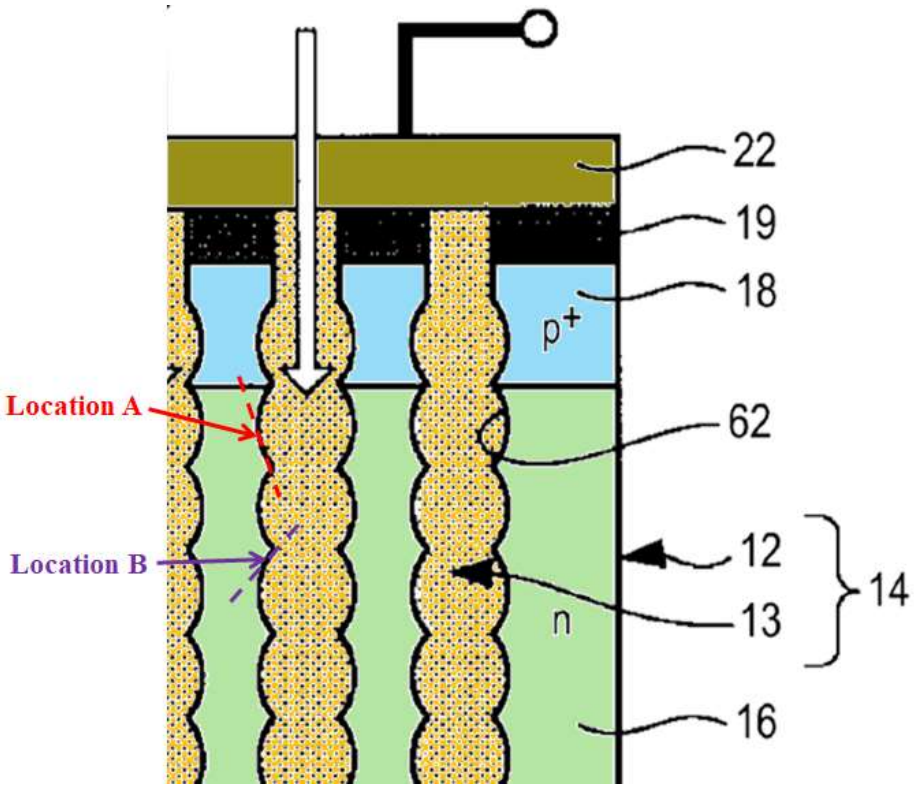


Kuboi, Fig. 9.

195. Figure 9 depicts photoelectric conversion portion 14, where the Bosch process is employed to create holes 62 with a "concavo-convex shape … at the interface between the semiconductor layer 12 and the organic photoelectric conversion film 13." *Kuboi*, ¶[137]. *Kuboi* discloses that the size of the concavo-

convex shape can be adjusted in the Bosch process. *Kuboi*, ¶¶[139]-[140]. Organic photoelectric conversion films 13 are subsequently embedded into these holes. *Kuboi*, ¶[139]. According to *Kuboi*, the fabrication process in Figure 9, which includes concavo-convex holes 62, is "basically the same" as that for photoelectric conversion portion 14 in Figure 1A, except that the Bosch process is used to form the holes. *Kuboi*, ¶¶[137], [139].

196. Concavo-convex holes 62 feature sidewalls that slope in planes transverse to the stacked n^+-type region 17, n-type region 16, and p^+-type region 18. For example, the sidewalls of the holes 62 at the locations marked A and B, shown below, are sloped in planes parallel to the plane of this paper, which is oriented transversely to the stacked layers.



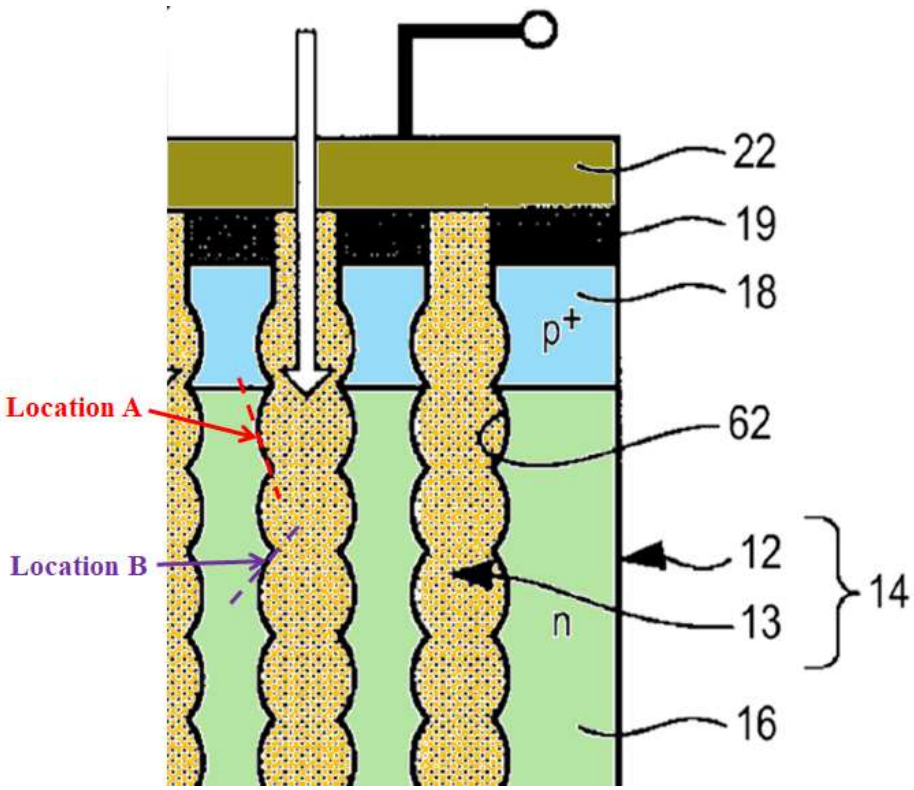
Kuboi, Fig. 9 (cropped).

197. In my opinion, a person of ordinary skill would have been motivated to incorporate concavo-convex holes 62 in photoelectric conversion portion 14 of Figure 1A to enhance electron mobility and thus improve light absorption efficiency and sensitivity of photoelectric conversion portion 14. *Kuboi*, ¶¶[72], [80], [137], [139]. Since *Kuboi* explicitly states that the Bosch process can be used to create holes with concavo-convex walls in photoelectric conversion portion 14 of Figure 1A, the results would have been entirely predictable and a person of ordinary skill would have had a reasonable expectation of success in carrying out this modification. *Kuboi*, ¶[72].

11. Claim 17

a. [17]: "The single-chip device of claim 1, in which at least some of said holes have sidewalls with plural different slopes along the inside walls of the holes."

198. In my opinion, *Kuboi* renders obvious this additional limitation. As outlined for claim [16], a person of ordinary skill would have been motivated to integrate concavo-convex holes 62 into *Kuboi*'s photoelectric conversion portion 14 to boost electron mobility, light absorption efficiency, and sensitivity. *Supra* XI.A.10.a; *Kuboi*, ¶¶[72], [80], [137], [139]. The same analysis applies here. As shown below, concavo-convex holes 62 feature sidewalls with varying slopes along the inner walls.



Kuboi, Fig. 9 (cropped).

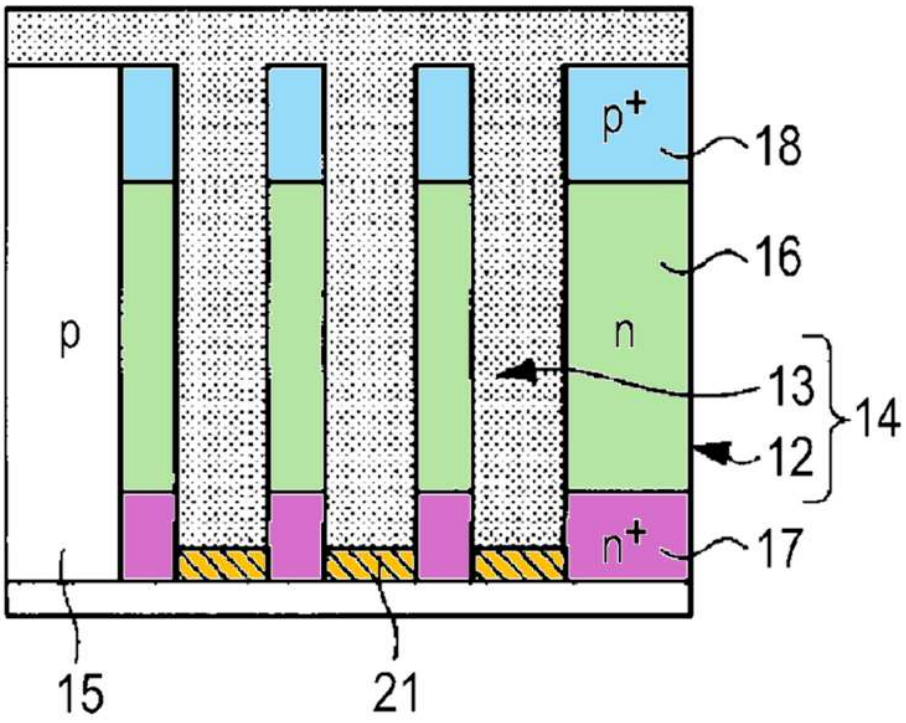
199. A person of ordinary skill would have understood that the sidewalls at locations A and B have different slopes, as required by the claim.

12. Claim 20

a. [20]: "The single-chip device of claim 1, in which the holes are at least partly filled with a dielectric material."

200. In my opinion, *Kuboi* discloses this additional limitation. During the manufacturing of *Kuboi*'s pixel, vertical holes 38 extending from the p^+-type region 18 to the n^+-type region 17 are first formed in a region of the semiconductor layer 12. *Kuboi*, ¶¶[71]-[72]. Then, according to *Kuboi*, "an electron blocking film 21 having a thickness of several tens of nm, for example[,] is formed on the bottom portions of the vertical holes 38" by chemical vapor deposition. *Kuboi*, ¶[73], Fig. 4C. Electron blocking film 21 is annotated in the figure below:

FIG.4C



Kuboi, Fig. 4C.

201. *Kuboi* discloses that electron blocking film 21 is composed of an insulating material, such as silicon nitride (Si_3N_4) or silicon dioxide (SiO_2). *Kuboi*, ¶[59]. In my opinion, a person of ordinary skill would have understood that silicon nitride (Si_3N_4) and silicon dioxide (SiO_2) are dielectric materials. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. Ex. 1020, 34-35; Ex. 1019, 9, 12. Thus, the holes of the photoelectric conversion portion 14 "are at least partly filled with a dielectric material," as claimed.

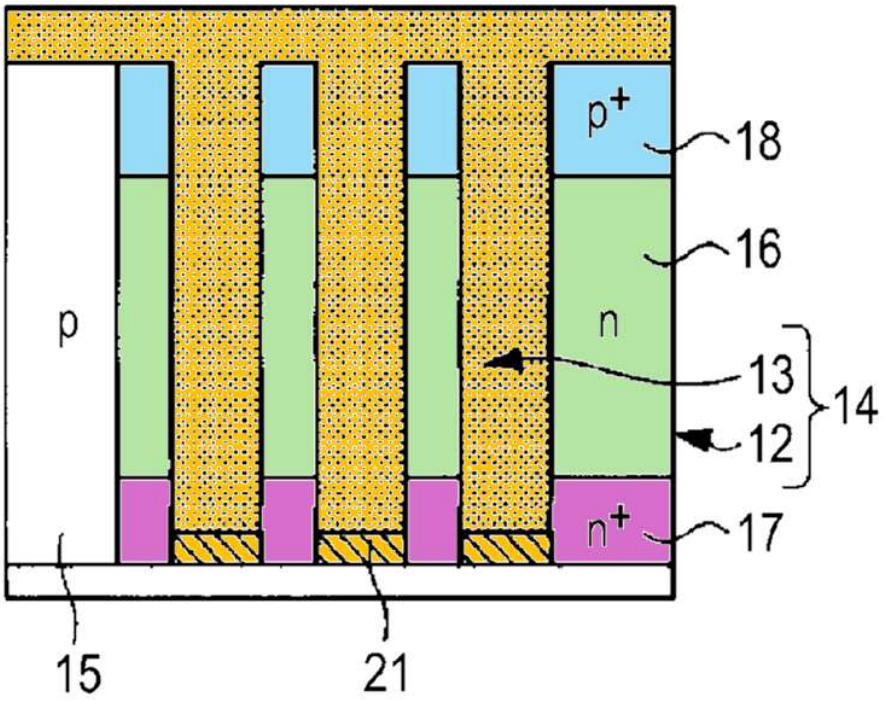
13. Claim 21

a. [21]: "The single-chip device of claim 1, in which the holes are entirely filled with a dielectric material."

202. In my opinion, *Kuboi* discloses this additional limitation. As detailed for claim [20], after the formation of holes 38, electron blocking film 21 composed of a dielectric material such as silicon nitride (Si_3N_4) or silicon dioxide (SiO_2) is deposited at the bottom portions of holes 38. *Supra* XI.A.12.a; *Kuboi*, ¶¶[71]-[73].

203. As part of the next step of the manufacturing process and as shown below, *Kuboi* discloses that an organic material is deposited to fill the remaining portions of the holes, thereby forming organic photoelectric conversion films 13 embedded within the hole. *Kuboi*, ¶¶[73], [58], [85], Fig. 4C.

FIG.4C



Kuboi, Fig. 4C.

204. *Kuboi* discloses that "[a]s the p-type organic material sensitive to a visible light region, perylene-based compounds, phthalocyanine compounds, quinacridone compounds, porphyrin compounds, merocyanine compounds, and the like can be used, for example." *Kuboi*, ¶[58].

205. In my opinion, a person of ordinary skill would have recognized that phthalocyanine compounds, perylene-based compounds, and porphyrin compounds function as dielectric materials. Various prior art references examine their dielectric properties and behavior in optoelectronic devices. For instance, Exhibit

1021 discusses the dielectric characteristics of phthalocyanine and perylene compounds used in organic solar cells. Ex. 1021, 3, 17, 47, 52-56. Additionally, Exhibit 1022, 1-4, 7, explores the dielectric behavior of phthalocyanine compounds, noting that their dielectric constant decreases with increasing frequency and rises with increasing temperature. Exhibit 1034, 4-11, presents experimental studies on porphyrin as a dielectric material, while Exhibit 1035, 1-6, details dielectric investigations of porphyrin compounds used in optical devices. Exhibit 1036, 1-6, discusses the measurement of photocurrents generated by illuminating a porphyrin compound, alongside its dielectric property evaluations. Exhibit 1037, 1, explains that the dielectric properties of phthalocyanine compounds increase with temperature and decrease with frequency. Lastly, Exhibit 1038, 1-5, describes perylene compounds as organic dielectric materials with "high photoluminescence efficiency," employed in solar cells.

206. Thus, both electron blocking film 21 and organic photoelectric conversion film 13 that together entirely fill the holes of photoelectric conversion portion 14 are dielectric materials. Accordingly, *Kuboi*'s holes are entirely filled with a dielectric material.

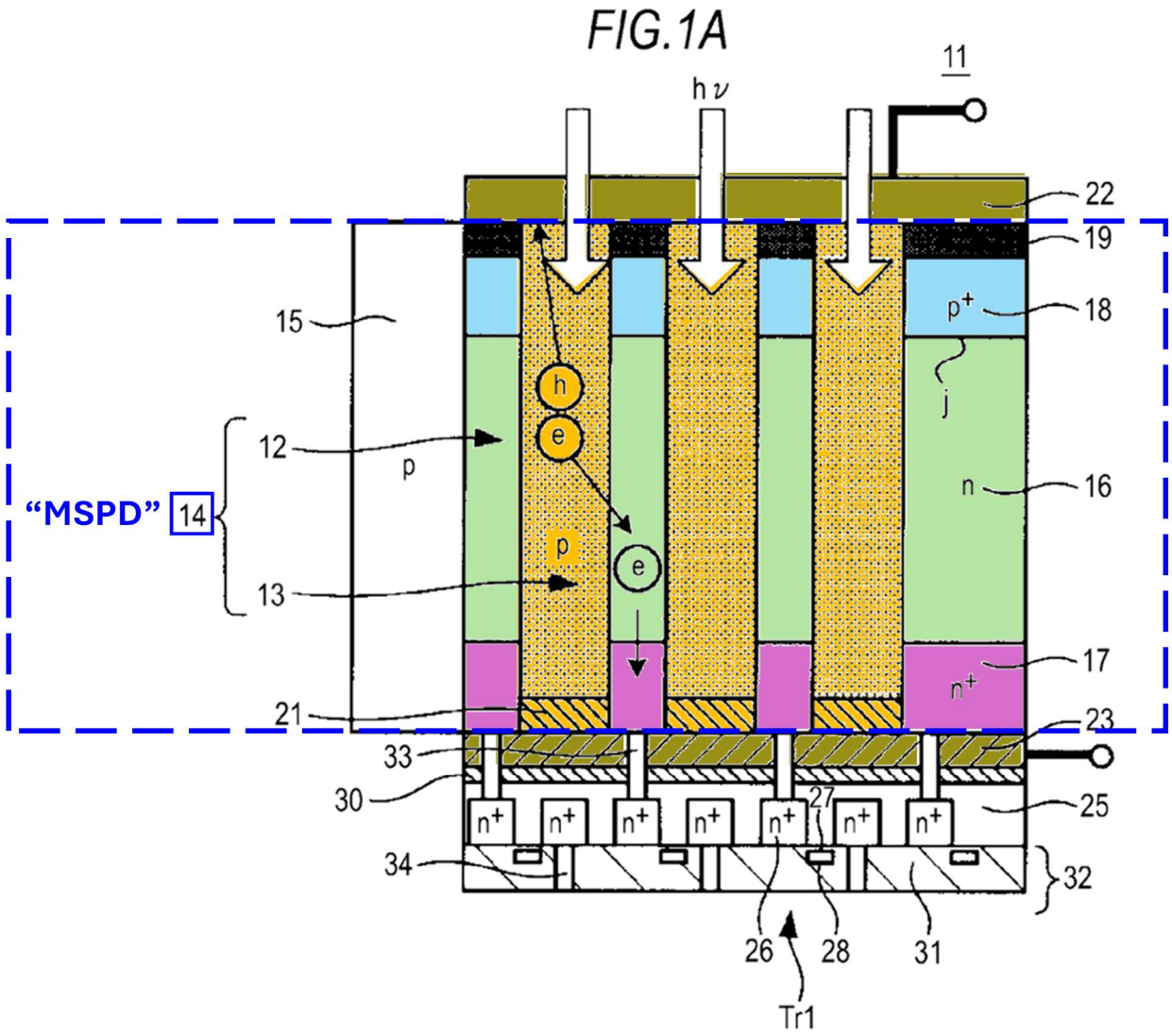
207. Notably, consistent with *Kuboi*'s disclosure, the '543 Patent acknowledges that a hole filled with a dielectric material can be filled with multiple dielectric materials. For example, the '543 Patent discloses that "holes

1916 can be partially filled, and/or completely filled with another dielectric(s) and/or amorphous semiconductor and can be multiple layers." '543 Patent, 30:64-67. It also discloses that "microstructure holes are passivated and filled fully and/or partially with dielectrics." '543 Patent, 104:28-31.

14. Claim 24

a. [24]: "The single-chip device of claim 1, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD."

208. In my opinion, *Kuboi* discloses this additional limitation. As detailed for claim [1h], photoelectric conversion portion 14 includes upper electrode 22 on its upper surface and lower electrode 23 on its lower surface that are configured for reverse-biasing photoelectric conversion portion 14. *Supra* XI.A.1.k; *Kuboi*, ¶¶[60], [64], [77], Fig. 1A. These electrodes are shown below:



Kuboi, Fig. 1A.

209. Lower electrode 23 "is formed of metal exhibiting ohmic properties." *Kuboi*, ¶[60]. Meanwhile, an indium tin oxide (ITO) film serves as upper electrode 22. *Kuboi*, ¶[60].

210. In my opinion, a person of ordinary skill would have understood that an electrode made of ITO establishes ohmic contact and thus comprises ohmic

contacts. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. Ex. 1023, Abstract ("ITO contact with p-type silicon semiconductor is a robust ohmic contact for Si[-]based optoelectronic devices."); Ex. 1024, 3 ("[F]ormation of ohmic contact on a p-type doped c-Si at room temperature has been … achieved."); Ex. 1025, 1 (discussing the use of ITO as an ohmic contact for an optoelectronic component).

211. This is also consistent with the '543 Patent, which acknowledges that ITO makes ohmic contact. For example, the '543 Patent explains that an "ohmic contact" can include a "transparent conducting metal oxide such as indium tin oxide (ITO)." '543 Patent, 39:20-26. As a result, in my opinion, both upper electrode 22 and lower electrode 23 are ohmic contacts, as claimed.

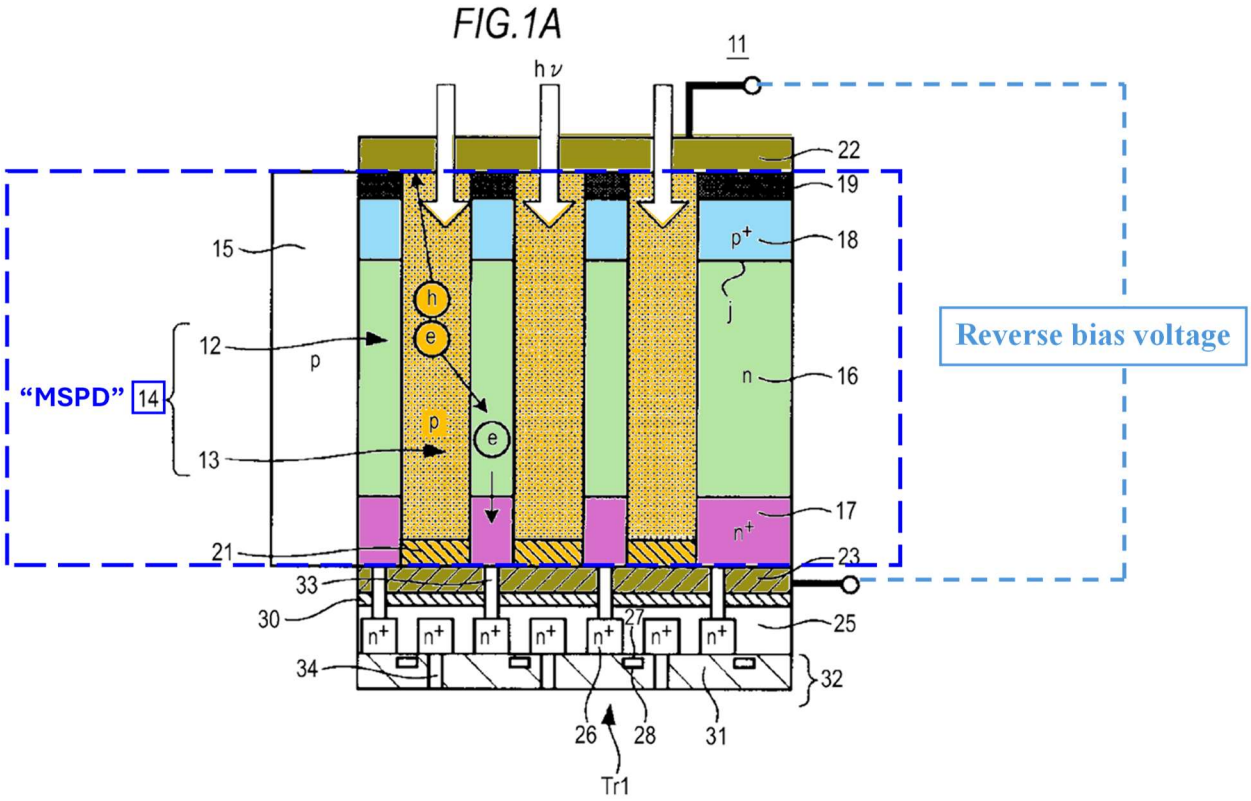
15. Claim 25

a. [25]: "The single-chip device of claim 1, in which the MSPD further includes ohmic contacts to said first and second regions, at least one of said ohmic contact[s] being through a via in said substrate."

212. In my opinion, *Kuboi* renders obvious this additional limitation. As explained for claim [24], upper electrode 22 and lower electrode 23 are ohmic contacts. *Supra* XI.A.14.a. These ohmic contacts meet each limitation of claim 25.

213. Electrodes 22, 23 make contact with each of the "first and second regions," as claimed. Upper electrode 22 is formed over the entire upper surface of

photoelectric conversion portion 14 on top of light shielding film 19, which is made of tungsten. *Kuboi*, ¶¶[59]-[60], [77].



Kuboi, Fig. 1A.

214. In my opinion, a person of ordinary skill would have understood that tungsten is an electrically conductive material. Ex. 1019, 21-22 (discussing the use of tungsten as the first level metal and contact plugs of IC devices); Ex. 1020, 14-15. Consequently, upper electrode 22 makes ohmic contact with p^+-type region 18. Lower electrode 23 is formed over the entire lower surface of photoelectric conversion portion 14, covering the back surface of n^+-type region 17. *Kuboi*,

¶¶[59]-[60], [77], Fig. 1A. Therefore, lower electrode 23 makes ohmic contact with n^+-type region 17.

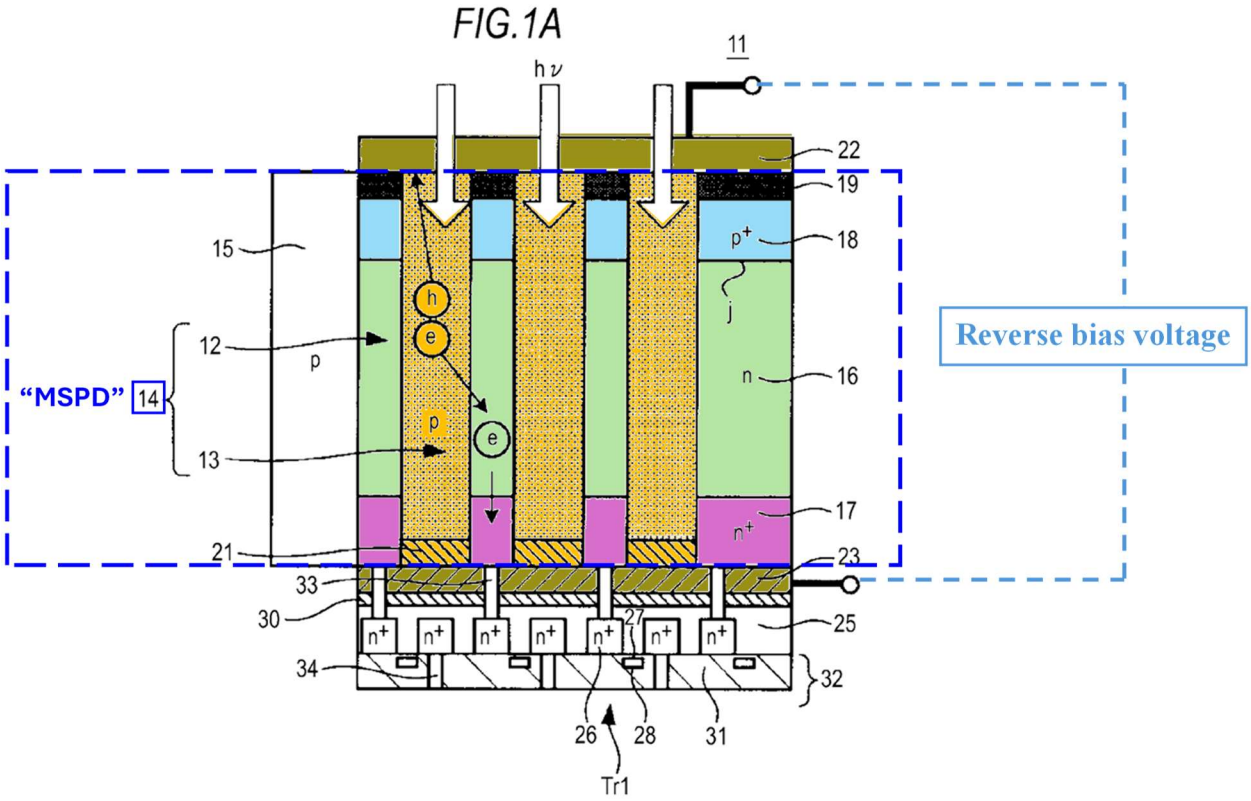
215. *Kuboi* further teaches and renders obvious that "at least one of said ohmic contact[s] [is] through a via in said substrate," as claimed. In *Kuboi*'s imaging device 201, pixels 11 (with photoelectric conversion portion 14) and the peripheral circuit portion are formed on substrate 211. *Kuboi*, ¶¶[48], [78]; *supra* XI.A.1.b (claim [1pre(b)]). Subsequently, a different substrate with pixel transistors Tr1 and lower electrode 23 formed on its top surface is bonded to the lower surface of substrate 211. *Kuboi*, ¶¶[70], [78]; *see Kuboi*, Fig. 15. These two substrates are bonded such that the photoelectric conversion portions 14 on substrate 211 connect to the n-type charge accumulation regions 26 of corresponding pixel transistors Tr1 via conductors 33 that penetrate through the lower electrode 23. *Kuboi*, ¶¶[48], [62].

216. In my opinion, a person of ordinary skill, however, would have been motivated to fabricate photoelectric conversion portions 14 and the pixel transistors on the same substrate 211. Given that an exemplary pixel in *Kuboi* measures approximately 1.4 µm x 1.4 µm, *e.g.*, *Kuboi*, ¶¶[94], [122], [145], a person of ordinary skill would have recognized that challenges in spatially aligning the conductors 33 with the photoelectric conversion portions 14 during substrate bonding reduce the yield of the bonding process. *See* Ex. 1039, 5-6, 8-9, 11-13. A

person of ordinary skill would have understood that fabricating photoelectric conversion portions 14 and the pixel transistors on the same substrate 211 would eliminate the need for aligning the electrodes 33 and thereby increase yield. This is supported by at least *Shinohara*. *Shinohara*, ¶¶[58], [81].

217. Integrating signal processing circuits on the same substrate as photodetectors was well known and beneficial. Such integration was known to lower costs and improve fabrication reliability. Ex. 1029, 1; Ex. 1030, 1-2. Consequently, a person of ordinary skill would have found it obvious to fabricate *Kuboi*'s photoelectric conversion portions 14 and pixel transistors Tr1 on substrate 211 to simplify fabrication and reduce costs. Additionally, methods for fabricating photoelectric conversion portions and pixel transistors on the same substrate were well established, including in references such as *Shinohara*. *Shinohara*, ¶¶[68]-[89]. This is also consistent with the '543 Patent, which acknowledges that integrating photodetectors with signal processing circuits on the same substrate was a common practice to reduce costs and enhance performance. '543 Patent, 28:58-29:3, 32:50-67, 47:11-21. Thus, in my opinion, a person of ordinary skill would have had the motivation, requisite skill, and reasonable expectation of success in fabricating photoelectric conversion portions 14 and pixel transistors on substrate 211.

218. When the pixel transistors Tr1 are fabricated on substrate 211, as illustrated below, lower electrode 23 is positioned within substrate 211.



Kuboi, Fig. 1A.

219. As explained for claim [1h], a reverse bias is applied to photoelectric conversion portion 14 via upper and lower electrodes 22, 23. *Supra* XI.A.1.k. In my opinion, a person of ordinary skill would have understood that an electrical connection (to apply the "necessary voltage" for biasing, *see Kuboi*, ¶[64]) to lower electrode 23 positioned within substrate 211 is made using "vias." This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. *See* Ex. 1020, 13 (Fig. 2.21), 18 (explaining that

"a [v]ia gives an electrical connection between Metal1 and Metal2 lines"); Ex. 1018, 7 (defining "via" as "a hole in the insulator between two metal layers on a multilayer integrated circuit that is etched and filled with a conducting material so that the two metal layers are electrically connected").

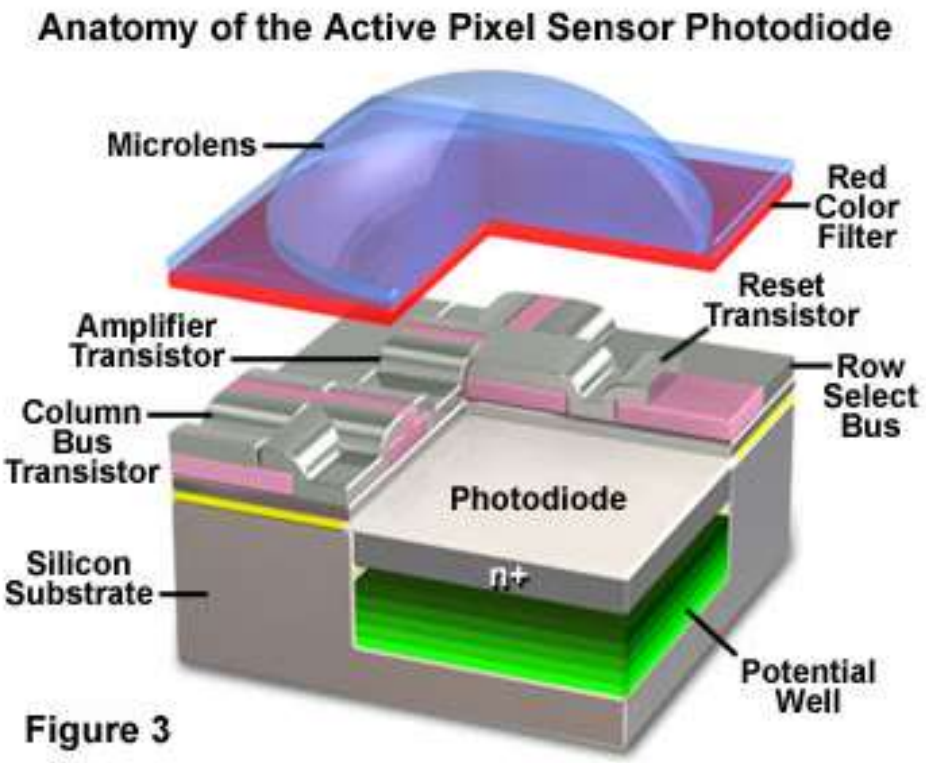
220. In addition, in my opinion, a person of ordinary skill would have also been motivated to implement vias in substrate 211 for electrical connection to lower electrode 23 so that a "necessary voltage" can be applied to this electrode for biasing photoelectric conversion portion 14. *See Kuboi*, ¶[64]. In *Kuboi*, conductors 33 extend through vias on semiconductor region 25 of the substrate to interconnect the pixel transistors to photoelectric conversion portions 14. *See Kuboi*, ¶[62], Fig. 1A. Given that "vias" are conventional components commonly used in similar devices for electrical connections through substrates and that *Kuboi* already incorporates electrical connections through the substrate, a person of ordinary skill would have also had a reasonable expectation of success in using "vias" through substrate 211 to provide electrical connection to lower electrode 23. Therefore, it would have been obvious to a person of ordinary skill that, in *Kuboi*, electrical contact to lower electrode 23 will be made through a "via," as claimed.

16. Claim 26

a. [26a]: "The single-chip device of claim 1, further comprising a light guide to said MSPD for directing said optical input thereto,"

221. In my opinion, *Kuboi* discloses this additional limitation. *Kuboi* discloses that, although not depicted in the drawings, "an on-chip microlens" ("light guide") is formed on upper electrode 22, allowing light to pass through this microlens to reach photoelectric conversion films 13 of photoelectric conversion portion 14, where the light undergoes photoelectric conversion. *Kuboi*, ¶¶[63]-[64].

222. A person of ordinary skill would recognize that the on-chip microlens is a light guide, directing light to the photoelectric conversion portion 14. This is supported by other prior art that demonstrates what would have been known to a person of ordinary skill in the art. For instance, Exhibit 1015 describes a CMOS image sensor with a two-dimensional array of photodiodes (or pixels) with a microlens formed over each photodiode. Ex. 1015, 2-4. This is shown below:



Ex. 1015, Fig. 3.

223. The microlens "serves to focus incident light directly into the photosensitive area of the photodiode." Ex. 1015, 3. Similarly, Exhibit 1027 explains with reference to Fig. 2(a) and 2(b) below, that a functional pixel is comprised of several elements (as detailed in Fig. 2(a)), and that "[i]ncident light first passes through a plano-convex microlens to help focus the light in the center of the pixel." Ex. 1027, 4.

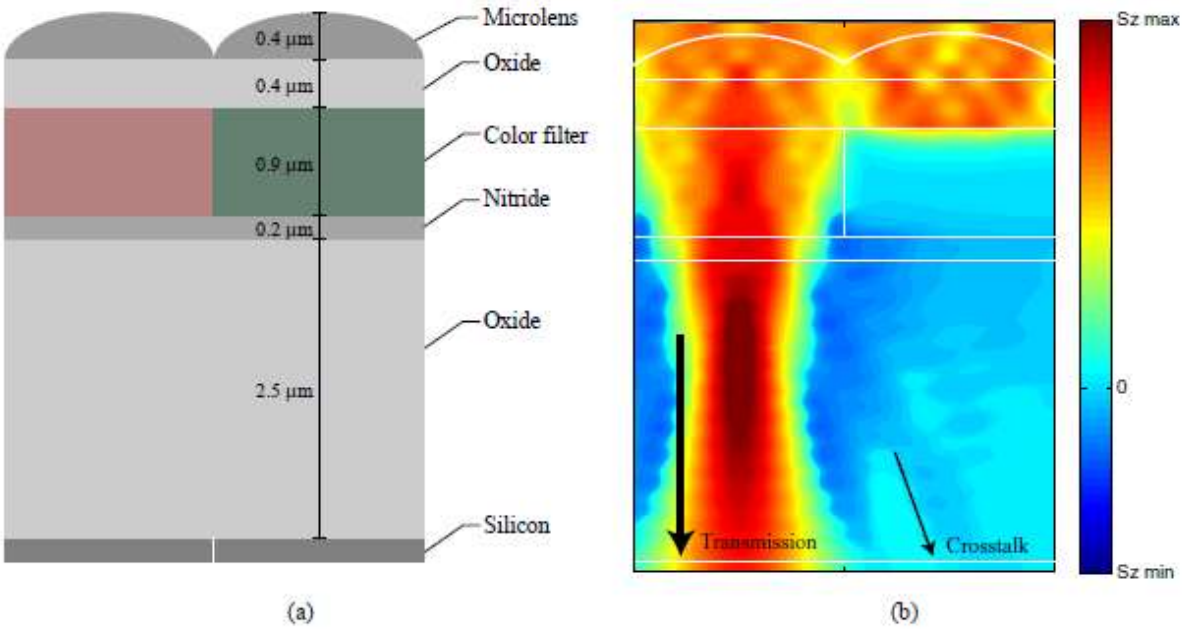
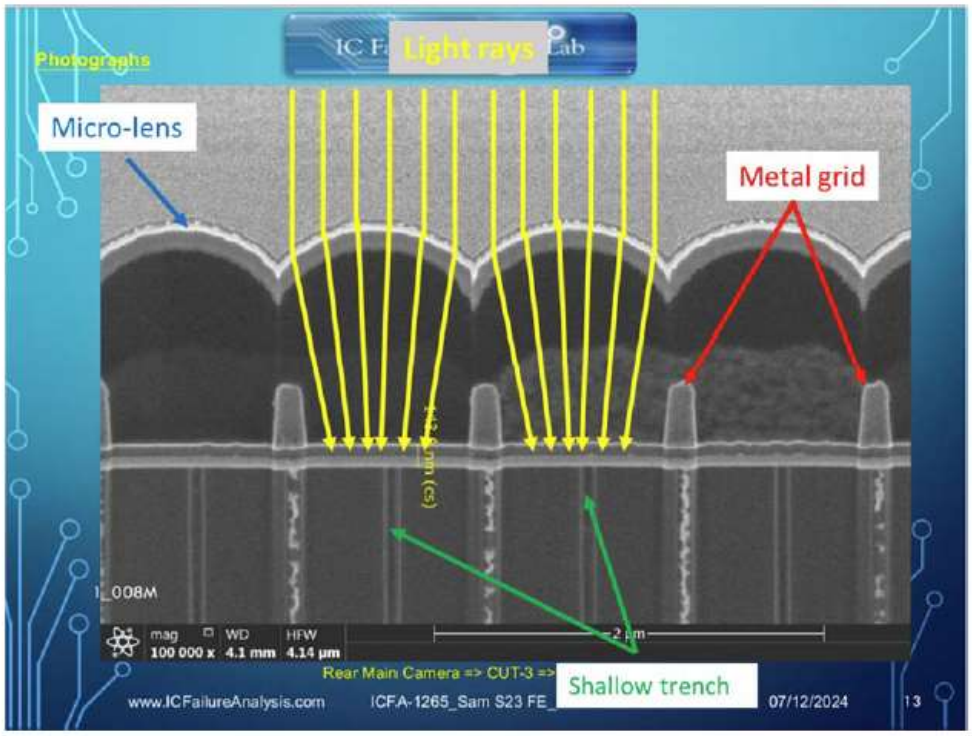


Fig. 2. (a). Two-dimensional (2D) pixel model with layer materials and thicknesses. (b). Electromagnetic field simulation result showing energy flow toward the photodiode (z-component of the Poynting vector, S_z) with significant diffraction effects, reducing optical efficiency (transmission) and leading to spatial crosstalk even at normal incidence.

Ex. 1027, 4.

224. Thus, in my opinion, a person of ordinary skill would have understood that *Kuboi*'s on-chip microlens operates a light guide that directs light to photoelectric conversion portion 14.

225. This is also consistent with Patent Owner's infringement contentions in the parallel litigation. For instance, referring to the annotated figure shown below, Patent Owner asserts that "[t]he micro-lens directs the input light toward the center of the MSPD, thereby guiding the light." Ex. 1046, 38; *see also* Ex. 1047, 36.



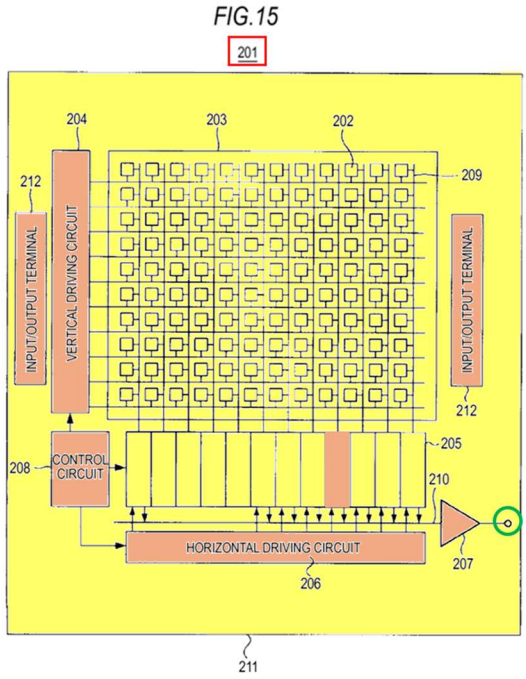
WWSENS004710-WWSENS004753 at 4723 (annotated to illustrate the effect of the mu-lenses to focus the light rays to the MSPDs).

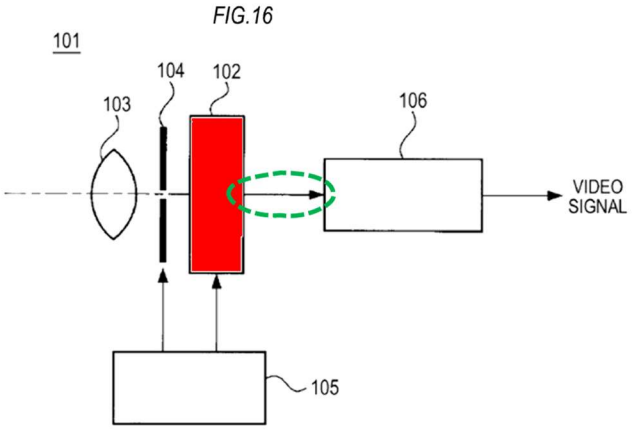
Ex. 1046, 38.

b. [26b]: "and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip device."

226. In my opinion, *Kuboi* discloses and renders obvious this additional limitation. As explained for claim [1pre(a)], the "active electronic circuit" of *Kuboi*'s imaging device 201 includes vertical driving circuit 204, column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208. *Supra* XI.A.1.a; *Kuboi*, ¶¶[48]-[49]. *Kuboi* discloses that output circuit 207 "outputs the processed signals" from imaging device 201. *Kuboi*, ¶[54]. *Kuboi* discloses that its imaging device (labelled 102 in Figure 16) can be

integrated into various apparatuses (e.g., cameras, mobile phones) with an external signal processing circuit 106, as illustrated below:





Kuboi, Figs. 15, 16; *Kuboi*, ¶¶[191]-[193].

227. When used in an apparatus above, output circuit 207 sends the processed signals to the external signal processing circuit 106. *Kuboi*, Fig. 16. In my opinion, a person of ordinary skill would have understood that output circuit 207 would require electrical contacts to interconnect it with external signal processing circuit 106, allowing the processed signals to be transferred from imaging device 201 to external processing circuit 106. *Kuboi*, ¶[192]. Additionally, *Kuboi* discloses that imaging device 201 includes "[a]n input/output terminal 212

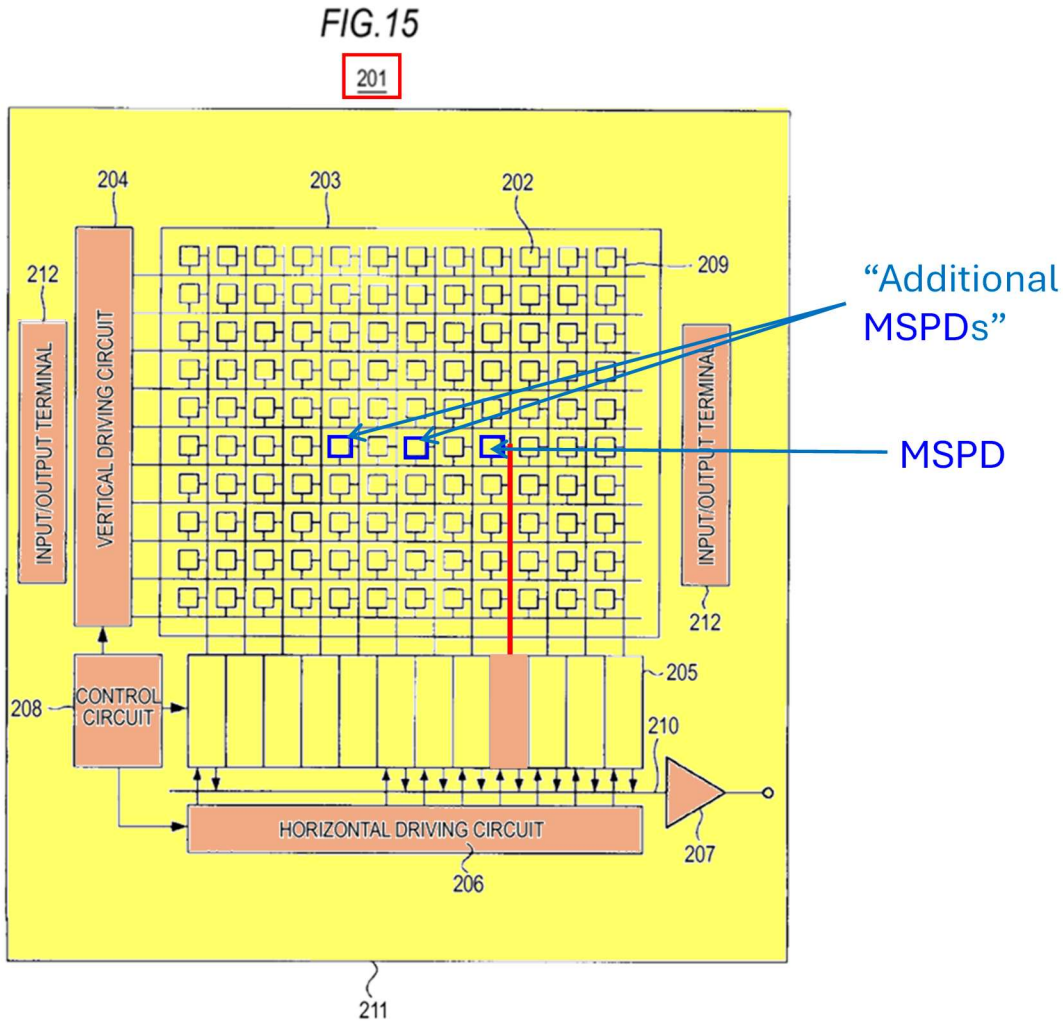
[to] exchange[] signals with an external device." *Kuboi*, ¶[54]. *Kuboi* thus discloses this limitation.

228. A person of ordinary skill would have also found it obvious to incorporate electrical contacts in *Kuboi*'s imaging device 201 to transfer processed signals from output circuit 207 to external signal processing circuitry, given that the use of such contacts was well known in CMOS solid-state integrated circuit devices. Ex. 1016, 1-3. Since the use of electrical contacts to output signals from CMOS devices was well known and *Kuboi* discloses exchanging signals with an external device, a person of ordinary skill would have been motivated to include electrical contacts in imaging device 201 and would have had a reasonable expectation of success in implementing this modification.

17. Claim 28

a. [28a]: "The single-chip device of claim 1, further comprising one or more additional MSPD on or in the same substrate,"

229. In my opinion, *Kuboi* discloses this additional limitation. Imaging device 201 ("single-chip device") includes a plurality of pixels 202, each with a photoelectric conversion portion 14, arranged in a two-dimensional array on the same substrate 211 (addressing how each MSPD is formed on or in substrate 211). *Kuboi*, ¶[48], Fig. 15; *supra* XI.A.1.b (claim [1pre(b)]).



Kuboi, Fig. 15.

230. Imaging device 201 includes multiple pixels 11 with photoelectric conversion portions 14 ("MSPD" of claim 1 and "additional MSPD[s]" of this claim). *Kuboi*, ¶¶[48],[55].

231. For instance, as illustrated below, *Kuboi* describes an embodiment where four pixels—blue pixel 53B, red pixel 53R, and two green pixels 53G—are arranged in a two-dimensional Bayer pattern:

FIG.6A

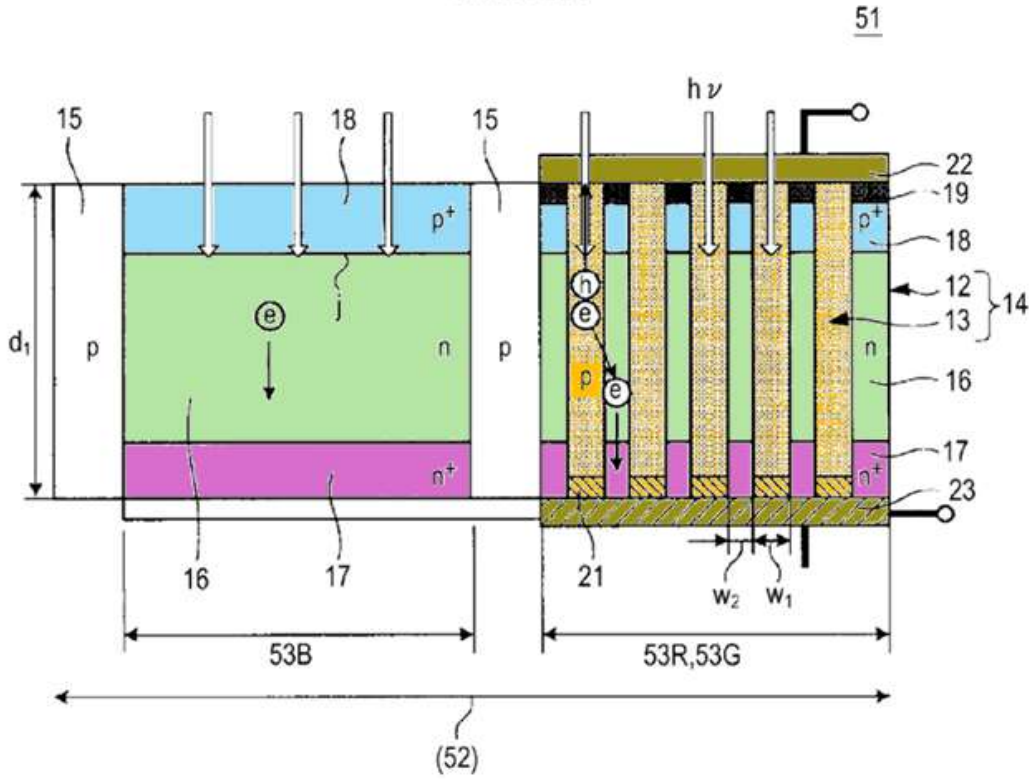
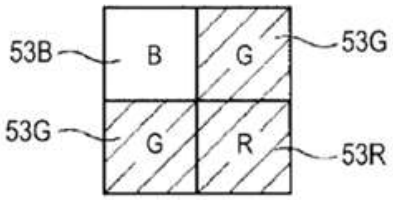


FIG.6B



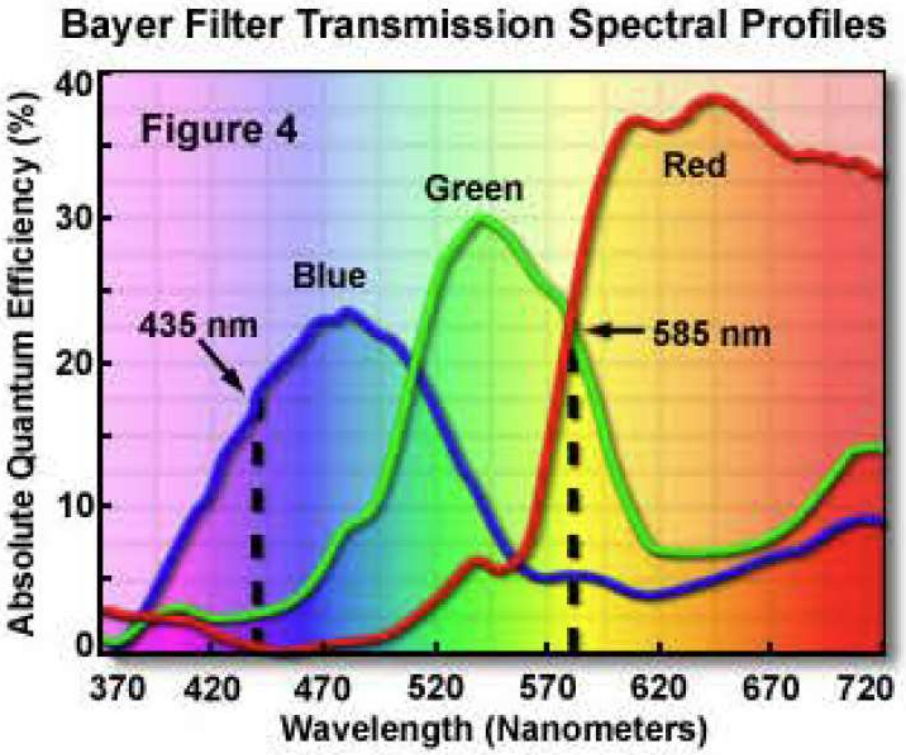
Kuboi, Figs. 6A-6B, ¶[90].

232. Red pixel 53R and green pixels 53G "are formed by the hybrid photoelectric conversion portion 14 shown in FIGS. 1A and 1B." *Kuboi*, ¶[90]. *Kuboi* teaches incorporating this pixel grouping into the imaging device 201. *Kuboi*, ¶¶[48], [90]. Thus, *Kuboi*'s imaging device 201 includes multiple pixels 11

(e.g., one red pixel 53R and two green pixels 53G) with photoelectric conversion portions 14 (MSPD) on or in substrate 211.

b. [28b]: "and respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input."

233. *Kuboi* discloses this additional limitation. The four pixels (blue pixel 53B, red pixel 53R, and two green pixels 53G), which each include their own MSPD, also include corresponding color filters and on-chip microlenses in a Bayer arrangement formed over the pixels' upper electrodes 22. *Kuboi*, ¶¶[90], [93]. Each color filter is an optical bandpass filter that allows light at a specific band of wavelengths (or "wavelength band") corresponding to the filter color to pass through (while blocking other wavelengths). *Kuboi*, ¶[92] ("red wavelength band," "green wavelength band"); Ex. 1015, 4-5. For example, as shown below, red, green, and blue color filters each have different wavelength bands:



Ex. 1015, 4.

234. Thus, photoelectric conversion portions 14 of red pixel 53R and green pixels 53G are coupled to different optical bandpass filters.

235. In my opinion, red pixel 53R and green pixels 53G are designed to respond to different wavelength ranges that are within the incident light ("optical input"). For instance, photoelectric conversion films 13 of red pixel 53R are composed of a material "sensitive to [the] red wavelength band," while the films 13 of green pixels 53G are made of a material "sensitive to [the] green wavelength band." *Kuboi*, ¶[92]. The red and green wavelength bands represent different wavelength ranges. *See* Ex. 1015, 4. Thus, films 13 of red pixel 53R convert the

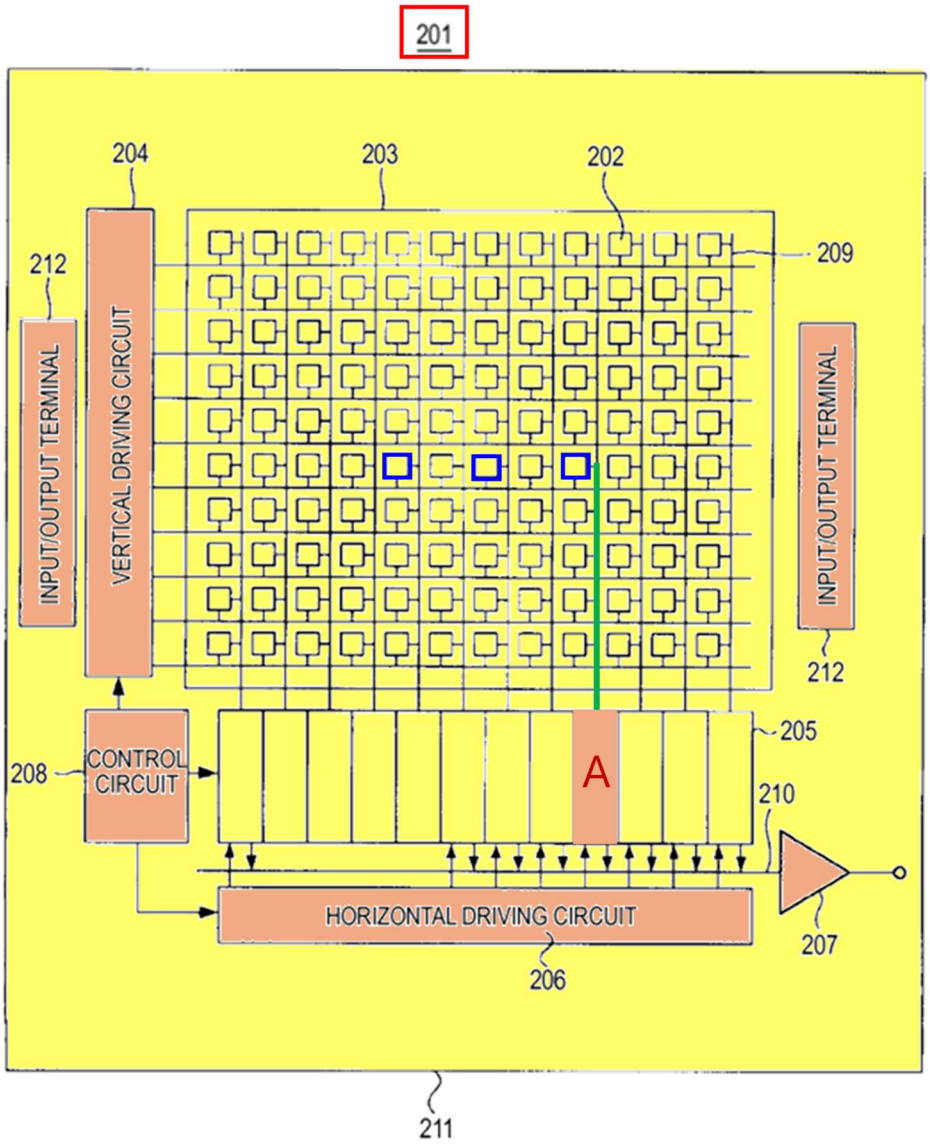
red wavelength range in the incident light into electrical output, while films 13 of green pixels 53G convert the green wavelength range in the incident light into electrical output.

18. Claim 29

a. [29]: "The single-chip device of claim 1, further comprising one or more additional MSPDs on or in said single substrate, one or more additional active electronic circuits on or in the said single substrate, and one or more additional communication channels configured to supply electrical outputs from the MSPDs to the one or more of the active electronic circuits."

236. In my opinion, *Kuboi* discloses this additional limitation. As detailed for claim [28a], imaging device 201 comprises multiple MSPDs on or in substrate 211. *Supra* XI.A.17.a. As also explained for claims [1pre(a)] and [1pre(b)], *Kuboi*'s active electronic circuit (which includes vertical driving circuit 204, a column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208) is on or in substrate 211. *Supra* XI.A.1.a, XI.A.1.b; *Kuboi*, ¶¶[48]-[49], [78], Fig. 15. As explained for claim [1n], imaging device 201 includes a communication channel (vertical signal line 209) that supplies the electrical output from a pixel 11 to a column signal processing circuit 205. *Supra* XI.A.1.p. These components are shown below:

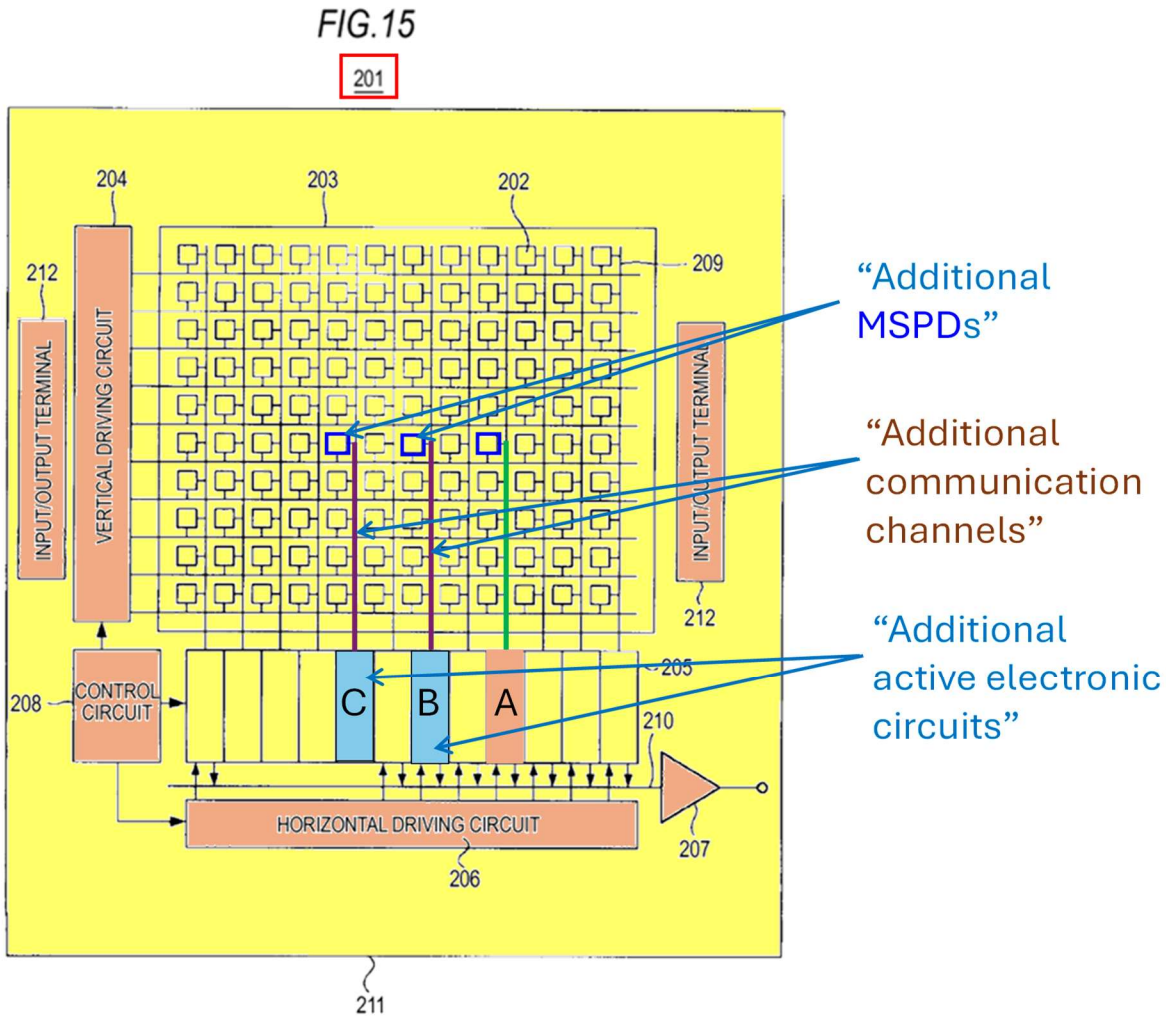
FIG.15



Kuboi, Fig. 15.

237. In addition to column signal processing circuit 205 of the claimed active electronic circuit (marked A in the figure above), the peripheral circuit portion includes multiple column signal processing circuits 205 provided "for each column of the pixels 202 and perform signal processing such as noise removal for each pixel column on signals output from pixels 202 of one row." *Kuboi*, ¶[52].

Vertical driving circuit 204 activates pixels in a selected row and supplies the electrical output from each pixel (including pixels 11) to a corresponding column signal processing circuit 205 through a vertical signal line 209. *Kuboi*, ¶¶[51]-[52]; *supra* XI.A.1.c (claim [1pre(c)]). This is shown below:



Kuboi, Fig. 15.

238. Thus, the electrical output from the first pixel 11 (and MSPD) is directed to a first signal processing circuit 205 (marked A) via a signal line 209,

the electrical output from a second pixel 11 is routed to a second signal processing circuit 205 (marked B) via a second signal line 209, the electrical output from a third MSPD is conveyed to a third signal processing circuit 205 (marked C) via a third signal line 209, and so on. *Kuboi*, ¶¶[51]-[52].

239. The MSPD associated with the first pixel 11 is the "MSPD" of claim 1, while the MSPDs associated with the second and third pixels 11 are the "additional MSPDs" of this claim. The first signal processing circuit 205 (A) constitutes part of the "active electronic circuit" of claim 1, whereas the second and third signal processing circuits 205 (B and C) are the "additional active electronic circuits" of this claim. Similarly, signal line 209 is the "communication channel" of claim 1, and the signal lines 209 are the "additional communication channels" of this claim. As explained for claims [1pre(a)] and [1pre(b)], all logic circuits of the peripheral circuit portion (including signal processing circuits B and C) are "active" electronic circuits comprising transistors, and all pixels and logic circuits of the peripheral circuit portion of imaging device 201 are formed on or in substrate 211. *Supra* XI.A.1.a, XI.A.1.b.

19. Claim 30

a. [30]: "The single-chip device of claim 1, further comprising one or more additional active electronic

circuits that are formed on or in the said single substrate."

240. In my opinion, *Kuboi* discloses this additional limitation. As explained for claim [29], the one or more additional active electronic circuits (signal processing circuits 205 B and C) are formed on or in substrate 211 of imaging device 201. *Supra* XI.A.1.a (claim [1pre(a)]), XI.A.1.b (claim [1pre(b)], XI.A.18.a (claim [29]); *Kuboi*, ¶[52].

20. Claim 32

a. [32]: "The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate and comprise one or more of CMOS, BiCMOS, and bipolar active devices."

241. In my opinion, *Kuboi* discloses this additional limitation. As explained for claim [29], the one or more additional active electronic circuits (signal processing circuits 205 B and C) are formed on or in substrate 211. *Supra* XI.A.1.a (claim [1pre(a)]), XI.A.1.b (claim [1pre(b)], XI.A.18.a (claim [29]); *Kuboi*, ¶[52].

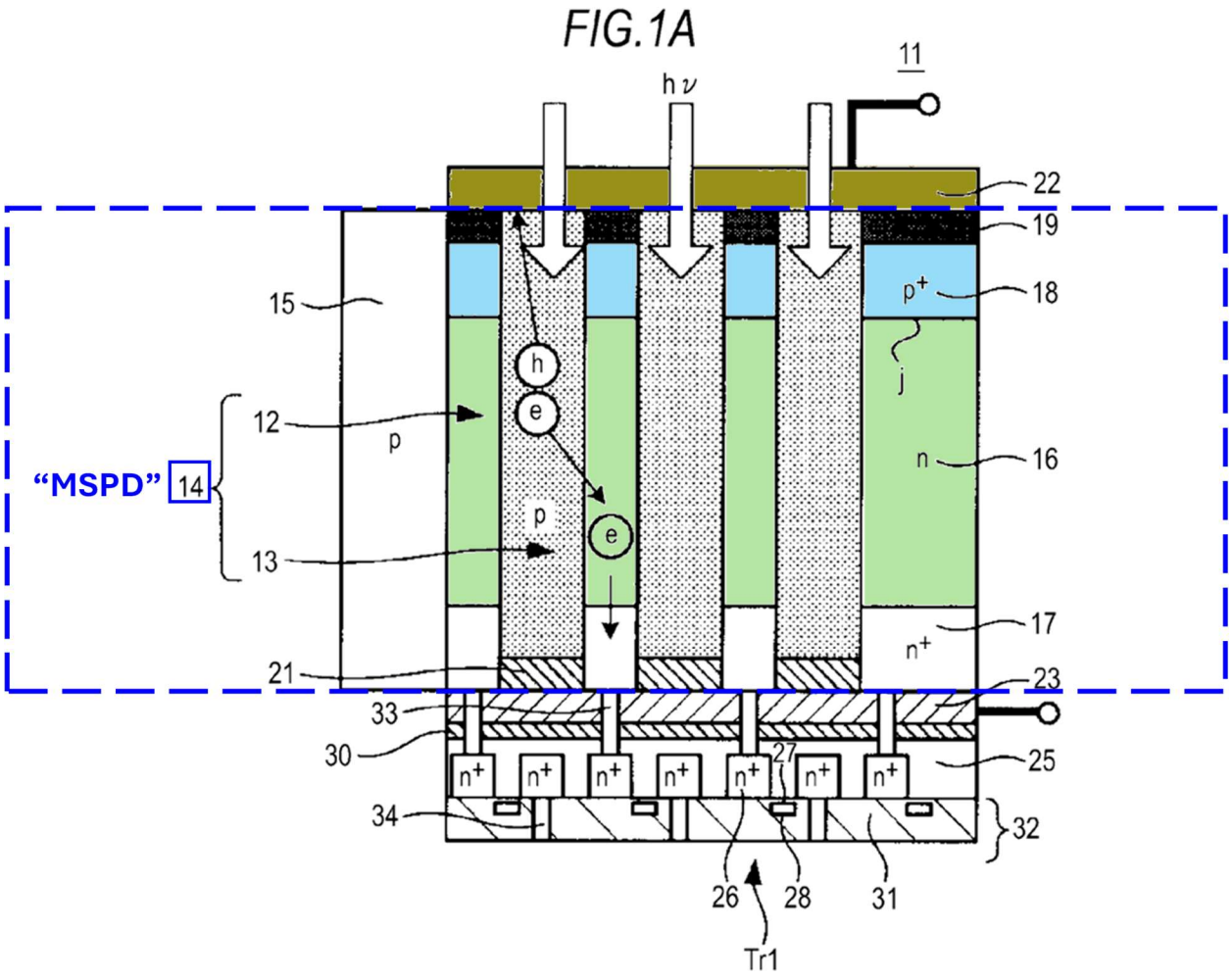
242. *Kuboi* further discloses that imaging device 201 is a "CMOS solid-state imaging device" fabricated using "existing CMOS techniques." *Kuboi*, ¶¶[3], [7], [48], [55]. A person of ordinary skill would have understood that, in a CMOS solid-state device fabricated using existing CMOS fabrication techniques, all logic

circuits of the peripheral circuit portion (including the active electronic circuit and the additional active electronic circuits) would be CMOS active devices.

21. Claim 35

a. [35]: "The single-chip device of claim 1, further including a region of selected material that is over a side of one of the first and second regions facing away from the intermediate region and is configured to reduce sheet resistance."

243. In my opinion, *Kuboi* discloses this additional limitation. As shown below, a transparent upper electrode 22 ("selected material") which is made of indium tin oxide (ITO), covers the entire light incident side of pixel 11's photoelectric conversion portion 14. *Kuboi*, ¶¶[60], [93], Fig. 1A.



Kuboi, Fig. 1A.

244. Light enters photoelectric conversion portion 14 through transparent upper electrode 22. *Kuboi*, ¶¶[60], [64]. In my opinion, a person of ordinary skill would have understood that upper electrode 22 is formed over a side (the light incident side) of p^+-type region 18 ("first layer"), which faces away from n-type region 16 ("intermediate layer"). *See Kuboi*, Fig. 1A.

245. A person of ordinary skill would also have understood that an ITO film reduces sheet resistance. *Higuchi* demonstrates what would have been known to a person of ordinary skill in the art. For example, *Higuchi* explains that an ITO film on a photoelectric conversion device decreases the sheet resistance of the device due to the low sheet resistance of ITO. *Higuchi*, ¶¶[16]-[17]. Consistent with this established knowledge, the '543 Patent recognizes that the presence of an ITO layer on a photodiode reduces sheet resistance. '543 Patent, 27:56-59 ("Layer 1450 is a thin ITO like material … that can be deposited on the P and/or N layer(s) to reduce the sheet resistance of these layers."), 29:42-45 ("transparent conducting metal oxide may be used to reduce the sheet resistance"). In my opinion, *Kuboi*'s upper electrode 22 is thus "configured to reduce sheet resistance," as claimed.

XII. CONCLUSION

246. For the reasons set forth above, it is my opinion that one skilled in the art would have found claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 of the '543 Patent anticipated by or obvious over the prior art. My opinion would remain the same even if the level of skill in the art was slightly lower (e.g., requiring only a bachelor's degree instead of a master's degree).

247. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be

subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

248. I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001.

Date: Wednesday, May 14, 2025

By: 

Michael Lebby