

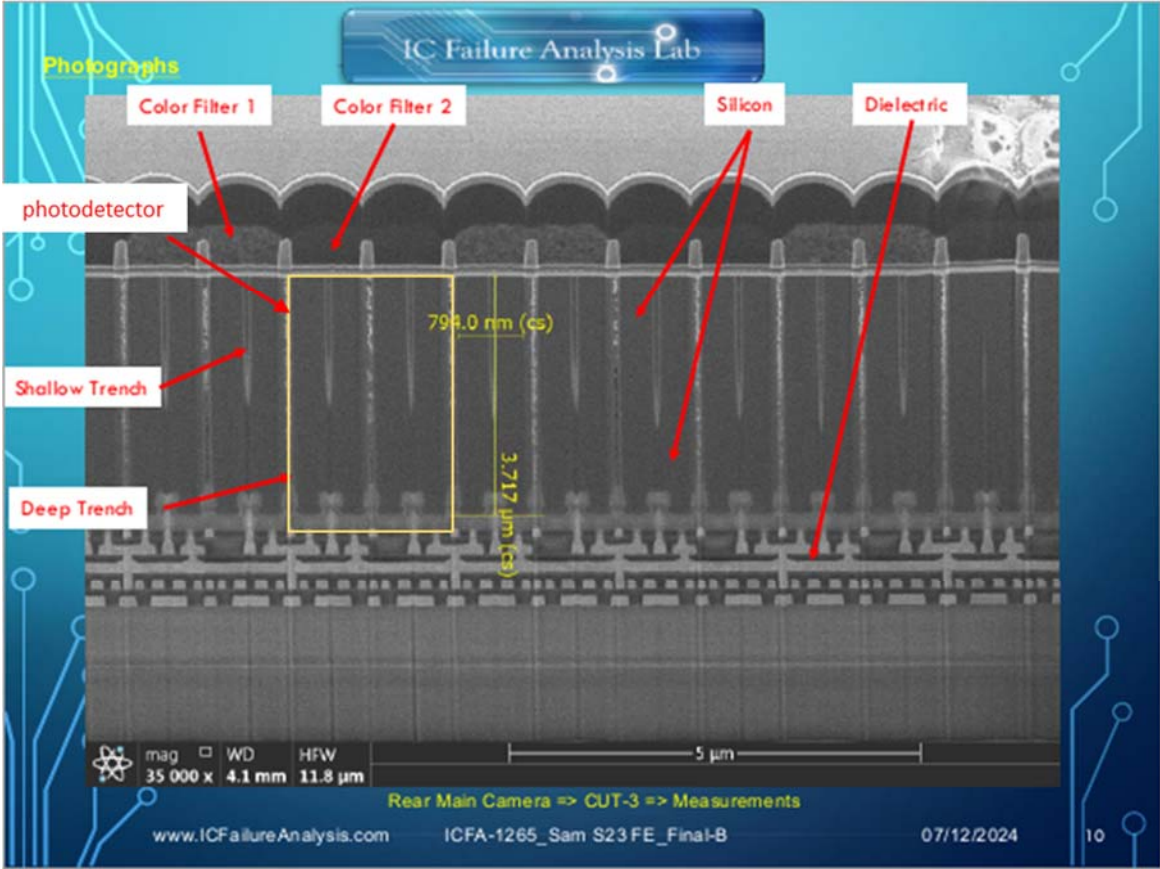
# **APPENDIX C-2**

**C-2: The CIS Accused Products with the RGB Bayer Feature Infringe the Asserted Claims of U.S. Patent No. 10,468,543 (the “’543 Patent”)**

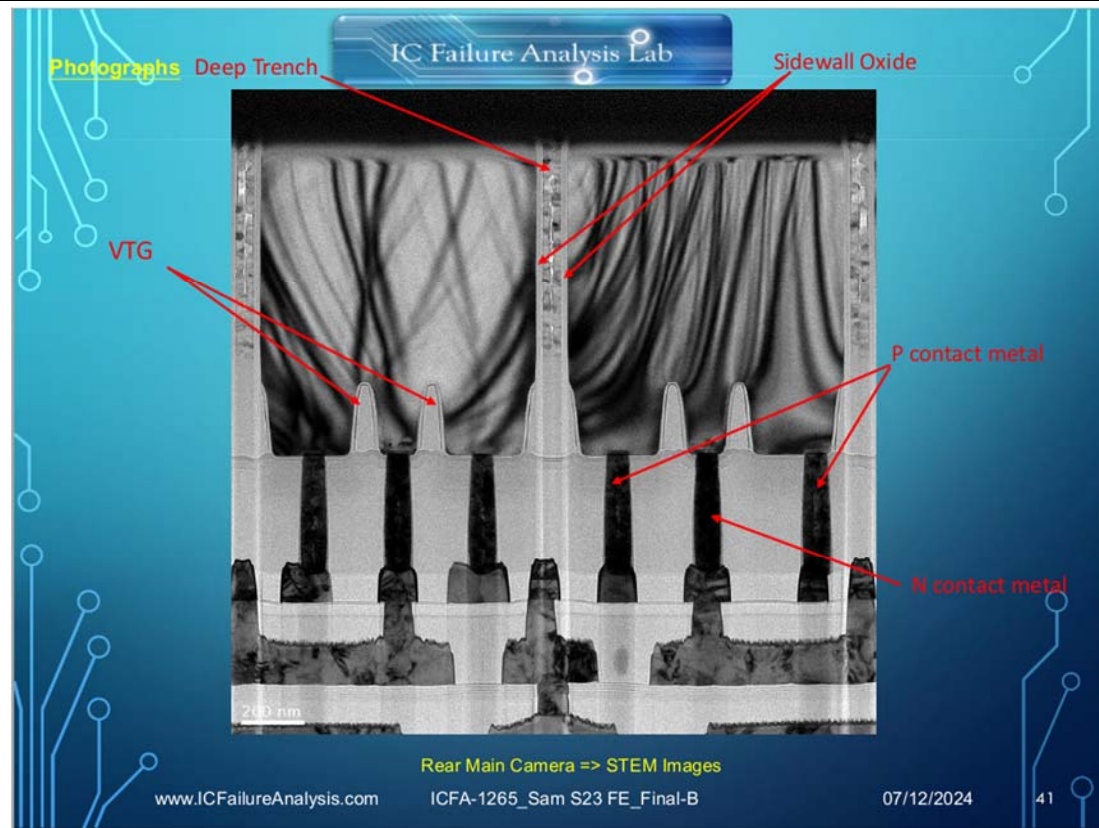
W&W provides the following chart pursuant to Patent Local Rule 3-1(c) regarding infringement of the Asserted Claims of the ’543 Patent, i.e., Claims 1, 3, 7, 9, 10, 16, 20, 24, 26, 28, 29, 30, and 32, by Samsung’s CIS Accused Products with the RGB Bayer feature, as defined and described in W&W’s infringement contentions cover disclosure to which this chart is appended (“Cover Disclosure”).

CIS Accused Products as used in this chart refers to all CIS Accused Products with the RGB Bayer feature, including the following Samsung ISOCELL models, as described in Section II of the Cover Disclosure: HP2 (S5KHP2), HPX (S5KHPX), HP3 (S5KHP3), HP1 (S5KHP1), HM6 (S5KHM6), HM3 (S5KHM3), HM2 (S5KHM2), HMX (S5KHMX), HM1 (S5KHM1), GWB (S5KGWB), GW3 (S5KGW3), GW1 (S5KGW1), GN9 (S5KGN9), GN5 (S5KGN5), GN3 (S5KGN3), GN2 (S5KGN2), GN1 (S5KGN1), JN1 (S5KJN1), GM5 (S5KGM5), GM2 (S5KGM2), GM1 (S5KGM1), GH1 (S5KGH1), JD1 (S5KJD1), GD2 (S5KGD2), GD1 (S5KGD1), 3P8 (S5K3P8), 3P9 (S5K3P9), 3T1 (S5K3T1SP), 3T2 (S5K3T2, S5K3T2SP), GN8 (S5KGN8), 2X5 (S5K2X5), HP9 (S5KHP9), GNJ (S5KGNJ), JN5 (S5KJN5), and GNK (S5KGNK). *See* WWSSENS 005094-005505 (documents showing that each of these ISOCELL models includes the RGB Bayer feature). These product models include the same technology and function the same with respect to the Asserted Claims, as explained in further detail in Section II of the Cover Disclosure. Accordingly, to the extent this chart identifies or describes a particular model of the CIS Accused Products, including Samsung’s ISOCELL GN3, such model is used as an example of a CIS Accused Product with the RGB Bayer feature and is representative in relevant part of the CIS Accused Products that include the RGB Bayer feature. As such, the analysis in this chart applies to all CIS Accused Products with the RGB Bayer feature, as well as all CIS Accused End Products that include a CIS Accused Product with the RGB Bayer feature.

Ref.	10,468,543 Claim Element	CIS Accused Products (RGB Feature)
1 [pre]	A single-chip device comprising	<p>Samsung's CIS Accused Products with the RGB Feature are CMOS image sensors built on a single chip and are, therefore, single-chip devices.</p> <p>Samsung's CIS Accused Products operate as one photodiode because Samsung's CIS Accused Products use a single photodetector by combining all buried photodiodes under one color filter at the same time. WSENS004643-WSENS004646 at 4643 ("Three 1x3 shared pixel units are combined to create a 3x3 pixel with the same color. In nona-binning operation mode, 9 pixels are read simultaneously, signal electrons in shared three PDs are summed in the floating diffusion (FD), and the three vertical outputs are averaged at the voltage domain."). For example, Samsung's CIS Accused Products use remosaic mode where the photodiode connected to TG1 (or TG2, or TG3) is used individually, while the other two buried photodiodes are read until VFD is reset. The reset instruction is performed chip-wise. Each time VFD is reset, the buried photodiodes are reset as well. The 3 metal connections (columns) correspond to one analog-to-digital converter. To avoid interference between the three 1x3 shared pixels, only one of them will be selected at any given time, and the transistors, together, perform the storage, transmission, amplification, and signal processing. <i>Id.</i> Therefore, these buried photodiodes never operate as independent pixels from one another, but instead operate as one photodetector.</p>
1.a	an integrated combination of a microstructure-enhanced photodetector (MSPD)	<p>Samsung's CIS Accused Products are an integrated combination of a microstructure-enhanced photodetector (MSPD). This is because Samsung's CIS Accused Products are CMOS image sensors that convert light (optical input) to an electrical output. For example, as confirmed by the ICFA lab analysis and shown below, each color filter is a pixel outlined by deep trenches (DTI) into a laterally extending array of pillars. The pillars with microstructure-enhanced photodetectors (MSPD) have shallow and/or deep trenches filled with dielectric material, which are microstructures to enhance photo sensitivity (performing the photodetector operation).</p>

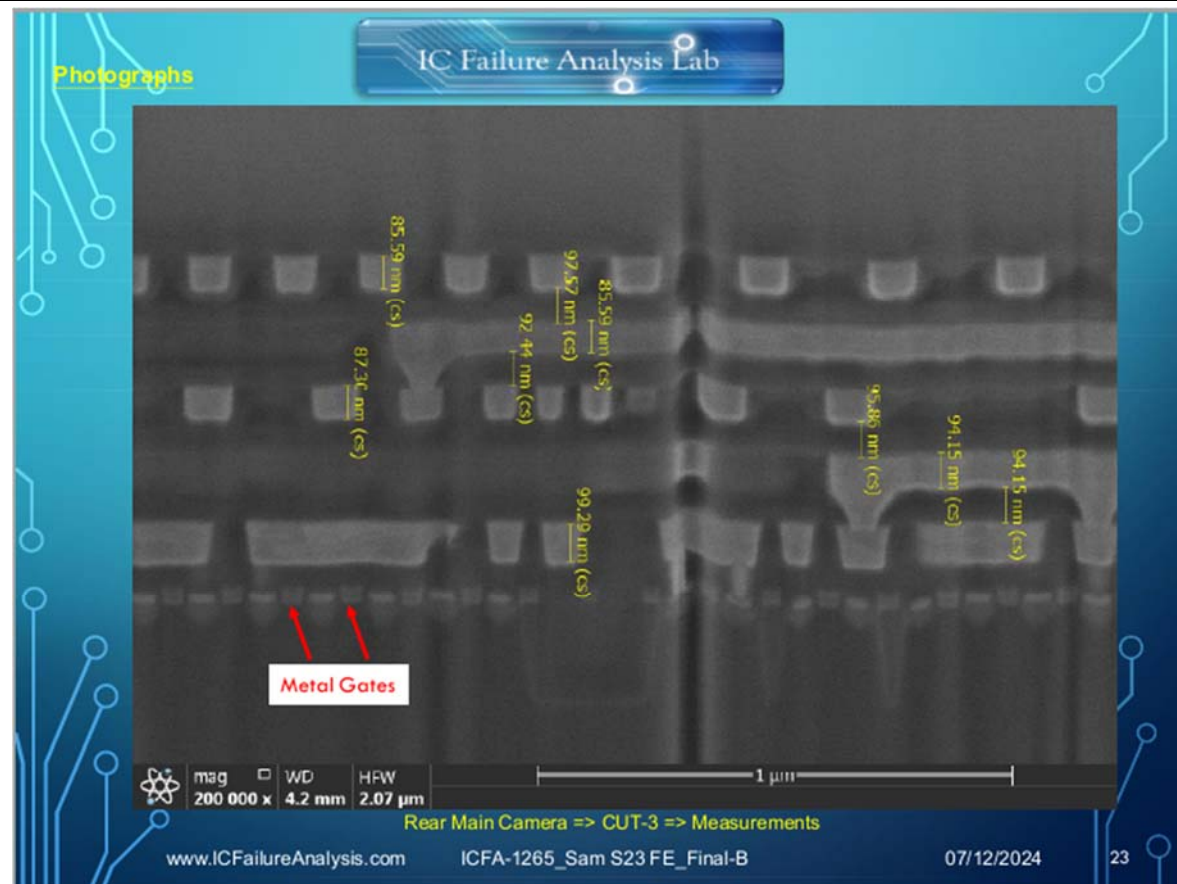
		 <p>WWSSENS004710-WWSSENS004753 at 4720 (annotated to show photodetector, showing shallow and/or deep trenches covered with dielectric materials).</p>
1.a.1	configured for reverse-bias operation	<p>Samsung's CIS Accused Products are configured for reverse-bias operation. The MSPDs are reverse biased for detecting lights. WWSSENS004643-WWSSENS004646 at 4645. The cathodes of the MSPDs are biased to a positive voltage, <math>V_{DD}</math>, when integrated active electronics RG, DCG, TG1, TG2, TG3 are turned on, as shown below:</p>

		<p>WWSENS004643-WWSENS004646 at 4645 (annotated schematics of pixel circuit).</p> <p>Specifically, for example, the transistor symbols denoted by RG, DCG, TG1, TG2, TG3, etc. are for n-MOSFETs, which are type of transistor. When the voltages, <math>V_{RG}</math>, <math>V_{DCG}</math>, <math>V_{TG1}</math>, <math>V_{TG2}</math>, <math>V_{TG3}</math> are high, a positive voltage, <math>V_{DD}</math>, is applied to the cathodes of the MSPDs, causing reverse biasing to MSPDs.</p>
1.a.2	and an active electronic circuit,	<p>Samsung's CIS Accused Products comprise an active electronic circuit because the transistors TG1, TG2, TG3 labeled as VTG (i.e., vertical transfer gate) in the TEM (i.e., Transmission Electron Microscopy) pictured below, are an active electronic circuit integrated into the MSPDs. WWSENS004710-WWSENS004753 at 4751.</p>

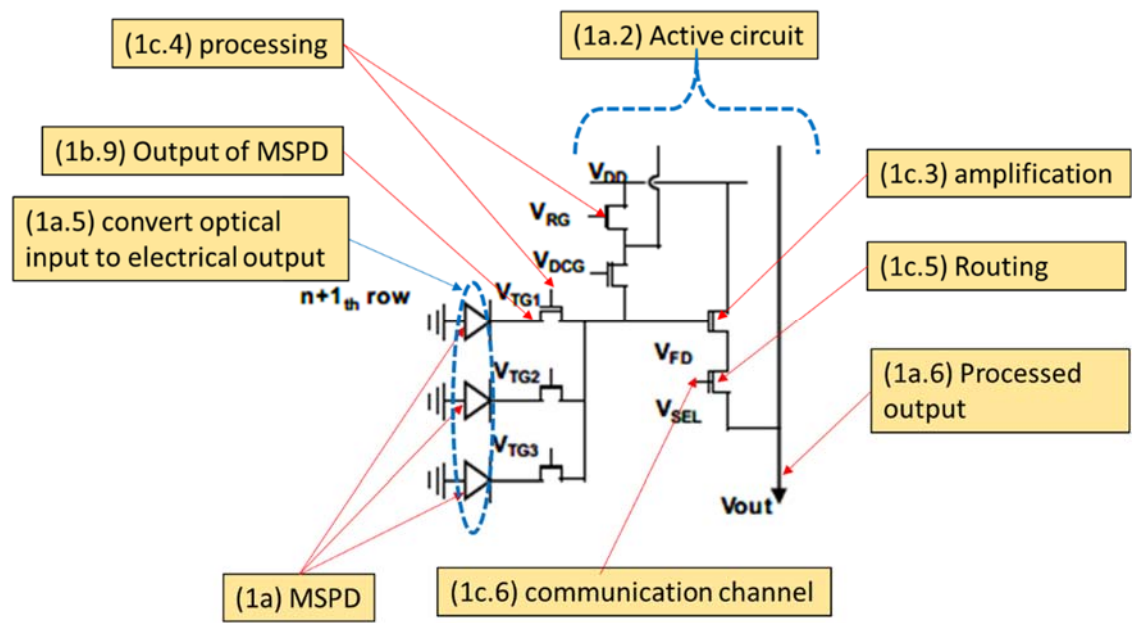


WWSSENS004710-WWSSENS004753 at 4751 (TEM showing VTG's (vertical transfer gates) are integrated into the photodetector; the p-contact and n-contact facilitate reverse biasing of the photodetector).

Additionally, as shown in Figure 4a below, there are two separate portions of active electronics. WWSSENS004643-WWSSENS004646 at 4645. The first portion is located in each pixel on the top chip and the second portion is located in the bottom chip. These two chips are manufactured separately using different technologies and subsequently bonded together for an integrated combination.

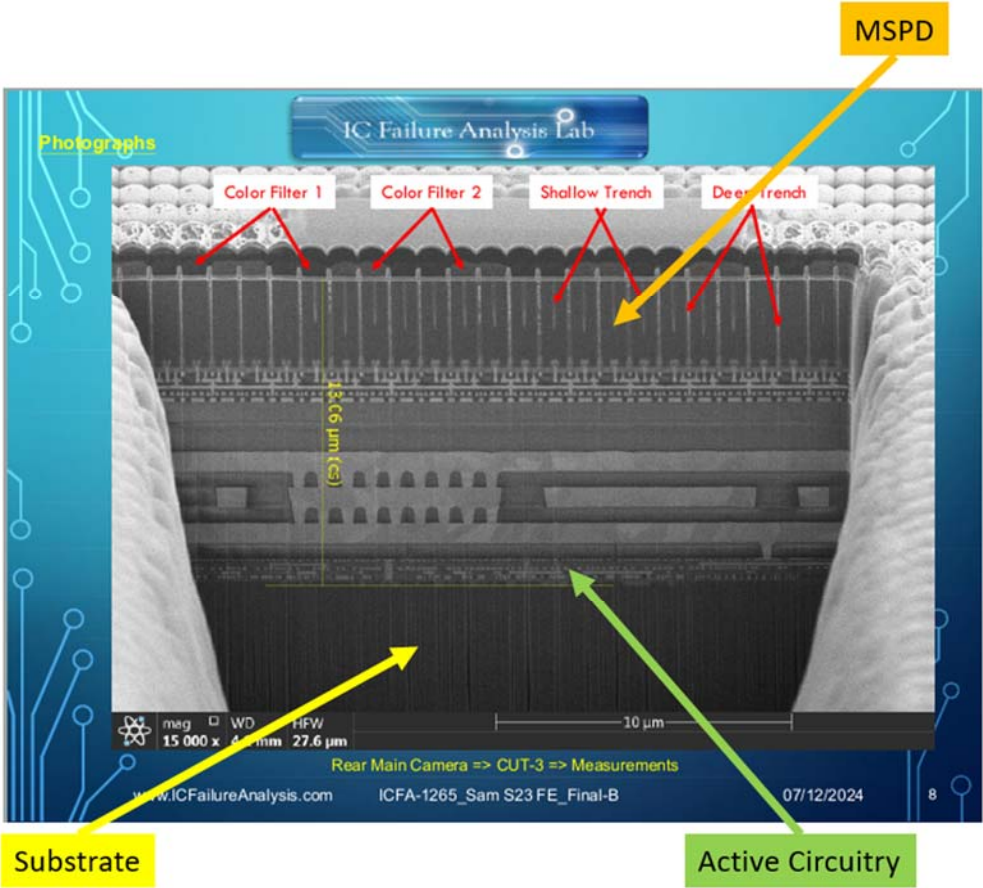


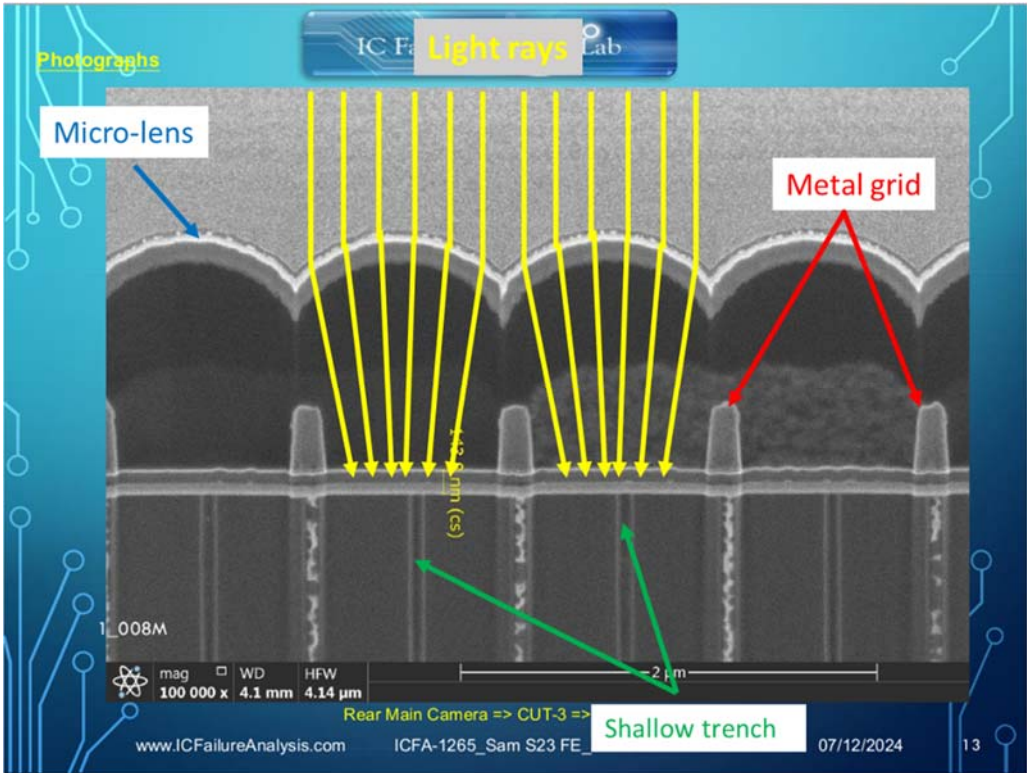
WWSSENS004710-WWSSENS004753 at 4733 (SEM showing the active circuitry at the bottom chip).

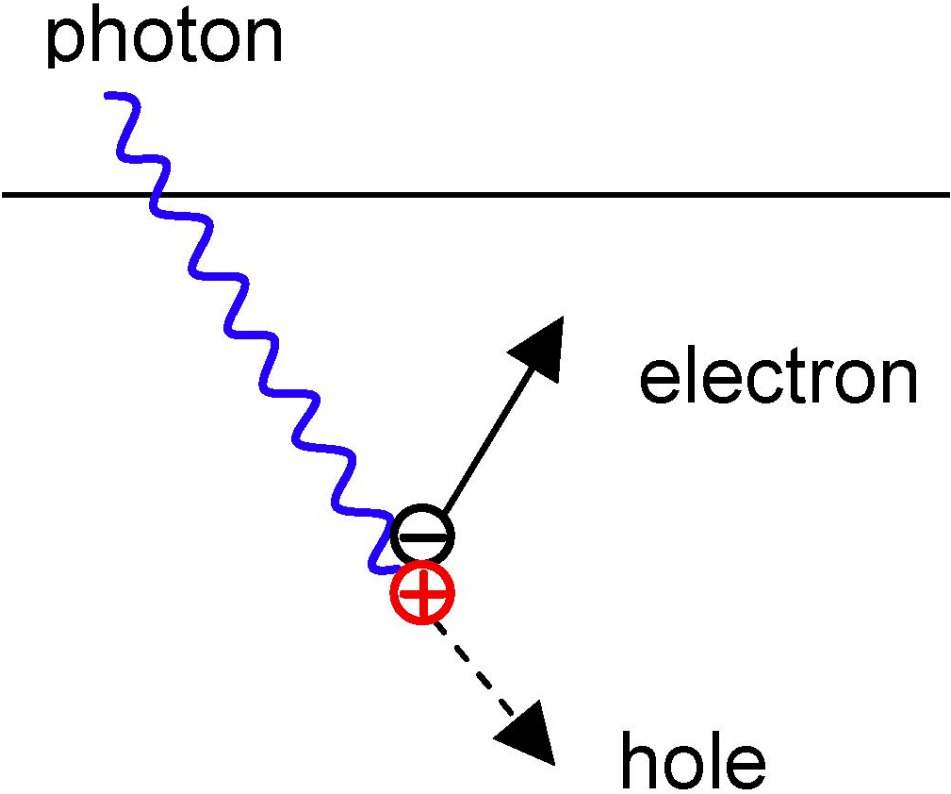


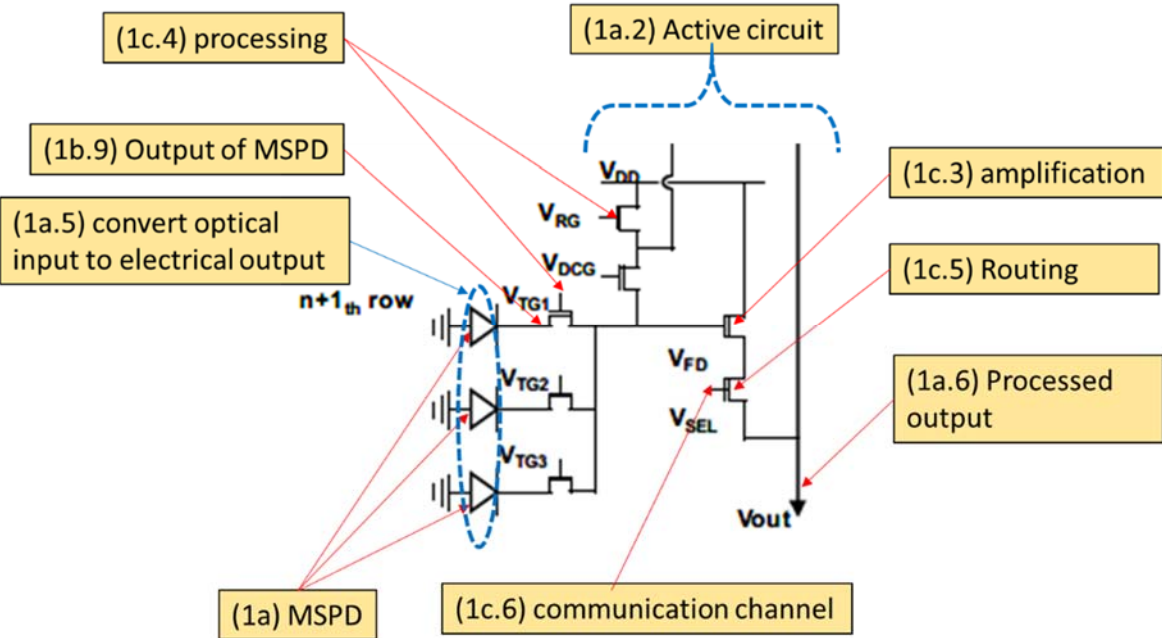
WWSSENS004643-WWSSENS004646 at 4645 (annotated schematics of pixel circuit and other active electronics to perform processing of the electrical output form the detector).

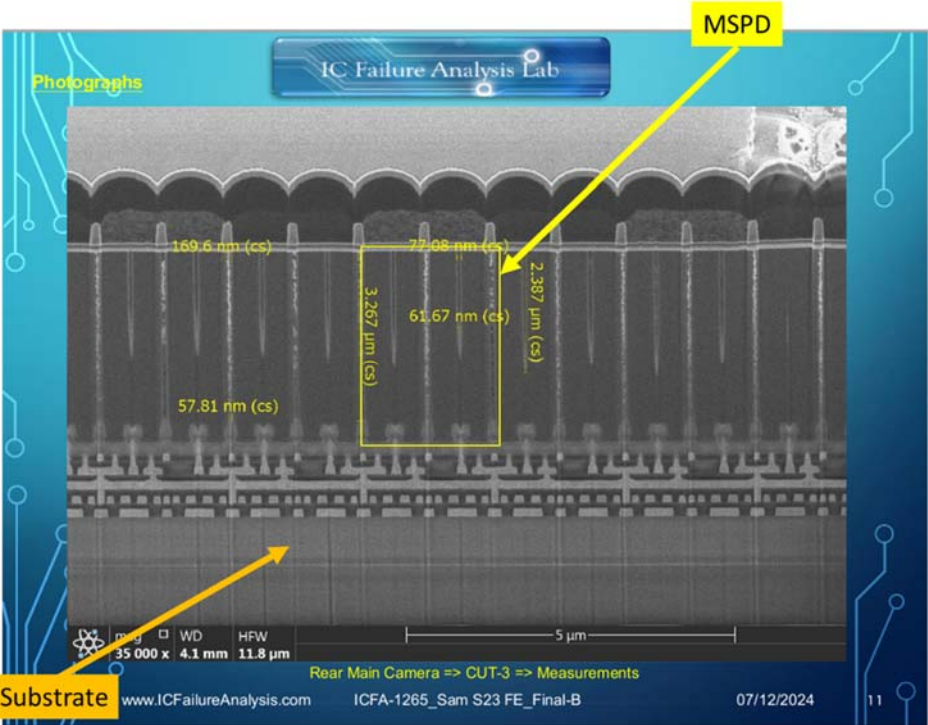


1.a.3	both formed on or in a single substrate	<p>Samsung's CIS Accused Products comprise MSPDs with the active electronic circuit formed on a single substrate, as shown below:</p>  <p>WWSENS004710-WWSENS004753 at 4718 (annotated to show MSPD and active circuitry on a single substrate).</p>
-------	---	---

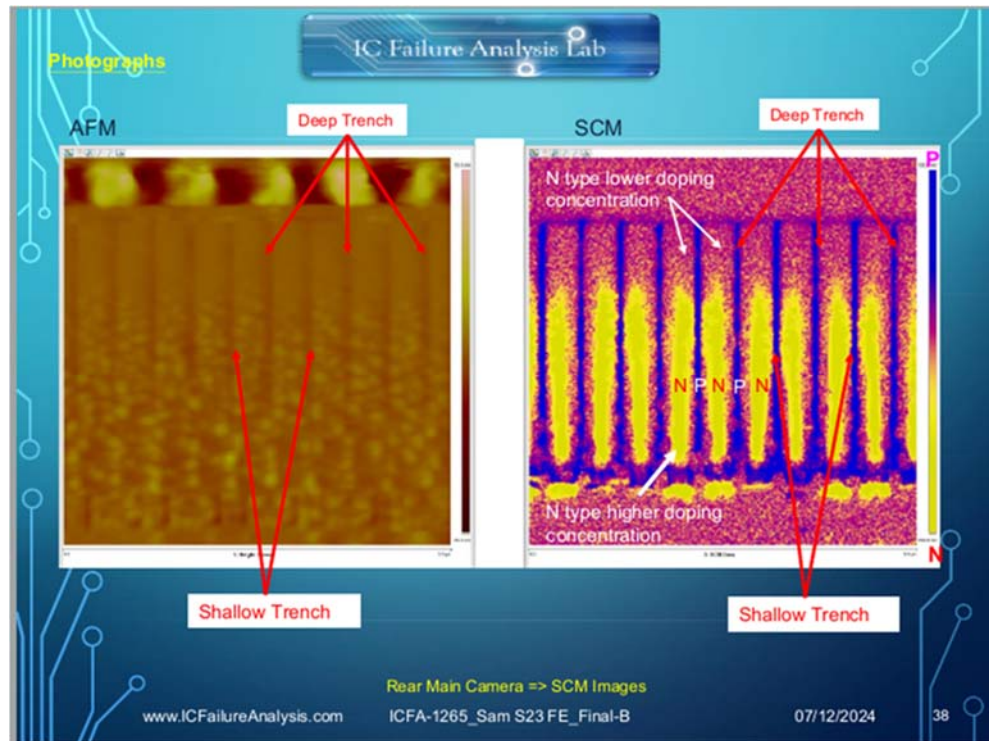
1.a.4	and configured to receive an optical input that in cross-section is substantially continuous spatially,	<p>Samsung's CIS Accused Products are configured to receive an optical input that in cross-section is substantially continuous. This is because each pixel has at least one <math>\mu</math>-lens to focus light to the input portion of the MSPD, which is substantially continuous spatially, as illustrated below.</p>  <p>WWSENS004710-WWSENS004753 at 4723 (annotated to illustrate the effect of the <math>\mu</math>-lenses to focus the light rays to the MSPDs).</p>
-------	---	--

1.a.5	convert the optical input to an electrical output,	<p>Samsung's CIS Accused Products convert the optical input to an electrical output because they are CMOS image sensors. The MSPD absorbs the input light and generates electrical current. The image below generally shows that when a photodetector absorbs a photon, it generates electrical current due to the photoelectric effect.</p>  <p>The diagram illustrates the photoelectric effect. A horizontal black line represents the surface of a photodetector. A blue wavy line, labeled 'photon', originates from the top left and points towards a black circle with a minus sign (representing an electron) on the surface. From this electron, a solid black arrow labeled 'electron' points upwards and to the right. Below the electron, a red circle with a plus sign (representing a hole) is shown. A dashed black arrow labeled 'hole' points downwards and to the right from the hole. The labels 'photon', 'electron', and 'hole' are placed near their respective symbols.</p> <p>WWSENS 007748-WWSENS 007754 at 7748; WWSENS 007762.</p>
-------	--	--

1.a.6	and process the electrical output into a processed output,	<p>Samsung's CIS Accused Products process the electrical output into a processed output. For example, the circuitry of Samsung's GN3 processes the photo-generated charges into a processed output, as explained by Figure 4a in Samsung's 2020 Nonacell Article below:</p>  <p>WWSSENS004643-WWSSENS004646 at 4645 (annotated schematics of pixel circuit and other active electronics to perform processing of the electrical output from the detector).</p>
-------	--	--

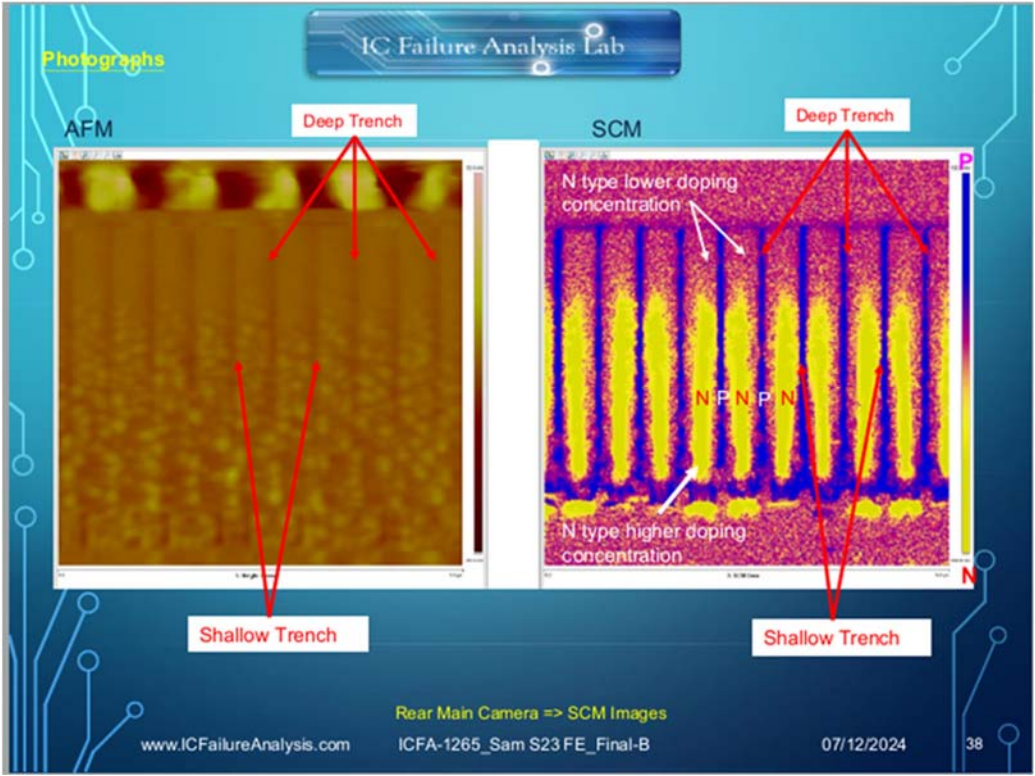
1.b	wherein: the MSPD on or in said single substrate comprises	<p>Samsung's CIS Accused Products have an MSPD on the single substrate. The MSPD comprises elements color filter to dielectric material.</p>  <p>WWSSENS004710-WWSSENS004753 at 4721 (annotated to show the MSPD on the single substrate).</p>
1.b.1	an intermediate region,	<p>Samsung's CIS Accused Products include an MSPD with an intermediate region, specifically an intermediate semiconductor material. Scanning Capacitance Microscopy (SCM) is used to examine a cross-section view of microstructures and doping profiles. The doping concentrations are color coded that heavily-doped p-type regions are shown in blue and heavily-doped regions are shown in yellow.</p>

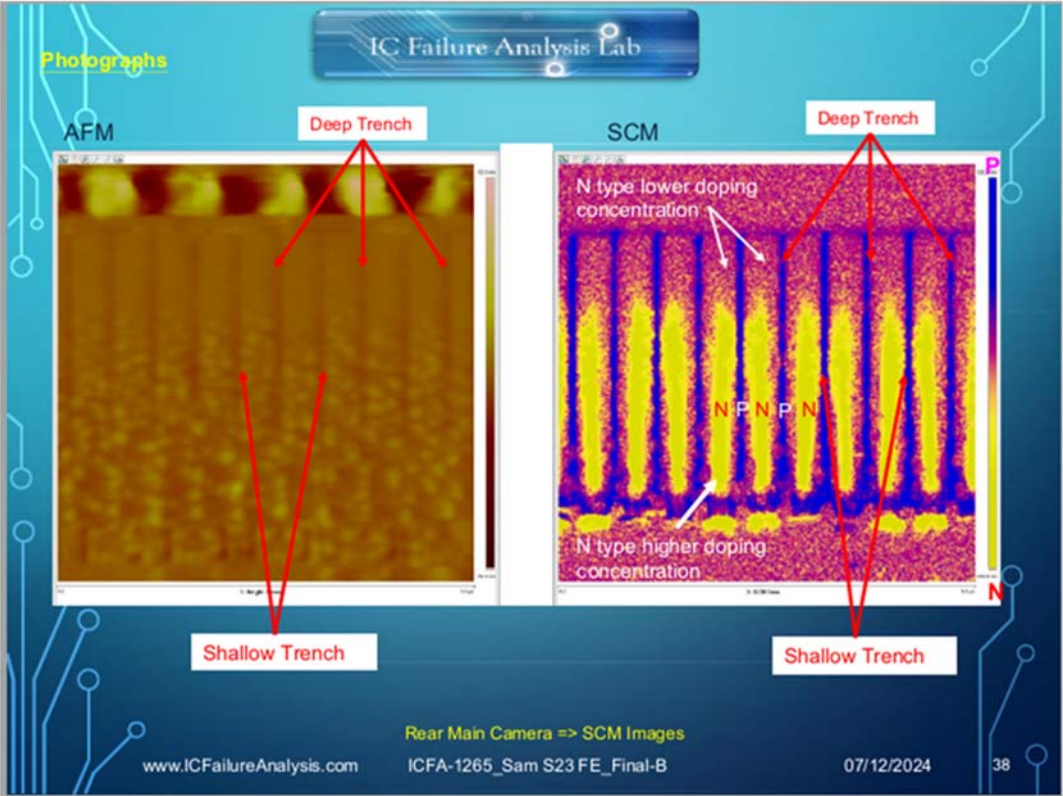
This region is in between the first and second doped semiconductor materials, thereby making it an intermediate region. The image below illustrates an intermediate region as the absorption region. WWSSENS004710-WWSSENS004753 at 4748. The absorption region is an intermediate region, shown in pink, as it is in between a first region, shown in blue, and a second region, shown in yellow.



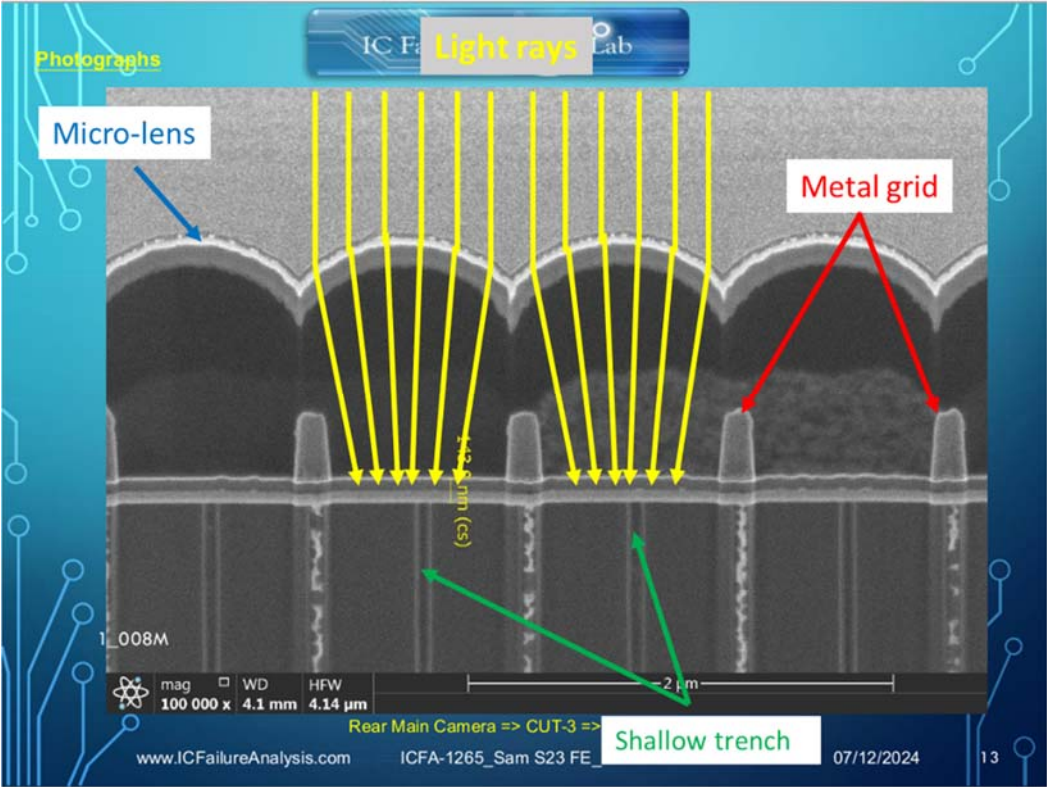
WWSSENS004710-WWSSENS004753 at 4748 (SCM images showing doping profile inside the pillars).

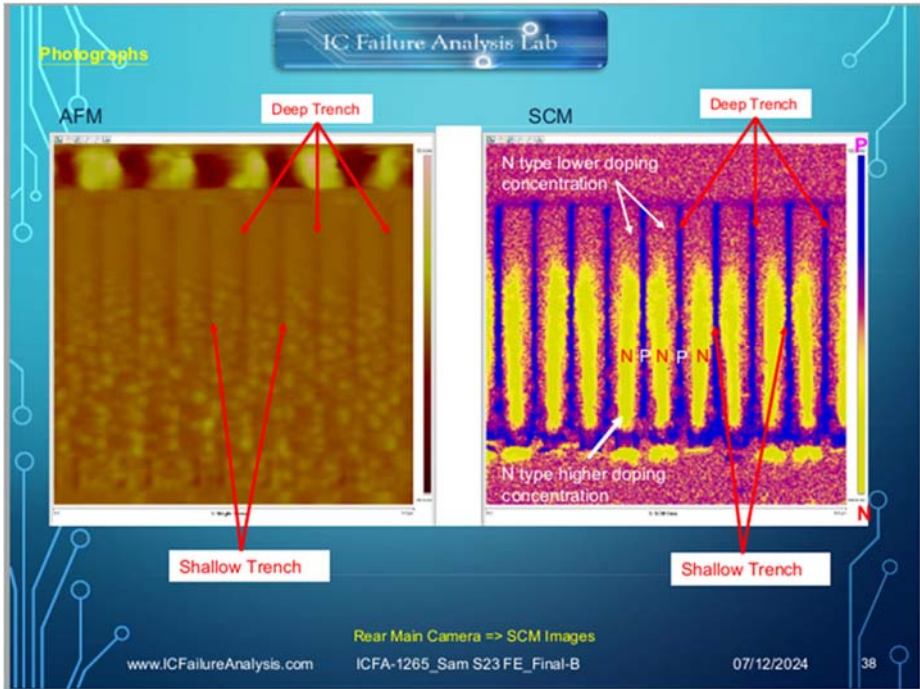


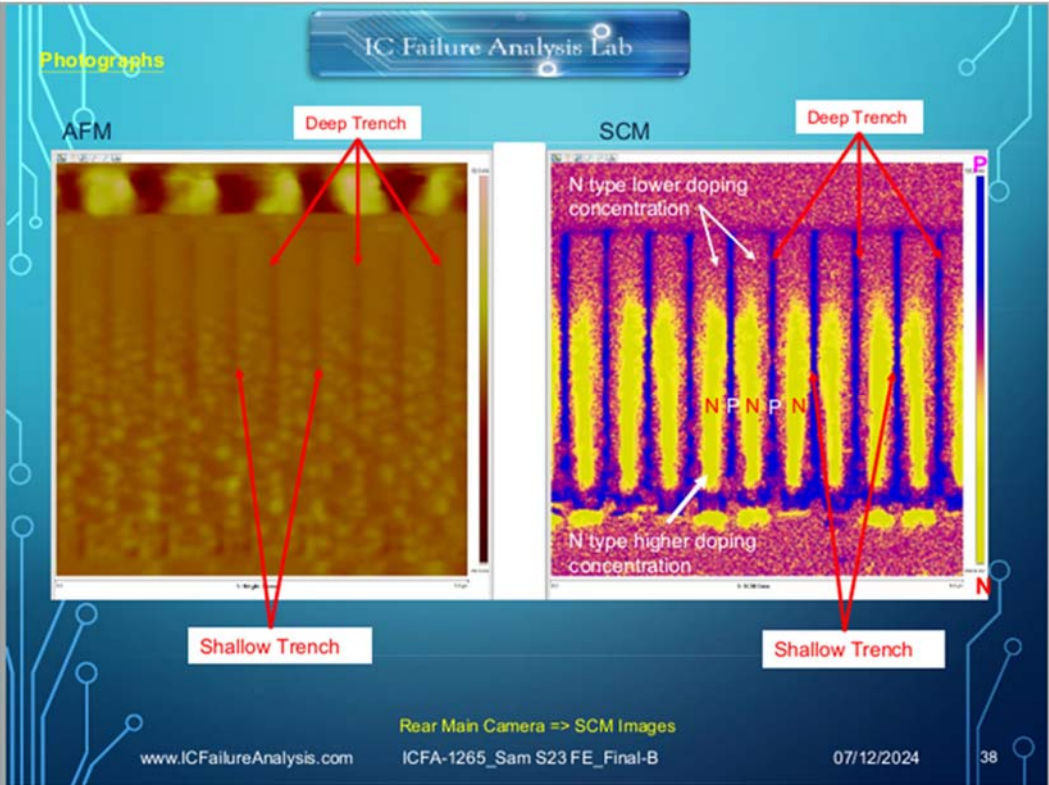
1.b.2	a first region at one side of the intermediate region,	<p>Samsung's CIS Accused Products have an MSPD with a first region at one side of the intermediate region. For example, the p-region, shown below in blue, is at one side of the intermediate region, which provides the ground potential. WWSSENS004710-WWSSENS004753 at 4748.</p>  <p>WWSSENS004710-WWSSENS004753 at 4748 (SCM images showing doping profile inside the pillars).</p>
-------	--	--

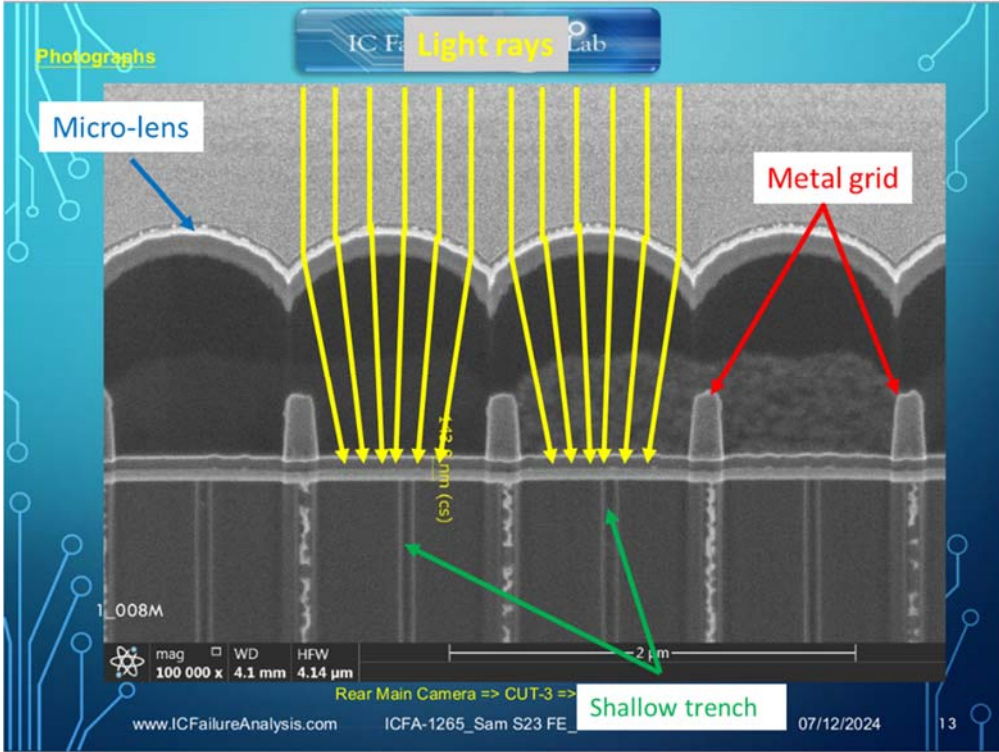
1.b.3	and a second region at an opposite side of the intermediate region,	<p>Samsung's CIS Accused Products have an MSPD with a second region on an opposite side of the intermediate region. For example, the n-region, shown below in yellow, is at the opposite side. Its potential is determined by a contact point to the transfer gate.</p>  <p>WWSSENS004710-WWSSENS004753 at 4748 (SCM images showing doping profile inside the pillars).</p>
1.b.4	wherein: each of the regions comprises Silicon, Germanium, or an alloy thereof;	In Samsung's CIS Accused Products, each of the first and second doped semiconductor materials are intermediate semiconductor material comprising silicon.

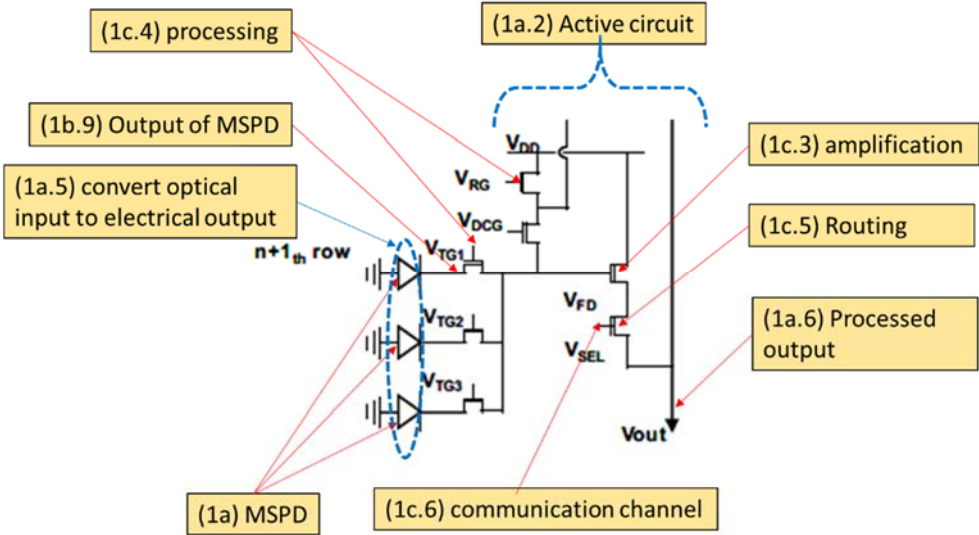


1.b.5	at least one of said regions, and an optional overlying covering region, have holes intentionally formed therein	<p>In Samsung's CIS Accused Products, the first region and the second region have holes (shallow and/or deep trenches) that are fabricated extending in directions transverse to the regions, as shown below. WWSENS004710-WWSENS004753 at 4723.</p>  <p>The image is a scanning electron micrograph (SEM) showing a cross-section of a CMOS Image Sensor (CIS) structure. At the top, there are several arched structures labeled 'Micro-lens' with a blue arrow. Below the micro-lenses is a layer labeled 'Metal grid' with a red arrow. Yellow arrows labeled 'Light rays' point downwards from the micro-lenses through the metal grid into the underlying silicon. At the bottom, there are vertical structures labeled 'Shallow trench' with a green arrow. The image includes technical data at the bottom: '1_008M', 'mag 100 000 x', 'WD 4.1 mm', 'HFW 4.14 μm', 'Rear Main Camera ==&gt; CUT-3 ==&gt;', 'www.ICFailureAnalysis.com', 'ICFA-1265_Sam S23 FE_', '07/12/2024', and '13'.</p> <p>WWSENS004710-WWSENS004753 at 4723 (annotated to show the shallow trenches).</p>
-------	--	--

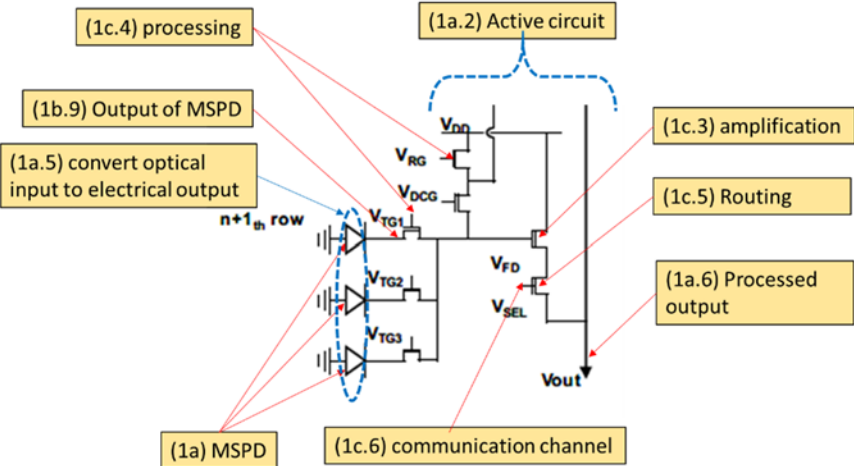
1.b.6	each of the first and second regions comprises a doped material;	<p>In Samsung's CIS Accused Products, the first and second regions are doped semiconductor material (silicon), as shown below. WWSENS004710-WWSENS004753 at 4748.</p>  <p>WWSENS004710-WWSENS004753 at 4748 (SCM images showing doping profile inside the pillars).</p>
-------	--	---

1.b.7	<p>the intermediate region [1b.1] comprises a material that is less doped than at least one of the first [1b.2] and second regions [1b.3] or is undoped, wherein the degree of doping is the same or different for different positions in the intermediate region;</p>	<p>In Samsung's CIS Accused Products, the intermediate semiconductor material [1b.1] is less doped than at least one of the first [1b.2] and second [1b.3] doped regions. WWSSENS004710-WWSSENS004753 at 4748. As shown in the image below, the intermediate region (shown in pink) is less doped than the first region, shown in blue, and the second region, shown in yellow. As further shown by the image below, the degree of doping is the same or different for different positions in the intermediate region.</p>  <p>WWSSENS004710-WWSSENS004753 at 4748 (SCM images showing doping profile inside the pillars).</p>
-------	--	---

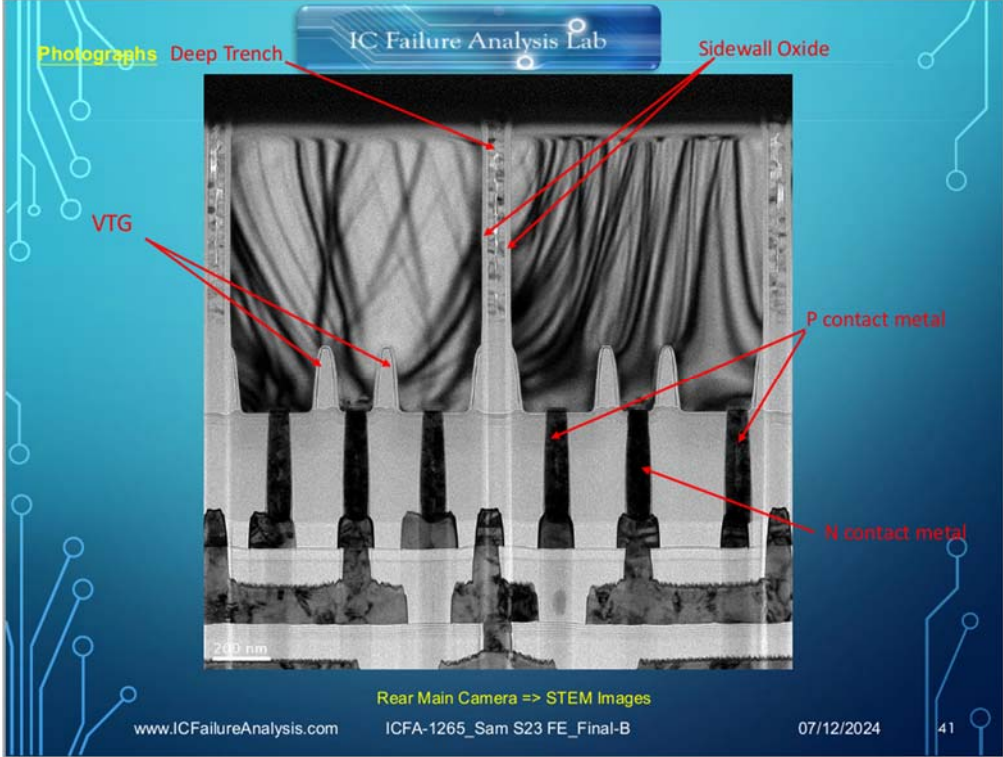
1.b.8	<p>an input portion configured to concurrently receive at a plurality of said holes [1b.5] said optical input that has said substantially continuous cross-section;</p>	<p>In Samsung's CIS Accused Products, the focused light rays (optical input) enter the photo-detecting regions having holes (shallow and/or deep trenches) fabricated therein (input portion), as shown below. WWSENS004710-WWSENS004753 at 4723. As further shown below, the light rays have a substantially continuous cross-section.</p>  <p>The image is a scanning electron micrograph (SEM) showing a cross-section of a CMOS Image Sensor (CIS) structure. At the top, a blue header bar contains the text 'Photographs' in yellow, 'IC Failure Lab' in white, and 'Light rays' in yellow. The main image shows a series of repeating structures. A blue arrow points to a 'Micro-lens' on the top surface. Yellow arrows, labeled 'Light rays', originate from the top and converge through the micro-lenses into a horizontal layer. Below this layer is a 'Metal grid', indicated by a red arrow. Further down, a green arrow points to a 'Shallow trench' in the substrate. Technical data at the bottom includes '1_008M', 'mag 100 000 x', 'WD 4.1 mm', 'HFW 4.14 μm', 'Rear Main Camera =&gt; CUT-3 =&gt;', 'www.ICFailureAnalysis.com', 'ICFA-1265_Sam S23 FE', '07/12/2024', and '13'.</p> <p>WWSENS004710-WWSENS004753 at 4723 (annotated to illustrate the effect of the <math>\mu</math>-lenses to focus the light rays to the MSPDs).</p>
-------	---	--

1.b.9	and an output portion configured to provide said electrical output from the MSPD;	<p>In Samsung's CIS Accused Products, an output portion is configured to provide the electrical output from the MSPD because after light enters the photo-detecting regions, it is converted into photo-generated charges, an electrical output. WWSSENS004643-WWSSENS004646 at 4645. For example, the circuitry of Samsung's GN3 processes the photo-generated charges into a processed output, as explained by Figure 4a in Samsung's 2020 Nonacell Article.</p> <p>As further evidence, GN3's circuitry turns off the Reset Gate (RG, DCG) and Transfer Gate (TG1, TG2, TG3), such that photo-generated charges are swept by the electrical field, causing the positively charged holes to move to GND and the negatively charged electrons to move to the cathode of the MSPD.</p>  <p>WWSSENS004643-WWSSENS004646 at 4645 (annotated schematics of pixel circuit and other active electronics to perform processing of the electrical output from the detector).</p>
-------	---	--



1.c	the MSPD includes reverse-bias contacts coupled therewith	<p>The MSPD of Samsung's CIS Accused Products is coupled to reverse-biased electrodes. The reverse-bias contacts are coupled to the active circuit (1a.2) which is configured to provide reverse bias to the MSPD. For example, as shown in Figure 3 of Samsung's 2020 2PD Article, the GN3's circuitry turns on the Reset Gate (RG, DCG) and Transfer Gate (TG1, TG2, TG3), such that <math>V_{DD}</math> is applied to the MSPD so that MSPD's cathode is biased with more positive voltage to establish electric fields in the P-N junction to sweep the photo-generated charges. WWSENS004643-WWSENS004646 at 4645.</p>  <p>WWSENS004643-WWSENS004646 at 4645 (annotated schematics of pixel circuit).</p>
-----	---	--

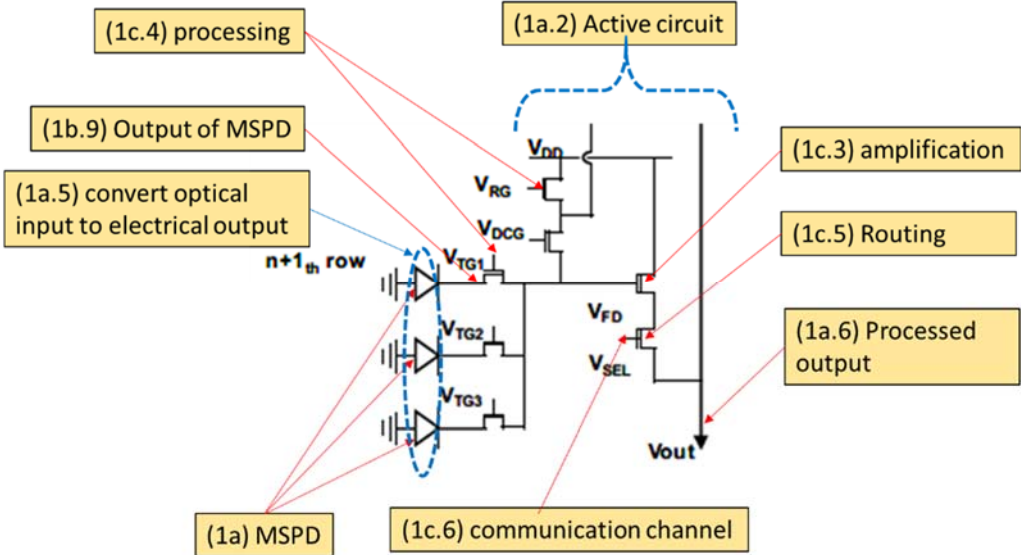


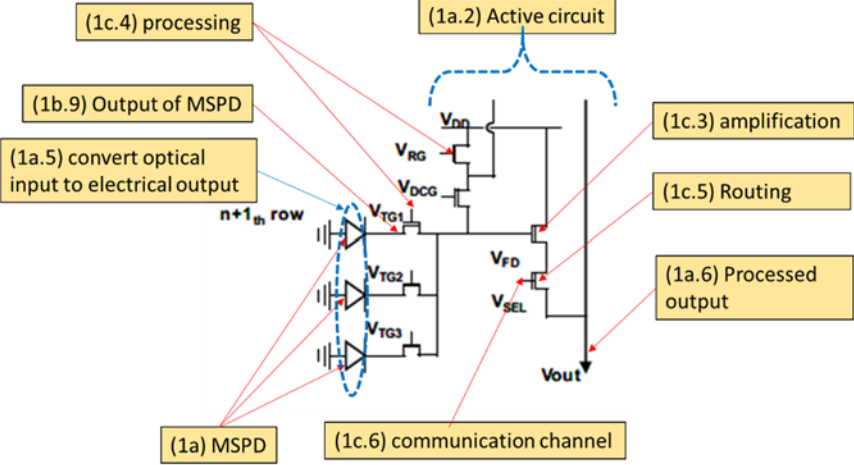
		 <p>WWSSENS004710-WWSSENS004753 at 4751 (TEM showing VTG's (vertical transfer gates) are integrated into the photodetector; the p-contact and n-contact facilitates reverse biasing of the photodetector).</p>
1.c.2	and the active electronic circuit [1a.2] on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:	In Samsung's CIS Accused Products the active electronic circuit is configured to process the electrical output from the MSPD, as shown in the circuit diagram below.

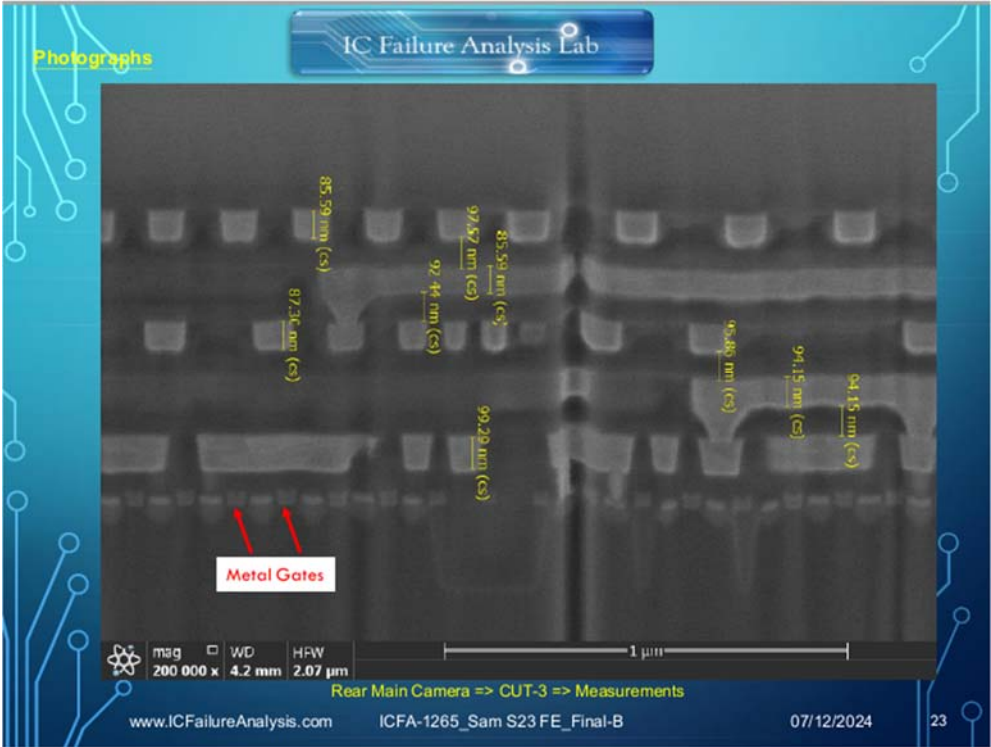


		<p>WWSENS004643-WWSENS004646 at 4645 (annotated schematics of pixel circuit).</p>
1.c.3	amplification to form said processed output from the single-chip device;	<p>Samsung's CIS Accused Products amplify the output from the device. As shown in Figure 4a of Samsung's 2020 Nonacell Article, the circuitry turns on the Transfer Gate (TG1, TG2, TG3) only, such that the photogenerated charges are transferred to the gate of the source-follower circuit and the current is amplified. WWSENS004643-WWSENS004646 at 4645.</p>



1.c.5	and routing to one or more selected destinations;	<p>In Samsung's CIS Accused Products, the output is routed to one or more selected destinations. WWSENS004643-WWSENS004646 at 4645. The row driving signal (1c.6) coupled to the select switch determines which pixel in a column is read to the column output. By sequentially turning on the select transistor of each cell row by row, the data of each row in the same column can be read out one by one.</p>  <p>WWSENS004643-WWSENS004646 at 4645 (annotated schematics of pixel circuit, annotated with claim elements of Claim 1 of the '700 Patent).</p>
-------	---	--

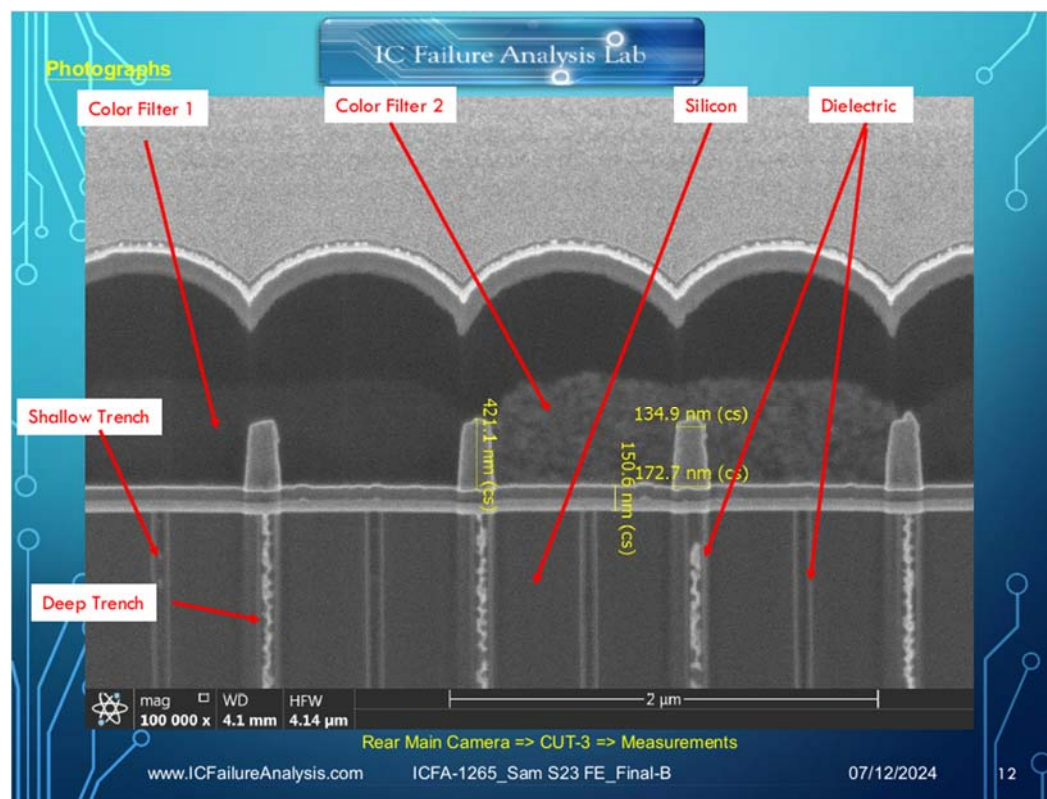
1.c.6	and a communication channel on or in said single-chip device, configured to deliver the electrical output from the MSPD to the active electronic circuit.	<p>In Samsung's CIS Accused Products, a communication channel delivers the electrical output from the MSPD to the active electronic circuit. The row driving signal is a communication channel, driven by a timing control circuit to select a row of pixels to be read to off-chip column analog-to-digital converter via column metal trace <math>V_{out}</math>, as shown in the figure below. WWSSENS004643-WWSSENS004646 at 4645.</p>  <p>WWSSENS004643-WWSSENS004646 at 4645 (annotated schematics of pixel circuit, annotated with claim elements of Claim 1 of the '700 Patent).</p>
-------	---	--

3	<p>The single-chip device of claim 1, in which said active electronic circuit is at least partly inside said substrate.</p>	<p>In Samsung's CIS Accused Products, the active electronic circuit is at least partly inside the substrate. This is because CMOS devices are fabricated with conducting channels inside the substrate and the gate, source, drain electrodes, and interconnect metals above the substrate, as shown below. WWSSENS004710-WWSSENS004753 at 4733.</p>  <p>WWSSENS004710-WWSSENS004753 at 4733 (showing CMOS devices partly inside the substrate).</p>
---	---	---

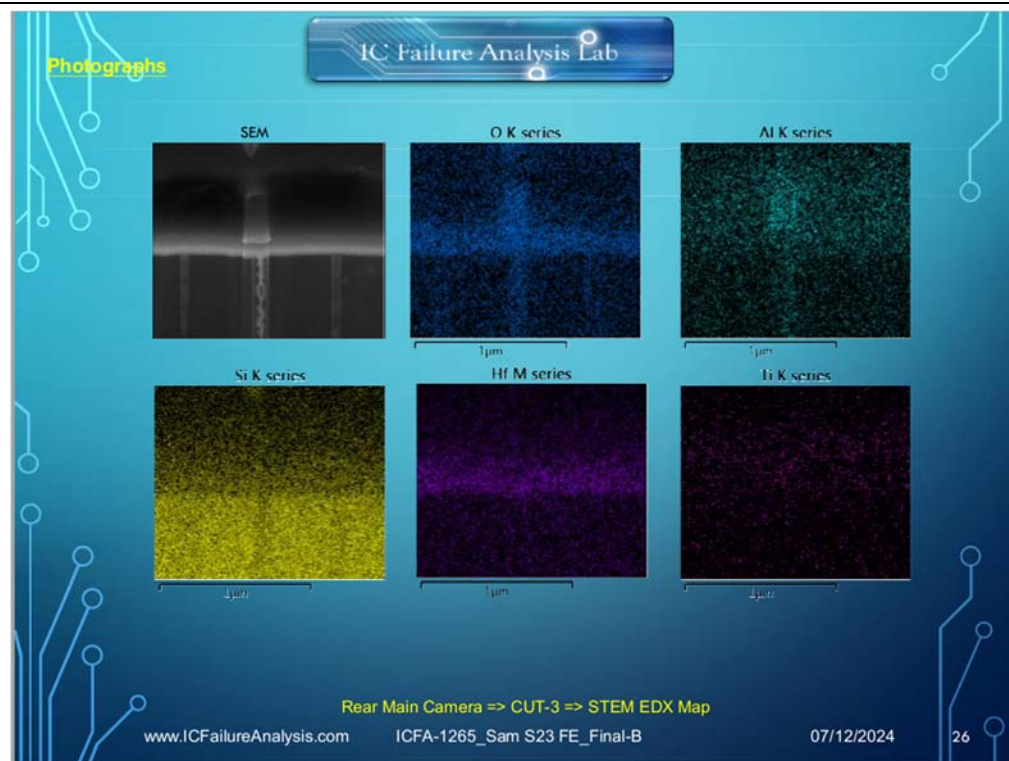
7

The single-chip device of claim 1, further including a region of a dielectric material that covers the holes and is in the propagation path of said optical input.

Samsung's CIS Accused Products include a region of a dielectric material that covers the holes and is in the propagation path of said optical input. As shown in the below image of the GN3, the shallow and/or deep trenches are coated with a region of dielectric material (shown in brighter grey as annotated below). WWSSENS004710-WWSSENS004753 at 4722. The dielectric regions are in the propagation path (vertical direction) of the optical input. The dielectric regions contain both oxygen and silicon as shown by the EDX (Energy Dispersive X-Ray) image below. WWSSENS004710-WWSSENS004753 at 4736.  $\text{Si}_x\text{O}_y$ , shown in the EDX image, is a dielectric material.



WWSSENS004710-WWSSENS004753 at 4722 (showing shallow and/or deep trenches covered with dielectric materials, shown in grey).



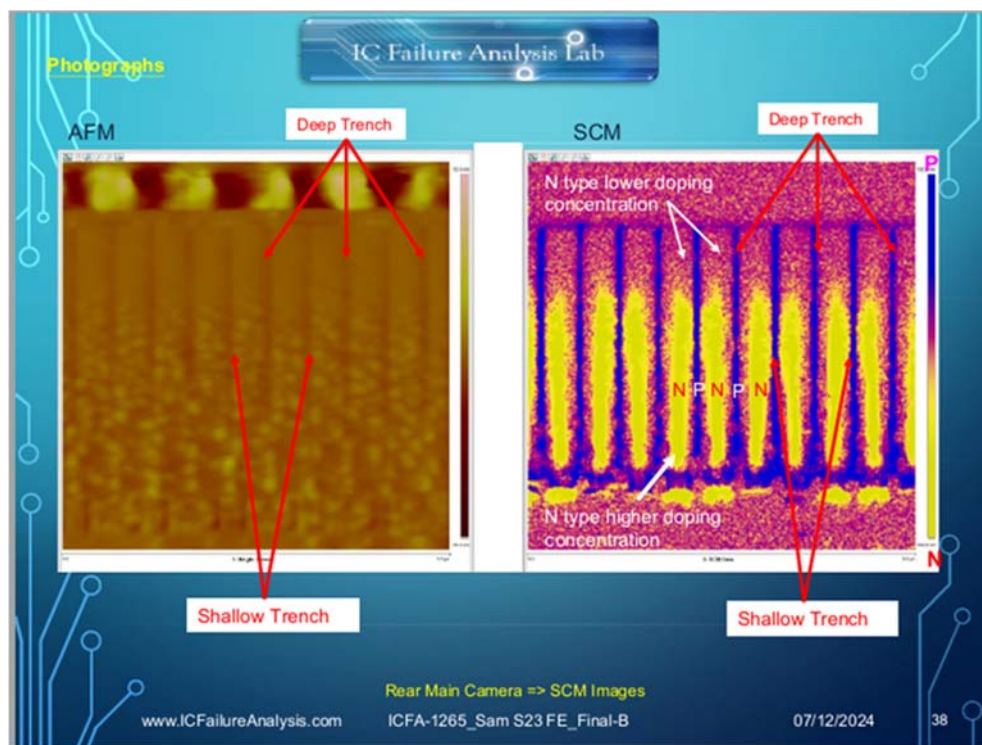
WWSENS004710-WWSENS004753 at 4736 (EDX images showing signals of oxygen and silicon inside both shallow trenches and/or deep trenches).



9

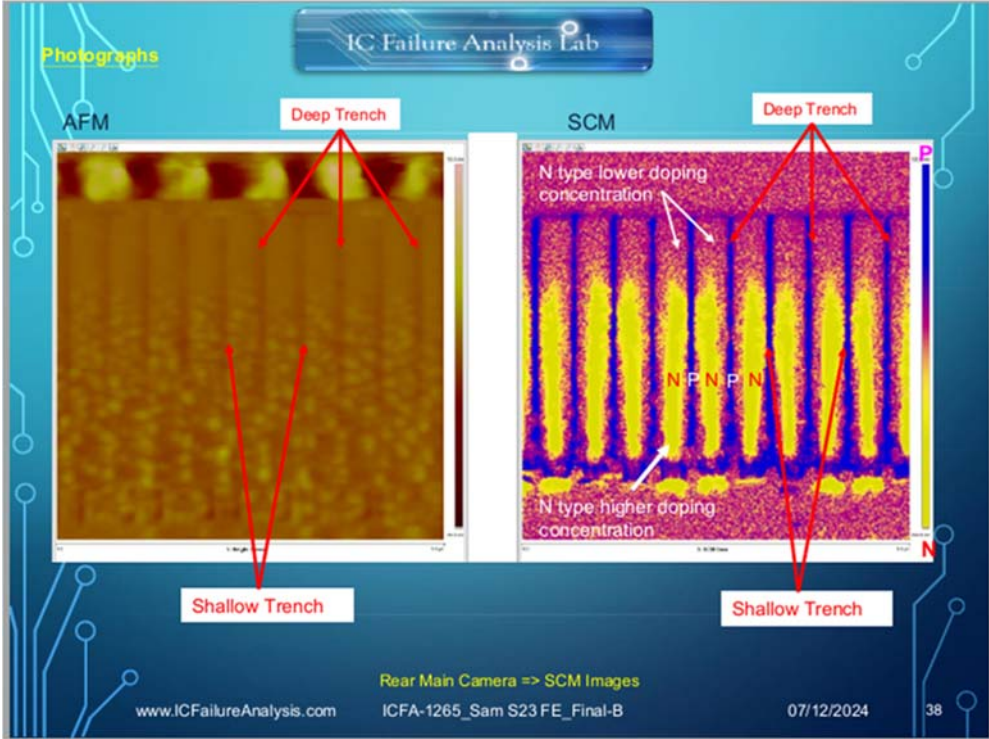
The single-chip device of claim 1, in which said holes are present in said intermediate region.

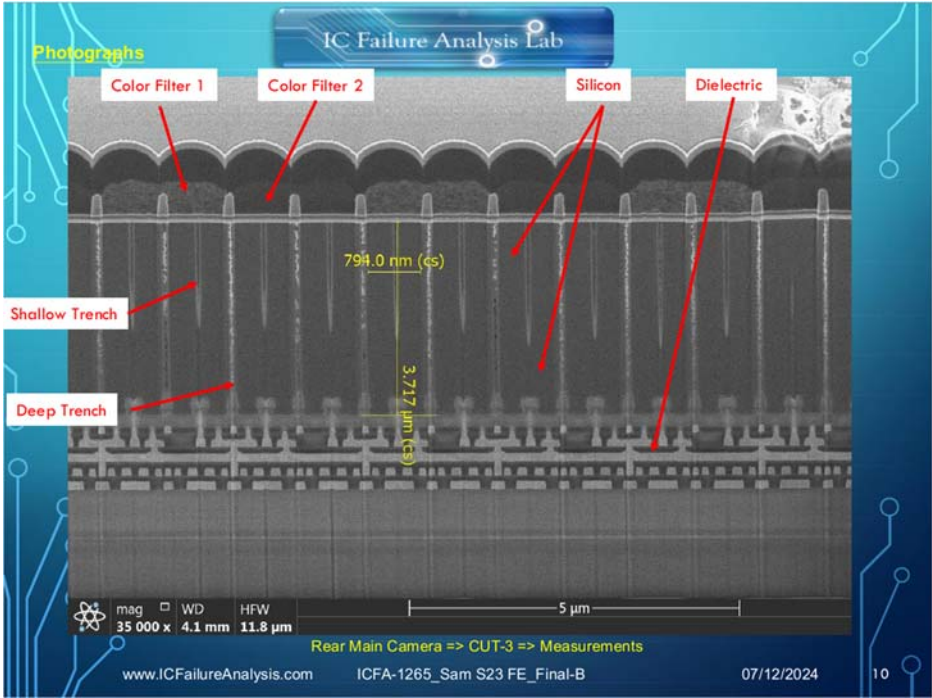
The holes of Samsung's CIS Accused Products are present in the intermediate region discussed above. As shown in the SCM image below, the shallow trenches and deep trenches penetrate the blue, pink and yellow regions. WWSSENS004710-WWSSENS004753 at 4748. Thus, the holes are present in the intermediate region.

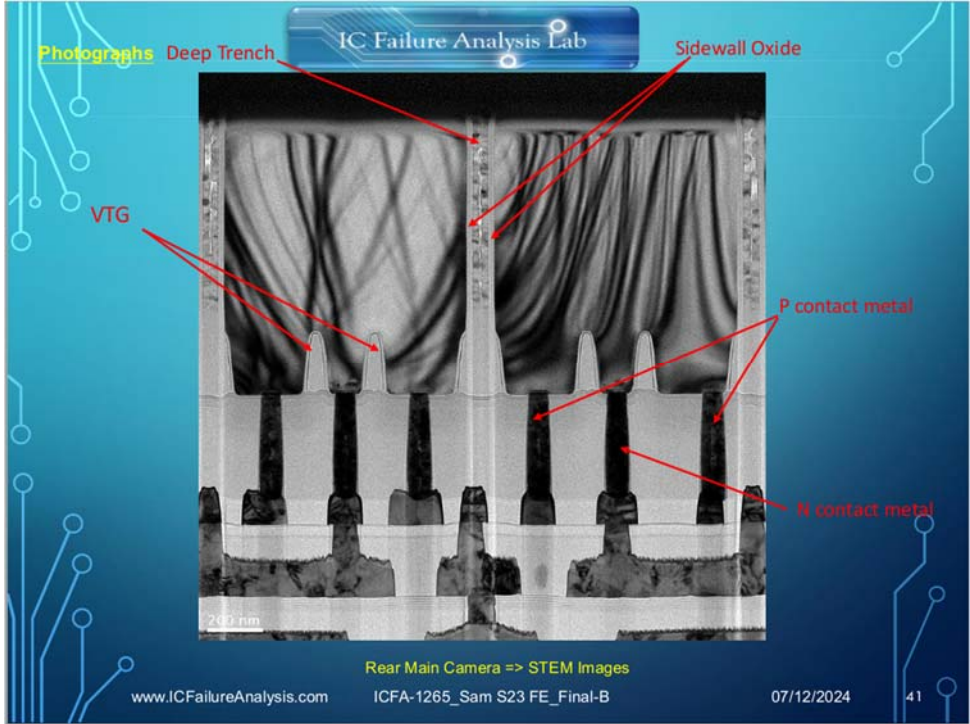


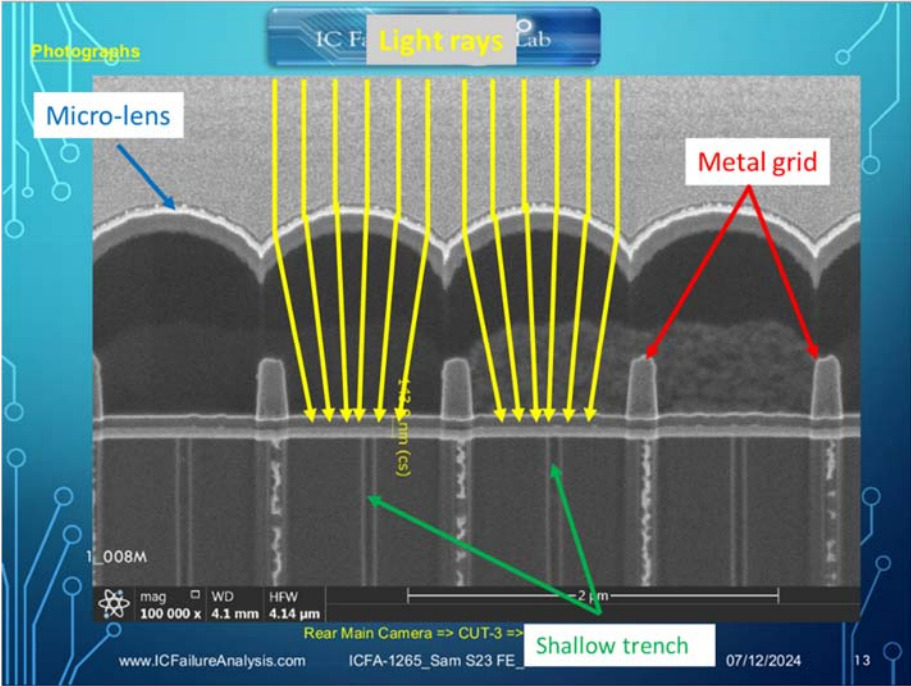
WWSSENS004710-WWSSENS004753 at 4748. (SCM images showing doping profile inside the pillars).

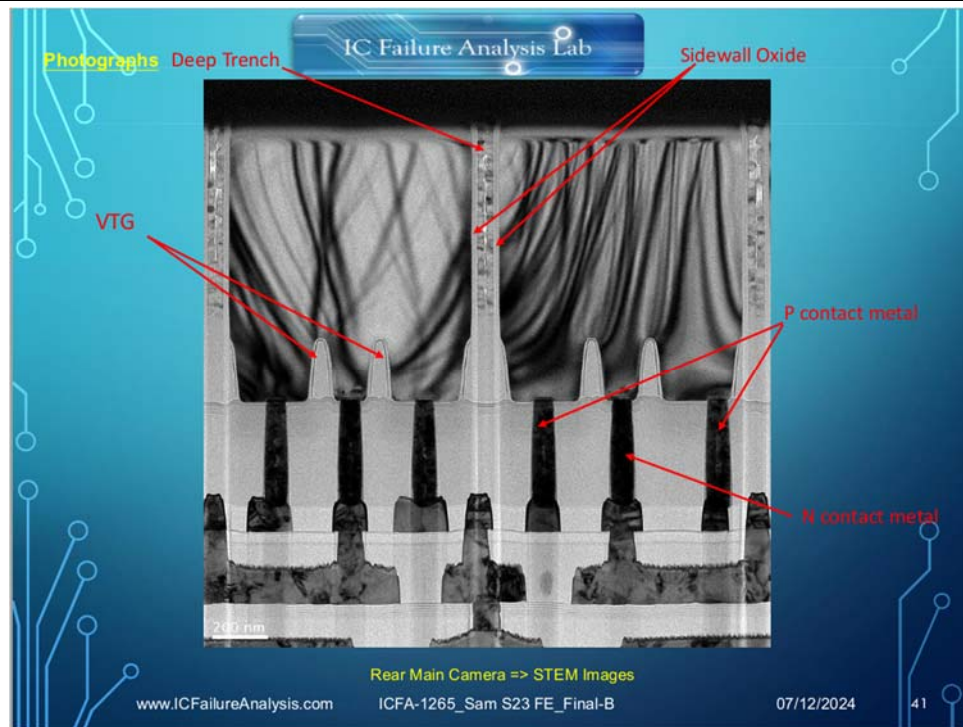


<p>10</p>	<p>The single-chip device of claim 1, in which said holes are present in said intermediate region as well as in at least one of the first and second regions.</p>	<p>The holes of Samsung's CIS Accused Products are present in the intermediate, first, and second regions. As shown in the SCM images below, the shallow trenches and deep trenches penetrate the blue, pink and yellow regions, which correspond to those regions. WWSENS004710-WWSENS004753 at 4748.</p>  <p>WWSENS004710-WWSENS004753 at 4748. (SCM images showing doping profile inside the pillars).</p>
-----------	---	--

16	<p>The single-chip device of claim 1, in which at least some of said holes have sidewalls that slope in planes transverse to said regions.</p>	<p>The holes in Samsung's CIS Accused Products have sidewalls that slope in planes transverse to the regions discussed above. As shown below, the sidewalls of the shallow trenches and the deep trenches are perpendicular to the semiconductor regions which are horizontal. WWSSENS004710-WWSSENS004753 at 4720.</p>  <p>WWSSENS004710-WWSSENS004753 at 4720 (showing shallow and/or deep trenches have sidewalls in the vertical (transverse) direction).</p>
20	<p>The single-chip device of claim 1, in which the holes are at least partly filled with a dielectric material.</p>	<p>As discussed for Claim 7, the holes contain <math>\text{Si}_x\text{O}_y</math>, which is a dielectric material.</p>

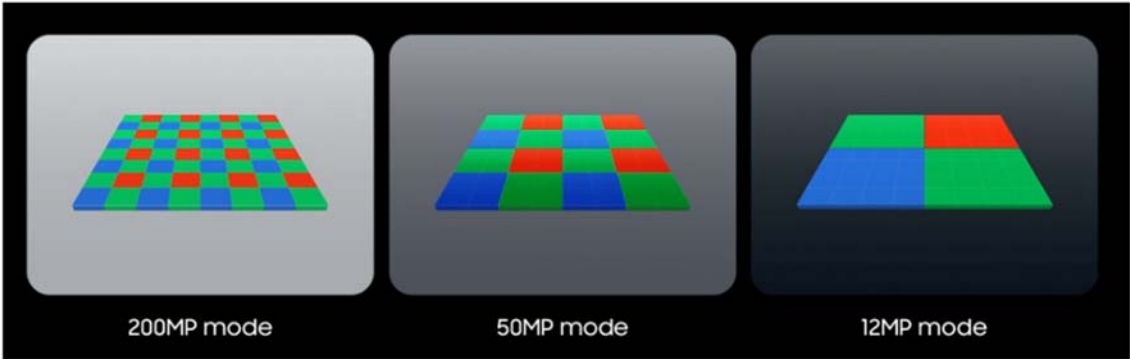
24	<p>The single-chip device of claim 1, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD.</p>	<p>The MSPD of Samsung's CIS Accused Products includes ohmic contacts configured for reverse-biasing the MSPD. As shown below, the annotated n- and p- contacts are designed to have very low contact resistance (meaning they are ohmic contacts). The p-contact and n-contact facilitate reverse biasing of the photodetector.</p>  <p>WWSSENS004710-WWSSENS004753 at 4751 (TEM showing VTG's (vertical transfer gates) are integrated into the photodetector).</p>
----	--	--

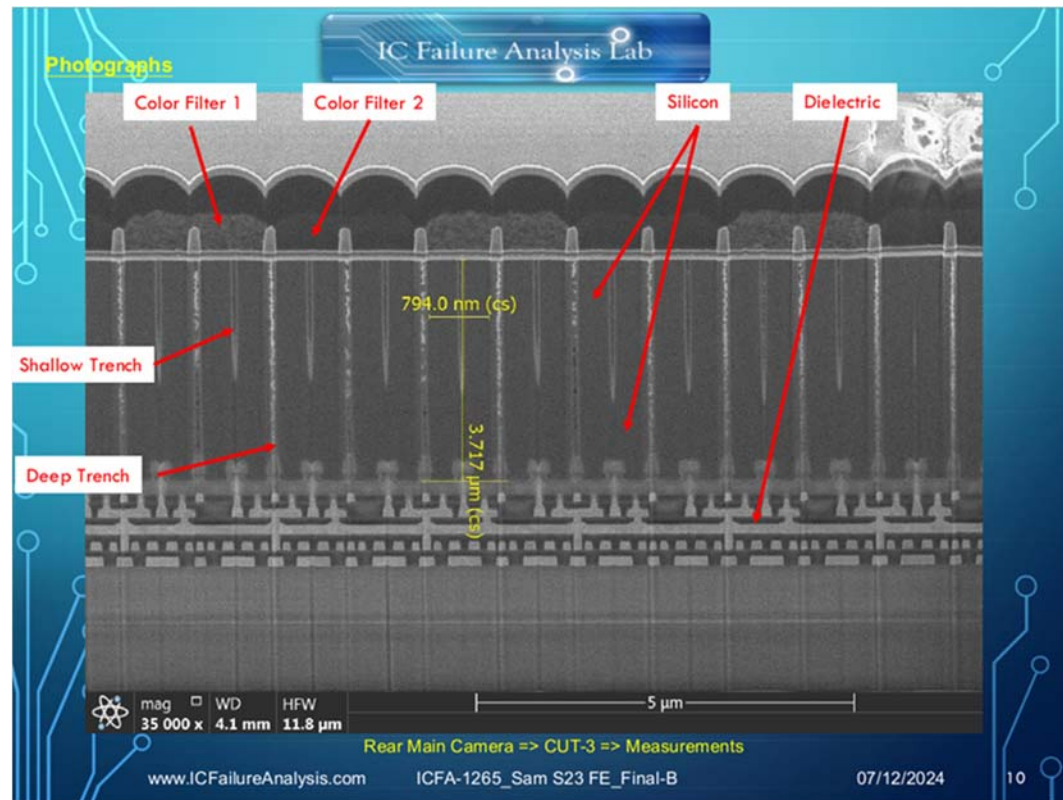
26	<p>The single-chip device of claim 1, further comprising a light guide to said MSPD for directing said optical input thereto, and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip device.</p>	<p>Samsung's CIS Accused Products include a light guide for directing the optical input and electrical contacts from the active electronic circuit configured to carry the processed output. The micro-lens directs the input light toward the center of the MSPD, thereby guiding the light, to avoid the metal grid. WWSSENS004710-WWSSENS004753 at 4723. This blocks the light and the p- and n-contacts conduct currents from the MSPD controlled by the gate signals to the VTGs. WWSSENS004710-WWSSENS004753 at 4751.</p>  <p>WWSSENS004710-WWSSENS004753 at 4723 (annotated to illustrate the effect of the micro-lenses to focus the light rays to the MSPDs).</p>
----	---	---



WWSSENS004710-WWSSENS004753 at 4751 (TEM showing VTGs (vertical transfer gates) are integrated into the photodetector; the p-contact and n-contact facilitate reverse biasing of the photodetector).



28	<p>The single-chip device of claim 1, further comprising one or more additional MSPD on or in the same substrate, and respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input.</p>	<p>Samsung's CIS Accused Products include additional MSPDs on the same substrate with different optical bandpass filters coupled the MSPDs, whereby the MSPDs are configured to respond to different wavelength ranges that are within the optical input. As shown below, Samsung's CIS Accused Products incorporate three different color filters (red, green and blue) to produce color images.</p> <p><b>Shoot at the Resolution You Need</b></p> <p>Do you think that all pictures need to be 200 million pixels? With the versatile ISOCELL, you don't need to worry. Specially designed with the Tetra<sup>2</sup>pixel technology, the ISOCELL HP2 within the Galaxy S23 Ultra ensures optimal quality by giving users resolutions from which to choose. It combines up to 16 individual pixels together into one, which then operates as one big pixel.</p> <p>Thus, the ISOCELL HP2 sensor provides 200MP, 50MP and 12MP output options that allow the user to change resolution depending on their needs. In its default mode, the ISOCELL HP2 produces a 12MP image by merging 16 pixels into one big pixel. When you need a photo that has ultra-high quality, you can choose 200MP mode and the ISOCELL HP2 produces the image with rich details.</p>  <p>WWSENS005064-WW005072 at 5068.</p>
----	--	--

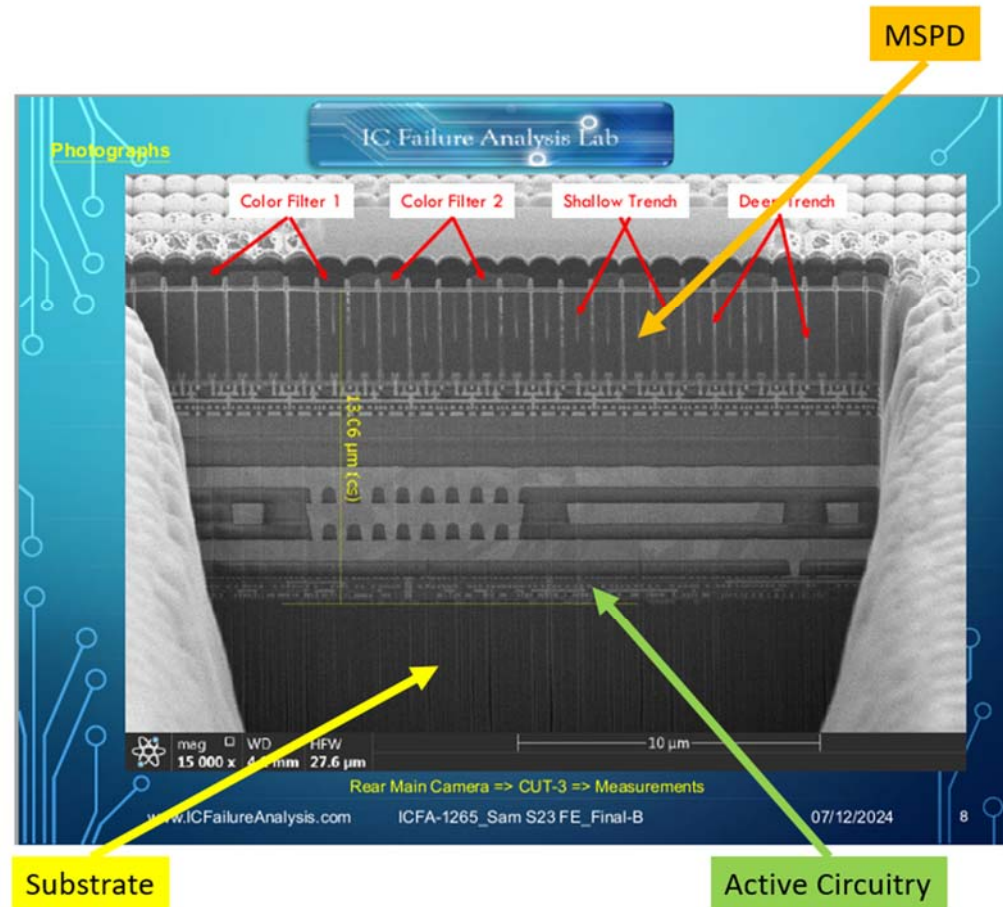


WWSSENS004710-WWSSENS004753 at 4720 (showing shallow and/or deep trenches covered with dielectric materials).

29

The single-chip device of claim 1, further comprising one or more additional MSPDs on or in said single substrate, one or more additional active electronic circuits on or in the said single substrate, and one or more additional communication channels configured to supply electrical outputs from the MSPDs to the one or more of the active electronic circuits.

Samsung's CIS Accused Products include additional MSPDs, active electronic circuits, and communication channels configured to supply electrical outputs from the MSPDs to the active electronic circuits. As shown below, Samsung's CIS Accused Products have more than one million photoreactors (pixels) to create raster color images, each of which has an MSPD, active electronic circuit, and communication channel on the substrate.



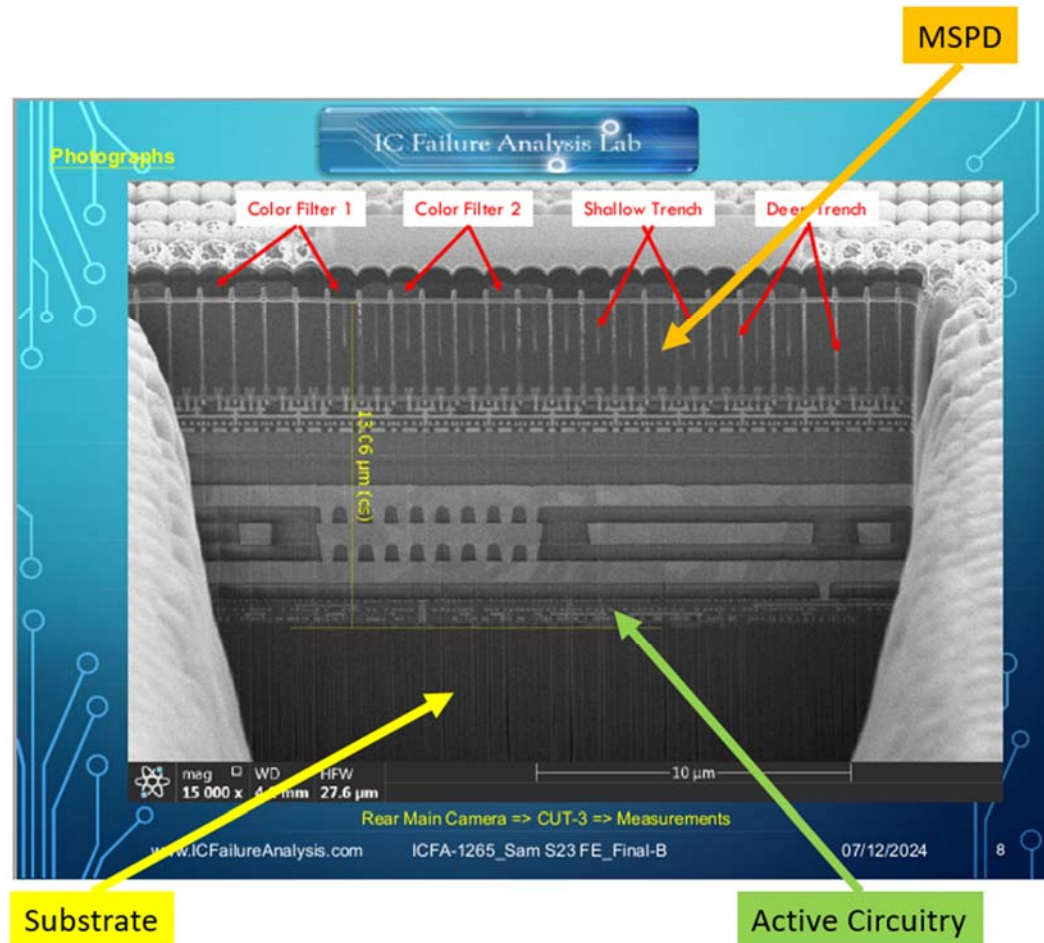
WWSSENS004710-WWSSENS004753 at 4720 (annotated to show MSPDs on the single substrate).



30

The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate.

Samsung's CIS Accused Products include additional active electronic circuits that are formed on the said single substrate. As shown below, a second chip containing active electronics circuits is bonded to the MSPD. WWSSENS004710-WWSSENS004753 at 4720.



WWSSENS004710-WWSSENS004753 at 4720 (annotated to show additional active circuit formed on the single substrate).

32	The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate and comprise one or more of CMOS, BiCMOS, and bipolar active devices.	<i>See</i> discussion of Claim 30. The second chip contains active CMOS electronic circuits.
----	--	--