

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Marvell Semiconductor, Inc.,

Petitioner,

v.

Credo Technology Group Ltd.,

Patent Owner.

IPR2025-01218

U.S. Patent No. 10,877,233

PETITION FOR *INTER PARTES* REVIEW

OF U.S. PATENT NO. 10,877,233

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 10,877,233 to Dai, et al. (“the ’233 patent”)
1002	Certified Prosecution File History for the ’233 patent (“Prosecution History”)
1003	Declaration of Michael Shuo-wei Chen
1004	U.S. Patent No. 9,882,706 to Lugthart, et al. (“Lugthart”)
1005	U.S. Patent No. 7,233,617 to Gorecki (“Gorecki”)
1006	U.S. Patent No. 8,516,238 to Cornelius, et al. (“Cornelius”)
1007	Samaan, High-speed Serial Bus Repeater Primer (“Samaan”)
1008	Ars Technica, Why Thunderbolt cables will be expensive until 2013
1009	Intersil, ISL37231 [Datasheet]
1010	U.S. Patent Application Publication No. 2019/0028262 A1 to Kobayashi, et al. (“Kobayashi”)
1011	TE Connectivity, SFP+ High Speed Copper Cable Assemblies
1012	Cisco, Cisco 40GBASE QSFP Modules Data Sheet
1013	AppleInsider, Intel details Thunderbolt, says Apple has full year head start
1014	macstories, Intel: Apple Transferring Thunderbolt Trademark To Us
1015	AnandTech, Intel’s Codename Light Peak Launches as Thunderbolt
1016	Ars Technica, The technology inside Apple’s \$50 Thunderbolt cable
1017	Gasca, et al., CMOS Continuous-Time Adaptive Equalizers for High-Speed Serial Links
1018	Declaration of June Munford re: Samaan
1019	Excerpts from 10G SFP+ Video
1020	Excerpts from Stauffer, High Speed Serdes Devices and Applications (“Stauffer”)
1021	PCI-SIG, PCI Express® Retimers vs. Redrivers An Eye-Popping Difference
1022	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 37 to Complaint, Credo’s Infringement Claim Chart Showing Molex’s Infringement of the ’233 Patent

Exhibit No.	Description
1023	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 40 to Complaint, Credo's Infringement Claim Chart Showing TE Connectivity's Infringement of the '233 Patent
1024	<i>Certain Active Electrical Cables and Components Thereof</i> , ITC Investigation 337-TA-1446, Exhibit 65 to Complaint, Credo's Domestic Industry Claim Chart for the '233 Patent
1025	SFF-8431 Rev 4.1 + Addendum
1026	Texas Instruments Technical Article, How to Reduce Jitter and Improve Signal Integrity in Source and Sink System Designs Supporting HDMI 2.0
1027	Intel, Thunderbolt™ Networking Bridging and Routing Instructional White Paper
1028	Intel, PCI Express Ethernet Networking White Paper
1029	U.S. Patent No. 9,231,846 to Sinha, et al. ("Sinha")
1030	<i>Reserved</i>
1031	U.S. Patent No. 8,787,430 to Rhagavan, et al. ("Raghavan")
1032	<i>Reserved</i>
1033	Intel, PCI Express Architecture
1034	Internet Archive Capture, The Wayback Machine, Wikipedia, "PCI Express"
1035	Intel Website Search Results

Petitioner Marvell is a leading supplier of retimer chips for active cables. Since 2013, ClariPhy and Inphi (Inphi acquired ClariPhy in 2016, and Marvell acquired Inphi in 2021) began filing and obtaining patents for active cable technologies. Those patents described active cable details, including a common serial communication technique called “pre-equalization.” Earlier active cables on the market—such as Apple and Intel’s Thunderbolt—also taught pre-equalization.

The ’233 patent, filed years later, identified the need for greater equalization in active cables and proposed pre-equalization as its point of novelty. But the Challenged Claims are invalid because this was widely known and used.

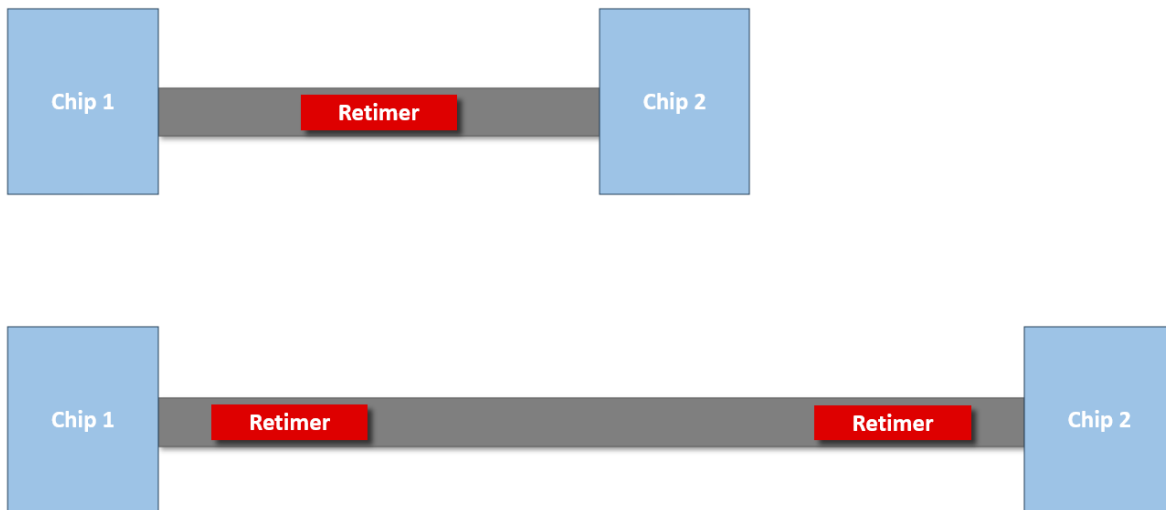
I. OVERVIEW OF THE TECHNOLOGY

High-speed serial communications became widespread in the 1990s as an alternative to parallel communications, which used multiple signal lines in parallel. As transmission speeds increased, parallel systems faced synchronization/routing challenges. Serial communication addressed these limitations by using a single channel, simplifying synchronization and reducing pin count. Ex-1003, ¶4.

By the early 2000s, computer busses and networks largely shifted to serial connections. Serial ATA (“SATA”) replaced parallel ATA; serial PCIe replaced parallel PCI; and Universal Serial Bus (“USB”) replaced legacy parallel interfaces. Ethernet had long utilized serial connections. Ex-1020, 000058-000061; Ex-1003, ¶5.

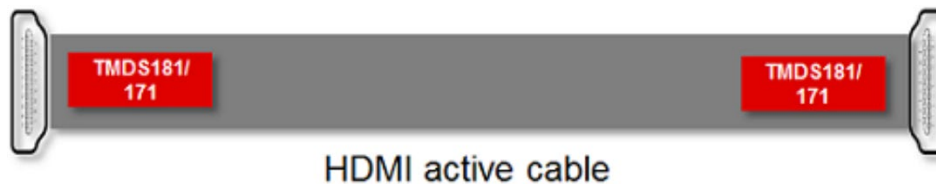
A. Active Cables

In serial communications, retimers were often used to extend link length and bandwidth by recovering digital data from the channel and re-modulating it. Ex-1021, 000001; Ex-1007, ¶¶15-16. This removed noise and effectively renewed the signal for longer distances.

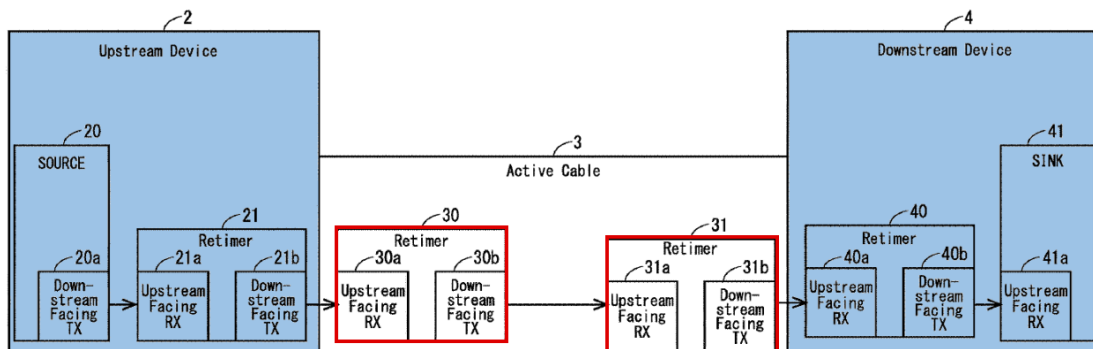


Ex-1003, ¶6.

Active electric cables extended the length of cables by incorporating retimers at each end of a cable. Ex-1010, ¶13. For example, Texas Instruments offered a retimer chip (TMDS181) for active HDMI cables. Ex-1026, Fig. 1:



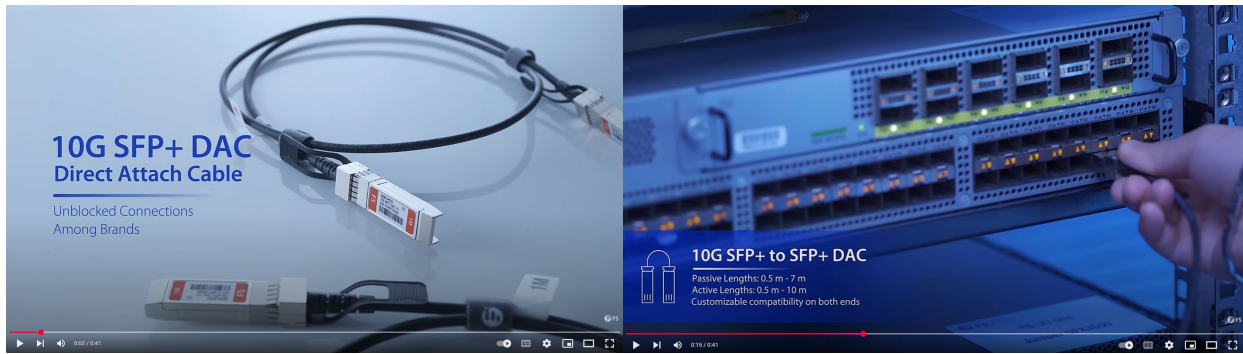
Active electric cables commonly included a retimer at each end. Ex-1010, Fig.1:¹



By 2015, active electric cables were used for a variety of protocols including DisplayPort, PCIe, USB, and Ethernet. Ex-1003, ¶7.

Ethernet has been a widely used networking standard since the 1990s. By the 2010s, Ethernet had become the primary high-speed serial communication standard for enterprise and data center networks, scaling from 1 Gigabit Ethernet (GbE) to widespread 10 GbE adoption. To support higher speeds and longer distances, manufacturers introduced active Ethernet cables with integrated retimers. By 2014, active Ethernet cables and components were available from various vendors. Ex-1011 (TE SFP+ cables); Ex-1012 (various Cisco products). Active Ethernet cables often used the SFP+ form factor for the modules at each end, connected by twinaxial cable. Ex-1019:

¹ All emphasis and annotations added unless stated otherwise.



```

{master:0}
root> show interfaces brief xe-0/0/40
Physical interface: xe-0/0/40, Enabled, Physical link is up
Link-level type: Ethernet, MTU: 1514, Speed: 10Gbps, Duplex: Full-Duplex,
Loopback: Disabled, Source filtering: Disabled, Flow control: Enabled
Device flags : Present Running
Interface flags: SNMP-Traps Internal: 0x0
Link flags   : None

Logical interface xe-0/0/40.0
Flags: SNMP-Traps 0x0 Encapsulation: Ethernet-Bridge
bridge

{master:0}
root>

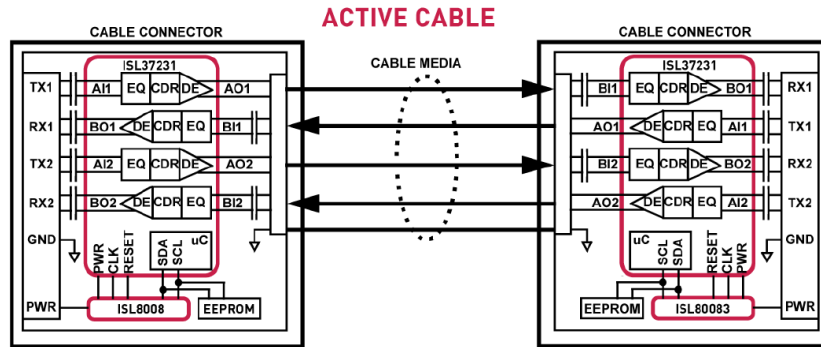
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The link is up

ethernet compatibility

Ex-1003, ¶¶8-9.

Thunderbolt, a high-profile active cable, was developed through a collaboration between Apple and Intel. Apple developed and marketed the cable (Ex-1014, 000002; Ex-1013, 000001-000002), while Intel provided the port and retimer architectures. Ex-1016, 000001-000002; Ex-1015, 000003. Macintosh computers featured Thunderbolt ports in 2011 (Ex-1013, 000001), with other vendors offering Thunderbolt solutions by 2013. Ex-1009, 000001; Ex-1008, 000003-000005 (discussing ISL37231 retimers for Thunderbolt).



Ex-1003, ¶10.

B. Pre-Equalization

As connection protocols transitioned to serial links, established serial communication techniques like pre-equalization were adopted. Well before 2018, pre-equalization was a standard topic in undergraduate courses on serial communications and routinely covered in relevant textbooks. Ex-1020, 000020-000024; Ex-1037, §1.1.1; Ex-1003, ¶¶11-12.

Pre-equalization was performed at the transmitter to adjust the signal prior to the signal being sent over the channel, compensating for anticipated signal loss. Equalization was also performed at the receiver to adjust for channel losses after the signal crossed the channel. This combination of pre-equalization at the transmitter and equalization at the receiver enabled robust, high-speed transmission across noisy channels. Ex-1020, 000020-000024; Ex-1003, ¶13.

Because channels attenuate different frequencies unevenly, pre-equalization selectively boosted signal frequencies expected to experience greater loss. This ensured the received signal more closely matched the original signal after crossing

the channel. Pre-equalization is illustrated below: the red boxes show the original waveform with and without pre-equalization. Ex-1020, 000021:

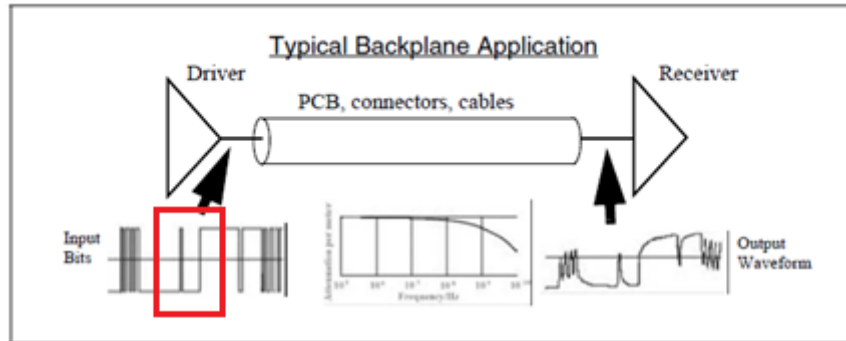


Fig. 1.9 Signal distortion for a typical channel application

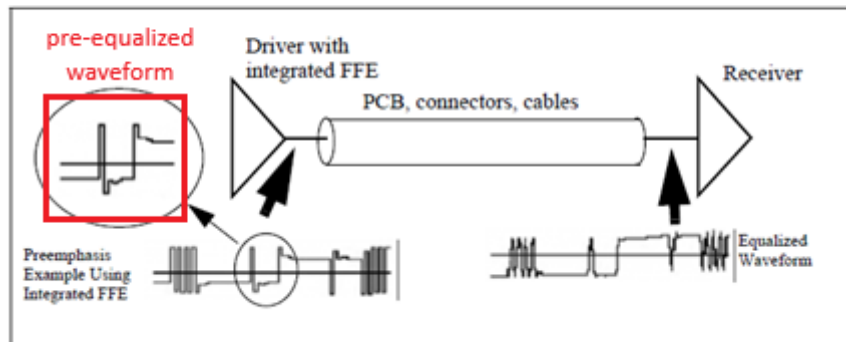


Fig. 1.10 Typical channel application with equalization at the transmitter

Ex-1003, ¶14.

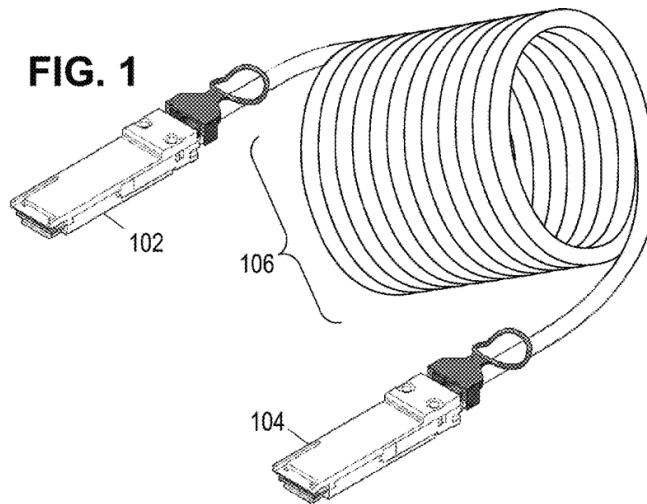
Pre-equalization was often implemented at the transmitter using a finite impulse response (“FIR”) filter. An FIR filter performs a weighted sum by multiplying adjacent data “taps” with coefficients. For pre-equalization, these coefficients are selected to amplify frequencies that the channel diminishes. As a result, the effects of the filter and channel cancel each other out, leaving the signal closer to its original form. Ex-1020, 000020-000021; Ex-1017, 000025-000027.

Ex-1003, ¶¶15-17.

It was common practice for equalization and pre-equalization filter coefficients to start with baseline values based on an estimated channel response; these coefficients could, in some cases, be subsequently updated during operation according to the actual channel conditions. Ex-1020, 000020-000021. These baseline coefficients were often programmed as fixed values. “[P]re-programmed or pre-set” equalizer coefficients were saved in various forms of nonvolatile memory. Ex-1005, 7:18-33; Ex-1003, ¶18.

II. THE '233 PATENT

The '233 patent is directed to an active electrical cable:



According to the patent, ever-higher data rates caused “increased channel attenuation and dispersion even as the equalizers are forced to operate at faster symbol rates.” Ex-1001, 1:15-28. For longer distances, data centers relied on “[a]ctive ethernet cable (AEC)” products with “hard-wired data recovery and

remodulation (DRR) chips in the cable connectors.” Ex-1001, 1:25-36. The patent admits these were used in the background art. Ex-1003, ¶20.

According to the ’233 patent, there was a need for increased levels of equalization as cable lengths extended. Ex-1001, 1:37-40. The patent purports to address this need with pre-equalization, “employing preset transmit-side equalization to provide enhanced performance and/or to reduce receive-side equalization requirements.” Ex-1001, 1:44-48, 1:61-63; Ex-1003, ¶21.

However, as explained above, pre-equalization was a textbook component of serial communication systems. Years before the ’233 patent, Petitioner’s own prior art included pre-equalization in active cables (Lugthart). Prior art from Apple and Intel likewise taught pre-equalization in active cables (Ground 4), and preset equalizer coefficients were both known and trivial. *See, e.g.*, Ex-1005, 7:18-33; Ex-1004, 29:21-28, 23:59-64, 9:39-49; Ex-1003, ¶22.

A. Prosecution History

The ’233 patent was granted without any rejections. Ex-1002, 000563. The Notice of Allowance (“NOA”) stated the prior art does not teach or suggest limitations [1f], [8f] and [15c]. Ex-1002, 000568-000571; Ex-1003, ¶23.

After allowance, the Applicant requested continued examination to submit an Information Disclosure Statement citing four Office communications from two separate patent applications. Ex-1002, 000591-000596. In less than a month, the

Examiner issued another NOA without addressing the new information in the IDS, indicating that “[n]o new art is cited” and concluding that the prior art did not teach limitations [1f], [8f], and [15c]. Ex-1002, 000668-000673, 000671; Ex-1003, ¶24.

B. Priority Date

This Petition analyzes invalidity as of June 21, 2019. Ex-1003, ¶26-27.

III. FIELD AND LEVEL OF ORDINARY SKILL

The field of the '233 patent is high-speed communications. The patent describes its background with high data rates over various physical mediums including twinaxial cable, fiber optics, and electrical backplanes, and then recognizes the demand for “ever-higher data rates.” Ex-1001, 1:16. The patent acknowledges that active Ethernet cables are used to provide “high-bandwidth data transport over distance” (Ex-1001, 1:25-36) and proposes improving high-bandwidth serial communications with pre-equalization. Ex-1001, 1:38-48. The patent’s embodiments describe numerous examples of high-speed communications, “e.g., the Ethernet standard for 400 Gbps” (Ex-1001, 3:63-4:1, Fig. 1), 200 Gbps, or 50 Gbps. Ex-1001, 4:23-45, Fig. 2; Ex-1003, ¶29.

A person of ordinary skill in the art (“POSITA”) would have been a person with a bachelor’s degree in electrical or computer engineering with at least three years of experience in the field (explained above). A person with less practical

experience but more relevant education may also meet this standard. Ex-1003, ¶¶30-31.

In the relevant timeframe, a POSITA with the above-described skill would have been able to:

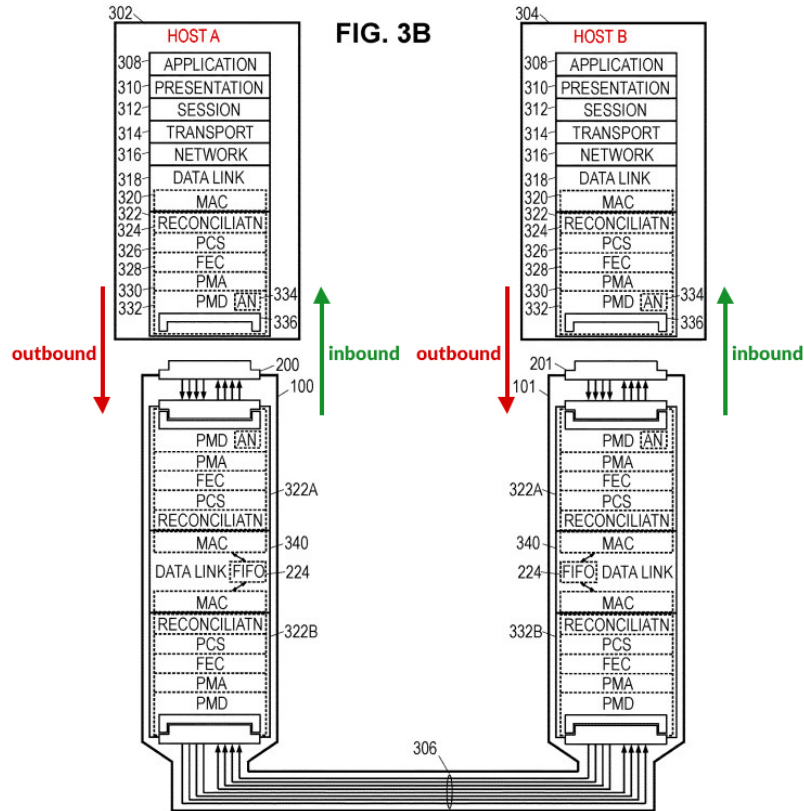
- Understand common high-speed serial components, e.g., equalization, CDR, pre-equalization, and FIR filters;
- Design high-speed serial communication systems;
- Design active electric cables;
- Design equalization/pre-equalization filters, including FIR filters and coefficients;
- Program DSPs to perform common transceiver functions; and
- Implement protocols for calibrating/setting equalization parameters.

Ex-1003, ¶32.

IV. CLAIM CONSTRUCTION

A. “inbound”/“outbound”

The '233 patent defines “inbound” and “outbound” from the host’s perspective. Ex-1001, 3:57-60 (“inbound ... to the host interface”; “outbound ... from the host”), 4:46-52, Figs. 3A-3B.



Ex-1003, ¶35.

V. INVALIDITY GROUNDS

Petitioner requests *inter partes* review and cancellation of the challenged claims on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1, 6, 8, 13, 15	§103	Lugthart
2	1-20	§103	Lugthart and Gorecki
3	7, 14, 20	§103	Lugthart, Gorecki, and Samaan
4	1-20	§103	Cornelius, Samaan, and Gorecki

The Grounds render the challenged claims obvious because any differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a POSITA to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

None of these references were considered during examination. Ex-1003, ¶25.

A. Grounds 1-3

For Ground 1, Lugthart teaches an active cable with all limitations of the independent claims and several dependent claims.

Ground 2 combines Lugthart and Gorecki. To the extent PO disputes Lugthart's teachings, Gorecki teaches preset equalizer coefficients stored in nonvolatile memories. For dependent claims, Gorecki also teaches a controller that reads and configures the coefficients, including at power-up.

For Ground 3, Samaan teaches a limitation for three dependent claims. Samaan is introduced in §V.B.2.

1. U.S. Patent 9,882,706 (“Lugthart”) (“Ex-1004”)

Lugthart is post-AIA §102(a) prior art; it was filed December 2016 and issued January 2018, claiming priority to December 2013. Lugthart is directed to an active cable with transceivers at each end. Ex-1004, Fig. 2A, 6:65-7:3.

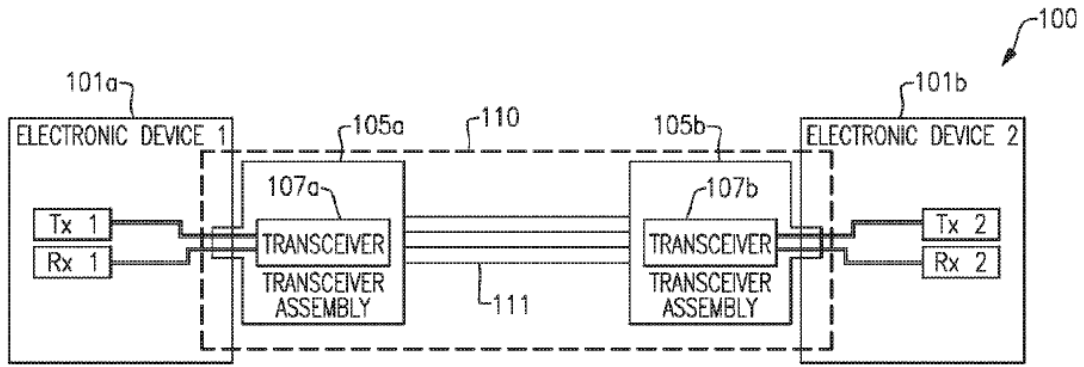


FIG.2A

Ex-1003, ¶40.

The transceivers use an FIR filter to perform “output pre-emphasis” on signals before transmission “to compensate for channel losses.” Ex-1004, 29:21-28, Figs. 1A.

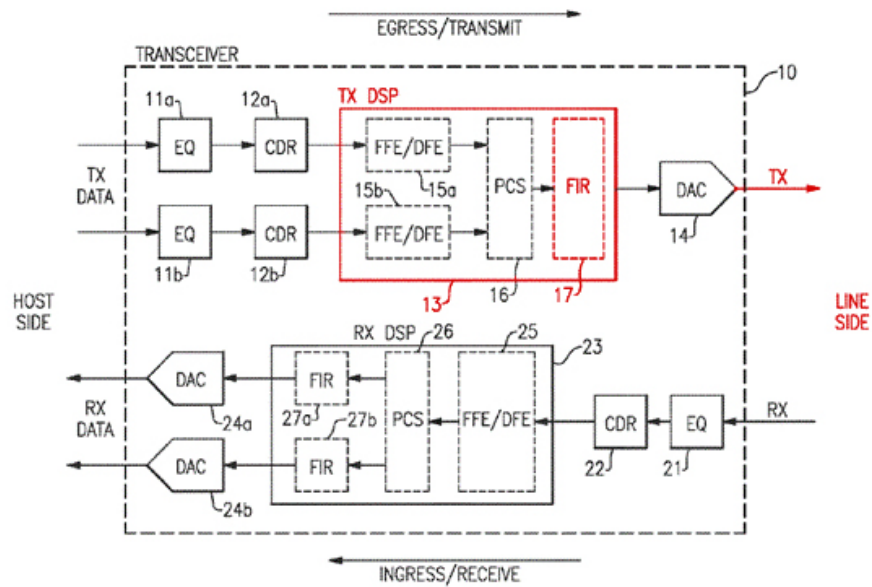


FIG.1A

Ex-1003, ¶41.

Lugthart is analogous art because it is in the same field. *Supra* §III.

Lugthart is directed to “methods for high speed communications” to “achieve reliable high-speed point-to-point communication[.]” Ex-1004, Abstract, 3:12-16, 4:10-12, 6:55-7:5, 14:29-31. Lugthart’s objective is to “establish high-speed point-to-point links[.]” Ex-1004, 47:24-27. Lugthart is also reasonably pertinent because it teaches pre-equalization/equalization for high-speed serial communications. Ex-1004, 23:59-24:2, 9:39-49, 47:24-27, Figs. 1A, 4B; Ex-1003, ¶42.

2. U.S. Patent 7,233,617 (“Gorecki”) (“Ex-1005”)

Gorecki is post-AIA §102(a) prior art; it was filed April 2003 and issued June 2007, claiming priority to October 2002.

Gorecki enhances high-speed serial communications over backplanes and cables (Ex-1005, 1:12-17) with transmitter “equalization circuitry” that includes multiple coefficients stored in nonvolatile memory, e.g., “EEPROM.” Ex-1005, 7:18-26, 3:11-15; Ex-1003, ¶44.

Gorecki is analogous art because it is in the same field (high-speed communications). *Supra* §III. Gorecki enhances the performance of “high-speed communication” over a cable and discloses a “high-speed digital communication system[.]” Ex-1005, Abstract, 3:11-15, 6:3-22, 8:1-4, Fig. 3. The ’233 patent addressed a problem where “equalizers are forced to operate at faster symbol rates”

and “increasing levels of equalization” increased receiver power consumption. Ex-1001, 1:15-20, 1:36-40. The ’233 patent addresses this with preset transmit-side equalization. Ex-1001, Abstract, 1:44-50. Gorecki is reasonably pertinent to this problem; Gorecki recognizes similar challenges where “increase[s] in data rate[s]” make it more difficult to recover the transmitted signal (Ex-1005, 1:17-24) and provides solutions using transmit-side equalization and “pre-set” coefficients stored in nonvolatile memory. Ex-1005, Abstract (“[T]ransmitter includes equalization circuitry ... in high-speed digital communication systems.”), 1:12-17, 7:18-33. Ex-1003, ¶45.

3. Claim 1

For each of the following limitations, the “first” and “second” designations can be swapped between elements at either end of the cable. Lugthart’s active cable is symmetric; each side has identical components and operation. Ex-1003, ¶46.

[1pre] A cable that comprises:

Lugthart describes a high-speed communication link that includes “a cable.” E.g., Ex-1004, 6:65-7:5, 3:12-4:13, Figs. 2A-4A. The cable further includes the elements discussed below for [1a]-[1f]. Ex-1003, ¶¶48-49.

[1a] a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;

Lugthart teaches a **first DRR device**. For example, Lugthart discloses “a pair of transceivers provided at respective ends of the cable.” Ex-1004, 6:65-7:3, Figs. 2A, 4A. Figure 1A details transceiver internals. Either transceiver would be a first DRR device, as explained below.

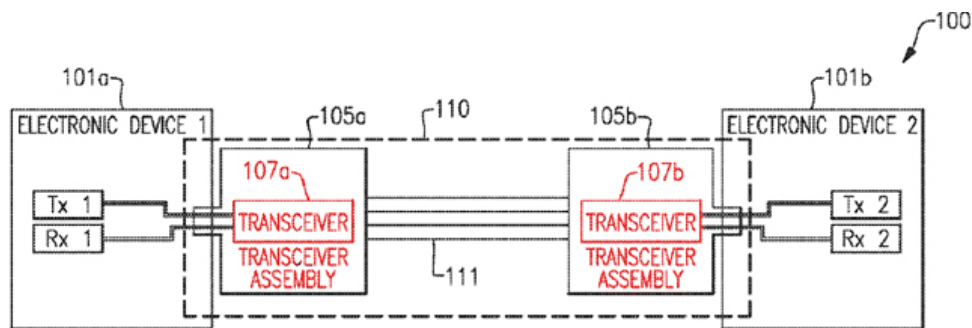


FIG. 2A

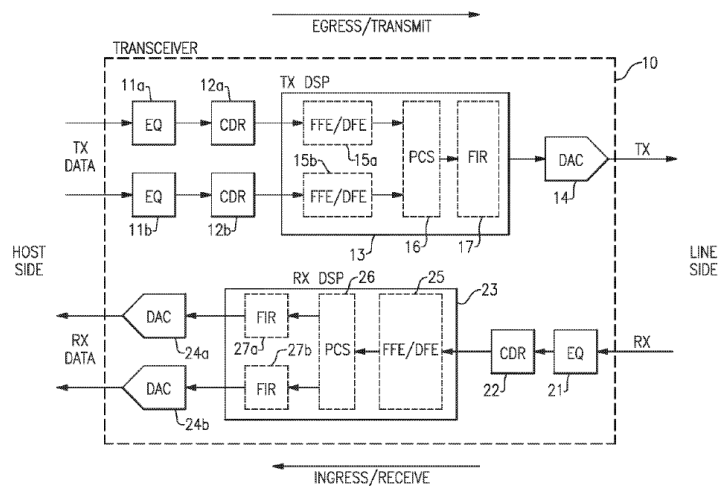
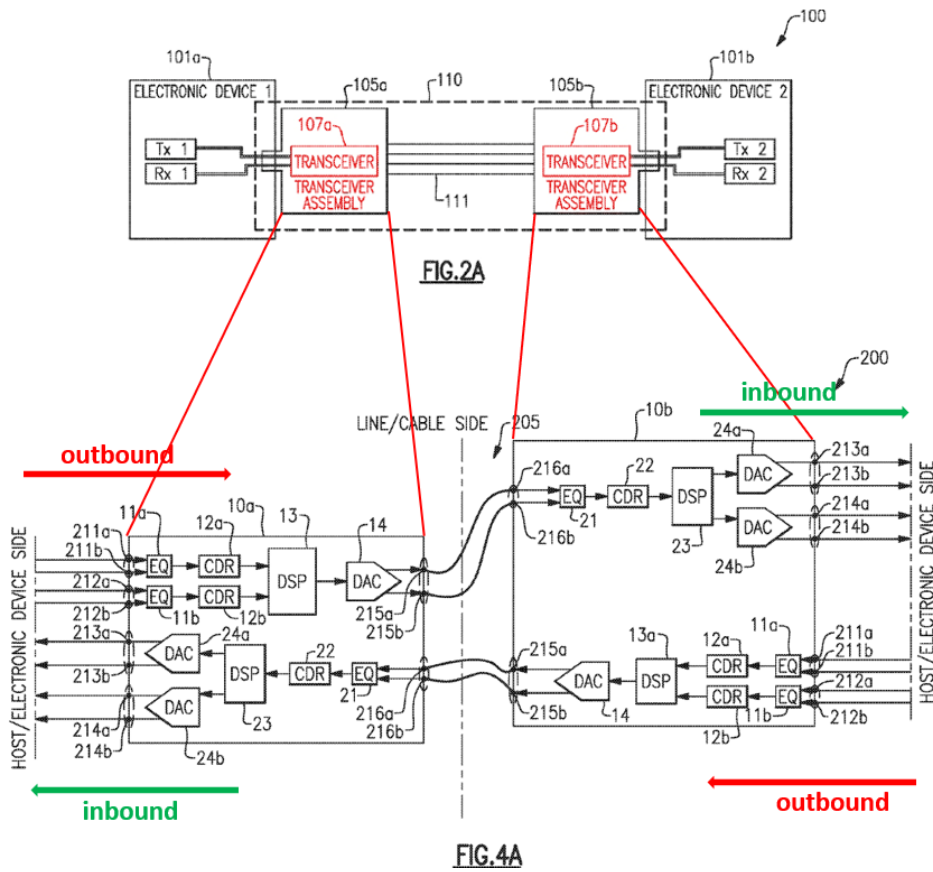


FIG. 1A

Ex-1003, ¶¶50-51.

Figure 4A illustrates transceiver internals for both sides of the active cable, annotated below. Ex-1004, 7:67-10:22, 19:34-64.



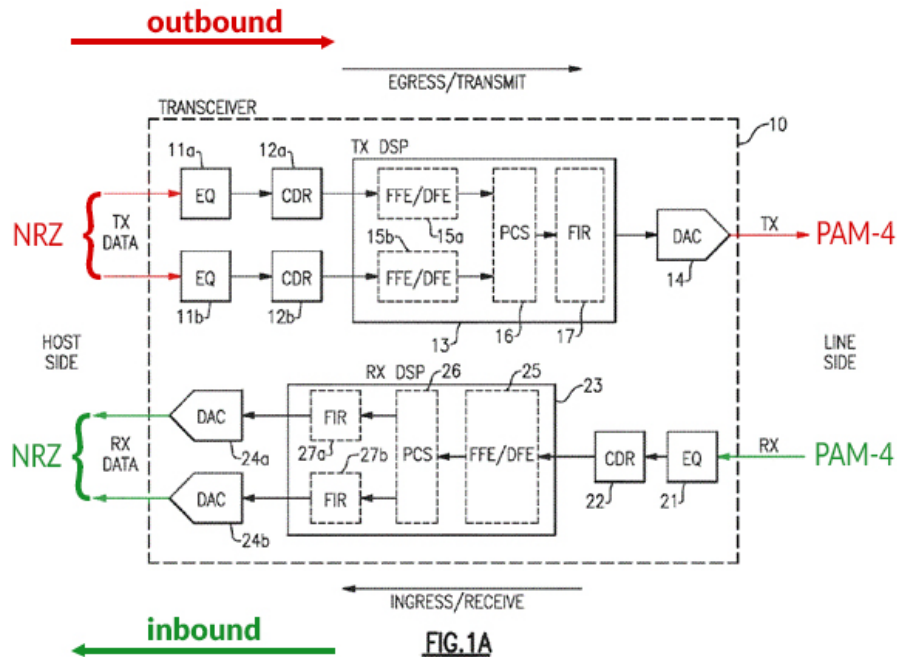
Ex-1003, ¶51.

Each transceiver includes “a first transmit path clock and data recovery (CDR) circuit” and “a second transmit path CDR circuit[.]” Ex-1004, 7:66-8:7, 1:63-2:3, 9:26-37, 21:35-46, 33:23-28, Figs. 1A, 4A-4B, 8. These CDR circuits “perform clock and data recovery operations” (Ex-1004, 9:26-28), and “recover

data in data streams generated by...transmit path equalizers.” Ex-1004, 9:34-37.
Ex-1003, ¶52.

After data recovery, the transceiver performs remodulation. Lugthart teaches a “multi-level modulation encoding” process in which “each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable,” or “vice versa.” Ex-1004, 7:13-33, 8:48-60, 15:64-16:10, 23:44-24:23, Figs. 1A, 4B. In other words, Lugthart’s transceiver recovers data from an NRZ signal from the host and then remodulates the recovered data signal into PAM-4 over the cable (for the outbound direction), or vice versa for the inbound direction to the host.² Therefore, Lugthart’s transceiver performs remodulation by converting a data signal for transmission over a communications channel (e.g., outbound over the cable or inbound over the path to the host).

² Likewise, in the ’233 patent embodiments, the DRR devices “convert[] 1 lane of PAM4 symbols into 2 lanes of NRZ symbols[.]” Ex-1001, 4:43-45.



Ex-1003, ¶53.

Figures 6A-6B further explain the process of data recovery and remodulation. The transceivers “recover[] ... digital data signals” and then convert it “to an analog differential signal having a suitable modulation format[.]” Ex-1004, Figs. 6A-6B, 30:20-31:22.

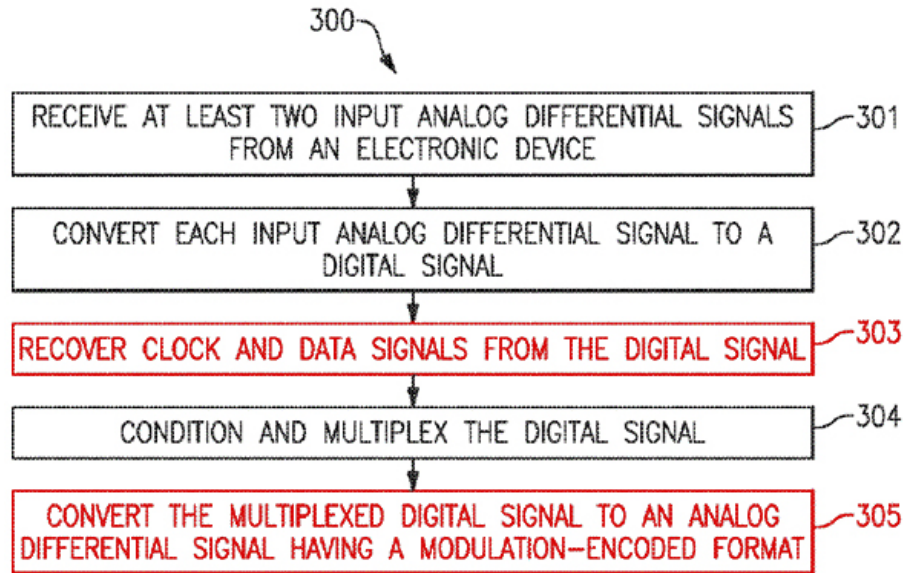


FIG.6A

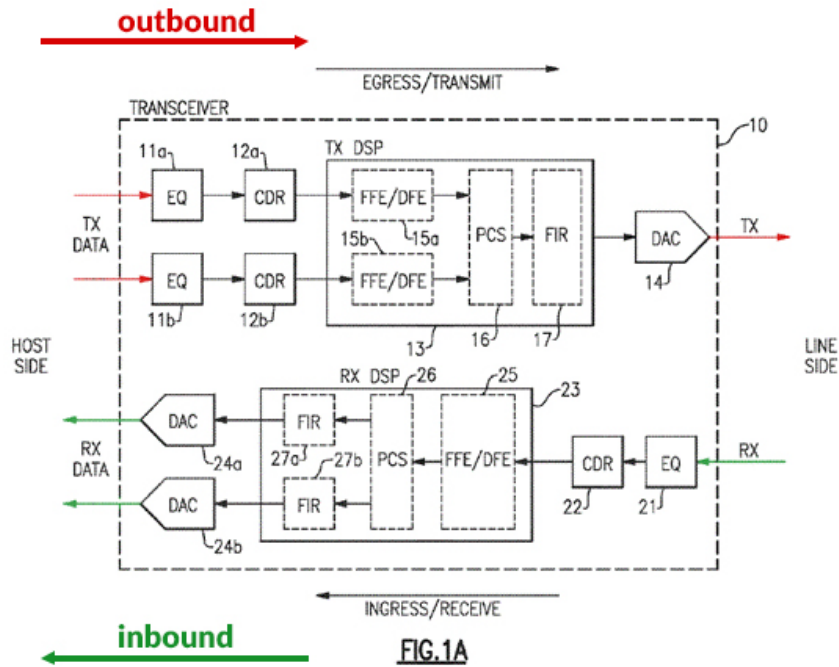
Ex-1003, ¶54.

The DRR device (e.g., transceiver) **exchanges inbound and outbound multi-lane data streams**. Each transceiver includes an “egress/transmit path” “capable of receiving...signals on the host side and multiplexing these signals...for transmission to the line side over the cable.” Ex-1004, 8:48-60, 15:64-16:3, 19:56-64, Figs. 1A, 2A, 4A. From the host’s perspective,³ this constitutes an exchange of outbound data streams with the transceiver (from host to transceiver). Lugthart also includes a path going the other way: each transceiver includes an “ingress/receive path” that is “capable of receiving ...on the line side and de-

³ The ’233 patent defines inbound/outbound from the host’s perspective.

Supra §IV.A.

multiplexing this signal...for communication to the host side.” Ex-1004, 8:48-60, 16:11-15, 19:56-64, Figs. 1A, 2A, 4A. From the host’s perspective, this constitutes an exchange of inbound data with the transceiver.



Ex-1003, ¶55.

The inbound/outbound streams are multi-lane data streams. Lugthart’s transceiver has more than one lane for host-side data streams, including “two” or “four host-side 10 Gbps NRZ data streams” in each direction. Ex-1004, 7:21-30, 13:13-48, 23:50-58, Figs. 1A, 4B. Therefore, the transceiver exchanges multi-lane data streams in each direction at the host interface. Ex-1003, ¶56.

The DRR device exchanges inbound/outbound data streams **with a first host interface port via a first end connector plug** (e.g., at one end of the cable).

Lugthart also describes the transceiver assembly as a pluggable module, where “[t]he first pluggable module can include a first transceiver[.]” Ex-1004, 4:10-14, Fig. 2A, 15:30-31 (each transceiver “enclosed in a packaging”). The pluggable module exchanges “host-side signals[.]” Ex-1004, 4:13-19. Each transceiver assembly “has an input port that is configured to mechanically and electrically connect...to a corresponding port or other interface on the respective electronic device[.]” Ex-1004, 14:14-15 (referring to electronic devices 101a and 101b as “host devices”), Fig. 2A, 15:42-47.

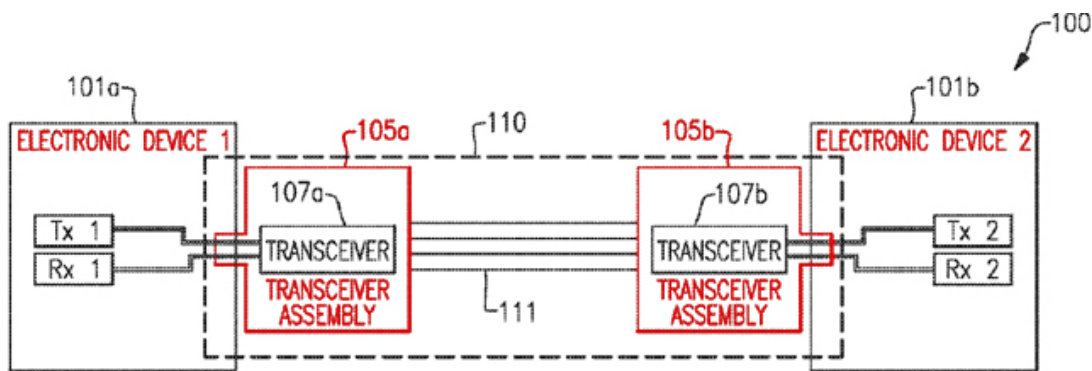


FIG. 2A

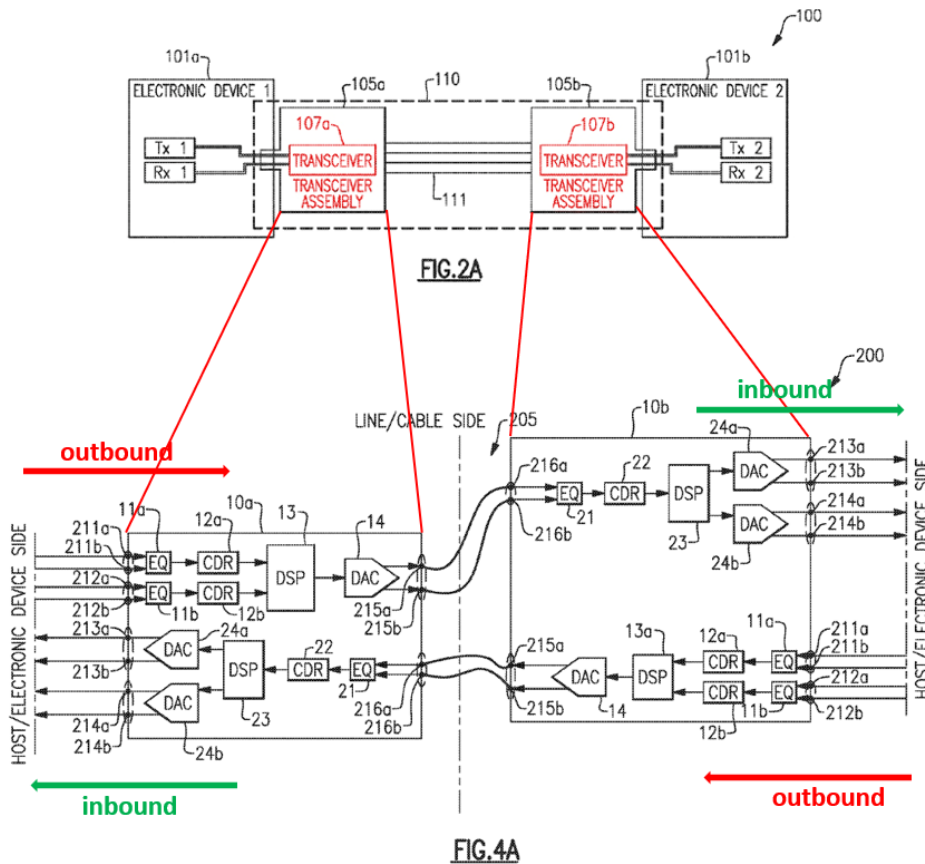
Ex-1003, ¶57.

Lugthart teaches that the input port includes a pluggable connector compliant with, e.g., SFP, SFP+, or QSFP. Ex-1004, 15:47-52. These pluggable connectors allow the transceiver assembly’s input port to be connected to the host interface port “in a releasable fashion.” Ex-1004, 15:42-52; Ex-1003, ¶¶58-60.

[1b] second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug

Limitation [1b] mirrors [1a] but changes “first” to “second.” Ex-1003, ¶61.

Lugthart teaches a cable with two symmetric DRR devices (e.g., two transceivers, one at each end). Each cable has “a pair of transceivers provided at respective ends,” and Lugthart’s teachings apply to both. Ex-1004, 6:65-7:3, 7:13-20, 14:7-31, 19:34-40 (both transceivers implemented “in a manner similar to that of the transceiver 10 of 1A.”), Figs. 1A, 2A, 4A.



Ex-1003, ¶62.

Either transceiver would be the first DRR device; the other would be the second. The corresponding interface port and plug would be the second host interface port and end connector plug. Therefore, the analysis from [1a] also applies here to [1b]. *Supra* §V.A.3[1a]; Ex-1003, ¶¶63-64.

[1c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,

Lugthart teaches **electrical conductors connecting the first and second DRR devices**. Lugthart’s active cable that includes “electrical conducting lines” which connect the first/second DRR devices (e.g., transceivers) at opposite ends of the cable. Ex-1004, 16:11-15, 14:29-42, 19:34-48, Figs. 2A, 4A.

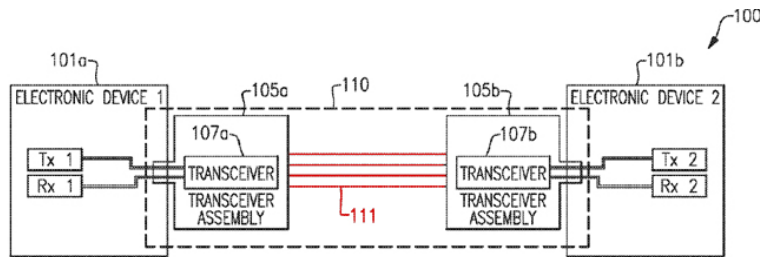


FIG. 2A

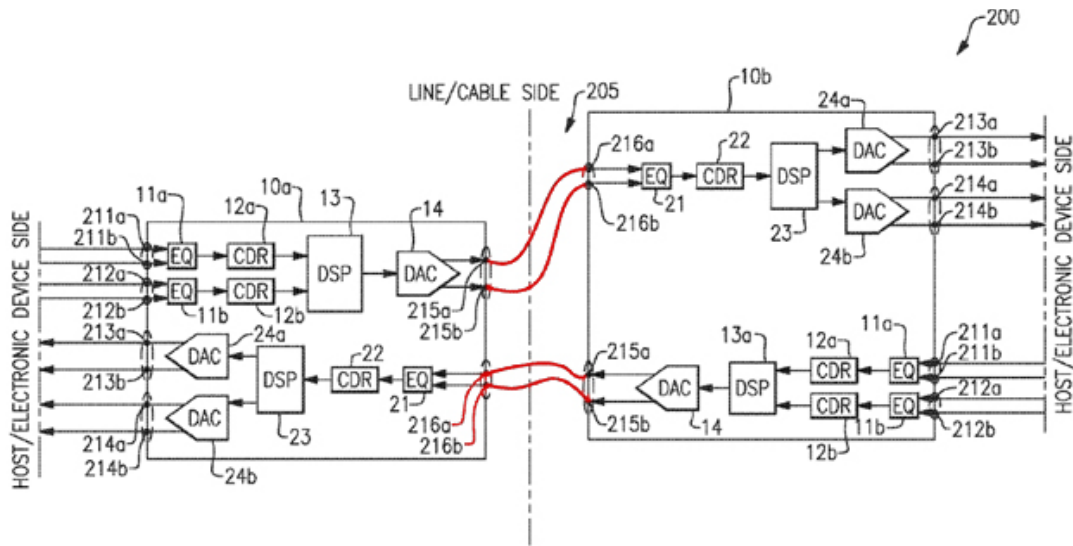


FIG.4A

Ex-1003, ¶65.

The cable includes two pairs of “conducting lines,” each including micro coaxial cables with inner and outer conductors. Ex-1004, 17:43-56, 18:40-63, Figs. 3A-3B.

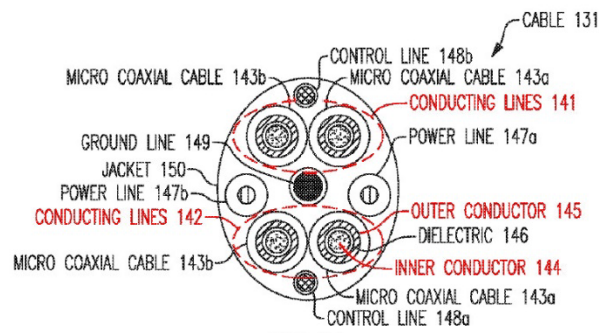


FIG.3A

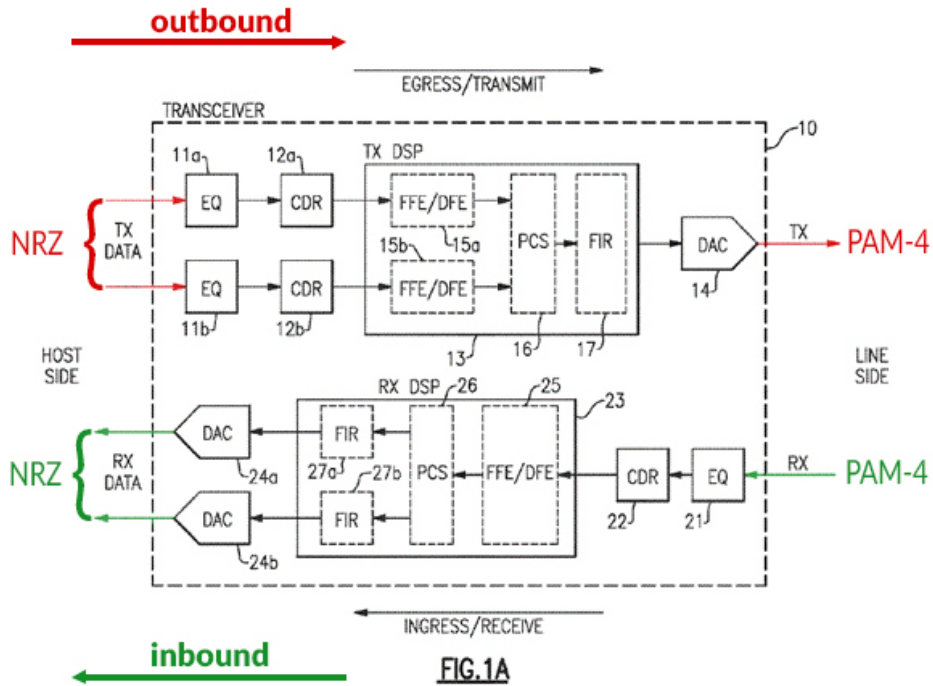
Ex-1003, ¶66.

The conductors **convey electrical transit signals** between the DRR devices. The “electrical conducting lines” “transport electrical signals between” the two transceivers. Ex-1004, 16:11-15, 4:11-13; Ex-1003, ¶¶67-68.

[1d] first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and

Lugthart teaches **the first DRR device** (e.g., transceiver) **converting between said electrical transit signals** (which are sent over the cable) **and said inbound and outbound multi-lane data streams for the first host interface port**. Each transceiver converts between (1) the NRZ signals of the inbound/outbound data streams for the host interface, and (2) PAM-4 electrical transit signals on the cable side. Ex-1004, 7:13-33 (receiving “(NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via ... (PAM-4) for transmission over the cable,” or “vice versa”), 8:48-60, 15:64-16:10, 23:44-24:23, Figs. 1A, 4B.⁴

⁴ The '233 patent confirms that this falls within its scope. In the specification, the DRR devices perform “format conversion” by “converting 1 lane of PAM4 symbols into 2 lanes of NRZ symbols, and vice versa.” Ex-1001, 4:43-45.



Ex-1003, ¶69.

The host-side of the transceiver includes inbound/outbound multi-lane data streams exchanged with the first host interface port, explained previously. *Supra* §V.A.3[1a]; Ex-1004, 8:48-60, 15:42-47; Ex-1003, ¶¶70-71.

[1e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,

Limitation [1e] mirrors [1d] but changes “first” to “second.” The analysis for [1d] (*Supra* §V.A.3[1d]) also applies here because Lugthart teaches a cable with symmetric DRR devices (e.g., transceivers), one at each end. *Supra* §V.A.3[1b] (explaining symmetry). Either transceiver would be the first DRR

device; the other would be the second, with corresponding second host interface port, for reasons explained previously. Ex-1003, ¶¶72-73.

[1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

Lugthart teaches **the first and second DRR devices** (e.g., transceivers at respective ends of the cable) **providing pre-equalization of the electrical transit signals**. The DRR devices were explained above. *Supra* §V.A.3[1a]-[1b]. The transceiver at one end is the first DRR device; the other is the second. Ex-1004, 19:34-40, 6:65-7:3, Fig. 4A.

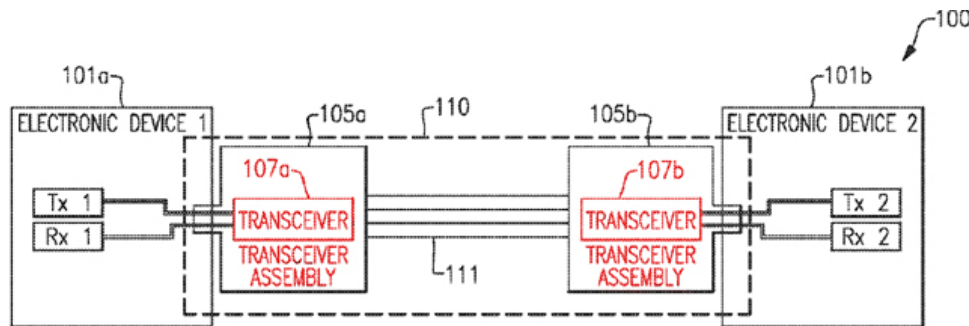


FIG. 2A

Ex-1003, ¶74.

Each transceiver performs pre-equalization using “output pre-emphasis” on electric signals that are to be transmitted over the cable. Ex-1004, 29:21-28.

Before transmission, an FIR filter within DSP 13 performs “emphasis on the signal to compensate for channel losses.” Ex-1004, 23:59-64, 9:39-49, Figs. 1A, 4B.

“DSP 13 can include additional processing...to further process signals” including

“de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies”; this is also pre-equalization. Ex-1004, 23:66-24:2, Fig. 4B; Ex-1003, ¶75.

“Pre-emphasis” is the most common way to perform pre-equalization, so much so that they are often used interchangeably. *See, e.g.*, Ex-1020, 000020-000021, Fig. 1.10 (describing “[p]re-emphasis” as “equalization at the transmitter”); Ex-1031, 2:39-42. “De-emphasis” is another way to perform pre-equalization by attenuating certain frequency components instead of boosting them. Lugthart uses pre-emphasis, with an option of also using de-emphasis, to perform pre-equalization by shaping the signal before transmission to account for anticipated channel losses. Ex-1003, ¶76.

This is illustrated in Figure 4A, which depicts the DSP in each transceiver, which as explained by Figures 1A and 4B, includes an FIR filter in the egress path for pre-equalization before transmission. Ex-1004, 23:59-24:2, 9:39-49, 19:34-40.

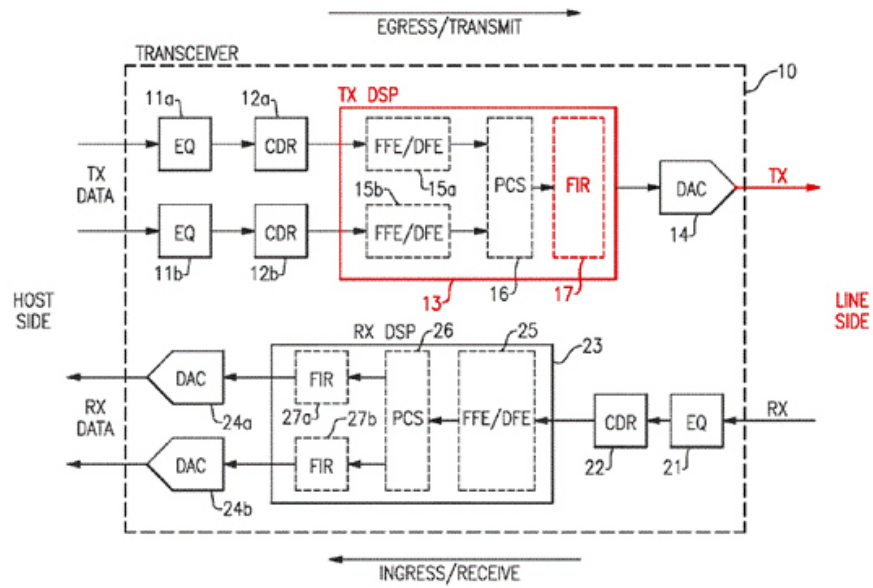


FIG. 1A

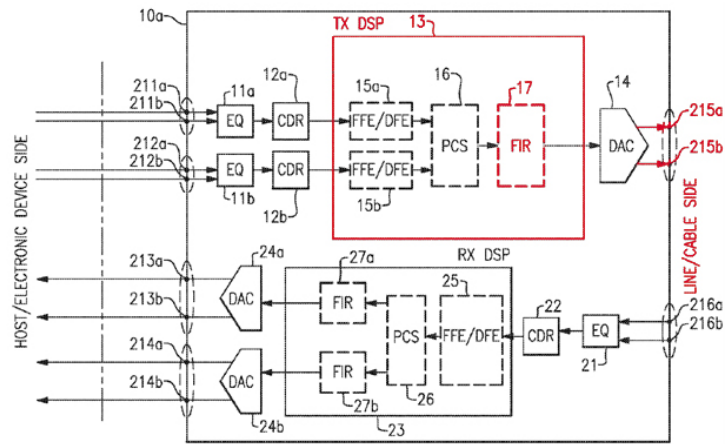
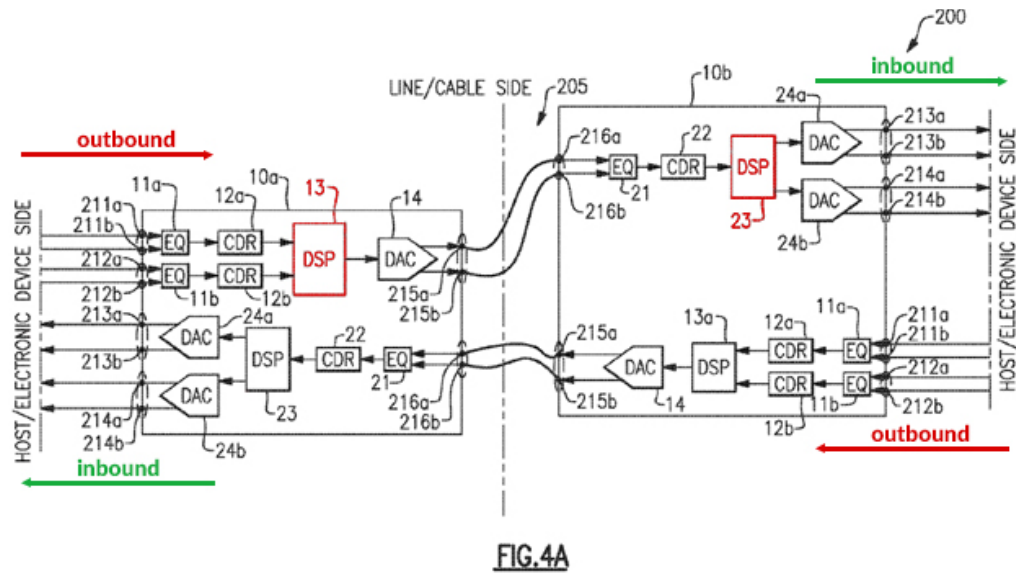


FIG. 4B



Ex-1003, ¶77.

The transceivers provide pre-equalization **using transmit filter coefficient values stored in nonvolatile memories**. The transceivers use an FIR filter for pre-equalization in the transmit path; this is a transmit filter. Ex-1004, 23:59-64 (using FIR filter to “condition” and “forward” signal for transmission), 9:38-51, 8:19-22, Figs. 1A, 4B. The FIR filter contains “tap coefficients” (Ex-1004, 22:13-17) and is implemented on a DSP. Ex-1004, Figs. 1A, 4A-4B (“TX DSP”), 7:67-8:7, 9:38-10:3; Ex-1003, ¶78.

Lugthart teaches or suggests storing the coefficients in nonvolatile memory. Lugthart teaches using software with a DSP (Ex-1004, 56:62-57:30) and teaches implementation as “computer programs ... encoded on a computer storage media[.]” Ex-1004, 57:30-39. This includes nonvolatile memories such as “ROM, EEPROM, ... or any other medium ... to store desired program code in the form of

instructions or data structures[.]” Ex-1004, 57:40-67. Because Lugthart’s FIR filter is implemented on its DSP, Lugthart teaches storing its FIR software program in nonvolatile memory, including FIR “instructions” and “data structures,” which would include the FIR coefficients used to perform the operations taught by Lugthart. Ex-1004, 57:40-67, 22:13-17, Fig. 4B; Ex-1003, ¶¶78-79.

If Patent Owner (“PO”) argues that FIR coefficients are somehow not part of the instructions/data for FIR software, a POSITA would have been motivated and found it obvious to store the FIR coefficients in nonvolatile memory. *See* Ex-1004, 57:40-67. It would not make sense to store some portions of the FIR program while excluding the coefficients, which are needed for FIR filter operation. Storing the coefficients was the simplest and fastest way to implement Lugthart’s teachings (*see id.*), and it allowed the coefficients to be quickly loaded at power-on as baseline parameters (further explained below for Ground 2). Manual re-entry of the coefficients with each reconnection would be impractical, especially given the straightforward nature of storing coefficients in memory that would already include the rest of the FIR DSP program. Even if that initial storage of coefficients is performed manually, subsequent uses of the cable would simply load the stored parameters. Ex-1003, ¶¶80-82.

Ground 2: Gorecki teaches storing coefficients in nonvolatile memory

To the extent PO disputes Lugthart's teachings for storing coefficients, Gorecki teaches it. *Supra* §V.A. Like Lugthart, Gorecki teaches transmitter pre-equalization that conditions the signal before transmission to compensate for channel losses. Ex-1005, Abstract, 3:8-38, 8:1-8, 6:3-9, Fig. 3; Ex-1003, ¶83.

Gorecki teaches pre-equalization circuitry comprising an FIR filter with multiple tap coefficient values. Ex-1005, 6:38-41, 9:3-15. Gorecki further teaches storing "pre-programmed"/"pre-set" tap coefficient values in nonvolatile memories, including "ROM, PROM, EPROM, [or] EEPROM[.]" Ex-1005, 7:18-26.; Ex-1003, ¶¶84-85.

Motivation to Combine. A POSITA would have been motivated to apply Gorecki's teachings to store FIR coefficient values in nonvolatile memories. Ex-1003, ¶86. First, Lugthart teaches coefficient values, which, like all computer data, would naturally be stored in memory. There are two types of memory: (i) volatile (data lost when unpowered) and (ii) nonvolatile (data retained without power). A POSITA would have chosen nonvolatile memory as one of two solutions, with predictable results and a reasonable expectation of success, given the longstanding use of nonvolatile memory types (e.g., EEPROM) taught by Gorecki. Lugthart motivates this choice by teaching software implementations where

instructions/data are stored in nonvolatile memory, as previously explained. Ex-1004, 57:40-67, Figs. 1A, 4A-4B, 7:67-8:7, 9:38-10:3; Ex-1003, ¶87.

Moreover, a POSITA would have been motivated to use *nonvolatile* memory to store Lugthart's coefficients, so that they are preserved when the cable is disconnected—a common scenario for Ethernet cables—and available for subsequent use in the manner taught by Lugthart. Ex-1004, 22:13-17, 23:59-24:2, 24:23-29. If stored only in volatile memory, the coefficient values would be lost whenever the cable is disconnected and the transceivers lose power, such as during shipping or when connecting to different devices. In cases where coefficients are manually determined and entered for a specific deployment, storing them in nonvolatile memory allows the coefficients to be saved for future uses, without recalculation or re-entry. This was a combination of prior art elements (e.g., nonvolatile memory) according to known methods to yield predictable results (e.g., data stored in memory). Ex-1003, ¶88, ¶93.

Nonvolatile storage would also have allowed the cable to immediately access and use the coefficients upon connection, which saves time. Even if link training is used to fine-tune coefficients during operation (Ex-1005, 7:50-61), a POSITA would nonetheless have been motivated to start with a baseline set of coefficients as a default on initial power-up, providing immediate equalization and reducing adjustment time. Therefore, a POSITA would have been motivated to

use nonvolatile memory to have coefficient values readily available whenever the cable is connected. Ex-1003, ¶88.

Furthermore, given the storage of coefficients in memory, a POSITA would have applied Gorecki's teachings of a controller to distribute coefficients to a "transmitter or set of transmitters." Ex-1005, 7:14-17. Each transceiver in Lugthart includes two DSPs and two transmitters (one in each direction). Ex-1004, Fig. 1A. Having a controller configure both, as Gorecki teaches, simplified configuration and required only a single controller to access the memory, rather than multiple DSPs; controllers were routinely used for these types of configuration purposes. Therefore, a POSITA would have been motivated to apply Gorecki's teachings and use a controller to read the requisite coefficient values from memory when the cable is plugged in (and thus powered on) and then to configure the FIR filters with the FIR coefficient values. Ex-1005, 7:1-33, 9:3-15; Ex-1003, ¶89.

Additionally, Lugthart and Gorecki both teach high-speed communications over a cable. Ex-1004, Abstract, 3:12-16, 4:10-12, 6:55-7:5, 14:29-31; Ex-1005, Abstract, 1:12-17. Both describe signal loss over the cable, and address it with pre-emphasis, using an FIR filter, in the transmitter. Ex-1004, 22:3-17, 23:13-64, 29:21-28; Ex-1005, Abstract, 3:8-16, 6:38-41, 9:3-7. Given these similarities, the combination would not have changed the principle of operation of either reference.

It simply uses a known technique (storing data in nonvolatile memory) to improve similar devices in the same way. Ex-1003, ¶¶90-91.

In addition to the reasons explained earlier in this section, a POSITA would have had a reasonable expectation of success because computers have, for decades, stored values in nonvolatile memory, e.g., EEPROM. This was a trivial implementation detail well within the level of ordinary skill. *Supra* §III; Ex-1003, ¶92.

4. Claim 2

<p>2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.</p>
--

The combination of Ground 2 was explained previously. *Supra* §V.A, §V.A.3[1f] (Motivation subsection). Ground 2 teaches a DRR device providing pre-equalization using transmit filter coefficient values stored in the nonvolatile memories. *Supra* §V.A.3[1f]; Ex-1003, ¶94.

Gorecki teaches **a first controller that configures the first DRR device in response to a power-on event**. Gorecki teaches a “controller” that distributes tap coefficients to the transmitter. Ex-1005, 7:1-17. Gorecki also teaches storing coefficients in memory and retrieving necessary information from memory at “start-up/power-up” events. Ex-1005, 7:14-33. This would have included the tap coefficients used for filter operation. Ex-1005, 7:14-33, 9:3-15. When a controller

is present, it would naturally read these coefficients from memory to configure the transmitters because controllers were commonly used for device configuration. *See* Ex-1005, 7:1-17. A POSITA would have found it obvious to add a controller to Lugthart’s active cable for reading and configuring transmitter coefficients. *Supra* §V.A.3[1f] (Motivation subsection); Ex-1003, ¶95.

Gorecki teaches **the first controller retrieves the transmit filter coefficient values from the nonvolatile memories as part of said configuring.**

Gorecki teaches that coefficients can be programmed by the user (Ex-1005, 7:1-4) and may be pre-programmed/pre-set in nonvolatile memories. Ex-1005, 7:18-31; *supra* §V.A.3[1f] (explaining memory teachings). It was obvious for the user to provide the coefficients by programming them into nonvolatile memory. When the controller configured transmit coefficients, it was obvious, as a matter of basic programming, for the controller to retrieve them from the memories where they were stored. Ex-1005, 7:13-31; Ex-1003, ¶96.

5. Claim 3

3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

“[T]ransmit coefficient values” lacks antecedent basis but, if not indefinite, refers to “the transmit filter coefficient values.” Ex-1003, ¶97.

The combination of Ground 2 was explained previously. *Supra* §V.A.; §V.A.3[1f] (Motivation subsection). Ground 2 teaches the first/second DRR devices (e.g., transceivers at respective ends of the cable) using transmit filter coefficient values to transmit signals. *Supra* §V.A.3[1f].

Lughart teaches that they are **programmed** to do so. Ex-1004, 11:58-60. For example, Lughart’s first/second DRR devices perform transmit pre-equalization using digital signal processors (“DSPs”). Ex-1004, Figs. 1A, 4A-4B (“TX DSP”), 7:67-8:7, 9:38-10:3, 30:39-47. DSP were programmable processors that ran software. *See* Ex-1004, 57:1-30. Therefore, the transceivers are programmed to perform Lughart’s teachings.

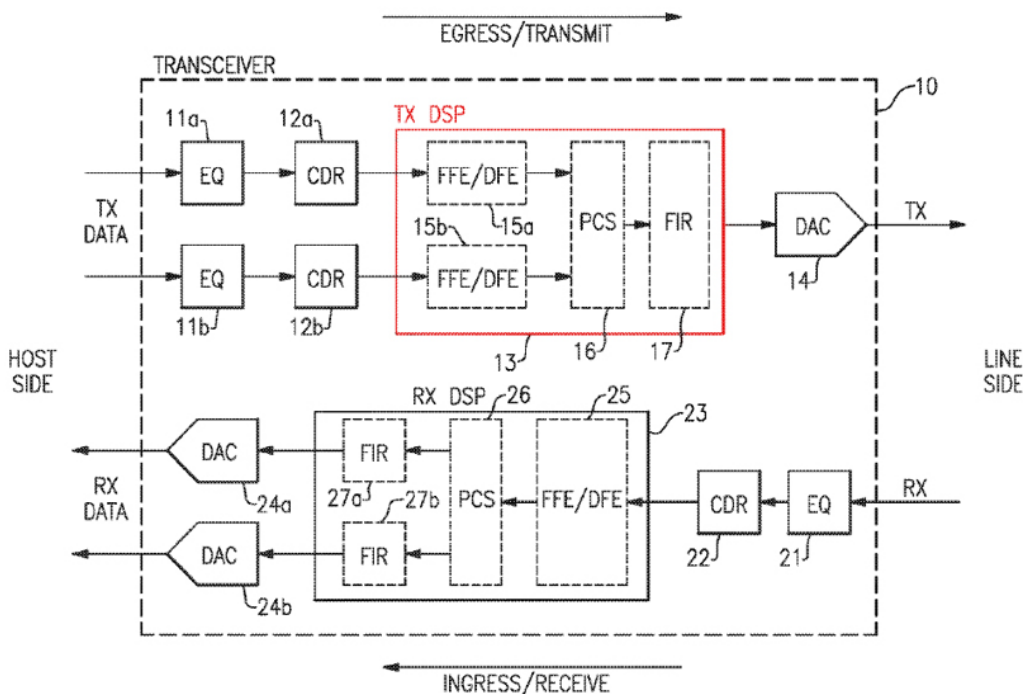


FIG. 1A

Ex-1003, ¶¶98-100.

Likewise, Gorecki teaches “programming” the transmit coefficient values used for equalization. Ex-1005, 7:1-4, 3:59-62; Ex-1003, ¶101.

The DRR devices are programmed to **use the transmit coefficient values each time power is supplied to the first and second end connector plugs.**

Gorecki teaches retrieving coefficient values from memory “during startup/power-up” and programming them in the equalization circuitry. Ex-1005, 7:18-33.

Lugthart teaches that each end of the active cable has a transceiver and an end connector plug. *Supra* §V.A.3[1a]-[1b]. Power is supplied to the first/second DRR devices via power lines connected to their perspective end connector plugs.

Ex-1004, 14:29-31, 17:26-29, 17:57-59. Therefore, Ground 2 teaches that the transceivers are programmed to use the transmit coefficient values each time power is supplied to the plugs. Ex-1003, ¶102.

6. Claim 4

4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

The combination of Ground 2 was explained previously. *Supra* §V.A; §V.A.3[1f] (Motivation subsection).

Gorecki teaches or suggests fine-tuning coefficients during operation (after assembly) and re-programming coefficients in the memories where they are stored, including EEPROM. Gorecki teaches that coefficient values may be “determined

or controlled in response to a[n] ... adaptive algorithm[.]” Ex-1005, 6:56-61. Tap coefficients can be adjusted “either before or during operation of the transmitter.” Ex-1005, 7:1-4. Coefficients may be “fine-tuned to enhance the system performance” which happens “after (or during) the performance of an initialization or re-initialization process[.]” Ex-1005, 7:50-59. Both options occur after assembly. Indeed, Gorecki teaches storing coefficients “semi-permanently” or “temporarily” until “re-programmed.” Ex-1005, 7:18-33. Thus, Gorecki teaches re-programming the coefficients with updated values. A POSITA would have been motivated to combine these teachings with Lugthart because Gorecki teaches one of a finite number of known, predictable solutions: determine/store the coefficients before cable assembly, rather than after. Gorecki’s adjustments/fine-tuning would not be possible before assembly. Updating the coefficients after assembly, based on actual cable measurements, because it allows them to be tailored to each cable, improving signal quality. This was beneficial for high-performance and extended cable-length applications in data centers, and it would have naturally fit into testing and quality assurance manufacturing stages. Therefore, it was obvious to re-program updated coefficients to reflect current cable characteristics, e.g., when the cable is first connected after assembly or periodically. Ex-1005, 7:50-59; Ex-1003, ¶¶103-104.

7. Claim 5

5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

The combination of Ground 2 was explained previously. *Supra* §V.A, §V.A.3[1f] (Motivation subsection).

Lugthart teaches that **the first and second DRR devices** (e.g., transceivers at respective ends of the cable) **employ receiver-based equalization of the electrical transit signals**. Each transceiver receiver path performs equalization (e.g., “EQ” and “FFE/DFE”) on the electrical transit signal received from the cable (“RX”). Ex-1004, Figs. 1A, 4A-4B, 8:5-25, 9:42-44, 22:40-23:21. The receiving path equalizer (e.g., “receive path equalizer 21”) is “used to provide signal equalization to compensate for transmission line losses on the line side[.]” Ex-1004, 9:10-15.

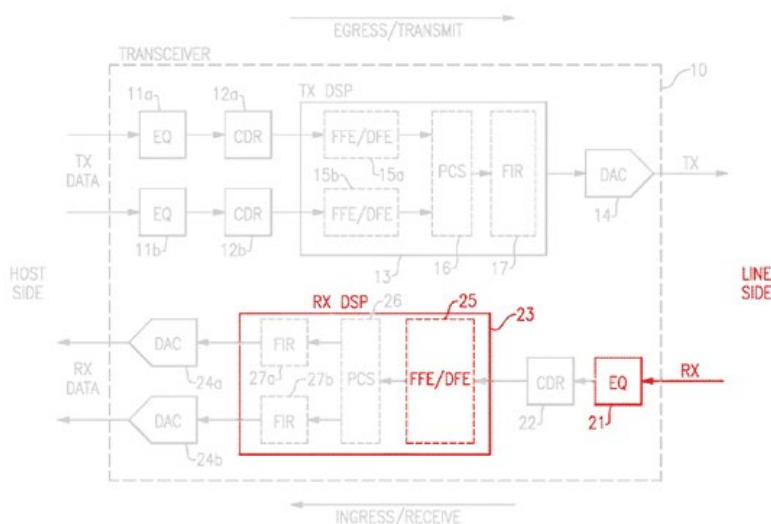


FIG.1A

Similarly, Gorecki teaches “a finite impulse response filter (‘FIR filter’), in the receiver to equalize the transmitted signals...” Ex-1005, 1:59-65; Ex-1003, ¶105.

Because Lugthart teaches symmetric transceivers at both cable ends (*supra* §V.A.3[1a]-[1b]), the first/second transceivers use receiver-based equalization in opposite directions. Ex-1004, 7:55-8:5, Figs. 2A, 4A; Ex-1003, ¶106.

The receiver-based equalization **uses coefficient values stored in the nonvolatile memories**. Lugthart teaches software implementations with program instructions and data (which would include coefficients) stored in nonvolatile memories. *Supra* §V.A.3[1f]; e.g., Ex-1004, 56:65-57:67, Figs. 1A, 4A-4B.

Gorecki teaches that the equalization circuitry comprising the FIR filter “typically includes a one or more taps having fixed or pre-programmed...coefficients.” Ex-1005, 1:65-67. Gorecki teaches storing equalization coefficient values in nonvolatile memories; this was simple and obvious. Ex-1005, 7:18-26; *supra* §V.A.3[1f] (explaining obviousness). Ex-1003, ¶107.

Motivation to Combine. A POSITA would have been motivated to combine Lugthart and Gorecki’s teachings for receiver-side equalization—by storing filter coefficient values in nonvolatile memory—for the same reasons that were explained for transmit-side pre-equalization. *Supra* §V.A.3[1f] (explaining combination and motivation). Lugthart provides express motivation to store DSP program instructions and data in EEPROM. E.g., Ex-1004, 57:40-55; *supra*

§V.A.3[1f]. This would have been the simplest implementation of Lugthart’s receiver-based equalization (Ex-1004, 9:10-15, 22:40-49), and it allows coefficients to be saved when the cable is disconnected and retrieved when powered on. Ex-1003, ¶108.

8. Claim 6

6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

Lugthart teaches that the cable includes “twinaxial cables (‘Twinax’), where each Twinax cable includes two inner conductors” (Ex-1004, 19:2-6) “implement[ing] differential signaling” to carry electrical transit signals in differential form across the cable (in both directions). Ex-1004, 19:2-6, 2:45-47, 3:12-16, 12:13-15, 16:27-30, Figs. 6A-6B. A POSITA would have been motivated to apply these teachings because it “provide[d] enhanced noise immunity via common-mode noise rejection.” Ex-1004, 16:37-49; Ex-1003, ¶109.

9. Claim 7

7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

Ground 2 teaches claim 7. The combination of Ground 2 was explained previously. *Supra* §V.A, §V.A.3[1f] (Motivation subsection). Lugthart and Gorecki teach the first/second DRR devices (e.g., transceivers at respective ends of

the cable) using FIR filters (*supra* §V.A.3[1f]) with leading, main cursor, and trailing taps. Ex-1005, 9:3-21. Gorecki teaches that leading/trailing taps can be “changed” (Ex-1005, 9:24-25), including where “leading and/or trailing taps may be ‘turned off’ or disabled” (Ex-1005, 18:15-18), leaving only the main cursor tap, which is mathematically equivalent to performing no pre-equalization because only the current sample tap is enabled. Ex-1003, ¶¶110-111.

A POSITA would have been motivated to apply Gorecki’s teaching to Lugthart by disabling equalization of the multi-lane data streams provided to the host interface ports. Those paths were far shorter than the cable; for designs with requirements of shorter lengths and low-loss connectors (thus reduced loss), it was obvious to turn off pre-emphasis because it is not needed, and to reduce power. A POSITA would have had a reasonable expectation of success because it merely involves turning off the FIR filter (passing the signal through as-is) by disabling taps, which simply changed values/settings. Ex-1003, ¶¶112-113.

Ground 3: Samaan further teaches claim 7.

If PO disputes Gorecki’s teachings, Samaan teaches modifying coefficient values to disable pre-equalization. First, Samaan teaches pre-equalization using an FIR filter. Ex-1007, ¶¶78-82, ¶¶139-142, Figs. 21-22, 34-35. Samaan explains how FIR filters have coefficients C_{-1} (analogous to leading taps) and C_{+1} (trailing taps). Ex-1007, ¶¶78-82. Both coefficients can “range from 0 to 0.25.” Ex-1007,

¶¶78-82, Figs. 21-22. When both are 0, the only remaining tap is the main cursor, which as explained above is mathematically equivalent to turning pre-emphasis off. *Id.* Ground 3 therefore teaches the first/second DRR devices not performing pre-equalization.

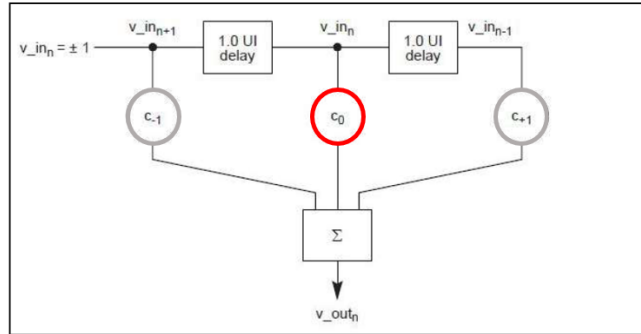


Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).

Ex-1003, ¶¶114-115.

Motivation to Combine. A POSITA would have been motivated to apply Samaan’s teachings by adjusting coefficients already present in the active cable of Lugthart and Gorecki; doing so enables the active cable to achieve a desired amount of equalization. Ex-1005, 9:37-40. Setting leading/trailing taps to 0 disables pre-equalization when it is not needed, e.g., designs with shorter host-side traces and low-loss connectors, as explained above for Ground 2. Ex-1003, ¶116.

A POSITA would have had a reasonable expectation of success because Gorecki already teaches disabling leading/trailing taps (explained above). Gorecki further teaches fine-tuning the amount of equalization (Ex-1005, 7:50-53, 9:37-40) by changing leading/trailing tap coefficients (Ex-1005, 9:16-26). Samaan teaches

doing just that. Ex-1007, ¶¶78-82, ¶¶139-142, Figs. 21-22. This combined prior art elements according to known methods (e.g., altering leading/trailing coefficients), to achieve a predictable result (e.g., disabling the FIR filter). Ex-1003, ¶¶117-118.

10. Claim 8

[8pre] A cable manufacturing method that comprises:

Grounds 1-2 teach the cable of claim 1 (*supra* §V.A.3) and a method of manufacturing a cable by connecting the cable's components together, including limitations below. Ex-1004, Figs. 2A, 4A, 6:65-67, 7:66-8:7; Ex-1003, ¶120.

[8a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;

Limitation [8a] mostly mirrors [1a]; Grounds 1-2 teach the overlapping limitations for the same reasons. *Supra* §V.A.3[1a]; Ex-1003, ¶121.

Lugthart further teaches **connecting a first connector plug** to the first DRR device (e.g., transceiver). Lugthart's cable assembly has "a first pair of conductors including a first pluggable module"; "the first pluggable module can include a first transceiver[.]" Ex-1004, 4:10-14, 15:30-31. Each transceiver assembly "has an input port" which includes a connector, and that the input port "is configured to mechanically and electrically connect... to a corresponding port or other interface"

on the host. Ex-1004, 15:42-47, 14:14-15. Lugthart illustrates a first connector plug connected to the first transceiver. Ex-1004, Figs. 1A, 2A, 4A-4B.

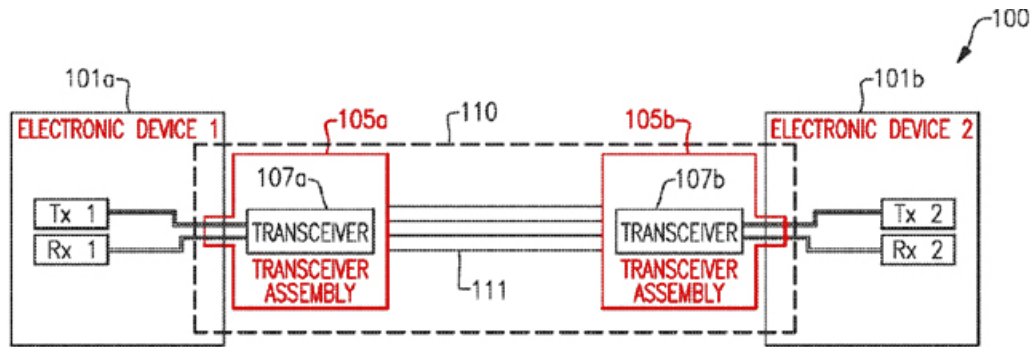


FIG. 2A

Ex-1003, ¶122.

Therefore, Lugthart teaches or suggests the step of connecting these components together. Ex-1004, Figs. 1A, 2A, 4A-4B, 4:11-17, 15:47-52. For these components to be connected in an assembled cable, they would have obviously been connected during manufacturing, when the components were assembled. Ex-1004, Figs. 2A, 4A. Ex-1003, ¶123.

[8b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;

Limitation [8b] mirrors [8a], differing only by changing “first” to “second.” Lugthart teaches a cable with two symmetric DRR devices. *Supra* §V.A.3[1b] (explaining symmetry). Either transceiver would be the first DRR device; the other would be the second. The second transceiver’s corresponding interface port and plug would be the second host interface port and end connector plug.

Therefore, [8b] is satisfied for the same reasons as [8a]. *Supra* §V.B.10[8a]; Ex-1003, ¶¶124-125.

[8c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,

Limitation [8c] mostly mirrors [1c]; Grounds 1-2 teach the overlapping limitations for the same reasons. *Supra* §V.A.3[1c]. Ex-1003, ¶126.

Lugthart further teaches **connecting** electrical conductors to the first/second DRR devices (e.g., transceivers at respective ends of the cable). Lugthart teaches that they are connected (*supra* §V.A.3[1c]) and therefore teaches or suggests the step of connecting these components together. Ex-1004, Figs. 1A, 2A, 3A-3B, 4A-4B, 4:11-17, 15:47-52, 17:35-39. For these components to be connected in an assembled cable, they would have obviously been connected during manufacturing, when the components were assembled. Ex-1004, Figs. 2A, 4A. Ex-1003, ¶127.

[8d]-[8f]

The limitations in [8d]-[8f] also appear in [1d]-[1f], respectively, and are satisfied for the same reasons. *Supra* §V.A.3[1d]-[1f]; Ex-1003, ¶128.

11. Claim 9

9. **The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring**

Claim 9 mostly overlaps with claim 2; Ground 2 teaches the overlapping limitations as explained above. *Supra* §V.A.4; Ex-1003, ¶129.

Ground 2 also teaches **providing** a first controller **device** by teaching a first controller, which is a device, as part of the active cable. *Supra* §V.A.4. It was obvious to provide a controller to perform the functions Ground 2 teaches. Ex-1003, ¶130.

Ground 2 teaches **internal** nonvolatile memory. Ground 2 teaches using nonvolatile memory, internal to the active cable, to store coefficient values. *Supra* §V.A.3[1f]; Ex-1005, 7:43-48 (“...the memory used to store...the coefficients of the tap(s)...may reside on the integrated circuit containing the transmitter, receiver or transceiver.”). Ex-1003, ¶131.

12. Claim 10

Claim 10 is identical to claim 3, other than verb tense and passive voice; it is satisfied for the same reasons. *Supra* §V.A.5; Ex-1003, ¶132.

13. Claim 11

11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.

The combination of Ground 2 was explained previously. *Supra* §V.A, §V.A.3[1f] (Motivation subsection). Ground 2 teaches the transmit filter coefficient values being determined and stored in the nonvolatile memories after cable assembly (*supra* §V.A.6), which includes connecting the electrical conductors (*supra* §V.A.10[8c], §V.A.3[1c]). Ex-1003, ¶133.

Ground 2 further **characterizes channel characteristics of the electrical conductors to determine the transmit filter coefficient values.** The purpose of Lugthart's pre-equalization is "to compensate for channel losses." Ex-1004, 23:59-24:2; Ex-1005, 3:8-16. Gorecki explains that the FIR coefficients are "pre-programmed or pre-set" to provide "the inverse of the effects caused by the communication channel." Ex-1005, 7:18-33, 9:3-15. Therefore, Ground 2 teaches determining the coefficients by characterizing channel characteristics, so that Lugthart's pre-equalization filter can compensate for those channel characteristics as taught. Ex-1004, 22:3-24:2; Ex-1005, 3:8-16; Ex-1003, ¶134.

14. Claims 12-14

The limitations of claims 12-14 are identical to claims 5-7 and are satisfied for the same reasons. *Supra* §V.A.7-9; Ex-1003, ¶135.

15. Claim 15

[15pre] A communications method that comprises:

Lugthart teaches **a communications method**. Lugthart teaches “methods for high speed communications” that “achieve reliable high-speed point-to-point communication” (Ex-1004, Abstract, 6:65-7:1) using the active cables explained for claim 1. *Supra* §V.A.3; Ex-1003, ¶137.

Likewise, Gorecki teaches “a technique of...enhancing...high-speed digital communications through a communications channel.” Ex-1005, Abstract, 1:12-17. Ex-1003, ¶138.

The communications method of Grounds 1-2 further includes the limitations discussed below. Ex-1003, ¶139.

[15a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and

Lugthart teaches **inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first**

DRR device (e.g., first transceiver). This is shown in Figure 2A, with Electronic Device 1 as the first host and an end connector plug inserted into its interface port; wiring connects the transceiver to the end connector plug. Ex-1004, 14:14-15, Figs. 1A-2A, 4A-4B (teaching connections from transceivers to end connector plugs).

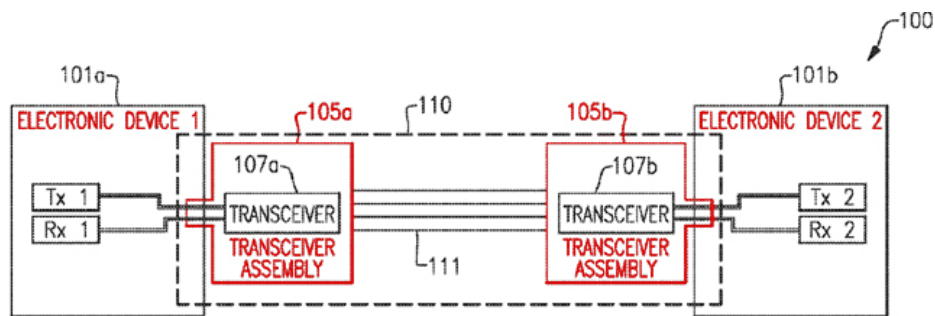


FIG. 2A

Ex-1003, ¶140.

Additionally, Lugthart teaches or suggests inserting the plug into the host interface port. Lugthart explains that “[e]ach of the transceiver assemblies...has an input port[,]” which includes a pluggable connector, and that the input port “is configured to mechanically and electrically connect...to a corresponding port or other interface on the respective electronic device...” Ex-1004, 15:42-52 (teaching releasable plug); Ex-1003, ¶141.

The rest of [15a] combines elements recited in [1a], [1c], and [1d] and are taught for the same reasons explained previously. *Supra* §V.A.3[1a], [1c]-[1d].

Ex-1003, ¶142.

[15b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,

Limitation [15b] mirrors [15a] and differs only by changing “first” to “second.” Lugthart teaches a cable with two identical transceivers, one at each end. *Supra* §V.A.3[1a], [1b] (explaining Lugthart’s symmetry). Either transceiver would be the first DRR device; the other would be the second. The second transceiver’s corresponding interface port and plug would be the second host interface port and end connector plug. Therefore, [15b] is satisfied for the same reasons explained for [15a]. *Supra* §V.A.15[15a]; Ex-1003, ¶143.

[15c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

Limitation [15c] is identical to [1f] and is satisfied for the same reasons. *Supra* §V.A.3[1f]; Ex-1003, ¶144.

16. Claim 16

16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.

The combination of Ground 2 was explained previously. *Supra* §V.A, §V.A.3[1f] (Motivation subsection).

Ground 2 teaches **supplying power to the first and second end connector plugs**. Lugthart teaches its “active cable including actively powered componentry,” e.g., “first and second transceiver assemblies” at each end. Ex-1004, 14:29-42. Lugthart teaches the power consumption of several form factors for active cables. Ex-1004, 54:45-55:45. Additionally, the obvious implementation was to supply power to both end connector plugs because Lugthart explains that they include “actively powered componentry” that requires power. Ex-1004, 14:29-42, 54:45-55:45. Without power, Lugthart’s cable would not operate as taught. Ex-1003, ¶145.

Ground 2 teaches **the first and second end connector plugs being connected to first and second controller devices, respectively**. Gorecki teaches the “controller” distributing the coefficient values to the transmitter. *Supra* §V.A.4, §V.A.3[1a]-[1b]. To do this, the controller would have been connected to

the DRR device and connector plug at its end of the cable, so it can configure the DRR device and also receive power. Ex-1005, 7:14-17; Ex-1003, ¶146.

Ground 2 teaches the rest of claim 16 with respect to a first controller and DRR device, explained above. *Supra* §V.A.4. Because Lugthart’s cable is symmetric, Ground 2 teaches the second controller and DRR device for the same reasons. *Supra* §V.A.3[1b] (explaining symmetry); Ex-1003, ¶147.

17. Claims 17-20

Claims 17-20 recite identical limitations to claims 3-5 and 7, respectively, and are satisfied for the same reasons. *Supra* §V.A.5-7, 9; Ex-1003, ¶148.

B. Ground 4

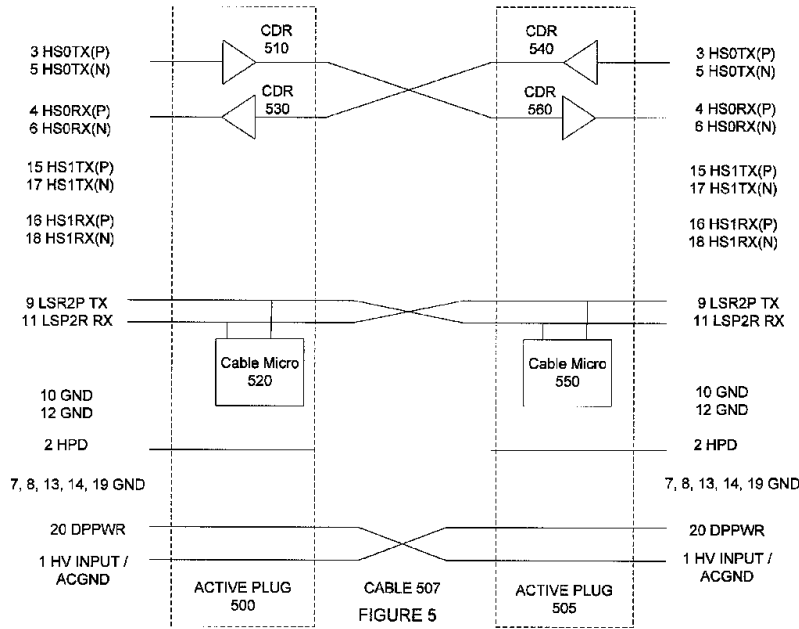
Cornelius is Apple prior art that teaches an active cable with CDR circuitry that “retime[s] data” and performs equalization. Ex-1006, 6:6-32. Samaan, an Intel paper, teaches retimer details, e.g., for performing CDR and equalization. Gorecki stores equalizer coefficients in nonvolatile memories and, for dependent claims, teaches a controller that reads and configures the coefficients, including at power-up. Ex-1003, ¶149.

1. U.S. Patent 8,516,238 (“Cornelius”) (“Ex-1006”)

Cornelius is post-AIA §102(a) prior art; it was filed June 2011 and issued August 2013, claiming priority to February 2011. Ex-1003, ¶150.

Cornelius teaches “an active cable” with CDR circuits that “retime data at each of its ends[.]” Ex-1006, 6:6-29. Cornelius’s CDR circuits perform more than

typical clock/data recovery; they also “employ equalizer circuits, buffers, emphasis, and de-emphasis circuits” to improve reliability and accuracy. Ex-1006, 6:30-32, 11:45-48.



Ex-1003, ¶¶151-152

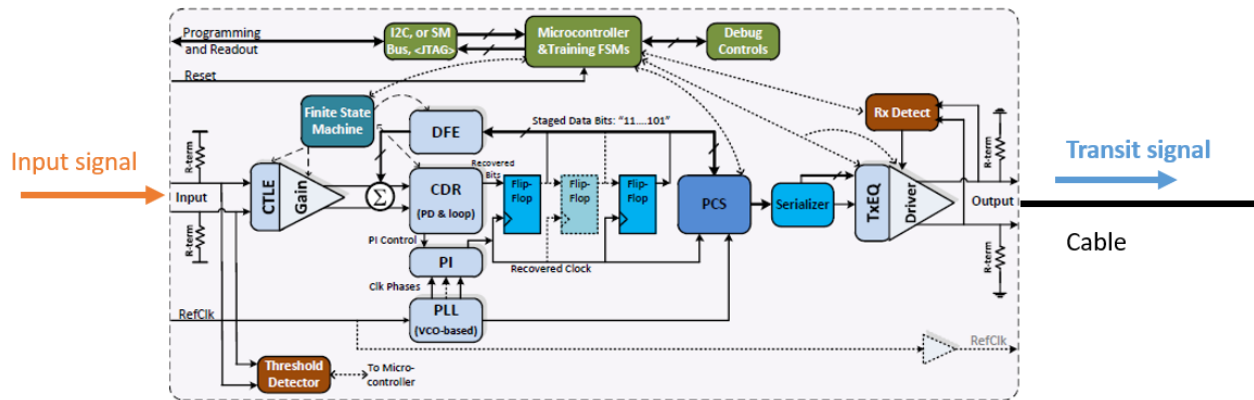
Cornelius is analogous art because it is in the same field (high-speed communications). *Supra* §III. Cornelius teaches an active cable that provides a “high-speed connection.” Ex-1006, 3:27-64, 4:22-54, 8:57-9:6. Each active plug provides and receives “high-speed signals.” Ex-1006, 6:11-24, Fig. 5. Cornelius is reasonably pertinent to the problem addressed by the ’233 patent because Cornelius teaches pre-equalization/equalization for high-speed serial communications. Ex-1006, 6:30-42, 6:6-20, 11:45-62; *supra* §V.A.2 (explaining problem); Ex-1003, ¶153.

2. High-Speed Serial Bus Repeater Primer, Intel Corp., Revision 1.2 (“Samaan”) (“Ex-1007”)

Samaan is post-AIA §102(a) prior art.

Prior Art Publication. Samaan is an Intel whitepaper published in 2015 (Ex-1007, ¶1) and freely available for download on Intel’s public website (www.intel.com) by at least February 2, 2016. Ex-1018, ¶7. Intel published whitepapers that were sought out by interested members of the public, including researchers at Texas Instruments that in fact accessed and cited Samaan in their own work. Ex-1018, ¶18, ¶¶11-17. A POSITA could easily find white papers on Intel’s website with a few clicks and a search. For example, searching for Samaan’s title “High-Speed Serial Bus Repeater Primer” returns a single result “PCIe Architecture” (Ex-1035, 000001) that directly links to Samaan under “White Papers” (Ex-1033). Related search terms likewise return the PCIe Architecture page, with an accessible link to Samaan. Ex-1035, 000003, 000007-000080, 000011, 000015. Snapshots from the Internet Archive confirm the PCIe Architecture webpage was available and provided access to Samaan before 2018. Ex-1018, 000105-000106, 000029-000030. This same page is cited in the PCIe Wikipedia entry. Ex-1034, 000028; Ex-1018, 000105-000106, 000029-000030. Notably, Cornelius also cites this Wikipedia page, and a POSITA, like Cornelius’s inventors, would have followed such links for further information. Ex-1006, 000002 (“Other Publications”); Ex-1003, ¶¶155-158.

Overview. Samaan teaches re-timer architectures for high-speed copper channels. Ex-1007, ¶¶2-6. Samaan details how re-timers utilize equalization and CDR to extract bits from an input signal and then perform pre-equalization and modulation to transmit the signal on the other end. Ex-1007, Fig. 35:



Ex-1003, ¶159.

Samaan is analogous art because it is in the same field (high-speed communications). *Supra* §III. This is stated in Samaan’s title. Samaan teaches re-timers for high-speed serial environments. Ex-1007, ¶1, ¶¶5-8, ¶¶12-15. Samaan is reasonably pertinent to the problem addressed by the ’233 patent (§V.A.2) because Samaan likewise addresses channel loss at high frequencies (Ex-1007, ¶¶2-4) with pre-equalization/equalization for high-speed serial communications. Ex-1007, ¶1, ¶¶5-8, ¶¶207-220, Figs. 34-35; Ex-1003, ¶160.

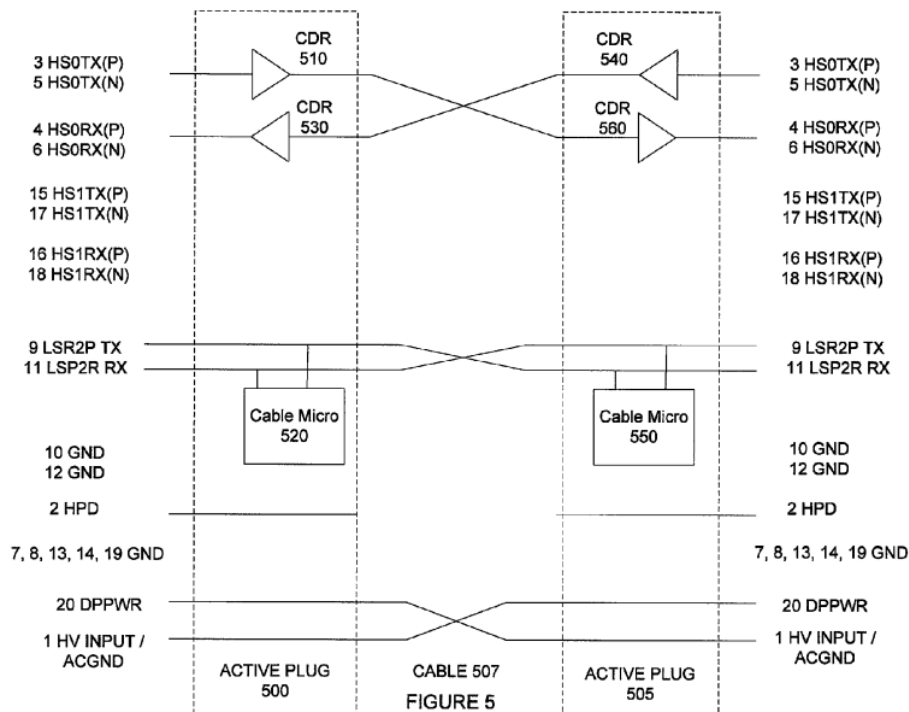
3. Claim 1

For each of the below limitations, the “first” and “second” designations can be swapped between elements at one end of the active cable. Cornelius’ cable

design is symmetric; each side has identical components and operation. E.g., Ex-1006, 6:14-23, 8:20-40, Figs. 5-6. Ex-1003, ¶161.

[1pre] A cable that comprises:

Cornelius teaches an active cable. Ex-1006, Title, 5:33-39, 6:6-20, 8:20-40, Figs. 5-6, Claims 1-10.



The cable includes the elements discussed below for [1a]-[1f]. Ex-1003, ¶163.

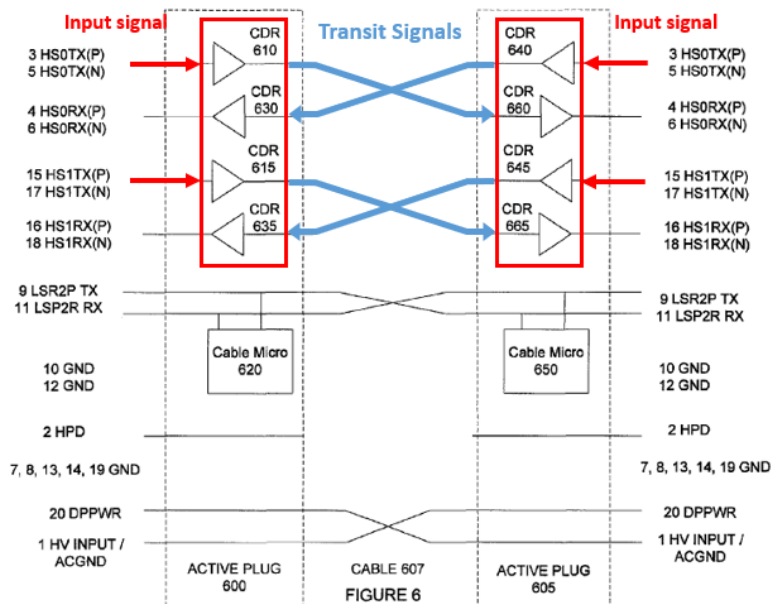
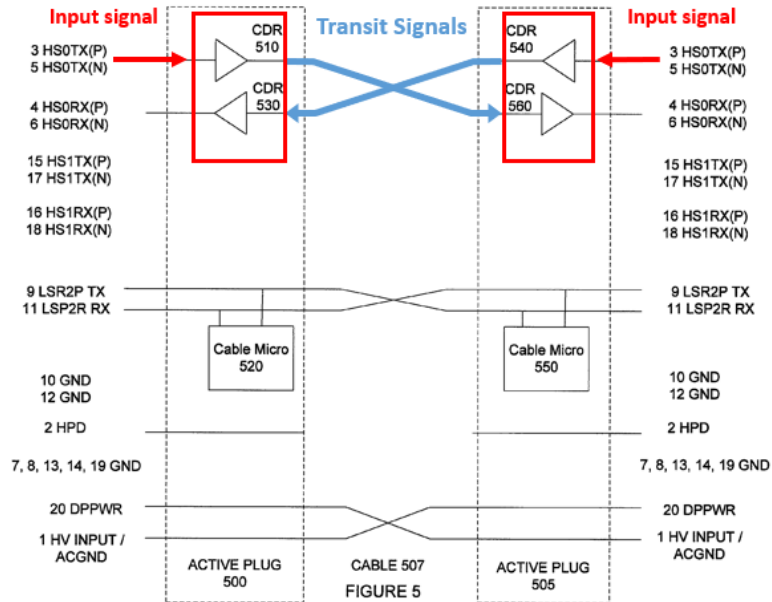
[1a] a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;

Cornelius's cable includes active plugs. Each plug contains multiple CDR circuits that perform additional functions beyond clock/data recovery; the CDR

circuits also retime data and “employ equalizer circuits, buffers, emphasis, and de-emphasis circuits[.]” Ex-1006, 6:15-33; Ex-1003, ¶164.

Ground 4 teaches a **first DRR device**. Cornelius teaches CDR/retimer circuitry that recovers clock and data from incoming signals and “retime[s]⁵ signals received at an input.” Ex-1006, 6:6-24, Claims 1&6, 8:20-26, Figs. 5-6. It also re-modulates the input data stream for transmission across the cable. Thus, the collective CDR/retimer circuitry in Cornelius’s active plug comprise a DRR device:

⁵ Patent Owner has taken the position that [1a] is satisfied by retimers in an active cable. Ex-1024, 000003-000005 (highlighting “retiming” as evidence of remodulation and data extraction); Ex-1022, 000002-000008 (highlighting retimers); Ex-1023, 000003-000010 (same).

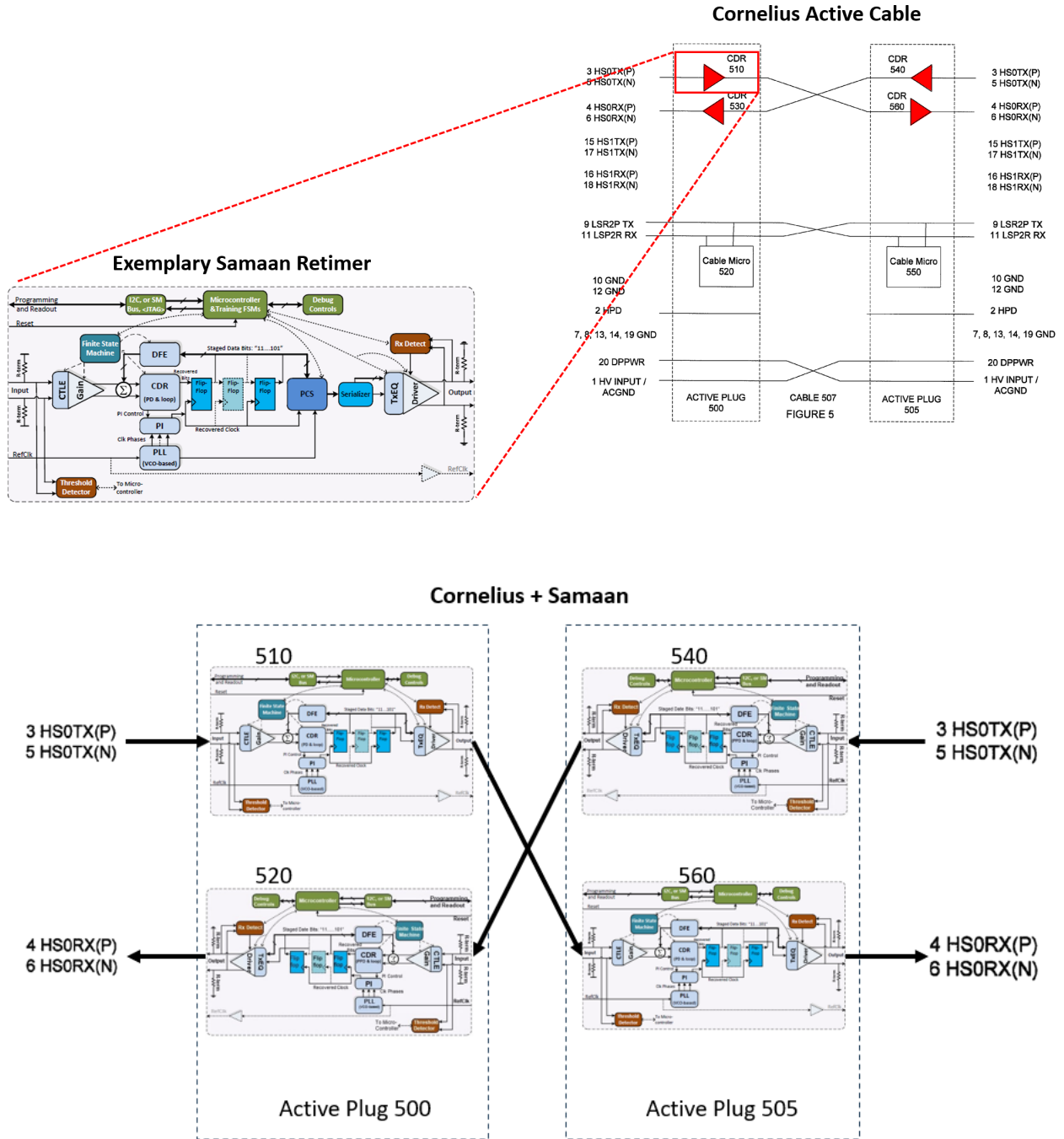


Ex-1003, ¶165.

Samman provides additional retimer details, including two retimer flavors: protocol-aware or unaware retimers. Both flavors include the same functionalities Cornelius describes in its active plug and CDR. Ex-1006, 6:6-32; Ex-1007, ¶225,

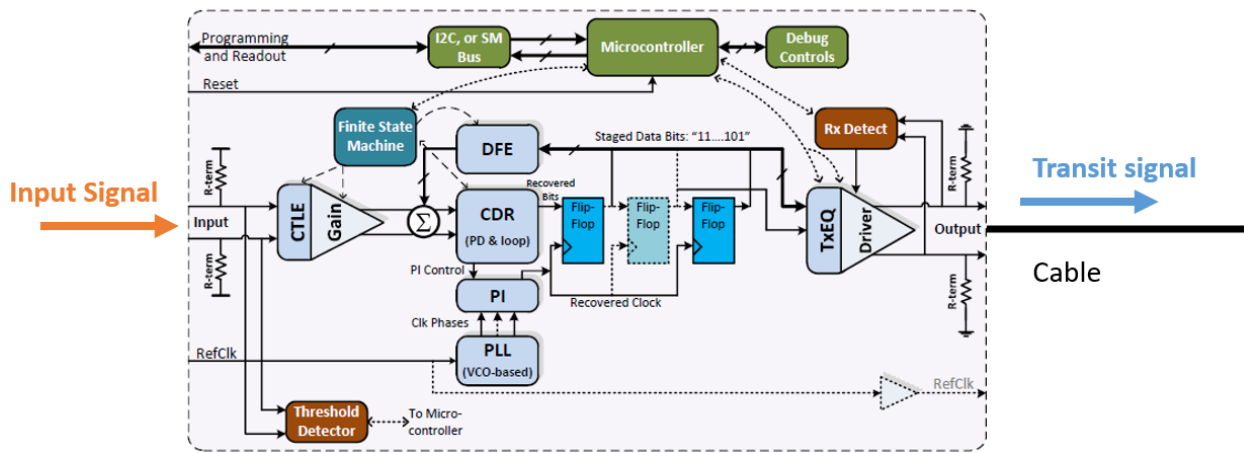
¶79, ¶91, Figs. 34-35. A POSITA would have applied Samaan's retimer teachings (either protocol-aware or unaware) to Cornelius's active plugs as illustrated below.

Ex-1006, Fig. 5; Ex-1007, Figs. 34-35.

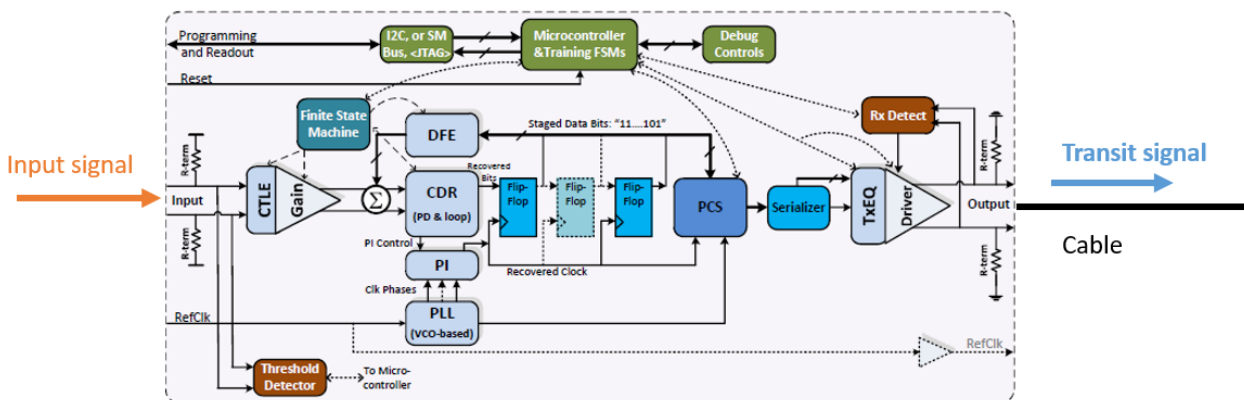


Ex-1003, ¶166.

Each Samaan retimer performs CDR to recover digital “data bits” (stored in flip-flops) from its input data stream. Ex-1007, ¶¶202 ¶¶203-212, ¶¶216-217, Figs. 34-35. Next, the retimer re-modulates the digital bitstream and “re-transmits the digital data anew.” Ex-1007, ¶¶202. For this re-modulation process in a protocol-unaware retimer, the data signal flows through TxEQ for output equalization and then the driver. Ex-1007, ¶¶216-231, Fig. 34:



For the re-modulation process in protocol-aware retimers, the data signal flows through the physical coding/decoding sublayer (PCS), serializer, TxEQ, and driver. Ex-1007, ¶¶218-231, Fig. 35:



Ex-1003, ¶167.

Like Cornelius’s CDR/retimer circuitry, both of Samaan’s retimer architectures re-modulate the inbound data stream by converting the extracted data bits into a signal for cable transmission, with jitter and timing characteristics independent of the input signal. Ex-1007, ¶15, ¶202; Ex-1003, ¶168.

Ground 4 teaches a first DRR device (e.g., CDR/retimer circuitry) **that exchanges inbound and outbound multi-lane data streams**. The host transmits outbound data signals to the active cable via TX pins (3, 5, 15, 17) and receives inbound data signals from the active cable through RX pins (4, 6, 16, 18). Ex-1006, Fig. 3, 4:23-54, 3:33-4:9. Cornelius describes transmit (Tx) and receive (Rx) from the host’s perspective. Ex-1006, Figs. 3, 5, 6:16-24. The DRR device exchanges Tx and Rx signals from/to the host device through an end connector plug. Ex-1006, 6:16-24, Ex-1006, 4:22-38, Figs. 2-3, 5-6.

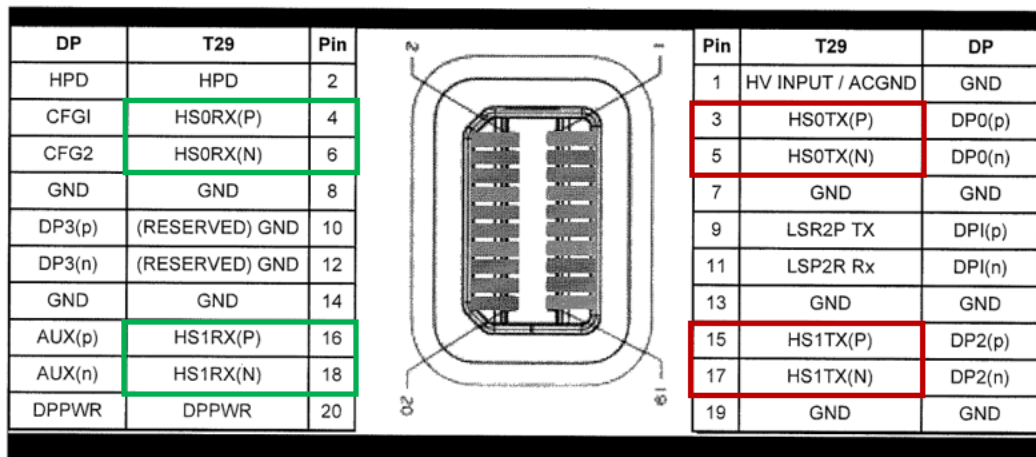
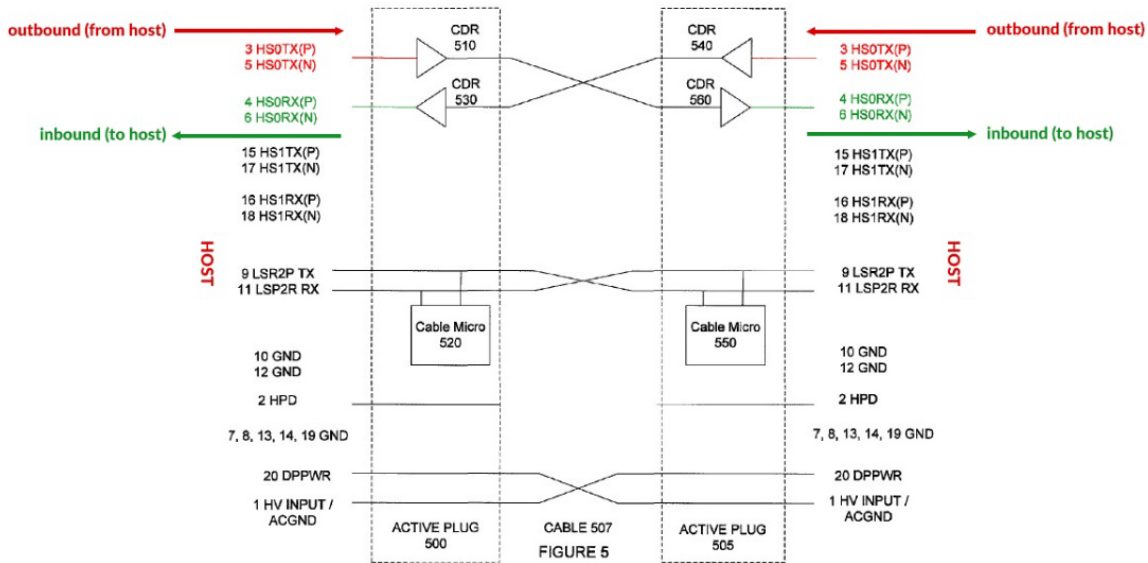
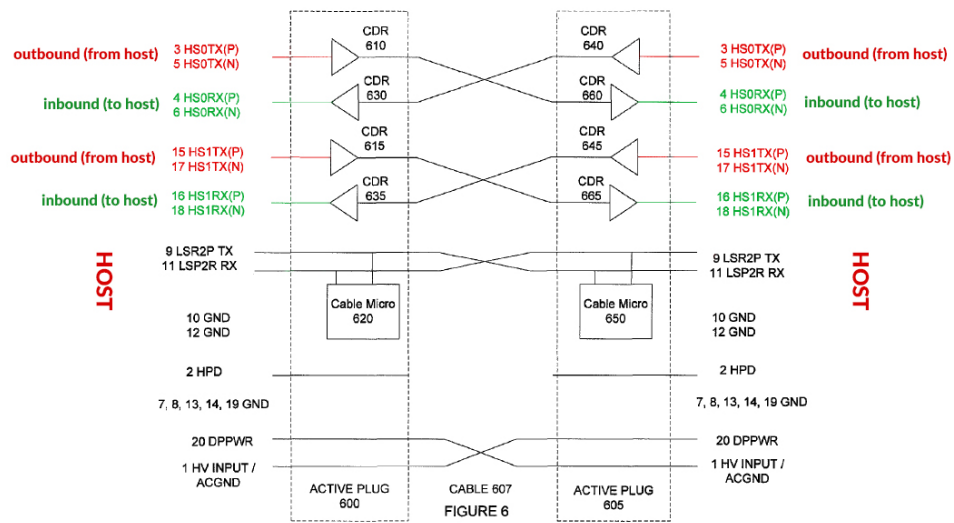


FIGURE 3

Based on Cornelius’s figures and specification, data flows following the direction of the triangle arrows, which is the normal convention in the field. Ex-1006, 6:11-20, 8:20-26; Ex-1003, ¶¶169-170.



As shown in Figure 6, each DRR device exchanges more than one lane of inbound and outbound data streams—using pins 4, 6, 16 and 18 for inbound data to the host, and pins 3, 5, 15 and 17 for outbound data from the host. The signals on these pins carry data streams, with each CDR/retimer circuitry recovering data as a stream of bits from the host and also sending a stream of data bits in the opposite direction. Ex-1006, Figs. 5-6; Ex-1007, ¶202, Figs. 34-35 (flip-flops storing recovered bits).



Ex-1003, ¶171.

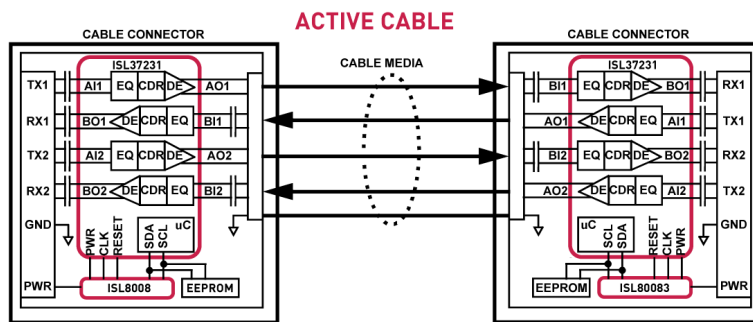
The inbound/outbound data streams are exchanged **with a first host interface port via a first end connector plug**. Cornelius teaches “two active plugs...one on each end of cable.” Ex-1006, 6:11-20, 8:20-26, Fig. 6. Each comprises an end portion that is an end connector plug used to connect one end of the active cable to corresponding host devices, such as computers or other devices. Ex-1006, 8:27-40 (“...host device connected to plug 600...”), 3:28-64, Figs. 2-3, 6:6-10, 5:33-39. The host interface port would be the mating interface where the end connector plug is inserted. Cornelius teaches or suggests this by providing a connector pinout for the active plug to exchange inbound/outbound streams with a host. Ex-1006, 4:22-38, Fig. 3. Without such an interface port, the active cables would not operate as described by Cornelius. Ex-1003, ¶¶172-174.

Motivation to Combine. In 2011, Apple and Intel co-developed active cable technologies later known as Thunderbolt. Ex-1013, 000001. Their collaboration drew significant attention, with Apple developing and marketing the cable (Ex-1014, 000001; Ex-1013, 000001-000002), and Intel providing port and retimer architecture for the active plugs. Ex-1016, 000001-000002; Ex-1015, 000003. Thunderbolt ports appeared in Mac computers beginning in 2011 (Ex-1013, 000001), and other vendors soon offered Thunderbolt solutions. Ex-1009, 000001; Ex-1008, 000003-000005. Thunderbolt cables were commercially available by 2011. Ex-1016, 000001; Ex-1003, ¶175.

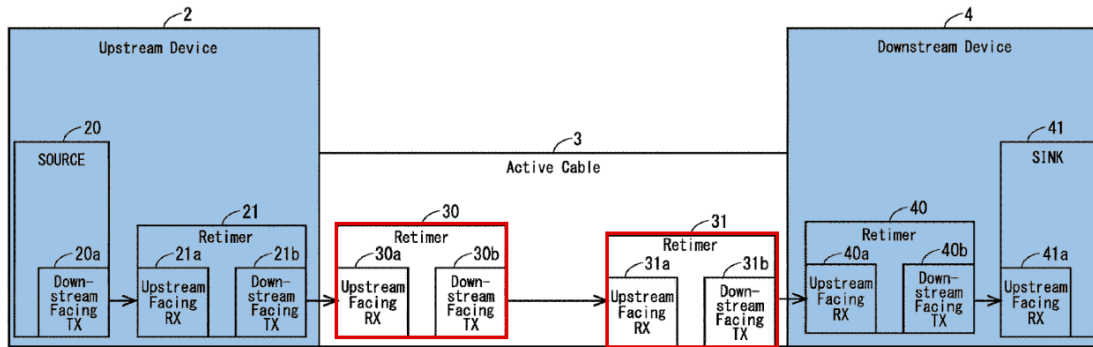
Therefore, by 2019, a POSITA developing active cables would have been motivated to consult Apple’s cable art (e.g., Cornelius) and Intel’s technical references on transceiver/retimer architecture (e.g., Samaan)—specifically, to apply Samaan’s retimer teachings when implementing the “circuits for retiming data” in Cornelius’s active plugs. Ex-1006, 6:11-32, 8:20-26, Figs. 5-6. Because Cornelius does not provide implementation details—understandable given Apple’s focus on the broader Thunderbolt assembly—a POSITA would have looked to known retimer architectures (Ex-1006, 12:21-34 (providing motivation to modify)) like Samaan. This combined prior art elements according to known methods to yield predictable results (e.g., a retimer in an active cable, as Cornelius teaches). Ex-1003, ¶¶176-177.

Samaan’s retimer teachings provide several benefits, e.g., jitter isolation, enhanced debug capabilities, and increased length. Ex-1007, ¶15, ¶202. Samaan applies its teachings to cables, explaining how re-timers are “usable in a reversible cable” (Ex-1007, ¶238) and with known cable/module standards, e.g., SFP+ (Ex-1007, 000072, ¶204, ¶72). See Ex-1011 (using SFP+ for Ethernet); Ex-1025, Tbl. 1; Ex-1012, 000001-000009 (same); Ex-1019 (same). The combination applies known retimer architectures to known active cables that were ready for improvement to yield predictable results: a retimer in an active cable. Ex-1003, ¶¶178-179.

The prior art provided express motivation to incorporate retimers in active cables and recognized numerous benefits. Ex-1026; Ex-1009, 000001 (explaining retimer benefits), Fig. 1:



Ex-1010, ¶2, Fig. 1:



Ex-1003, ¶180.

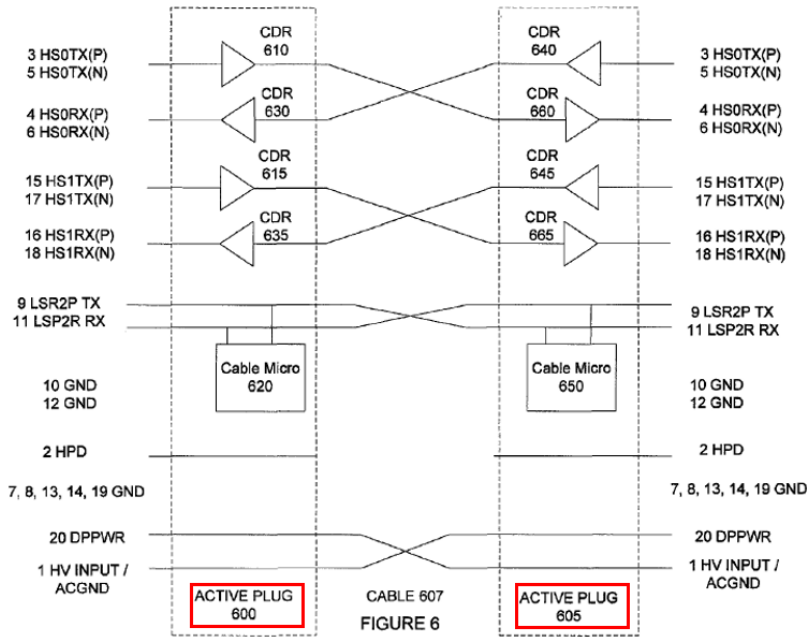
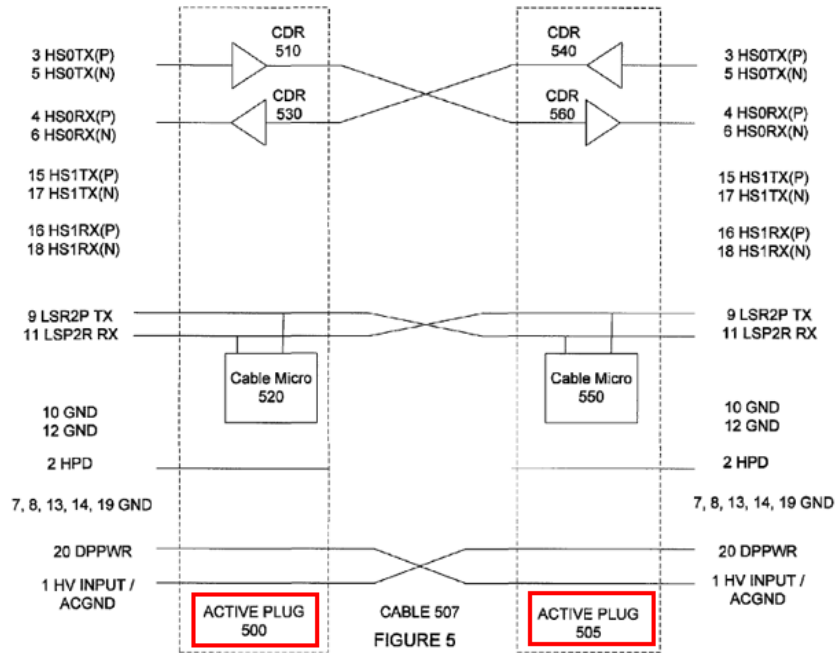
The combination would not alter the principle of operation for either reference. Cornelius already teaches retimers in its active cable for various protocols, employing CDR, equalization, and pre-equalization (Ex-1006, 000002, 6:6-32), which Samaan likewise teaches for its retimers. Ex-1007, ¶¶202-231, ¶15, Figs. 34-35. Samaan already teaches cables and provides a broadly applicable retimer architecture. In an active cable, Samaan’s retimer would function the same way and for the same purpose: to recover bits from one end and re-transmit them on the other. Ex-1003, ¶181.

In addition to the above-explained reasons, a POSITA would have had a reasonable expectation of success because retimers and active electric cables were well established in the art. Samaan’s retimers exemplify common techniques used in high-speed serial communications and taught in universities for many years. Active cables were commercially available and deployed in data centers.

Therefore, a POSITA with the requisite level of education/experience (*supra* §III) would have understood how to use retimers with cables. Ex-1003, ¶182.

<p>[1b] second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug</p>
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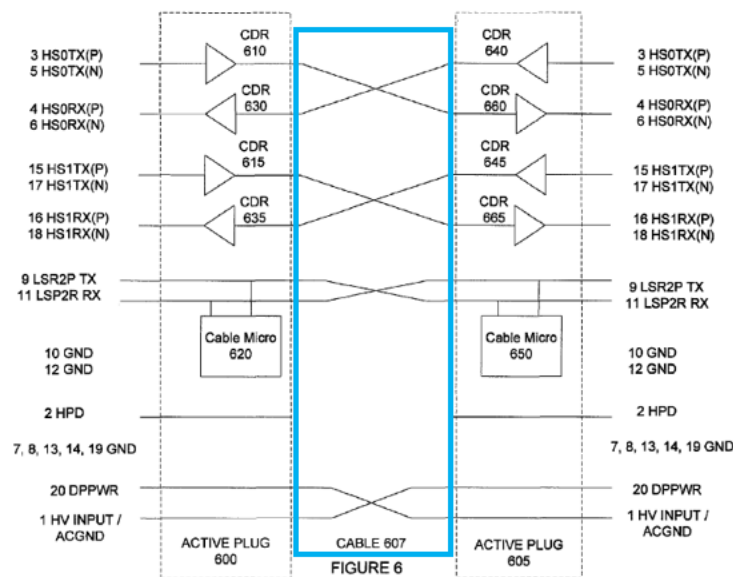
Limitation [1b] mirrors [1a] but changes “first” to “second.” Ex-1003, ¶183. The analysis from [1a] (*supra* §V.B.3[1a]) also applies to [1b] because Ground 4 teaches a bidirectional cable with two symmetric DRR devices: the CDR/retimer circuitry located in the active plug at each end of the cable. Ex-1006, 6:11-20, 8:20-40, Figs. 5-6; *supra* §V.B.3[1a] (explaining DRR devices). The relevant teachings apply to both. *Id.* Therefore, either would be the first DRR device; the other would be the second. The corresponding interface port and plug would be the second host interface port and end connector plug.



Ex-1003, ¶¶184-186.

[1c] electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,

Ground 4 teaches **electrical conductors** (e.g., in a cable) **connecting the first and second DRR devices** (e.g., CDR/retimer circuitry in each active plug) **to convey electrical transit signals therebetween**. For example, Cornelius teaches an “active cable” that “includes two active plugs...one on each end of cable.” Ex-1006, 6:11-20, 8:20-26, Fig. 6. Each plug has a DRR device. *Supra* §V.B.3[1a]-[1b]. Pairs of electrical conductors in the cable connect one DRR device (e.g., CDR/retimer circuitry in plug 500/600) to the other (e.g., CDR/retimer circuitry in active plug 505/605, or vice versa), Figs. 5-6:

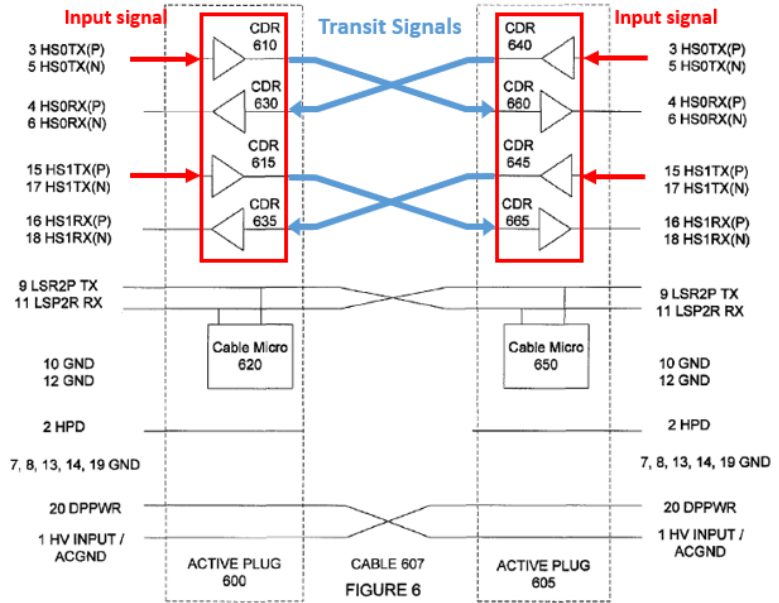
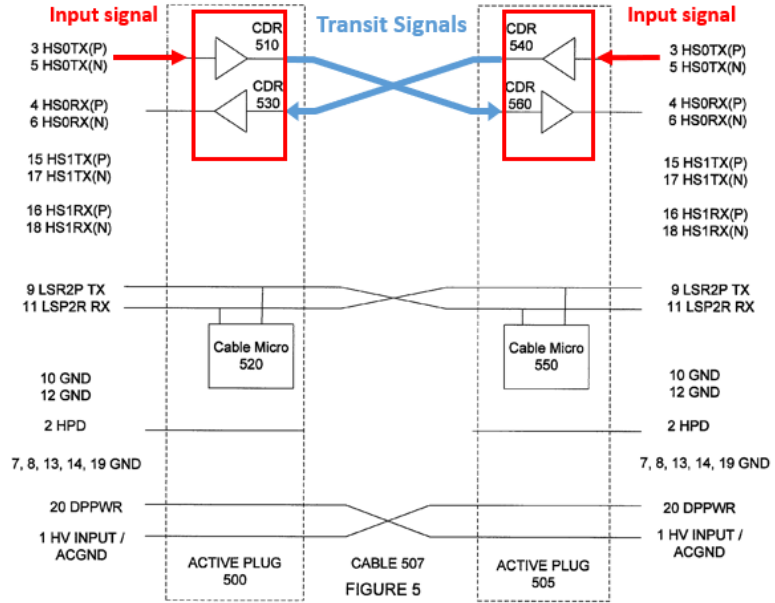


Ex-1003, ¶187.

The cable comprises “copper or other conductor.” Ex-1006, 7:26-41. A POSITA would have been motivated to apply these teachings, rather than other

embodiments for fiber optics, for reduced costs and improved bend radius. Apple provided motivation by moving Thunderbolt cables from initially-envisioned fiber optics (Ex-1013, 000001-000002) to “construct the cable out of copper instead[.]” Ex-1014, 000002; Ex-1013, 000001; Ex-1003, ¶188.

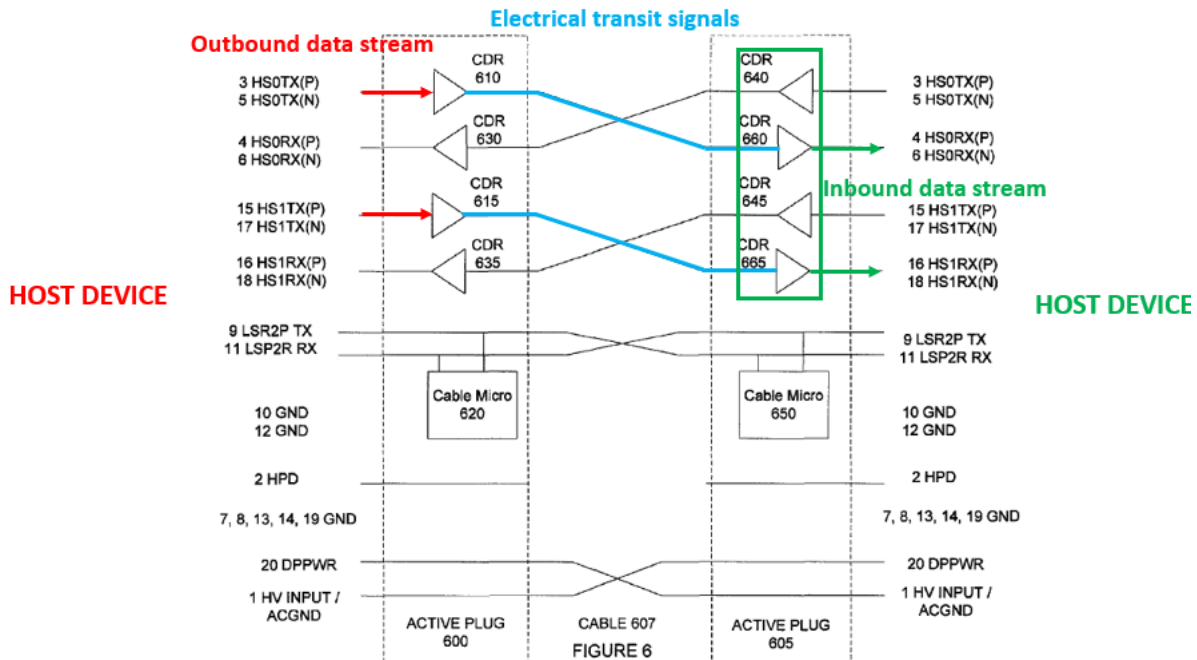
The electrical conductors in the cable convey electrical transit signals between the CDR/retimer circuitry in each plug. Ex-1006, 7:26-41; Figs. 5-6.



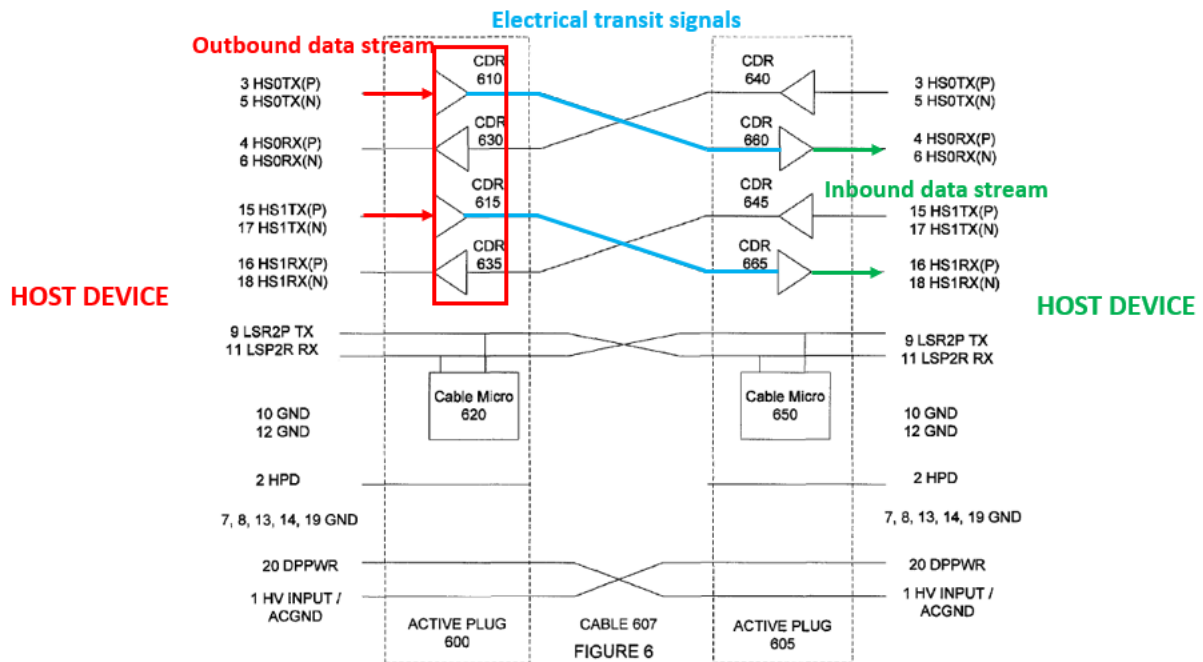
Ex-1003, ¶¶189-190.

[1d] first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and

Ground 4 teaches the first DRR device (e.g., CDR/retimer circuitry) converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port. After the electrical transit signal traverses the cable and enters the DRR device on the other end, Cornelius performs clock/data recovery to extract data bits from the transit signals. The CDR/retimer circuitry “retime[s] signals received from the cable” (the transit signals), and transmits the converted signals to the host interface port as the inbound data stream (inbound from the host’s perspective). Ex-1006, Claim 1, 6:11-24, 8:20-26, 3:28-64, 6:6-10, 5:33-39, Figs. 2, 5-6.



In the other direction, Cornelius performs clock/data recovery to extract data bits from data stream outbound from the host interface port; the CDR/retimer circuitry retimes those signals and transmits the converted signals over the cable as the electrical transit signals. Ex-1006, 6:11-24, Figs. 5-6.



Ex-1003, ¶191.

Cornelius teaches multiple lanes for inbound/outbound data streams for the host interface port. Ex-1006, 6:11-24, 8:20-26, Figs. 5-6; *supra* §V.B.3[1a] (explaining lanes and host interface ports); Ex-1003, ¶¶192-193.

[1e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,

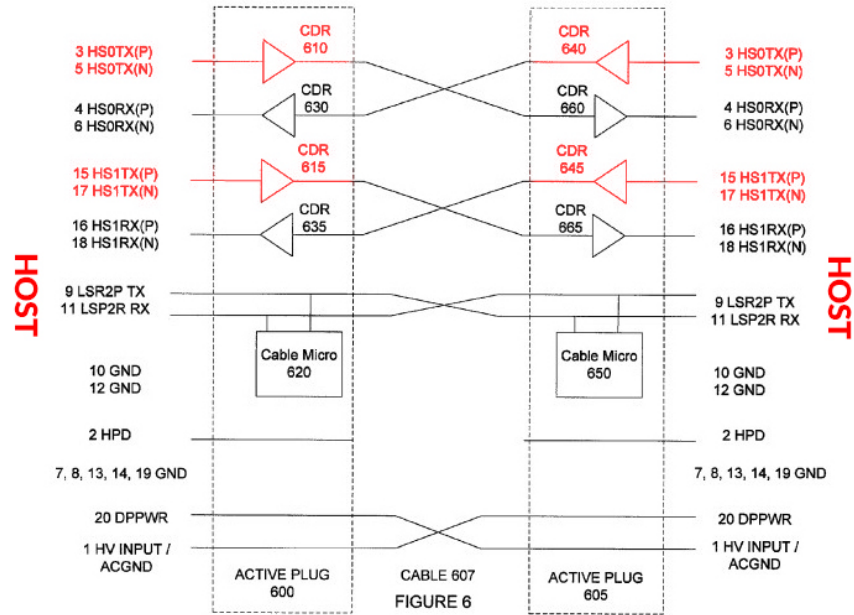
Limitation [1e] mirrors [1d] but changes “first” to “second.” The analysis for [1d] (*supra* §V.B.3[1d]) applies here because Ground 4 teaches a cable with

symmetric CDR/retimer circuitry at each end. *Supra* §V.B.3[1b] (explaining symmetry). Either CDR/retimer circuitry would be the first DRR device; the other would be the second, with corresponding second host interface port, for reasons explained previously. Ex-1003, ¶¶194-195.

[1f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

Ground 4 teaches **the first and second DRR devices** (e.g., CDR/retimer circuitry at respective ends of the cable) **providing pre-equalization of the electrical transit signals**. The first/second DRR devices were explained above. *Supra* §V.B.3[1a]-[1b]. The CDR/retimer circuitry in one active plug is the first DRR device; the other is the second. Ex-1003, ¶196.

Cornelius employs “emphasis, and de-emphasis” in its CDR/retimer circuitry, including in the transmitting path, to perform pre-equalization by shaping the signal before transmission to account for anticipated channel losses. Ex-1006, 6:11-42, 8:20-40, Figs. 5-6, Claims 5&10. Emphasis and de-emphasis were common ways to implement pre-equalization. *Supra* §V.A.3[1f] (explaining emphasis/de-emphasis). Therefore, Cornelius teaches the first/second DRR devices providing pre-equalization of the electrical transit signals:



Ex-1003, ¶197.

Samaan provides additional support by addressing signal distortion in high-speed copper links and explaining that “a significant fraction of the ... distortion due to channel loss could be compensated for using simple equalization circuits in the transmitter...” Ex-1007, ¶¶5-8. This is pre-equalization. Samaan teaches two flavors of retimers (protocol-unaware or protocol-aware); both include an output driver with TxEQ for this purpose. Ex-1007, ¶¶207-220. The “output TxEQ” is “used to add de-emphasis and usually pre-emphasis also to the output.” Ex-1007, ¶225, Figs. 34-35.

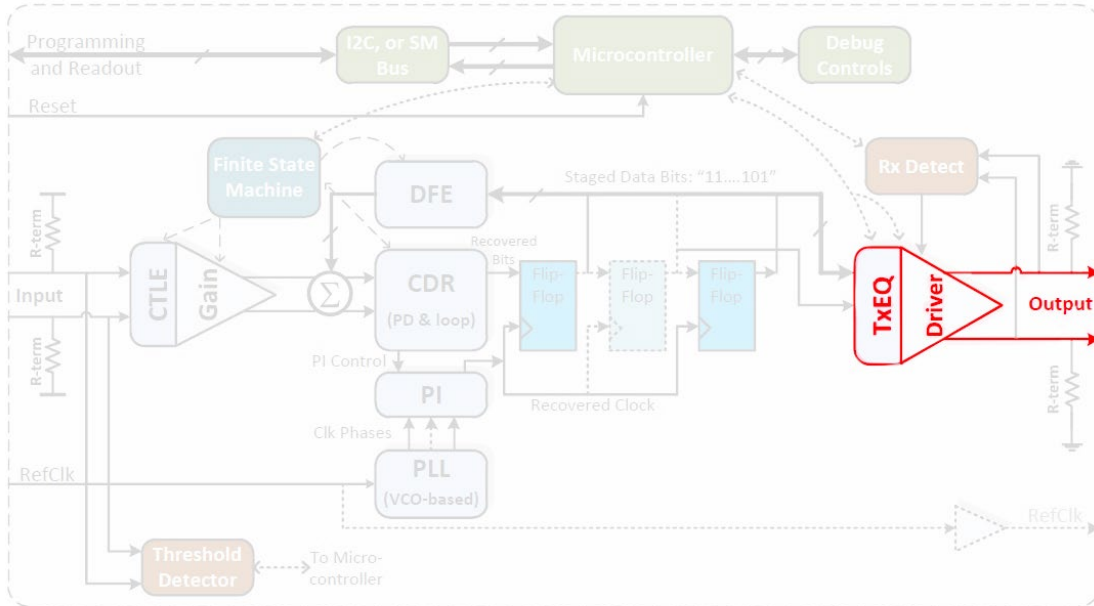


Figure 34 Conceptual micro-architecture of a “Bit Re-timer”, showing input CTLE, AGC, DFE, a CDR, and a data path connected directly to an **output driver with TxEQ**.

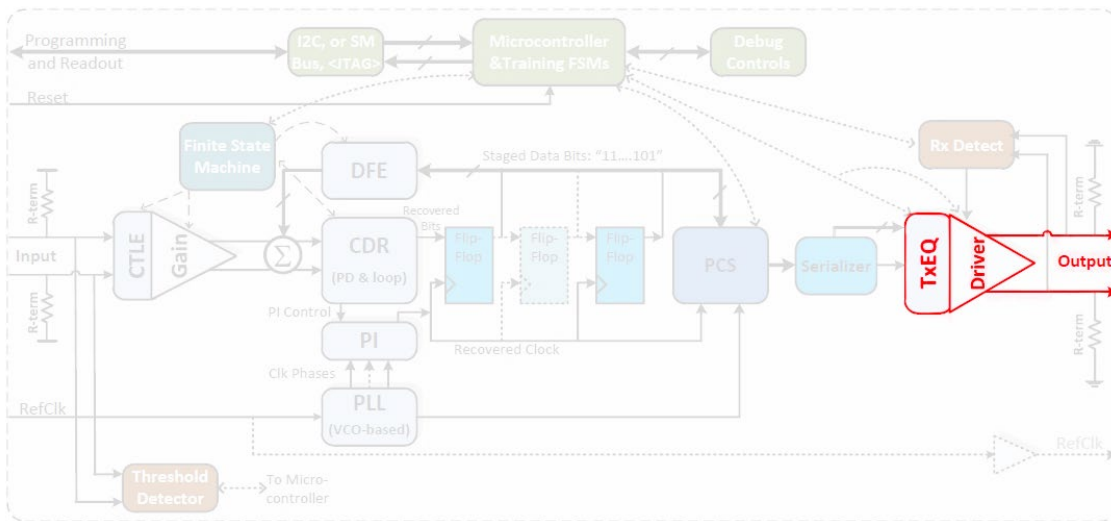
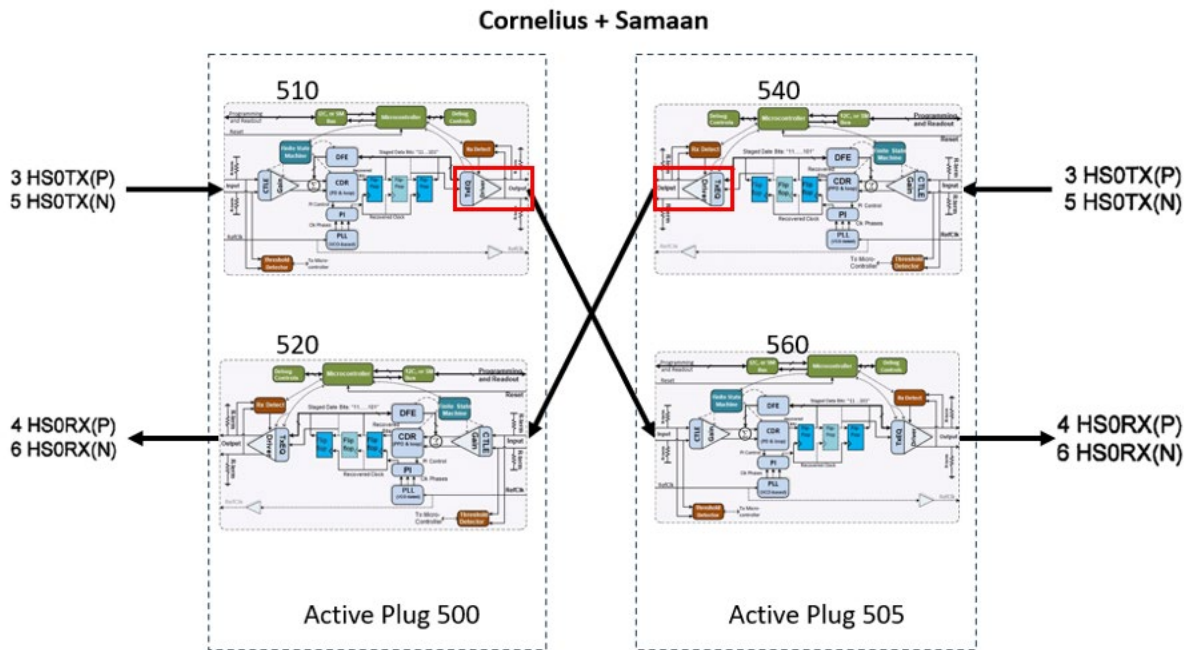


Figure 35 Conceptual micro-architecture of a “Protocol-aware Re-timer”, showing input equalization, a CDR, and a data path connected to a PCS, Serializer, and **output TxEQ driver**, with a Micro-controller.

Ex-1003, ¶¶198-199.

For the cable-facing transmitting side of an active plug, the output is the electrical transit signal sent over the cable; an example with Cornelius is illustrated below. *Supra* §V.B.3[1a] (explaining motivation and combination). Here, pre-

emphasis and de-emphasis, applied at the transmitter, perform pre-equalization to improve signal-to-noise ratio by adjusting the magnitude of certain frequency components before transmission. Ex-1007, ¶225, ¶¶5-8, Figs. 34-35. Therefore, the combination also teaches the first/second DRR devices providing pre-equalization of the electrical transit signals.



Ex-1003, ¶199.

Ground 4 teaches pre-equalization **using transmit filter coefficient values stored in nonvolatile memories**. Cornelius explains the channel compensation (equalization) circuit “may be adjusted using various parameters”—referring to filter coefficients—“determined by the manufacture and stored as presets for loading during operation.” Ex-1006, 11:45-62. The preset coefficient parameters would obviously have been stored in nonvolatile memory (otherwise they would be

lost). As Samaan explains, the transmit pre-equalization circuitry (e.g., output TxEQ circuit driver) is an “FIR filter” with “coefficients.” Ex-1007, ¶¶225, ¶¶78-81, Figs. 21-22, 34-35.

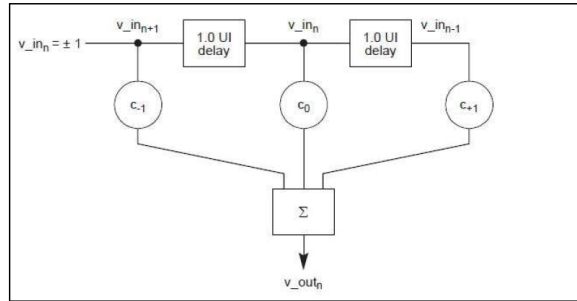


Figure 22 The PCIe 3.0 Tx Equalization FIR filter representation. (Note: The 10G-KR Filter is similar in definition).

Ex-1003, ¶200.

Gorecki likewise teaches transmitter pre-equalization (Ex-1005, 3:12-38, Abstract) using an FIR filter with tap coefficients. Ex-1005, 1:12-17, 6:38-41, 8:4-9:15. Gorecki further teaches storing “pre-programmed”/“pre-set” tap coefficient values in nonvolatile memories, including “ROM, PROM, EPROM, [or] EEPROM[.]” Ex-1005, 7:18-26; Ex-1005, 7:18-26; Ex-1003, ¶¶201-202.

Motivation to Combine. The combination of Cornelius and Samaan performs pre-equalization using filter coefficients. *Supra* §V.B.3[1a] (Motivation subsection). A POSITA would have been motivated to further apply Gorecki’s teachings by storing coefficient values in nonvolatile memory and retrieving the coefficient values using a controller. Ex-1005, 7:1-16, 9:3-15; Ex-1003, ¶203.

First, Cornelius already teaches preset coefficients stored during manufacturing (Ex-1006, 11:45-62) which teaches or suggests nonvolatile memory to preserve those presets. *Supra* §V.A.3[1f] (Motivation subsection explaining coefficient preservation). Using nonvolatile memory (e.g., EEPROM) had predictable results and a reasonable expectation of success because it has been used to store data in computers for many decades. Ex-1003, ¶204.

Moreover, a POSITA would have been motivated to use nonvolatile memory to store Cornelius and Samaan's coefficients, ensuring they are preserved when the cable is disconnected. Ex-1006, 11:45-62 (teaching power-up/restart); Ex-1007, ¶¶224-225, ¶¶139-147, Figs. 22, 31, Tables 1-2. For example, in situations where coefficient values were manually determined and entered for a specific cable deployment, storing them in nonvolatile memory avoids the need for recalculation and re-entry after each disconnection. Ex-1003, ¶205.

Storing coefficients in nonvolatile memory was advantageous because the cable could immediately access and use these values upon connection, eliminating the need to determine them on-the-fly. Even if link training were used to adjust coefficients during operation, a POSITA would still have been motivated to start with a baseline set of coefficients as a default when the cable is first connected, providing some level of equalization from the outset. *See* Ex-1007, ¶¶123-126 (describing "standard presets"). Thus, a POSITA would have been motivated to

use nonvolatile memory to have coefficient values readily available. Ex-1003, ¶206.

Additionally, all three references address high-speed communications, including for cables. E.g., Ex-1006, 3:33-64, 4:22-54; Ex-1007, ¶1, ¶¶5-8; Ex-1005, Abstract. As previously explained, all three recognize signal loss over cables and address it with transmitter pre-emphasis; both Samaan and Gorecki use FIR filters. Therefore, the combination uses a known technique (storing data in nonvolatile memory and reading with a controller) to improve similar devices in the same way. Ex-1003, ¶207.

The combination would not have changed the principle of operation. Storing and loading coefficients with a controller is consistent with Cornelius (Ex-1006, 11:45-62, Figs. 5-6), while Samaan leaves this trivial detail to the POSITA's knowledge. Gorecki already applies its teaching in the context of a cable. Ex-1006, 11:45-62. Ex-1003, ¶208.

In addition to the above-explained reasons, a POSITA would have had a reasonable expectation of success because computers have, for decades, stored values they require in nonvolatile memory, including e.g., EEPROM. This was a basic, undergraduate-level programming skill (*supra* §III) and a combination of prior art elements (using nonvolatile memory) according to known methods to yield predictable results. Ex-1003, ¶¶209-210.

4. Claim 2

2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.

Ground 4 was explained previously. *Supra* §V.B, §V.B.3[1a], [1f] (Motivation subsections). The DRR device (e.g., CDR/retimer circuitry), coefficients, and nonvolatile memories were explained previously. *Supra* §V.B.3[1f].

Gorecki teaches the rest of claim 2. Though explained in the context of Ground 2, Gorecki’s teachings likewise apply here. *Supra* §V.A.4; Ex-1003, ¶211.

A POSITA would have been motivated to combine Gorecki’s teachings—e.g., by using a controller to retrieve coefficients from memory and configure transmit filters—because Cornelius expressly teaches microcontrollers for configuration. Ex-1006, 6:21-24, 6:43-49, Claims 1, 3, 5, 8. The general programmability of microcontrollers make them well-suited for configuration; this was the easiest way to implement Cornelius and Gorecki’s teachings. Ex-1003, ¶212.

Cornelius teaches that the cable experiences “power-up” (Ex-1006, 11:58-62), thus providing motivation to apply Gorecki’s controller configuration teachings at power-up—particularly because Cornelius teaches coefficient

parameters “stored as presets for loading during operation.” Ex-1006, 11:45-55. Ex-1003, ¶213.

Samaan further supports this claim because it teaches that the “output TxEQ” is “usually under micro-controller control...” Ex-1007, ¶¶224-225. The micro-controller manages “all the phases of TxEQ adaptation from beginning to the end.” Ex-1007, ¶227. Samaan first sets the equalization parameters to “standard presets” values, meaning coefficients are stored in nonvolatile memories; the microcontroller retrieves them to use as baseline coefficients for the training process. Ex-1007, ¶¶123-126; Ex-1003, ¶214.

5. Claim 3

3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

Ground 4 was explained previously. *Supra* §V.B, §V.B.3[1a], [1f] (Motivation subsections). Ground 4 teaches the first/second DRR devices (e.g., CDR/retimer circuitry at respective ends) use transmit filter coefficient values. *Supra* §V.B.3[1f]. The configuration of filter coefficients was explained previously. *Supra* §V.B.4; Ex-1003, ¶¶215-216.

Gorecki teaches claim 3. Though explained in the context of Ground 2, Gorecki’s teachings likewise apply here. *Supra* §V.A.5; Ex-1003, ¶219.

Ground 4 further teaches the first/second DRR devices are **programmed** to use the coefficients. Cornelius teaches coefficient parameters “stored as presets for loading during operation” (Ex-1006, 11:45-55) and that the DRR devices are configured (e.g., programmed) by microcontrollers (Ex-1006, 6:11-24, 6:43-49, Claims 1, 3, 5, 8). Likewise, Samaan teaches that the TxEQ circuit, which is part of the DRR device has to be “programmable.” Ex-1007, ¶¶5-8, ¶¶207-220, ¶225, Figs. 34-35. Therefore, a POSITA would have been motivated to use microcontrollers to program the DRR devices to use preset coefficients. Ex-1003, ¶217.

The DRR devices are programmed **each time power is supplied to the first and second end connector plugs**. Cornelius describes power being supplied to the end connector plugs by connected hosts. Ex-1006, 8:27-40, 4:32-44, 8:10-15; *supra* §V.B.3[1a] (explaining plugs). When power is supplied, it was obvious to apply the references’ configuration teachings (explained above) to program both DRR devices to use their transmit coefficient values, so equalization can function properly. *See* Ex-1005, 7:18-33; Ex-1006, 6:11-20, 8:27-40; Ex-1003, ¶218.

6. Claim 4

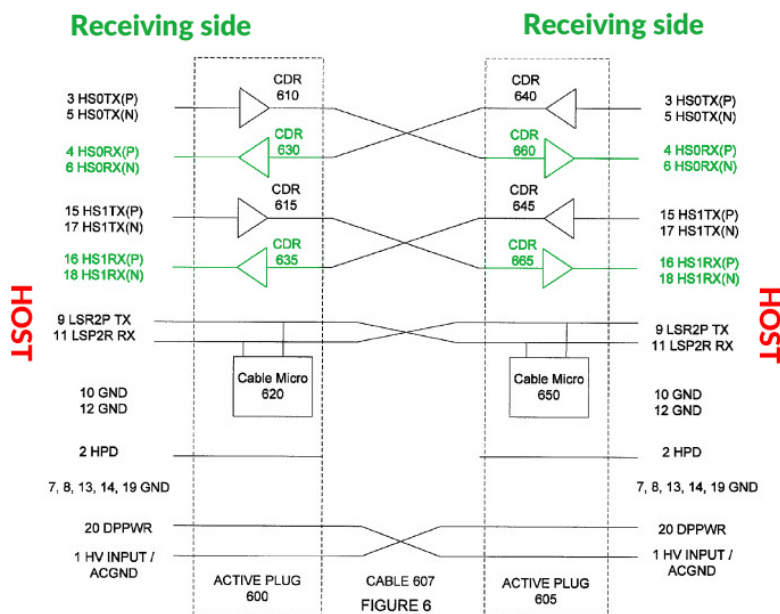
Gorecki teaches claim 4. Though explained in the context of Ground 2, Gorecki’s teachings likewise apply here. *Supra* §V.A.6; Ex-1003, ¶¶220-221.

7. Claim 5

5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

The combination of Ground 4 was explained previously. *Supra* §V.B, §V.B.3[1a], [1f] (Motivation subsections).

Cornelius teaches **the first and second DRR devices employ receiver-based equalization of the electrical transit signals**. Cornelius teaches symmetric DRR devices (e.g., CDR/retimer circuitry at respective cable ends). *Supra* §V.B.3[1b]. Each employs “equalizer circuits” including on the receiving side (Ex-1006, 6:30-42, Fig. 6, Claims 5, 10) to perform equalization on electrical transit signals to compensate for channel losses after crossing the cable.



Ex-1003, ¶222.

Samaan similarly teaches that “...channel loss could be compensated for using simple equalization circuits in...the receiver...” Ex-1007, ¶¶5-8. Samaan teaches Discrete Feedback Equalization (DFE) and CTLE and Gain (or AGC) Stage circuits in the re-timers to perform equalization to “cancel the residual pulse response tails (and ripples) in the incoming analog signal.” Ex-1007, ¶215, ¶220, ¶¶20-21. Incorporating Samaan’s re-timer structure into Cornelius’s active plugs (*supra* §V.B.3[1a]-[1b]) enables DFE and CTLE circuits to perform receiver-based equalization. Ex-1007, ¶215, ¶220, ¶¶20-21.

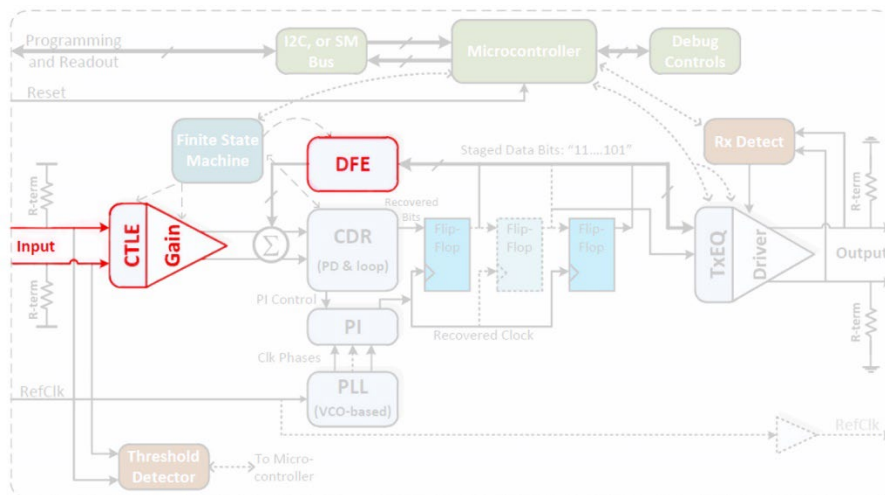
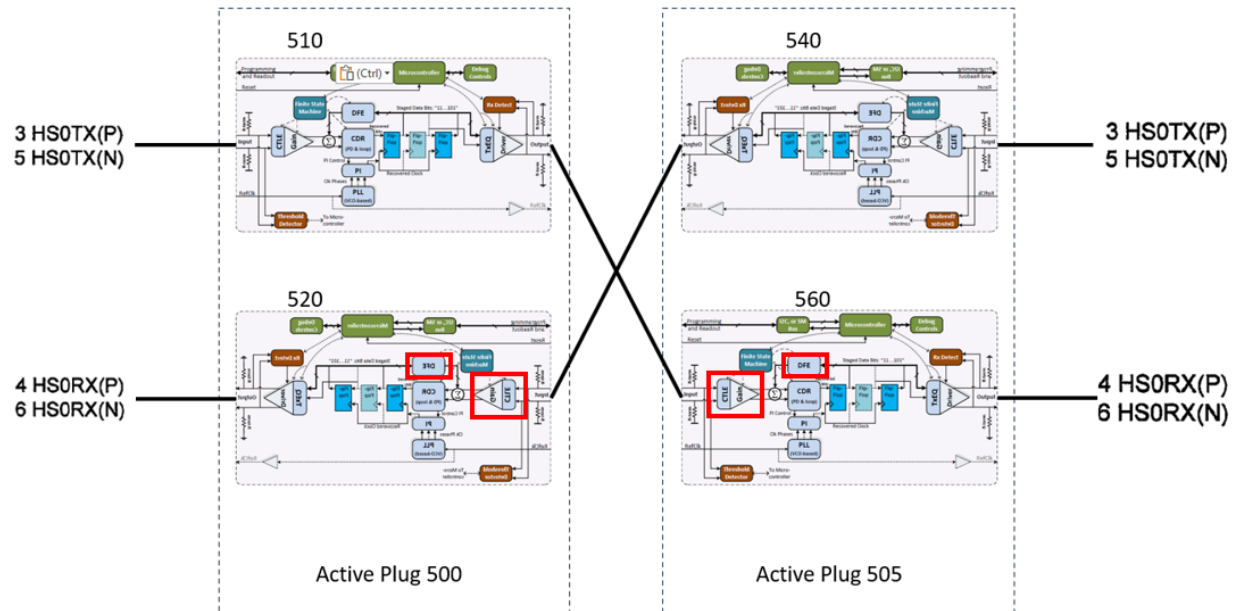


Figure 34 Conceptual micro-architecture of a “Bit Re-timer”, showing input CTLE, AGC, DFE, a CDR, and a data path connected directly to an output driver with TxEQ.



Ex-1003, ¶223.

Gorecki teaches **using coefficient values stored in the nonvolatile memories**. Though explained in the context of Ground 2, Gorecki’s teachings likewise apply here. *Supra* §V.A.7; Ex-1003, ¶224.

8. Claim 6

6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

Cornelius teaches providing “high-speed differential signal paths.” Ex-1006, 1:64-2:2; 9:62-65. Twin-axial conductors were associated with high-speed differential signals because they were one of the most commonly-used cables for high-speed differential signals. Therefore, it was obvious to use twin-axial

conductors for Cornelius's high-speed differential signal paths. *Id.*; Ex-1003, ¶225.

9. Claim 7

As previously explained, Gorecki and Samaan teach claim 7; that analysis applies here. *Supra* §V.A.9; Ex-1003, ¶226.

10. Claim 8

[8pre] A cable manufacturing method that comprises:

Ground 4 teaches the cable of claim 1. *Supra* §V.B.3. Ground 4 further teaches a method of manufacturing a cable by connecting the components of Cornelius's active cable together, including the steps explained for limitations below. Ex-1006, Title, 5:33-39, 6:6-20, 8:20-40, Figs. 5-6, Claims 1-10; Ex-1003, ¶228.

[8a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;

Most of limitation [8a] mirrors [1a]; Ground 4 teaches the overlapping limitations as explained above. *Supra* §V.B.3[1a]; Ex-1003, ¶229.

Cornelius further teaches **connecting a first connector plug** to the first DRR device (e.g., CDR/retimer circuitry). Each plug comprises an end portion with pins the CDR/retimer circuitry uses to exchange inbound/outbound data streams with the host. *Supra* §V.B.3[1a]; Ex-1006, Figs. 3, 5-6.

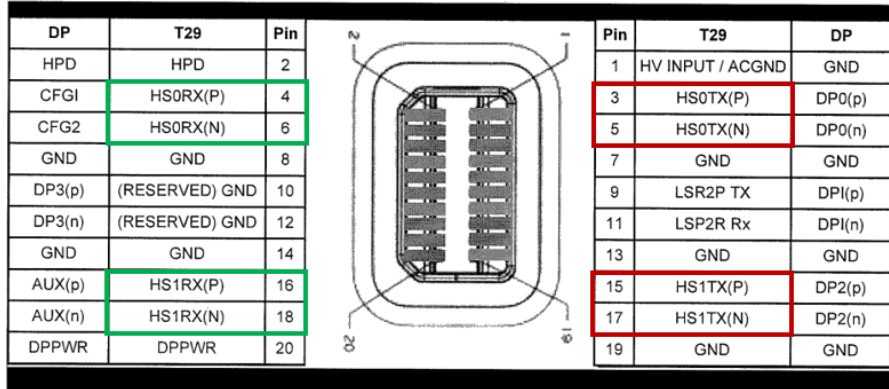
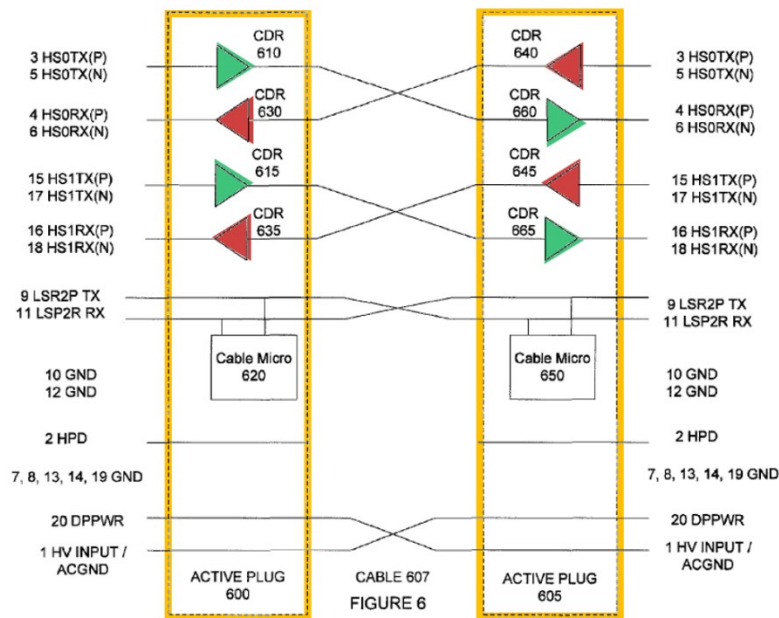


FIGURE 3

Each CDR/retimer circuitry is connected to specific connector pins.



Ex-1003, ¶230.

Therefore, Cornelius teaches or suggests that these components were connected during manufacturing because they are connected in an assembled cable.

Ex-1006, Figs. 5-6; Ex-1003, ¶231.

[8b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;

Limitation [8b] mirrors [8a], differing only by changing “first” to “second.” Cornelius teaches a cable with symmetric CDR/retimer circuitry at each end. *Supra* §V.B.3[1a]-[1b] (explaining Cornelius’ symmetry). Either CDR/retimer circuitry would be the first DRR device; the other would be the second. *Supra* §V.B.10[8a]. The interface port and plug for the second CDR/retimer circuitry would be the second host interface port and second connector plug. Therefore, limitation [8b] is satisfied for the same reasons explained for [8a]. *Supra* §V.B.10[8a]; Ex-1003, ¶¶232-233.

[8c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,

Most of limitation [8c] mirrors [1c]; Ground 4 teaches the overlapping limitations as explained above. *Supra* §V.B.3[1c]; Ex-1003, ¶234.

Cornelius also teaches **connecting electrical conductors to the first and second DRR devices** (e.g., CDR/retimer circuitry at respective ends of the cable). Cornelius teaches that they are connected. *Supra* §V.B.3[1c]. Therefore, Cornelius teaches or suggests that these components were connected during manufacturing because they are connected in an assembled cable. Ex-1006, Figs. 5-6; Ex-1003, ¶235.

[8d]-[8f]

The limitations in [8d]-[8f] also appear in [1d]-[1f], respectively, and are satisfied for the same reasons. *Supra* §V.B.3[1d]-[1f]; Ex-1003, ¶236.

11. Claim 9

Beyond the preamble, claim 9 mostly overlaps with claim 2; Ground 4 teaches the overlapping limitations. *Supra* §V.B.4; Ex-1003, ¶237.

Ground 4 also teaches **providing** a first controller **device** because Ground 4 teaches a first controller, a device that is part of the active cable. *Supra* §V.B.4. It was obvious to provide a controller to perform the functions Ground 2 teaches. Ex-1003, ¶238.

As explained before, Gorecki teaches **internal** nonvolatile memory. *Supra* §V.A.11; Ex-1003, ¶239.

12. Claim 10

10. The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

The limitation of claim 10 is identical to claim 3, other than a change to verb tense and passive voice (“programmed” to “programming”). Therefore, claim 10 is satisfied for the same reasons. *Supra* §V.B.5; Ex-1003, ¶240.

13. Claim 11

11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.

Ground 4 was explained previously. *Supra* §V.B, §V.B.3[1a], [1f] (Motivation subsections). For Ground 4, Gorecki teaches the transmit filter coefficient values being determined and stored in nonvolatile memory after cable assembly (*supra* §V.A.6, §V.B.6), which includes connecting the electrical conductors (*supra* §V.B.10[8c], §V.B.3[1c]); Ex-1003, ¶241.

Pre-equalization compensates for the loss characteristics of the channel. As Samaan explains, the “equalization circuits in the transmitter” (e.g., FIR filters), compensate signal “distortion due to channel loss.” Ex-1007, ¶8, ¶225. Likewise, Gorecki teaches transmitter pre-equalization to “compensate for bandwidth limitations and reflections[.]” Ex-1005, 3:8-27. FIR filter coefficients are “pre-programmed or pre-set” so that the introduced “compensation...is ideally the inverse of the effects caused by the communication channel.” Ex-1005, 7:18-33, 9:3-15. Therefore, Ground 4 teaches determining filter coefficients by characterizing channel characteristics, so that the pre-equalization filter in the active cable can compensate for them. *See, e.g.*, Ex-1007, ¶225, ¶¶78-81, Figs. 21-22, 35; Ex-1005, 3:8-27, 7:18-33, 9:3-15; Ex-1003, ¶242.

14. Claims 12-14

The limitations of claims 12-14 are identical to claims 5-7 and satisfied for the same reasons. *Supra* §V.B.7-9; Ex-1003, ¶243.

15. Claim 15

[15pre] A communications method that comprises:

Ground 4 teaches a **communications method**. Cornelius teaches “[c]ircuits, methods, and apparatus” for its cable teachings. Ex-1006, Abstract, 1:50-51, 1:55-58, 4:66-5:1. Similarly, Samaan’s teachings encompass retiming steps and a “method of propagating” related messages. E.g., Ex-1007, ¶¶257-260, Figs. 39-40, Table 3. The communications method further includes limitations [15a]-[15c]. Ex-1003, ¶¶245-246.

[15a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and

Cornelius teaches **inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first DRR device** (e.g., CDR/retimer circuitry). Each active plug comprises an end portion that is a connector plug. *Supra* §V.B.3[1a]. The end portion is “inserted” in a first host device. Ex-1006, 7:7-17, 8:27-40 (“...a host device connected to

plug 600...”). Additionally, it was obvious to insert the plug given the nature of cables. The first CDR/retimer circuitry exchanges inbound/outbound data streams via a first end connector plug and therefore is connected to it. *Supra* §V.B.3[1a]; Ex-1003, ¶247.

The rest of [15a] combines elements recited in [1a], [1c], and [1d] and are taught for the same reasons. *Supra* §V.B.3[1a], [1c]-[1d]; Ex-1003, ¶248.

[15b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,

Limitation [15b] mirrors [15a] but changes “first” to “second.” The analysis for [15a] (*supra* §V.B.15[15a]) applies here because Ground 4 teaches a cable with symmetric CDR/retimer circuitry at each end. *Supra* §V.B.3[1a]-[1b] (explaining symmetry). Either CDR/retimer circuitry would be the first DRR device; the other would be the second, with corresponding second host interface port and end connector plug, for reasons explained previously. Ex-1003, ¶¶249-250.

[15c] ...

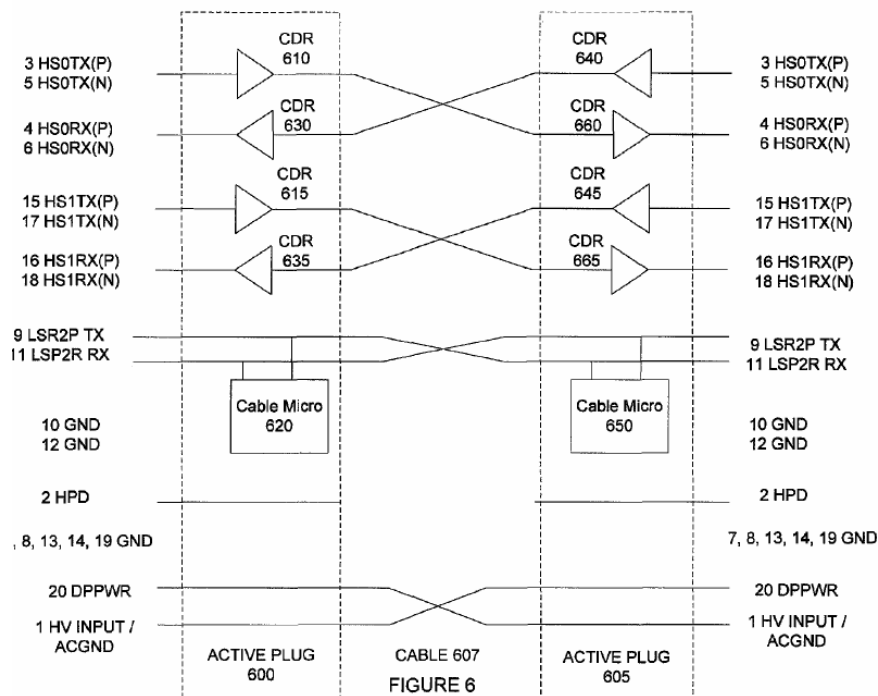
Limitation [15c] is identical to [1f] and is satisfied for the same reasons. *Supra* §V.B.3[1f]; Ex-1003, ¶251.

16. Claim 16

16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.

Cornelius teaches **supplying power to the first and second end connector plugs**. For example, Cornelius teaches that “a host device connected to plug 600 may provide power for plugs 600 and 605.” Ex-1006, 8:27-40, 8:10-15, 7:26-4; Ex-1003, ¶252.

Ground 4 teaches **the first and second end connector plugs being connected to first and second controller devices, respectively**. Cornelius teaches a microcontroller in each active plug. Ex-1006, 6:21-24, 6:43-49, Claims 1, 3, 5 and 8, Figs. 5-6. Each active plug comprises an end portion that is a connector plug. *Supra* §V.B.3[1a]-[1b]. That end connector plug is connected to the microcontroller on pins 9 and 11. Ex-1006, Figs. 3, 5-6.



Ex-1003, ¶253.

Ground 4 teaches the rest of claim 16 with respect to a first controller and DRR device, explained above. *Supra* §V.B.4. Because Cornelius’s cable is symmetric, Ground 4 teaches claim 16 for the second controller and DRR device for the same reasons. *Supra* §V.B.3[1b] (explaining symmetry); Ex-1003, ¶254.

17. Claims 17-20

Claims 17-20 recite identical limitations to claims 3-5 and 7, respectively, and are satisfied for the same reasons. *Supra* §V.B.5-7, 9; Ex-1003, ¶255.

VI. STANDING

Petitioner certifies that Petitioner is not barred or estopped from requesting this inter partes review, and the ’233 patent is eligible for it.

VII. MANDATORY NOTICES AND FEES

Real Party In Interest: The real party-in-interest here is Marvell Semiconductor Inc. No other parties directed, controlled, or funded this Inter Partes Review proceeding (IPR).

Related Matters:

- Certain Active Electrical Cables and Components Thereof, ITC Investigation 337-TA-1446
- *Credo Semiconductor Inc. and Credo Technology Group Ltd. v. Volex PLC*, 2:25-cv-00298-JRG (EDTX)

Lead and Backup Counsel: Pursuant to 37 C.F.R. §42.8(b)(3) and 42.10(a), Petitioner designates Harper Batts (Reg. No. 56,160) as lead counsel and Chris Ponder (Reg. No. 77,167) and Jeffrey Liang (Reg. No. 69,043) as back-up counsel, each of Sheppard, Mullin, Richter & Hampton LLP.

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Petitioner's counsel may also be served by mail or hand delivery at Sheppard, Mullin, Richter & Hampton LLP, 1540 El Camino Real Suite 120, Menlo Park, CA 94025. Petitioner's counsel may be reached by telephone at (650) 815-2673 and by facsimile at (650) 815-4668.

Fees: The Office is authorized to charge fees for this Petition to Deposit
Account 50-4561, Ref. 20SW-408772.

Respectfully submitted,

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/Harper Batts/

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CLAIM APPENDIX

Claim 1	
[1pre]	A cable that comprises:
[1a]	a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;
[1b]	a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and
[1c]	electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween,
[1d]	the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and
[1e]	the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,
[1f]	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
Claim 2	
2	The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.
Claim 3	
3	The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

Claim 4	
4	The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.
Claim 5	
5	The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
Claim 6	
6	The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
Claim 7	
7	The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.
Claim 8	
[8pre]	A cable manufacturing method that comprises:
[8a]	connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;
[8b]	connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;
[8c]	connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween,
[8d]	the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and
[8e]	the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,
[8f]	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

Claim 9	
9	The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.
Claim 10	
10	The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
Claim 11	
11	The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.
Claim 12	
12	The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
Claim 13	
13	The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
Claim 14	
14	The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.
Claim 15	
[15pre]	A communications method that comprises:
[15a]	inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane

	data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and
[15b]	inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,
[15c]	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
Claim 16	
16	The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.
Claim 17	
17	The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.
Claim 18	
18	The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.
Claim 19	
19	The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.
Claim 20	
20	The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on August 1, 2025, true and correct copies of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,877,233 and Exhibits 1001-1035 were served in their entirety on the Patent Owner at the following addresses of record as listed on Patent Center, via Priority Mail Express®:

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**CERTIFICATE OF COMPLIANCE WITH
TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS,
AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,365 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

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