



PCI Express* Architecture

These free resources are available to the Intel® Developer Network for PCI Express* Architecture community.

PCI Express* (PCIe) Specifications

[Root Complex IDE Key Configuration Unit - Software Programming Guide](#) defines the Intel Root Port register programming interface for configuring PCI Express* (PCIe*) Integrity and Data Encryption (IDE) and Compute Express Link (CXL) Integrity and Data Encryption (IDE) capabilities. Send your feedback to rc_ide_spec_support@intel.com.

The [PHY Interface for the PCI Express* \(PIPE\) Architecture Revision 7.0](#) is an updated version of the PIPE spec that supports PCI Express*, SATA, USB3.2, DisplayPort, and USB4 Architectures.

The [LPIF Adapter for Die-to-Die Interconnect Revision 0.5](#) outlines implementation guidelines for using the Logical PHY Interface (LPIF) for die-to-die transport.

The PCI Express* Device Security Enhancements Specification is deprecated and is not recommended for new implementations. Instead, please refer to the Security Protocol and Data Model (SPDM) Specification (<https://www.dmtf.org/dsp/DSP0274>) and Component Measurement and Authentication (CMA) & Data Object Exchange (DOE) ECNs (<https://pcisig.com/specifications>).

PCI Express* Resources

If you're new to PCI Express*, check out content from the PCI-SIG*.

[Read the PDF \(744 KB\) >](#)

Compute Express Link™ (CXL) Resources

[CXL-cache/mem Protocol Interface \(CPI\) specification](#), has been developed to map coherent protocols between an agent and a fabric.

[Streaming Fabric Interface \(SFI\) Specification](#) has been developed to map Load/Store protocols (like PCIe) between an agent and a fabric.

[CXL Memory Device SW Guide](#) describes how System Firmware, OS and UEFI may configure CXL Type 3 devices.

White Papers

- [High-Speed Serial Bus Repeater Primer](#)
- [PCI Express* 4.0 Retimer Supplemental Features and Standard BGA Footprint](#)
- [PCIe* 5.0 Retimer Supplemental Features and Standard BGA Footprint](#)

Tools

In addition to the software and resources available through the PCI-SIG*, Intel has developed the procedures and design information below to assist in verifying connector suitability for use in systems implementing PCI Express*.

- [PCI Express* 5.0 CEM Connector High Speed Electrical Test Procedure](#)
- [PCI Express* 5.0 Connector Measurement Board File](#)
- [PCI Express* 4.0 Connector Measurement Board File](#)
- [PCI Express* 4.0 Connector High Speed Electrical Test Procedure](#)
- [PCI Express* 3.0 Connector High Speed Connector Evaluation Board \(CEB\) \(ZIP 1.6MB\)](#)
- [PCI Express* 3.0 Characterization Board Support Bracket Design \(ZIP 334KB\)](#)