

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Marvell Semiconductor, Inc.,

Petitioner,

v.

Credo Technology Group Ltd.,

Patent Owner.

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IPR2025-01220

U.S. Patent No. 11,032,111

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**PETITION FOR *INTER PARTES* REVIEW**

**OF U.S. PATENT NO. 11,032,111**

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## EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 11,032,111 to Sun et al. (the '111 patent)
1002	Certified Prosecution History for the '111 patent ("Prosecution History")
1003	Declaration of Michael S. Chen
1004	U.S. Patent App. Pub. No. 2019/0288881 to Berke et al. ("Berke")
1005	U.S. Patent No. 8,516,238 to Cornelius, et al. ("Cornelius")
1006	U.S. Patent No. 10,715,357 to Ran ("Ran")
1007	U.S. Prov. App. Serial No. 62/722,517 ("Ran Provisional")
1008	Excerpts from Stauffer, High Speed Serdes Devices and Applications ("Stauffer")
1009	U.S. Patent App. Pub. No. 2014/0237301 to Mejia et al. ("Mejia")
1010	PCI Express Base Specification Revision 3.0 (Nov. 10, 2010)
1011	Serial ATA Revision Specification 3.1 (July 18, 2011)
1012	Excerpts of IEEE 802.3-2015 Standard
1013	Declaration of June Munford re: Stauffer
1014	Library of Congress Certification for Stauffer
1015	Internet Archive Declaration of Mina Ching re: Stauffer
1016	Declaration of Liliana Nunez re: Stauffer
1017	U.S. Patent App. Pub. No. 2013/0223506 to Kolze
1018	U.S. Patent App. Pub. No. 2010/0232493 to Thirumoorthy
1019	U.S. Patent App. Pub. No. 2013/0201316 to Binder et al.
1020	U.S. Patent No. 5,648,972 to Gharakhanian
1021	U.S. Prov. App. Serial No. 63467_62723701 ('111 Patent Provisional)
1022	Excerpts from Gasca, et al., CMOS Continuous-Time Adaptive Equalizers for High-Speed Serial Links
1023	U.S. Patent No. 7,233,617 to Gorecki
1024	U.S. Patent App. Pub. No. 2003/0035497 to Gorecki et al.
1025	TE Connectivity, SFP+ High Speed Copper Cable Assemblies
1026	Cisco, Cisco 40GBASE QSFP Modules Data Sheet
1027	Wang & Bovik, Mean Squared Error: Love It or Leave It?
1028	U.S. Patent No. 8,665,941 to Eliaz
1029	U.S. Patent No. 8,600,039 to Chen et al.
1030	U.S. Patent No. 5,392,315 to Laud

Serial communications have long used a technique called equalization, which used filters to improve the quality of signals transmitted over a channel. These filters included coefficients that were adjusted to match the specific characteristics of the channel. When conditions changed—e.g., from temperature shifts—training processes updated the initial coefficients. These fundamental techniques were taught in textbooks and college courses. Moreover, to accommodate different environments, systems often stored multiple sets of initial coefficients to choose from as a starting point for operation.

Against this backdrop, the '111 patent identified an increasing need for equalization as data rates increased. As a solution, the patent proposes the use of link training, with a set of initial coefficients. This, however, was a trivial concept that was already known in the art.

## **I. OVERVIEW OF THE TECHNOLOGY**

High-speed serial communications became widespread in the 1990s as an alternative to parallel communications, which used multiple signal lines in parallel. As transmission speeds increased, parallel systems faced synchronization/routing challenges. Serial communication addressed these limitations by using a single channel, simplifying synchronization, and reducing pin count. Ex-1003, ¶4.

By the early 2000s, computer bus and networking protocols had largely shifted to serial connections. Serial ATA (“SATA”) replaced parallel ATA; serial

PCIe replaced parallel PCI; and Universal Serial Bus (“USB”) replaced legacy parallel interfaces. Ethernet had long utilized serial connections. This process—where parallel data within a chip was converted into a serial bitstream (serialization), sent over a serial link, and then converted back into parallel (deserialization)—was called “SerDes.” Ex-1003, ¶5.

Ethernet has been a widely used networking standard since the 1990s. By the 2010s, Ethernet had become the primary high-speed serial communication standard for enterprise and data center networks, scaling from 1 Gigabit Ethernet (GbE) to widespread 10 GbE adoption. Serial cables are examples that implement the ubiquitous Ethernet standard. Ex-1008, 000058-000061. Ex-1003, ¶6.

#### **A. Equalization**

As connection protocols shifted to serial links, established serial communication techniques like equalization were adopted. Well before 2018, equalization was a standard topic in undergraduate courses on serial communications and routinely covered in relevant textbooks. Ex-1008, 000020-000024; Ex-1022, §1.1.1; Ex-1003, ¶7.

Equalization performed at the transmitter was called “preequalization.” Preequalization adjusts the signal prior to the signal being sent over the channel to compensate for anticipated signal loss. Equalization was also performed at the receiver to adjust for channel losses after the signal crossed the channel. This

combination of pre-equalization at the transmitter and equalization at the receiver enabled robust, high-speed transmission across noisy channels. Ex-1008, 000020-000024; Ex-1003, ¶8.

Because channels attenuate different frequencies unevenly, pre-equalization selectively boosted signal frequencies expected to experience greater loss. This ensured the received signal more closely matched the original signal after crossing the channel. Pre-equalization is illustrated below: the red boxes show the original waveform with and without pre-equalization. Ex-1008, FIGS. 1.9-1.10 at 000021:<sup>1</sup>

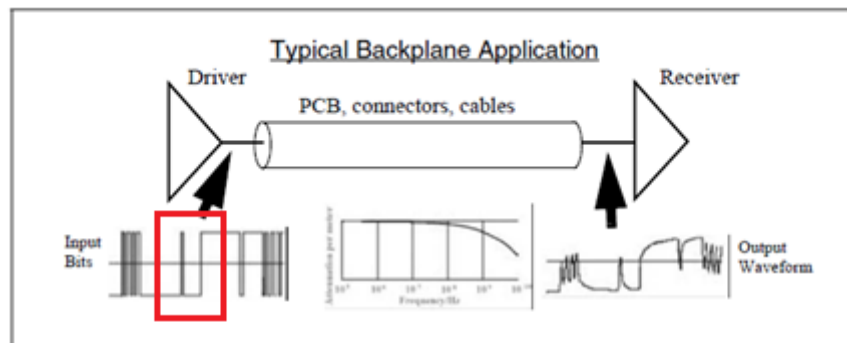


Fig. 1.9 Signal distortion for a typical channel application

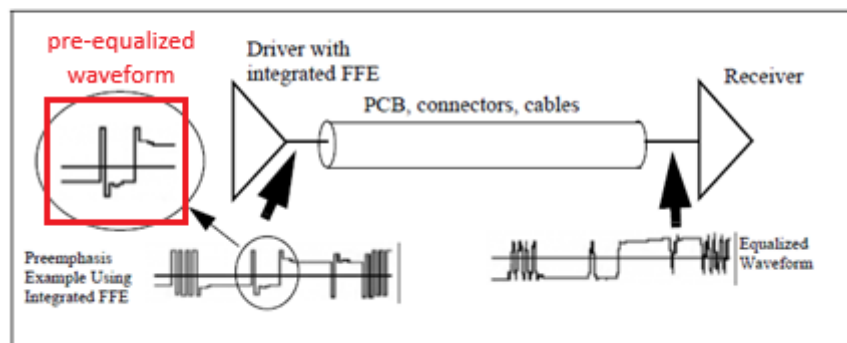


Fig. 1.10 Typical channel application with equalization at the transmitter

<sup>1</sup> All emphasis and annotations added unless stated otherwise.

Ex-1003, ¶9.

Pre-equalization was often implemented at the transmitter using a finite impulse response (“FIR”) filter. An FIR filter performs a weighted sum by multiplying adjacent data “taps” with coefficients. For pre-equalization, these coefficients are selected to amplify frequencies that the channel diminishes. As a result, the effects of the filter and channel cancel each other out, leaving the signal closer to its original form. A specific implementation is a Feed-Forward Equalizer (“FFE”). Ex-1008, 000020-000021, 000050; Ex-1022, 000025-000027.

Equalization could also be added at the receiver end of the channel to further compensate for the channel loss. Ex-1003, ¶¶10-11.

Because channel conditions changed, for example due to temperature variation, many serial communications systems used “training” to update equalization coefficients to the current channel characteristics. Training was a basic concept taught in textbooks and undergraduate courses on serial communications. Ex-1008, 000067-000069; Ex-1004, ¶3; Ex-1006, Abstract, 3:29-50, 15:45-50; Ex-1009, ¶32; Ex-1003, ¶12.

Coefficient training usually started by configuring the channel with initial equalization coefficient values. Since the effectiveness of the training process depended on the quality of the initial coefficient values, it was common practice for serial communications systems to store multiple sets of “preset” or

“whitelisted” equalization coefficient values for use as the starting point or initial values for coefficient training. Ex-1004, ¶¶30-32; Ex-1006, 10:6-14, Fig. 3B.

Bit 13	Bit 12	Description
1	1	Preset3
1	0	Preset2
0	1	Preset1
0	0	Co-efficient Control

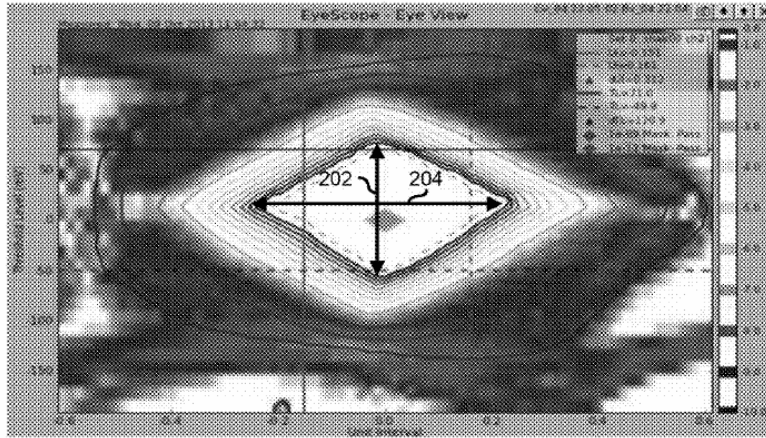
**FIG. 3B**

Different baseline coefficients sets reflected different channel characteristics, allowing selection of the most suitable set as a starting point for training based on its performance for a particular channel. Ex-1004, ¶¶30-33, Ex-1009, ¶¶31-32, ¶36; Ex-1003, ¶12.

### **B. Channel Loss & Transmission Performance**

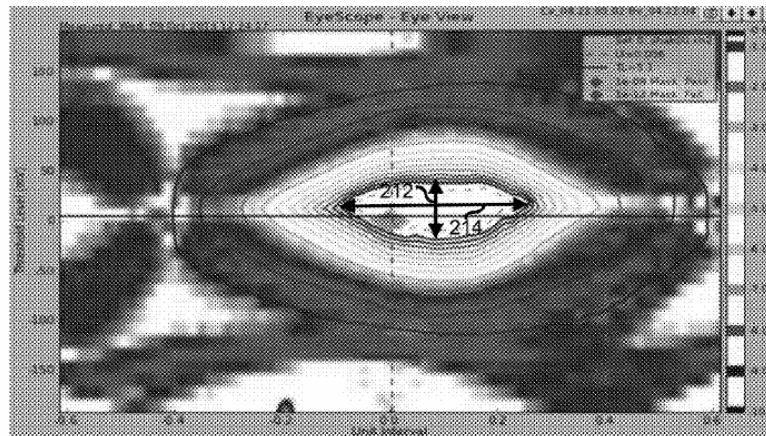
Bit Error Rate (“BER”) and opening of an eye diagram were common criteria for evaluating performance of high-speed serial communications systems. Ex-1008, 000014-000015, 000020-000021; Ex-1003, ¶¶13-15.

BER quantifies how often errors occur due to noise, interference, or distortion in the transmission channel. A lower BER indicates a more reliable communication link, and vice versa. Ex-1008, 000014-000015; Ex-1003, ¶16. Eye diagrams visually display overlapping traces of a digital waveform to allow quality assessment based on noise, jitter, and signal distortion:



200

Run 1	T0	T1	T2	T3	T4	CTLE <sub>L</sub>	CTLE <sub>H</sub>	VGA
Whitelist Coefficient	8	5	-2	-1	0	10	7	13



210

Run 2	T0	T1	T2	T3	T4	CTLE <sub>L</sub>	CTLE <sub>H</sub>	VGA
Converged Coefficient	7	4	-1	-1	0	9	8	10

**FIG. 2**

Ex-1004, FIG. 2, ¶22. It was a well-known metric taught in undergraduate courses to measure “eye opening” for assessing the overall link quality in high-speed serial communications, including the impact of equalization. Ex-1008, 000014-000015; Ex-1003, ¶17.

## **II. THE '111 PATENT**

The '111 patent notes a problem of increased channel attenuation and dispersion in serial communications caused by the demand of “ever-higher data rates.” Ex-1001, 1:28-34. To address the problem, the '111 patent purports to select initial pre-equalizer coefficients, stored in registers, and then use link training to refine them. Ex-1001, 1:39-58; Ex-1003, ¶18.

### **A. Prosecution History**

The application for the '111 patent was allowed after two Office Actions, where the Examiner rejected some claims as being obvious and identified other claims as allowable. Ex-1002, 000331-000345, 000389-000396. The Applicant overcame the Office Actions by incorporating allowable subject matter, including “each of the multiple registers corresponding to a different channel model,” without disputing the Examiner’s obviousness rejections. Ex-1002, 000370-000375, 000413-18. Neither the Examiner nor the Applicant explained why the allowable subject matter was non-obvious in view of the prior art. Ex-1003, ¶¶19-20.

### **B. Priority Date**

The specification of the '111 patent includes disclosure that is not in its provisional application, including that related to “channel model,” “chip-to-module (C2M) communications link,” or “pluggable module.” The '111 patent is not entitled to the priority date of its provisional application because each of its

independent claim is not adequately supported by the written description of the provisional application. Ex-1003, ¶23. Nonetheless, this Petition analyzes invalidity as of August 28, 2018, and the analysis does not change for obviousness as of August 27, 2019. Ex-1003, ¶¶22-24.

### **III. FIELD AND LEVEL OF ORDINARY SKILL**

The field of the patent is serial communications. *See, e.g.*, Ex-1001, Abstract, 1:19-35. The patent is directed to methods for sending data in serial form over a channel. *Id.*, Abstract, 1:49-54, cls.11, 16. The specification states that the '111 patent's communications method is implemented on a transceiver "as application-specific integrated circuitry for very high-rate serial data transmission and reception." *Id.*, 5:10-16, Abstract, 1:39-41, 5:24-34, 10:4-11, 6:34-37, FIGS. 4-5, 10:39-40. Independent claims 8, 11, and 16 all recite "serial" communications, and claim 1 recites "SerDes," which includes serialization for serial communications. *Supra* §I.A; Ex-1003, ¶26.

A person of ordinary skill in the field of art ("POSITA") would have been a person with a bachelor's degree in electrical or computer engineering with at least three years of experience in serial communications. A person with more education but less practical experience may also meet this standard. Ex-1003, ¶28.

In the relevant timeframe, a POSITA with the above-described level of skill would have been able to:

- Understand common high-speed serial components, including equalization, pre-equalization, and FIR filters;
- Evaluate channel loss, compensation, and channel performance using indicators such as BER and eye diagrams;
- Design high-speed serial communication systems;
- Design equalization/pre-equalization filters, including FFE and coefficients;
- Design equalization training methods;
- Program a digital signal processor (“DSP”) to perform common transceiver functions;
- Implement protocols for calibrating and setting equalization parameters; and
- Configure host port connector and cable/card plugs with embedded transceivers.

Ex-1003, ¶29.

#### **IV. CLAIM CONSTRUCTION**

Claims should be construed according to the ordinary and customary meaning as understood by a POSITA.

## V. INVALIDITY GROUNDS

Petitioner requests *inter partes* review and cancelation of the challenged claims on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1, 3, 4, 6-8, 10-11, 13-17, 19	§103	Berke and Cornelius
2	1, 3, 4, 6-8, 10-11, 13-17, 19	§103	Berke and Ran
3	2, 5, 9, 12, 18	§103	Berke, Cornelius, and Stauffer
4	2, 5, 9, 12, 18	§103	Berke, Ran, and Stauffer
5	1-19	§103	Ran, Mejia, and Stauffer

The Grounds render the challenged claims obvious because any differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a POSITA to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

None of these references were considered during examination. Ex-1003, ¶21.

### A. Ground 1

Ground 1 applies Berke's techniques for selecting and updating pre-equalizer coefficient values to Cornelius's active cable teachings, in particular for

communications between a pluggable module of the cable and host. *Infra* §V.A.9[8pre]; Ex-1003, ¶33.

### **1. Berke (Ex-1004)**

Berke is post-AIA §102(a)(2) prior art; it was filed March 19, 2018 and published September 19, 2019. Berke teaches optimizations for equalization coefficients in a high-speed serial interface, namely that coefficients known to provide “robust” performance are stored in a “whitelist” comprising a “group of registers.” Ex-1004, ¶¶12-15, 30, FIG. 1. Whitelisted coefficients are selected as starting points for adaptive equalization training. Ex-1004, ¶33, ¶30, ¶13, ¶¶24-26; Ex-1003, ¶¶35-36.

Berke is analogous art because it is in the same field. *Compare supra* §III *with* Ex-1004, Title, ¶¶1-4, 13, 35, 39. Berke is also reasonably pertinent because it relates to ensuring reliable data transmission through a communication channel. Ex-1004, ¶3; Ex-1003, ¶37.

### **2. Cornelius (Ex-1005)**

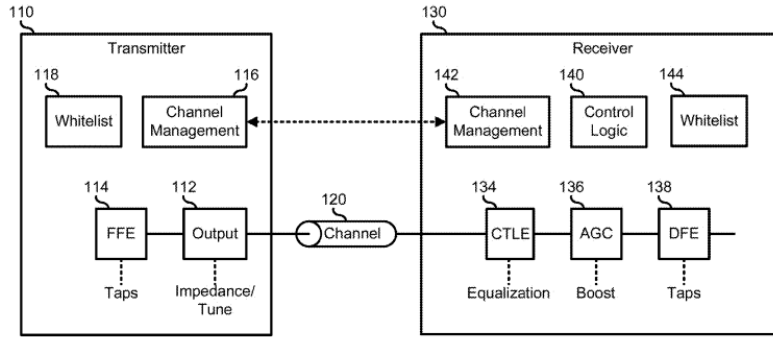
Cornelius is prior art under post-AIA §§102(a)(1)-(2); it issued August 2013. Cornelius teaches a high-speed active cable with transceivers at each end. Ex-1005, 4:22-65, 6:11-24, 8:20-26, FIGS. 5-6. Cornelius uses equalization for various communication paths. *Id.*, 11:45-51; Ex-1003, ¶39.

Cornelius is analogous art because it is in the same field. *Compare supra* §III *with* Ex-1005, Abstract, 1:15-22. Cornelius is also reasonably pertinent; it relates to ensuring reliable data transmission through a serial communications channel. Ex-1005, 11:45-62; Ex-1003, ¶40.

### 3. Claim 1

**[1pre] A SerDes communications method that comprises, in a transceiver:**

To the extent the preamble is limiting, Ground 1 teaches a **SerDes communications method**. Berke teaches “a high-speed serial channel 100 of an information handling system,” where two components communicate over “a bi-directional serial data link,” which suggests a common serial architecture where data is serialized, transmitted, and then deserialized. Ex-1004, Abstract, ¶12 (“Serial channel 100 includes a transmitter 110, a transmission channel 120, and a receiver 130.”), ¶1, ¶4 (“High-speed serial data interface ... may include a transmitter and a receiver.”), FIG. 1:



100

FIG. 1

Ex-1003, ¶41.

Berke applies its teachings to standards with SerDes architectures, such as PCIe and SATA. Ex-1004, ¶12. Both included serialization and deserialization, which a POSITA would have understood given their widespread use. *E.g.*, Ex-1010, 000192-000193; Ex-1011, 000621 (“[S]erializer/deserializer (SerDes) circuits make up a typical Serial ATA interface Phy.”); Ex-1008, 000058-61 (listing SATA and PCI Express as “protocol standards for which HSS [High-Speed SerDes] cores are used.”), 000018. Therefore, Berke teaches or suggests a method for SerDes communications. Ex-1003, ¶42.

Likewise, Cornelius teaches PCIe and uses its active cable to provide high-speed serial connections between computers. Ex-1005, 2:65-3:53.

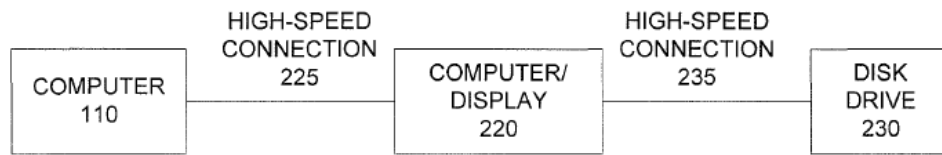
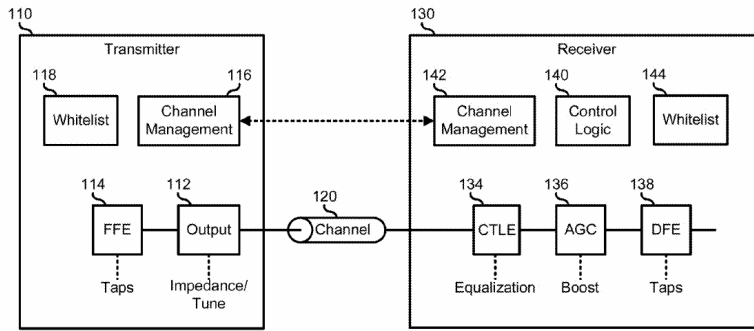


FIGURE 2

This architecture serializes parallel computer data into a narrow, high-speed stream for cable transmission—similar to funneling water into a narrow pipe—and then restores it to its original parallel form through deserialization at the other end. Ex-1003, ¶43. The types of serial communications taught by Berke and Cornelius presume serialization in the transmitter and deserialization in the receiver; a POSITA would have recognized this when reading Berke and Cornelius because that is how serial communications have been used for decades. *Supra* §I. Therefore, a POSITA would have been motivated, and found it obvious, to combine Berke and Cornelius’s teachings by using Berke’s high-speed serial communications in a SerDes context. Ex-1003, ¶44.

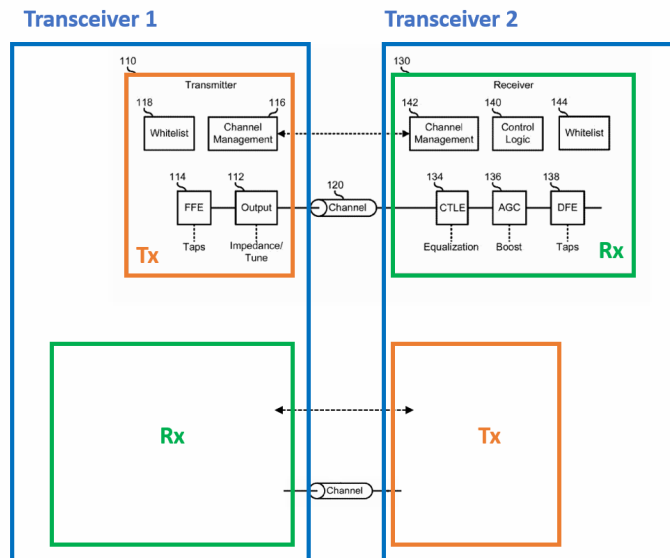
Berke further teaches a **transceiver**. Figure 1 shows a “[s]erial channel 100 includes a transmitter 110, a transmission channel 120, and a receiver 130.”



100

FIG. 1

Ex-1003, ¶45. This represents “one half” of a bi-directional data link, with the “other half” having “a receiver in the first component, and a transmitter in the second component, for communicating data back from the second component to the first component.” Ex-1004, ¶12. Berke thus teaches a transceiver at each end of the communication link, comprising a transmitter and a receiver and coupled to two unidirectional channels, as shown below:



Ex-1004, FIG. 1; Ex-1003, ¶46.

**[1a] selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;**

Berke teaches **pre-equalizer coefficient values**. For example, Berke's transmitter 110 includes "a feed-forward equalization (FFE) module 114," which "operates to proactively provide compensation to a transmitted signal." Ex-1004, ¶¶14-15. Berke's FFE module performs pre-equalization because it is configured on the transmitter side, and it provides compensation to a signal before it is transmitted to the receiver. *Id.* Berke's "transmitter 110 and receiver 130 communicate with each other to optimize and adjust various compensation values within the transmitter and the receiver to compensate for the insertion loss and other signal degradations of transmission channel 120." Ex-1004, ¶13. Here, Berke's compensation values refer to equalization coefficients. Ex-1004, ¶4, ¶¶22-23, ¶30. The compensation values or equalization coefficients include those that configure Berke's FFE. Ex-1004, ¶15 ("The amount of compensation is determined by enabling a number of circuit feed-forward taps."). A POSITA would have understood Berke's equalization coefficients that are used to configure the transmitter's pre-equalization process (e.g., FFE) to be pre-equalizer coefficient values. Ex-1003, ¶47.

Berke teaches **selecting one of multiple registers to specify initial pre-equalizer coefficient values**. The registers comprise two or more of the registers that store pre-equalizer coefficients in the whitelist. Berke teaches that the “[t]ransmitter 110 includes ... an equalization coefficient whitelist 118” that stores “certain equalization coefficient settings or combinations of equalization coefficient settings [that] are known to produce one or more of a particularly robust eye height or eye width.” Ex-1004, ¶14, ¶30, ¶32, FIG. 1; Ex-1003, ¶48.

Berke teaches two options for implementing the whitelists: registers or memory. Ex-1004, ¶30 (teaching “a register or group of registers of transmitter 110 and receiver 130”). Because Berke teaches storing multiple sets of whitelisted coefficient settings (Ex-1004, ¶33) in a group of registers (Ex-1004, ¶30), Berke teaches or suggests using each register to store a set of pre-equalizer coefficients. For example, one whitelist register in the transmitter stores one set of pre-equalizer coefficients for the transmitter. Indeed, Berke teaches using an addressable register design, with each register structured in a certain bit width (e.g., 32 bits or higher)—evident from Berke’s I/O interfaces (e.g., I<sup>2</sup>C and SPI). Ex-1004, ¶36. Given the typical width of multi-bit registers in transceiver circuits, storing a set of three or more FFE tap coefficients per register was a straightforward and efficient design choice that allowed reading/writing Berke’s register in one clock cycle (*see id.*), as compared to more complicated schemes. This use of registers was a long-

standing practice in the field. *See, e.g.*, Ex-1030, 1:10-25, 2:23-51 (“coefficient register 14” supplies coefficients C0-C3), FIG. 1. Furthermore, it simplified control logic, among other benefits. Therefore, a POSITA would have been motivated and found it obvious to apply Berke’s register teachings, as explained above. Ex-1003, ¶¶49-50.

A POSITA would have had a reasonable expectation of success given the simplicity of a register-based approach. Reading/writing to registers was a basic undergraduate skill supported by well-known protocols (e.g., I<sup>2</sup>C and SPI) that allowed specifying preferred bit width and total number of registers. Using multiple registers—each holding a set of coefficients—falls squarely within Berke’s teachings (Ex-1004, ¶¶30-33) and was an obvious implementation detail that would have applied a known technique to a known device ready for improvement to yield predictable results (a register-based whitelist, as Berke teaches). *See* Ex-1004, ¶30; Ex-1003, ¶51.

Berke further teaches selecting one of the multiple registers to specify initial pre-equalizer coefficient values. Berke selects a whitelist set of equalization coefficients from multiple sets by configuring the serial channel with each set of coefficients for training and monitoring the performance of the channel, until a whitelist set of equalization coefficients that satisfies a desired performance level is selected:

[A]fter a first whitelist set of equalization coefficients is utilized for training serial channel 100, control logic module 140 operates to monitor the performance of the serial channel. ... If the performance of serial channel 100 falls below the desired performance level, then control logic module 140 selects a second whitelist set of equalization coefficients...

Ex-1004, ¶33.<sup>2</sup> The pre-equalizer coefficients stored in the whitelist at the transmitter are initial pre-equalizer coefficient values because they are used as the starting point for the training process. Ex-1004, ¶30 (“utiliz[ing] the coefficient settings ... stored in equalization coefficient whitelist[] 116 [sic] ... as a starting point for running the training algorithm.”). Because each set of coefficients is stored in a register (explained above), Berke teaches selecting the register with that set of coefficients. Ex-1003, ¶52.

Berke teaches **each of the multiple registers corresponding to a different channel model**. Berke stores sets of pre-equalizer coefficients known to provide “robust” performance for respective channel characteristics, so that one of them can be selected to use for training. Ex-1004, ¶¶30-33. The whitelist registers contain coefficients used “to compensate for channel loss.” Ex-1004, ¶3, ¶15.

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<sup>2</sup> A POSITA would have understood that different parts of Berke are intended to be implemented together in a flexible manner. Ex-1004, ¶40.

Variations in channel loss arise from differences in channel characteristics—such as design, settings, and environmental conditions—where different channel characteristics correspond to different channel models. Ex-1003, ¶53.

Berke determines pre-equalizer coefficients to include in its whitelist based on different channel characteristics, which “can be determined based upon knowledge gained during the design, development, or manufacturing of serial channel 100.” Ex-1004, ¶30. Such knowledge would have informed one about “variations in circuit design, component manufacture” (Ex-1004, ¶3), such as characteristics of circuit traces, connectors, and cables (e.g., length of a trace) (Ex-1004, ¶12), characteristics such as “insertion loss and other signal degradations” (Ex-1004, ¶13), and channel characteristics such as “impedance ... based upon a design target” (Ex-1004, ¶19). Ex-1003, ¶54. In addition, whitelisted equalization coefficients can also be “determined based upon knowledge gained during normal operation of serial channel” (Ex-1004, ¶31), which would have included settings that were used during operation such as receiver equalization settings (Ex-1004, ¶16, ¶18; *infra* §V.A.4) and environmental conditions such as temperature and noise levels (Ex-1004, ¶21). Ex-1003, ¶55.

Each of the aforementioned channel characteristics impact the channel loss and frequency response characteristics. Ex-1004, ¶3, ¶¶12-13, ¶¶16-21. A set of whitelisted pre-equalizer coefficients added to the whitelist based on knowledge of

channel characteristics (Ex-1004, ¶¶30-31) corresponds to a channel model that represents or assumes the known and relied-upon channel characteristics. Ex-1004, ¶¶12-13, ¶¶16-21; Ex-1003, ¶56. Since Berke teaches or suggests using each of multiple multi-bit registers at the transmitter side to store a set of pre-equalizer coefficients, each of the multiple registers with FFE coefficients in the whitelist correspond to a different channel model. Ex-1003, ¶57.

<b>[1b] updating the initial pre-equalizer coefficient values during a training phase; and</b>
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Berke teaches a training process that updates the pre-equalizer coefficient values, among other compensation values. Ex-1004, ¶13 (“[T]ransmitter 110 and receiver 130 communicate with each other to optimize and adjust various compensation values within the transmitter and the receiver.”). Ex-1003, ¶58.

Berke describes a training phase during which variations of pre-equalizer coefficients of the transmitter (e.g., “equalization setting,” “FFE tap settings”) are run and performance characteristics (e.g., “eye height and eye width,” “BER”) of data transmission are recorded. Ex-1004, ¶20; Ex-1003, ¶59.

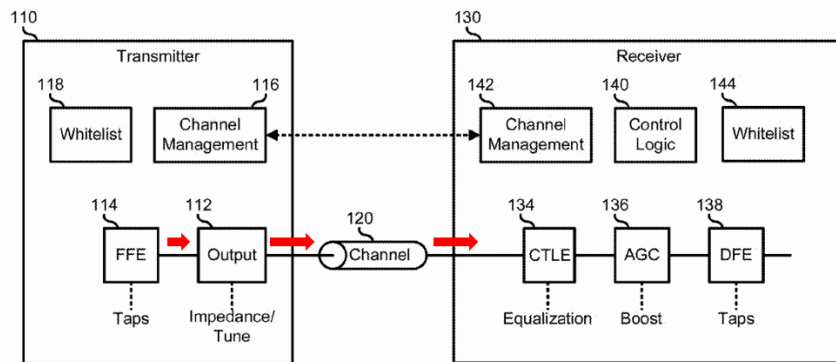
For the training process, Berke teaches using a “best-effort” approach to update pre-equalizer coefficient values. Ex-1004, ¶3; *see also* ¶¶24-29, FIG. 3; Ex-1003, ¶60. To do so, first, Berke “determine[s] if the variability in equalization coefficients derived over different runs of the training algorithm is greater than an

equalization variation threshold.” Ex-1004, ¶24; *see also* ¶¶27-28. If so, a new set of training runs are commenced to pick out a small number of variables in equalization coefficients (which includes pre-equalizer coefficients) to which the performance of serial channel is most sensitive. *Id.*, ¶24; *see also* ¶¶25, 28, FIG. 3 (“318 Determine Sensitive Coefficients,” “320 Tighten Training Range For Sensitive Coefficients”). After the narrowed set of variables (“knobs”/“coefficients”) are determined, Berke “determines a narrowed set of knob settings ... [and] utilizes the narrowed set of knob settings for the selected knobs to converge on a best set of equalization settings.” *Id.*, ¶26, ¶29. The training concludes once it is determined that the variability is not greater than the equalization variation threshold, and “the set of equalization coefficients associated with the best performance of serial channel 100 ... is selected.” *Id.*, ¶24; Ex-1003, ¶61.

As explained above, Berke teaches using the whitelist set of equalization coefficients “as a starting point for running the training algorithm.” Ex-1004, ¶30. Accordingly, the training phase updates the initial pre-equalizer coefficients to a converged set of pre-equalizer coefficients. Ex-1003, ¶62.

**[1c] using the updated pre-equalizer coefficient values to convey a transmit data stream.**

As demonstrated in Figure 1, in the transmitter 110, the FFE module 114 uses the pre-equalizer coefficients to process a serial data stream, outputs the pre-equalized signals to a channel output module 112, which in turn outputs the transmit data stream for transmission on channel 120 to be received by receiver 130. *Id.*, FIG. 1, ¶14.



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**FIG. 1**

Ex-1003, ¶63. After updating the pre-equalizer coefficients, they are used to convey a data stream. Ex-1004, ¶24; Ex-1003, ¶64.

#### 4. Claim 3

**3. The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.**

Berke teaches **different types of receiver equalization**. Berke's receiver 130 includes a "continuous time linear equalization (CTLE) module 134" and a "decision feedback equalization (DFE) module 138," which provide different types of receiver equalization. Ex-1004, ¶16, ¶18. Berke further teaches that each of the CTLE module and the DFE module supports different amounts of equalization, or alternatively, could be turned off. *Id.*, ¶16, ¶18. Accordingly, Berke teaches different types of receiver equalization, corresponding to using CTLE, DFE, or both for receiver equalization. Furthermore, the use of CTLE and/or DFE at different settings and/or taps to provide different amounts of equalization constitutes different types of receiver equalization. Ex-1003, ¶66.

Berke teaches a whitelist with registers that store sets of preequalizer coefficients, each set corresponding to a channel model of channel characteristics such as the receiver equalization. *Supra* §V.A.3[1a]. The type of receiver equalization used impacts the channel performance. Ex-1004, ¶29 ("[C]hanges to the CTLE settings may result in widely varying performance on the serial channel."). For a set of equalization settings for pre-equalization to achieve high performance, they must be suitable for the receiver equalization type. *Supra* §V.A.3[1a]. As Berke's transmitter and receiver communicate to jointly decide

pre-equalization settings on the transmitter side and the equalization settings on the receiver side (Ex-1004, ¶13), Berke teaches or suggests that **at least some of the different channel models**, to which pre-equalizer coefficients correspond, **presume** different types of receiver equalization. Ex-1003, ¶67.

## 5. Claim 4

**4. The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.**

In its process of selecting one set of pre-equalizer coefficients from multiple (*supra* §V.A.3[1a]), Berke explains configuring the channel using each of multiple sets of whitelisted equalization coefficients (e.g., “a first whitelist set of equalization coefficients,” “a second whitelist set of equalization coefficients”) and evaluating its performance level using a “receiver eye diagram” with “eye height and eye width” and/or “a BER of serial channel 100.” Ex-1004, ¶33; *see also* ¶¶13, 20, 24-26, 31. Eye diagram and BER are characteristics commonly used to evaluate equalization performance and thus constitute **performance characteristics** for pre-equalizer coefficient settings. *Supra* §I; *see also* Ex-1008, 000014-000015; Ex-1003, ¶69.

Since the whitelisted equalization coefficients include initial pre-equalizer coefficient values (*supra* §V.A.3[1a]), Berke **uses the initial pre-equalizer coefficient values to determine a performance characteristic**. As Berke teaches

or suggests using different registers to each store a set of pre-equalizer coefficients (*supra* §V.A.3[1a]), the performance characteristics determined using each set of equalization coefficients are determined for the corresponding register. Berke thus teaches using the initial pre-equalizer coefficient values to determine a performance characteristic **for each of multiple registers**. Ex-1003, ¶70.

#### 6. Claim 6

<b>6. The method of claim 4, wherein the performance characteristic is a bit error rate.</b>
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As explained with respect to claim 4, Berke teaches using the bit error rate (BER) as a “performance characteristic.” *Supra* §V.A.5; Ex-1003, ¶71.

#### 7. Claim 7

<b>7. The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.</b>
---

Berke teaches updating the initial pre-equalizer coefficient values from those stored in the selected register of the whitelist to updated pre-equalizer coefficient values during a training phase. *Supra* §V.A.3[1b]. Further, Berke teaches storing the results of the training process in the whitelist. Ex-1004, ¶32 (“[W]hen all of the knobs and settings have been characterized, control logic module 140 determines a whitelist set of equalization coefficients... and stores the whitelist set of equalization coefficients to equalization coefficient whitelists 118 and 144.”). A POSITA would have found it obvious and been motivated to replace the initial pre-

equalizer coefficient values that were used as the starting point of the training process with the updated pre-equalizer coefficient values resulting from the training process, as the latter is known to provide “robust” performance characteristics “during normal operation.” *Id.*, ¶31. An obvious and straightforward way to do this was to update the selected register with the updated pre-equalizer coefficient values. Ex-1003, ¶73.

## 8. Claim 8

**[8pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:**

Cornelius teaches a **chip-to-module communications link** between a host and a module in an active cable, to which a POSITA would have found it obvious and been motivated to apply Berke’s equalization techniques. Cornelius applies serial communications techniques to active cables and teaches a path from a host to either end of a cable that includes a module, which is a chip-to-module communications link. Ex-1005, 11:59-62, 5:33-45, FIGS. 1-2; Ex-1003, ¶74.

Cornelius’s host has a **port connector**, e.g., a “connector on computer 110” (Ex-1005, 3:43-53, 1:15-22, 4:55-65, FIGS. 1-3) that is connected to a **port transceiver**, as evidenced by its pins for transmitting and receiving high-speed signals, such as “[h]igh-speed transmit pins 3 and 5” and “high-speed receive pins

4 and 6.” *Id.*, 4:22-31, FIG. 3. The circuitry that transmits the Tx signals and receives the Rx signals is the transceiver. *Id.*; Ex-1003, ¶75.

Cornelius’s active cable comprises two **pluggable modules** that are “two active plugs 500 and 505, one on each end of cable 507.” Ex-1005, 6:11-20, FIG. 5; *see also* 8:20-26, FIG. 6. Each active plug includes a transceiver (e.g., dual clock and data recovery (CDR) circuits). Ex-1005, 6:11-20, 6:25-29 (“The clock and data recovery circuits ... may include optical receivers and transmitters.”). Cornelius’s CDR circuits perform a range of functions, including clock and data recovery, retiming data, equalization and pre-equalization, and transmitting and receiving data. Ex-1005, 6:11-24, 6:30-42, FIGS. 5-6. The dual CDR circuitry in each plug is a transceiver because it receives a signal and transmits a signal. *Id.*, 6:11-29; Ex-1003, ¶76.

**The port connector**, through its transmit and receive pins, **couples the port transceiver to the pluggable module transceiver**. Ex-1005, 1:15-22, 3:44-53, 6:16-18 (“Specifically, active plug 500 provides high-speed transmission signals on pins 3 and 5 and receives high-speed signals on pins 4 and 6.”), 6:21-24. Therefore, when Cornelius’s active cable is plugged in the port connector on a host (e.g., a computer), it forms **a chip-to-module communications link** interconnecting a chip in the host and a pluggable module. Ex-1003, ¶77.

**Motivation to Combine.** Berke's serial communications teachings apply to a wide variety of channels including circuit traces and cables. Ex-1004, ¶12. Cornelius teaches an active cable with transceivers at each end. Ex-1005, 11:59-62. Cornelius's active cable includes precisely the types of traces/cables that Berke applied its teachings to, including paths over the cable and between transceivers and their nearby host. Ex-1005, 11:59-62. Therefore, a POSITA would have been motivated to apply Berke's teachings to the serial communication paths in Cornelius's active cable because it would have simply used Berke's known serial techniques to improve similar devices (e.g., Cornelius's serial channels) in the same way as taught by Berke. Ex-1003, ¶78.

Active cables were widely known and in commercial use by 2018 to enable faster data rates and longer cable lengths. These would have motivated a POSITA to apply Berke to Cornelius's active cable teachings to further improve performance. *See* Ex-1025; Ex-1026, 000001, 000005, 000008-000009; Ex-1003, ¶79.

Furthermore, Cornelius teaches pre-equalization. Ex-1005, 6:30-57, 7:7-17, 11:45-62. Berke's best-effort link training techniques provided satisfactory equalization configurations in a shorter amount of time. *Supra* §V.A.3[1b]; Ex-1004, ¶3, ¶13; Ex-1003, ¶80.

Berke and Cornelius’s teachings were readily compatible with each other. Both are in the same field. *Supra* §§V.A.1-2. Both apply their teachings to circuit boards and cables, for computers and external devices. *See, e.g.*, Ex-1004, ¶12, ¶37; Ex-1005, FIGS. 1-2. Both references apply their teachings to similar devices and support common standards such as PCIe and USB. Ex-1004, ¶¶12, 34, 37; Ex-1005, 1:15-22, 3:17-23, 4:55-65. A POSITA would have had a reasonable expectation of success because the combination simply applies Berke’s serial communications techniques to Cornelius’s serial links and does not change the principle of operation for either reference. *Supra* §I; Ex-1003, ¶81.

**[8a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and**

As explained with respect to limitation [1a], Berke teaches a “feed-forward equalization (FFE) module 114” that performs pre-equalization in a transceiver based on pre-equalizer coefficient values. *Supra* §V.A.3[1a]. As serial channels transmit data symbols sequentially, the data going through a serial channel is a serial symbol stream. Berke’s FFE module is configured at the transmitter and pre-equalizes a serial symbol stream to be transmitted on the chip-to-module communications link. *Id.* This teaches a transmit filter because a feed-forward equalizer is a type of FIR filter commonly used in serial communications. *See, e.g.*, Ex-1008, 000020 (referring to a three-tap FFE as “the filter” and each tap’s tap

weight value as “a filter coefficient”). Therefore, Berke teaches **one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted**. Ex-1003, ¶82.

Cornelius teaches performing pre-equalization at the transceiver of its pluggable module (e.g., dual CDR circuits). Ex-1005, 6:11-20 (“Each active plug includes dual clock and data recovery circuits.”), 6:30-42 (“[T]he clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits as appropriate.”), 11:45-62. As explained above, a POSITA would have been motivated to apply Berke’s pre-equalization techniques to Cornelius’s system. *Supra* §V.A.8[8pre] (motivation subsection explaining how and why Berke and Cornelius would have been combined). Under this combination, FFE functionalities, as taught by Berke, are implemented in Cornelius’s pluggable module transceiver to pre-equalize a corresponding serial symbol stream being transmitted **to the port transceiver**. Ex-1003, ¶83.

<p><b>[8b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.</b></p>
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As explained above with respect to limitation [1a], Berke teaches multiple registers, each containing a set of initial coefficient values corresponding to a different channel model. *Supra* §V.A.3[1a]. In addition, Berke teaches selecting

one of the multiple registers to specify initial pre-equalizer coefficient values for the FFE module, in which case the selected register is used to set initial coefficient values for the one or more transmit filters. *Supra* §V.A.3[1a], §V.A.8.[8a]; Ex-1003, ¶84.

The combination of Berke and Cornelius further teaches **a controller having the multiple registers and using one of them to set initial coefficient values**. Berke teaches whitelist and channel management functionalities on the transmitter side (e.g., the functionalities of the channel management module and the equalization coefficient whitelist) that control the selection and training of pre-equalizer coefficients. Ex-1004, ¶14, ¶19, ¶33, FIG. 1. The components of Berke's transceiver that implement these functionalities on the transmitter side constitute a controller. Ex-1003, ¶85.

Berke's controller controls the pre-equalizer settings on the transmitter side based on instructions from the receiver side. The control logic module 140, configured on the receiver side, selects a whitelist set of pre-equalizer coefficient values and its corresponding register by determining their corresponding performance characteristics. Ex-1004, ¶33; *supra* §V.A.3[1a]; Ex-1003, ¶86. The control logic module 140 communicates "adaptation instructions" to channel management module 116 that is on the transmitter side. Ex-1004, ¶19. Pre-equalization on the transmitter side is configured based on the adaptation

instructions. Ex-1004, ¶13 (“[T]ransmitter 110 and receiver 130 communicate with each other to optimize and adjust various compensation values within the transmitter and the receiver.”). The adaptation instructions indicate the selected set of whitelist pre-equalizer coefficient values since Berke teaches “the backchannel adaptation mechanism may operate to provide different sets of compensation values.” *Id.*, ¶¶13, 20; *Supra* §V.A.3[1a]. The selected set of whitelist pre-equalizer coefficient values are stored in the equalization coefficient whitelist 118. Ex-1004, ¶30, ¶32; *Supra* §V.A.3[1a]. By causing the selected set of whitelist pre-equalizer coefficient values to be used for the transmitter side based on adaptation instructions, the channel management module 116 performs the controller function of using one of the registers to set initial coefficient values for the one or more transmit filters. Ex-1003, ¶¶87-88.

Furthermore, Cornelius teaches that its active plug includes a “cable microcontroller” that is “used to configure clock and data recovery circuits,” which include pre-equalization. Ex-1005, 6:11-42. When combined with Berke (*Supra* §V.A.8[8pre]), it would have been obvious for the microcontroller to include the registers taught by Berke and perform the Berke’s teachings for selecting and using those registers. Ex-1003, ¶89.

## 9. Claim 10

The limitations of claim 10 appear in claim 3 and are satisfied for the same reasons. *Supra* §V.A.4; Ex-1003, ¶90.

## 10. Claim 11

Limitations [11pre]-[11a] are identical to [8pre]-[8a] and satisfied for the same reasons. *Supra* §§V.A.8[8pre]-[8b]; Ex-1003, ¶91.

**[11b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic, the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.**

The combination of Berke and Cornelius teaches a controller having multiple registers, each containing a set of initial coefficient values, the controller using one of the registers to specify the initial coefficient values for the one or more transmit filters. *Supra* §V.A.8[8b]; Ex-1003, ¶92. Berke teaches a controller on the transmitter side controlling the pre-equalizer settings based on adaptation instructions from the control logic module 140, configured on the receiver side. *Supra* §V.A.8[8b]; Ex-1004, ¶13, ¶¶19-20. The control logic module 140 selects a whitelist set of pre-equalizer coefficient values and its corresponding register by determining their corresponding performance characteristics. *Supra* §V.A.3[1a], §V.A.5, §V.A.8[8b]; Ex-1004, ¶33; Ex-1003, ¶¶93-94.

The channel management module 116 is part of the transceiver that teaches the pluggable module transceiver. *Supra* §V.A.8[8b]. It follows that the control logic module 140, being on the receiver side, is part of the transceiver that teaches the **port transceiver**. *Supra* §V.A.8[8pre]. The combination thus teaches **the port transceiver** determines a performance characteristic and the controller using one of the registers **selected by the port transceiver** to specify the initial coefficient values. Ex-1003, ¶95.

### 11. Claim 13

The limitations of claim 13 appear in claim 6 and are satisfied for the same reasons *Supra* §V.A.6; Ex-1003, ¶96.

### 12. Claim 14

**14. The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.**

Berke teaches a training process that updates the pre-equalizer coefficient values. *Supra* §V.A.3[1b]. A pre-equalizer is a transmit filter. *Supra* §V.A.8[8a]; Ex-1003, ¶98.

The control logic module 140 conducts the training process that generates the updates. Ex-1004, ¶20 (“control logic module 140 trains transmitter 110”), ¶24. Because the control logic module 140 is part of the transceiver that teaches the port transceiver (*supra* §V.A.10[11b]), the combination teaches that the port transceiver

generates updates for the coefficient values of the one or more transmit filters. Ex-1003, ¶99.

### 13. Claim 15

**15. The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.**

Berke's control logic module 140 conducts the training process that generates updated coefficient values (*supra* §V.A.12) and communicates adaptation instructions to channel management module 116 for effectuation on the transmitter side (Ex-1004, ¶19; *supra* §V.A.8[8b]). The "adaptation instructions" include updated pre-equalizer coefficient values since "the backchannel adaptation mechanism may operate to provide different sets of compensation values." Ex-1004, ¶¶13, 20; Ex-1003, ¶101.

As explained above, Berke teaches updating the selected register with the updated pre-equalizer coefficient values. *Supra* §V.A.7. Berke further teaches that the "control logic module 140 ... stores the whitelist set of equalization coefficients to equalization coefficient whitelists 118 and 144." Ex-1004, ¶32. A POSITA would have understood that the storing is done through the channel management module 116 on the transmitter side, which is part of the controller (*supra* §V.A.8[8b]) and causes updated pre-equalizer coefficient values to be stored in the equalization coefficient whitelist 118 based on adaptation instructions. Ex-1003, ¶102.

#### **14. Claims 16, 17, 19**

The limitations of claims 16, 17, and 19 appear in claim 8, limitation 11[b], and claim 6, respectively, and are satisfied for the same reasons. *Supra* §§V.A.8[8pre]-[8b], §V.A.10[11b], §V.A.6; Ex-1003, ¶¶103-105.

#### **B. Ground 2**

Ground 2 applies Berke's techniques for selecting and updating pre-equalizer coefficient values to Ran's serial communications channel between a network interface controller and a pluggable optical module. *Infra* §V.B.8[8pre]; Ex-1003, ¶106.

#### **1. Ran (Ex-1006)**

Ran is prior art to the '111 patent under post-AIA §102(a)(2); it was filed April 30, 2019, and claims priority to a provisional application filed August 24, 2018 (Ex-1007), which provides clear and unambiguous support for Ran's teachings relied upon in this Petition. Ex-1003, ¶¶108-109.

Ran teaches "adaptation of a transmit equalizer using management registers" (Ex-1006, Title), including "[s]election of equalization coefficients to configure a communications link" and "[c]ontinuous modification of the selected equalization coefficients" are performed. Ex-1006, Abstract. Ran implements its serial communications link between a host and pluggable optical module. Ex-1006, 1:23-33, 4:5-30, FIGS. 1, 2A-2B; Ex-1003, ¶¶110-111.

Ran is analogous art because it is in the same field. *Compare supra* §III with Ex-1006, 1:34-41. Ran is also reasonably pertinent; it relates to ensuring reliable data transmission through a communications channel. Ex-1006, Abstract, 1:23-41; Ex-1003, ¶112.

## 2. Claims 1, 3, 4, 6, and 7

Ground 2 teaches claims 1, 3, 4, and 6-7 based on the teachings of Berke for the same reasons previously explained for Ground 1. *Supra* §§V.A.3-7. Ran additionally teaches SerDes communications as explained below. *Infra* §V.D.2[1pre]. A POSITA would have found it obvious to combine Berke and Ran's teachings and use Berke's high-speed serial communications in a SerDes context. Ex-1003, ¶113.

## 3. Claim 8

**[8pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:**

Ran teaches a **chip-to-module communications link** between a chip and an optical module, to which a POSITA would have found it obvious and been motivated to apply Berke's equalization techniques. Berke teaches implementing its communications link with "a NIC disposed within information handling system 400." Ex-1004, ¶¶35, 39; Ex-1003, ¶114.

Ran teaches an “optical module” being connected to “a chip” via a “serial link,” forming a “chip-to-module interconnection[.]” Ex-1006, 1:23-33; 5:4-14, FIGS. 1, 2A:

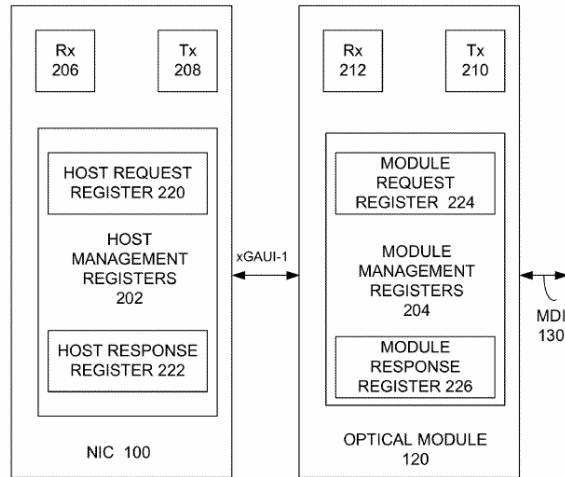


FIG. 2A

Ex-1003, ¶115.

Ran teaches a **port connector** on a host device, such as an “Ethernet port” on the “network interface controller” (NIC). Ex-1006, 4:5-13, FIGS. 1, 2A, 2B.

The port connector is connected to a **port transceiver**. Ex-1006, 5:26-33, 8:1-10 (“Host 250 can include transceiver 252 for communication with module 232.”); FIGS. 2A-B; Ex-1003, ¶116.

Ran teaches a **pluggable module transceiver** that is configured on the module. Ex-1006, 1:23-33 (“An optical module is a hot-pluggable optical

transceiver.”), 5:26-33 (“The optical module 120 also includes a module receiver 212 and module transmitter 210.”),<sup>3</sup> FIGS. 2A, 2B; Ex-1003, ¶117.

Ran’s Ethernet port acts as a port connector that couples the host device with the optical module. Ex-1006, 4:23-30 (“The network interface controller 50 is communicatively coupled via an ... electrical connection to an optical module 70.”), 5:4-14, FIG. 1. As the connector facilitates transmitting and receiving data, it couples the port transceiver to the pluggable module transceiver. *See, e.g.*, Ex-1006, 5:26-33, 7:36-59, 7:60-67, FIGS. 2A-2B. Ex-1003, ¶118.

**Motivation to Combine.** Berke’s serial communications techniques apply to a wide variety of channels including circuit traces, connectors, and/or cables. Ex-1004, ¶12. Ran teaches a chip-to-module link that couples a host device with an optical module. Ex-1006, 1:23-33; 4:23-30, 5:4-14. Ran uses the traces, connectors, and cables that Berke teaches. Therefore, a POSITA would have been motivated to apply Berke’s teachings to Ran’s serial link because it would have simply used Berke’s known serial techniques to improve similar devices (e.g., Ran’s serial link) in the same way as taught by Berke. Ex-1003, ¶119. This is the case especially because the references apply their teachings to similar devices. Ex-

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<sup>3</sup> Ran illustrates a transceiver as a transmitter and a receiver in the same device. Ex-1006, FIG. 2A, 1:23-33.

1004, ¶¶38-39; Ex-1006, 1:23-33, 4:5-13, 5:26-33, FIGS. 1 and 2A-2B; Ex-1003, ¶120.

Ran’s configuration, coupling a host device and an external module via an Ethernet port connector, was well-known before 2018. A POSITA would have understood Berke’s network interface to contemplate configurations connecting a NIC with an external pluggable optical module, as taught by Ran, given the prevalence of such modules in enterprise and data center applications. Ex-1003, ¶121.

Berke’s technique of configuring pre-equalization coefficient values (Ex-1004, ¶13) was readily applicable to Ran to solve a problem recognized by Ran—the increase in data rate necessitating optimized equalization settings. Ex-1006, 2:26-39; *see also* Ex-1006, 1:34-41; *infra* §§V.B.3[8a]-[8b]. Berke’s technique obtained satisfactory equalization configurations in a shorter amount of time. Ex-1004, ¶3. Berke’s approach would have been a good fit for Ran’s applications that “handle varying operating conditions such as temperature and humidity.” Ex-1006, Abstract; Ex-1003, ¶122.

Berke and Ran’s teachings were readily compatible. Ran and Berke are in the same field. *Supra* §§V.A.1, V.B.1. Both apply their teachings to circuit boards and cables, for computers and external devices. *See, e.g.*, Ex-1004, ¶12, ¶37; Ex-1006, 1:23-33, 4:23-30, 5:4-14, 5:33-45, FIGS. 1, 2A-2B. Berke and Ran both

contemplated connections according to common standards (PCIe, SATA, Ethernet). Ex-1004, ¶12, ¶39; Ex-1006, 13:31-40, 14:59-67, 5:4-14, FIGS. 1, 2A, 2B. A POSITA would have had a reasonable expectation of success because it would have been a straight-forward combination that simply applies Berke's serial communications techniques to Ran's serial link and would not have changed the principle of operation for either reference. *Supra* §I; Ex-1003, ¶123.

**[8a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and**

Berke teaches **one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted.** *Supra* §V.A.8[8a]. Ran teaches performing equalization on the chip-to-module communication link. *See, e.g.,* Ex-1006, 3:14-28. Under the combination of Berke and Ran (*supra* §V.B.3[8pre]), FFE functionalities, as taught by Berke, are implemented in Ran's pluggable module transceiver to pre-equalize a corresponding serial symbol stream being transmitted **to the port transceiver.** Ex-1003, ¶124.

**[8b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.**

Berke teaches this limitation. *Supra* §V.A.8[8b]. Furthermore, Ran teaches or suggests a management entity implemented on the optical module to configure pre-equalization settings for transmission from the optical module to the host. *Infra*

§V.D.2[1a], §V.D.9[8b]; Ex-1006, 5:4-25, 5:39-61, 6:52-62, 9:45-59, 11:65-12:31, 13:24-30, Abstract, FIGS. 2A, 3, 6. When combined with Berke (*supra* §V.B.3[8pre]), the management entity would obviously have included the registers taught by Berke and performed Berke's teachings for selecting and using those registers to configure the pre-equalization settings. Ex-1003, ¶125.

#### 4. Claim 10

The limitations of claim 10 appear in claim 3 and are satisfied for the same reasons. *Supra* §V.A.4; Ex-1003, ¶126.

#### 5. Claim 11

Limitations [11pre]-[11a] are identical to [8pre]-[8a] and satisfied for the same reason explained for [8pre]-[8a]. *Supra* §§V.B.3[8pre]-[8a]; Ex-1003, ¶127.

<p><b>[11b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic, the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.</b></p>
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The combination of Berke and Ran teaches a controller having multiple registers, each containing a set of initial coefficient values, the controller using one of the registers to specify the initial coefficient values for the one or more transmit filters. *Supra* §V.B.3[8b]. Berke's control logic module 140, configured on the receiver side, **determines a performance characteristic** for each set of initial coefficient values contained in the multiple registers to select a set of initial pre-

equalizer values for training. *Supra* §§V.A.5, V.A.10[11b]; Ex-1004, ¶33; Ex-1003, ¶128. The control logic module 140 communicates “adaptation instructions” to channel management module 116, which is on the transmitter side to update the pre-equalizer coefficients. *Supra* §V.B.3[8b], §V.A.8[8b]. The channel management module 116 is part of the transceiver that teaches the pluggable module transceiver. *Supra* §V.A.8[8b], §V.A.8[8b]. It follows that the control logic module 140, being on the receiver side, is part of the transceiver that teaches the **port transceiver**. *Supra* §V.B.8[8pre]. The combination thus teaches **the port transceiver** determines a performance characteristic and the controller using one of the registers **selected by the port transceiver** to specify the initial coefficient values. Ex-1003, ¶129.

## 6. Claims 13-15

Ground 2 teaches claims 13-15 based on Berke’s teachings as previously explained for Ground 1; that analysis applies here. *Supra* §§V.A.11-13; Ex-1003, ¶130.

## 7. Claims 16, 17, 19

The limitations of claims 16, 17, and 19 appear in claim 8, limitation [11b], and claim 13, respectively, and are satisfied for the same reasons. *Supra* §§V.B.3[8pre]-[8b], §V.B.5[11b], §V.B.6; Ex-1003, ¶¶131-132.

### **C. Grounds 3 and 4**

Claims 2, 5, 9, 12, and 18 recite basic concepts such as insertion loss/package loss and error signal energy. Stauffer, a textbook, teaches these concepts. *Infra* §§V.C.2-3; Ex-1003, ¶133.

#### **1. Stauffer (Ex-1008)**

Stauffer was published in 2009 and is post-AIA §102(a)(1) prior art. Ex-1013; Ex-1014; Ex-1015; Ex-1016. Stauffer is a textbook on “High Speed Serdes (HSS) Devices and Applications.” Ex-1008, 000001. Stauffer teaches uses for equalization, including that “[t]he equalization scheme used by Serdes devices must compensate for the channel loss and other impairments in order to achieve the desired BER.” Ex-1008, 000020-000021, 000029; Ex-1003, ¶¶135-136.

Stauffer is analogous art because it is in the same field of serial communications. *Compare supra* §III with Ex-1008, 000011. Stauffer is also reasonably pertinent; it relates to ensuring reliable data transmission through a communication channel by discussing signal integrity issues and solutions. Ex-1008, 000029-000033; Ex-1003, ¶137.

## 2. Claim 2

2. **The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.**

Berke teaches storing sets of pre-equalizer coefficients, respectively corresponding to different channel models, in registers of a whitelist. *Supra* §V.A.3[1a]. Ground 1 and Ground 2 each teaches applying Berke’s techniques to a chip-to-module (C2M) communications link. *Supra* §§V.A.8[8pre], V.B.3[8pre]. Thus, it would have been obvious for **at least some of the different channel models** to be directed to **chip-to-module (C2M) channels**. Ex-1003, ¶139.

In Berke, for a set of pre-equalizer coefficients to be added to the whitelist, they must yield robust performance for a set of channel characteristics of a channel model. *Supra* §V.A.3[1a]; Ex-1004, ¶30, ¶32, ¶15. Berke teaches that “insertion loss and other signal degradations” are among the characteristics that have an impact on the performance and can be considered as part of a channel model. Ex-1004, ¶13; *supra* §V.A.3[1a]. It would have been obvious for Berke’s “other signal degradations” to include package loss, as package loss can be determined based on “knowledge gained during the design, development, or manufacturing of serial channel.” Ex-1004, ¶30; Ex-1003, ¶140.

To the extent Berke does not literally mention “package loss,” Stauffer expressly teaches package loss as a cause of signal degradation that should be

considered in configuring equalization coefficients. In discussing “signal integrity analysis” (Ex-1008, 000029-000031), Stauffer explains “signal degradation due to the package” is a challenge to signal integrity and that package loss can be determined based on information from the manufacturer. Ex-1008, 000031; Ex-1003, ¶141. In light of Stauffer, a POSITA would have understood Berke’s “other signal degradations” to include signal degradation caused by package loss and Berke’s “knowledge gained during the design, development, or manufacturing of serial channel” to include manufacturer package models for determining package loss. Thus, Grounds 3 and 4 each renders obvious that at least some of the different channel models are for chip-to-module (C2M) channels **with different insertion loss and package loss characteristics**. Ex-1003, ¶142.

**Motivation to Combine.** Stauffer teaches that package loss causes signal degradation, separate from channel insertion loss. Ex-1008, 000031, 000029. Berke provides express motivation to apply Stauffer’s teachings—aimed at package loss—because Berke aims “to compensate for ... signal degradations of transmission channel.” Ex-1004, ¶13. That is the reason why Berke uses whitelisted coefficients to begin with. *Supra* §V.A.3[1a]; Ex-1004, ¶30. For high-speed scenarios where robust performance is needed (*id.*), a POSITA would have been motivated to maximize signal quality. While a POSITA might also address other factors, that would not preclude them from specifically addressing package

loss—known source of signal degradation. Therefore, a POSITA would have found it obvious and been motivated to select sets of pre-equalizer coefficients to address the package loss characteristics that Stauffer teaches, as part of the channel model. *See* Ex-1008, 000031; Ex-1003, ¶143.

A POSITA would have had a reasonable expectation of success because methods for measuring and addressing package loss were readily known; Berke teaches configuring equalization to address signal degradations. Ex-1004, ¶13. Berke and Stauffer are compatible because they are in the same field and teach serial communications using common standards (PCIe and SATA). Ex-1004, ¶¶12, 37; Ex-1008, 000058, 000061. The combination would not have changed the principle of operation of any reference. Ex-1003, ¶¶144-145.

### 3. Claim 5

<p><b>5. The method of claim 4, wherein the performance characteristic is an error signal energy.</b></p>
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As explained above, Berke teaches using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers. *Supra* §V.A.5. Berke does not limit what performance characteristic to determine. Ex-1004, ¶33; Ex-1003, ¶147.

Stauffer teaches various methods for determining metrics of channel performance, including calculation of the “root-mean-square value” (RMS). Ex-1008, 000031-32. The well-known RMS was calculated by taking the square root

of the mean square error (MSE)—the mean of the squares of error signals. The mean square error was a well-known measure of the error signal energy. Ex-1027, 000002. By teaching assessing channel performance based on RMS, Stauffer teaches or suggests using the error signal energy, as measured by MSE, as a performance characteristic. Ex-1003, ¶148.

A POSITA would have found it obvious to apply Stauffer's teachings to Berke and use error signal energy as measured by MSE as one of the metrics of channel performance. This would have been obvious because the same signal data used to generate Berke's eye diagram and BER (e.g., received signal and expected signal) would have been available for calculating the error signal energy. *See generally* Ex-1024, cls.1-2, FIGS. 6A-6B, ¶17, FIG. 7; Ex-1004, ¶20, ¶22, ¶¶24-30. The error signal energy simply involves applying the MSE calculation to the difference between the received and expected signals. This was well-known and commonly applied to error signals in the context of equalizer adaptation in characterizing channel performance as taught in textbooks. *See, e.g.,* Ex-1022, 000033. Accordingly, no additional data collection or measurement would have been required to determine error signal energy, and its calculation would have been known and obvious to a POSITA. Ex-1003, ¶149.

A POSITA would have been motivated, with a reasonable expectation of success, to determine the error signal energy as an indicator of channel

performance on top of those enumerated by Berke. The consideration of MSE metrics would have been consistent with Berke's teaching of evaluating channel performance based on the height of eye diagram opening. Ex-1004, ¶22. A POSITA would have recognized that the MSE of the error signal quantifies vertical eye closure. Given that Berke already teaches using the eye diagram as performance characteristics, it would have been an obvious and natural extension to quantify that performance by computing the MSE of the underlying error signals. *See generally* Ex-1028, cl.19; Ex-1029, 7:35-62, Table 1. A POSITA would have been motivated to incorporate this additional performance characteristic to advance Berke's interest in using the training method to find coefficient settings that are "more robust." *See, e.g.*, Ex-1004, ¶31; Ex-1003, ¶150.

#### **4. Claims 9, 12, 18**

The limitations of claims 9, 12, and 18 appear in claims 2, 5, and 5, respectively, and are satisfied for the same reasons. *Supra* §V.C.2, §V.C.3; Ex-1003, ¶¶151-153.

#### **D. Ground 5**

Ground 5 combines teachings from Ran, Mejia, and Stauffer. Ran teaches techniques for selecting among presets of equalization settings and updating the settings in the context of serial communications between a network interface controller and a pluggable optical module; Mejia teaches a preset search process

for selecting a preset that is suitable for a channel; Stauffer teaches storing equalization coefficients in registers, among other teachings. *Infra* §§V.D.2[1a], V.D.3, V.D.4; Ex-1003, ¶154.

### 1. Mejia (Ex-1009)

Mejia is post-AIA §§102(a)(1)-(2) prior art; it was filed February 2013, and published August 2014. Mejia “utiliz[es] preset evaluation to improve input/output performance in high-speed serial interconnects” by “select[ing] the best equalization preset for the given system.” Ex-1009, ¶1, ¶10. Mejia selects a preset that best fits the characteristics of a channel. Ex-1009, ¶12, ¶¶29-32; Ex-1003, ¶¶156-157.

Mejia is analogous art because it is in the same field. *Compare supra* §III with Ex-1009, Abstract, ¶¶1-2, ¶¶10-14. Mejia is also reasonably pertinent because it relates to ensuring reliable data transmission through a communication channel. Ex-1009, ¶2; Ex-1003, ¶158.

### 2. Claim 1

**[1pre]. A SerDes communications method that comprises, in a transceiver:**

To the extent the preamble is limiting, Ran discloses a **SerDes communications method**. Ran is directed to “[s]erial communication between a transmitter and a receiver at very high data rates.” Ex-1006, 1:34-41, 4:23-30. Ran teaches “a high data rate serial link (referred to as xGAUI-n ...)” connecting an

“optical module” on a cable to an Ethernet port on a network interface controller (NIC). Ex-1006, 1:23-33, FIG. 2A:

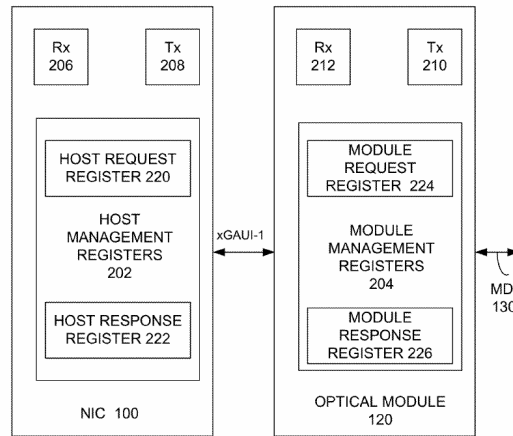


FIG. 2A

Ex-1003, ¶159.

As was well-known to a POSITA, xGAUI-n interfaces transmit high-speed serial data over multiple electrical lanes. Each electrical lane typically implements a SerDes to convert wide parallel data links (inside the chip) into serial symbol streams for transmission over the lane (i.e., serialization), and to perform the inverse operation on the receiving end (i.e., deserialization). Furthermore, Ran applies its teachings to standards with SerDes architectures, such as PCIe and SATA. Ex-1006, 13:31-40, 14:59-67. The PCIe and SATA standards include serialization and deserialization. *Supra* §V.A.3[1pre]; Ex-1010, 000192-000193; Ex-1011, 000621; Ex-1008, 000058-61; Ex-1003, ¶160. Because Ran provides

teachings for common SerDes architectures, Ran teaches a method for SerDes communications. Ex-1003, ¶160.

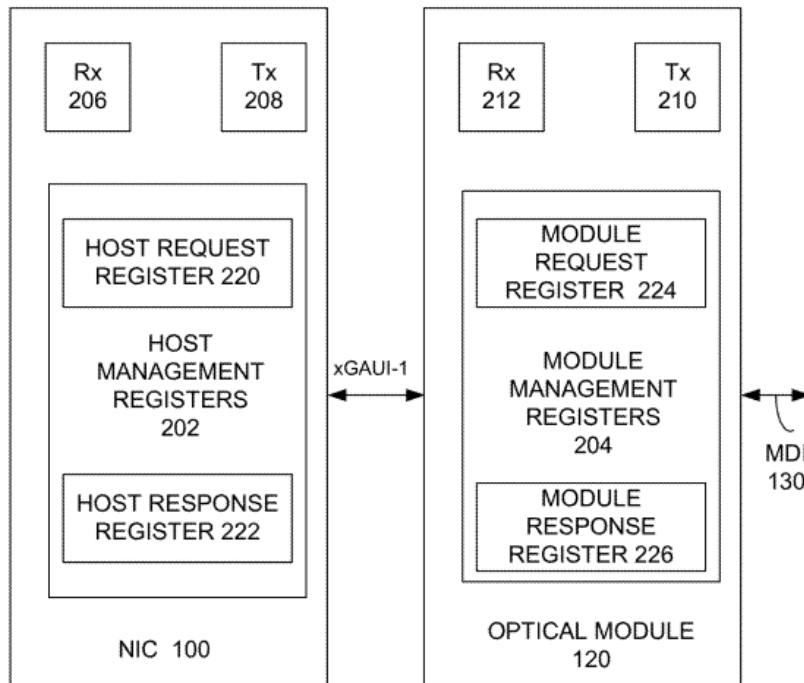
Ran further teaches a **transceiver** configured on the optical module or the NIC. Ex-1006, 1:23-33 (“An optical module is a hot-pluggable optical transceiver.”), 5:26-33 (“The optical module 120 also includes a module receiver 212 and module transmitter 210.”), 5:26-33 (“The network interface controller 100 also includes a host receiver 206 and a host transmitter 208.”), FIGS. 2A-B; Ex-1003, ¶161.

<p><b>[1a] selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;</b></p>
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Ran teaches performing pre-equalization in a transceiver based on pre-equalizer coefficient values. Ran teaches a pre-equalizer that is “a transmitter FFE of any length and step size” which has “settings” that could be adjusted “using requests from a receiver.” Ex-1006, 3:14-28, 1:34-41. These adjustable “settings” include equalization coefficients of the transmitter FFE, which are pre-equalizer coefficient values. Ex-1006, 3:14-28. Ran adjusts the equalization coefficients for the transmitter side based on “requests” from the receiver side. Ex-1006, 3:14-28; Ex-1003, ¶162.

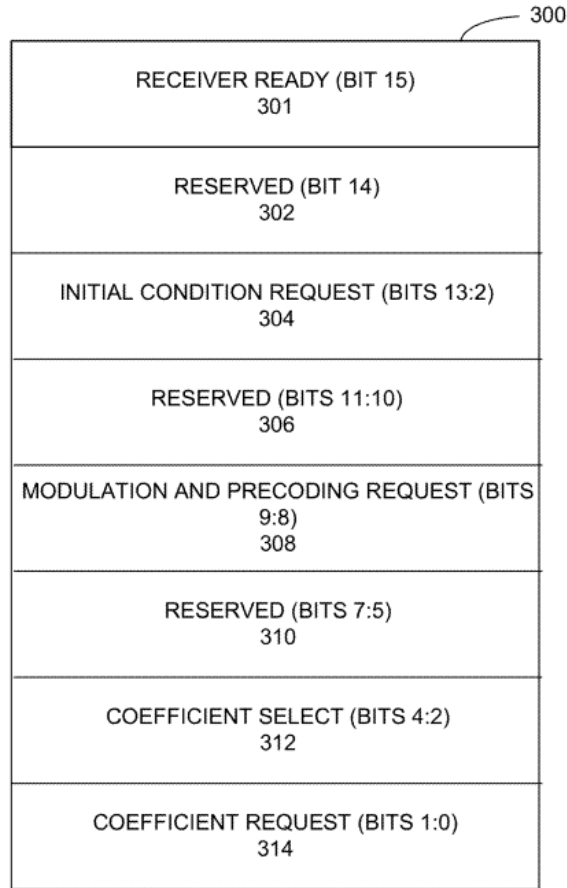
Ran teaches using a register to **specify initial pre-equalizer coefficient values** that are selected from multiple sets of pre-equalizer coefficient values,

called “presets.” Ex-1006, 10:6-14, FIG. 3. Ran teaches “management registers,” configured on the transceiver on both sides of the serial link, for controlling selection of a preset. Ex-1006, 5:4-14, 5:15-25, FIG. 2A:



**FIG. 2A**

The management registers on each side include a “request register” and a “response register.” Ex-1006, 5:15-25. The request registers have a control field structure illustrated in Figure 3A. Ex-1006, 9:45-59, FIG. 3A:



**FIG. 3A**

Ex-1003, ¶163.

Ran teaches selecting preset values for the transmitter FFE by setting the module request register’s two-bit “initial condition request field 304” “to select one of three predefined transmitter equalizer configurations (‘presets’).” Ex-1006, 10:6-14, Figure 3B (illustrating bits 12 and 13 are set differently to select one of Preset1-Preset3 for transmitter equalizer configurations.):

Bit 13	Bit 12	Description
1	1	Preset3
1	0	Preset2
0	1	Preset1
0	0	Co-efficient Control

**FIG. 3B**

A predefined transmitter equalizer configuration includes settings for coefficients of the pre-equalizer. Because these coefficients are specified as an “initial condition,” they are used as **initial pre-equalizer coefficient values**. By setting the two bits in the initial condition request field of the request register, the initial pre-equalizer coefficient values are specified by **selecting** from Preset1, Preset2, and Preset3. Ex-1003, ¶164.

Mejia teaches a “preset search” technique for **selecting** the initial pre-equalizer coefficient values from multiple sets of initial pre-equalizer coefficient values. Ex-1009, ¶10; Ex-1003, ¶165.

Mejia is directed to “utiliz[ing] preset evaluation to improve input/output (I/O or IO) performance in high-speed serial interconnects such as PCIe.” Ex-1009, ¶10, ¶1, ¶12. A preset is used as the starting point of the equalization training process where initial equalization coefficients are refined into final coefficients for use in transmitting data. Ex-1009, ¶12, ¶13 (“A preset generally refers to starting setting(s) (which may be later refined into final settings).”). Here, the equalization

settings for the transmitter include pre-equalizer coefficient values. Ex-1009, ¶11; Ex-1003, ¶166.

Mejia teaches selecting or specifying a set of pre-equalizer coefficients from among multiple sets. Mejia's preset search technique is "provided to evaluate the system performance at different recommended equalization preset values and select the best equalization preset for the given system." Ex-1009, ¶¶31, 10. Performance is evaluated based on "margin(s)" and "gain, jitter and equalization controls." Ex-1009, ¶10. Preset search also evaluates the presets for their bit error ratio ("BER"). Ex-1009, ¶32, ¶12; Ex-1003, ¶167.

Mejia's different equalization presets **correspond to different channel models**. Mejia's different presets contain pre-equalizer coefficient values that are defined to compensate for "signal distortion" of a communication channel. Ex-1009, ¶2, ¶12. Different presets are designed to be suitable for the communication channels of different systems. Ex-1009, ¶10, ¶31. As a POSITA would have understood, variations in channel loss or signal distortion arise from differences in channel characteristics—such as design, settings, and environmental conditions—where different channel characteristics correspond to different channel models. Ex-1003, ¶168.

Pre-equalizer coefficients of Mejia's different presets correspond to and deliver high performance for different channel characteristics that impact channel

loss, including channel characteristics related to the design (e.g., channel topology, material) and settings (e.g., channel configurations) of the systems. Ex-1009, ¶32 (“[T]he flow ensures that the system is going to be adjusted to use the best preset on any topology/configuration ... some board manufactures may use different type materials... Preset search flow will guarantee target BER by selecting the best preset on those boards.”). The channel characteristics further include the channel length and insertion loss, which also impacts channel loss. Ex-1009, ¶36 (“optimal preset that maximizes electrical margins may be a function of channel insertion loss” for “shortest channels,” “medium channel,” and “long channel”). In addition, Mejia further teaches recommending presets that provide high performance based on “equalization controls” from the receive circuits, which a POSITA would have understood to include the type and configurations of equalization on the receiver side. Ex-1009, ¶10.

Each of the aforementioned channel characteristics impact the channel loss/distortion and frequency response characteristics. Ex-1009, ¶¶31-32, ¶36. As Mejia’s pre-equalizer coefficients for each preset provide high performance for certain channel characteristics (Ex-1009, ¶¶31-32, ¶36), this preset corresponds to a channel model that represents or assumes the channel characteristics. Accordingly, Mejia teaches selecting from different presets corresponding to different channel models. Ex-1003, ¶170.

**Motivation to Combine.** Ran teaches selecting one preset from multiple presets but does not limit how the selection is performed. Ex-1006, 10:6-14. FIG. 3B. Mejia teaches a preset search technique that enables identifying a preset that is suitable for the characteristics of a communication channel, which precisely provides a way of implementing Ran's functionality. Ex-1009, ¶10, ¶31. A POSITA would have found it obvious and been motivated to apply Mejia's preset search technique to implement Ran's selection of a preset, because it simply applies a known technique (e.g., the preset search technique) to a known method/system ready for improvement (e.g., Ran's equalization training method/serial channel) in the same way to obtain a predictable result (e.g., selecting a preset set of pre-equalizer coefficient values with optimum performance). Ex-1003, ¶171.

Mejia's preset search allows identifying and selecting pre-equalizer coefficients that best fit the characteristics of a channel and provide optimum performance. Ex-1009, ¶10, ¶¶31-32, ¶36. A POSITA thus would have been motivated to apply Mejia's preset search teachings to Ran to bring about the benefits. Ex-1003, ¶172.

Both Ran and Mejia recognize variabilities in the channel, e.g., from manufacturing, configurations, and environmental conditions. Ex-1006, 2:26-39, 15:45-50, Abstract; Ex-1009, ¶32, ¶36. Having presets corresponding to different

sets of characteristics or channel models would have provided sets of initial pre-equalizer coefficients suitable for different channels, which a POSITA would have recognized to be beneficial. Mejia's preset search technique directly evaluates performance characteristics of pre-equalizer coefficients, providing an effective way to select from multiple sets, as Ran teaches. *See, e.g.*, Ex-1009, ¶¶31-32; Ex-1003, ¶¶173-174.

Additionally, Ran and Mejia's teachings were readily compatible; they are in the same field of serial communications (*supra* §§V.B.1, V.D.1) and both support serial communications for PCIe (Ex-1006, 13:31-40; Ex-1009, ¶10). Both select a preset to provide initial pre-equalizer coefficient values for equalization training. *See, e.g.*, Ex-1006, 10:6-14, FIG. 3B; Ex-1009, ¶¶12-14. A POSITA would have a reasonable expectation of success because it would not have changed the principle of operation of either reference. Ex-1003, ¶175.

Ran uses a value stored in register to select initial pre-equalizer coefficient values; Ran does not limit how the coefficient values themselves are stored. By 2018, there were a finite number of options: e.g., registers and memories. Ex-1004, ¶30. A POSITA would have had good reason to use registers, given that Ran's NIC and optical module were already configured with registers (Ex-1006, 5:4-25), making additional registers for storing equalization coefficients simple and obvious to implement. Furthermore, loading equalization coefficients into registers would

have taken advantage of faster access times. When each register stores a set of pre-equalizer coefficients, a set of coefficients can be accessed in a single clock cycle, as explained for Ground 1; that analysis applies here. *Supra* §V.A.3[1a]. Storing a set of three or more FFE tap coefficients per register was a straightforward and efficient design choice that would have been readily apparent to a POSITA with experience in serial communications, given well-known protocols such as I<sup>2</sup>C and SPI.<sup>4</sup> *Supra* §V.A.3[1a]. This was a long-standing practice the prior art provides express motivation to use. Ex-1030, 1:10-25, 2:23-51. This design was particularly suitable for Ran, which uses a two-bit “initial condition request field 304” “to select one of three predefined transmitter equalizer configurations (‘presets’).” Ex-1006, 10:6-14. When each register stores a set of equalizer configurations corresponding to one preset, selection merely required correlating values of two bits to different register addresses. This use of registers falls squarely within Ran’s teachings and also represents an obvious implementation of Ran’s teachings. Ex-1003, ¶176.

Here, the register for a certain preset corresponds to the channel model of that preset. By selecting one of the presets whose coefficients are stored in a

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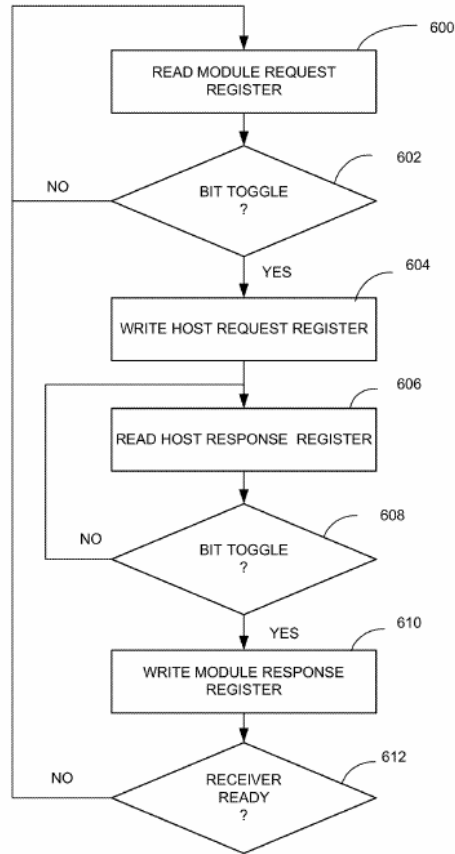
<sup>4</sup> Ran contemplates implementing these known protocols. Ex-1006, 8:43-50, 19:64-67, 20:59-62.

register, Ran teaches renders **selecting one of multiple registers** to specify initial pre-equalizer coefficient values, **each of the multiple registers** corresponding to a different channel model. Ex-1003, ¶176.

To the extent Ran does not expressly teach storing pre-equalizer coefficients in registers, Stauffer teaches using registers to store pre-equalizer coefficient values. Ex-1008, 000037-000042, 000050; Ex-1003, ¶177. Stauffer's teachings show that storing pre-equalizer coefficient values in registers was well known in the art in the context of serial communications and further confirms doing so was obvious. Ex-1003, ¶178.

<b>[1b] updating the initial pre-equalizer coefficient values during a training phase; and</b>
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After the initial condition is set, Ran teaches that “[c]ontinuous modification of the selected equalization coefficients is enabled on the communications link after the communications link is established.” Ex-1006, 13:41-48, 3:14-28; Ex-1003, ¶180. Ran illustrates example processes for updating equalization coefficient values in Figures 6A and 6B. *See generally* Ex-1006, 11:65-13:30, FIGS. 6A-6B. For example, Ran teaches “[a] management entity may continue monitoring [management registers] ... to enable continuous or periodic adaptation of equalizer settings used to transmit signals.” Ex-1006, 6:23-44.



**FIG. 6A**

Ex-1006, FIG. 6A. In the training process, the management entity relays a request from the optical module's receiver to change a pre-equalizer coefficient of the NIC's (i.e., host's) transmitter by reading and writing request and response registers. Ex-1006, 11:65-12:14, 6:37-44, 12:10-31, 6:37-44. The process is repeated, and the receiver continues to "tune any transmitter equalizer settings" until, for example, a sufficiently low bit error rate (BER) is detected by the receiver. Ex-1006, 12:41-50. Accordingly, Ran teaches updating the initial pre-equalizer coefficient values during a training phase. Ex-1003, ¶181. Ran teaches

using the same training process for the opposite direction of data transmission— updating pre-equalizer coefficients used by the transmitter of the optical module based on requests from the receiver of the NIC. Ex-1006, Abstract, 6:52-62, 13:24-30; Ex-1003, ¶182.

**[1c] using the updated pre-equalizer coefficient values to convey a transmit data stream.**

After the training process (*Supra* §V.D.2[1b]), Ran teaches using the updated pre-equalizer coefficient values to convey a transmit data stream. Ex-1006, 12:41-50 (“The management entity may use the indication of ‘receiver ready’ bit set to ‘1’ to permit transmission of real data (as opposed to training data) from the host transmitter to the module for transmission to a remote station (link partner).”), 10:60-67, 5:50-54, 6:23-44, 9:60-64, 12:64-13:23; Ex-1003, ¶183.

### **3. Claim 2**

**2. The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.**

Ran teaches chip-to-module (C2M) channels. *Supra* §V.B.3[8pre]. Ran teaches selecting a preset in the context of C2M channels. Ex-1006, 9:45-59, 10:6-14. The combination of Ran, Mejia, and Stauffer teaches storing presets with different sets of initial pre-equalizer coefficients that respectively provide high performance for different channel models, each having a set of characteristics of

the channel. *Supra* §V.D.2[1a]. In light of Ran’s teaching of using presets in the context of C2M channels, the combination suggests **channel models** corresponding to these presets **are for chip-to-module (C2M) channels**. Ex-1003, ¶185.

Mejia teaches using channel **insertion loss** as a characteristic of a channel model. *Supra* §V.D.2[1a]; Ex-1009, ¶36. In addition, Stauffer teaches that **package loss** as a cause of signal degradation should be considered in configuring equalization coefficients. *Supra* §V.C.2; Ex-1008, 000029-000031. Package loss impacts the performance of a particular pre-equalizer configuration. In light of Mejia’s goal of “selecting the best equalization preset for the given system” (Ex-1009, ¶31, ¶10), a POSITA would have found it obvious to consider package loss in defining presets because doing so would have provided high performance presets for different package loss characteristics. Accordingly, the combination of Ran, Mejia, and Stauffer teaches implementing presets corresponding to channel models that are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics. Ex-1003, ¶186.

**Motivation to Combine**. Stauffer teaches that package loss is a cause of signal degradation, separate from channel insertion loss (*supra* §V.C.2; Ex-1008, 000029-000031). Mejia aims to select the best equalization to address signal degradation. Ex-1009, ¶10. For “high-bandwidth data communications

applications” (Ex-1006, 1:23-41), a POSITA would have been motivated to maximize signal quality. While a POSITA might also be motivated to address other factors, that would not preclude them from addressing package loss, which was a known source of signal degradation. Therefore, a POSITA would have found it obvious and been motivated to select sets of pre-equalizer coefficients, per Ran and Mejia’s teachings (*supra* §V.D.2[1a]), to address the package loss characteristics that Stauffer teaches, as part of the channel model. *See* Ex-1008, 000031. Ex-1003, ¶¶187-188.

Ran, Mejia, and Stauffer are compatible with each other because they are in the same field of serial communications and teach support for the same standards (PCIe). Ex-1006, 13:31-40; Ex-1009, ¶10; Ex-1008, 000061. The combination would not have changed the principle of operation of any reference. Ex-1003, ¶189.

#### 4. Claim 3

**3. The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.**

Stauffer teaches applying **different types of receiver equalization**. Stauffer teaches a Decision Feedback Equalizer (DFE) at the receiver and that the receiver operates in “one of three equalization modes: non-DFE, DFE3, or DFE5.” Ex-1008, 000052-000053. DFE3 and DFE5, for example, refer to different types of receiver equalization because they include different filter taps. *Id.*, 000053-000054.

Mejia further teaches another type of receiver equalization, CTLE. Ex-1009, ¶32; Ex-1003, ¶191.

The combination teaches or suggests multiple registers that store sets of pre-equalizer coefficients, each of which corresponds to a channel model. *Supra* §V.D.2[1a]. Both Ran and Mejia teach that the transmitter communicates with the receiver to determine the equalization coefficients to use for the communication channel. Ex-1006, 3:14-28; Ex-1009, ¶31. Mejia teaches selecting a set of equalization coefficients based on “equalization controls” from the receiver side, which a POSITA would have understood to include the receiver equalization type. Ex-1009, ¶10; *supra* §V.D.2[1a]. The receiver equalization type is among channel characteristics that can be represented or assumed by channel models. *Supra* §V.D.2[1a]. Given that various types of receiver equalization were available, a POSITA would have found it obvious for **at least some of the different channel models to presume** different types of receiver equalization. Ex-1003, ¶¶192-193.

#### 5. Claim 4

The combination teaches multiple registers that store sets of preequalizer coefficients, each of which corresponds to a channel model. *Supra* §V.D.2[1a]. Mejia’s preset search technique evaluates the performance characteristics of the pre-equalizer coefficient values corresponding to each preset in order to select the best performing preset. *Supra* §V.D.2[1a]; Ex-1009, ¶31, ¶10. The performance

characteristics evaluated include margin, BER, gain, jitter, etc. *See, e.g.*, Ex-1009, ¶10, ¶¶31-32; Ex-1003, ¶195.

## 6. Claim 5

**5. The method of claim 4, wherein the performance characteristic is an error signal energy.**

Ground 5 teaches using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers. *Supra* §V.A.5. Mejia teaches using BER, margins, gain, and/or jitter as example performance characteristics without limiting the list. *Id.*; Ex-1009, ¶¶31-34; Ex-1003, ¶197.

As explained above, Stauffer teaches or suggests using the error signal energy, measured by MSE, as a performance characteristic. *Supra* §V.C.3; Ex-1008, 000031-3; Ex-1027, 000002; Ex-1003, ¶198.

A POSITA would have been motivated to apply Stauffer's teachings to Ran and Mejia by using error signal energy, measured by MSE, as a channel performance metric. This was obvious because the same signal data used to generate Mejia's margin and BER (e.g., the received signal and the expected signal) would have been available for calculating error signal energy. *See generally* Ex-1024, cls.1-2, ¶17, FIGS. 6A-6B, 7; Ex-1009, ¶11, ¶¶31-32. The error signal energy simply involves applying the MSE calculation to the difference between received and expected signals. This was a textbook technique for error signals in

the context of equalizer adaptation in characterizing channel performance. *See*, e.g., Ex-1022, 000033. No additional data collection or measurement would have been required to determine error signal energy, and its calculation would have been known and obvious to a POSITA. Ex-1003, ¶199.

A POSITA would have been motivated, with a reasonable expectation of success, to determine the error signal energy as an indicator of channel performance on top of those enumerated by Mejia. The consideration of MSE metrics was consistent with Mejia’s teaching of considering voltage margin as performance characteristics. Ex-1009, ¶¶10-11; *See generally* Ex-1028, cl.19; Ex-1029, 7: 35-62 (using “error signal power” to compare performance of different “channel models”), Table 1. A POSITA would have been motivated to incorporate this additional performance characteristic alongside margin and BER to advance Mejia’s goal of “select[ing] the best equalization preset for the given system.” *E.g.*, Ex-1009, ¶31; Ex-1003, ¶200.

#### 7. Claim 6

Mejia teaches using **bit error rate** as a “performance characteristic.” *Supra* §V.D.5; Ex-1009, ¶¶12, 32; Ex-1003, ¶201.

#### 8. Claim 7

The combination teaches or suggests storing pre-equalizer coefficients in registers and updating the initial pre-equalizer coefficient values to updated pre-

equalizer coefficient values during a training phase. *Supra* §V.D.2[1b]. Because the updated pre-equalizer coefficients provide better performance than the starting point of the training, using the updated values would have improved the efficiency of future training processes by having a better starting point. This would have motivated a POSITA to replace the initial pre-equalizer coefficients with the updated pre-equalizer coefficients. Given the limited number of available presets (Ex-1006, 10:6-14, FIG. 3B), it would have been obvious to update the selected register with the updated pre-equalizer coefficient values. Ex-1003, ¶203.

## 9. Claim 8

[8pre]

Ran teaches the preamble, as previously explained. *Supra* §V.B.3[8pre]; Ex-1003, ¶204.

[8a] **one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and**

Ran teaches a transmit FFE that pre-equalizes data to be transmitted on the chip-to-module communications link. *Supra* §V.D.2[1a]. The data going through a serial channel is a serial symbol stream. The transmitter FFE is a type of FIR filter commonly used in serial communications. *See, e.g.*, Ex-1008, 000020. Therefore, Berke teaches **one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted.** Ex-1003, ¶205.

**[8b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.**

Ran further teaches **a controller** performing the function of using a register to set initial coefficient values. Ran teaches using management registers (including request and response registers) located on both sides of the serial link to control equalization. *Supra* §V.D.2[1a]; Ex-1006, 5:4-25, FIG. 2A. Each request register includes an “initial condition request field” that is used to select a preset from multiple options. *Supra* §V.D.2[1a]; Ex-1006, 10:6-14, FIG. 3B. A “management entity” controls the value of the request register. Ex-1006, 9:45-59, 11:65-12:31, FIGS. 3, 6; Ex-1003, ¶207.

Ran teaches or suggests implementing the management entity on the transmitter side. For example, when setting pre-equalizer coefficients of a host’s transmitter based on requests from an optical module’s receiver, Ran teaches implementing the management entity on the host device (where the host transmitter is located). Ex-1006, 5:50-61 (“The host response register 222 and/or module request register 224 may also include a one-bit receiver ready field to indicate to a host management entity that the equalization tuning is complete and that data may be reliably transmitted from the NIC 100 to the optical module 120.”), 5:39-49. This would have been a reasonable design choice because the management entity

responds to requests by editing the host's request register; being located locally on the host would have allowed the management entity to easily edit that register. Ex-1003, ¶208.

Ran also teaches the same training process in the opposite direction, for setting pre-equalizer coefficients used by the optical module's transmitter based on requests from the host's receiver. *See* above §V.D.2[1b]; Ex-1006, Abstract, 6:52-62, 13:24-30. The management entity responds to requests—this time from the host—to edit the module's request register. *Id.*, Ex-1006, 11:65-12:14, 6:37-44. Because this request register resides on the optical module, a POSITA would naturally have interpreted Ran as teaching or at least suggesting that the management entity is likewise located on the optical module. Like the host example, where the management entity was local to the transmitter side (there, the host), it would also have made sense to have the management entity local to the transmitter (here, the optical module). This would have allowed the management entity to be local to the optical module, to locally edit the request register in that module. A POSITA would have recognized the benefits of doing so. For example, it would have been more efficient and secure to use a local management entity to access and edit the registers at the optical module, as compared with using a management entity on another device. In addition, such an in-module controller configuration would have simplified dependency management of the circuits. This

symmetric approach is consistent with Ran's teaching of using the same training process for both data transmission directions and would have simplified the control logic for implementing the management entity. Ex-1006, Abstract, 6:52-62, 13:24-30. Ex-1003, ¶208.

Components of Ran's optical module that carry out the functionalities of the management entity and the registers that store initial pre-equalizer coefficients (*supra* §V.D.2[1a]) constitute a controller at the pluggable module transceiver. Ex-1003, ¶210.

The remainder of [8b] overlaps with [1a] and [8a], and is satisfied for the same reasons previously explained. *Supra* §V.D.2[1a], §V.D.9.[8a].

#### **10. Claims 9-10**

The limitations of claim 9-10 appear in claims 2-3, respectively, and are satisfied for the same reasons. *Supra* §V.D.3, §V.D.4. Ex-1003, ¶¶211-212.

#### **11. Claim 11**

Limitations [11pre]-[11a] are identical to [8pre]-[8a] and satisfied for the same reasons. *Supra* §§V.D.9[8pre]-[8b]. Ex-1003, ¶213.

**[11b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic, the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.**

Mejia further teaches performing the **determining** and **selecting** on the receiver side. *See, e.g.*, Ex-1009, ¶31 (“recommend the best equalization preset value(s) based on information from the RX (Receive) circuits”). Furthermore, Ran teaches that the management entity sets pre-equalizer coefficient values on the transmitter side by copying bit values from the receiver’s request register to the transmitter’s request register, where the request register includes the initial condition request field that selects a set of initial pre-equalizer coefficient values. Ex-1006, 11:65-12:14, 10:6-14; *Supra* §V.D.2[1a-1b]. This teaches performing the selecting step on the receiver side. Ex-1003, ¶216.

Because Ran’s optical module includes a pluggable module transceiver that includes transmit filters (*supra* §V.D.9[8pre-8a], §V.B.3[8pre]), Ran’s port transceiver in the NIC (*Supra* §V.B.3[8pre]) is on the receiver side. The combination thus teaches the **port transceiver** performing the determining and selecting steps. Ex-1003, ¶217.

The remainder of claim 11 overlaps with [8b] and claim 4 and is satisfied for the same reasons previously explained. *Supra* §V.D.9[8b], §V.D.5; Ex-1009, ¶¶11-12, 31-34, 50-51, 61-68, FIG. 3; Ex-1003, ¶¶214-215.

## 12. Claims 12-13

The limitations of claims 12 and 13 appear in claims 5 and 6, respectively, and are satisfied for the same reasons. *Supra* §§V.D.6-7. Ex-1003, ¶¶218-219.

## 13. Claim 14

Ran teaches a training process that updates the equalization coefficient values for the transmitter FFE. *Supra* §V.D.2[1b]. The transmitter FFE is a transmit filter. *Supra* §V.D.9[8a]; Ex-1003, ¶221.

Ran's training process "provide[s] for a receiver to adjust settings of a transmitter FFE of any length and step size using requests from a receiver." Ex-1006, 3:14-28. The receiver generates updates, and because the port transceiver is on the receiver side (*supra* §V.D.11[11b]), the combination teaches or suggests that the port transceiver generates updates. Ex-1003, ¶¶222-223.

## 14. Claim 15

Ran teaches or suggests a training process that updates the initial pre-equalizer coefficient values (*supra* §V.D.2[1b]) and implements the management entity in the optical module (*supra* §V.D.9[8b]). The combination teaches or suggests updating the selected register with the updated pre-equalizer coefficient values. *Supra* §V.D.8. The combination teaches or suggests that the controller saves updated coefficient values in one of the registers because the registers and Ran's optical module components for carrying out management-entity

functionalities together constitute a controller at the pluggable module transceiver.

*Supra* §V.D.9[8b]; Ex-1003, ¶225.

### **15. Claim 16**

The limitations of claim 16 appear in claim 8 and are satisfied for the same reasons. *Supra* §§V.D.9[8pre]-[8b]; Ex-1003, ¶226.

### **16. Claims 17-19**

The limitations of claims 17, 18, and 19 appear in limitation 11[b], claim 5, and claim 6, respectively and are satisfied for the same reasons. *Supra* §V.D.11[11b], §V.D.6-7; Ex-1003, ¶¶227-229.

## **VI. STANDING**

Petitioner certifies that Petitioner is not barred or estopped from requesting this inter partes review, and the '111 patent is eligible for it.

## **VII. MANDATORY NOTICES AND FEES**

1. **Real Party In Interest:** The real party-in-interest here is Marvell Semiconductor, Inc. No other parties directed, controlled, or funded this Inter Partes Review proceeding (IPR).

2. **Related Matters:**

- Certain Active Electrical Cables and Components Thereof, ITC Investigation 337-TA-1446
- *Credo Semiconductor Inc. and Credo Technology Group Ltd. v. Amphenol Corporation*, 2:25-cv-00296-JRG (EDTX)

- *Credo Semiconductor Inc. and Credo Technology Group Ltd. v. TE Connectivity PLC*, 2:25-cv-00297-JRG (EDTX)
- *Credo Semiconductor Inc. and Credo Technology Group Ltd. v. Volex PLC*, 2:25-cv-00298-JRG (EDTX)
- *Credo Semiconductor Inc. and Credo Technology Group Ltd. v. Molex LLC*, 1:25-cv-00316-JLH (Dist. Del.)
- *Amphenol Corporation v. Credo Technology Group Ltd.*, IPR2025-00699 (PTAB)
- *Volex plc. v. Credo Technology Group Ltd.*, IPR2025-01387 (PTAB)

3. **Lead and Backup Counsel**: Pursuant to 37 C.F.R. §42.8(b)(3) and 42.10(a), Petitioner designates Harper Batts (Reg. No. 56,160) as lead counsel and Chris Ponder (Reg. No. 77,167) and Jeffrey Liang (Reg. No. 69,043) as back-up counsel, each of Sheppard, Mullin, Richter & Hampton LLP.

4. **Service Information**: Petitioner consents to service by electronic mail addressed to:

HBatts@sheppardmullin.com;

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Petitioner's counsel may also be served by mail or hand delivery at Sheppard, Mullin, Richter & Hampton LLP, 1540 El Camino Real Suite 120,

Menlo Park, CA 94025. Petitioner's counsel may be reached by telephone at (650) 815-2673 and by facsimile at (650) 815-4668.

5. **Fees:** The Office is authorized to charge fees for this Petition to Deposit Account 50-4561, Ref. 20SW-408772.

Respectfully submitted,

SHEPPARD, MULLIN,  
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## CLAIM APPENDIX

<b>Claim 1</b>	
[1pre]	A SerDes communications method that comprises, in a transceiver:
[1a]	selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;
[1b]	updating the initial pre-equalizer coefficient values during a training phase; and
[1c]	using the updated pre-equalizer coefficient values to convey a transmit data stream.
<b>Claim 2</b>	
2	The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.
<b>Claim 3</b>	
3	The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.
<b>Claim 4</b>	
4	The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.
<b>Claim 5</b>	
5	The method of claim 4, wherein the performance characteristic is an error signal energy.
<b>Claim 6</b>	
6	The method of claim 4, wherein the performance characteristic is a bit error rate.

<b>Claim 7</b>	
7	The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.
<b>Claim 8</b>	
[8pre]	A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
[8a]	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and
[8b]	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.
<b>Claim 9</b>	
9	The communications link of claim 8, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.
<b>Claim 10</b>	
10	The communications link of claim 8, wherein at least some of the different channel models presume different types of receiver equalization.
<b>Claim 11</b>	
[11pre]	A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
[11a]	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and

[11b]	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic, the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.
<b>Claim 12</b>	
12	The communications link of claim 11, wherein the performance characteristic is an error signal energy.
<b>Claim 13</b>	
13	The communications link of claim 11, wherein the performance characteristic is a bit error rate.
<b>Claim 14</b>	
14	The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.
<b>Claim 15</b>	
15	The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.
<b>Claim 16</b>	
[16pre]	A pluggable module transceiver including:
[16a]	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to a port transceiver; and
[16b]	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.

<b>Claim 17</b>	
17	The pluggable module transceiver of claim 16, wherein the port transceiver determines a performance characteristic for each register.
<b>Claim 18</b>	
18	The pluggable module transceiver of claim 17, wherein the performance characteristic is an error signal energy.
<b>Claim 19</b>	
19	The pluggable module transceiver of claim 17, wherein the performance characteristic is a bit error rate.

**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that on August 8, 2025, true and correct copies of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 11,032,111 and Exhibits 1001-1030 were served in entirety on the Patent Owner at the following addresses of record as listed on Patent Center, via Priority Mail Express®:

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**CERTIFICATE OF COMPLIANCE WITH  
TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS,  
AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,630 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

Respectfully submitted,

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