

9.1: 40 Inch FHD AM-OLED Display with IR Drop Compensation Pixel Circuit

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Abstract

Samsung Mobile Display has developed a full color 40" FHD AM-OLED display, the largest OLED display ever reported to data. It was based on the technologies of Low temperature polysilicon (LTPS) TFT backplane using Super Grain Silicon (SGS) crystallization method, and power line IR-drop cancellation pixel circuit. Through this designed panel, we can estimate the possibility of large-size and high-resolution AMOLED panel as TV applications.

1. Introduction

AMOLED has a lot of merits for flat panel display, such as high brightness, wide viewing angle, fast response time etc [1]. However, in order to compete with the AM-LCD and PDP in the market, large-size AMOLED should be realized. There are several problems to be solved for high quality and large-size AMOLED displays [2]. First is uniform backplane technology. In case of AM-LCD, hydrogenated amorphous silicon TFT (a-Si:H TFT) process is widely used. But the stability of a-Si:H is too poor to use a current driven device in AMOLED panel. So we consider the LTPS process for AMOLED, there are many methods for LTPS process such as ELA, SGS, SLS, MIC, SPC and so on [3]. Even though ELA is the only method as commercial AMOLED products, to obtain good short range uniformity which is called mura, we have to design the panel with vth compensation pixel circuits [4-6]. And the beam size of excimer laser is limited to about 460mm, which means the maximum size of display is around 31 inch. Another problem to be solved in large-size AMOLED is the IR-drop along with the power line. Due to the finite resistance of metal lines, currents flowing through the row and column line give rise to voltage drop (IR-drop), which may limit the uniform gray level operation of the panel. So it causes long range non-uniformity and loading effect.

In this paper, we have developed 40" AMOLED panel using SGS technology, vth and IR-drop compensation pixel circuit.

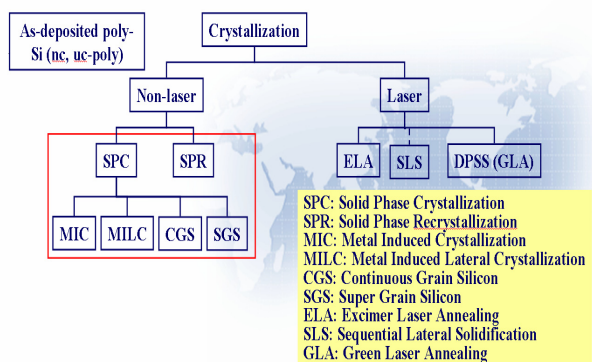


Figure 1. Classification of crystallization methods.

2. LTPS process for AMOLED backplane

Crystallization methods can be classified as shown in figure 1. Among these various crystallization methods, excimer laser annealing (ELA) has been the most widely used because ELA provides a good quality of polycrystalline silicon, which shows high field-effect mobility up to about 200cm²/Vs. However, there are still several issues such as the narrow process window, high initial investment cost and high maintenance cost. Especially limitation in laser beam length is critical obstacle for large size AMOLED panel.

2.1. Super Grain Silicon (SGS) Crystallization

Figure 2 shows a general crystallization process for SGS. First, a-Si is deposited on glass. Then, as a diffusion layer, a capping layer is deposited on a-Si. Nickel is sputtered on the capping layer. After deposition of nickel, simple thermal heating can induce nickel atoms to reach the a-Si layer, some nickel atoms aggregate to form nickel silicides. Some nickel silicides having a size bigger than a critical nucleus size for grain growth can play a role as seeds for crystallizing a-Si. Then by further heating, individual grains can grow until adjacent grains collide with one another with the aid of nickel silicides initially scattered in the a-Si region, resulting in cellular- or disk-shaped grains [3].

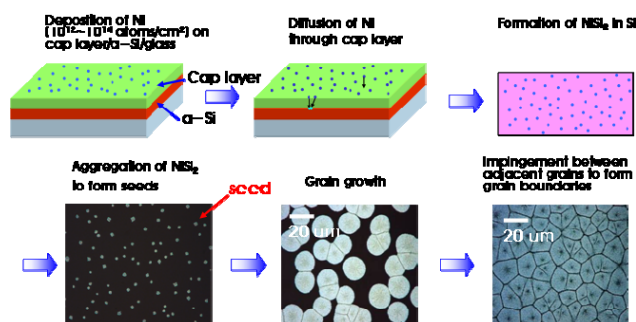


Figure 2. Crystallization process for SGS.

In Table 1, we compared TFT characteristics of poly-Si TFTs between ELA and SGS methods. Although TFT characteristics using ELA methods are better than SGS methods for high integrated panel design, it is more suitable for large size panel design using SGS methods. For large-size AMOLED display, we probably do not need very high TFT characteristics. Instead we will require applicability for large-size substrates, low cost for production, and uniformity in luminescence as long as the TFT characteristics meet the requirements for AMOLED displays.

	V _{th} (V)	Mobility (Cm ² /Vs)	I _{off} (A/um)	SS (V/dec)
ELA	-2.0	100	1e-13	0.25
SGS	-2.3	50	2e-12	0.4

Table 1. TFT characteristic comparison between ELA & SGS

3. Pixel circuit

3.1. Normal pixel circuit

The basic pixel circuit for the voltage-programmed pixel is 2-TFT pixel as shown in Fig. 3. In this case, the gray-scale control has become an important issue due to the non-uniformity feature of LTPS-TFT caused by the grain boundaries. The TFT non-uniformity problem still remains even though we use SGS technology. Another issue of 2-TFT pixel is IR-drop problem. The long range non-uniformity by IR-drop is more serious in large-size AMOLED panel.

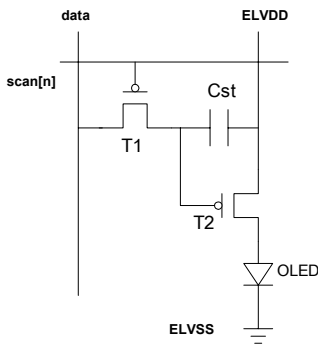


Figure 3. Normal pixel circuits.

3.2. IR-drop compensation pixel circuit

To improve uniformity of the panel, we developed threshold voltage (V_{th}) and power line (ELVDD) IR-drop compensation pixel circuit, which is composed of 5-TFT and 2-Capacitance as shown in Figure 4. Figure 5 shows the driving waveforms for pixel circuit. The driving period is divided into three periods: initializing period, v_{th} detecting period, writing period and display period. To compensate V_{th} variation of driving TFT(T1), v_{th} of T1 is stored at C_{vth}. Here, the other node of C_{vth} is connected to V_{sus} to compensate ELVDD IR-drop. After all, in display period, OLED current flows as shown in equation (1)

$$\begin{aligned}
 I_{OLED} &= \frac{\beta}{2} (|V_{GS1}| - |V_{th1}|)^2 \\
 &= \frac{\beta}{2} \{ ELVDD - (V_{data} - |V_{th1}| + ELVDD - V_{sus}) - |V_{th1}| \}^2 \\
 &= \frac{\beta}{2} (V_{sus} - V_{data})^2
 \end{aligned} \tag{1}$$

As known in equation (1), OLED current is not affected by V_{th} and ELVDD, but only depend on V_{sus} voltage and data voltage. because there is no current flow in V_{sus}, we can compensate v_{th} and ELVDD IR-drop.

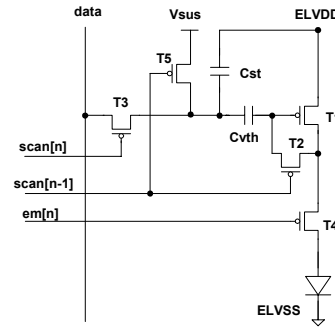


Figure 4. IR-drop compensation pixel circuits.

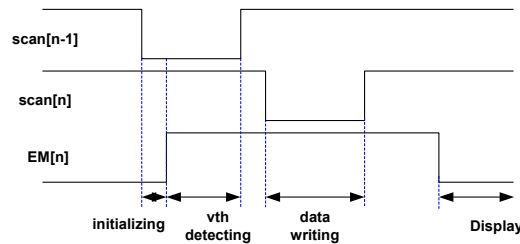


Figure 5. Pixel driving waveform.

3.3. IR-drop pixel simulation results

We verified the performance of pixel circuit by using smart-spice simulation. The simulation target is 40inch, FHD panel with peak 600cd luminance. Figure 6 shows the result of IR-drop simulation. X axis is the pixel position from ELVDD input area. We assumed that ELVDD is supplied Top and Bottom side. So, 0 on x axis means the pixel nearest from ELVDD input point, (maybe top and bottom edge area) 500 on x axis means the pixel far from ELVDD input point (panel center area). As you can see the simulation results, in case of normal pixel circuit (2TFT pixel), luminance difference from 0 pixel point to 500 pixel point is over than 9times, but in case of IR-drop compensation pixel circuit, luminance degradation from 0 pixel point to 500 pixel points is less than 3%. That means if we don't consider non-uniformity by the OLED material itself, we can obtain over 97% long-range uniformity in 40" AMOLED panel with IR-drop compensation pixel circuit

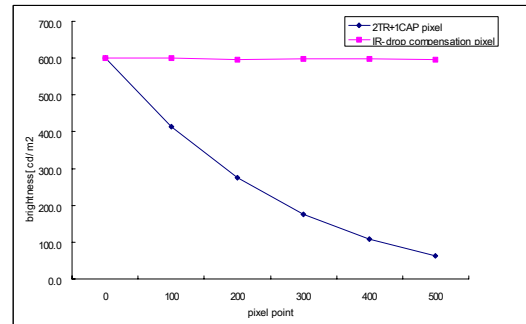


Figure 6. Pixel driving waveform.

4. Panel design

In design, we first decided target panel diagonal size to 40inch which is maximum panel size in 730x920 4-generation glass. Resolution is FHD(1920x1080) and target luminance and contrast ratio are over 500cd/m² and 10,000:1 respectively. Pixel and scan/emission driver circuits are integrated using pmos-only LTPS process using SGS method. In circuit design using SGS TFT, high TFT leakage current can be problem. Especially in pixel circuit design, high leakage current can make contrast ratio lower. So we used multi-finger gate TFT in critical leakage path. Figure 7 shows the panel diagram. We used total 12-number of 480ch driver ICs for driving the data line, 6 driver ICs are attached on top side, and the other 6 driver ICs are attached on bottom side. So, the odd data lines are driven by bottom driver ICs and the even data lines are driven by Top driver ICs. ELVDD powers are mainly supplied between driver ICs on top and bottom sides. And on left and right side, ELVSS powers are mainly supplied and scan/emission drivers are integrated.

4.1. Scan & Emission driver

The IR-drop compensation pixel circuit uses 2 kinds of control signals. So we need 2 types of gate driver. One . In 40" FHD panel, the gate line load is too big to drive only one side. So we integrated two drivers symmetrically at each side to drive the gate line at each side.

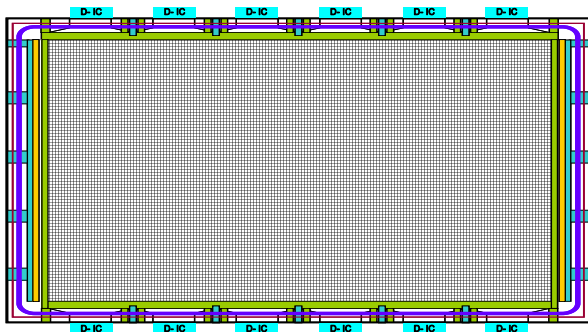


Figure 7. 40" FHD panel diagram.

PARAMETER	SEPCIFICATION	UNIT
DISPLAY SIZE	40	inch
NUMBER OF DOTS	1920 X 1080	dot
PIXEL PITCH	151 x 453	um
GRAY LEVEL	64	gray
ASPECT RATIO	16 : 9 (H x V)	-
PPI	56	ppi
PEAK INTENSITY	> 500	cd/m2
CONTRAST RATIO	> 10,000:1	-
TFT TYPE	PMOS only	-

Table 2. Specification of 40-inch AM-OLED display



Figure 8. Image of 40" FHD AM-OLED display

5. Conclusions

The developed display has 40-inch diagonal size with FHD resolution, sub-pixel size of 151x453um. The specifications of the 40-inch FHD AM-OLED prototype are indicated in Table 2. We applied new crystallization method (SGS) and a conventional shadow mask to deposit small molecule OLED material onto TFT substrates by thermal evaporation. Figure 8 shows the displayed image of it. The developed 40" AM-OLED shows good image quality and large color gamut providing that our approach for pixel design is effective for large area AM-OLED display. It shows perfect compensation for gradual luminance difference by using IR-drop pixel circuit.

6. References

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