

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; WUHAN
CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO. LTD.; AND
VISIONOX TECHNOLOGY, INC.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case No. IPR2023-00941
U.S. Patent No. 7,414,599

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,414,599**

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LISTING OF EXHIBITS

Exhibit	Description
EX1001	U.S. Pat. 7,414,599 (Chung)
EX1002	U.S. Pat. Pub. 2003/0132931 (Kimura)
EX1003	Expert Declaration of Dr. Daniel Foty
EX1004	U.S. Pat. 6,362,798 (Kimura '798)
EX1005	File History for U.S. Pat. 7,414,599
EX1006	U.S. Pat. Pub. 2001/0022565
EX1007	U.S. Pat. Pub. 2003/0030603
EX1008	Excerpts from <i>Analog Integrated Circuit Design</i> , David A. Johns et al., John Wiley & Sons, Inc., 1997.
EX1009	<i>Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits</i> , Harold Shichman et al., IEEE Journal of Solid-State Circuits, Vol. SC-3, No. 3, September 1968.
EX1010	Excerpts from <i>Physics and Technology of Semiconductor Devices</i> , A. Grove, John Wiley & Sons, 1967.
EX1011	Excerpts from <i>CMOS Digital Integrated Circuits: Analysis and Design</i> , (third edition), S. Kang et al., McGraw-Hill, 2003.
EX1012	U.S. Pat. 6,229,506 ("Dawson")
EX1013	U.S. Pat. 5,666,046
EX1014	<i>TFT AMOLED Pixel Circuits and Driving Methods</i> , J. Stanford, SID 03 Digest, pp. 10-13 (2003))
EX1015	<i>A New Pixel Circuit for Active Matrix Organic Light Emitting Diodes</i> , J. Goh, IEEE Electron Device Letters vol. 23, pp. 544-546 (2002)

Exhibit	Description
EX1016	<i>A Novel Pixel Circuit for Active-Matrix Organic Light-Emitting Diodes</i> , J. Goh et al., SID 03 Digest, pp. 494-497 (2003)
EX1017	<i>Current-Writing Active-Matrix Circuit for Organic Light-Emitting Diode Display Using a-Si:H Thin-Film-Transistors</i> , R. Hattori et al., IEICE Transactions on Electronics vol. E83-C, pp. 779 – 782 (2000).

I. INTRODUCTION

Petitioner requests *inter partes* review (“IPR”) of claims 1-18 (“Challenged Claims”) of U.S. Pat. 7,414,599 (EX1001, “the ’599 patent”). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim. Indeed, the Petition presents an extremely strong case of single-reference obviousness for all Challenged Claims, most of which resulted from a first-action allowance during prosecution.

The ’599 patent claims a pixel driver circuit for OLED displays that includes five transistors, all of which are PMOS transistors. The prior art Kimura reference (U.S. Pat. Pub. 2003/0132931, EX1002) discloses the same five-transistor circuit configuration, except that four transistors are NMOS. But, as was very well-known to POSITAs at the time, PMOS and NMOS transistors are interchangeable when used as switching transistors. Indeed, Kimura itself expressly teaches that NMOS transistors “function as simple switching devices, and therefore any polarity may be used” (*i.e.* NMOS and PMOS transistors are swappable). *See, e.g.* EX1002, [0396]. Making this well-known and expressly-disclosed substitution renders the Challenged Claims obvious.

II. REQUIREMENTS FOR *INTER PARTES* REVIEW

This Petition complies with all statutory requirements, as well as 37 C.F.R. §§42.104, 42.105, and 42.15, and should be accorded a filing date pursuant to 37

C.F.R. §42.106.

A. Certification

Petitioner certifies that the '599 patent “is available for *inter partes* review and that the petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in the petition.”

37 C.F.R. §42.104(a).

B. Identification of Challenges and Requested Relief

Under 37 C.F.R. §§42.104(b) and 42.22, Petitioner requests that the Board institute IPR on the Challenged Claims of the '599 patent and cancel those claims as unpatentable on the following ground:

Ground	Claims	Basis for Unpatentability
1	1-18	Obviousness under 35 U.S.C. §103 over Kimura (EX1002) and Knowledge of POSITA (defined in IV.D)

This Petition is supported by the Declaration of Dr. Daniel Foty (EX1003, “Foty”), a leading circuit design expert.

III. TECHNOLOGY BACKGROUND

A. OLED Basics

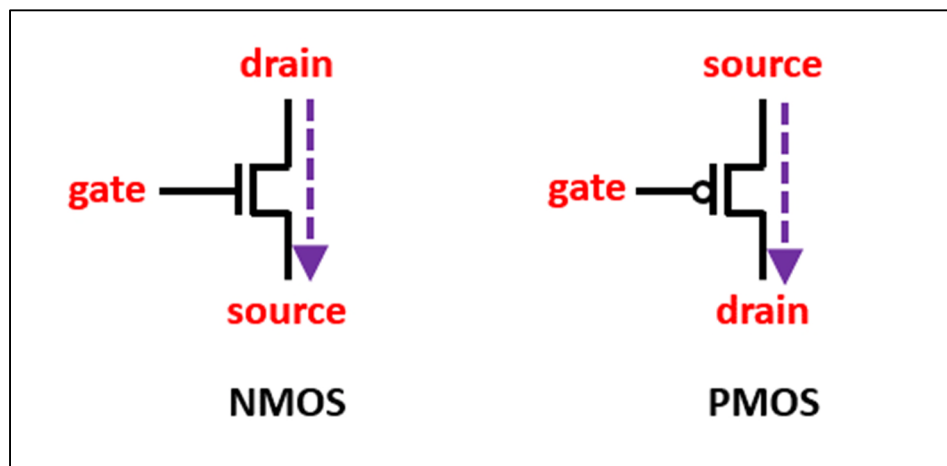
OLED is an acronym for organic light-emitting diode. Such diodes, also called electroluminescent elements, emit light in response to electric current. EX1003, ¶¶84-87. Typical OLED applications include television screens, computer monitors, and the like. OLED displays comprise a matrix of individual

pixels and each pixel includes driving circuitry that provides current to the diode. EX1003, ¶88-90. The amount of current (which determines the amount of light) results from a data voltage applied to the driving transistor. EX1003, ¶¶84-87.

Pixels are typically arranged and activated as horizontal rows or vertical lines called “scan lines.” EX1003, ¶¶91-93. Control circuitry activates the lines one at a time to display an image. EX1003, ¶¶91-93.

B. Transistor Basics

Both NMOS (also called “n-channel” or “n-type”) and PMOS (also called “p-channel” or “p-type”) transistors have existed for decades. EX1003, ¶¶37-44; EX1008. Each has a gate, source, and drain terminal. EX1008; EX1003, ¶¶48-53. The respective circuit symbols (shown below) differ only in the small circle on the PMOS gate. *Id.* It is definitional that current (represented by purple arrow) flows from drain to source in NMOS transistors and source to drain in PMOS transistors. *Id.*



The gate voltage controls transistor operation (*i.e.*, turns it on/off). EX1008; EX1003, ¶¶48-53. In particular, the minimum gate voltage (relative to the source) necessary to activate a transistor is called the threshold voltage (V_{th}). EX1008; EX1003, ¶¶59-67. NMOS transistors are “active high,” meaning high gate voltage activates the transistor and PMOS transistors are “active low,” meaning low gate voltage activates the transistor. EX1003, ¶57; EX1002, [0362] and [0445].

OLED driver circuits are formed from transistors. Each pixel has a “driving transistor” that supplies current for the light emitting element. EX1002, [0502]. The remaining transistors function as “switching transistors” and serve various supporting roles. EX1003, ¶88.

The complementary nature and interchangeability of NMOS and PMOS switching transistors was well-known by 2003. *See, e.g.*, EX1004 (U.S. Pat. 6,362,798, “Kimura ’798”) at 12:30-49 (“[E]very TFT can be N-channel type TFTs or all TFTs can be P-channel type TFTs....[I]t is often advantageous in manufacturing when all TFTs are of the same type.”); EX1003, ¶¶56-58. Making the relatively minor changes necessary for the substitution is well within the knowledge and skill of a POSITA circa 2003. EX1003, ¶¶56-58.

IV. THE ’599 PATENT

U.S. Pat. 7,414,599 is titled “Organic Light Emitting Device Pixel Circuit and Driving Method Therefor.” The ’599 patent claims priority through a Korean

application to July 7, 2003 and is a pre-AIA patent. The '599 patent contains 5 independent claims and 18 total claims.

A. Summary of the Patent

The '599 patent discloses an OLED driver circuit that powers an individual OLED pixel. EX1001, 1:16-20. The driver circuit forces current through the light emitting element which determines how much light is emitted. This is similar to an incandescent light bulb—more current results in more light.

The '599 patent explains that “current intensity flowing through the [light emitting] element change[s] over time” which causes problematic “display nonuniformity.” *Id.*, 1:38-50. The change in current “results from a change in...the threshold voltage of the driving transistor.” *Id.*; *see also id.*, 3:20-27 (threshold voltage variations “result[] in degraded image quality.”); 3:35-40 (“threshold voltage deviation of the driving transistor is not compensated.”).

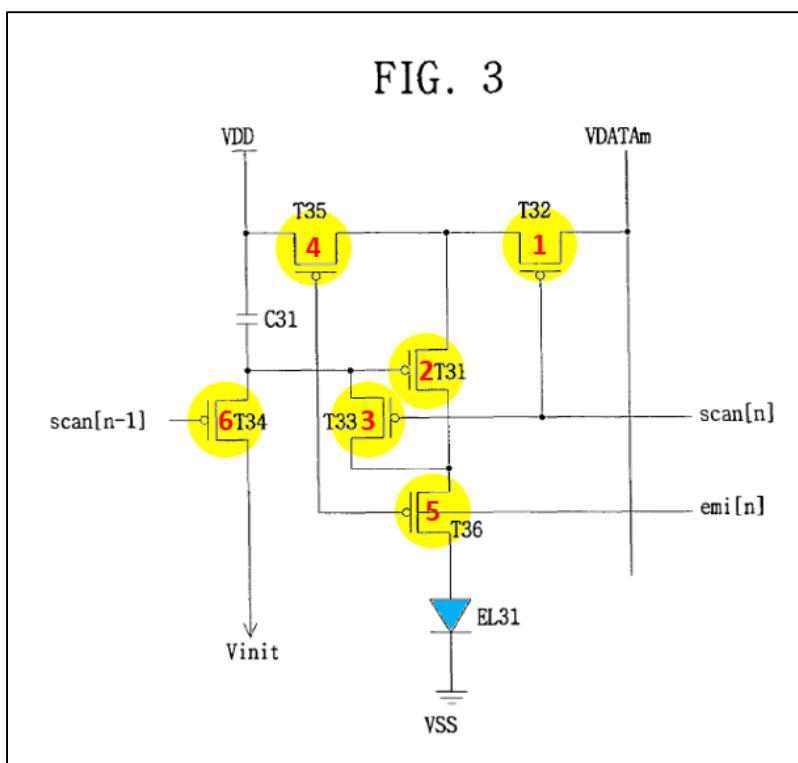
To address “display nonuniformity” caused by threshold voltage fluctuations affecting light output, the '599 patent proposes a circuit architecture where the driver circuit self-compensates for threshold voltage deviation in the driving transistor before emitting light. *See* '599, 3:46-47; 3:51-58 (proposed circuit “driv[es] current flowing through an EL element to be uniform regardless of threshold voltage deviation between respective pixels”).

Fig. 3 illustrates the purportedly novel architecture of the driving circuit.

Figs. 1 and 2 are labelled “PRIOR ART” and Figs. 4-7¹ show the circuit operation in Fig. 3. As understanding Fig. 3 (which directly maps to all Challenged Claims) will aid the patentability analysis, we discuss it here. We first identify the structural components of the driver circuit and then discuss its three operational modes.

Fig. 3 is a pixel circuit “composed of six transistors T31-T36, one capacitor C31 and electroluminescent (EL) element EL31.” *Id.*, 6:20-23. These elements are shown below in annotated Fig. 3. The electroluminescent element (EL31) is highlighted in blue and the capacitor is C31.

¹ As-issued Fig. 7 duplicates Fig. 6. This Petition uses the correct Fig. 7 (described at col. 7:50-65) from the original Korean application. *See* EX1005 (File History) at pdf466.



The red numbers correspond to how all claims (except claim 1 and its dependents) identify the transistors. This Petition only uses the claim 1 numbering scheme where specifically noted. The table below summarizes the purpose/function of each transistor described in the '599 patent specification and maps them to the claims. The ensuing discussion explains how each transistor, and the overall circuit, operates.

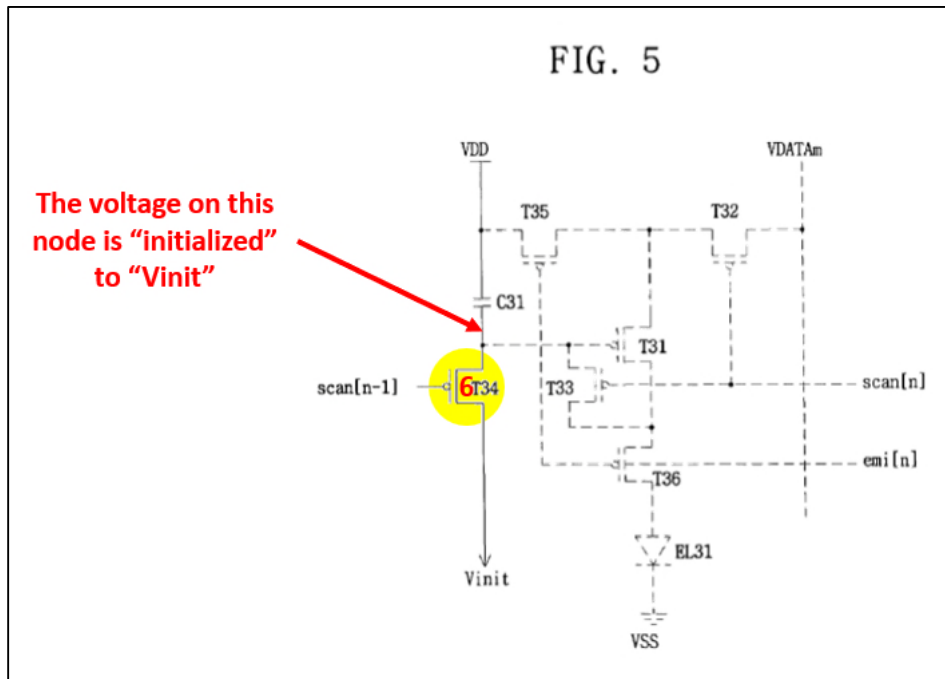
Claimed Transistor Number	Fig. 3	Description
1/first	T32	“switching transistor T32 for switching data signal voltage VDATAm” (col. 6:25-26)

Claimed Transistor Number	Fig. 3	Description
2/second	T31	“driving transistor T31 for supplying a driving current of the organic electroluminescent device [EL31]” (col. 6:28-30)
3/third	T33	“threshold voltage compensation transistor T33 for compensating the threshold voltage of driving transistor T31” (col. 6:32-34)
4/fourth (claim 1 calls this transistor 5)	T35	“switching transistor T35 for providing power supply voltage VDD” (col. 6:52-53)
5/fifth (claim 1 calls this transistor 6)	T36	“switching transistor T36 for providing a driving current, generated through driving transistor T31 [to] element EL31” (col. 6:55-57)
6/sixth (claim 2 calls this transistor 4)	T34	“initialization transistor T34 for initializing the data signal stored in capacitor C31” (col. 7:3-6)

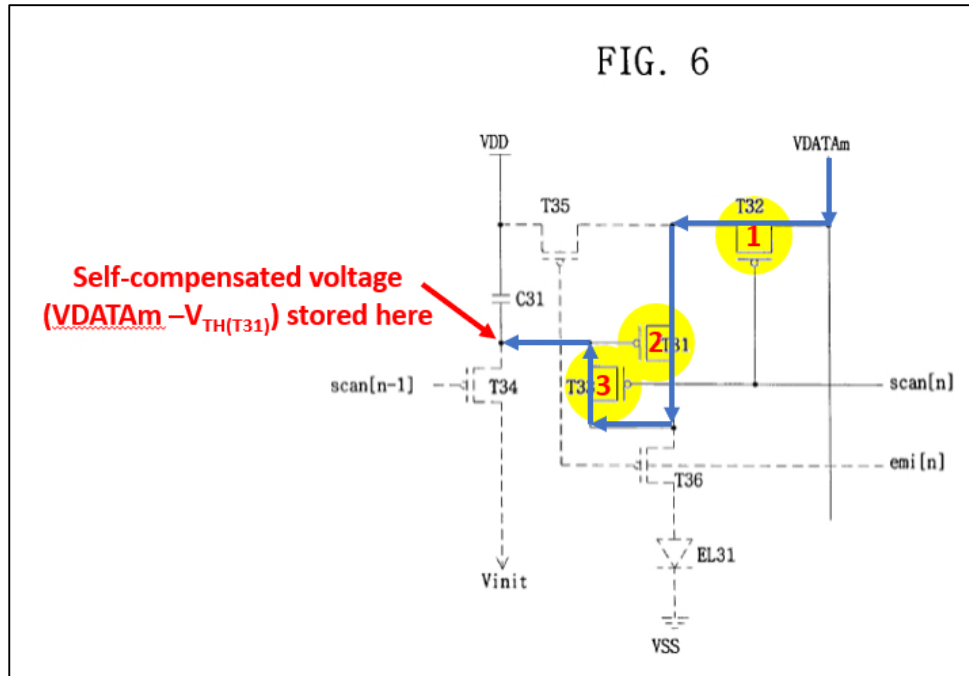
The '599 patent specification discloses three operating modes for Fig. 3: (1) initialization; (2) programming; and (3) light emitting. '599, 7:12-65; *see also id.*, Fig. 4 (control signals and timing diagram for each mode). These operational modes (described in Figs. 4-7, respectively) are discussed below.

Initialization. During initialization the circuit is “initialized” (*i.e.*, reset) to a baseline mode of operation. In particular, all transistors are turned off except for the sixth transistor. *Id.*, 7:15-26. The sixth transistor replaces any residual voltage stored on the capacitor with an initialization voltage (labeled “Vinit” in Fig 3). *Id.*

This operation is illustrated in Fig. 5 (dashed line transistors are turned off). *Id.*



Programming. During programming, the capacitor is “programmed” with (*i.e.*, stores) a “data voltage.” *Id.*, 7:28-48. Due to the “diode connected[ed]” arrangement of the second and third transistors, the capacitor’s voltage is set to a level which compensates for the threshold voltage of the second transistor (the driving transistor). *Id.* In particular, the “programmed” voltage stored on the capacitor is $V_{DATAin} - V_{TH(T31)}$, where V_{DATAin} is the input voltage to first transistor (T32) and $V_{TH(T31)}$ represents the threshold voltage of the second transistor (T31). *Id.* During programming (shown in Fig. 6 below), no current flows through the light emitting element (EL31) and no light is emitted. *Id.* The blue arrow (added) shows the direction of current flow during programming.



Light Emission. As the name suggests, during the light-emitting operation, the light emitting element (EL31) emits light. *Id.*, 7:50-65. This operation is shown in Fig. 7 (from Korean application). *Id.* The second (T31), fourth (T35), and fifth (T36) transistors turn on to provide a current path from VDD to ground that runs through the light emitting element (EL31), which causes it to emit light. *Id.* Notably, during light emission, the self-compensated voltage stored on the capacitor activates the second transistor (T31) to produce the driving current. *Id.* The light emission operation is followed by an initialization operation as described above, that resets the capacitor's voltage for the next image frame. *Id.*, 8:22-28.

allowable if re-written in independent form since the sole asserted reference (U.S. Pat. 6,229,506 (“Dawson”) had only four transistors. *Id.*

The applicant amended independent claim 1 to include the two additional transistors from claim 3 (*i.e.*, “fifth” and “sixth” transistors), which is why issued claim 1 recites “first,” “second,” “third,” “fifth,” and “sixth” transistors but not “fourth” transistor. EX1005 (Oct. 12, 2007 Office Action Response). Claims 1, 2, and 4-7 were thus allowed. EX1005 (Jan. 17, 2008 Office Action).

C. Discretionary Denial Under 35 U.S.C. 325(d) Is Not Warranted.

Kimura should not present a §325(d) issue, because neither prong of the two-part framework from *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (Feb. 13, 2020) is satisfied.

First, although the Japanese version of Kimura (without an English-language translation) was identified in an IDS *after* the examiner indicated the claims were allowable, Kimura is not substantially similar or cumulative to Dawson (the sole reference asserted during prosecution). *See* EX1005 (July 20, 2007 IDS, listing Japanese Pat. Pub. No. 2003-202833). Dawson has only four transistors. In contrast, Kimura discloses multiple circuits with five or more transistors. Thus, Kimura is not cumulative to Dawson and does not present the same (or substantially the same) arguments.

Because the first prong of *Advanced Bionics* is not met, the second prong is

inapplicable. Regardless, factor (c) from *Becton, Dickinson & Co. v. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (Dec. 15, 2017) strongly weighs against denying institution since none of the art or arguments in the Petition were evaluated during prosecution. Even if the examiner considered Kimura (which was only submitted in Japanese), the obviousness arguments presented here were not evaluated and are not cumulative to Dawson (as discussed above). Thus, even if *Advanced Bionics*' second prong applied, the Patent Office erred in not applying Kimura (or any other reference) that even had the minimum number of transistors recited in the claims.

D. Level of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") in the technology field of the '599 patent would have had a Bachelor's degree in electrical engineering or similar discipline, along with 2-3 years of circuit design/analysis experience. *See* EX1003, ¶31. Lack of work experience can be remedied by additional education, and vice versa. *Id.*

V. CLAIM CONSTRUCTION

In an IPR, claim terms are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*) and its progeny. The Board, however, only construes claim terms when necessary to resolve the controversy. *See, e.g., Toyota Motor Corp. v. Cellport Sys., Inc.*, No. IPR2015-00633, Paper No. 11 at 16

(P.T.A.B. Aug. 14, 2015). Petitioner submits that no term requires construction for this proceeding.²

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Description of Kimura

U.S. Pat. Pub. 2003/0132931 (EX1002, “Kimura”) was filed October 30, 2002 and is prior art to the ’599 patent under §102(e).

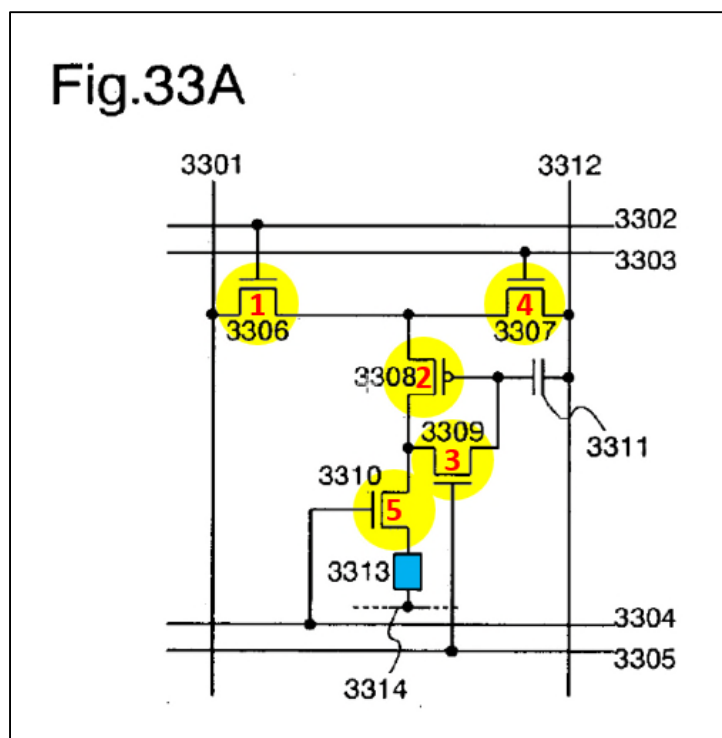
Kimura is titled “Semiconductor Device and Driving Method Thereof” and, like the ’599 patent, addresses “[b]rightness irregularities” in OLED displays resulting from “[dis]persion among pixels in the threshold values of [the transistors]” that drive current through the light emitting element. EX1002, Abstract; *see also id.*, [0359] (“If there is dispersion [in V_{th} values]...the sizes of the corresponding drain currents flowing in the TFTs differ, even if the same image signal is input, and there is dispersion in the brightness of the EL devices.”). Kimura discloses numerous circuit architectures for addressing this problem, but only those relevant here are discussed. For example, Kimura discloses the same diode-connected self-compensating transistor configuration as the ’599 patent. *See id.*, Abstract (“[A signal whose voltage] is offset by the amount of the threshold

² Petitioner reserves all rights to raise claim construction and other arguments in the ITC as relevant there.

value is therefore applied to the [driving transistor's gate]."); *see also id.*, Fig. 33D and [0655] (“[Driving transistor] thus behaves as a diode connected TFT”).

The baseline circuit for Petitioners’ patentability analysis is Kimura Fig. 33³ which, with only minor modifications taught by Kimura and known to POSITAs (*e.g.*, replacing NMOS transistors with PMOS), renders all Challenged Claims obvious. These modifications (and reasons for them) are discussed after reviewing unmodified Fig. 33, shown below with the electroluminescent element highlighted in blue and red numeric identifiers added for reference. The capacitor is element 3311. Note that the second and third transistors are diode-connected such that the circuit self-compensates for threshold voltage deviations in the second transistor. EX1002, [0655].

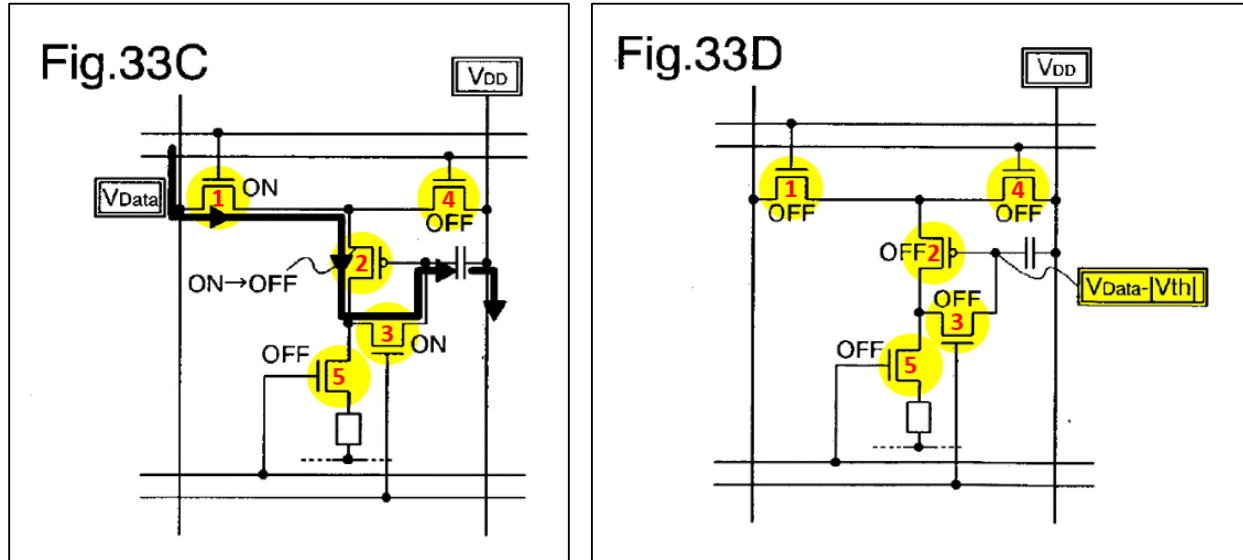
³ It should be noted to Kimura Fig. 36 is merely an extension of Fig. 33 and discussion of one applies equally to the other unless noted.



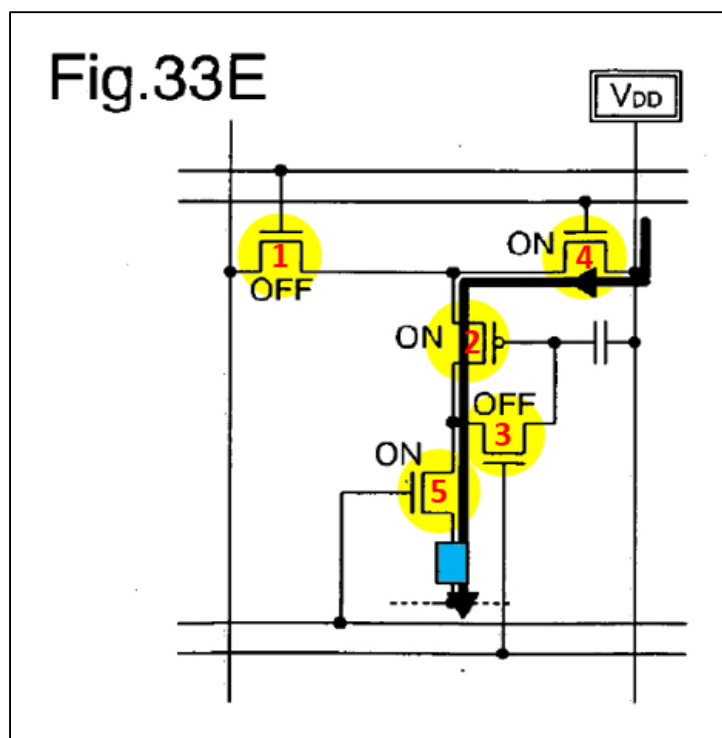
The operation of unmodified Fig. 33A is illustrated in Figs. 33B-33E (and described at [0652]-[0658]), which correspond to the three operational modes in the '599 patent: (1) initialization (*i.e.*, reset); (2) programming; and (3) light emitting. See EX1002, Fig. 16B (showing “erasure” (*i.e.* initialization), “input image signal” (*i.e.*, programming), and “sustain” (*i.e.*, light emitting)). We discuss initialization after programming and light emission.

Programming. We begin with Fig. 33C, which shows how current (illustrated by black arrows in original figure) flows through the first, second, and third transistors to charge the capacitor to a specified voltage. EX1002, [0655]. During programming the fourth and fifth transistors are off. The second transistor transitions ON→OFF when the voltage across the capacitor’s electrodes reaches

$V_{\text{Data}} - |V_{\text{th}}|$ (see Fig. 33D). *Id.*, [0655]. This is a self-compensated voltage relative to the second transistor's threshold voltage. *Id.*, [0655] and [0657].



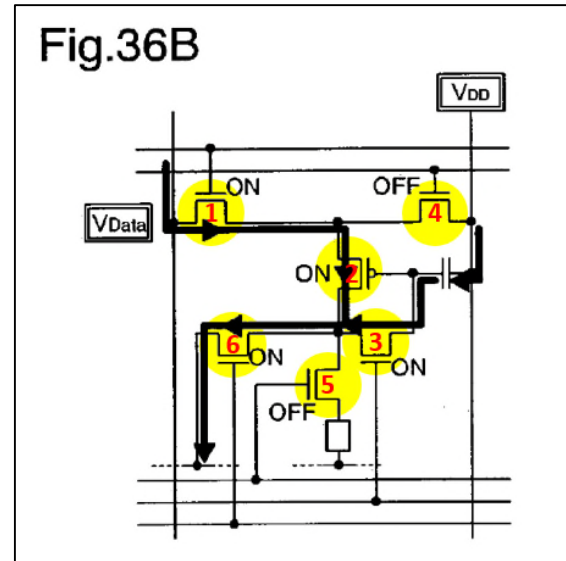
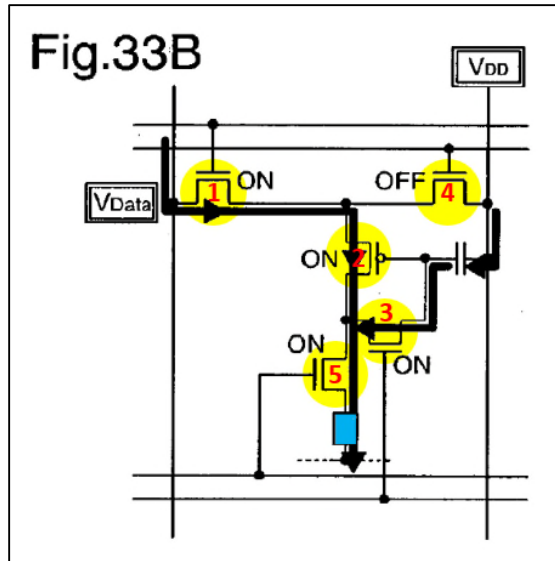
Light Emission. During light emission (shown in Fig. 33E) the electroluminescent light emitting element (highlighted in blue) emits light. EX1002, [0656]. As shown, the second, fourth, and fifth transistors are ON to provide a current path from V_{DD} to ground that runs through the light emitting element, causing it to emit light. *Id.* The black arrows reflect current flow. Notably, during light emission the self-compensated voltage stored on the capacitor activates the second transistor to produce the driving current. *Id.*, [0655]-[0656].



Initialization.⁴ Kimura discloses that the fifth transistor “can also be used as an erasure [transistor]” that resets the capacitor voltage to a default initialization value. EX1002, [0658]. This is shown in Fig. 33B below, where the black arrow coming from the right shows the current path which discharges the capacitor. This initialization approach, however, is less desirable because current discharges through the light emitting element causing undesired light emission. *Id.*, Fig. 33B; [0665] (“[C]urrent flows in the EL device to cause light emission, before or after threshold voltage acquisition, that is during a period that is not the normal light emitting period.”).

⁴ Kimura also calls this “reset” (*see* Fig. 1B) and “erasure” (*see* [0658]).

One way Kimura solves this problem is adding a dedicated initialization transistor (labelled sixth transistor) as shown in Fig. 36B below where, during initialization, the capacitor discharges through the sixth transistor instead of the light emitting element. EX1002, [0666]-[0667] (“A [sixth transistor] is therefore added as shown in FIG. 36[...Light emission by the EL device during unnecessary periods can thus be prevented.”). As reflected in Figs. 33 and 36, initialization is performed immediately before programming.



Another solution taught by Kimura (where the initialization transistor is placed in a different location) is discussed in connection with claim 8 *infra*.

Before the element-by-element patentability analysis, it is helpful to discuss a modification to Kimura Fig. 33. Thus far, all transistors (except the driving transistor) in Kimura Fig. 33 are NMOS transistors. However, Kimura repeatedly

and expressly teaches the interchangeability of NMOS and PMOS transistors used as switches, which is the case for all but the second transistor. *See, e.g.*, EX1002, [0438] (“Note that a structure is used [in Figs. 3B-3D] in which the TFTs 304 and 306 are n-channel TFTs....**However, the TFTs 304 and 306 function as simple switching devices, and therefore any polarity may be used.**”); *id.*, [0396] (same for Figs. 1-2); *id.*, [0445] (same for Figs. 4B-4D); *id.*, [0649] (“All other TFTs are only used as switching devices for performing only on and off control, and therefore may be of any polarity.”); *id.*, [0362] (showing an all-PMOS driver circuit in Fig. 22); EX1003, ¶¶146-154. Beyond these broad teachings (already known to POSITAs circa 2003, *see supra* §III.B), Kimura specifically discusses replacing various NMOS transistors in Fig. 33 with PMOS as discussed immediately below.

For example, Kimura expressly discloses that using a PMOS device for the **fifth transistor** (shown in Fig. 37A) enables “threshold voltage acquisition at higher speed.” EX1002, [0670]; *see also id.*, [0434] (“any polarity may be used” for series-connected switching transistor (labelled 1809 in Fig. 18A and discussed in Figs. 19A-C)); [0432] (using PMOS device in “close proximity” to driving transistor “increase[s] the aperture ratio within a pixel, and [] reduce[s] the tendency for dispersion in TFT characteristics”).

And Kimura expressly discloses replacing the **first or fourth transistor** in

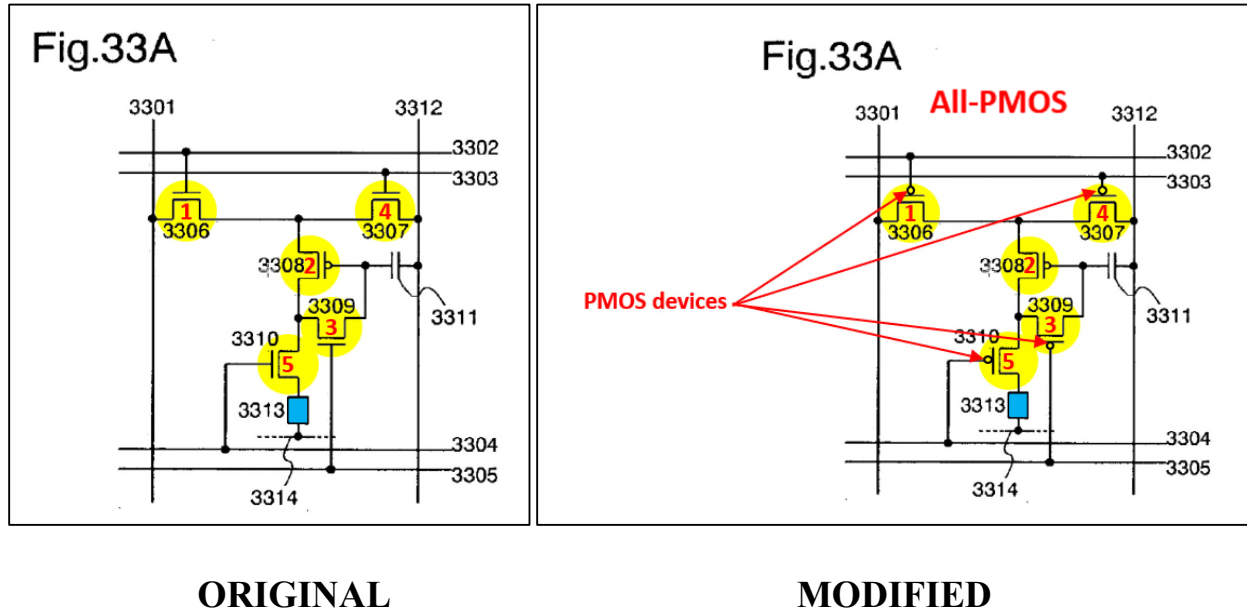
Fig. 33 with PMOS and shows an example (Fig. 34A) where the fourth transistor is PMOS. *See* EX1002, [0659] (“[T]he polarity of one of the TFTs [first or fourth transistors] may be made opposite to the polarity of the other TFT....”). A POSITA would have understood that making an NMOS transistor the “opposite [] polarity” means replacing it with PMOS. EX1003, ¶57.

Similarly, with respect to the sixth transistor, Kimura teaches that “there are no particular limitations placed on the polarity of the [initialization transistor].” EX1002, ¶[0418]. And changing the **third transistor** to PMOS in Kimura Fig. 33, was a simple design choice and would have been obvious to a POSITA because it is a switching device and it would have been “advantageous” to “manufactur[e] all TFTs [] of the same type.” EX1004 (Kimura ’798) at 12:30-49; *see also* EX1002, [0438]; EX1003, ¶¶56-58 and 146-154.

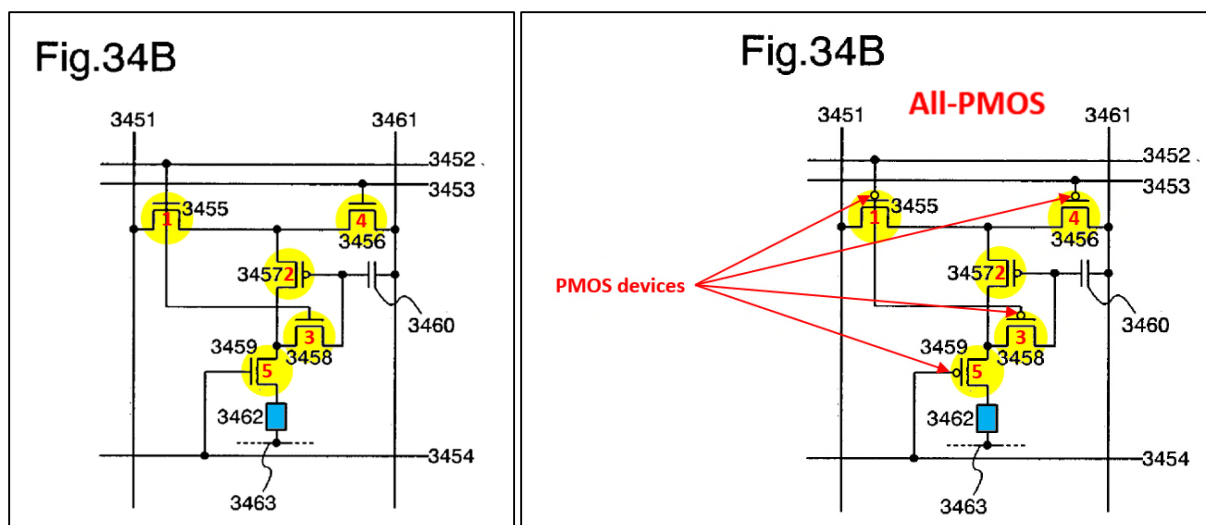
Applying Kimura’s express teachings (and/or POSITA knowledge) to create an all-PMOS implementation of Fig. 33 would have been a simple and obvious design choice.⁵ EX1004 at 12:30-49; EX1003, ¶¶146-154. And a POSITA would have had far more than a reasonable likelihood of success as making such changes

⁵ Of course, an all-PMOS implementation requires active-low signaling, but that was well-known to a POSITA and would have been trivial to implement. EX1003, ¶154 and ¶57.

was commonplace and well within a POSITA's skill. EX1003, ¶154. The all-PMOS Fig. 33 is shown below, side-by-side with the original for comparison. Because the modification is so trivial, arrows are added showing the changes (*i.e.*, small circles on transistors 1 and 3-5 indicate PMOS).



Petitioner uses the modified “All-PMOS” version of Fig. 33 for the patentability analysis and includes the label “All-PMOS” for clarity. Petitioner occasionally cites (and thus shows below) an “All-PMOS” version of Fig. 34B.



ORIGINAL

MODIFIED

B. Ground 1: Claims 1-18 are Obvious in View of Kimura and the Knowledge of a POSITA

The analysis begins with independent claim 7 rather than claim 1 for two reasons. *First*, claim 1 uses an unusual numbering scheme which skips the “fourth” transistor (which is an artifact from prosecution). *See* §IV.B. *Second*, all other independent claims use the claim 7 numbering scheme.

1. Claim 7

a. [Claim 7 Preamble]: “A pixel circuit in an organic light emitting device, comprising:”

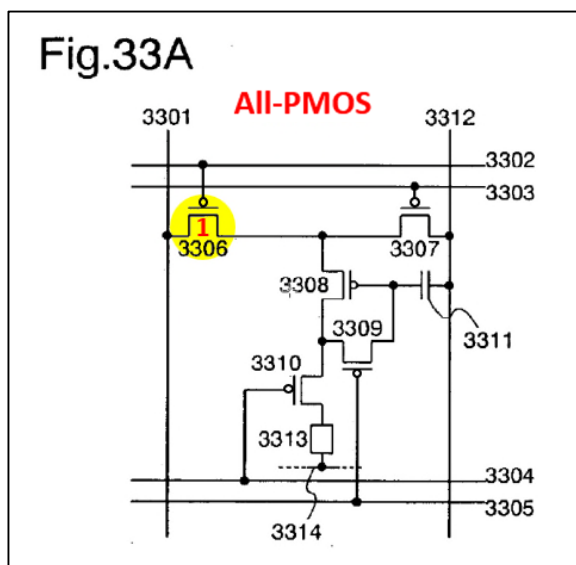
To the extent the preamble is limiting, Kimura discloses “[a] pixel circuit in an organic light emitting device.” Kimura “relates to the configuration of an active matrix *light emitting device*....” EX1002, [0001]. And Kimura discloses that “[a]n *organic light emitting material*...can be used as the EL layer.” *Id.*, [0556]-

[0557].

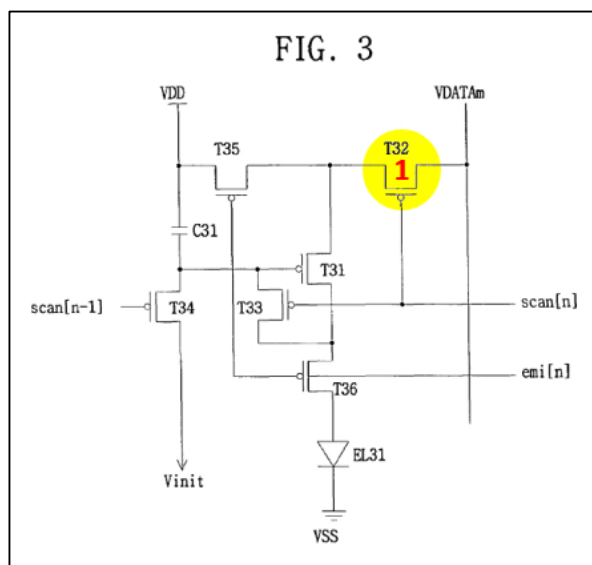
Kimura's semiconductor device has "*a plurality of pixels [] arranged in a matrix shape* over a substrate." *Id.*, [0476]; *see also id.*, [0035]; [0352]. In addition to the electroluminescent element that emits light, each pixel includes circuitry for driving the element as shown in Fig. 33. *See id.*, [0654] (Fig. 33A shows "driver TFT for performing control of electric current supplied to an EL device 3313.").

b. [7a]: "a first transistor for delivering a data signal voltage in response to a current scan line signal;"

Kimura discloses claim element 7[a]. The "**first transistor**" in Kimura is labelled 3306 in Fig. 33 (below left). In the claimed embodiment of the '599 patent, the "first transistor" is T32 (*see* Fig. 3 below right).



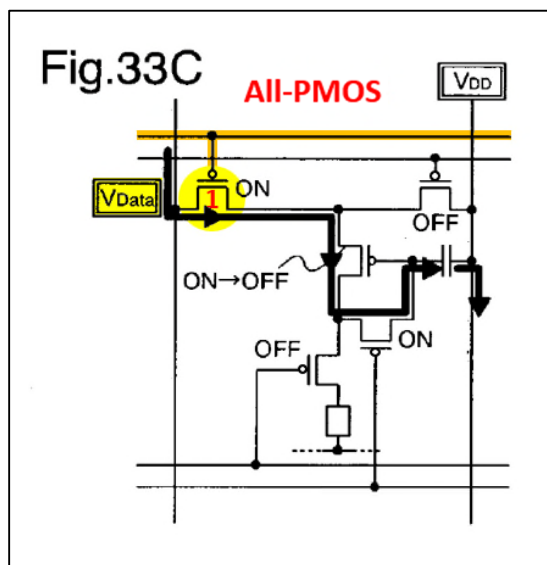
Kimura



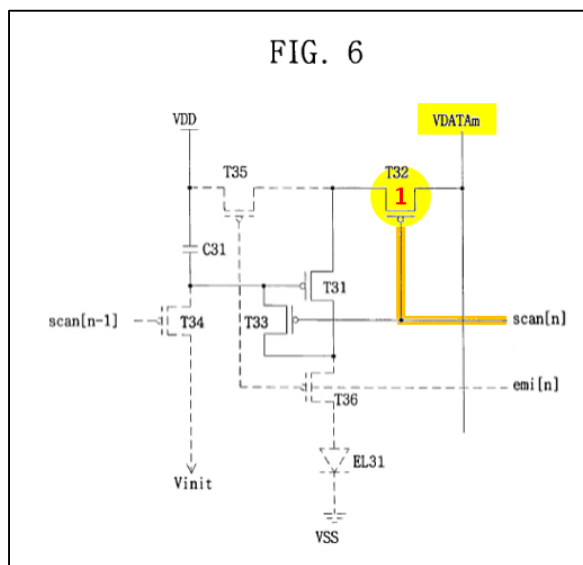
'599 Patent

As shown in '599 patent Fig. 6 (below right), the first transistor delivers the

data signal voltage (labelled “V_{DATA}m”). The corresponding “data signal voltage” in Kimura Fig. 33C is labelled “V_{Data}” (below left). EX1003, ¶167.



Kimura



'599 Patent

Claim element 7[a] also requires that the first transistor deliver the data signal voltage “**in response to a current⁶ scan line signal.**” A “scan [line] signal”

⁶ The modifier “**current**” in this context is not used in the electrical sense (*i.e.*, flow of charged particles); rather, it distinguishes the scan signal for a particular pixel line from adjacent ones (whose scan signal asserts before/after the “current” row). *See, e.g.*, EX1001, 2:17-32. This is apparent from dependent claim 8 which refers to “a scan signal just before the current scan signal.” The '599 patent specification's shorthand for “current scan [line] signal” is “scan[n],” where the

for an OLED display generally refers to the control signal for programming a line/row of pixels, and that is how the term is used here. EX1003, ¶¶92 and 169-170. As shown above, the '599 patent's "scan[n]" signal (in orange) is connected to the first transistor's (T32) gate and is the "scan line signal." See EX1001, 6:25-29.

Likewise, the orange signal in Fig. 33 connected to the gate of Kimura's first transistor is the claimed scan line signal. EX1003, ¶¶167-170 and ¶¶141-143. In Kimura, the term "first gate signal" (used 80+ times describing numerous figures) is what the '599 patent calls the "scan line signal." See, e.g., EX1002, Figs. 16-17 and accompanying discussion at [0422]-[0429]; EX1003, ¶¶167-170 and ¶¶141-143.

The "current scan line signal" (labelled "scan[n]") in the '599 patent controls the first transistor's gate. Similarly, Kimura discloses for numerous embodiments that the "gate electrode of the first transistor is electrically connected to the first

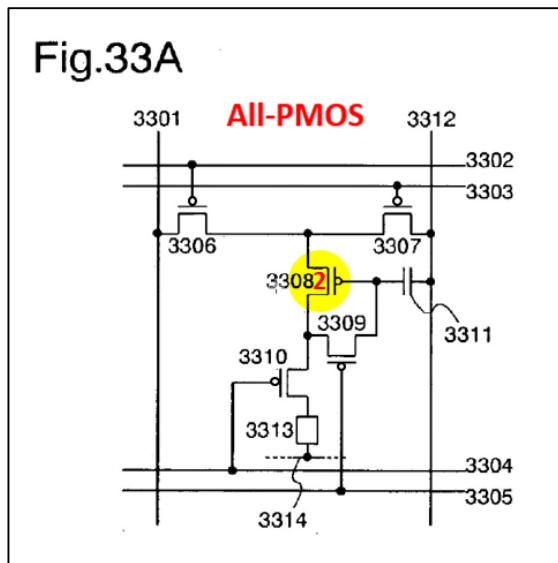
variable "n" denotes operations of the "current" pixel line (as opposed to "n-1" for operations on the previous pixel line). See, e.g., EX1001, 2:37-40 ("A scan signal applied to the n-th scan line is SCAN[n]. A scan line driven before the current scan line is the (n-1)th scan line. A scan signal applied to the (n-1)th scan line is SCAN[n-1].").

gate signal line.” EX1002, [0158]; *see also, e.g., id.*, [0176] (same); [0194] (same); [0211] (same); [0230] (same); and [0248] (same). A POSITA would understand the same gate connection applies to Fig. 33. EX1003, ¶¶167-170 and ¶¶141-143. As such, Kimura’s first transistor delivers a data signal voltage “in response to a current scan line signal” (*i.e.* in response to the “first gate signal” for the current row, which is the “i-th row”).⁷

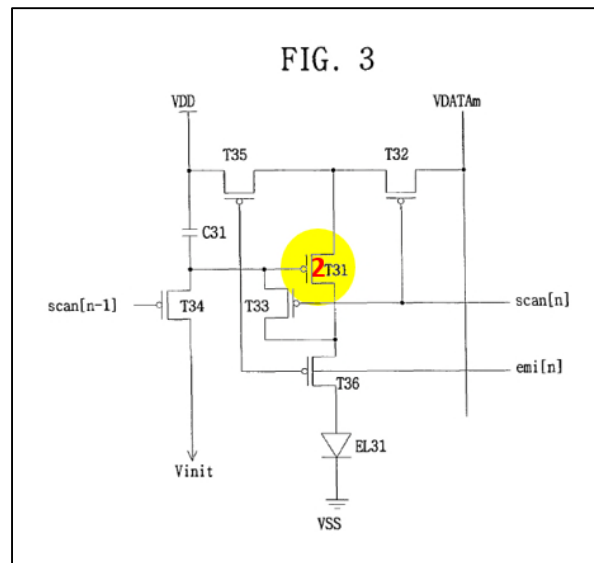
c. [7b]: “a second transistor for programming the data signal voltage and for generating a driving current in response to a programmed data signal when light is emitted;”

Kimura discloses claim element 7[b]. The “**second transistor**” in Kimura is the transistor labelled 3308 in Fig. 33. In ’599 patent Fig. 3 the “second transistor” is T31.

⁷ Instead of “n,” Kimura uses “i” as the index variable. *See, e.g.,* EX1002 Fig. 16B (“i” refers to current row, “i-1” refers to previous row, and “i+1” refers to subsequent row); EX1003, ¶169.



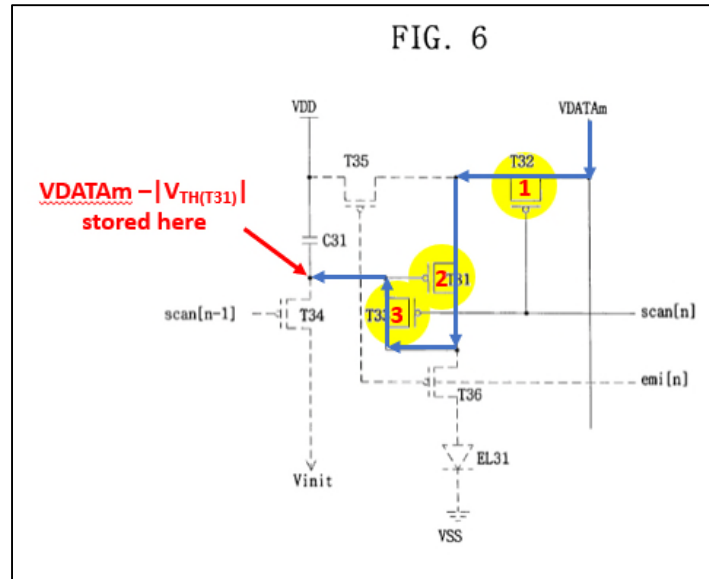
Kimura



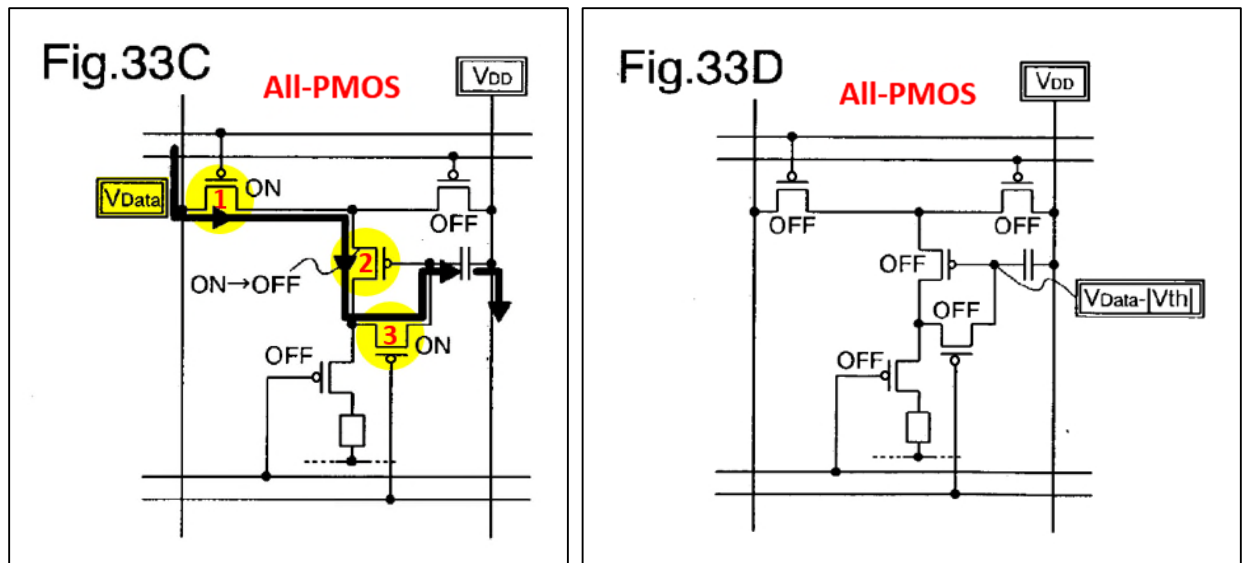
'599 Patent

The claimed “second transistor” performs the recited functions of (1) “programming the data signal voltage” and (2) “generating a driving current in response to a programmed data signal when light is emitted.” Each is addressed in turn.

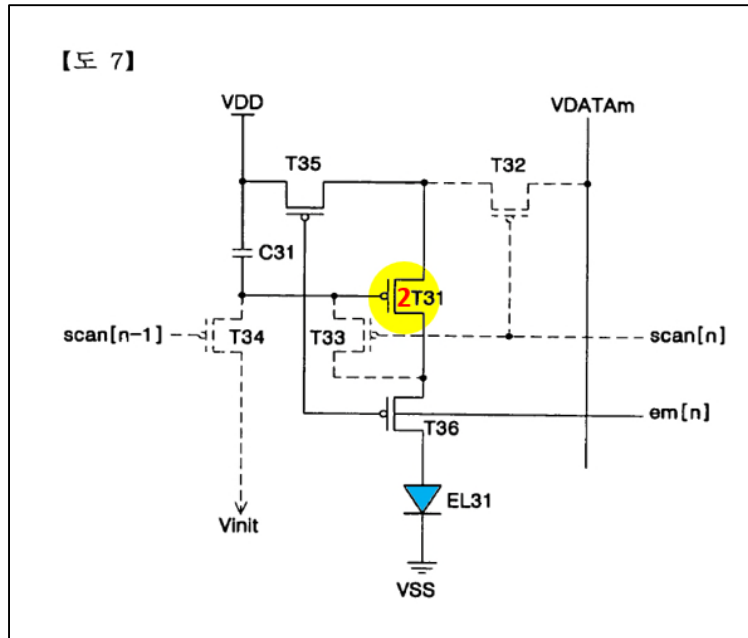
The '599 patent describes the claimed “**programming the data signal voltage**” operation in connection with Fig. 6 (the “data program operation”). *See* EX1001, 7:28-49. In summary, only the first (T32), second (T31), and third (T33) transistors are on during programming. *Id.* The second and third transistors are “connected in the form of a diode” such that the second transistor “program[s] the data signal voltage” in a self-compensating manner onto the capacitor. *See* EX1001, 7:35-49; EX1003, ¶¶174-175 and ¶¶113-127.



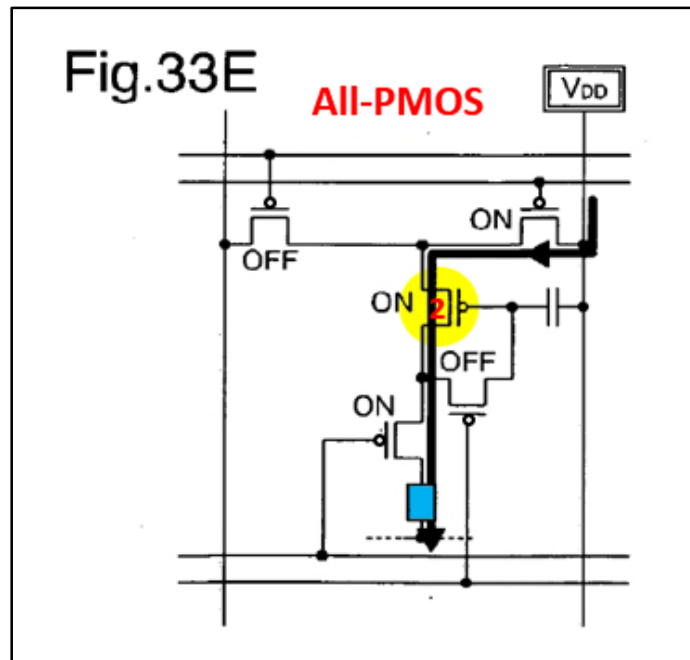
Kimura Fig. 33 likewise discloses “**programming the data signal voltage.**” In particular, Figs. 33C-33D (shown below) illustrate the programming operation. Kimura explains that, when the first, second, and third transistors are on (and all others off), current flows as shown in Fig. 33C. EX1002, [0655]. As a result, “the voltage between the gate and the source of the TFT 3308 [the second transistor] eventually becomes equal to the threshold voltage.” *Id.* The operation and role of the capacitor is discussed in more detail *infra* in connection with claim element 7[d] (“a capacitor for maintaining the data signal voltage programmed onto the second transistor”). Relevant here, just like the capacitor in ’599 patent Fig. 3, the capacitor in Kimura Fig. 33 charges to a self-compensating voltage (*viz.*, $V_{\text{Data}} - |V_{\text{th}}|$). See EX1002, Fig. 33D; EX1003, ¶¶135-137 and ¶180.



We now turn to the requirement that the second transistor “**generat[e] a driving current in response to a programmed data signal when light is emitted.**” This is shown and described in ’599 patent Fig. 7 which shows a “light-emitting operation” where a “light-emitting path [indicated by solid line] is formed.” EX1001, 7:50-55; *see also id.*, 6:27-31. As previously described, the “programmed data signal” that drives the second transistor (T31) is stored on the capacitor.

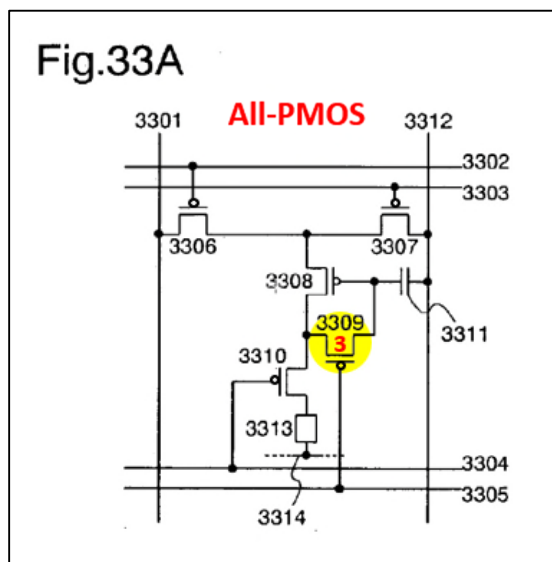


Kimura Fig. 33E illustrates the same operation where the second transistor generates the driving current for the light emitting diode when in light emitting mode. The solid black arrows in Fig. 33E illustrate current flowing through the “ON” transistors when in light emitting mode. *See* EX1002, [0656] (“The voltage between the gate and the source of the TFT3308 [shown in yellow] therefore exceeds the threshold voltage to cause it to turn on, so that electric current flows in the EL device 3313 to cause it to emit light.”). The “programmed data signal voltage” stored on the capacitor (*i.e.*, $V_{\text{Data}} - |V_{\text{th}}|$) activates the second transistor to push current through the light emitting diode to emit light.

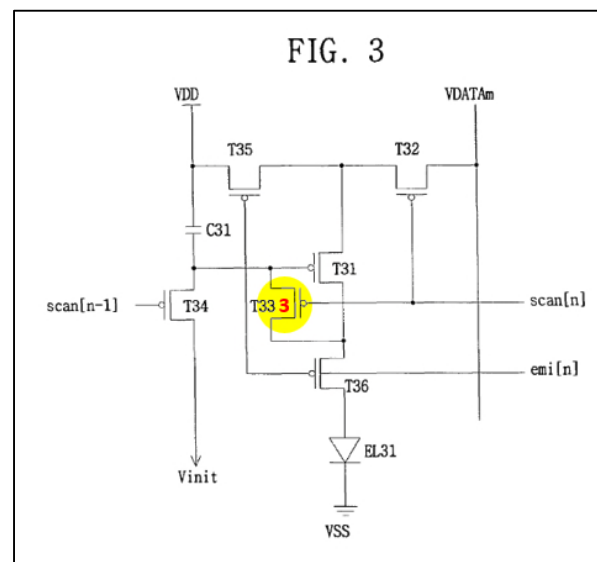


- d. [7c]: “a third transistor for providing the data signal voltage for the second transistor in response to the current scan signal;”

Kimura discloses claim element 7[c]. The “**third transistor**” in Kimura is labelled 3309 in Fig. 33. In '599 patent Fig. 3 the “third transistor” is T33.



Kimura



'599 Patent

The claimed “third transistor” performs the recited function of “providing the data signal voltage for the second transistor in response to the current scan signal.” This relates to the “programming” operation discussed in connection with Fig. 6 of the ’599 patent. *See supra* §IV.A; *see also* EX1001, 7:28-48. One aspect of Fig. 6 merits additional explanation here. In particular, the third transistor (T33) provides the data signal voltage for the second transistor “in response to the current scan signal.” To do so, the first transistor (T32) must also be on. EX1003, ¶¶105-106. This is accomplished by the shared control signal (scan[n])⁸ highlighted below in orange which is the claimed “current scan [line] signal.”

⁸ The ’599 patent specification uses “scan[n]” to identify the “current scan [line] signal.” *See, e.g.*, EX1001, 6:26-27; 6:36-47; 7:17-21; 7:30-39; 7:52; and 7:61.

signal” is a shared control signal that simultaneously controls both the first and third transistors.

Although Kimura Fig. 33 does not expressly show a shared signal that controls both the first and third transistors, Kimura explains that “the TFT 3306 [first transistor] and the TFT 3309 [third transistor] in FIG. 33A are controlled to turn on and off at the same time. They can therefore be controlled by using the same gate signal line 3452, as shown in FIG. 34B.” *Id.*, [0659]. A version of Fig. 34B highlighting the shared “current scan signal” line for the first and third transistors is shown below. In response to the signal on line 3452 (the “current scan line”), the third transistor (labelled 3458 in Fig. 34B and 3309 in Fig. 33A) charges the capacitor and provides the gate of the second transistor (labelled 3457 in Fig. 34B and 3308 in Fig. 33A) with the data signal voltage. It would have been obvious to a POSITA to use the shared signal of Fig. 34B in Fig. 33. EX1003, ¶185.

Fig.34B

The diagram illustrates an All-PMOS circuit. The power supply is 3V (3451) and the ground is 3454. The circuit includes a PMOS network (3455, 3456, 3457, 3458, 3459) and an NMOS network (3460, 3462). The output node (3463) is connected to the PMOS network and the NMOS network. The circuit is labeled "All-PMOS" in red text.

Based on the circuit operation and explanation accompanying Figs. 33 and 34, a POSITA would understand that the signal on wire 3452 is controlling the operation of the current cycle, not a previous or subsequent cycle. EX1003, ¶185 (including footnotes).

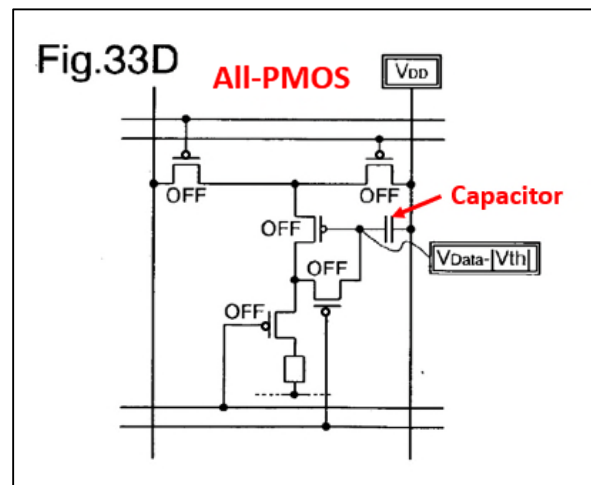
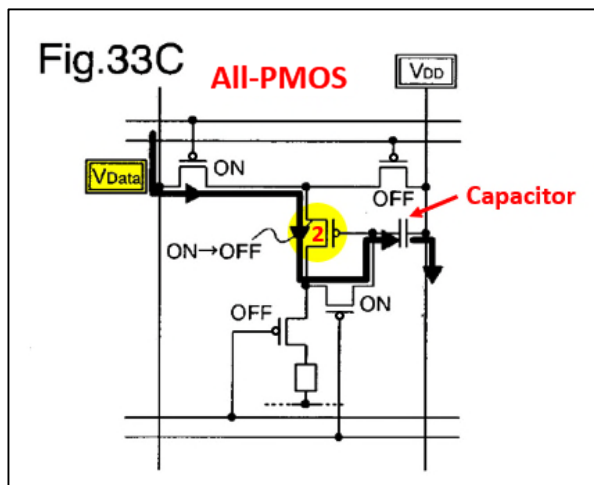
Although the signal on shared line 3452 is not expressly named in the figure, that is irrelevant and (as explained *supra*) a POSITA would understand that it is Kimura’s “first gate signal.” EX1003, ¶185 and ¶¶141-143. In any event, because the shared signal line 3452 simultaneously controls both the first and third transistors in the manner claimed, it qualifies as a “current scan signal.” Thus, Kimura discloses claim element 7[c].

e. [7d]: “a capacitor for maintaining the data signal voltage programmed onto the second transistor;”

Kimura discloses claim element 7[d]. This is shown in Kimura Figs. 33C and 33D. The black arrows in Fig 33C show current flow onto the capacitor which charges the capacitor (*i.e.* “program[s]” it) with the “data signal voltage.”

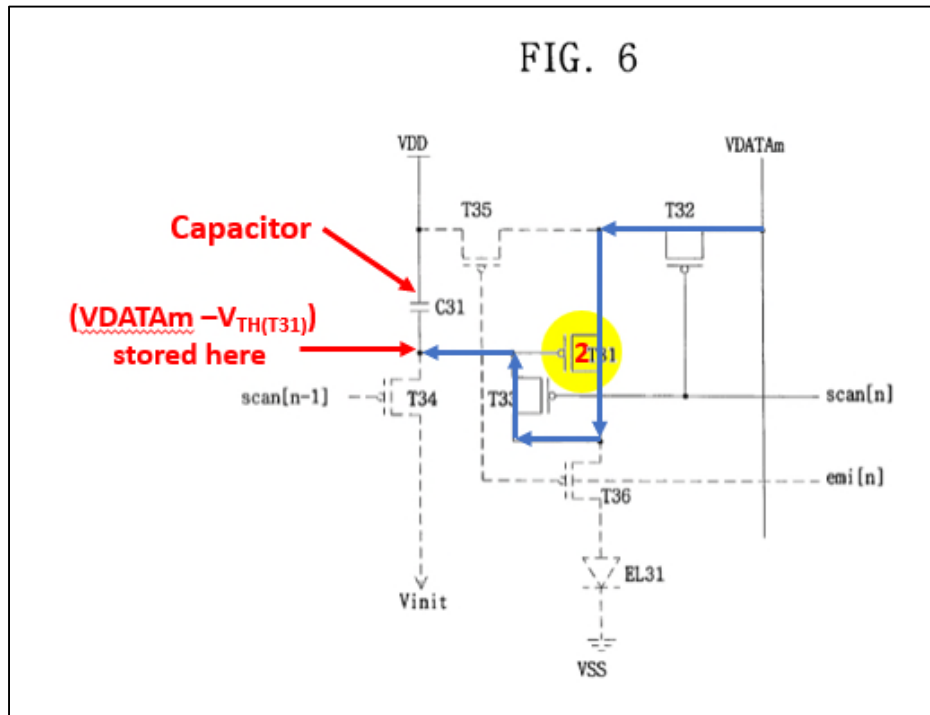
EX1002, [0655] (“[E]lectric charge moves as shown in FIG. 33C. The voltage between the source and the drain of the TFT 3308 [second transistor]...eventually becomes equal to the threshold voltage, at which point the TFT 3308 [second transistor] turns off as shown in FIG. 33D.”). As was well-known in the art at the relevant time, capacitors store charge and maintain a voltage until discharged.

EX1003, ¶37. Kimura’s capacitor—connected to the gate of second transistor 3308—maintains the “data signal voltage” on that node. As shown in Fig. 33D, the capacitor’s voltage across its electrodes equals $V_{\text{Data}} - |V_{\text{th}}|$. EX1003, ¶¶190-192 and ¶¶134-137. Thus, Kimura satisfies claim element 7[d].



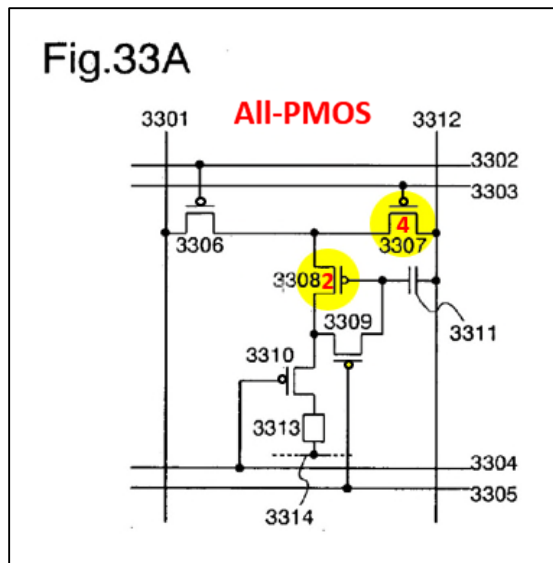
Kimura’s disclosure for claim element 7[d] aligns with the claimed

embodiment in '599 patent Fig. 6 (reproduced below) in which the “capacitor for maintaining the data signal voltage programmed onto the second transistor” functions in the same way. *See* EX1001, 7:28-49; *see also supra* §IV.A (discussing programming operation).

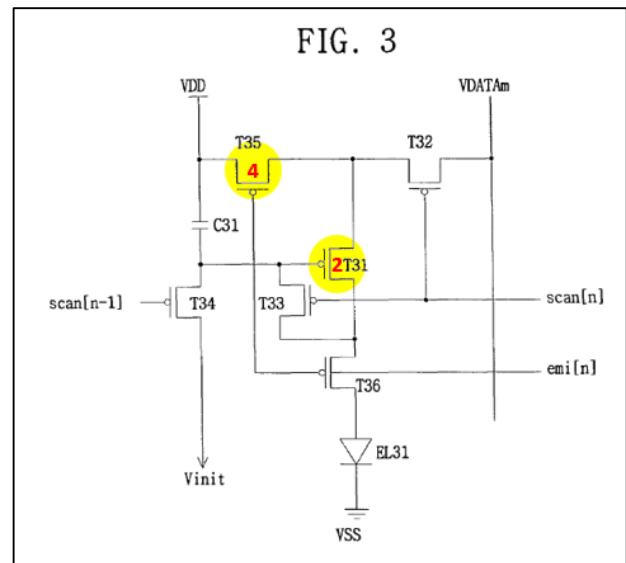


f. [7e]: “a fourth transistor for delivering a power supply voltage to the second transistor when the light is emitted;”

Kimura discloses claim element 7[e]. The “**fourth transistor**” in Kimura is labelled 3307 in Fig. 33A and is T35 in '599 patent Fig. 3. Claim element 7[e] references the second transistor so it is also identified.

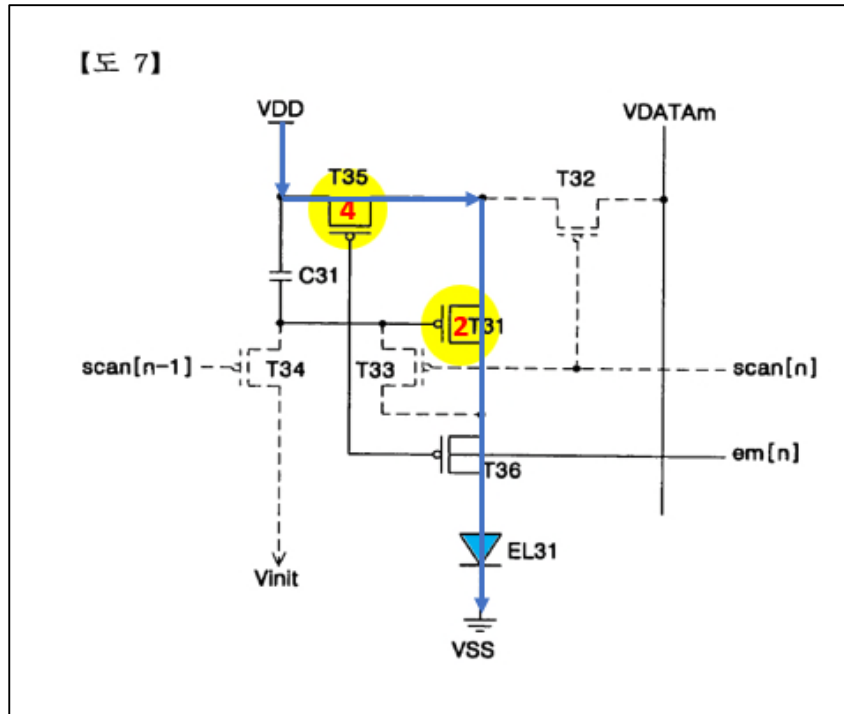


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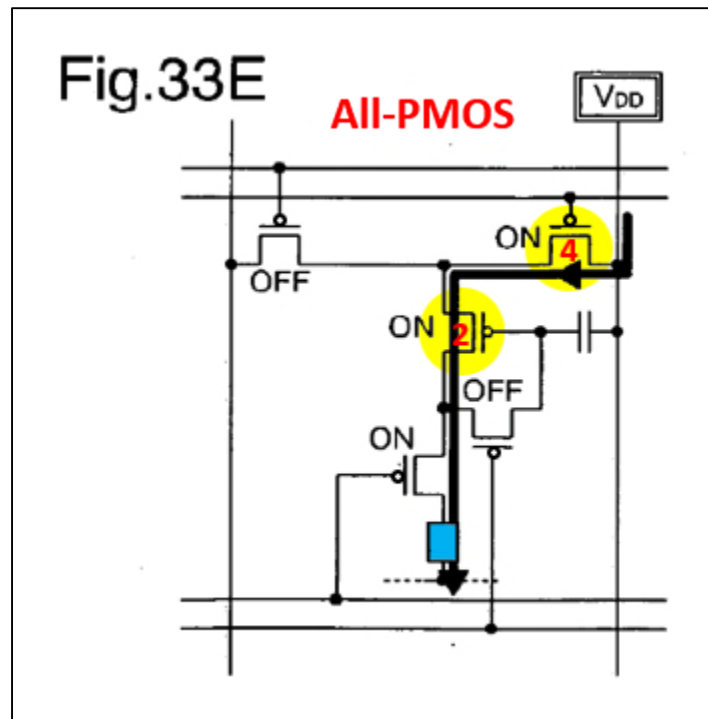


'599 Patent

The claimed “fourth transistor” performs the recited function of “delivering a power supply voltage to the second transistor when the light is emitted,” which is shown in '599 patent Fig. 7 where current flows as “indicated by the solid line” during light emission. EX1001, 7:50-65. During this operation, the fourth transistor (T35) is on and delivers the VDD power supply voltage to the second transistor (T31). *Id.*, 7:55-57.

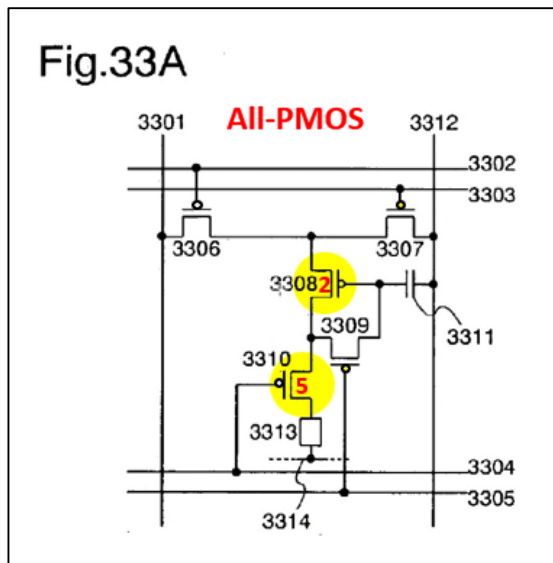


The fourth transistor 3307 in Kimura Fig. 33 operates in like manner as shown in Kimura Fig. 33E which illustrates current flow with a black line. EX1002, [0656]. Kimura explains that “[t]he TFTs 3307 [fourth transistor] and 3310 [fifth transistor] then turn on. The electric potential of a source region of the TFT 3308 [second transistor] increases from V_{Data} to VDD as the TFT 3307 [fourth transistor] turns on.” *Id.* This results in “electric current flows in the EL device 3313 to cause it to emit light, as shown in FIG. 33E.” *Id.*; *see also* EX1003, ¶¶194-198. Thus, Kimura discloses “a fourth transistor for delivering a power supply voltage to the second transistor when the light is emitted.”

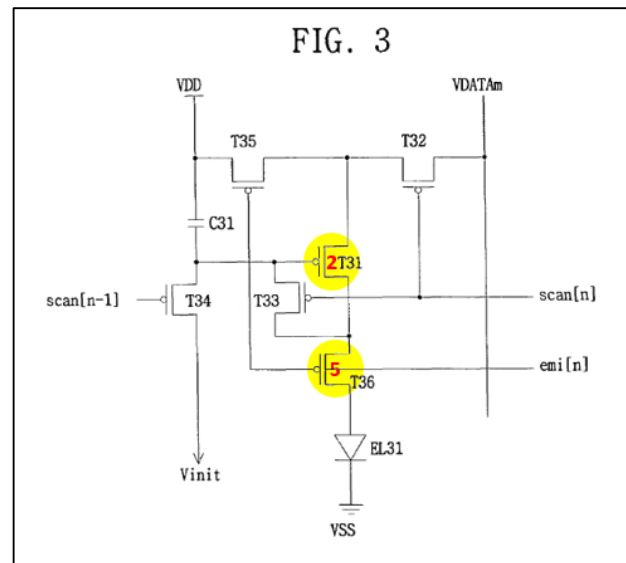


- g. [7f]: “a fifth transistor for delivering the driving current, provided from the second transistor, in response to the data signal voltage when the light is emitted;”**

Kimura discloses claim element 7[f]. The “**fifth transistor**” in Kimura is labelled 3310 in Fig. 33A (and T36 in ’599 patent Fig. 3). Because claim element 7[f] references the second transistor, it is also identified.

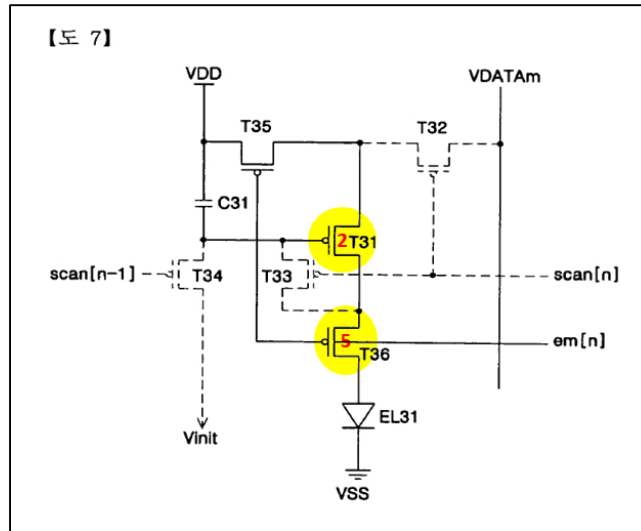


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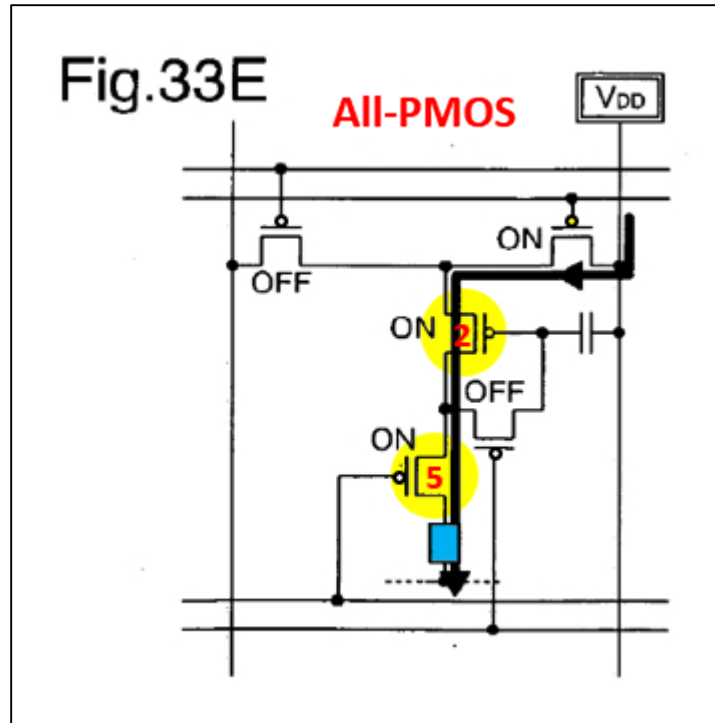


'599 Patent

The claimed “fifth transistor” performs the recited function of “delivering the driving current, provided from the second transistor, in response to the data signal voltage when the light is emitted.” In ’599 patent Fig. 7 (showing the “light-emitting operation”), current flow is “indicated by the solid line.” EX1001, 7:50-65. The ’599 patent explains that “a driving current [is] generated in response to the data signal voltage applied to the gate of driving transistor T31 [second transistor].” *Id.*, 7:61-65. The fifth transistor (T36) is in series with the second transistor (T31) and thus “deliver[s] the driving current[] from the second transistor” to the light emitting element. *Id.*, 7:50-65. The driving current is “in response to the data signal voltage” because that voltage is stored on the capacitor and controls the second transistor. *Id.*; EX1003, ¶¶199-203 and ¶¶101-102.



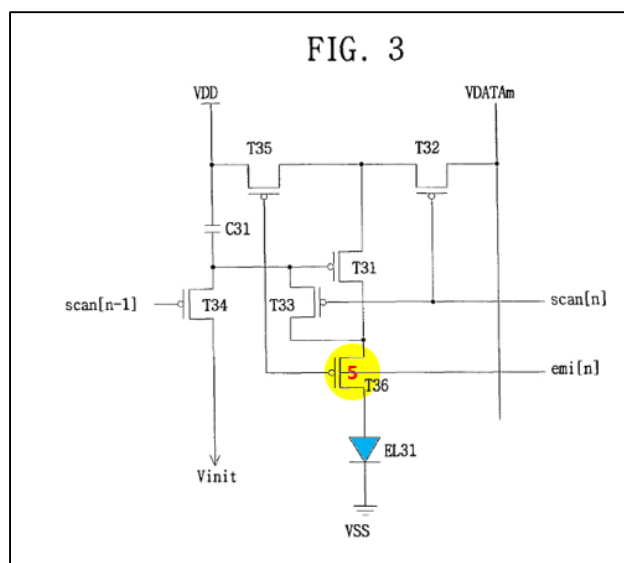
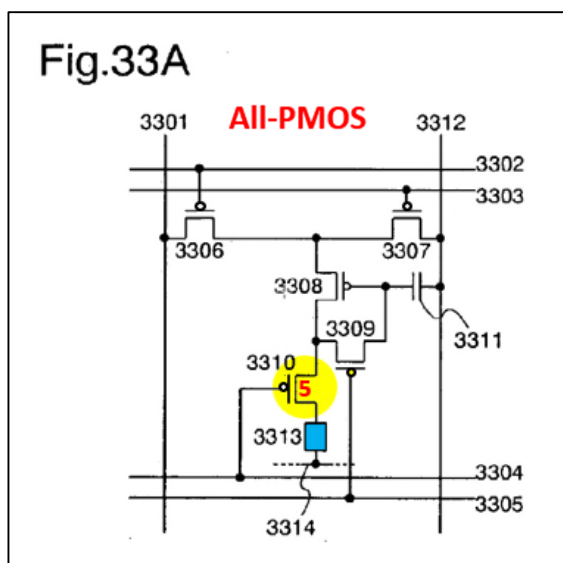
The fifth transistor 3310 in Kimura Fig. 33 likewise performs the recited function of claim element 7[f] as shown in Fig. 33E where the black line illustrates current flowing through the second and fifth transistors. EX1002, [0656]. After the fourth and fifth transistors turn on, “[t]he voltage between the gate and the source of the TFT 3308 [second transistor] exceeds the threshold voltage to cause it to turn on, so that electric current flows in the EL device 3313 to cause it to emit light.” *Id.* The fifth transistor is connected in series with the second transistor such that the fifth transistor delivers the drive current provided by the second transistor. EX1003, ¶202. The driving current is “in response to the data signal voltage” because that voltage is stored on the capacitor and controls the second transistor. *Id.*, [0655] (explaining that electric charge flows onto the capacitor in Fig. 33C); *see also* EX1003, ¶202 and ¶¶136-140. Thus, Kimura satisfies claim element 7[f].



h. [7g]: “an electroluminescent element for emitting light corresponding to the driving current delivered through the fifth transistor”

Kimura discloses claim element 7[g]. The “**electroluminescent element for emitting light**” in Kimura is labelled 3313 in Fig. 33 and EL31 in ’999 patent Fig.

3. Kimura explains that “electric current flows in the EL device 3313 to cause it to emit light.” EX1002, [0656]. Elsewhere, Kimura explains the “EL” refers to “electroluminescent.” *See, e.g., id.*, [0002]. Because claim element 7[g] references the fifth transistor, it is also identified.



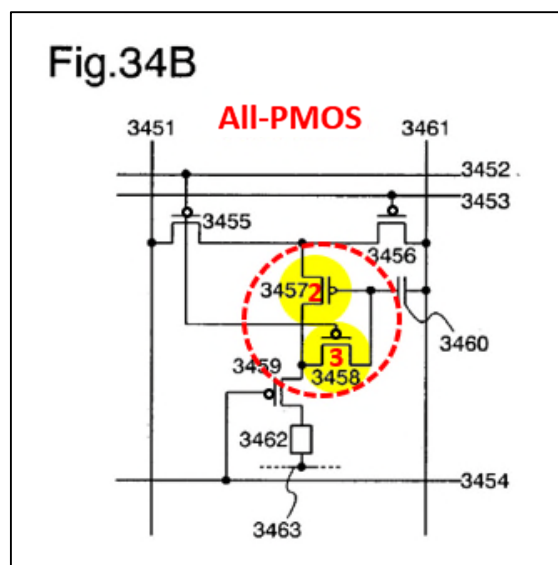
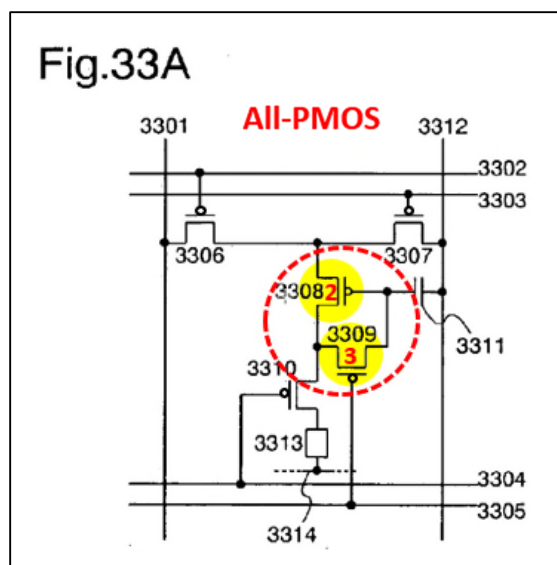
In both Kimura Fig. 33 and '599 patent Fig. 3, the claimed electroluminescent element emits light “corresponding to the driving current delivered through the fifth transistor” because the second transistor (which regulates the drive current) is in series with the fifth transistor (which merely acts as an on/off switch). Due to this circuit configuration, the current driven by the second transistor is delivered through the fifth transistor to the electroluminescent element. EX1003, ¶¶204-207.

The amount of light emitted from an OLED electroluminescent element varied based on the current driven through it. *See, e.g.*, EX1002, [0359] (discussing problems with the “dispersion in the brightness of the EL devices” due to differences in current flow), [0390]; EX1001, 4:22-24 (“An electroluminescent element emits light corresponding to the driving current....”); *see also* EX1003, ¶85. And the amount of current driven was determined, in part, by the gate voltage

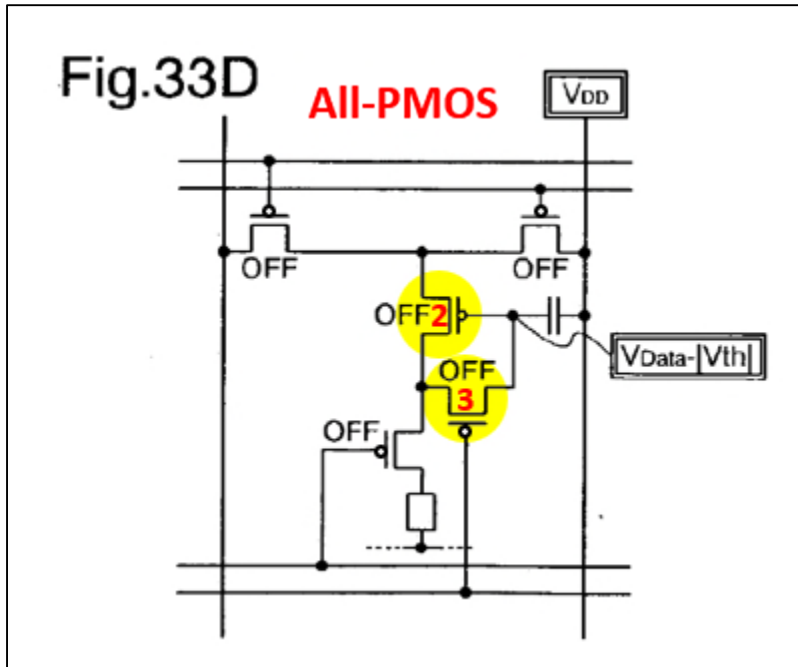
applied to the driving transistor. EX1002, [0359], [0654] (second transistor “behaves as a driver TFT for performing control of electric current supplied to an EL device 3313.”); EX1003, ¶¶205-206. Indeed, fixing problems caused by this characteristic was a motivation in Kimura. EX1002, [0390]. Accordingly, the amount of light emitted by the electroluminescent element “correspond[s] to” the drive current delivered through the fifth transistor. EX1003, ¶¶205-206. Thus, Kimura satisfies claim element 7[g].

- i. [7h]: “wherein the third transistor connects the second transistor in the form of a diode in response to the current scan signal so that the second transistor detects and compensates its threshold voltage deviation in itself.”*

Kimura discloses claim element 7[h]. As an initial matter, the circuit configuration highlighted in Figs. 33A and 34B between second transistor 3308 and third transistor 3309 is referred to as a “diode connection” configuration. EX1002, [0379]. And, as Kimura explains, “the TFT 3308 [second transistor] exhibits the behavior as a diode connected TFT when the TFT 3309 [third transistor] is on.” EX1002, [0654].



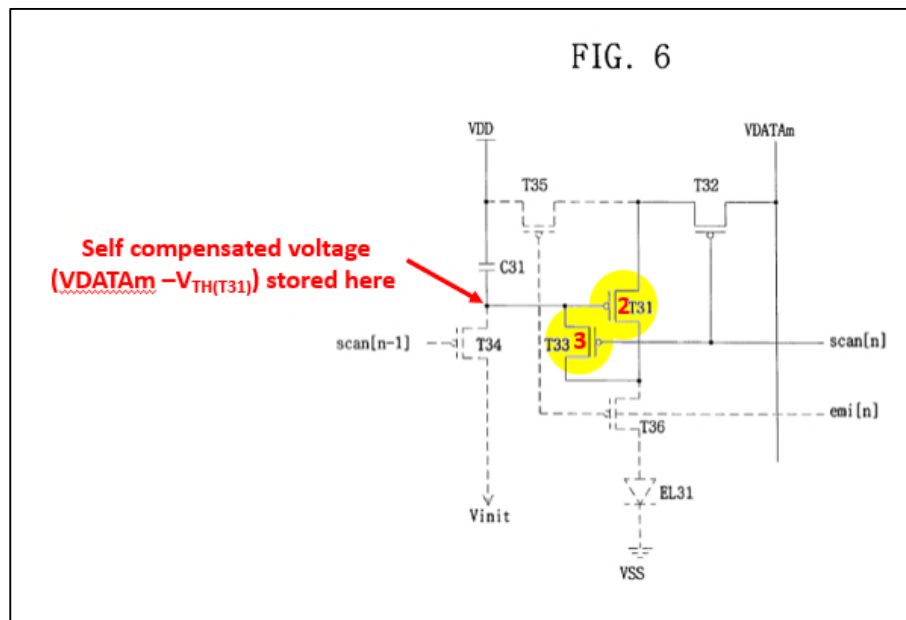
Kimura's third transistor (3309 in Fig. 33A and 3458 in Fig. 34B) connects the second transistor (3308 in Fig. 33A and 3457 in Fig. 34B) in the form of a diode "in response to the current scan signal" (*i.e.*, only when the signal controlling the gate of third transistor is asserted). EX1003, ¶¶211-212 and ¶¶80-81. Fig. 33C illustrates how current flows onto the capacitor when the second and third transistors operate in diode connected mode. EX1002, [0655] ("the TFT 3309 [third transistor]...turn[s] on, and the TFT 3308 thus behaves as a diode connected TFT."). And Fig. 33D shows the result in which a self-compensated voltage (*i.e.*, $V_{Data}-|V_{th}|$) is stored on the capacitor. EX1002, [0655]; EX1003, ¶¶135-137 and ¶213.



This is precisely why Fig. 33 includes the third transistor—*i.e.*, to help self-compensate for threshold voltage variation of the second transistor. EX1002, [0652]-[0657]. The same self-compensating operation applies to Fig. 34B, with the only difference being that the first and third transistors share a control signal (which, as discussed *supra*, is the “current scan signal”). EX1002, [0659]; EX1003, ¶¶212-213. Self-compensation avoids undesirable variations in light emission from adjacent pixels. *Id.*

Notably, the second transistor (3308 in Fig. 33A and 3457 in Fig. 34B) only acts as a diode when the third transistor (3309 in Fig. 33A and 3458 in Fig. 34B) is activated by the control signal on its gate (*viz.*, the “current scan signal”). See EX1002, Figs. 33C, 33D, and 34B; EX1003, ¶¶135-137 and ¶213. Thus, Kimura satisfies claim element 7[h].

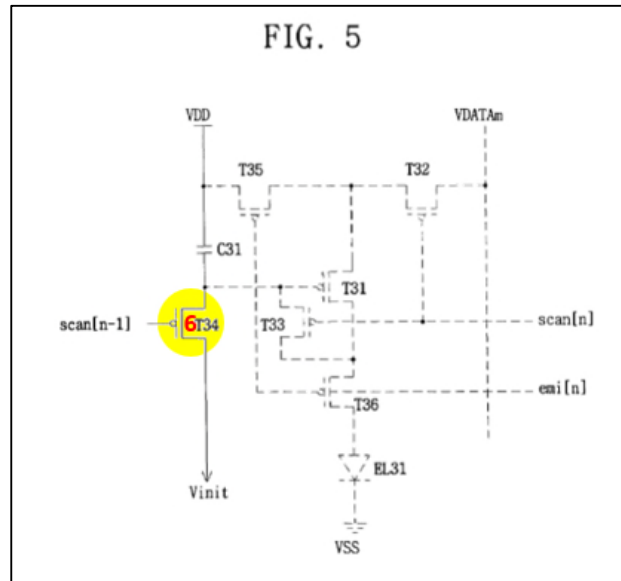
Moreover, the claimed embodiment of the '599 patent has the same diode-connected transistor configuration. *See* '599, Fig. 6 and col. 7:28-49 (second transistor T31 is diode connected by third transistor T33 when the third transistor is activated by the scan[n] signal (*i.e.*, the claimed “current scan signal”)); *see also id.*, 4:34-41 and 8:29-31 (“[D]riving transistor T31 in the present invention can self-compensate the threshold voltage deviation by detecting its own threshold voltage.”); EX1003, ¶211. In operation, the diode connected configuration of the claimed embodiment in the '599 patent is the same as Fig. 34B in Kimura.



2. Claim 8

Claim 8 depends from claim 7 and further requires “a sixth initialization transistor for discharging the data signal voltage stored in the capacitor in response to a scan signal just before the current scan signal upon initialization.” Kimura

renders this claim limitation obvious. Before explaining Kimura's operation, we review the claimed embodiment of the '599 patent, in which the "sixth transistor" is T34 as shown in Fig. 5 below. EX1003, ¶¶218-220.

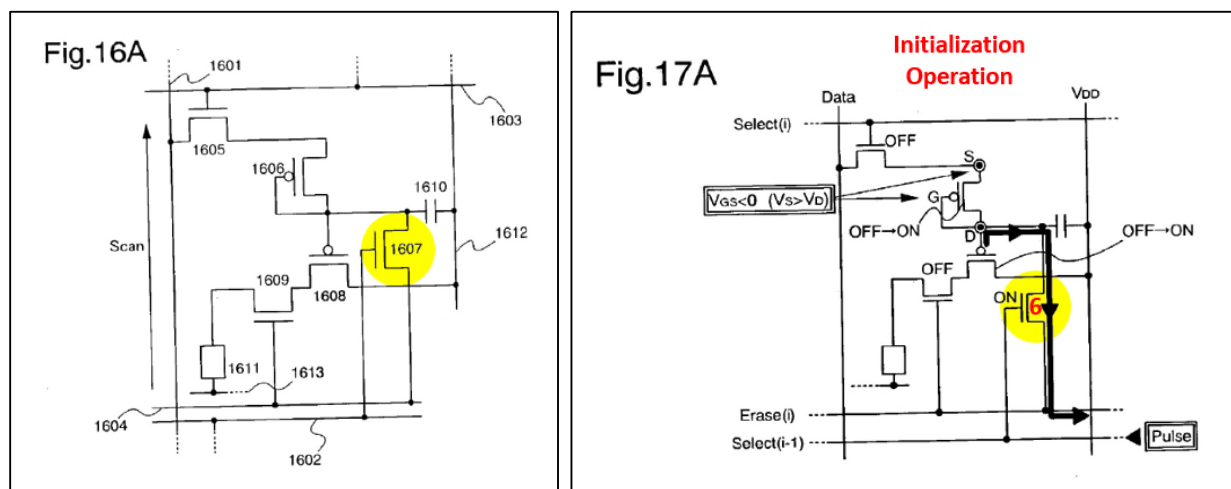


The purpose and operation of sixth transistor T34 is described at col. 7:15-27. In summary, the sixth transistor (T34) is active during an "initialization operation" when the control signals for other transistors are unasserted. EX1001, 7:15-17. As shown in Fig. 5, the sixth transistor (T34) is connected to the capacitor and, during initialization, discharges the capacitor from a residual voltage to "Vinit" voltage. *Id.*; EX1003, ¶¶218-220. Because the sixth transistor's gate is controlled by the scan[n-1] signal (*i.e.*, the previous scan signal), the sixth transistor performs the discharge function "in response to a scan signal just before the current scan signal upon initialization." *See* EX1001, 7:6-8; 7:15-27.

Turning now to Kimura, incorporating the initialization transistor from Figs.

16-17 into Fig. 33 renders claim 8 obvious. EX1003, ¶¶221-230. Kimura discloses that the fifth transistor in Fig. 33 “can also be used as an erasure [transistor]” that resets the capacitor voltage to a default initialization value. EX1002, [0658]. This approach, however, is less desirable because (as shown in Fig. 33B) during initialization the current discharges through the light emitting element causing undesired light emission. *See* EX1002, Fig. 33B; [0665].

One way Kimura solves this problem is by including a dedicated initialization transistor as shown and discussed in Figs. 16-17, where transistor 1607 (labelled “sixth transistor” in Fig. 17A for reference) drains the capacitor without current running through the light emitting element. EX1002, [0426].



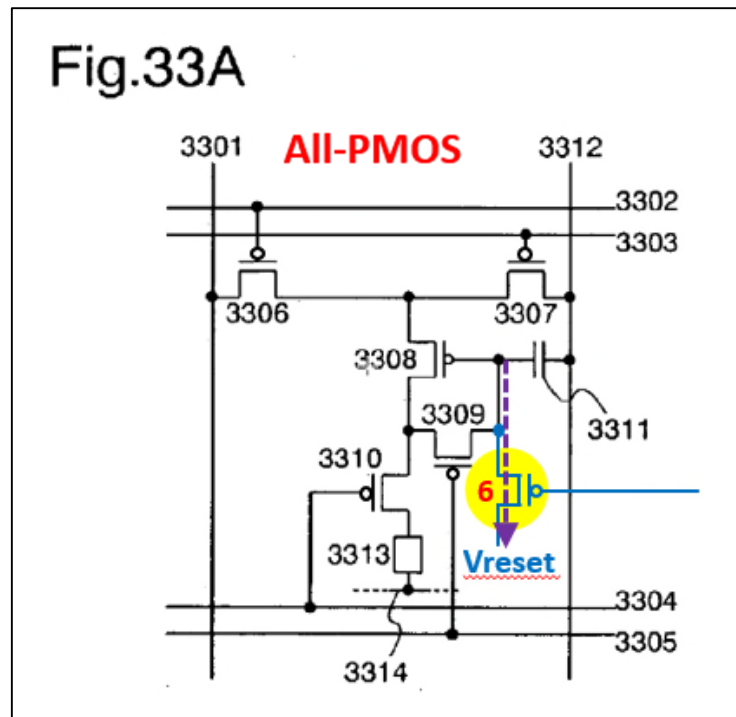
Operation of the initialization transistor (1607) is discussed in Kimura [0422]-[0429]. In summary, transistor 1607 resets the voltage on capacitor 1610. *Id.*, [0429]. The “gate electrode of the TFT 1607 is connected to the gate signal line 1602 of an (i-1)th row.” EX1002, [0423]. Just like the capacitor in Fig. 33,

the capacitor in Figs. 16-17 “stores [a voltage] applied to the gate electrode of the TFT 1608 during the sustain (light emitting) period.” *Id.*; EX1003, ¶¶221-223. The function of transistor 1607 is to initialize/reset the capacitor by discharging it, as shown in Fig. 17A. EX1002, [0426]; *see also id.*, [0425] (referring to the initialization voltage as “VReset”).

Kimura explains that “to perform initialization of a certain row, [the circuit] utilizes the selection pulse of the gate signal line of the previous row in controlling the TFT 1607.” EX1002, [0429]; *see also id.*, [0426] (“The TFT 1607 turns on when the first gate signal line 1602 of the (i-1)th row is selected.”). This initialization operation provides a clean slate for subsequently charging the capacitor to the appropriate voltage (*i.e.*, $V_{\text{Data}} - V_{\text{th}}$) for driving current during light emission. *Id.*, [0427]. This operation (shown in Fig. 17B) is similar to that shown in Figs. 33C-33D. EX1003, ¶¶221-230 and ¶¶155-158.

A POSITA would have been motivated to combine the initialization approach disclosed in Kimura Figs. 16-17 with Kimura Fig. 33 by adding a dedicated initialization transistor (*i.e.*, the sixth transistor as illustrated below). EX1003, ¶¶221-230 and ¶¶155-158. Such an approach is readily applicable to the baseline circuit of Fig. 33. *Id.*; *see also id.*, ¶¶141-143. Indeed, when discussing Fig. 33, Kimura expressly teaches that “the erasure [transistor] can be placed in any location, provided that it is a location at which electric current supplied to the

EL device can be cut off at an arbitrary timing.” EX1002, [0658]. Thus, a POSITA would have been motivated to place the initialization transistor discussed in Figs. 16-17 in the same location (*i.e.*, directly connected to the capacitor) in Fig. 33. EX1003, ¶¶221-230 and ¶¶155-158. Modified Fig. 33 below shows the “sixth transistor” (*i.e.*, initialization transistor) in blue as a PMOS device. Given that all other transistors in the All-PMOS implementation are PMOS devices, a POSITA would have been motivated to implement the initialization transistor as a PMOS device. *See* EX1004 (Kimura ’798) at 12:30-49 (“[E]very TFT can be N-channel type TFTs or all TFTs can be P-channel type TFTs....[I]t is often advantageous in manufacturing when all TFTs are of the same type.”); *see also* EX1002, [0418] (“[T]here are no particular limitations placed on the polarity of the [initialization transistor]”). Just like Fig. 17B, during initialization in Fig. 33A the sixth transistor turns on and creates a current path (shown by purple arrow) that discharges the capacitor to an initialization/reset value with no current passing through the light emitting element. EX1002, ¶[0666]; *see also id.*, [0425] (discussing “VReset” voltage); EX1003, ¶¶221-230 and ¶¶155-158.



Additional reasons a POSITA would have made this modification include:

- Extensive discussion of the dedicated initialization transistor approach in Figs. 16-17, including detailed control signal/timing waveforms. See Kimura [0420]-[0430]; EX1003, ¶¶141-143.
- The simplicity of the solution and ease of implementation (*viz.*, no other transistors or circuit elements require changing) creates a reasonable expectation of success. EX1003, ¶229. And Kimura Fig. 36 (discussed *infra*) confirms this by showing a similar modification vis-à-vis initialization transistor 3612 (placed in another location).
- Kimura's express teachings about the flexible location of the transistor and the fact that adding a dedicated initialization transistor solves a known drawback in Fig. 33 (*i.e.*, spurious light emission during initialization). EX1002, [0658] and [0666].

- Initializing/resetting circuits (including OLED drivers) was a common and well-known practice at the relevant time. EX1003, ¶155. While other initialization protocols were available (discussed elsewhere in Kimura), selecting one was a mere design choice and there were limited options/locations for initialization transistor placement. EX1003, ¶158.
- Adding the initialization transistor as described in Fig. 16-17 does not require any additional control signals. *See* EX1002, [0422] (only two total control signals needed for pixel circuit); *id.*, [0429] (“[T]o perform initialization of a certain row, it utilizes the selection pulse of the gate signal line of the previous row in controlling the [sixth transistor]...The number of signal lines can be kept to a minimum.”).

It would have been obvious to a POSITA to control the sixth transistor with “a scan signal just before the current scan signal is applied.” EX1003, ¶¶223-229. Indeed, the timing diagram of Kimura Fig. 16B shows exactly this—initializing a given row occurs when the “first gate signal” of the “(i-th) row” (*i.e.* the claimed current scan signal) is asserted. EX1002, [0423] (“A gate electrode of the TFT 1607 [sixth transistor] is connected to the gate signal line 1602 of an (i-1)th row.”); EX1003, ¶¶223-229. As Kimura explains for Figs. 16-17, “to perform initialization of a certain row, [the circuit] utilizes the selection pulse of the gate signal line of the previous row in controlling the TFT 1607 [sixth transistor].” EX1002, [0429]; *see also id.*, [0423] and [0426]. Indeed, the only change needed

to use Fig. 16B's control signals for the modified Kimura circuit is to use active-low signaling. EX1003, ¶223 and ¶¶141-143.

One reason a POSITA would have been motivated to use “a scan signal just before the current scan signal” (*i.e.*, first gate signal of “i-1th” row) to control the sixth transistor is because that signal already exists in the circuit. EX1003, ¶228. As such, it is a simple and elegant solution requiring no new signals. Indeed, when introducing this simplified control scheme, Kimura contrasts a more complex scheme requiring a “third gate signal line.” *See* EX1002, [0421]-[0422] (“In Embodiment Modes 2 and 3, erasure TFT control is performed using an additional third gate signal line” resulting in increased “surface area occupied by wirings.”).

Kimura further observes that by reusing an existing signal “[t]he number of signal lines can be kept to a minimum and a high aperture ratio[] can be obtained.” EX1002, [0429]. Further, Fig. 16B shows that the first gate signal is never simultaneously asserted on two rows, making use of the previous scan signal a convenient solution for controlling the initialization transistor.

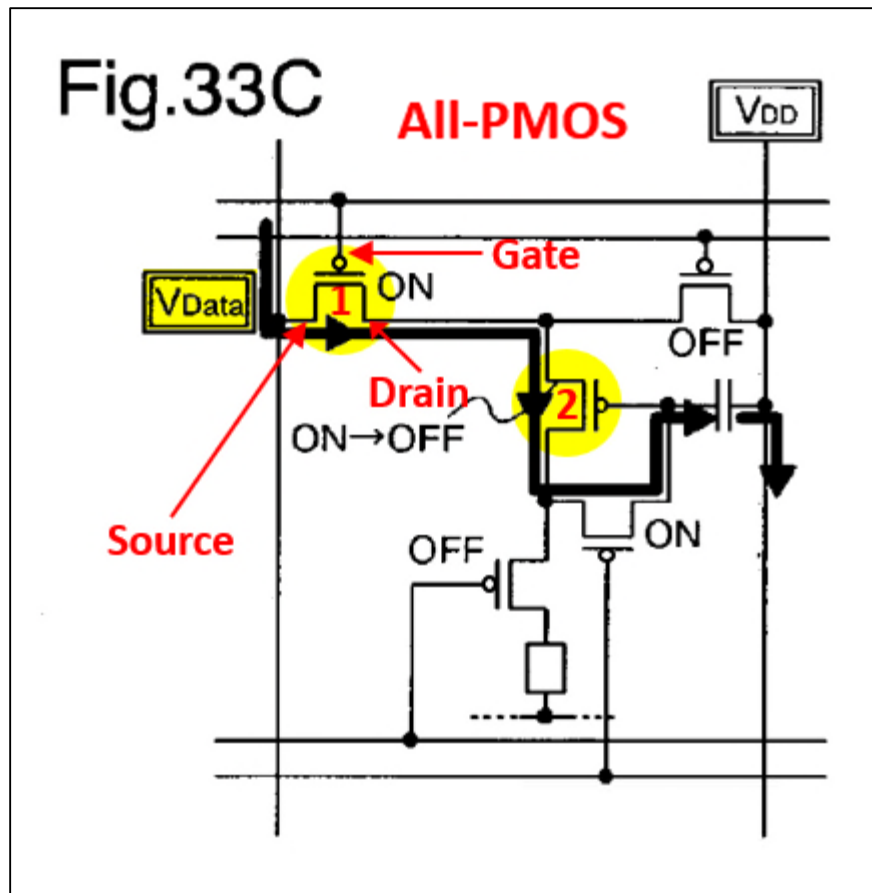
Thus, Kimura Fig. 33 combined with the initialization transistor 1607 from Fig. 16 renders claim 8 obvious.

3. Claim 9

Claim 9 depends from claim 7 and further requires that “the first transistor is composed of a PMOS transistor including a gate to which the current scan line

signal is applied, a source to which the data signal voltage is applied, and a drain coupled to the second transistor.” In all-PMOS Kimura Fig. 33, the first transistor is PMOS. The reasons for using an all-PMOS implementation are discussed *supra* §§III.B and VI.A. As discussed for claim elements 7[a], 7[c], and 7[h] *supra*, the first transistor’s gate is connected to the current scan line signal. EX1003, ¶¶231-235.

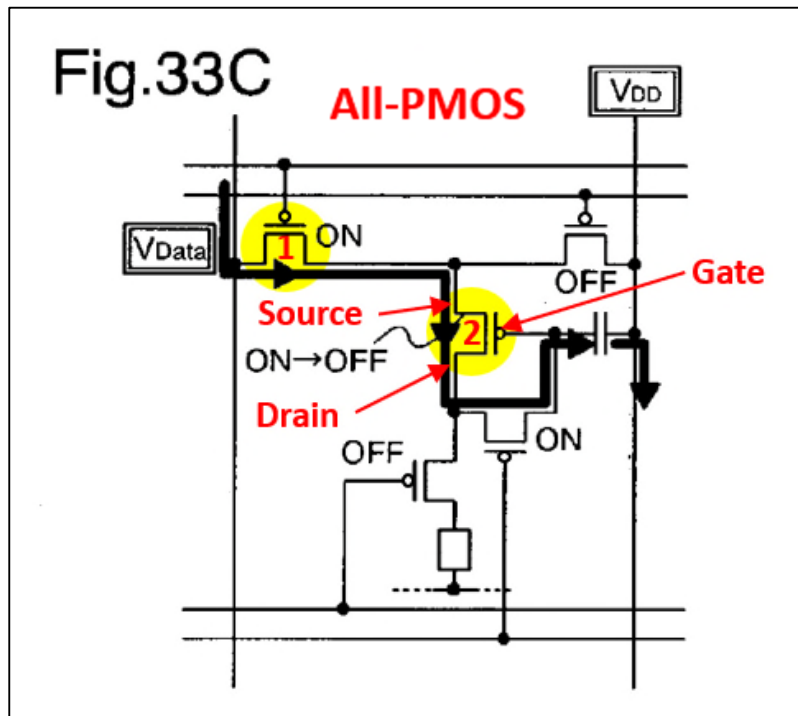
The PMOS “source” is the terminal with higher voltage. *See supra* §III.B; EX1003, ¶¶50-53. The black arrow in Kimura Fig. 33C shows current flowing from V_{Data} (higher voltage) through the first transistor, meaning the “data signal voltage” is connected to the first transistor’s source and the drain is coupled to the second transistor. EX1003, ¶¶233-234.



4. Claim 10

Claim 10 depends from claim 7 and further requires that the “second transistor is composed of a PMOS transistor including a gate coupled to one terminal of the capacitor, a source coupled to the first transistor, and a drain coupled to the electroluminescent element.” Kimura Fig. 33 discloses this limitation. As shown below, the second transistor’s gate is coupled to a capacitor terminal. The PMOS “source” has higher voltage than the drain. *See supra* §III.B; EX1003, ¶¶50-53. The current flow in Kimura 33C confirms the source/drain labelling below. EX1003, ¶¶237-238. Accordingly, Kimura discloses the claimed

electroluminescent element coupling just as '599 patent Fig. 3. EX1003, ¶¶236-239.



5. Claim 11

Claim 11 depends from claim 10 and further requires that “the third transistor is composed of a PMOS transistor including a gate to which the current scan signal is applied, and a drain and a source which are coupled to the gate and the drain of the second transistor, respectively, so that the third transistor connects the second transistor in the form of a diode in response to the current scan signal to self-compensate a threshold voltage of the second transistor.” Claim element 7[h] already explained the diode connection configuration and operation of the second and third transistors (including the current scan signal’s role) to perform threshold

voltage self-compensation of the second transistor. Thus, claim 11 merely adds that the third transistor is PMOS with specified source/drain connections as illustrated in Kimura Fig. 33C below.

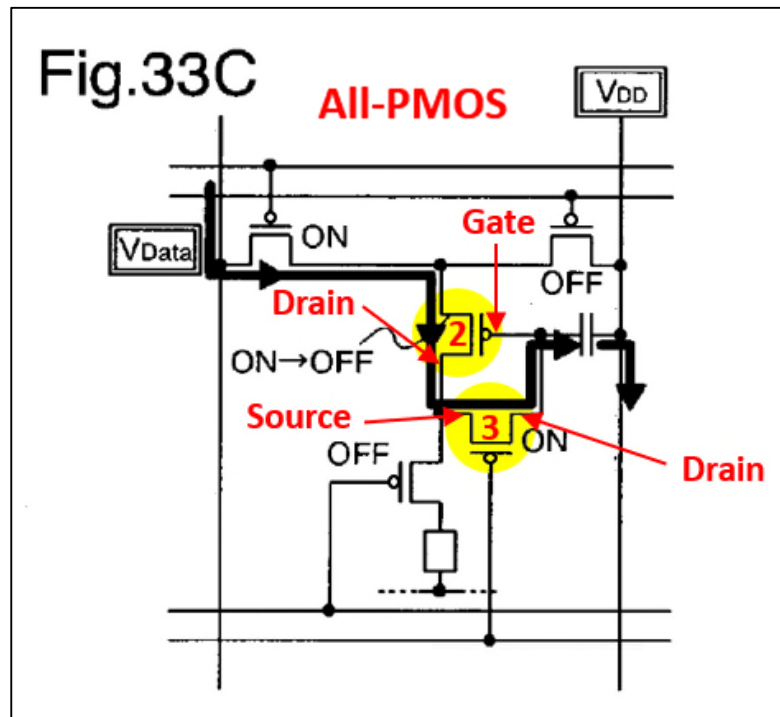
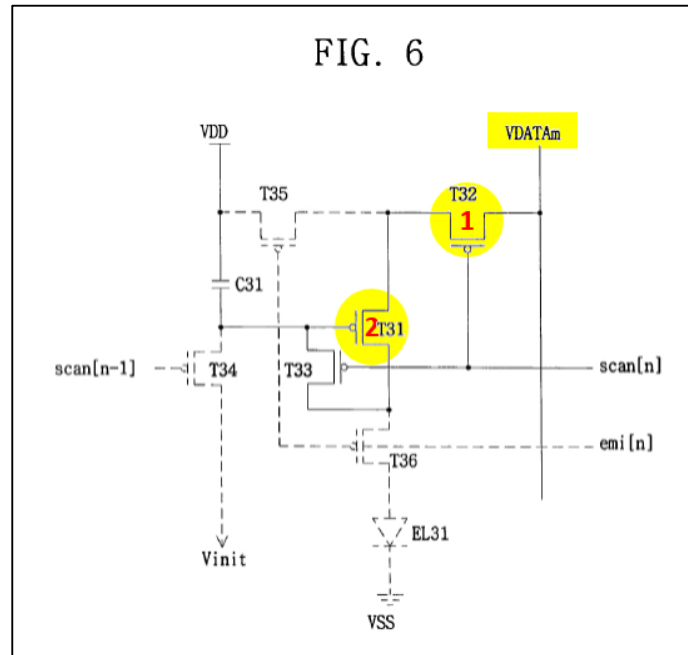


Fig. 33C shows current flow when the capacitor is charging which confirms the respective source/drain labels of the second and third transistors. EX1003, ¶¶240-246. Thus, the third transistor's drain is connected to the second transistor's gate and the third transistor's source is connected to the second transistor's drain. *Id.*

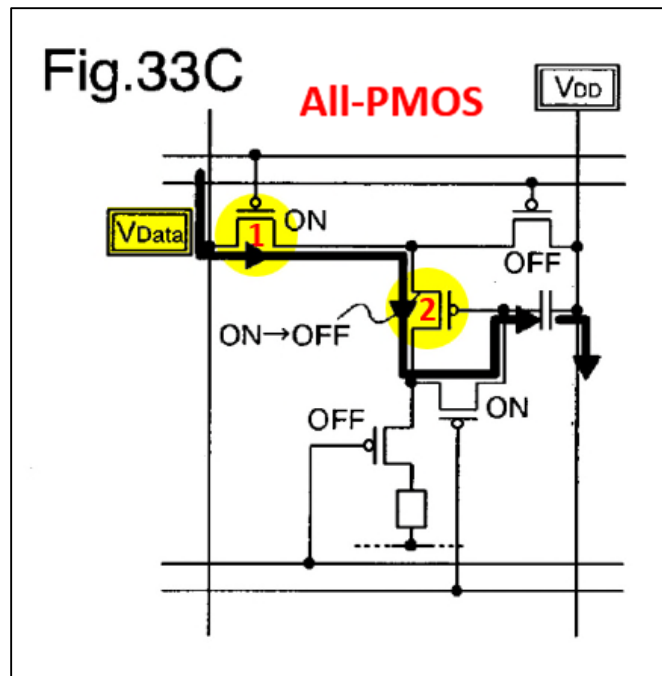
6. Claim 12

Claim 12 depends from claim 7 and further requires “a voltage source for providing the data signal voltage through the first transistor for the second transistor.” In '599 patent Fig. 6, the “voltage source for providing the data signal

voltage” is VDATAm connected to the first transistor’s (T32) source. EX1003, ¶248.



Kimura likewise discloses “a voltage source for providing the data signal voltage through the first transistor for the second transistor.” As shown in Fig. 33C below, the voltage source V_{Data} passes through the first transistor to the second transistor. *See also* EX1002, [0655] (“the [first transistor] turns on, and an image signal V_{Data} is input.”); EX1003, ¶¶247-250. A POSITA would understand that V_{Data} is a voltage source (and not a current source). EX1003, ¶249.



7. Claim 13

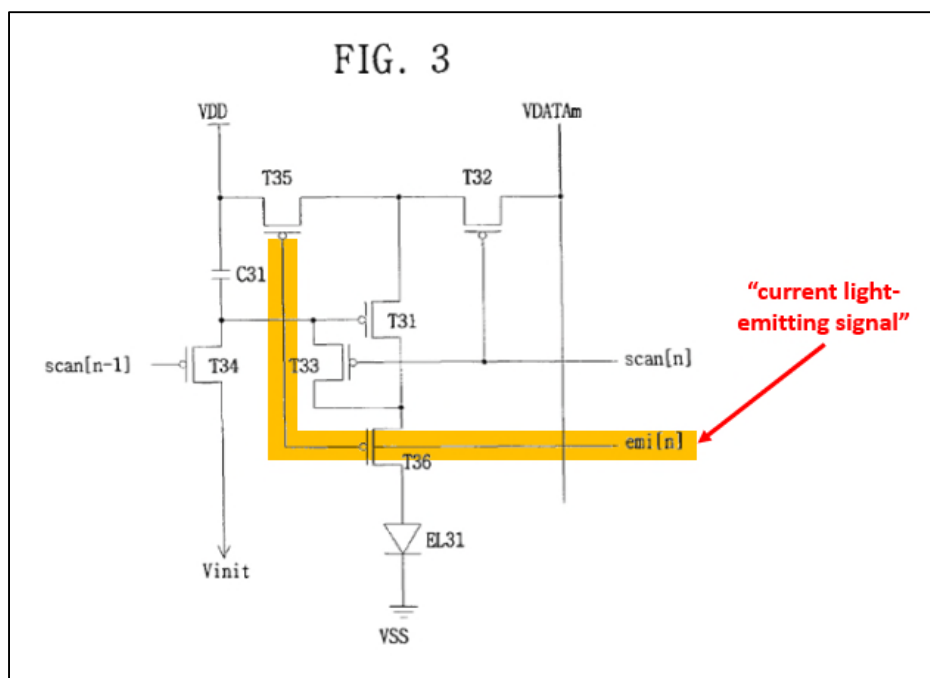
Claim 13 depends from claim 7 and further requires that “the fourth transistor is composed of a PMOS transistor including a gate to which the current light-emitting signal is applied, a source to which a power supply voltage is applied, and a drain coupled to the second transistor; and the fifth transistor is composed of a PMOS transistor including gate to which the current light-emitting signal is applied, a source coupled to the second transistor, and a drain coupled to the electroluminescent element.” In summary, claim 13 requires that both the fourth and fifth transistors are PMOS devices and specifies the connections for their respective gate, source, and drain terminals. The fourth and fifth transistors are already PMOS in the all-PMOS version of Fig. 33. And the all-PMOS version

of Kimura Fig. 36, discussed below, renders claim 13 obvious.

Claim 13 requires that “the current light emitting signal” control the gates of both the fourth and fifth transistors. This aspect of claim 13 merits elaboration. As an initial matter, the modifier “*current*” in this context simply distinguishes the light emitting signal for a particular line of pixels from the signals for adjacent lines.⁹ *See, e.g.* EX1001, 2:17-32; EX1003, ¶256 (and n.22).

As the claimed embodiment of the ’599 patent shows, the “light emitting signal” is a shared control signal that simultaneously (1) activates the fourth (T35) and fifth (T36) transistors so current flows through the light emitting element during light emission and (2) turns them off during other circuit operation (*i.e.* during initialization and programming). *See, e.g.*, EX1001, Fig. 7 and 7:50-65; *see also id.*, Fig. 4 (showing that emi[n] is not asserted during initialization or programming).

⁹ The ’599 patent specification’s “emi[n]” shorthand refers to “emission” and the variable “n” denotes operations on the “current” pixel line (as opposed to “n-1” for operations on the previous pixel line). *See, e.g.*, EX1001, 2:37-40).



In Kimura, the “second gate signal” (used 100+ times to describe operation of numerous figures) is the claimed “current light emitting signal.” *See, e.g.*, EX1002, Figs. 16-17 and accompanying discussion at [0422]-[0429]; EX1003, ¶¶256 and ¶¶141-143. As shown, for example, in the timing diagram of Fig. 16B, the “light emitting” period for each row is controlled by the corresponding “second gate signal” for that row. EX1003, ¶¶256-259 and ¶¶141-143. Similar to how the ’599 patent uses the index “n” to distinguish between adjacent lines of pixels, Kimura uses the index “i” for the same purpose. *See, e.g., id.* (referring to the “(i-1)th row” of pixels, the “i-th” row of pixels, and the “(i+1)th” row of pixels).

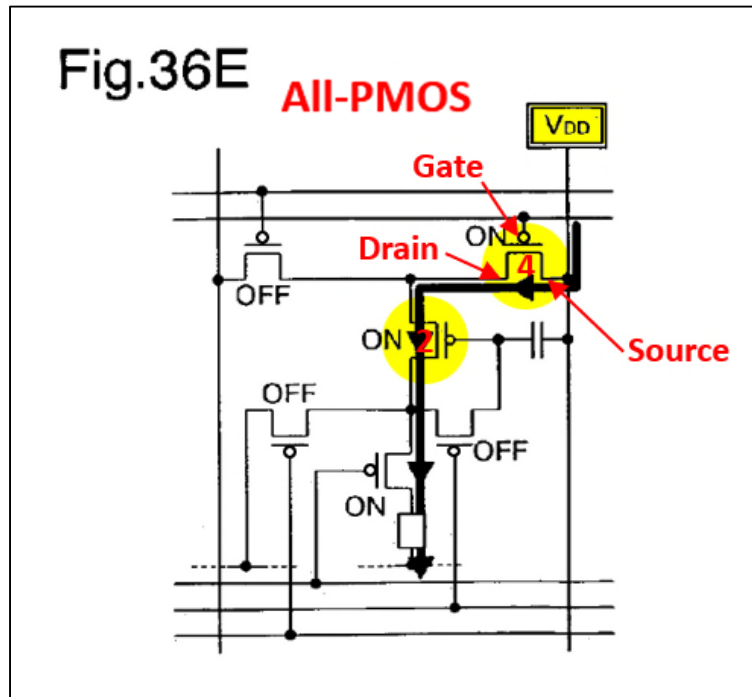
Although Fig. 33B shows the fourth and fifth transistors controlled by different signals (*viz.*, fourth transistor OFF while fifth transistor ON), that is not the case for Fig. 36. EX1003, ¶257. In all operation states of Fig. 36 (*viz.*, Fig.

36B (initialization), Figs. 36C-D (programming), and Fig. 36E (light emission)), the fourth and fifth transistors are always ON/OFF together. EX1003, ¶257. Thus, a POSITA would have understood (or at least found it obvious) that Kimura uses a shared light-emitting signal to control them. EX1003, ¶256-259. Kimura itself provides one reason for doing so—reducing the number of control lines improves aperture ratio. *See, e.g.*, EX1002, [0429]; *see also id.*, [0421]-[0422] (control scheme with fewer signals reduces “surface area occupied by wirings in a pixel”). Additionally, the fourth and fifth transistors must both be active during light emission, otherwise the electroluminescent element will not emit light. EX1003, ¶¶138-140; *see also* EX1002, [0659] (signals “turn[ing] on and off at the same timing...can therefore be controlled by using the same gate signal line”). This, too, would have naturally led a POSITA to use a shared light-emitting signal. EX1003, ¶¶258-259.

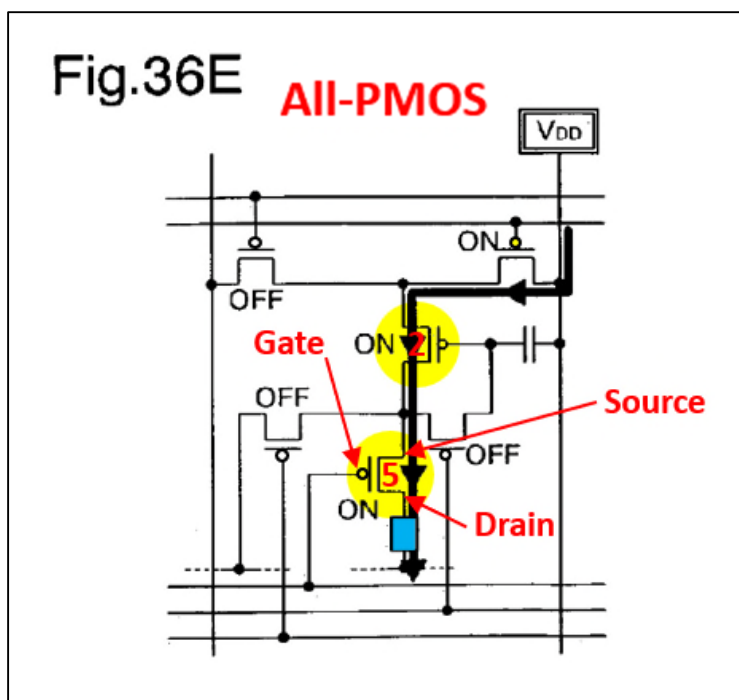
Moreover, Kimura discloses a timing diagram and control scheme utilizing only two signals (*i.e.*, first and second gate signals which map to the claimed “scan line signal” and “light emitting signal” respectively). *See* EX1002, Figs. 16-17 and explanation at [0420]-[0429]; EX1003, ¶259. This disclosure would have motivated a POSITA to use a shared light emitting signal for the fourth and fifth transistors and provided a reasonable expectation of success. EX1003, ¶259.

Claim 13 also requires that “a power supply voltage is applied” to the fourth

transistor's source and that the "drain [is] coupled to the second transistor." In Fig. 36E below, the fourth transistor's source is coupled to V_{DD} (power supply voltage) and its drain is coupled to the second transistor. EX1003, ¶261. The source and drain labels are confirmed by the current flow direction. EX1003, ¶261.



Claim 13 further requires that the fifth transistor's "source [is] coupled to the second transistor" and that its "drain [is] coupled to the electroluminescent element." In Fig. 36E below, the fifth transistor's source connects to the second transistor and the fifth transistor's drain connects to the electroluminescent element. EX1003, ¶263. The black current flow arrow confirms the source and drain labels annotations are correct. EX1003, ¶263. Thus, Kimura renders claim 13 obvious.



8. Claim 14

Kimura renders obvious independent claim 14 for largely the same reasons as independent claim 7. Like claim 7, claim 14 is an apparatus claim requiring five transistors (with same numbering as claim 7), a capacitor, and an electroluminescent element arranged in a particular manner. Each limitation is addressed below.

- a. [Claim 14 Preamble]: “A pixel circuit in an organic light emitting device, comprising:”**

The preambles of claims 7 and 14 are identical and met for the same reasons.

- b. [14a]: “an electroluminescent element for emitting light in response to an applied driving current;”**

Kimura satisfies claim element 14[a] as explained for claim element 7[g].

- c. [14b]: “a first transistor for delivering a data signal voltage in response to a current scan line signal;”***

Claim elements 14[b] and 7[a] are identical and met for the same reasons.

- d. [14c]: “a second transistor for generating a driving current to drive the electroluminescent element in response to the data signal voltage;”***

Claim element 7[b] includes all requirements of claim element 14[c] and is disclosed by Kimura for the same reasons. Both require a “second transistor for...generating a driving current.” And a POSITA would understand claim element 14[c]’s requirement of “driv[ing] the electroluminescent element in response to the data signal voltage” is substantively the same as claim element 7[b]’s requirement that the “driving current” be generated “in response to a programmed data signal when light is emitted.” EX1003, ¶¶276-277. In particular, “light is emitted” from an electroluminescent element when driven by a “driving current.” *Id.* That claim element 7[b] has additional requirements beyond claim element 14[c] is irrelevant.

- e. [14d]: “a third transistor for connecting the second transistor in the form of a diode in response to the current scan signal to self-compensate a threshold voltage of the second transistor;”***

Claim elements 7[c] (“third transistor...”) and 7[h] (“the third transistor connects the second transistor in the form of a diode in response to the current scan signal so that the second transistor detects and compensates its threshold voltage

deviation in itself”) collectively include all requirements of claim element 14[d]. A POSITA would understand that “self-compensat[ing] a threshold voltage of the second transistor” (14[d]) is the same as the “second transistor detect[ing] and compensat[ing] its threshold voltage deviation in itself” (7[h]). EX1003, ¶¶278-280. Accordingly, Kimura discloses claim element 14[d] as explained for claim element 7[c] and 7[h].

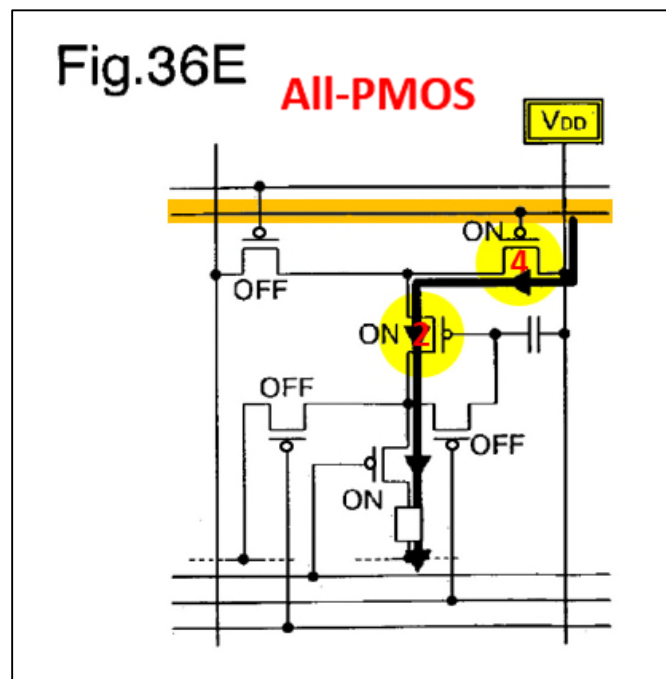
f. [14e]: “a capacitor for storing the data signal voltage delivered to the second transistor;”

Claim elements 14[e] and 7[d] are nearly identical. In claim element 14[e] the capacitor “stor[es]” the data signal voltage “delivered” to the second transistor, whereas in claim element 7[d] the capacitor “maintain[s]” the data signal voltage “programmed onto” the second transistor. The slight semantic difference makes no difference vis-à-vis Kimura and claim elements 14[e] and 7[d] are satisfied for the same reasons. EX1003, ¶¶281-282.

g. [14f]: “a fourth transistor for delivering a power supply voltage to the second transistor in response to a current light-emitting signal;”

Claim elements 7[e] and 14[f] both require “a fourth transistor for delivering a power supply voltage to the second transistor” and this aspect is met for the same reasons. Claim element 14[f] additionally requires the fourth transistor to deliver a power supply voltage to the second transistor “in response to a current light-

emitting signal.” Kimura teaches this in Fig. 36E by the signal line highlighted in orange which controls the fourth transistor’s gate to deliver V_{DD} (power supply voltage) to the second transistor. As discussed for claim 13, it would have been obvious to a POSITA to use the second scan signal (the “current light-emitting signal”) to control the fourth transistor. EX1003, ¶¶283-285.



- h. [14g]: “a fifth transistor for providing the driving current, provided from the second transistor, for the electroluminescent element in response to the current light-emitting signal.”*

Claim elements 7[f] and 14[g] both require “a fifth transistor for providing the driving current, provided from the second transistor.” Claim element 14[g] requires that the fifth transistor provide the driving current “for the electroluminescent element” and claim element 7[f] requires that the fifth transistor

provide the driving current “when the light is emitted.” Kimura discloses, and a POSITA would understand, that “light is emitted” from the “electroluminescent element” when a driving current passes through it. *See, e.g.*, EX1002, [0656]; EX1003, ¶¶286-288. Thus, Kimura discloses these aspects of claim elements 14[g] and 7[f] for the same reasons.

Claim element 14[g] additionally requires that the fifth transistor provide drive current “in response to the current light-emitting signal.” Kimura satisfies this requirement as explained for claim 13 vis-a-vis a shared control signal for the fourth and fifth transistors.¹⁰ In summary, Kimura renders obvious claim element 14[g] as explained for claim 13 and claim element 7[f].

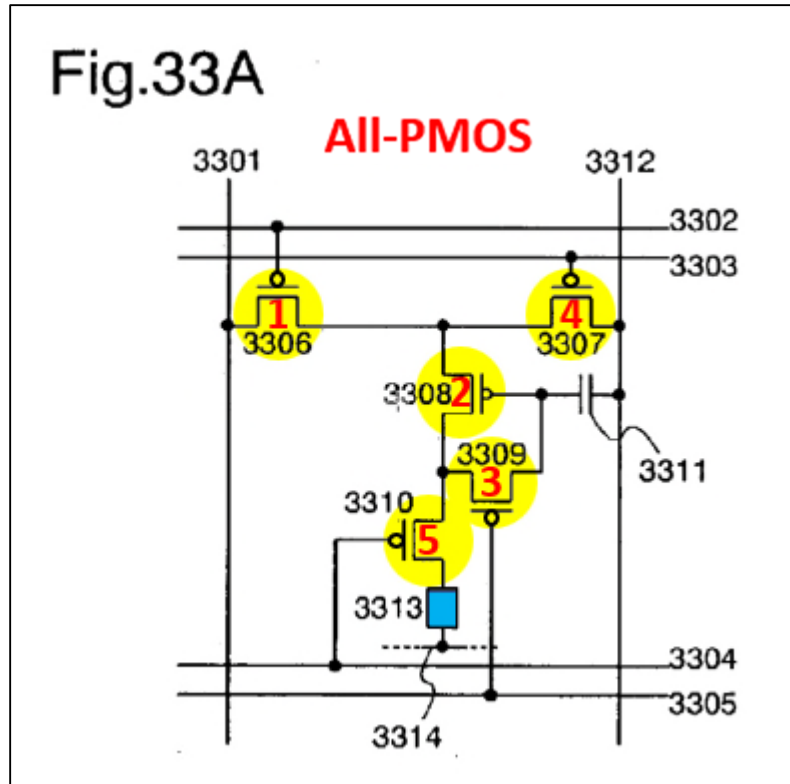
9. Claim 15

Kimura renders obvious independent claim 15 for largely the same reasons as independent claim 7. Like claim 7, independent claim 15 is an apparatus claim requiring five transistors (with same numbering as claim 7), a capacitor, and an electroluminescent element arranged in a particular manner. It is helpful at the

¹⁰ Because claim element 14[g] refers to “*the* current light emitting signal,” the signal controlling the fifth transistor is the same “current light emitting signal” (introduced in claim element 14[f]) that controls the fourth transistor.

outset to understand that the primary difference between claims 7 and 15 is that all transistors in claim 15 must be PMOS based on the recited source/drain/gate connections. Even though claim 7 is not limited to PMOS devices, Kimura's all-PMOS embodiment was used for consistency. Accordingly, much of the claim 7 patentability analysis applies to claim 15.

A holistic view of Kimura Fig. 33 identifying the claimed transistors is repeated for reference and used throughout the claim 15 analysis.



a. [Claim 15 Preamble]: “A pixel circuit in an organic light emitting device, comprising:”

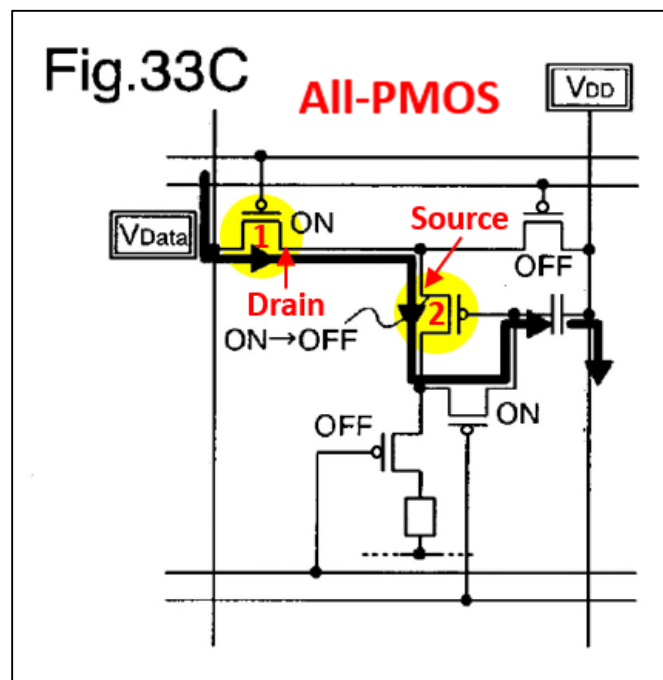
The preambles of claims 7 and 15 are identical and met for the same reasons.

- b. [15a]: “a first transistor including a gate to which a current scan signal is applied, and a source to which a data signal voltage is applied;”***

Claim element 15[a] is met as explained in claim 9 and claim element 7[a].

- c. [15b]: “a second transistor whose source is coupled to a drain of the first transistor;”***

Claim elements 15[b] and 7[a] both require “a second transistor,” but claim element 15[b] further requires that second transistor’s source “is coupled to the drain of the first transistor.” Fig. 33C shows this connection, with the source/drain labels confirmed by current flowing from higher to lower voltage. EX1003, ¶298-300.

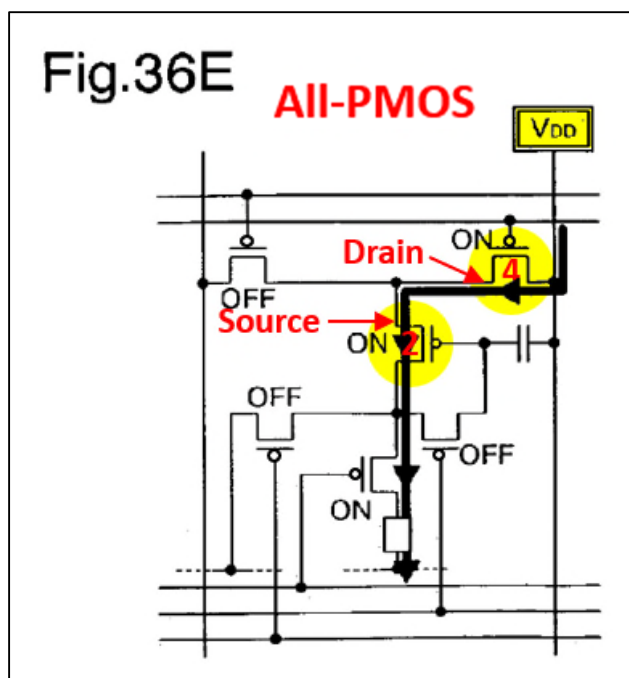


- d. [15c]: “a third transistor whose drain and source are connected between a gate and a drain of the second transistor;”***

The requirements of claim element 7[c] (“a third transistor...”) and claim 11 (including that “a drain and a source [of the third transistor] are coupled to the gate and the drain of the second transistor, respectively”) collectively include all requirements of claim element 15[c]. Accordingly, Kimura renders obvious claim element 15[c] for the same reasons as claim element 7[c] and claim 11. EX1003, ¶¶301-303.

- e. [15d]: “a fourth transistor including a gate to which a current light-emitting signal is applied, a source to which a power supply voltage is applied, and a drain coupled to the source of the second transistor;”*

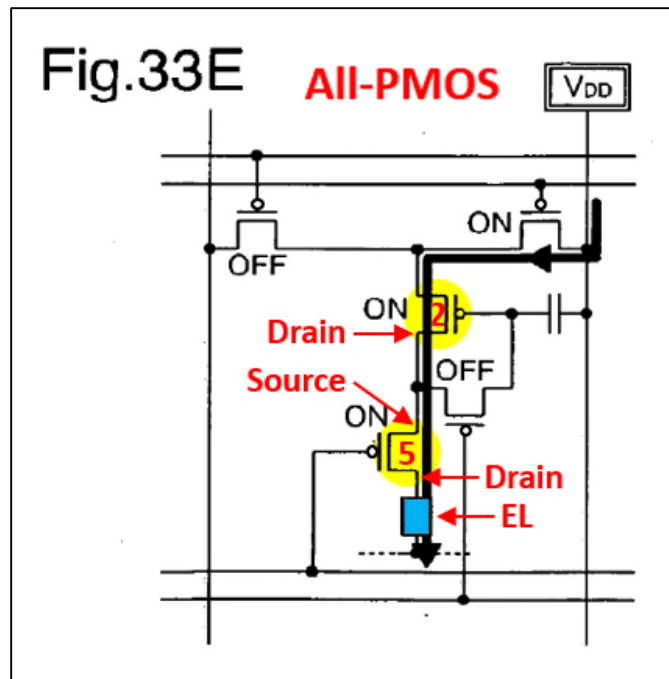
The only requirement of claim element 15[d] not in claim 13 is that the fourth transistor’s “drain [is] coupled to the source of the second transistor.” But Kimura Fig. 33E shows this, with the current flow arrows confirming the drain/source labels are correct. *See supra* §III.B; EX1003, ¶¶304-307. For this reason and the reasons explained for claim 13, Kimura renders claim element 15[d] obvious. *See also* analysis for claim elements 7[e] and 14[f] (discussing “fourth transistor”).



- f. [15e]: “a fifth transistor including a gate to which the current light-emitting signal is applied, a source coupled to the drain of the second transistor, and a drain coupled to one terminal of an electroluminescent element;”*

The only requirements of claim element 15[e] not in claim 13 and claim element 14[g] are that the fifth transistor’s source is coupled to **the drain** of the second transistor and that the fifth transistor’s drain is coupled to **one terminal** of the electroluminescent element. But both are shown below in Kimura Fig. 33E, with the current flow direction confirming the drain/source labels are correct.

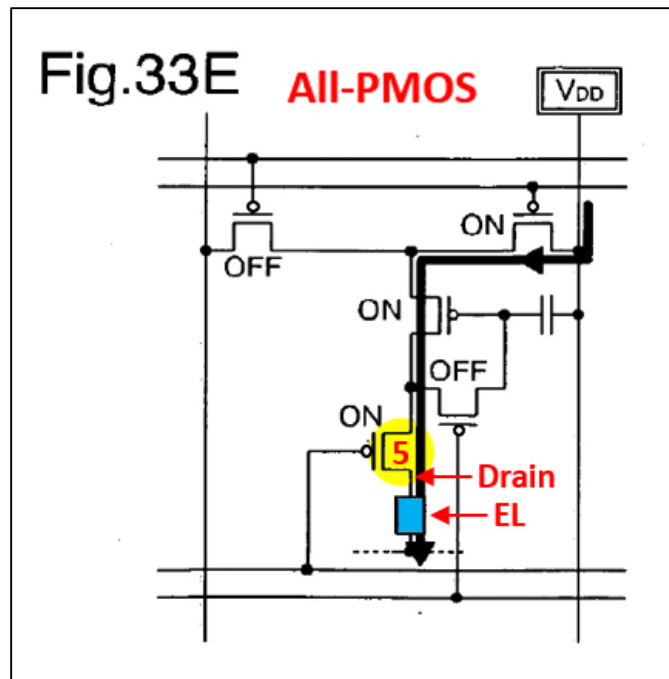
EX1003, ¶¶308-310. The electroluminescent element (EL) has two terminals, one of which is connected to the fifth transistor’s drain. EX1003, ¶¶308-310.



Thus, as just explained and for the reasons as claim 13 and claim element 14[g], Kimura renders obvious claim element 15[e].

- g. [15f]: “the electroluminescent element having the one terminal coupled to the drain of the fifth transistor and the other terminal grounded;”**

Kimura renders obvious claim element 15[f]. Fig. 33E below shows the electroluminescent element (in blue) coupled to the fifth transistor’s drain as confirmed by the current flow direction. EX1003, ¶¶311-314.

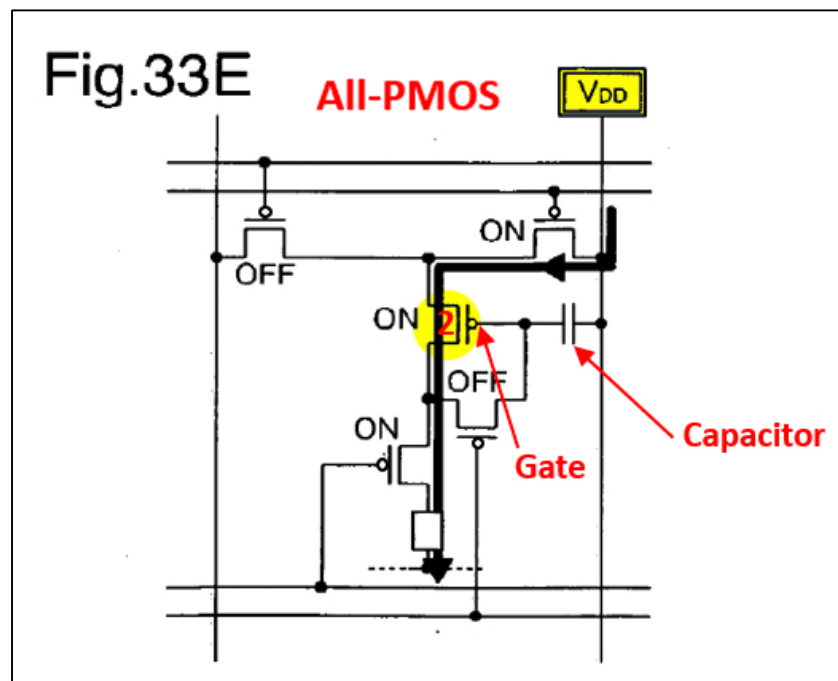


Although the electroluminescent element's other terminal is not expressly identified as connected to ground in Fig. 33, a POSITA would have found it obvious to do so. EX1003, ¶¶311-314. It was well-known to POSITAs in 2003 that a forward-bias current must be applied to an LED to emit light. Because of Kimura's circuit configuration (with positive voltage at the light-emitting terminal connected to the fifth transistor), the simplest and most-obvious choice for a POSITA would be to connect the other terminal to ground (*i.e.*, 0V). EX1003, ¶¶311-314. Such a solution very well-known in the art as shown by U.S. Pat. Pub. Nos 2001/0022565 (EX1006), 2003/0030603 (EX1007), and U.S. Pat. 6,229,506 (EX1012). Accordingly, Kimura renders obvious claim element 15[f]. *See also* analysis for claim elements 7[g] and 14[a] (analyzing "electroluminescent element") as well as claim elements 7[f], 14[g] and claim 13 (analyzing "fifth

transistor”).

- h. [15g]: “a capacitor in which one terminal of the capacitor is coupled to the gate of the second transistor and a power supply voltage is applied to the other terminal of the capacitor.”*

Kimura discloses claim element 15[g]. Fig. 33E below shows one capacitor terminal coupled to the second transistor’s gate and the other capacitor terminal connected the V_{DD} power supply. EX1003, ¶315-317.

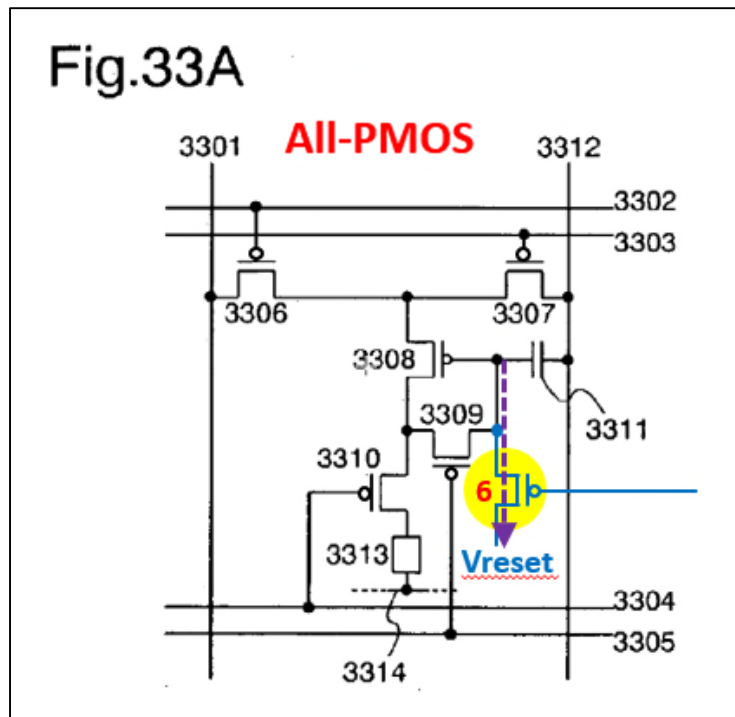


10. Claim 16

Claim 16 depends from claim 15 and further requires “a sixth transistor including a gate to which a scan signal just before the current scan signal is applied; a source coupled to the one terminal of the capacitor; and a drain to which an initialization voltage is applied.” Kimura renders claim 16 obvious for the

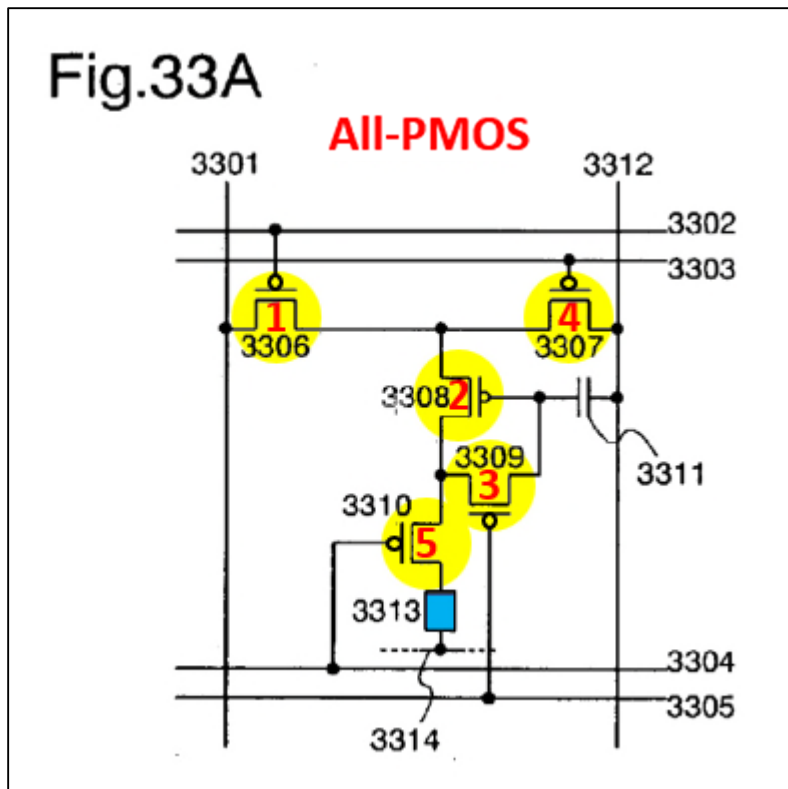
reasons below and as explained for claim 8. As a reminder, original Kimura Fig. 33 only has five transistors but modifying Fig. 33 in accordance with Figs. 16-17 by adding an initialization transistor supplies the missing “sixth transistor.” The purpose/operation of the initialization transistor (including controlling it with “a scan signal just before the current scan signal is applied”) in Kimura Figs. 16-17 is described for claim 8 *supra*. So, too, are the reasons for incorporating the initialization transistor into Fig. 33 and are not repeated here.

When the initialization transistor is added to Fig. 33A, the resulting circuit is shown below where the sixth transistor’s source is coupled to one capacitor terminal and its drain connects an “initialization voltage” (called “erase” voltage in Fig. 17A and “VReset” voltage in paragraph [0425]). The actual voltage used a merely a design choice. EX1003, ¶¶318-322. Thus, Kimura renders claim 16 obvious.



11. Claim 17

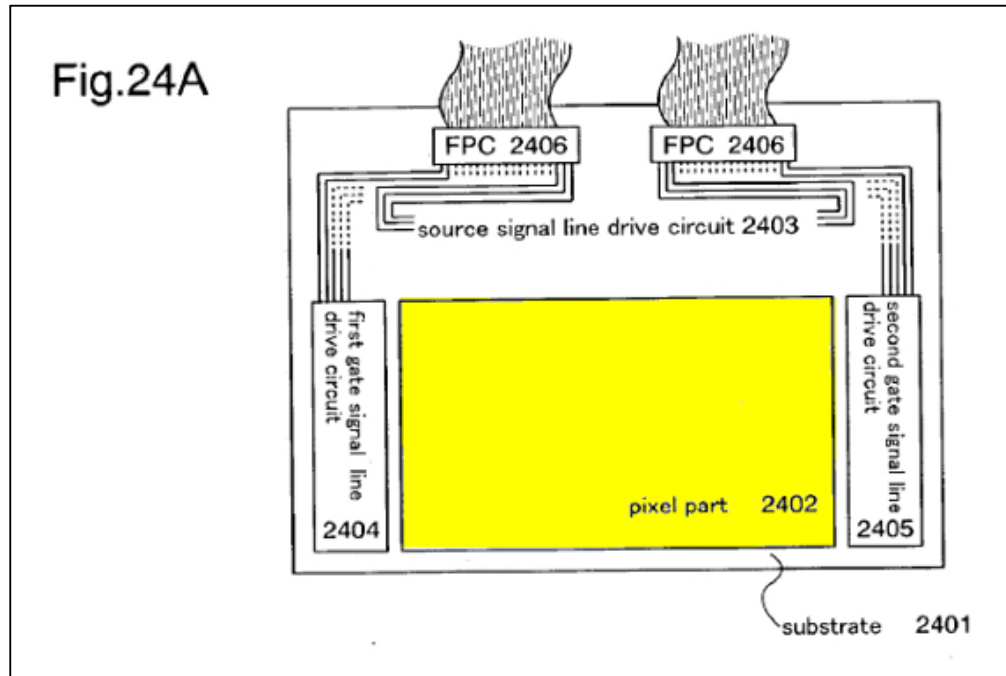
Kimura renders obvious independent claim 17 for substantially the same reasons as independent claims 7 and 15. Like those claims, independent claim 17 is an apparatus claim requiring five transistors (with same numbering as claims 7 and 15), a capacitor, and an electroluminescent element arranged in a particular manner. Like claim 15, the recited gate/drain/source connections mean all transistors in claim 17 are PMOS and much of the claim 17 patentability analysis is similar and/or identical to claim 15. For reference, the same all-PMOS version of Fig. 33 previously used is reproduced below.



- a. *[Claim 17 Preamble]: “A pixel circuit in an organic light emitting device having a plurality of data lines, a plurality of scan lines, a plurality of power lines, and a plurality of pixels each connected to one associated data line, scan line and power line of the plurality of data lines, scan lines and power lines, each pixel comprising:”*

To the extent limiting, Kimura discloses the preamble. Kimura discloses “[a] pixel circuit in an organic light emitting device” as discussed for claim 7 preamble. Kimura further discloses that its “light emitting device” is an “**active matrix**” with a plurality of pixels. EX1002, [0001]; *see also id.*, [0476] (“The device [includes] **a plurality of pixels [] arranged in a matrix** shape over a substrate.”); [0487] (same); [0401] (discussing “pixels within a screen”), and [0708] (OLED screens used in “video cameras, digital cameras,...notebook type

personal computers,...mobile telephones,...’)). For example, Fig. 24A illustrates a pixel matrix (in yellow). Kimura [0476].



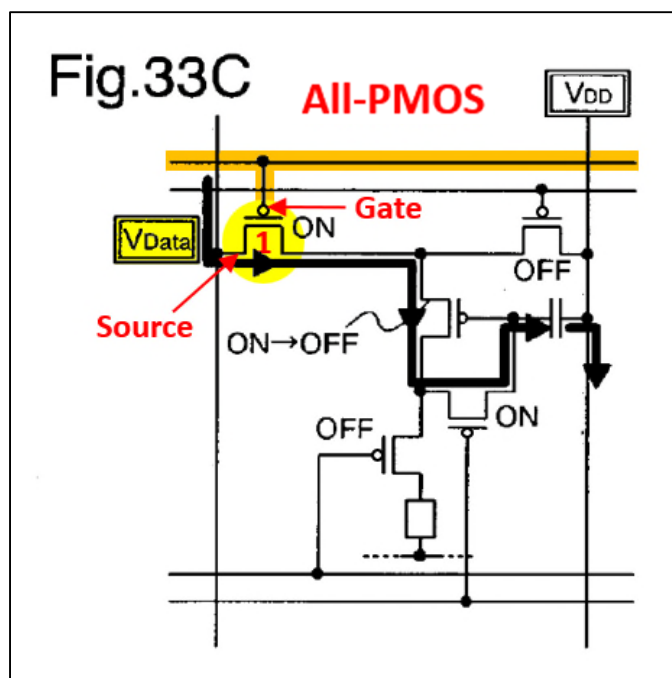
Circuits 2403, 2404, and 2405 drive the pluralities of “source signal line[s]” (the claimed “data lines”), “first gate signal line[s]” (the claimed “scan lines”), and “second gate signal line[s],” respectively, for the pixel matrix. Kimura [0476]; *see also id.*, Figs. 24-27 (illustrating control circuitry that provides signals to the pixels). Although not shown in Fig. 24, a POSITA would understand that the pixel matrix is supplied with power lines as illustrated throughout Kimura. EX1003, ¶331.

The pixels are organized into rows/lines controlled by common signals. *See, e.g.*, EX1002, Fig. 16B and [0422]-[0430] (discussing operation of pixel rows); EX1003, ¶332. Numerous Kimura figures show the signals connected to each

pixel in a row. For example, Fig. 17A shows a “Data” signal input (*i.e.*, “data line”), “VDD” connection (*i.e.*, power supply), and various control signals such as “Erase” and “Select” lines (*i.e.*, scan lines) for each row. *See also* EX1002, [0655] (discussing “V_{Data}” image signal on data line); [0656] (discussing V_{DD} power supply line); and [0659] (discussing “gate signal line[s]” (*i.e.*, the claimed “scan lines”) for controlling rows of pixels); EX1003, ¶¶329-333. Thus, Kimura discloses the claim 17 preamble.

b. [17a]: “a first transistor including a gate to which a current scan signal to be applied to the associated scan line is applied, and a source to which a data signal voltage from the data line is applied;”

The only language in claim element 17[a] not in claim element 15[a] is shown in bold: “a first transistor including a gate to which a current scan signal **to be applied to the associated scan line** is applied, and a source to which a data signal voltage **from the data line** is applied.” This additional language is trivial. In Kimura Fig. 33, the “data signal voltage” (V_{Data}) is supplied from the data line. EX1003, ¶335. This makes sense because the first transistor needs to provide V_{Data} to charge the capacitor as Fig. 33C shows. EX1003, ¶335. And, as previously explained, the “current scan signal” (Kimura’s first gate signal line) is applied to the scan line shown in orange. EX1003, ¶336. Accordingly, Kimura satisfies claim element 17[a].



- c. [17b]: “a second transistor whose source is coupled to a drain of the first transistor;”

Claim elements 17[b] and 15[b] are identical and met for the same reasons.

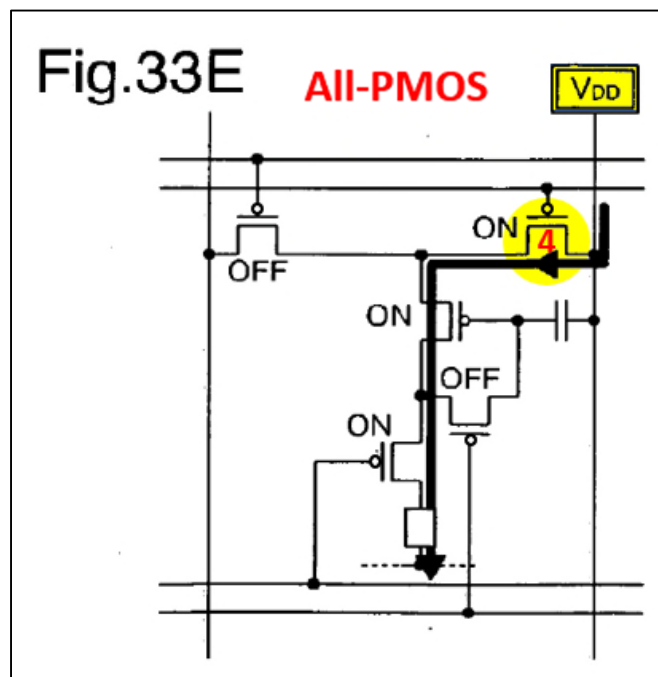
- d. [17c]: “a third transistor whose drain and source are connected between a gate and a drain of the second transistor, respectively;”

Claim element 17[c] and 15[c] are identical except claim element 17[c] adds the word “respectively.” But claim element 15[c] analysis reflects this and thus claim element 17[c] is satisfied as explained for claim element 15[c].

- e. [17d]: “a fourth emitting transistor including a gate to which a current light-emitting signal is applied, a source to which a power supply voltage from the power line is applied, and a drain coupled to the source of the second transistor;”

The only language in claim element 17[d] not in claim element 15[d] is shown in bold: “a fourth **emitting** transistor including a gate to which a current light-emitting signal is applied, a source to which a power supply voltage **from the power line** is applied, and a drain coupled to the source of the second transistor.”

The new language is addressed below while all other requirements are met as explained for claim element 15[d]. The fourth transistor is identified in Fig. 33E below, which shows current flow during light emission. EX1002, [0656]. The fourth transistor is an “emitting” transistor because it must be on (and is only on) during light emission when activated by the light emitting signal. EX1003, ¶344. Additionally, power supply voltage V_{DD} is supplied on a power supply line. EX1003, ¶345. Thus, Kimura satisfies claim element 17[d].



- f. [17e]: “a fifth transistor including a gate to which the current light-emitting signal is applied, and a source coupled to the drain of the second transistor;”***

Claim element 15[e] includes all the requirements of claim element 17[e] and is met for the same reasons.

- g. [17f]: “an electroluminescent element including one terminal coupled to the drain of the fifth transistor and the other terminal grounded;”***

Claim elements 17[f] and 15[f] are substantively identical and met for the same reasons.

- h. [17g]: “a capacitor including one terminal coupled to the gate of the second transistor, and the other terminal to which the power supply voltage from the power line is applied.”***

Claim element 15[g] includes all requirements of claim element 17[g], except that 17[g] additionally requires power supply voltage to come “from the power line.” This additional language is trivial and power supply voltage V_{DD} in Kimura Fig. 33 is plainly delivered “from the power line.” *See, e.g.*, EX1002, [0352] (discussing “electric current supply line”); EX1003, ¶351-352.

12. Claim 18

Claims 18 and 16 are substantially identical and met for the same reasons.

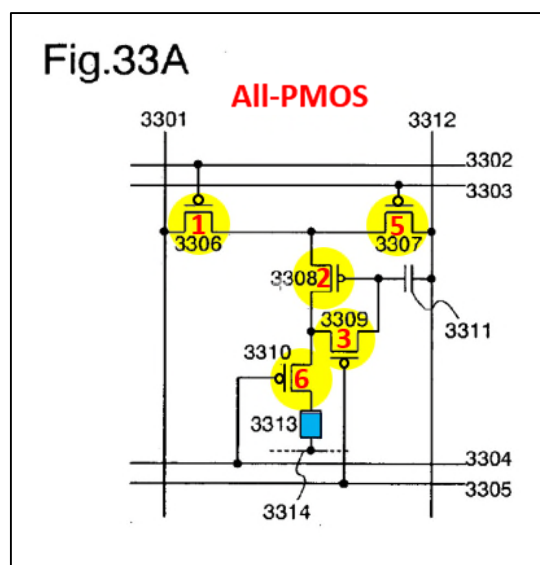
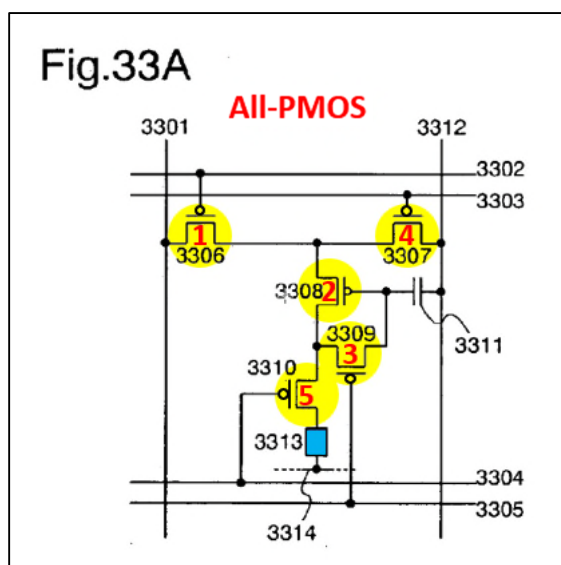
13. Claim 1

Kimura renders obvious independent claim 1 for substantially the same

reasons as independent claim 7. Like claim 7, claim 1 is an apparatus claim requiring five transistors, a capacitor, and an electroluminescent element arranged in a particular manner. The primary difference between claims 1 and 7 is that claim 1 numbers two transistors differently (highlighted below).

Claim 7	Claim 1
First transistor	First transistor
Second transistor	Second transistor
Third transistor	Third transistor
Fourth transistor	Fifth transistor
Fifth transistor	Sixth transistor

For reference, Kimura Fig. 33 transistor mappings are shown below for claims 7 and 1. The underlying circuits are identical and only the transistor numbers differ. The “Claim 1” version is used for analyzing claim 1.



CLAIM 7

CLAIM 1

- a. [Claim 1 Preamble]: “A pixel circuit in an organic light emitting device, comprising:”*

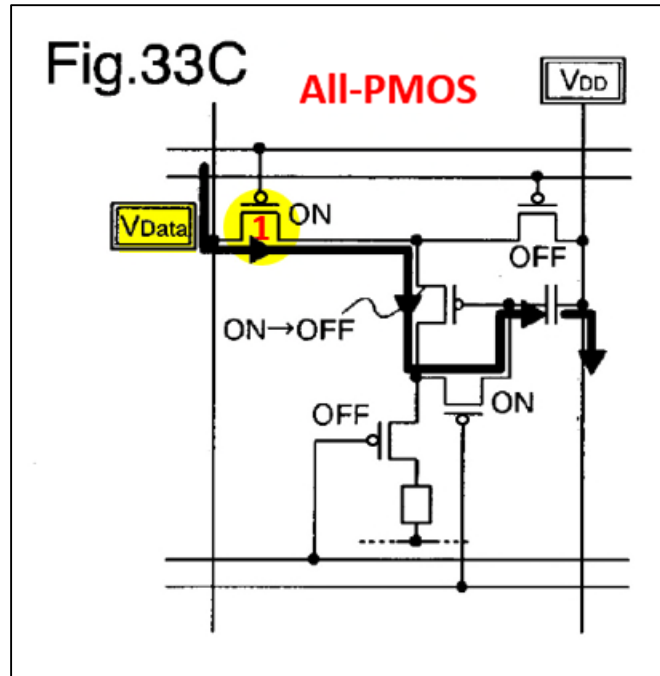
The preambles of claims 1 and 7 are identical and met for the same reasons.

- b. [1a]: “a first transistor for delivering a data signal voltage in response to a current scan line signal;”*

Claim elements 1[a] and 7[a] are identical and met for the same reasons.

- c. [1b]: “a second transistor for generating a driving current depending on the data signal voltage delivered through the first transistor;”*

Claim elements 7[b] and 1[b] both require a “second transistor for [] generating a driving current.” And a POSITA would understand that a driving current that “depend[s] on the data signal voltage delivered through the first transistor” (1[b]) is substantively the same as driving current generated “in response to a programmed data signal when light is emitted” (7[b]). EX1003, ¶¶371-374. In particular, the “data signal voltage” in claim element 1[b] is the same voltage used to store the “programmed data signal” on the capacitor that controls the drive current during light emission. See EX1002, Figs. 33C-E; EX1003, ¶¶371-374. And Fig. 33C below shows the V_{Data} voltage delivered through the first transistor en route to charging the capacitor. Thus, claim elements 7[b] and 1[b] are met for the same reasons.



- d. [1c]: “a third transistor for detecting and self-compensating threshold voltage deviation in the second transistor;”***

Claim element 1[c] is satisfied for the same reasons as claim elements 7[c] (“a third transistor for...”) and 7[h] (“the third transistor connects the second transistor in the form of a diode...so that the second transistor detects and compensates its threshold voltage deviation in itself”). EX1003, ¶¶375-377.

- e. [1d]: “a fifth transistor for providing a power supply voltage for the second transistor in response to a current light-emitting signal;”*

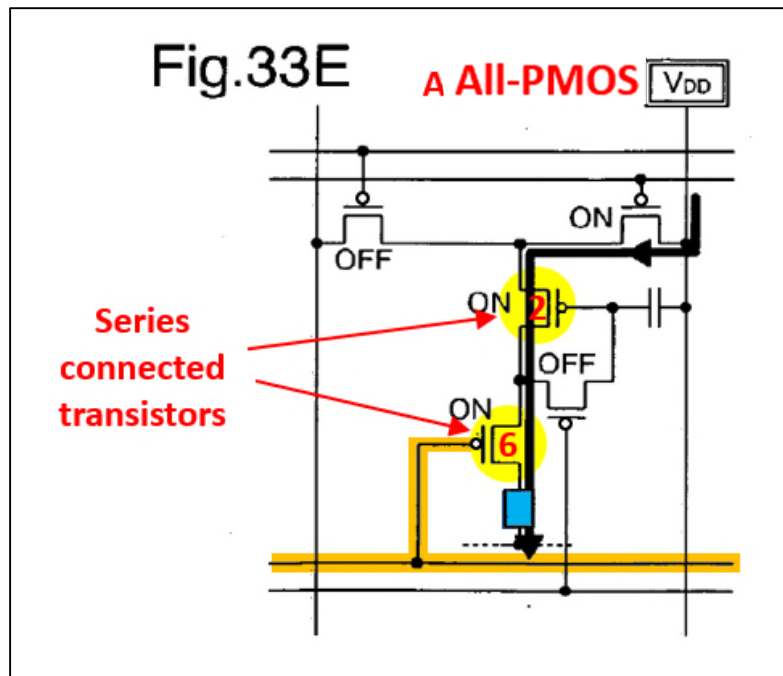
As noted previously, the “fifth” transistor in claim 1 corresponds to the “fourth” transistor in all other independent claims. *See supra* §IV.B. Apart from transistor numbering, claim elements 1[d] and 7[e] have only two other linguistic differences. But they are equally inconsequential. First, claim element 1[d] recites

“*providing* a power supply voltage” whereas 7[e] recites “*delivering* a power supply voltage,” but this does not impact the Kimura analysis. EX1003, ¶¶378-384. Second, claim element 1[d] requires that power is supplied “in response to a current light-emitting signal” whereas claim element 7[e] states that power is supplied “when the light is emitted.” Again, this is inconsequential. As explained previously, Kimura Fig. 33 emits light in response to the “current light-emitting signal.” *See supra* §VI.A. Accordingly, claim elements 1[d] and 7[e] are substantially similar and met for the same reasons.

f. [1e]: “a sixth transistor which is coupled in series between the second transistor and an electroluminescent element and for providing the driving current for the electroluminescent element through the second transistor in response to the current light-emitting signal;”

The “sixth transistor” in claim element 1[e] corresponds to the “fifth transistor” in claim element 7[f]. *See supra* §IV.B. Although similar in several respects, the claim language differs enough that claim element 1[e] is fully analyzed here.

Kimura discloses “a sixth transistor which is coupled in series between the second transistor and an electroluminescent element.” Kimura’s “**sixth transistor**” in Fig. 33E below is connected in series between the second transistor and the electroluminescent element (in blue).



Kimura also discloses that the sixth transistor “provid[es] the driving current for the electroluminescent element through the second transistor in response to the current light-emitting signal.” In Fig. 33E above, the black arrow indicates current flow. *See* EX1002, [0656]. The sixth transistor provides the driving current to the electroluminescent element because it is the only transistor connected to the electroluminescent element. And it would have been obvious to a POSITA to use an active-low version of the timing/signal scheme illustrated in Fig. 16B to control the fifth and sixth transistors. EX1003, ¶389 and ¶57; *see also* EX1002, Fig. 36 (showing common operational states for fourth and sixth transistors), [0668] (disclosing use of shared control signal lines). Thus, the orange signal line provides the current light-emitting signal (called “second gate signal” in Kimura) to the sixth transistor’s gate. EX1003, ¶389. Accordingly, “in response to the

current light-emitting signal” (*i.e.*, when it activates the sixth transistor) the sixth transistor “provid[es] the driving current” (through series-connected second transistor) to the electroluminescent element. *See* EX1002, [0656]; EX1003, ¶¶385-391. In this manner Kimura satisfies claim element 1[e].

g. [1f]: “a capacitor for storing the data signal voltage delivered to the second transistor”

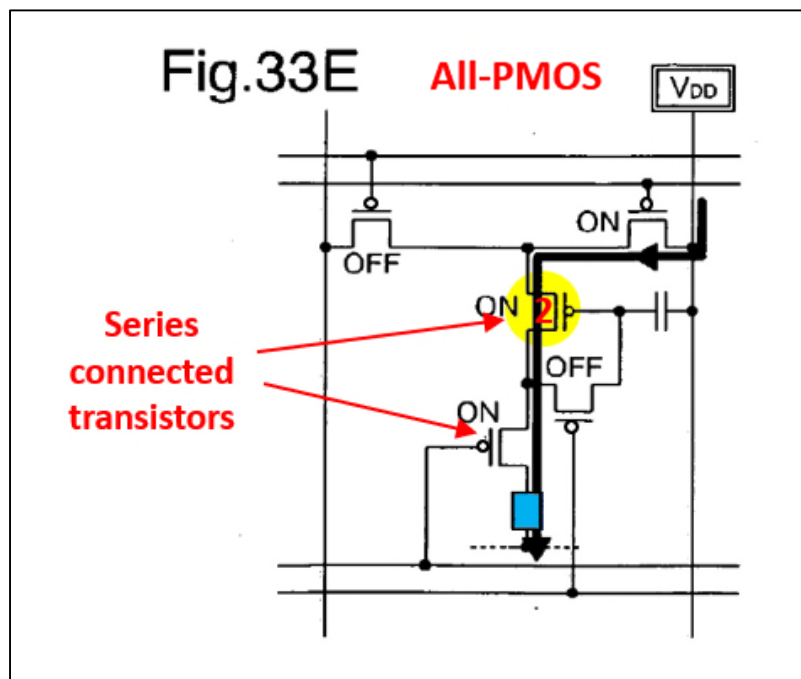
Claim elements 1[f] and 7[d] are the same, except that claim element 1[f] recites “***storing*** the data signal voltage ***delivered to*** the second transistor” instead of “***maintaining*** the data signal voltage ***programmed onto*** the second transistor” (7[d]). But these minor linguistic differences do not substantively affect the Kimura analysis and claim element 1[f] is satisfied as explained for claim element 7[d]. EX1003, ¶¶392-396.

h. [1g]: “wherein the electroluminescent element emits light corresponding to the driving current generated through the second transistor.”

Claim elements 1[g] and 7[g] are the same, except that claim element 1[g] refers to a driving current “generated through the second transistor” and claim element 7[g] refers to a driving current “delivered through the fifth¹¹ transistor.” However, Kimura Fig. 33 meets both requirements because the two transistors are

¹¹ Claim 7’s “fifth transistor” is claim 1’s “sixth transistor.”

in series and the electroluminescent element emits light when both are on, as shown below in Fig. 33E. EX1003, ¶¶397-400. The amount of light emitted is a function of the driving current and thus “correspond[s] to” the driving current. *See, e.g.*, EX1002, [0359] (brightness levels vary according to driving current); EX1003, ¶398. As summarized here, and explained further at claim element 7[g], Kimura satisfies claim element 1[g].



14. Claim 2

Except that “fourth transistor” in claim 2 is called “sixth transistor” in claim 8, the claims are substantially similar and met for the same reasons.

15. Claims 3-5

Claims 3-5 are identical to claims 9-11 respectively, and met for the same

reasons.

16. Claim 6

All limitations of claim 6 are present in claim 12 and Kimura satisfies claim 6 for the same reasons.

C. Secondary Considerations of Non-Obviousness

Petitioner is unaware of any applicable secondary considerations of non-obviousness. None were identified during prosecution. *See generally* EX1005. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

VII. DISCRETIONARY DENIAL IS NOT WARRANTED

Discretionary denial under 35 U.S.C. §314(a) is not warranted. There is no co-pending district court case and the Director has instructed that the Board “will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.” Director Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, at 7 (June 21, 2022); *see also* Federal Register, Vol. 88, No. 77 (Apr. 21, 2023) at 24514 (“[I]t is the current practice of the USPTO not to deny institution of an IPR or PGR petition based on parallel proceedings in the ITC.”). Thus, no basis exists to discretionarily deny institution under §314(a).

VIII. MANDATORY NOTICES

A. Real Party-in-Interest

Mianyang BOE Optoelectronics Technology Co., Ltd. (BOE”); Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd.; Tianma Microelectronics Co. Ltd.; and Visionox Technology, Inc. and their subsidiaries are the real parties-in-interest.

B. Related Proceedings

No previous IPR or post-grant proceeding has been filed challenging the ’599 patent. The ’599 patent has been asserted by Samsung in the following ITC action: *Certain Active Matrix Organic Light-Emitting Diode Display Panels And Modules For Mobile Devices, And Components Thereof*; Inv. No. 337-TA-1351 (Violation) ITC-337-TA-1351. In addition to the ’599 patent, the ITC action asserts U.S. Patent Nos. 9,330,593; 9,818,803; 10,854,683; and 11,594,578. Petitioner BOE has intervened as a respondent in the ITC action.

C. Counsel Information

Petitioner designates the following counsel:

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D. Electronic Service

Petitioner consents to email service at the email addresses above.

IX. FEES

The required fee is being paid electronically through P-TACTS.

X. CONCLUSION

Petitioner respectfully requests institution and a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

Dated: June 9, 2023

/Travis Jensen/

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing Petition with the word count limits set forth in 37 C.F.R. §42.24(a)(1)(i). Excluding the parts of the Petition exempted by 37 C.F.R. §42.24(a)(1), this Petition contains 13,997 words as determined using the word count feature in Microsoft Word, which was used to prepare this Petition.

CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on June 9, 2023 via overnight courier on the Patent Owner at the correspondence address of record for U.S. Patent No. 7,414,599:

23363 - Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

Courtesy copies were also served via email on Patent Owner's counsel of record in a related ITC investigation styled Certain Active Matrix Organic Light-Emitting Diode Display Panels And Modules For Mobile Devices, And Components Thereof; Inv. No. 337-TA-1351 (Violation) ITC-337-TA-1351):

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Dated: June 9, 2023

By: /Travis Jensen/